product data handbook

UNITRODE

The Linear IC Company Everyone Follows

Unitrode's reputation and success as an innovator is evidenced by the strong market acceptance to the products described in this book. The Company has achieved significant technological breakthroughs in all areas of power management, motion control, and high speed data communication ICs.

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LIFE SUPPORT POLICY

Unitrode's products are not authorized for use as critical components in the life support devices or systems without express written approval.

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Unitrode Corporation is a world leader in the design and manufacture of innovative, high performance linear and mixed signal ICs. This catalog will introduce you to our products for commercial, industrial and mil/aero applications.

With a focus on power management, motion control and high speed data communications, our product portfolio includes:

- Off-line Power Management
- DC/DC Power Management
- Protection/Supervisory Circuits
- Portable Power Management
- Motion/Motor Controls
- High Speed Interface

Unitrode also offers an assortment of special function ICs including fiber to curb ringers, CAN transceivers, IrDA transceivers, cellular power management products and pager/PDA power controllers.

All our products are backed by a design and applications team that really understands how our ICs interact with the rest of your system/subsystem. We take special pride in the intelligence of our designs and their ability to anticipate as well as respond to customer needs.

Whatever your applications – Power Management, Motion Control or Ultrafast Data Communications – we are an innovative, dependable and customer-driven source for catalog, semi-custom and custom linear/mixed signal ICs.

Around The World Service

Unitrode serves its customers around the world from:

- its design centers in New Hampshire, California and North Carolina;
- its extensive test, assembly subcontractor coordination, and customer service facility in Singapore;
- and from our network of manufacturers' representatives and distributors.

Process Capabilities

Unitrode's bipolar process, optimized for both precision analog and power functions, is constantly updated to incorporate leading edge process options such as:

- operating voltage ranges from 4 to 65 volts;
- Schottky and integrated injection logic;
- ion implant;
- thin film resistors for high accuracy;
- double-level metallization for high density, high current layouts;
- and buried zener reference.

Its BiCMOS process is ideal for high density linear and mixed mode designs, especially where speed and low power consumption are of primary importance.

Options include:

- 3, 2.5, and 1 micron processes;
- up to 15V operation;
- high current, double level metallization;
- fully isolated, vertical NPN transistors;
- and thin film resistors

This year, there is a new BCDMOS process. It offers all the options available with BiCMOS, plus a lateral DMOS device with up to 35V operation for added power handling capability.

An ISO9001 and 9002 Firm

Unitrode was one of the first U.S. electronics companies to achieve IS/ISO 9001/EN29001 registration.

In order to be registered, the Company had to pass a rigorous examination of its quality systems – from product design through shipment. The registration thus assures customers all over the world that the Company is adhering to very high, precisely defined standards.

Listening To Customers

In the development of custom and semi-custom parts, Unitrode design engineers work very closely with customers. This close cooperation assures that all requirements are accurately understood, that all possibilities are fully explored, and that the resulting products meet and exceed specified needs.

Unitrode also pays careful attention to customers and markets to help guide its development of catalog parts. Continuing close contact makes it possible to anticipate industry requirements, and to create devices that will satisfy them.

A Resource You Can Count On

Unitrode Corporation has earned its reputation for excellence in computer, Communications, Industrial, Commercial, Automotive and Mil/Aero markets. It is totally committed to continuing excellence in everything it does.

With products and services that are among the most innovative in the industry, with proven quality and reliability, and with superb design engineering and the industry's best applications technical support, Unitrode is a resource you can depend on.

This book describes Unitrode's linear and mixed signal IC solutions in detail. Ideally, it will stimulate your interest to request further information, request product samples and/or to check for available evaluation boards.

For additional information on devices offered in this catalog, or if you need a customized product, please contact Unitrode Marketing at 603-429-8725. You may also consult our website for current information about Unitrode and its products at http://www.unitrode.com.

INDEX

1 ..... Part Number Index 1

2 ..... General Information 2

3 ..... General Power Supply 3

4 ..... Linear Regulators 4

5 ..... PFC Controllers 5

6 ..... Interface/SCSI Circuits 6

7 ..... Power Drivers 7

8 ..... Portable Products 8

9 ..... Hot Swap Power Managers 9

10 ..... Intelligent Motion Circuits 10

11 ..... Military/Aerospace Products 11

12 ..... Packaging Information 12

13 ..... Sales Offices 13

1. *Part Number Index* 1-1

2. *General Information*

- About this Databook 2-1
- Ordering Information 2-2
- Quality 2-3
- New Products 2-9
- Die and Wafers 2-12

3. *General Power Supply*

- Selection Guides 3-1
- Data Sheets 3-17

4. *Linear Regulators*

- Selection Guides 4-1
- Data Sheets 4-3

5. *PFC Controllers*

- Selection Guides 5-1
- Data Sheets 5-3

6. *Interface/SCSI Circuits*

- Selection Guides 6-1
- Data Sheets 6-5

7. *Power Drivers*

- Selection Guides 7-1
- Data Sheets 7-3

8. *Portable Products*

- Selection Guides 8-1
- Data Sheets 8-5

9. *Hot Swap Power Managers*

- Selection Guides 9-1
- Data Sheets 9-3

10. *Intelligent Motion*

- Selection Guides 10-1
- Data Sheets 10-3

11. *Military/Aerospace Products*

- Capabilities 11-2
- Standardized Military Drawings (SMDs) 11-3

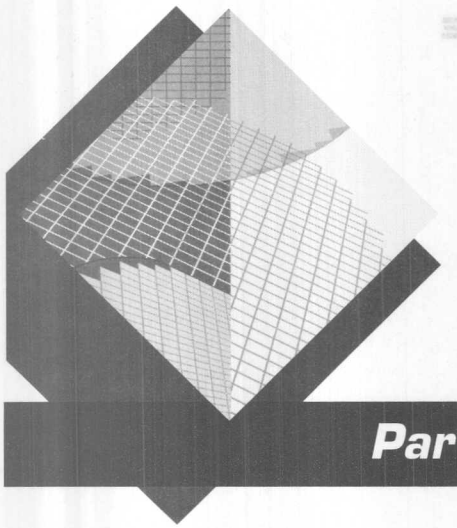
12. *Packaging Information*

- Index 12-1
- Device Temperature Management 12-3
- Thermal Characteristics of Surface Mount Packages 12-7
- Mechanical Drawings 12-12

13. *Sales Offices*

- Domestic Representatives 13-1
- Domestic Distributors 13-8
- International Agents - Distributors 13-10


UNITRODE



Part Number Index

1

UNITRODE

Part Number Index

1

Part Number Index

PAGE	PART #	DESCRIPTION
10-43	UC1517	Stepper Motor Drive Circuit
3-41	UC1524	Advanced Regulating PWM
3-46	UC1524A	Advanced Regulating PWM
3-52	UC1525A	Regulating PWM
3-59	UC1525B	Regulating PWM
3-66	UC1526	Regulating PWM
3-73	UC1526A	Regulating PWM
3-52	UC1527A	Regulating PWM
3-59	UC1527B	Regulating PWM
3-81	UC1543	Power Supply Supervisory Circuit
3-81	UC1544	Power Supply Supervisory Circuit
3-86	UC1548	Primary Side PWM Controller
3-94	UCC1570	Low Power PWM
3-101	UC1572	Negative Output Flyback PWM
3-105	UC1573	Buck PWM Stepdown Voltage Regulator
3-114	UCC1580-1	Single Ended Active Clamp/Reset PWM
3-114	UCC1580-2	Single Ended Active Clamp/Reset PWM
3-114	UCC1580-3	Single Ended Active Clamp/Reset PWM
3-114	UCC1580-4	Single Ended Active Clamp/Reset PWM
3-122	UCC1581	Micropower Voltage Mode PWM
3-129	UCC1582	High Efficiency Synchronous, Step Down Controller
3-133	UCC1583	Switch Mode Secondary Side Post Regulator
3-141	UC1584	Secondary Side Synchronous Post Regulator
3-146	UC1610	Dual Schottky Diode Bridge
3-148	UC1611	Quad Schottky Diode Array
3-151	UC1612	Dual Schottky Diode
3-17	UC161A	Micropower Quad Comparator
3-17	UC161B	Micropower Quad Comparator
3-17	UC161C	Micropower Quad Comparator
10-50	UC1620	Switchmode Driver for 3-Ø Brushless DC Motors
10-56	UC1625	Brushless DC Motor Controller
10-68	UC1633	Phase Locked Frequency Controller
10-75	UC1634	Phase Locked Frequency Controller
10-79	UC1635	Phase Locked Frequency Controller
10-83	UC1637	Switched Mode Controller for DC Motor Drive
10-89	UC1638	Advanced PWM Motor Controller
7-5	UC1702	Quad PWM Relay Driver
7-13	UC1705	High Speed Power Driver
7-16	UC1706	Dual Output Driver
7-21	UC1707	Dual Channel Power Driver
7-27	UC1708	Dual Non-Inverting Power Driver
7-31	UC1709	Dual High-Speed FET Driver
7-34	UC1710	High Current FET Driver
7-37	UC1711	Dual Ultra High-Speed FET Driver
7-39	UC17131	Smart Power Switch
7-39	UC17132	Smart Power Switch
7-44	UC1714	Complementary Switch FET Driver
7-44	UC1715	Complementary Switch FET Driver
10-97	UC1717	Stepper Motor Drive Circuit
7-51	UC1724	Isolated Drive Transmitter
7-54	UC1725	Isolated High Side FET Driver
7-58	UC1726	Isolated Drive Transmitter
7-63	UC1727	Isolated High Side IGBT Driver
3-153	UC1730	Thermal Monitor
7-69	UCC1776	Quad FET Driver
3-167	UCC1800	Low-Power BiCMOS Current-Mode PWM
3-167	UCC1801	Low-Power BiCMOS Current-Mode PWM
3-167	UCC1802	Low-Power BiCMOS Current-Mode PWM
3-167	UCC1803	Low-Power BiCMOS Current-Mode PWM
3-167	UCC1804	Low-Power BiCMOS Current-Mode PWM
3-167	UCC1805	Low-Power BiCMOS Current-Mode PWM
3-174	UCC1806	Low Power, Dual Output, Current Mode PWM Controller
3-180	UCC1807-1	Programmable Maximum Duty Cycle PWM Controller
3-180	UCC1807-2	Programmable Maximum Duty Cycle PWM Controller
3-180	UCC1807-3	Programmable Maximum Duty Cycle PWM Controller
3-185	UCC1808-1	Low Power Current Mode Push-Pull PWM
3-185	UCC1808-2	Low Power Current Mode Push-Pull PWM
3-189	UCC1809-1	Economy Primary Side Controller
3-189	UCC1809-2	Economy Primary Side Controller
3-192	UCC1810	Dual Channel Synchronized Current Mode PWM
3-199	UCC1812	12V Boost Regulator
4-7	UC182-1	Fast LDO Linear Regulator
4-7	UC182-2	Fast LDO Linear Regulator
4-7	UC182-3	Fast LDO Linear Regulator
4-7	UC182-ADJ	Fast LDO Linear Regulator
3-209	UC1823	High Speed PWM Controller
3-215	UC1823A	High Speed PWM Controller
3-215	UC1823B	High Speed PWM Controller
3-223	UC1824	High Speed PWM Controller
3-230	UC1825	High Speed PWM Controller
3-215	UC1825A	High Speed PWM Controller
3-215	UC1825B	High Speed PWM Controller
3-237	UC1826	Secondary Side Average Current Mode Controller

Part Number Index (cont'd)

PAGE	PART #	DESCRIPTION
3-247	UC1827-1	Buck Current/Voltage Fed Push-Pull PWM Controller
3-247	UC1827-2	Buck Current/Voltage Fed Push-Pull PWM Controller
3-252	UCC1829-1	High Speed PWM Controller
3-252	UCC1829-2	High Speed PWM Controller
4-20	UC1832	Precision Low Dropout Linear Controller
4-20	UC1833	Precision Low Dropout Linear Controller
4-27	UC1834	High Efficiency Linear Regulator
4-33	UC1835	High Efficiency Regulator Controller
4-33	UC1836	High Efficiency Regulator Controller
4-37	UCC1837	8-Pin N-FET Linear Regulator Controller
3-265	UC1838A	Magnetic Amplifier Controller
3-269	UCC1839	Secondary Side Average Current Mode Controller
*	UC1840	Programmable, Off-Line, PWM Controller
3-274	UC1841	Programmable, Off-Line, PWM Controller
3-282	UC1842	Current Mode PWM Controller
3-289	UC1842A	Current Mode PWM Controller
3-282	UC1843	Current Mode PWM Controller
3-289	UC1843A	Current Mode PWM Controller
3-282	UC1844	Current Mode PWM Controller
3-289	UC1844A	Current Mode PWM Controller
3-282	UC1845	Current Mode PWM Controller
3-289	UC1845A	Current Mode PWM Controller
3-295	UC1846	Current Mode PWM Controller
3-295	UC1847	Current Mode PWM Controller
3-302	UC1848	Average Current Mode PWM Controller
3-310	UC1849	Secondary Side Average Current Mode Controller
4-49	UC185-1	Fast LDO Linear Regulator
4-49	UC185-2	Fast LDO Linear Regulator
4-49	UC185-3	Fast LDO Linear Regulator
4-49	UC185-ADJ	Fast LDO Linear Regulator
3-320	UC1851	Programmable, Off-Line, PWM Controller
5-3	UC1852	High Power-Factor Preregulator
5-8	UC1853	High Power Factor Preregulator
5-12	UC1854	High Power Factor Preregulator
5-20	UC1854A	Enhanced High Power Factor Preregulator
5-20	UC1854B	Enhanced High Power Factor Preregulator
5-26	UC1855A	High Performance Power Factor Preregulator
5-26	UC1855B	High Performance Power Factor Preregulator

PAGE	PART #	DESCRIPTION
3-326	UC1856	Improved Current Mode PWM Controller
5-34	UCC1857	Isolated Boost PFC Preregulator Controller
5-39	UCC1858	High Efficiency, High Power Factor Preregulator
3-334	UC1860	Resonant Mode Power Supply Controller
3-342	UC1861	Resonant-Mode Power Supply Controller
3-342	UC1862	Resonant-Mode Power Supply Controller
3-342	UC1863	Resonant-Mode Power Supply Controller
3-342	UC1864	Resonant-Mode Power Supply Controller
3-342	UC1865	Resonant-Mode Power Supply Controller
3-342	UC1866	Resonant-Mode Power Supply Controller
3-342	UC1867	Resonant-Mode Power Supply Controller
3-342	UC1868	Resonant-Mode Power Supply Controller
3-348	UC1870-1	High Efficiency, Synchronous, Step-down (Buck) Controller
3-348	UC1870-2	High Efficiency, Synchronous, Step-down (Buck) Controller
8-5	UC1871	Resonant Fluorescent Lamp Driver
8-10	UC1872	Resonant Lamp Ballast Controller
3-355	UC1874-1	High Efficiency, Synchronous, Step-down (Buck) Controller
3-355	UC1874-2	High Efficiency, Synchronous, Step-down (Buck) Controller
3-363	UC1875	Phase Shift Resonant Controller
3-363	UC1876	Phase Shift Resonant Controller
3-363	UC1877	Phase Shift Resonant Controller
3-363	UC1878	Phase Shift Resonant Controller
3-385	UCC1881-1	High Performance Average Current Mode PWM
3-385	UCC1881-2	High Performance Average Current Mode PWM
3-385	UCC1881-3	High Performance Average Current Mode PWM
3-385	UCC1881-4	High Performance Average Current Mode PWM
3-385	UCC1881-5	High Performance Average Current Mode PWM
3-385	UCC1881-6	High Performance Average Current Mode PWM
3-398	UCC1883	Micropower Peak Current Mode Controller
3-407	UCC1884	Frequency Foldback Current Mode PWM Controller
3-414	UCC1885	Micropower Secondary Regulation IC

** Consult Factory*

Part Number Index (cont'd)

PAGE	PART #	DESCRIPTION
3-422	UC1886	Average Current Mode PWM Controller IC
3-429	UCC1888	Off-line Power Supply Controller
3-434	UCC1889	Off-line Power Supply Controller
3-440	UCC1890	Off-Line Battery Charger Circuit
3-447	UC1901	Isolated Feedback Generator
3-452	UC1902	Load Share Controller
3-457	UC1903	Quad Supply and Line Monitor
3-464	UC1904	Precision Quad Supply and Line Monitor
3-469	UC1907	Load Share Controller
3-475	UC1908	Programmable Voltage Clamp
3-482	UC1910	4-Bit DAC and Voltage Monitor
9-8	UCC1913	Negative Voltage Hot Swap Power Manager
9-14	UC1914	5V to 35V Hot Swap Power Manager
9-34	UCC1917	Positive Floating Hot Swap Power Manager
9-48	UCC1919	3V to 8V Hot Swap Power Manager
9-63	UCC1921	Latchable Negative Floating Hot Swap Power Manager
3-487	UC19431	Precision Adjustable Shunt Regulator
3-492	UC19432	Precision Analog Controller
8-50	UCC1946	Microprocessor Supervisor with Watchdog Timer
3-496	UC1965	Precision Reference with Low Offset Error Amplifier
3-33	UCC2305	HID Lamp Controller
3-41	UC2524	Advanced Regulating PWM
3-46	UC2524A	Advanced Regulating PWM
3-52	UC2525A	Regulating PWM
3-59	UC2525B	Regulating PWM
3-66	UC2526	Regulating PWM
3-73	UC2526A	Regulating PWM
3-52	UC2527A	Regulating PWM
3-59	UC2527B	Regulating PWM
3-81	UC2543	Power Supply Supervisory Circuit
3-81	UC2544	Power Supply Supervisory Circuit
3-86	UC2548	Primary Side PWM Controller
3-94	UCC2570	Low Power PWM
3-101	UC2572	Negative Output Flyback PWM
3-105	UC2573	Buck PWM Stepdown Voltage Regulator
3-21	UC2577-12	Simple Step-Up Fixed Voltage Regulators
3-21	UC2577-15	Simple Step-Up Fixed Voltage Regulators
3-26	UC2577-ADJ	Simple Step-Up Voltage Regulator
3-109	UC2578	Buck PWM Stepdown Voltage Regulator
3-114	UCC2580-1	Single Ended Active Clamp/Reset PWM
3-114	UCC2580-2	Single Ended Active Clamp/Reset PWM
3-114	UCC2580-3	Single Ended Active Clamp/Reset PWM
3-114	UCC2580-4	Single Ended Active Clamp/Reset PWM
3-122	UCC2581	Micropower Voltage Mode PWM
3-129	UCC2582	High Efficiency Synchronous, Step Down Controller
3-133	UCC2583	Switch Mode Secondary Side Post Regulator
3-141	UC2584	Secondary Side Synchronous Post Regulator
3-146	UC2610	Dual Schottky Diode Bridge
10-68	UC2633	Phase Locked Frequency Controller
10-75	UC2634	Phase Locked Frequency Controller
10-79	UC2635	Phase Locked Frequency Controller
10-83	UC2637	Switched Mode Controller for DC Motor Drive
10-89	UC2638	Advanced PWM Motor Controller
7-5	UC2702	Quad PWM Relay Driver
7-13	UC2705	High Speed Power Driver
7-16	UC2706	Dual Output Driver
7-21	UC2707	Dual Channel Power Driver
7-27	UC2708	Dual Non-Inverting Power Driver
7-31	UC2709	Dual High-Speed FET Driver
7-39	UC27131	Smart Power Switch
7-39	UC27132	Smart Power Switch
7-44	UC2714	Complementary Switch FET Driver
7-44	UC2715	Complementary Switch FET Driver
10-97	UC2717	Stepper Motor Drive Circuit
7-51	UC2724	Isolated Drive Transmitter
7-54	UC2725	Isolated High Side FET Driver
7-58	UC2726	Isolated Drive Transmitter
7-63	UC2727	Isolated High Side IGBT Driver
3-153	UC2730	Thermal Monitor
3-157	UCC2750	Source Ringer Controller
3-166	UCC2751	Single Line Ring Generator Controller
7-69	UCC2776	Quad FET Driver
3-167	UCC2800	Low-Power BiCMOS Current-Mode PWM
3-167	UCC2801	Low-Power BiCMOS Current-Mode PWM
3-167	UCC2802	Low-Power BiCMOS Current-Mode PWM
3-167	UCC2803	Low-Power BiCMOS Current-Mode PWM
3-167	UCC2804	Low-Power BiCMOS Current-Mode PWM
3-167	UCC2805	Low-Power BiCMOS Current-Mode PWM

Part Number Index (cont'd)

PAGE	PART #	DESCRIPTION
3-174	UCC2806	Low Power, Dual Output, Current Mode PWM Controller
3-180	UCC2807-1	Programmable Maximum Duty Cycle PWM Controller
3-180	UCC2807-2	Programmable Maximum Duty Cycle PWM Controller
3-180	UCC2807-3	Programmable Maximum Duty Cycle PWM Controller
3-185	UCC2808-1	Low Power Current Mode Push-Pull PWM
3-185	UCC2808-2	Low Power Current Mode Push-Pull PWM
3-189	UCC2809-1	Economy Primary Side Controller
3-189	UCC2809-2	Economy Primary Side Controller
4-3	UCC281-3	Low Dropout 1 Ampere Linear Regulator
4-3	UCC281-5	Low Dropout 1 Ampere Linear Regulator
4-3	UCC281-ADJ	Low Dropout 1 Ampere Linear Regulator
3-192	UCC2810	Dual Channel Synchronized Current Mode PWM
3-199	UCC2812	12V Boost Regulator
3-202	UCC2813-0	Low Power Economy BiCMOS Current Mode PWM
3-202	UCC2813-1	Low Power Economy BiCMOS Current Mode PWM
3-202	UCC2813-2	Low Power Economy BiCMOS Current Mode PWM
3-202	UCC2813-3	Low Power Economy BiCMOS Current Mode PWM
3-202	UCC2813-4	Low Power Economy BiCMOS Current Mode PWM
3-202	UCC2813-5	Low Power Economy BiCMOS Current Mode PWM
4-7	UC282-1	Fast LDO Linear Regulator
4-7	UC282-2	Fast LDO Linear Regulator
4-7	UC282-3	Fast LDO Linear Regulator
4-7	UC282-ADJ	Fast LDO Linear Regulator
3-209	UC2823	High Speed PWM Controller
3-215	UC2823A	High Speed PWM Controller
3-215	UC2823B	High Speed PWM Controller
3-223	UC2824	High Speed PWM Controller
3-230	UC2825	High Speed PWM Controller
3-215	UC2825A	High Speed PWM Controller
3-215	UC2825B	High Speed PWM Controller
3-237	UC2826	Secondary Side Average Current Mode Controller
3-247	UC2827-1	Buck Current/Voltage Fed Push-Pull PWM Controller
3-247	UC2827-2	Buck Current/Voltage Fed Push-Pull PWM Controller
3-252	UCC2829-1	High Speed PWM Controller
3-252	UCC2829-1	High Speed PWM Controller
4-13	UCC283-3	Low Dropout 3 Ampere Linear Regulator
4-13	UCC283-5	Low Dropout 3 Ampere Linear Regulator
4-13	UCC283-ADJ	Low Dropout 3 Ampere Linear Regulator
3-258	UCC2830-4	5-Bit Microprocessor Power Supply Controller
3-258	UCC2830-5	5-Bit Microprocessor Power Supply Controller
3-258	UCC2830-6	5-Bit Microprocessor Power Supply Controller
4-20	UC2832	Precision Low Dropout Linear Controller
4-20	UC2833	Precision Low Dropout Linear Controller
4-27	UC2834	High Efficiency Linear Regulator
4-33	UC2835	High Efficiency Regulator Controller
4-33	UC2836	High Efficiency Regulator Controller
4-37	UCC2837	8-Pin N-FET Linear Regulator Controller
3-265	UC2838A	Magnetic Amplifier Controller
3-269	UCC2839	Secondary Side Average Current Mode Controller
4-44	UCC284-12	Low Dropout 0.5A Negative Linear Regulator
4-44	UCC284-5	Low Dropout 0.5A Negative Linear Regulator
4-44	UCC284-ADJ	Low Dropout 0.5A Negative Linear Regulator
*	UC2840	Programmable, Off-Line, PWM Controller
3-274	UC2841	Programmable, Off-Line, PWM Controller
3-282	UC2842	Current Mode PWM Controller
3-289	UC2842A	Current Mode PWM Controller
3-282	UC2843	Current Mode PWM Controller
3-289	UC2843A	Current Mode PWM Controller
3-282	UC2844	Current Mode PWM Controller
3-289	UC2844A	Current Mode PWM Controller
3-282	UC2845	Current Mode PWM Controller
3-289	UC2845A	Current Mode PWM Controller
3-295	UC2846	Current Mode PWM Controller
3-295	UC2847	Current Mode PWM Controller
3-302	UC2848	Average Current Mode PWM Controller
3-310	UC2849	Secondary Side Average Current Mode Controller
4-49	UC285-1	Fast LDO Linear Regulator
4-49	UC285-2	Fast LDO Linear Regulator
4-49	UC285-3	Fast LDO Linear Regulator
4-49	UC285-ADJ	Fast LDO Linear Regulator
3-320	UC2851	Programmable, Off-Line, PWM Controller
5-3	UC2852	High Power-Factor Preregulator
5-8	UC2853	High Power Factor Preregulator

** Consult Factory*

Part Number Index (cont'd)

PAGE	PART #	DESCRIPTION
5-12	UC2854	High Power Factor Preregulator
5-20	UC2854A	Enhanced High Power Factor Preregulator
5-20	UC2854B	Enhanced High Power Factor Preregulator
5-26	UC2855A	High Performance Power Factor Preregulator
5-26	UC2855B	High Performance Power Factor Preregulator
3-326	UC2856	Improved Current Mode PWM Controller
5-34	UCC2857	Isolated Boost PFC Preregulator Controller
5-39	UCC2858	High Efficiency, High Power Factor Preregulator
3-334	UC2860	Resonant Mode Power Supply Controller
3-342	UC2861	Resonant-Mode Power Supply Controller
3-342	UC2862	Resonant-Mode Power Supply Controller
3-342	UC2863	Resonant-Mode Power Supply Controller
3-342	UC2864	Resonant-Mode Power Supply Controller
3-342	UC2865	Resonant-Mode Power Supply Controller
3-342	UC2866	Resonant-Mode Power Supply Controller
3-342	UC2867	Resonant-Mode Power Supply Controller
3-342	UC2868	Resonant-Mode Power Supply Controller
3-348	UC2870-1	High Efficiency, Synchronous, Step-down (Buck) Controller
3-348	UC2870-2	High Efficiency, Synchronous, Step-down (Buck) Controller
8-5	UC2871	Resonant Fluorescent Lamp Driver
8-10	UC2872	Resonant Lamp Ballast Controller
3-355	UC2874-1	High Efficiency, Synchronous, Step-down (Buck) Controller
3-355	UC2874-2	High Efficiency, Synchronous, Step-down (Buck) Controller
3-363	UC2875	Phase Shift Resonant Controller
3-363	UC2876	Phase Shift Resonant Controller
3-363	UC2877	Phase Shift Resonant Controller
3-363	UC2878	Phase Shift Resonant Controller
3-373	UC2879	Phase Shift Resonant Controller
3-378	UCC2880-4	Pentium® Pro Controller
3-378	UCC2880-5	Pentium® Pro Controller
3-378	UCC2880-6	Pentium® Pro Controller
3-385	UCC2881-1	High Performance Average Current Mode PWM
3-385	UCC2881-2	High Performance Average Current Mode PWM
3-385	UCC2881-3	High Performance Average Current Mode PWM
3-385	UCC2881-4	High Performance Average Current Mode PWM
3-385	UCC2881-5	High Performance Average Current Mode PWM
3-385	UCC2881-6	High Performance Average Current Mode PWM
3-389	UCC2882	Average Current Mode Synchronous Controller with 5-Bit DAC
3-398	UCC2883	Micropower Peak Current Mode Controller
3-407	UCC2884	Frequency Foldback Current Mode PWM Controller
3-414	UCC2885	Micropower Secondary Regulation IC
3-422	UC2886	Average Current Mode PWM Controller IC
3-429	UCC2888	Off-line Power Supply Controller
3-434	UCC2889	Off-line Power Supply Controller
3-440	UCC2890	Off-Line Battery Charger Circuit
3-447	UC2901	Isolated Feedback Generator
3-452	UC2902	Load Share Controller
3-457	UC2903	Quad Supply and Line Monitor
3-464	UC2904	Precision Quad Supply and Line Monitor
8-16	UC2906	Sealed Lead-Acid Battery Charger
3-469	UC2907	Load Share Controller
3-475	UC2908	Programmable Voltage Clamp
8-23	UC2909	Switchmode Lead-Acid Battery Charger
3-482	UC2910	4-Bit DAC and Voltage Monitor
9-8	UCC2913	Negative Voltage Hot Swap Power Manager
9-14	UC2914	5V to 35V Hot Swap Power Manager
9-26	UCC2915	15V Programmable Hot Swap Power Manager
9-34	UCC2917	Positive Floating Hot Swap Power Manager
9-42	UCC2918	Low On Resistance Hot Swap Power Manager
9-48	UCC2919	3V to 8V Hot Swap Power Manager
9-57	UCC2920	–3V to –15V Hot Swap Power Manager
9-63	UCC2921	Latchable Negative Floating Hot Swap Power Manager
10-3	L293	Push-Pull Four Channel Driver
8-36	UCC2930-3	Cellular Telephone Power Converter
8-36	UCC2930-5	Cellular Telephone Power Converter
10-3	L293D	Push-Pull Four Channel Driver

Part Number Index (cont'd)

PAGE	PART #	DESCRIPTION
3-487	UC29431	Precision Adjustable Shunt Regulator
3-492	UC29432	Precision Analog Controller
8-50	UCC2946	Microprocessor Supervisor with Watchdog Timer
7-3	UC2950	Half-Bridge Bipolar Switch
8-74	UCC2956	Switch Mode Lithium-Ion Battery Charger Controller
3-496	UC2965	Precision Reference with Low Offset Error Amplifier
10-8	UC3172A	Full Bridge Power Amplifier
10-19	UC3173A	Full Bridge Power Amplifier
10-29	UC3175B	Full Bridge Power Amplifier
10-34	UC3176	Full Bridge Power Amplifier
10-34	UC3177	Full Bridge Power Amplifier
10-38	UC3178	Full Bridge Power Amplifier
3-33	UCC3305	HID Lamp Controller
10-43	UC3517	Stepper Motor Drive Circuit
3-41	UC3524	Advanced Regulating PWM
3-46	UC3524A	Advanced Regulating PWM
3-52	UC3525A	Regulating PWM
3-59	UC3525B	Regulating PWM
3-66	UC3526	Regulating PWM
3-73	UC3526A	Regulating PWM
3-52	UC3527A	Regulating PWM
3-59	UC3527B	Regulating PWM
3-81	UC3543	Power Supply Supervisory Circuit
3-81	UC3544	Power Supply Supervisory Circuit
3-86	UC3548	Primary Side PWM Controller
3-94	UCC3570	Low Power PWM
3-101	UC3572	Negative Output Flyback PWM
3-105	UC3573	Buck PWM Stepdown Voltage Regulator
3-109	UC3578	Buck PWM Stepdown Voltage Regulator
3-114	UCC3580-1	Single Ended Active Clamp/Reset PWM
3-114	UCC3580-2	Single Ended Active Clamp/Reset PWM
3-114	UCC3580-3	Single Ended Active Clamp/Reset PWM
3-114	UCC3580-4	Single Ended Active Clamp/Reset PWM
3-122	UCC3581	Micropower Voltage Mode PWM
3-129	UCC3582	High Efficiency Synchronous, Step Down Controller
3-133	UCC3583	Switch Mode Secondary Side Post Regulator
3-141	UC3584	Secondary Side Synchronous Post Regulator
3-146	UC3610	Dual Schottky Diode Bridge
3-148	UC3611	Quad Schottky Diode Array
3-151	UC3612	Dual Schottky Diode
10-50	UC3620	Switchmode Driver for 3-Ø Brushless DC Motors
10-56	UC3625	Brushless DC Motor Controller
10-67	UCC3626	Brushless DC Motor Controller
10-68	UC3633	Phase Locked Frequency Controller
10-75	UC3634	Phase Locked Frequency Controller
10-79	UC3635	Phase Locked Frequency Controller
10-83	UC3637	Switched Mode Controller for DC Motor Drive
10-89	UC3638	Advanced PWM Motor Controller
7-5	UC3702	Quad PWM Relay Driver
7-9	UC3704	Bridge Transducer Swtich
7-13	UC3705	High Speed Power Driver
7-16	UC3706	Dual Output Driver
7-21	UC3707	Dual Channel Power Driver
7-27	UC3708	Dual Non-Inverting Power Driver
7-31	UC3709	Dual High-Speed FET Driver
7-34	UC3710	High Current FET Driver
7-37	UC3711	Dual Ultra High-Speed FET Driver
7-39	UC37131	Smart Power Switch
7-39	UC37132	Smart Power Switch
7-44	UC3714	Complementary Switch FET Driver
7-44	UC3715	Complementary Switch FET Driver
10-97	UC3717	Stepper Motor Drive Circuit
10-105	UC3717A	Stepper Motor Drive Circuit
7-51	UC3724	Isolated Drive Transmitter
7-54	UC3725	Isolated High Side FET Driver
7-58	UC3726	Isolated Drive Transmitter
7-63	UC3727	Isolated High Side IGBT Driver
3-153	UC3730	Thermal Monitor
3-157	UCC3750	Source Ringer Controller
3-166	UCC3751	Single Line Ring Generator Controller
10-113	UC3770A	High Performance Stepper Motor Drive Circuit
10-113	UC3770B	High Performance Stepper Motor Drive Circuit
7-69	UCC3776	Quad FET Driver
3-167	UCC3800	Low-Power BiCMOS Current-Mode PWM
3-167	UCC3801	Low-Power BiCMOS Current-Mode PWM
3-167	UCC3802	Low-Power BiCMOS Current-Mode PWM
3-167	UCC3803	Low-Power BiCMOS Current-Mode PWM
3-167	UCC3804	Low-Power BiCMOS Current-Mode PWM
3-167	UCC3805	Low-Power BiCMOS Current-Mode PWM
3-174	UCC3806	Low Power, Dual Output, Current Mode PWM Controller
3-180	UCC3807-1	Programmable Maximum Duty Cycle PWM Controller

Part Number Index (cont'd)

PAGE	PART #	DESCRIPTION
3-180	UCC3807-2	Programmable Maximum Duty Cycle PWM Controller
3-180	UCC3807-3	Programmable Maximum Duty Cycle PWM Controller
3-185	UCC3808-1	Low Power Current Mode Push-Pull PWM
3-185	UCC3808-2	Low Power Current Mode Push-Pull PWM
3-189	UCC3809-1	Economy Primary Side Controller
3-189	UCC3809-2	Economy Primary Side Controller
4-3	UCC381-3	Low Dropout 1 Ampere Linear Regulator
4-3	UCC381-5	Low Dropout 1 Ampere Linear Regulator
4-3	UCC381-ADJ	Low Dropout 1 Ampere Linear Regulator
3-192	UCC3810	Dual Channel Synchronized Current Mode PWM
3-199	UCC3812	12V Boost Regulator
3-202	UCC3813-0	Low Power Economy BiCMOS Current Mode PWM
3-202	UCC3813-1	Low Power Economy BiCMOS Current Mode PWM
3-202	UCC3813-2	Low Power Economy BiCMOS Current Mode PWM
3-202	UCC3813-3	Low Power Economy BiCMOS Current Mode PWM
3-202	UCC3813-4	Low Power Economy BiCMOS Current Mode PWM
3-202	UCC3813-5	Low Power Economy BiCMOS Current Mode PWM
4-7	UC382-1	Fast LDO Linear Regulator
4-7	UC382-2	Fast LDO Linear Regulator
4-7	UC382-3	Fast LDO Linear Regulator
4-7	UC382-ADJ	Fast LDO Linear Regulator
3-209	UC3823	High Speed PWM Controller
3-215	UC3823A	High Speed PWM Controller
3-215	UC3823B	High Speed PWM Controller
3-223	UC3824	High Speed PWM Controller
3-230	UC3825	High Speed PWM Controller
3-215	UC3825A	High Speed PWM Controller
3-215	UC3825B	High Speed PWM Controller
3-237	UC3826	Secondary Side Average Current Mode Controller
3-247	UC3827-1	Buck Current/Voltage Fed Push-Pull PWM Controller
3-247	UC3827-2	Buck Current/Voltage Fed Push-Pull PWM Controller
3-252	UCC3829-1	High Speed PWM Controller
3-252	UCC3829-2	High Speed PWM Controller
4-13	UCC383-3	Low Dropout 3 Ampere Linear Regulator
4-13	UCC383-5	Low Dropout 3 Ampere Linear Regulator
4-13	UCC383-ADJ	Low Dropout 3 Ampere Linear Regulator

PAGE	PART #	DESCRIPTION
3-258	UCC3830-4	5-Bit Microprocessor Power Supply Controller
3-258	UCC3830-5	5-Bit Microprocessor Power Supply Controller
3-258	UCC3830-6	5-Bit Microprocessor Power Supply Controller
4-17	UCC3831	Universal Serial Bus Power Controller
4-20	UC3832	Precision Low Dropout Linear Controller
4-20	UC3833	Precision Low Dropout Linear Controller
4-27	UC3834	High Efficiency Linear Regulator
4-33	UC3835	High Efficiency Regulator Controller
4-33	UC3836	High Efficiency Regulator Controller
4-37	UCC3837	8-Pin N-FET Linear Regulator Controller
3-265	UC3838A	Magnetic Amplifier Controller
3-269	UCC3839	Secondary Side Average Current Mode Controller
4-44	UCC384-12	Low Dropout 0.5A Negative Linear Regulator
4-44	UCC384-5	Low Dropout 0.5A Negative Linear Regulator
4-44	UCC384-ADJ	Low Dropout 0.5A Negative Linear Regulator
*	UC3840	Programmable, Off-Line, PWM Controller
3-274	UC3841	Programmable, Off-Line, PWM Controller
3-282	UC3842	Current Mode PWM Controller
3-289	UC3842A	Current Mode PWM Controller
3-282	UC3843	Current Mode PWM Controller
3-289	UC3843A	Current Mode PWM Controller
3-282	UC3844	Current Mode PWM Controller
3-289	UC3844A	Current Mode PWM Controller
3-282	UC3845	Current Mode PWM Controller
3-289	UC3845A	Current Mode PWM Controller
3-295	UC3846	Current Mode PWM Controller
3-295	UC3847	Current Mode PWM Controller
3-302	UC3848	Average Current Mode PWM Controller
3-310	UC3849	Secondary Side Average Current Mode Controller
4-49	UC385-1	Fast LDO Linear Regulator
4-49	UC385-2	Fast LDO Linear Regulator
4-49	UC385-3	Fast LDO Linear Regulator
4-49	UC385-ADJ	Fast LDO Linear Regulator
3-320	UC3851	Programmable, Off-Line, PWM Controller
5-3	UC3852	High Power-Factor Preregulator
5-8	UC3853	High Power Factor Preregulator
5-12	UC3854	High Power Factor Preregulator

** Consult Factory*

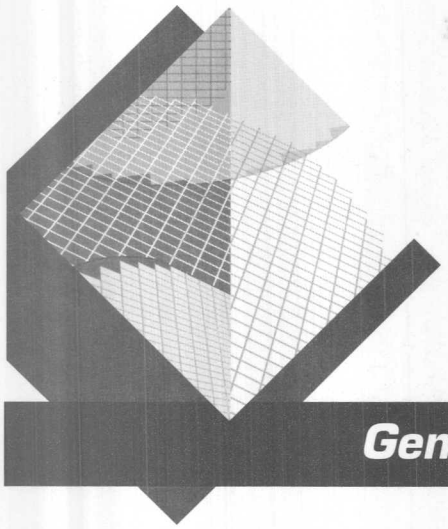
Part Number Index (cont'd)

PAGE	PART #	DESCRIPTION
5-20	UC3854A	Enhanced High Power Factor Preregulator
5-20	UC3854B	Enhanced High Power Factor Preregulator
5-26	UC3855A	High Performance Power Factor Preregulator
5-26	UC3855B	High Performance Power Factor Preregulator
3-326	UC3856	Improved Current Mode PWM Controller
5-34	UCC3857	Isolated Boost PFC Preregulator Controller
5-39	UCC3858	High Efficiency, High Power Factor Preregulator
3-334	UC3860	Resonant Mode Power Supply Controller
3-342	UC3861	Resonant-Mode Power Supply Controller
3-342	UC3862	Resonant-Mode Power Supply Controller
3-342	UC3863	Resonant-Mode Power Supply Controller
3-342	UC3864	Resonant-Mode Power Supply Controller
3-342	UC3865	Resonant-Mode Power Supply Controller
3-342	UC3866	Resonant-Mode Power Supply Controller
3-342	UC3867	Resonant-Mode Power Supply Controller
3-342	UC3868	Resonant-Mode Power Supply Controller
3-348	UC3870-1	High Efficiency, Synchronous, Step-down (Buck) Controller
3-348	UC3870-2	High Efficiency, Synchronous, Step-down (Buck) Controller
8-5	UC3871	Resonant Fluorescent Lamp Driver
8-10	UC3872	Resonant Lamp Ballast Controller
3-355	UC3874-1	High Efficiency, Synchronous, Step-down (Buck) Controller
3-355	UC3874-2	High Efficiency, Synchronous, Step-down (Buck) Controller
3-363	UC3875	Phase Shift Resonant Controller
3-363	UC3876	Phase Shift Resonant Controller
3-363	UC3877	Phase Shift Resonant Controller
3-363	UC3878	Phase Shift Resonant Controller
3-373	UC3879	Phase Shift Resonant Controller
3-378	UCC3880-4	Pentium® Pro Controller
3-378	UCC3880-5	Pentium® Pro Controller
3-378	UCC3880-6	Pentium® Pro Controller
3-385	UCC3881-1	High Performance Average Current Mode PWM
3-385	UCC3881-2	High Performance Average Current Mode PWM
3-385	UCC3881-3	High Performance Average Current Mode PWM
3-385	UCC3881-4	High Performance Average Current Mode PWM
3-385	UCC3881-5	High Performance Average Current Mode PWM
3-385	UCC3881-6	High Performance Average Current Mode PWM
3-389	UCC3882	Average Current Mode Synchronous Controller with 5-Bit DAC
3-398	UCC3883	Micropower Peak Current Mode Controller
3-407	UCC3884	Frequency Foldback Current Mode PWM Controller
3-414	UCC3885	Micropower Secondary Regulation IC
3-422	UC3886	Average Current Mode PWM Controller IC
3-429	UCC3888	Off-line Power Supply Controller
3-434	UCC3889	Off-line Power Supply Controller
3-440	UCC3890	Off-Line Battery Charger Circuit
3-447	UC3901	Isolated Feedback Generator
3-452	UC3902	Load Share Controller
3-457	UC3903	Quad Supply and Line Monitor
3-464	UC3904	Precision Quad Supply and Line Monitor
8-16	UC3906	Sealed Lead-Acid Battery Charger
3-469	UC3907	Load Share Controller
3-475	UC3908	Programmable Voltage Clamp
8-23	UC3909	Switchmode Lead-Acid Battery Charger
3-482	UC3910	4-Bit DAC and Voltage Monitor
8-31	UCC3911	Lithium-Ion Battery Protector
9-3	UCC3912	Programmable Hot Swap Power Manager
9-8	UCC3913	Negative Voltage Hot Swap Power Manager
9-14	UC3914	5V to 35V Hot Swap Power Manager
9-26	UCC3915	15V Programmable Hot Swap Power Manager
9-31	UCC3916	SCSI Termpower Manager
9-34	UCC3917	Positive Floating Hot Swap Power Manager
9-42	UCC3918	Low On Resistance Hot Swap Power Manager
9-48	UCC3919	3V to 8V Hot Swap Power Manager
9-57	UCC3920	–3V to –15V Hot Swap Power Manager
9-63	UCC3921	Latchable Negative Floating Hot Swap Power Manager
8-36	UCC3930-3	Cellular Telephone Power Converter

Part Number Index (cont'd)

PAGE	PART #	DESCRIPTION
8-36	UCC3930-5	Cellular Telephone Power Converter
8-41	UCC3941-3	1V Synchronous Boost Converter
8-41	UCC3941-5	1V Synchronous Boost Converter
8-41	UCC3941-ADJ	1V Synchronous Boost Converter
3-487	UC39431	Precision Adjustable Shunt Regulator
3-487	UC39431B	Precision Adjustable Shunt Regulator
3-492	UC39432	Precision Analog Controller
3-492	UC39432B	Precision Analog Controller
8-50	UCC3946	Microprocessor Supervisor with Watchdog Timer
8-55	UCC3951	Lithium-Ion Battery Monitor
8-69	UCC3954	Single Cell Lithium-Ion to +3.3V Converter
8-74	UCC3956	Switch Mode Lithium-Ion Battery Charger Controller
8-83	UCC3957	Three - Four Cell Lithium-Ion Protector Circuit
3-496	UC3965	Precision Reference with Low Offset Error Amplifier
3-499	UC494A	Advanced Regulating PWM
3-499	UC494AC	Advanced Regulating PWM
3-499	UC495A	Advanced Regulating PWM
3-499	UC495AC	Advanced Regulating PWM
6-5	UC5170C	Octal Line Driver
6-9	UC5171	Octal Line Driver
6-13	UC5172	Octal Line Driver
6-17	UC5180C	Octal Line Receiver
6-20	UC5181C	Octal Line Receiver
8-87	UCC5340	IrDA Receiver
8-91	UCC5341	IrDA 2.4kbps to 115.2kbps Receiver
8-93	UCC5342	IrDA 2.4kbps to 115.2kbps Transceiver
8-96	UCC5343	IrDA Transceiver with Encoder/Decoder
8-100	UCC5344	9.6kbps to 4Mbps IrDA Transceiver
6-23	UC5350	CAN Transceiver
4-54 & 6-28	UC560	27-Line SCSI Source/Sink Regulator
6-32	UC5601	SCSI Active Terminator
6-36	UC5602	SCSI Active Terminator
6-41	UC5603	9-Line SCSI Active Terminator
6-45	UC5604	9-Line Low Capacitance SCSI Active Terminator
6-49	UC5605	9-Line Low Capacitance SCSI Active Terminator
6-53	UCC5606	9-Line 3-5 Volt SCSI Active Terminator, Reverse Disconnect
6-57	UC5607	Plug and Play, 18-Line SCSI Active Terminator
6-60	UC5608	18-Line Low Capacitance SCSI Active Terminator
6-63	UC5609	18-Line Low Capacitance SCSI Active Terminator
6-66	UCC5610	18-Line 3-5 Volt Low Capacitance SCSI Active Terminator
6-70	UCC5611	18-Line 3-5 Volt SCSI Active Terminator, Reverse Disconnect
6-74	UC5612	9-Line Low Capacitance SCSI Active Terminator
6-78	UC5613	9-Line Low Capacitance SCSI Active Terminator
6-82	UCC5614	9-Line 3-5 Volt Low Capacitance SCSI Active Terminator
6-86	UCC5615	9-Line SCSI Terminator, Reverse Disconnect
6-89	UCC5616	9-Line SCSI Terminator
6-93	UCC5617	18-Line SCSI Terminator, Reverse Disconnect
6-97	UCC5618	18-Line SCSI Terminator
6-101	UCC5619	27-Line SCSI Terminator, With Reverse Disconnect
6-104	UCC5620	27-Line SCSI Terminator
6-107	UCC5621	27-Line SCSI Terminator, With Split Reverse Disconnect
6-110	UCC5622	27-Line SCSI Terminator, With Split Disconnect
6-113	UCC5630	Low Voltage Differential (LVD/SE) SCSI 9 Line Terminator
6-117	UCC5632	Multi-mode (LVD/SE) SCSI-9 Line Terminator w/ 2.85V Regulator
6-118	UCC5640	Low Voltage Differential (LVD) SCSI-9 Line Terminator
6-119	UC5661	Ethernet Coaxial Impedance Monitor
10-116	UCC5950	10-Bit Serial D/A Converter


UNITRODE



General Information

2



General Information

2

About this Databook

PRODUCT CLASSIFICATION STATUS

The following definitions apply to describe Unitrode's current product production status. Unitrode also reserves the right to make changes without further notice in order to improve design performance, reliability, or manufacturability.

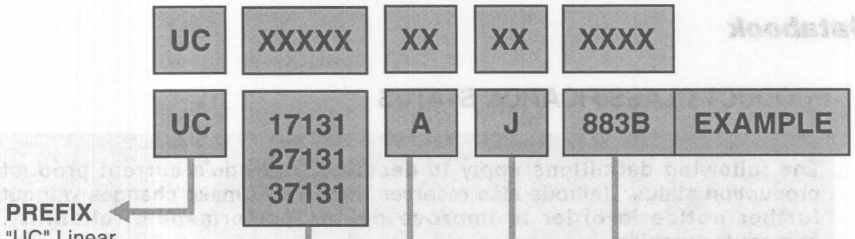
CLASSIFICATION	PRODUCT STAGE	DESCRIPTION
Advance Information Data Sheet	Formative or Design	This document contains the design specifications for product under development. Specifications may be changed in any manner without notice.
Preliminary Data Sheet	First Production	Supplementary data may be published at a later date. Unitrode reserves the right to make changes at any time without notice, in order to improve design and supply the best product possible.
No Classification Noted	Full Production	Product in Full Production

This databook contains complete data sheet information about Unitrode's integrated circuits for Commercial, Industrial and Military/Aero applications. It includes all our latest new products including products that will be introduced throughout the year 1997.

For more information about any new products or any of Unitrode service capabilities, please call, write or fax.

Visit our website @ http://www.unitrode.com

Part Numbering System



PREFIX
"UC" Linear Integrated Circuits
"UCC" BiCMOS

PART NUMBER
First digit "1" = Military Temp. Range*
First digit "2" = Industrial Temp. Range*
First digit "3" = Commercial Temp. Range*

*Consult individual data sheets for specific temperature ranges on each part.

OPTIONAL GRADES
A or B - Improved Version

SCREEN/PROCESSING OPTIONS
"883" - MIL-STD-883
Class Q of MIL-PRF-38535

PACKAGE OPTIONS

Letter Designator	Package Type
D	Plastic Narrow Body (150 mil) S.O.I.C.
DW	Plastic Wide Body (300 mil) S.O.I.C.
DP	Plastic Narrow Body Power S.O.I.C.
DS	Plastic Narrow Body (150 mil) S.O.I.C. with Shunt Current Sense
DWP	Plastic Wide Body Power S.O.I.C.
FP	Power Plastic Metric Quad Flatpack (MQFP)
FQ	Plastic Low Profile Quad Flatpack (LQFP)
J	Ceramic Dual-in-Line (300 & 600 mil widths)
L	Ceramic Leadless Chip Carrier (LCC)
LP	Power LCC
M	Shrink Small Outline (150 mil)
MWP	Power Quasi Shrink Small Outline (300 mil body, 0.8mm Pitch)
N	Plastic Dual-in-Line (300 & 600 mil widths)
PW	Thin Shrink Small Outline (TSSOP)
PWP	Power TSSOP
Q	Plastic Leadless Chip Carrier (PLCC)
QP	Power PLCC
SP	Power Ceramic Dual-in-Line
T	Plastic TO-220
TD	Plastic TO-263 Power Surface Mount
Z	Zig-Zag In-Line Power Package

For More Information See Packaging Section

Unitrode's Commitment to Quality

Quality, reliability, and innovation are the hallmarks of our products! Everything Unitrode does aims at providing to our customers the highest levels of quality, reliability and customer satisfaction available in the marketplace. These are the keys to "Building Customer Loyalty," the theme of our quality program.

These achievements do not happen by chance. Our accomplishments have come from a strong and sustained commitment to Total Business Excellence. We demonstrate our commitment with our TBE Policy Statement.

Total Business Excellence Policy

Unitrode pledges to satisfy our customers', employees', and stakeholders' expectations in all business activities. We are committed to achieving this through Total Business Excellence. This means:

- We actively support and enable a Total Business Excellence environment.
- We perform our work with the highest level of quality workmanship.
- We make decisions based on the analysis of data.
- We perform our work in a controlled and disciplined manner.
- We make decisions that build customer loyalty.
- We solve problems to their root cause in a timely manner.
- We foster empowerment and teamwork.
- We continuously improve our performance.
- We assure our quality system provides value to our company and to our customers.
- We routinely self assess Total Business Excellence for effectiveness.
- We continually improve Total Business Excellence.

Quality and Reliability Assurance

The foundation of our commitment begins with our effective Quality Assurance System. In the October of 1992, Unitrode Corporation became one of the first in our industry to achieve IS/ISO 9001/EN 29001 Registration. Currently, Unitrode's quality assurance system exceeds the rigorous requirements of ISO 9001-1994 and MIL-PRF-38535.

In August of 1996, the Defense Supply Center-Columbus (DSCC) granted Unitrode full Q-Level certification to MIL-PRF-38535 for listing on the Qualified Manufacturers List (QML). In addition, DSCC continued Unitrode's laboratory suitability by certifying that our test methods are performed in accordance with MIL-STD-883.

All Unitrode's products and processes that are used to manufacture our products meet extensive qualification requirements before shipping to customers. Qualification ensures:

- Customer and/or design requirements are translated efficiently into manufacturing requirements;
- That all groups are integrated, coordinated and capable;
- Our processes are manufacturable;
- Our products meet or exceed the reliability requirements of our customers.

Process Qualification

When a process qualification is required, Quality Assurance organizes a cross functional team who prepares and completes a formal qualification plan per QP 2515. Key requirements for major processes include: documented design rules and process specifications; process and device simulation with full SPICE models; completed process control plan with identified critical, significant and non-critical characteristics; implemented process control charts; demonstrated Cp, and Cpk for significant and critical characteristics; documented out of control action plans (OCAPs); completed quality audit; process acceptance criteria; Gage R&R studies; construction analyses; and extensive reliability testing.

Our extensive reliability requirements ensure our new processes demonstrate a 200 FIT (calculated @70 degrees C, .7 eV activation energy, 60% confidence) or better at the time of qualification using a minimum of 3 wafer lots. Figure 1, on page 2-5, provides typical reliability tests that are performed for new major processes.

Package Qualification

Whenever a new package is introduced, in addition to qualifying the manufacturing process using requirements appropriate to assembly processing, Unitrode performs a complete battery of reliability tests.

Figure 2, on page 2-6, depicts typical requirements for plastic packages. Figure 3, on page 2-7, presents the requirements for hermetic packages.

Product Qualification

New products must be manufactured using qualified processes and packages. Unitrode's new product qualification consists of 2 major milestones: Release For Introduction (RFI) and Release to Production (RTP).

RFI is the term Unitrode uses to describe devices that: are built on a qualified process; meet the preliminary data sheet over the specified temperature range; demonstrate no infant mortality; have been verified in the appropriate application; had ESD measured and classified; have a released preliminary test program.

Devices which achieve **RTP** meet all the **RFI** requirements plus additional requirements and completes Unitrode's product qualification. Typical RTP requirements include: bench and temperature characterization; demonstrated compliance to all datasheet parameters; meet Cp, Cpk targets for all untrimmed parameters in datasheet; test program complete and released to production; machine capability less than 5% of the device specification range; test schematic(s), test program(s), bonding diagram(s), burn-in diagrams approved and released; ESD measured and classified (human body model); passed latch-up and HTOL test to 1000 hrs; and, final data sheet approved and released.

Results

As a result of our comprehensive qualification procedures, we are able to report long-term device reliability of 4.0 FITs or lower failure rates for combined functional families. This is estimated through the accumulation of millions of hours of life testing at accelerated temperatures.

Failure Analysis

If we do experience a failure during pre-production qualification, we have an extensive failure analysis lab to determine and fix the root cause before they ever reach our customers. We begin by verifying the failure to published specifications. We provide written failure verification to our customers within 72 hours.

Figure 1 Typical Reliability Tests for New Processes

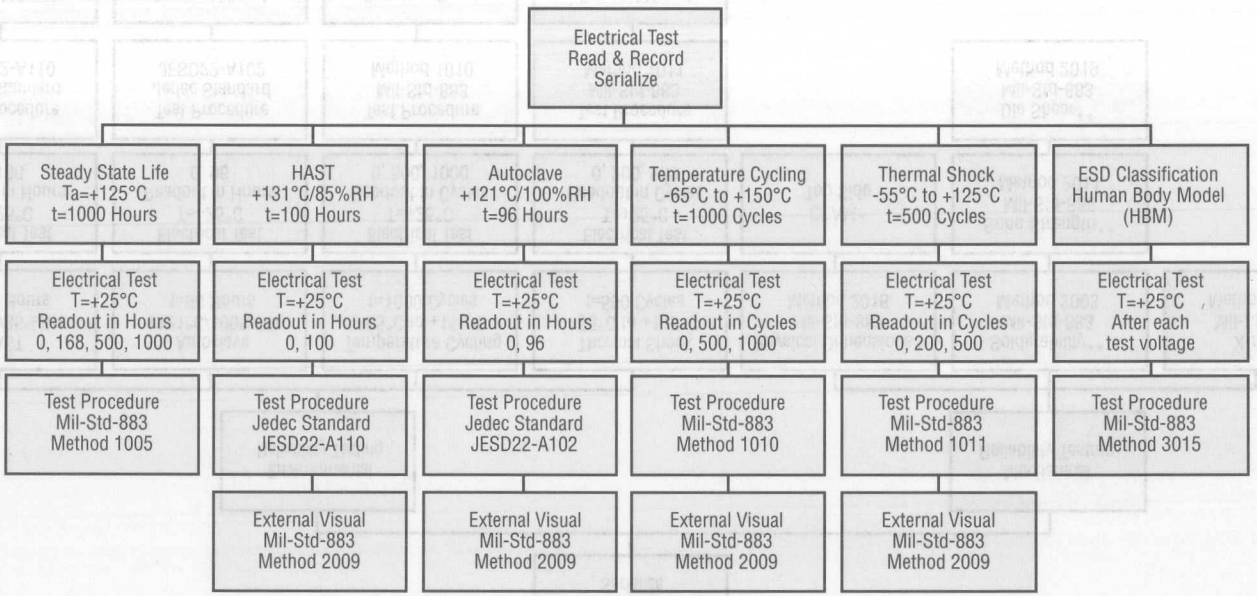
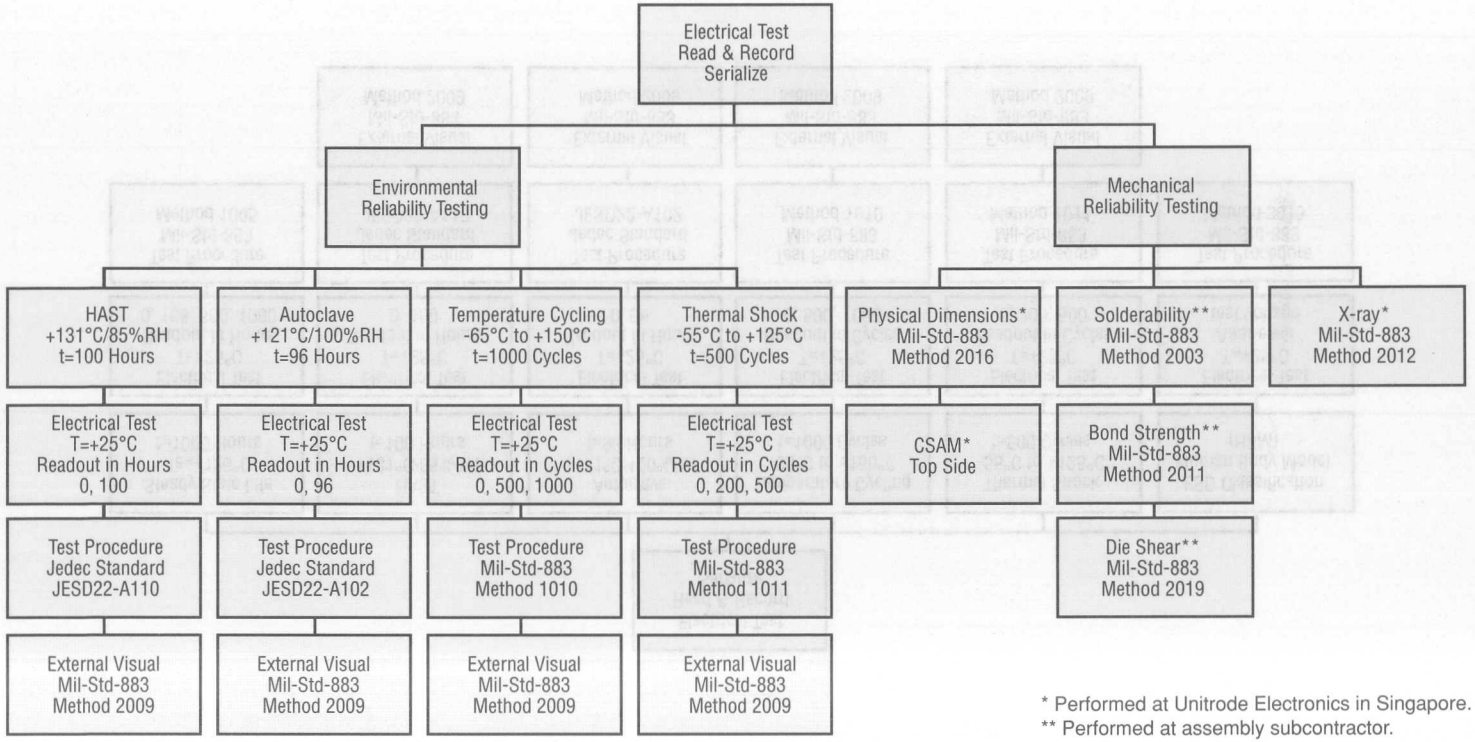
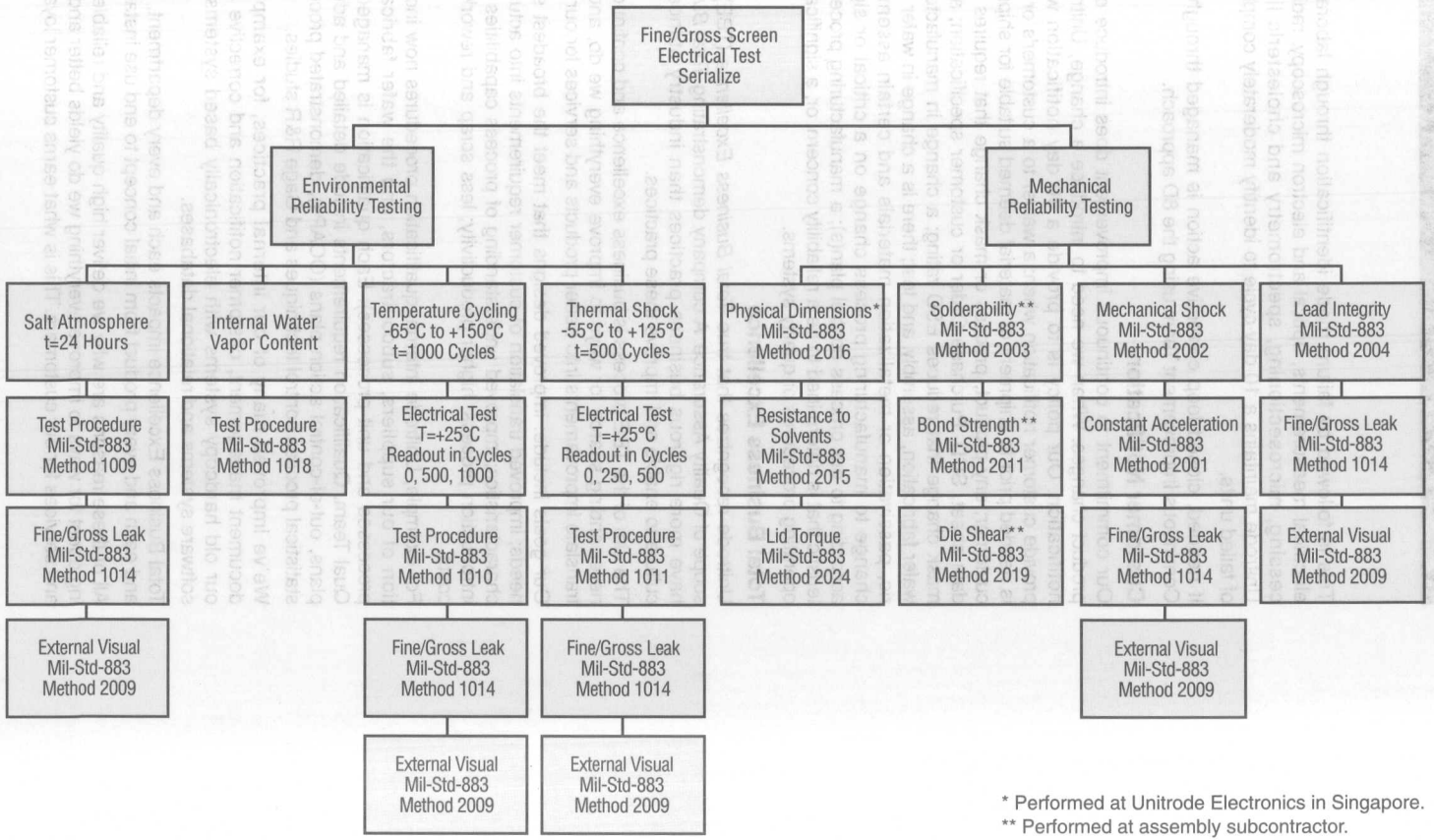


Figure 2 Typical Reliability Requirements for Plastic Packages



* Performed at Unitrode Electronics in Singapore.
** Performed at assembly subcontractor.

Figure 3 Typical Reliability Requirements for Hermetic Packages



* Performed at Unitrode Electronics in Singapore.
** Performed at assembly subcontractor.

This is followed by failure mode identification through laboratory analyses such as electrical measurements, optical and electron microscopy, radiography, device deprocessing, microsectioning, spectrometry and cholesteric liquid crystal analysis. Unitrode maintains a 10 day cycle to identify moderately complex failures from receipt of failed units.

If needed, closed loop corrective action is managed through our Corrective Action Continuous Improvement Team using the 8D approach.

Customer Notification

Our commitment to continuous improvement does introduce occasional process and product changes. When we need to introduce a change, Unitrode issues a customer notification. Our policy is to provide a 90 day notification whenever possible. We provide customer notification when: a waiver to a customer's or Unitrode's specification is needed prior to shipment of material deemed suitable for shipment by Unitrode or our customer; any product, process or mask change that requires a change to Unitrode's data sheet, SCD, Purchase Order or customer specification; any product, process or mask change that reduces ESD rating; a change in manufacturing location including: wafer fabrication, assembly, and test; there is a change in wafer starting material, dielectric, passivation or metalization materials and certain assembly materials; a major change to manufacturing process change on a critical or significant characteristic according to our process control plan(s); a manufacturing process change to a characteristic that is determined to be a reliability concern; or, a significant change to Unitrode's operating procedures or quality systems.

Total Business Excellence

Unitrode recognizes that true *Total Business Excellence* (TBE) goes well beyond the scope of Quality Assurance. A company demonstrating *Total Business Excellence* must have more rigorous business practices than industry standards and a supporting culture to enable and improve these practices.

The aim of the TBE process is business excellence and continuous improvement. It is a never ending search for ways to improve everything we do, and a pledge to ultimately translate improvements into better products and services for our customers.

Our goals include: improved designs that meet the broadest spectrum of application needs; improved translation of customer requirements into actual product performance characteristics; improved understanding of process capabilities to improve the product introduction process; higher productivity; less scrap and rework; and lower production costs.

For example, Unitrode internal qualification procedures now include rigorous qualification of our suppliers, subcontractors, and the wafer fabrication (both major new processes and unit processes). Each qualification is managed by a cross functional Qual Team. Qualification requirements include detailed and advanced process control plans, out-of-control action plans (OCAPs), demonstrated process capability, advance statistical process control techniques and Gage R&R studies.

We've improved many of our internal practices, for example: shop floor control, document management, customer notification and corrective action. We've replaced our old hardcopy systems with electronically based systems using state-of-the art software systems and relational databases.

Total Business Excellence impacts each and every department, each and every activity, and each and every product from initial concept to end use installation and operation.

All of these reasons are why we deliver high quality and reliable products. Our continuing quest for ways to improve everything we do yields better and more reliable products and services for our customers. This is what earns customer loyalty!

Battery Chargers/Protection

Part Number	Description	Page Number
UC3956	Lithium-ion Battery Charger	8-74
UCC3911	Two Cell Lithium-ion Protector	8-31
UCC3957	3-4 Cell Lithium-ion Battery Protector	8-83
UCC3951	Lithium-ion Battery Monitor	8-55

DC/DC Switching Regulators

Part Number	Description	Page Number
UCC3812	Boost Regulator	3-199
UCC3941-3/-5/-ADJ	1V Synchronous Boost Converter	8-41
UCC3954	Single Cell Lithium-ion to 3.3V Converter	8-69
UC3886	P6 Power Controller	3-422
UCC3582	8 Pin DC/DC Controller	3-129
UCC3585	Low Voltage DC/DC Controller	*
UCC3830-4/-5/-6	P6 Power Controller	3-258
UCC3880-4/-5/-6	P6 Power Controller	3-378
UCC3881-1/-2/-3/-4/-5/-6	Average Current Mode DC/DC Controller	3-385
UCC3882	P6 Synchronous Buck PWM	3-389

Intelligent Motion Control

Part Number	Description	Page Number
UC3638	Advanced PWM Motor Controller	10-89

Interface

Part Number	Description	Page Number
UCC5344	4MB IrDA Transceiver	8-100
UC5350	CAN Transceiver	6-23
UCC5615	Simple 9 Line SCSI Terminator	6-86
UCC5616	Simple 9 Line SCSI Terminator	6-89
UCC5617	18 Line Low Capacitance SCSI Terminator	6-93
UCC5618	18 Line Low Capacitance SCSI Terminator	6-97
UCC5619	27 Line Low Capacitance SCSI Terminator	6-101
UCC5620	27 Line Low Capacitance SCSI Terminator	6-104
UCC5621	27 Line Low Capacitance SCSI Terminator	6-107
UCC5622	27 Line Low Capacitance SCSI Terminator	6-110
UCC5630	9 Line Dual Mode Low Voltage Differential SCSI Terminator	6-113
UCC5632	LVD/SE Regulator SCSI Terminator	6-117
UCC5640	9 Line Low Voltage Differential SCSI Terminator	6-118

** Consult Factory*

Low Dropout Linear Regulators

Part Number	Description	Page Number
UCC3837	N-FET LDO Linear Regulator	4-37
UCC381-3/-5/-ADJ	Low Dropout 1 Amp Linear Regulator	4-3
UCC383-3/-5/-ADJ	Three amp LDO	4-13
UCC384-5,-12,-ADJ	Negative LDO	4-44
UC385-1/-2/-3/-ADJ	5 Amp Fast Low Dropout Linear Regulator	4-49

Power Drivers

Part Number	Description	Page Number
UC3702	Quad Relay Driver	7-5
UC37131/2	Smart Power Switch	7-39
UCC3729	FET Driver with UVLO	*
UCC3776	Quad FET Driver	7-69

Power Supply Support

Part Number	Description	Page Number
UCC3857	Isolated PFC Controller	5-34
UCC3858	Energy Star PFC Controller	5-39
UC3902	Load Share Controller	3-452
UCC3926	Integrated Current Sensor	*
UC3960	Primary Side Startup Circuit	*
UC3961	Advanced Primary Side Startup Circuit	*
UC3965	Precision Voltage Reference w/Low Offset Error Amplifier	3-496

Pulse Width Modulators

Part Number	Description	Page Number
UC3548	Average Current Mode Primary Side PWM Controller	3-86
UC3578	Buck PWM Stepdown Voltage Regulator	3-109
UC3584	Secondary Side Synchronous Post Regulator	3-141
UCC3580-1/-2/-3/-4	Single Ended Active Clamp/Reset PWM	3-114
UCC3583	Switch Mode Secondary Side Post Regulator	3-133
UCC3807-1/-2/-3	Programmable Maximum Duty Cycle PWM Controller	3-180
UCC3808-1/-2	8-Pin Push-Pull Controller	3-185
UCC3809-1/-2	Economy Primary Side Controller	3-189
UCC3813-0/-1/-2/-3/-4/-5	Low Power Economy BiCMOS Current Mode PWM	3-202
UCC3827-1/-2	Buck Current/Voltage Fed PWM Controller	3-247
UCC3829-1/-2	High Speed PWM Controller	3-252
UCC3839	Secondary Side Average Current Mode Controller	3-269

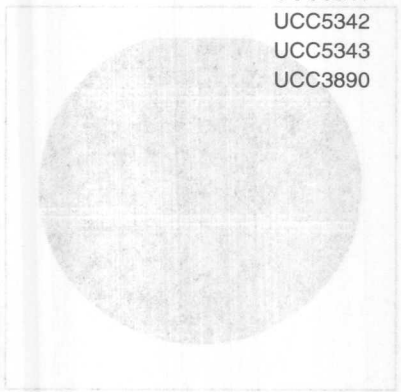
** Consult Factory*

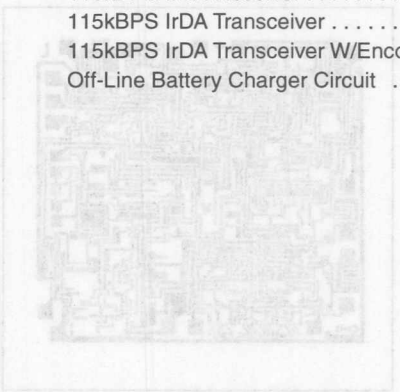
Pulse Width Modulators (cont'd)

Part Number	Description	Page Number
UCC3839	Secondary Side Average Current Mode Controller	3-269
UCC3884	Frequency Foldback Current Mode PWM	3-407
UCC3888	Off-Line Power Supply Controller	3-429

Special Function

Part Number	Description	Page Number
UCC3831	USB Hub Power Controller	4-17
UC3910	P6 Reference/DAC/Monitor	3-482
UCC3750	Source Ring Generator	3-157
UC3908	Programmable Voltage Clamp	3-475
UC3914	5V to 35V Hot Swap Power Manager	9-14
UCC3916	SCSI Termpower Manager	9-31
UCC3917	Floating Positive Hot Swap Power Manager	9-34
UCC3918	Low RDSon Hot Swap Power Manager	9-42
UCC3919	3V to 8V Hot Swap Power Manager	9-48
UCC3920	Negative Voltage Hot Swap Power Manager	9-57
UCC3921	Latchable Hot Swap Power Manager	9-63
UCC3930-3/-5	Cellular Telephone Power Converter	8-36
UCC5341	115kBPS IrDA Receiver	8-91
UCC5342	115kBPS IrDA Transceiver	8-93
UCC5343	115kBPS IrDA Transceiver W/Encoder/Decoder	8-96
UCC3890	Off-Line Battery Charger Circuit	3-440





** Consult Factory*

Description

Unitrode offers most of our products in die and/or wafer form through our die distributors. Unitrode's die utilize either linear bipolar or BiCMOS process technology featuring tight beta controls and resistor matching techniques.

Die thickness is either 12 mils or 15 mils, +/- 1 mil. Interconnects are an alloy of copper and aluminum (to reduce the possibility of electromigration). Most product's backside material is pure silicon.

Testing

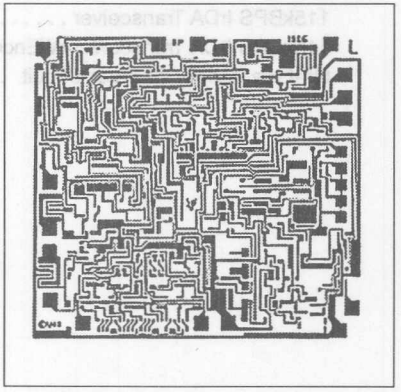
All products are tested at two separate points: (1) wafer process parameter in-line probing and (2) ambient electrical test probing. Die are tested to full data sheet specifications, with the exception of some high power or high speed devices where production probe equipment limit the test environment.

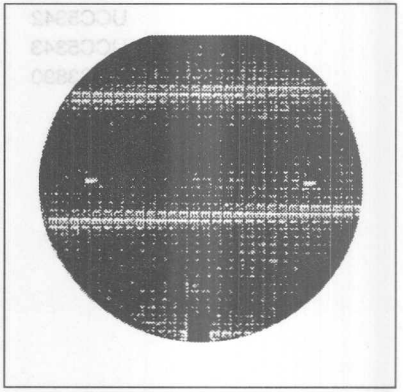
Inspection

Unitrode performs visual inspections on military grade die to MIL-STD-883, Method 2010, conditions A or B, or to individual customer specifications. Die is supplied in "waffle pack" or single wafer form. Standard wafers are 100 mils, generic 4- or 6-inch diameter.

Ordering

Product is available from Unitrode's authorized die distributors, and part numbers end with the suffix "c" for chip form or "chipwfr" for wafer form.

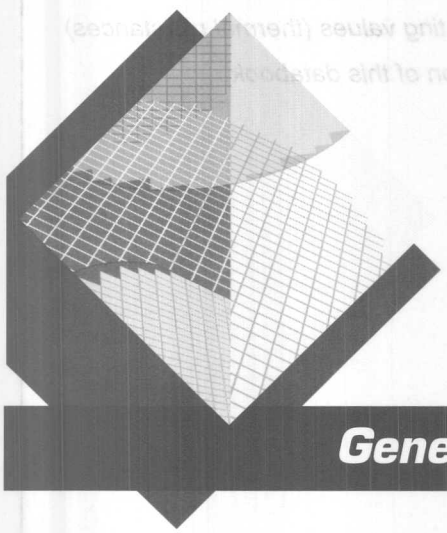






Consult Applications Handbook for available applications/design notes.

Datasheets in this section are organized in numeric order using the commercial part number.



General Power Supply

3

Packaging Note:

- *Values listed for recommended lead soldering time and temperature apply to ceramic thru-hole components only. Please consult the Packaging Section of this databook for recommendations on plastic SMD board attach processing.*

- *Unless otherwise noted, thermal resistance values listed on individual data sheets are for the device as it operates in a plastic thru-hole package. Results for other packaging options can be inferred by scaling the package rating values (thermal resistances) presented in the Packaging Section of this databook.*

Current Mode Controllers

Current Mode Controllers	UNITRODE PART NUMBER				
	UCC3305-⁜	UCC3800	UCC3801	UCC3802	UCC3803
Application	Constant Power HID Lamp Controller	DC-DC and Battery	DC-DC and Battery	Off-line	DC-DC and Battery
Topology	Boost, Flyback	Buck, Boost	Buck, Boost	Forward, Flyback	Buck, Boost
Voltage Reference Tolerance	2%	1.5%	1.5%	1.5%	1.5%
Peak Output Current	0.5A	1A	1A	1A	1A
Maximum Practical Operating Frequency	500kHz	1MHz	1MHz	1MHz	1MHz
Outputs	3 - Single and Dual Alternating, Totem Pole	Single, Totem Pole	Single, Totem Pole	Single, Totem Pole	Single, Totem Pole
Startup Current		100µA	100µA	100µA	100µA
Leading Edge Blanking		Y	Y	Y	Y
Soft Start		Y	Y	Y	Y
Maximum Duty Cycle		100%	50%	100%	100%
Separate Oscillator/ Synchronization Terminal					
Application/Design Note	U-161	DN-65, U-133A	DN-65, U-133A	DN-42A, DN-65, U-133A	DN-43, DN-48, DN-54, DN-56, DN-65, U-133A

Current Mode Controllers (cont'd)	UNITRODE PART NUMBER				
	UCC3804	UCC3805	UCC3806	UCC3807 ✚	UCC3808 ✚
Application	Off-line	DC-DC and Battery	Isolated Output, Push-pull Controller	Off-line, DC-DC and Battery	Off-line, DC-DC
Topology	Forward, Flyback	Forward, Flyback	Push-pull, Full Bridge, Half Bridge	Forward, Flyback Buck, Boost	Push-pull, Full Bridge, Half Bridge
Voltage Reference Tolerance	1.5%	1.5%	1%	1.5%	2%
Peak Output Current	1A	1A	0.5A	1A	0.5A Source, 1A Sink
Maximum Practical Operating Frequency	1MHz	1MHz	1MHz	1MHz	1MHz
Outputs	Single, Totem Pole	Single, Totem Pole	Dual Alternating, Totem Pole	Single, Totem Pole	Dual Alternating, Totem Pole
Startup Current	100µA	100µA	100µA	100µA	130µA
Leading Edge Blanking	Y	Y		Y	
Soft Start	Y	Y	Y	Y	Y
Maximum Duty Cycle	50%	50%	50%/50%	Programmable	50%/50%
Separate Oscillator/ Synchronization Terminal			Y		
Application/Design Note	DN-65, U-133A	DN-46, DN-65, U-133A	DN-45, DN-51, DN-65, U-144	DN-65	DN-65

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.

✚ New Product

⁜ Does Not Feature UVLO

Current Mode Controllers

Current Mode Controllers (cont'd)	UNITRODE PART NUMBER				
	UCC3809 +	UCC3810	UCC3813-0 +	UCC3813-1 +	UCC3813-2 +
Application	Isolated Off-line, DC-DC Primary Controller	Dual PWM Controller, Off-line, DC-DC	DC-DC and Battery	DC-DC and Battery	Off-line
Topology	Forward, Flyback, Buck, Boost	Forward, Flyback Buck, Boost	Buck, Boost	Buck, Boost	Forward, Flyback
Voltage Reference Tolerance	5%	1.5%	1.5%	1.5%	1.5%
Peak Output Current	0.4A Source, 1A Sink	1A	1A	1A	1A
Maximum Practical Operating Frequency	1MHz	1MHz	1MHz	1MHz	1MHz
Outputs	Single, Totem Pole	Dual, Totem Pole	Single, Totem Pole	Single, Totem Pole	Single, Totem Pole
Startup Current	100µA	150µA	100µA	100µA	100µA
Leading Edge Blanking		Y	Y	Y	Y
Soft Start	Y		Y	Y	Y
Maximum Duty Cycle	90%	50%	100%	50%	100%
Separate Oscillator/ Synchronization Terminal	N/A	Y			
Application/Design Note	DN-65	DN-65	DN-65, U-133A	DN-65, U-133A	DN-65, U-133A

Current Mode Controllers (cont'd)	UNITRODE PART NUMBER				
	UCC3813-3 +	UCC3813-4 +	UCC3813-5 +	UC3823	UC3823A
Application	DC-DC and Battery	Off-line	DC-DC and Battery	DC-DC	DC-DC
Topology	Buck, Boost	Forward, Flyback	Forward, Flyback	Buck, Boost	Buck, Boost
Voltage Reference Tolerance	1.5%	1.5%	1.5%	1%	1%
Peak Output Current	1A	1A	1A	1.5A	2A
Maximum Practical Operating Frequency	1MHz	1MHz	1MHz	1MHz	1MHz
Outputs	Single, Totem Pole	Single, Totem Pole	Single, Totem Pole	Single, Totem Pole	Single, Totem Pole
Startup Current	100µA	100µA	100µA	1.1mA	0.1mA
Leading Edge Blanking	Y	Y	Y		Y
Soft Start	Y	Y	Y	Y	Y
Maximum Duty Cycle	100%	50%	50%	100%	Programmable
Separate Oscillator/ Synchronization Terminal				Y	Y
Application/Design Note	DN-65, U-133A	DN-65, U-133A	DN-65, U-133A	U-131	U-128

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
+ New Product

Current Mode Controllers

Current Mode Controllers (cont'd)	UNITRODE PART NUMBER				
	UC3823B	UC3824	UC3825	UC3825A	UC3825B
Application	Off-line	Synchronous Rectifier, Forward Converter	DC-DC	DC-DC	Off-line
Topology	Buck, Boost	Forward, Flyback	Push-pull, Full Bridge, Half Bridge	Push-pull, Full Bridge, Half Bridge	Push-pull, Full Bridge, Half Bridge
Voltage Reference Tolerance	1%	1%	1%	1%	1%
Peak Output Current	2A	1.5A	1.5A	2A	2A
Maximum Practical Operating Frequency	1MHz	1MHz	1MHz	1MHz	1MHz
Outputs	Single, Totem Pole	Dual Complementary, Totem Pole	Dual Alternating, Totem Pole	Dual Alternating, Totem Pole	Dual Alternating, Totem Pole
Startup Current	0.1mA	1.1mA	1.1mA	0.1mA	0.1mA
Leading Edge Blanking	Y			Y	Y
Soft Start	Y	Y	Y	Y	Y
Maximum Duty Cycle	Programmable	100%	50%/50%	Programmable	Programmable
Separate Oscillator/ Synchronization Terminal	Y	Y	Y	Y	Y
Application/Design Note	U-128		U-110	U-128	U-128

Current Mode Controllers (cont'd)	UNITRODE PART NUMBER				
	UC3826 ❍	UC3827 ✚	UCC3829 ✚	UCC3839 ❍	UC3841
Application	Secondary Side, Average Current Mode	Multiple Output or High Voltage Output DC-DC Converters	Off-line, DC-DC	Secondary Side, Average Current Mode Control	Off-line, DC-DC
Topology	Forward, Flyback, Buck, Boost	Buck Current Fed or Voltage Fed, Push-pull	Buck, Boost, Push-pull, Full Bridge, Half Bridge	Any Topology	Forward, Flyback, Buck, Boost
Voltage Reference Tolerance	1%	4%	1%	1%	1%
Peak Output Current	0.25A	Floating 1A for Buck Stage, 0.8A for Push-pull Drivers	2.2A	10mA to Drive Opto-coupler	1A
Maximum Practical Operating Frequency	1MHz	500kHz	1MHz	1MHz	500kHz
Outputs	Single, Totem Pole	Floating Buck, Push-pull	Dual Alternating, Totem Pole	Opto-coupler Drive	Single, Open Collector
Startup Current		1mA	200µA		4.5mA
Leading Edge Blanking	N/A				
Soft Start	Y	Y	Y		Y
Maximum Duty Cycle	Programmable	90% for Buck Stage, 50%/50% for Push-pull Stage	50%/50%		Programmable
Separate Oscillator/ Synchronization Terminal	Y	Y	Y		
Application/Design Note			DN-65		DN-28

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
✚ New Product
❍ Pulse-by-Pulse Current Limiting Not Applicable

Current Mode Controllers

Current Mode Controllers (cont'd)	UNITRODE PART NUMBER				
	UC3842	UC3842A	UC3843	UC3843A	UC3844
Application	Off-line	Off-line	DC-DC	DC-DC	Off-line
Topology	Forward, Flyback, Buck, Boost	Forward, Flyback Buck, Boost	Forward, Flyback Buck, Boost	Forward, Flyback Buck, Boost	Forward, Flyback Buck, Boost
Voltage Reference Tolerance	1%	1%	1%	1%	1%
Peak Output Current	1A	1A	1A	1A	1A
Maximum Practical Operating Frequency	500kHz	500kHz	500kHz	500kHz	500kHz
Outputs	Single, Totem Pole	Single, Totem Pole	Single, Totem Pole	Single, Totem Pole	Single, Totem Pole
Startup Current	1mA	0.5mA	1mA	0.5mA	1mA
Leading Edge Blanking					
Soft Start					
Maximum Duty Cycle	100%	100%	100%	100%	50%
Separate Oscillator/ Synchronization Terminal					
Application/Design Note	DN-27, DN-40, U-100A	DN-27, DN-29, DN-40	DN-30, U-100A	DN-27, DN-29, DN-40	U-100A

Current Mode Controllers (cont'd)	UNITRODE PART NUMBER				
	UC3844A	UC3845	UC3845A	UC3846	UC3847
Application	Off-line	DC-DC	DC-DC	Off-line, DC-DC	Off-line, DC-DC
Topology	Forward, Flyback Buck, Boost	Forward, Flyback Buck, Boost	Forward, Flyback Buck, Boost	Push-pull, Full Bridge, Half Bridge	Push-pull, Full Bridge, Half Bridge
Voltage Reference Tolerance	1%	1%	1%	1%	1%
Peak Output Current	1A	1A	1A	0.5A	0.5A
Maximum Practical Operating Frequency	500kHz	500kHz	500kHz	500kHz	500kHz
Outputs	Single, Totem Pole	Single, Totem Pole	Single, Totem Pole	Dual Alternating, Totem Pole	Dual Alternating, Totem Pole
Startup Current	0.5mA	1mA	0.5mA		
Leading Edge Blanking					
Soft Start				Y	Y
Maximum Duty Cycle	50%	50%	50%	50%/50%	50%/50%
Separate Oscillator/ Synchronization Terminal				Y	Y
Application/Design Note	DN-27, DN-29, DN-40	U-100A	DN-27, DN-29, DN-40	DN-45, U-93, U-100A	U-93

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.

Current Mode Controllers

Current Mode Controllers (cont'd)	UNITRODE PART NUMBER				
	UC3848 ❍	UC3849 ❍	UC3851	UC3856	UC3875
Application	Average Current Mode, Off-line, DC-DC	Secondary Side, Average Current Mode	Off-line, Programmable, Primary Side	Isolated Output, Push-pull Controller	Zero Voltage Transition, Phase Shifted Bridge
Topology	Forward, Flyback	Forward, Flyback, Buck, Boost	Forward, Flyback, Buck, Boost	Push-pull, Full Bridge, Half Bridge	Full Bridge
Voltage Reference Tolerance	1%	1%	1%	1%	1%
Peak Output Current	2A	0.25A	0.2A	1.5A	2A
Maximum Practical Operating Frequency	1MHz	1MHz	500kHz	1MHz	1MHz
Outputs	Single, Totem Pole	Single, Totem Pole	Single, Totem Pole	Dual Alternating, Totem Pole	Quad, Phase Shifted, Totem Pole
Startup Current	500µA		4.5mA		150µA
Leading Edge Blanking	N/A	N/A			
Soft Start		Y	Y	Y	Y
Maximum Duty Cycle	Programmable	Programmable	50%	50%/50%	100%
Separate Oscillator/ Synchronization Terminal		Y		Y	Y
Application/Design Note	U-135, U-140	U-140	DN-28	DN-45	DN-63, U-136

Current Mode Controllers (cont'd)	UNITRODE PART NUMBER				
	UC3876	UC3877	UC3878	UC3879	UCC3883
Application	Zero Voltage Transition, Phase Shifted Bridge	Zero Voltage Transition, Phase Shifted Bridge	Zero Voltage Transition, Phase Shifted Bridge	Zero Voltage Transition, Phase Shifted Bridge	Primary Side Controller for ISDN Applications
Topology	Full Bridge	Full Bridge	Full Bridge	Full Bridge	Flyback
Voltage Reference Tolerance	1%	1%	1%	1%	1%
Peak Output Current	2A	2A	2A	0.1A	0.7A
Maximum Practical Operating Frequency	1MHz	1MHz	1MHz	300kHz	400kHz
Outputs	Quad, Phase Shifted, Totem Pole	Quad, Phase Shifted, Totem Pole	Quad, Phase Shifted, Totem Pole	Quad, Phase Shifted, Totem Pole	Single
Startup Current	150µA	150µA	150µA	150µA	
Leading Edge Blanking					Y
Soft Start	Y	Y	Y	Y	Y
Maximum Duty Cycle	100%	100%	100%	100%	50%
Separate Oscillator/ Synchronization Terminal	Y	Y	Y	Y	Y
Application/Design Note	DN-63, U-136	DN-63, U-136	DN-63, U-136	DN-63, U-136, U-154	

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❍ Pulse-by-Pulse Current Limiting Not Applicable

Current Mode Controllers

Current Mode Controllers (cont'd)	UNITRODE PART NUMBER	
	UCC3884 ✚	UCC3885
Application	Off-Line or DC-DC Frequency Foldback Controller	Secondary Side Regulator for ISDN Applications
Topology	Forward, Flyback, Buck, Boost	Flyback
Voltage Reference Tolerance	2%	1%
Peak Output Current	0.5A Source, 1A Sink	N/A
Maximum Practical Operating Frequency	750kHz	400kHz
Outputs	Single	Single
Startup Current	200µA	
Leading Edge Blanking		Y
Soft Start	Y	Y
Maximum Duty Cycle	80%	50%
Separate Oscillator/ Synchronization Terminal	Y	Y
Application/Design Note	DN-65, U-164	

Current Mode Controllers (Special Features)	UNITRODE PART NUMBER			
	UCC3830 ✚	UC3870 ❍	UC3874 ❍	UCC3880 ✚
Application	Microprocessor Power	Synchronous Rectifier, Average Current Mode	Synchronous Rectifier, Average Current Mode	Microprocessor Power
Topology	Buck	Buck	Buck	Buck
Voltage Reference Tolerance	1%*	2%	2%	1%*
Peak Output Current	1.5A	1A	1A	1.5A
Maximum Practical Operating Frequency	100kHz/200kHz/ 400kHz	300kHz	300kHz	100kHz/200kHz/ 400kHz
Outputs	Single	Dual, Totem Pole	Dual, Totem Pole	Single
Soft Start		Y	Y	
Average Current Mode	Y	Y	Y	Y
Foldback Current Limiting	Y			Y
Maximum Duty Cycle	95%	100%	100%	95%
Special Features	5 Bit Programmable Output Voltage, UV/OV Monitor	External Reference Input Down to 1.5V	Low Power Standby Mode	4 Bit Programmable Output Voltage, UV/OV Monitor

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.

✚ New Product

* Combined Reference, DAC, and Error Amplifier Tolerance

❍ Pulse-by-Pulse Current Limiting Not Applicable

Current Mode Controllers & Current Mode Lighting Controllers

Current Mode Controllers (Special Features) (cont'd)	UNITRODE PART NUMBER		
	UCC3881 ✚	UCC3882 ✚	UC3886 ✚
Application	Microprocessor Power	Microprocessor Power	Microprocessor Power
Topology	Buck	Synchronous Buck	Buck
Voltage Reference Tolerance	1%	1%*	1.5%
Peak Output Current	1.5A	1.5A	1.5A
Maximum Practical Operating Frequency	100kHz/200kHz/ 400kHz	700kHz	400kHz
Outputs	Single	Dual, N-FET Drive	Single
Soft Start			
Average Current Mode	Y	Y	Y
Foldback Current Limiting	Y	Y	
Maximum Duty Cycle	95%	95%	95%
Special Features		5 Bit Programmable Output Voltage, UV/OV Monitor	External Reference Input, Use with UC3910
Application/Design Note			U-156, U-157

Current Mode Lighting Controllers	UNITRODE PART NUMBER		
	UCC3305	UC3871 ★	UC3872 ★
Application	Constant Power HID Lamp Controller	Zero Voltage Switched Fluorescent Lamp Driver with LCD Bias Supply	Zero Voltage Switched Fluorescent Lamp Driver
Topology	Boost, Flyback	Push-Pull	Push-pull
Voltage Range	5V to 18V	4.5V to 20V	4.5V to 24V
Reference Tolerance	2%	1.2%	1.2%
Open Lamp Detect	Y	Y	Y
Soft Start	Y	Y	Y
External Synchronization	Y	Y	Y
Shutdown Current	N/A	1µA	1µA
Maximum Frequency	200kHz	200kHz	200kHz
Lamp Intensity Control	Y	Y	Y
Application/Design Note	DN-65, U-161	DN-75, U-141, U-148	DN-75, U-141, U-148

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.

✚ New Product

* Combined Reference, DAC, and Error Amplifier Tolerance

★ Refer to Portable Products Section for Product Data Sheet

Voltage Mode Controllers

Voltage Mode Controllers	UNITRODE PART NUMBER				
	UC3524 ∴	UC3524A	UC3525A	UC3525B	UC3526
Application	Fixed Frequency PWM, Off-line, DC-DC	Fixed Frequency PWM, Off-line, DC-DC	Fixed Frequency PWM, Off-line, DC-DC	Fixed Frequency PWM, Off-line, DC-DC	Fixed Frequency PWM, Off-line, DC-DC
Topology	Forward, Flyback, Buck, Boost	Forward, Flyback, Buck, Boost	Full Bridge, Half Bridge	Full Bridge, Half Bridge	Full Bridge, Half Bridge
Voltage Reference Tolerance	4%	1%	1%	0.75%	1%
Peak Output Current	100mA	200mA	400mA	200mA	100mA
Maximum Practical Operating Frequency	300kHz	500kHz	500kHz	500kHz	400kHz
Outputs	Dual Alternating, Uncommitted	Dual Alternating, Uncommitted	Dual Alternating, Totem Pole	Dual Alternating, Totem Pole	Dual Alternating, Totem Pole
Startup Current		4mA			
Voltage Feedforward					
Soft Start			Y	Y	Y
Maximum Duty Cycle	50%/50%	50%/50%	50%/50%	50%/50%	50%/50%
Separate Oscillator/ Synchronization Terminal	Y	Y	Y	Y	Y
Application/Design Note				DN-36	

Voltage Mode Controllers (cont'd)	UNITRODE PART NUMBER				
	UC3526A	UC3527A	UC3527B	UC3548 ✚	UCC3570
Application	Fixed Frequency PWM Off-line, DC-DC	Fixed Frequency PWM, Off-line, DC-DC	Fixed Frequency PWM, Off-line, DC-DC	Off-line, DC-DC	Wide Range, Off-line
Topology	Full Bridge, Half Bridge	Full Bridge, Half Bridge	Full Bridge, Half Bridge	Flyback, Forward	Forward, Flyback, Buck, Boost
Voltage Reference Tolerance	1%	1%	0.75%	1%	1%
Peak Output Current	100mA	400mA	200mA	2A	500mA
Maximum Practical Operating Frequency	550kHz	500kHz	500kHz	1MHz	500kHz
Outputs	Dual Alternating, Totem Pole	Dual Alternating, Totem Pole	Dual Alternating, Totem Pole	Single, Totem Pole	Single, Totem Pole
Startup Current				500µA	85µA
Voltage Feedforward				Y	Y
Soft Start	Y	Y	Y	Y	Y
Maximum Duty Cycle	50%/50%	50%/50%	50%/50%	Programmable	100%
Separate Oscillator/ Synchronization Terminal	Y	Y	Y		
Application/Design Note			DN-36		DN-65, U-150

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.

✚ New Product

∴ Does Not Feature UVLO

Voltage Mode Controllers

Voltage Mode Controllers (cont'd)	UNITRODE PART NUMBER				
	UC3572	UC3573	UC3578 +	UCC3580 + ◗	UCC3581 +
Application	Low Power, High Efficiency, Spot Regulator	Low Power, High Efficiency, Spot Regulator	DC-DC	Active Clamp/ Reset PWM	Off-line, Primary Side PWM for ISDN Applications
Topology	Negative Output Flyback	Buck	Buck	Forward, Flyback	Forward, Flyback
Voltage Reference Tolerance	2%	2%	2%	1.5%	1.5%
Peak Output Current	0.5A	0.5A	0.6A Source, 0.8A Sink	1A / 0.5A	1A
Maximum Practical Operating Frequency	300kHz	300kHz	100kHz Internal Oscillator	1MHz	100kHz
Outputs	Single, Totem Pole	Single, Totem Pole	Single, Floating Totem Pole	Dual Complementary, Totem Pole	Single, Totem Pole
Startup Current			N/A	50µA	100µA
Voltage Feedforward				Y	
Soft Start			Y	Y	Y
Maximum Duty Cycle	100%	100%	90%	Programmable	Programmable
Separate Oscillator/ Synchronization Terminal				Y	Y
Application/Design Note		DN-70			DN-65

Voltage Mode Controllers (cont'd)	UNITRODE PART NUMBER				
	UCC3582 +	UCC3583 +	UC3584 +	UC3823	UC3823A
Application	High Efficiency DC-DC	Secondary Side Post Regulation	DC-DC Secondary Side Synchronous Post Regulator	DC-DC	DC-DC
Topology	Synchronous Buck	Buck	Buck	Buck, Boost	Buck, Boost
Voltage Reference Tolerance	1.5%	1.5%	1%	1%	1%
Peak Output Current	0.5A	1.5A Source, 0.5A Sink	1.5A Source and Sink	1.5A	2A
Maximum Practical Operating Frequency	500kHz	500kHz	1MHz	1MHz	1MHz
Outputs	Dual Complementary, Totem Pole	Single, Totem Pole	Single, Totem Pole	Single, Totem Pole	Single, Totem Pole
Startup Current	15µA*	100µA	N/A	1.1mA	0.1mA
Voltage Feedforward	Y	N/A		Y	Y
Soft Start	Y	Y	Y	Y	Y
Maximum Duty Cycle	100%	95%	94%	100%	Programmable
Separate Oscillator/ Synchronization Terminal		Y	Y	Y	Y
Application/Design Note	DN-65			U-131	U-128

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.

+ New Product
◗ Does Not Feature Current Limiting
* Sleep Current

Voltage Mode Controllers

Voltage Mode Controllers (cont'd)	UNITRODE PART NUMBER				
	UC3823B	UC3824	UC3825	UC3825A	UC3825B
Application	Off-line	Synchronous Rectifier, Forward Converter	DC-DC	DC-DC	Off-line
Topology	Buck, Boost	Forward, Flyback	Push-pull, Full Bridge, Half Bridge	Push-pull, Full Bridge, Half Bridge	Push-pull, Full Bridge,Half Bridge
Voltage Reference Tolerance	1%	1%	1%	1%	1%
Peak Output Current	2A	1.5A	1.5A	2A	2A
Maximum Practical Operating Frequency	1MHz	1MHz	1MHz	1MHz	1MHz
Outputs	Single, Totem Pole	Dual Complementary, Totem Pole	Dual Alternating, Totem Pole	Dual Alternating, Totem Pole	Dual Alternating, Totem Pole
Startup Current	0.1mA	1.1mA	1.1mA	0.1mA	0.1mA
Voltage Feedforward	Y			Y	Y
Soft Start	Y	Y	Y	Y	Y
Maximum Duty Cycle	Programmable	100%	50%/50%	Programmable	Programmable
Separate Oscillator/ Synchronization Terminal	Y	Y	Y	Y	Y
Application/Design Note	U-128		U-110	U-128	U-128

Voltage Mode Controllers (cont'd)	UNITRODE PART NUMBER				
	UC3827 ✚	UCC3829 ✚	UC3841	UC3851	UC3875
Application	Multiple Output or High Voltage Output DC-DC Converters	Off-line, DC-DC	Primary Side, Programmable, Off-line, DC-DC	Off-line, Programmable, Primary Side Controller	Zero Voltage Transition, Phase Shifted Bridge
Topology	Buck Current Fed or Voltage Fed, Push-pull	Buck, Boost, Push-pull, Full Bridge, Half Bridge	Forward, Flyback, Buck, Boost	Forward, Flyback, Buck, Boost	Full Bridge
Voltage Reference Tolerance	4%	1%	1%	1%	1%
Peak Output Current	Floating 1A for Buck Stage, 0.8A For Push-pull Drivers	2.2A	1A	0.2A	2A
Maximum Practical Operating Frequency	500kHz	1MHz	500kHz	500kHz	1MHz
Outputs	Floating Buck, Push-pull	Dual Alternating, Totem Pole	Single, Open Collector	Single, Totem Pole	Quad Phase Shifted, Totem Pole
Startup Current	1mA	200µA	4.5mA		150µA
Voltage Feedforward	Y	Y	Y	Y	
Soft Start	Y	Y	Y	Y	Y
Maximum Duty Cycle	90% for Buck Stage, 50%/50% for Push-pull Stage	50%/50%	Programmable	50%	100%
Separate Oscillator/ Synchronization Terminal	Y	Y			Y
Application/Design Note		DN-65	DN-28	DN-28	DN-63, U-136

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
✚ New Product

Voltage Mode Controllers

Voltage Mode Controllers (cont'd)	UNITRODE PART NUMBER			
	UC3876	UC3877	UC3878	UC3879
Application	Zero Voltage Transition, Phase Shifted Bridge	Zero Voltage Transition, Phase Shifted Bridge	Zero Voltage Transition, Phase Shifted Bridge	Zero Voltage Transition, Phase Shifted Bridge
Topology	Full Bridge	Full Bridge	Full Bridge	Full Bridge
Voltage Reference Tolerance	1%	1%	1%	1%
Peak Output Current	2A	2A	2A	0.1A
Maximum Practical Operating Frequency	1MHz	1MHz	1MHz	300kHz
Outputs	Quad Phase Shifted, Totem Pole	Quad Phase Shifted, Totem Pole	Quad Phase Shifted, Totem Pole	Quad Phase Shifted, Totem Pole
Startup Current	150µA	150µA	150µA	150µA
Voltage Feedforward				
Soft Start	Y	Y	Y	Y
Maximum Duty Cycle	100%	100%	100%	100%
Separate Oscillator/ Synchronization Terminal	Y	Y	Y	Y
Application/Design Note	DN-63, U-136	DN-63, U-136	DN-63, U-136	DN-63, U-136, U-154

Voltage Mode Controllers (cont'd)	UNITRODE PART NUMBER		
	UCC3888 +	UCC3889	UCC3890 +
Application	Off-line Power Supply Controller	Off-line Power Supply Controller	Off-line Battery Charge Controller
Topology	Flyback	Flyback	Flyback
Voltage Reference Tolerance	3%	3%	4%
Peak Output Current	0.15A	0.15A	0.15A
Maximum Practical Operating Frequency	250kHz	250kHz	250kHz
Outputs	Single, Totem Pole	Single, Totem Pole	Single, Totem Pole
Startup Current	150µA	150µA	
Voltage Feedforward	Y	Y	Y
Soft Start			
Maximum Duty Cycle	55%	55%	N/A
Separate Oscillator/ Synchronization Terminal			
Application/Design Note	DN-59, U-149	DN-59, U-149	

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
+ New Product

Resonant Mode Controllers

Resonant Mode Controllers	UNITRODE PART NUMBER					
	UC3824	UC3852 ➤ ★	UC3855 ★	UC3860	UC3861	UC3862
Application	Synchronous Rectifier, Zero Voltage Transition, Forward	Power Factor Correction, Zero Current Transition	Power Factor Correction, Zero Voltage Transition	Off-line, DC-DC, Zero Current Switching	Off-line, Zero Voltage Switching	DC-DC and Battery, Zero Voltage Switching
Topology	Forward, Flyback	Boost	Boost	Half Bridge, Full Bridge	Half Bridge, Full Bridge	Forward, Flyback
Voltage Reference Tolerance	1%	7%	1%	1%	1%	1%
Peak Output Current	1.5A	0.5A	1.5A	2A	1A	1A
Maximum Practical Operating Frequency	1MHz	250kHz	500kHz	2MHz	1MHz	1MHz
Outputs	Dual Complementary, Totem Pole	Single	Dual Soft Switching, Totem Pole	Dual Programmable, Totem Pole	Dual Alternating, Totem Pole	Single, Totem Pole
Startup Current	1.1mA	1mA	150µA	300µA	150µA	150µA
Maximum Duty Cycle	100%	N/A	100%	Programmable	50%/50%	100%
Separate Oscillator/ Synchronization Terminal	Y	N/A	Y	Y		
Application/Design Note			U-153A		U-122, U-138	U-122, U-138

Resonant Mode Controllers (cont'd)	UNITRODE PART NUMBER					
	UC3863	UC3864	UC3865	UC3866	UC3867	UC3868
Application	DC-DC and Battery, Zero Voltage Switching	DC-DC and Battery, Zero Voltage Switching	Off-line, Zero Current Switching	Off-line, Zero Current Switching	DC-DC and Battery, Zero Current Switching	DC-DC and Battery, Zero Current Switching
Topology	Half Bridge, Full Bridge	Forward, Flyback	Half Bridge, Full Bridge	Forward, Flyback	Half Bridge, Full Bridge	Forward, Flyback
Voltage Reference Tolerance	1%	1%	1%	1%	1%	1%
Peak Output Current	1A	1A	1A	1A	1A	1A
Maximum Practical Operating Frequency	1MHz	1MHz	1MHz	1MHz	1MHz	1MHz
Outputs	Dual Alternating, Totem Pole	Single, Totem Pole	Dual Alternating, Totem Pole	Single, Totem Pole	Dual Alternating, Totem Pole	Single, Totem Pole
Startup Current	150µA	150µA	150µA	150µA	150µA	150µA
Voltage Feedforward	50%/50%	100%	50%/50%	100%	50%/50%	100%
Maximum Duty Cycle						
Separate Oscillator/ Synchronization Terminal						
Application/Design Note	U-122, U-138	U-122, U-138	U-122	U-122	U-122	U-122

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.

➤ Does Not Feature Soft Start

★ Refer to PFC Controllers Section for Product Data Sheet

Resonant Mode Controllers

Resonant Mode Controllers	UNITRODE PART NUMBER				
	UC3875	UC3876	UC3877	UC3878	UC3879
Application	Zero Voltage Transition, Phase Shifted Bridge	Zero Voltage Transition, Phase Shifted Bridge	Zero Voltage Transition, Phase Shifted Bridge	Zero Voltage Transition, Phase Shifted Bridge	Zero Voltage Transition, Phase Shifted Bridge
Topology	Full Bridge	Full Bridge	Full Bridge	Full Bridge	Full Bridge
Voltage Reference Tolerance	1%	1%	1%	1%	1%
Peak Output Current	2A	2A	2A	2A	0.1A
Maximum Practical Operating Frequency	1MHz	1MHz	1MHz	1MHz	300kHz
Outputs	Quad Phase Shifted, Totem Pole	Quad Phase Shifted, Totem Pole	Quad Phase Shifted, Totem Pole	Quad Phase Shifted, Totem Pole	Quad Phase Shifted, Totem Pole
Startup Current	150µA	150µA	150µA	150µA	150µA
Maximum Duty Cycle	100%	100%	100%	100%	100%
Separate Oscillator/ Synchronization Terminal	Y	Y	Y	Y	Y
Application/Design Note	DN-63, U-136	DN-63, U-136	DN-63, U-136	DN-63, U-136	DN-63, U-136, U-154

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.

Power Supply Support

Power Supply Support Products	UNITRODE PART NUMBER			
	UC2577	UC3610	UC3611	UC3612
Description	Simple Step-up Voltage Regulator	Dual Schottky Diode Bridge	Quad Schottky Diode Array	Dual Schottky Diode
Application	3 Amp Step-up Switching Regulator for Boost, Flyback, and Forward Converter Applications	Eight-diode Array for High Current, Low Duty Cycle Flyback Voltage Clamping for Inductive Loads	Four-diode Array for High Current Bridges and Voltage Clamps	Two-diode Array for High Current, Low Duty Cycle Flyback Voltage Clamping for Inductive Loads
Key Features	• Circuit Requires Few External Components • NPN Output Switches 3A • Current Mode Operation for Improved Response • Fixed and Adjustable Output Versions Available	• Monolithic Eight-diode Array • High Peak Current • Low Forward Voltage • Fast Recovery Time	• Matched, Four-diode Monolithic Array • High Peak Current • Low Forward Voltage • Parallelable for Higher Current or Lower Voltage Drop	• Monolithic Two-diode Array • High Peak Current • Low Forward Voltage • Fast Recovery Time
Application/Design Note	DN-49			

Power Supply Support Products (cont'd)	UNITRODE PART NUMBER		
	UCC3750 ✚	UCC3751	UCC3812 ✚
Description	Source Ringer Controller	Single Line Ring Generator Controller	12V Boost Regulator
Application	4 Quadrant Flyback Controller Develops High Voltage AC Output	Controls Low Cost Circuit for Generating High Voltage AC Output with DC Offset	12V Bias Supplies
Key Features	• On Chip Low THD Sinewave Reference, Pin Selectable 20Hz, 25Hz, and 50Hz • Programmable Output Amplitude and DC Offset • AC and DC Current Limiting With Short Circuit Protection	• Off-hook Detection With Automatic Transition to DC Operation • Pin Selectable 20Hz, 25Hz, and 50Hz Output Frequency • Operates From a Single 12V Supply • AC Current Limiting and Short Circuit Protection	• Fixed 12V Output • 3V to 5V Input Voltage • Minimal External Components Required

✚ New Product

Power Supply Support

Power Supply Support Products (cont'd)	UNITRODE PART NUMBER		
	UCC3831 + ★	UC3901	UC3902 +
Description	Universal Serial Bus Hub Power Controller	Isolated Feedback Generator	8-Pin Load Share Controller
Application	Powers Four 5V Peripherals and One 3.3V USB Controller	Amplitude Modulation System Used to Couple a Control Signal Across a Voltage Isolation Barrier	Allows Multiple Independent Power Supplies to be Paralleled so that Each Unit Supplies Only its Proportional Share of Total Load Current
Key Features	• Fully USB Compliant • Separate Power Enables • 500mA Current Limit for Each 5V Output • 100mA Current Limit for 3.3V Output • 6V to 9V Input Voltage Range	• Transformer Couples Isolated Feedback Error Signal • Low Cost Alternative to Optical Couplers • 5MHz Carrier Provides Fast Response Capability • Modulator Synchronizable to an External Clock	• Highly Tolerant of Voltage Differences Between Power Supply Returns • 2.7V to 20V Operation • High Gain, Low Offset Current Sense Amplifier Permits Low Shunt Resistor Values • Single Capacitor Sets Load Share Filter Response
Application/Design Note		DN-19, DN-33, U-94	U-163

Power Supply Support Products (cont'd)	UNITRODE PART NUMBER		
	UC3907	UC3908	UC3910 +
Description	Load Share Controller	Voltage Clamp	Reference, 4-bit DAC and Fault Monitor
Application	Allows Multiple Independent Power Supplies to be Paralleled so that Each Unit Supplies Only its Proportional Share of Total Load Current	Protects a Power Supply Load in the Event of an Overvoltage	Sets Control Voltage for UC3886, UC3870 and other Precision PWMS
Key Features	• Fully Differential High Impedance Voltage Sensing • Accurate Current Amplifier for Precise Load Sharing • Optocoupler Driving Capability • 4.5V to 35V Operation	• Shunt Regulator Keeps Power Supply Overvoltage to a Predetermined Level by Clamping the Power Supply Output • Programmable Input Voltage from 3V to 10V • Up to 10A Shunt Regulator Automatically Activated • Gate Drive to External SCR Provided if Fault Persists	• 4-bit DAC Sets Output Voltage of PWM, Meets Intel VID Code • 1% Combined Reference and DAC Tolerance • Over and Under Voltage Monitoring and Protection
Application/Design Note	U-129	DN-69	U-157, U-158

+ New Product
★ Refer to Linear Regulator Section for Product Data Sheet

Power Supply Support Products, Supply Monitors & Active Clamps & Special Function

Power Supply Support Products (cont'd)	UNITRODE PART NUMBER		
	UC39431	UC39432	UC3965 +
Description	Precision Adjustable Shunt Regulator	Precision Analog Controller	Precision Reference with Low Offset Error Amplifier
Application	Adjustable 100mA Shunt Regulator, Voltage Reference Optocoupler Driver, Voltage to Current Converter	Adjustable 100mA Shunt Regulator, Optocoupler Driver, Programmable Transconductance Voltage to Current Converter	Used for High Precision PWM Switching Regulators
Key Features	• Multiple On-chip Programmable Reference Voltages • 2.2V to 36V Operating Supply Voltage and User Programmable Reference • Linear Transconductance for Optocoupler Feedback Applications	• Programmable, Linear Transconductance for Optimum Optocoupler Current Drive • Precision Reference and Error Amplifier Inputs Externally Available • 2.2V to 36V Operating Supply Voltage and User Programmable Reference	• 2.5V Precision Reference with 0.4% Accuracy • Low 1mV Offset Error Amplifier • 2X Inverting Amplifier/Buffer Output • Drivers Optocoupler Diode for Isolated Applications
Application/Design Note		DN-52	

Supply Monitors & Active Clamps	UNITRODE PART NUMBER					
	UC3543	UC3544	UC3903	UC3904	UC3908	UC3910 +
Power Supply Monitor	Single	Single	Quad	Quad		Single
Voltage Clamp					Single	
Voltage Range	5V to 35V	5V to 35V	8V to 40V	4.75V to 18V	3V to 10V	8V to 12V
Window Adjust	N	N	Y	Y	N	Y
Current Range					0A to 10A	
Current Limit	Y	Y	N	N	N	N
Programmable Threshold	Y	Y	Y	Y	Y	Y
Programmable Time Delay	Y	Y	Y	Y	N	Y
Application/Design Note			DN-33		DN-69	U-157, U-158

Special Function Circuits	UNITRODE PART NUMBER			
	UC161A/B/C	UC3730	UC3838A	UC494/5A,AC
Part Name	Quad Micropower Comparator	Thermal Monitor	Mag-Amp Controller	PWM
Description	Contains Four High Gain, Programmable Speed CMOS Compatible Comparators with Microwatt Operation	Combines a Temperature Transducer, Precision Reference, and Temperature Comparator for Maximum System Flexibility	Dual Op-amps and 1% Reference with –120V Reset Driver for Magnetic Amplifier Control Applications	Versatile PWM Featuring Dual 40V "Floating" Output Transistors and Dual Error Amplifiers for Single and Dual Ended Uses
Application/Design Note			DN-47, U-109	DN-38

+ New Product

Micropower Quad Comparator

FEATURES

- Programmable Output Drive Capability
- Direct CMOS Logic Compatibility
- Low Power
- Direct Wire-OR of Outputs
- Wide Input Common Mode Range

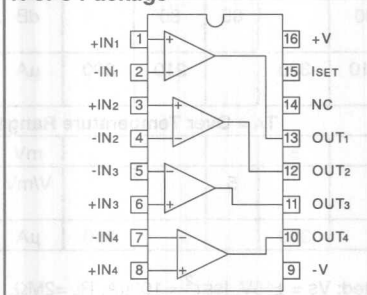
DESCRIPTION

The UC161 family of quad comparators feature programmable DC and AC parameters. A single external resistor can set the comparators to operate in the microwatt region for battery applications, or higher current levels can be set to obtain improved speed or drive capabilities. The outputs on these devices can be wire OR'd together, simplifying external logic requirements in some applications.

These devices are available in three temperature ranges, the UC161A is specified for the full military range, -55° C to +125°C, the UC161B for the industrial range, -25°C to +85°C, and the UC161C for the commercial range of 0°C to +70°C.

CONNECTION DIAGRAM

DIL-16 (TOP VIEW)
N or J Package

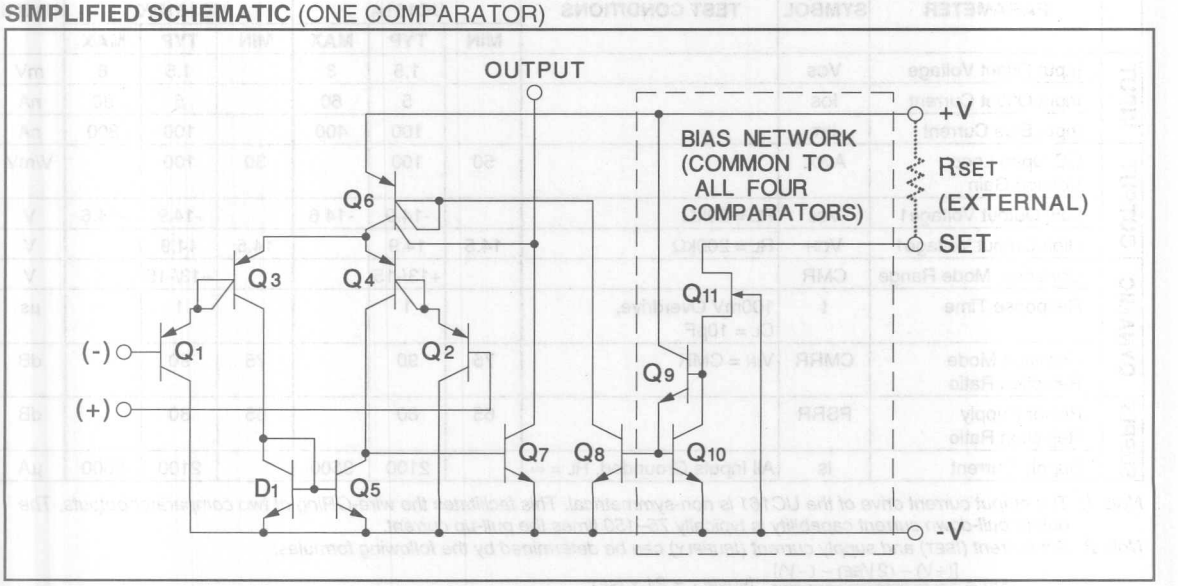


ABSOLUTE MAXIMUM RATINGS

Supply Voltage (+V to -V)	36V
Differential Input Voltage	±30V
Input Voltage	–V–0.3V to +V
Power Dissipation at T_A = 25°C	1000 mW
Power Dissipation at T_C = 25°C	2000 mW
Operating Junction Temperature	-55°C to +150°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 10 Sec.)	+300°C

Note: Consult Packaging Section of Databook for thermal limitations and considerations of package.

SIMPLIFIED SCHEMATIC (ONE COMPARATOR)



ELECTRICAL CHARACTERISTICS: Temperature range is -55° to +125°C for the UC161A, -25°C to +85°C for the UC161B, and 0°C to +70°C for the UC161C.

LOW POWER ELECTRICAL CHARACTERISTICS: Unless Otherwise Stated: $V_S = \pm 3V$, $I_{SET}^2 = 10\mu A$, $R_2 = 10M\Omega$, $C_L = 10pF$, $T_A = 25°C$, $T_A = T_J$.

	PARAMETER	SYMBOL	TEST CONDITIONS	UC161A			UC161B/C			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
INPUT	Input Offset Voltage	V_{OS}			1	3		1	6	mV
INPUT	Input Offset Current	I_{OS}			1	20		1	25	nA
INPUT	Input Bias Current	I_{BT}			20	100		20	200	nA
OUTPUT	DC Open Loop Voltage Gain	A_{VOL}		20	30		10	30		V/mV
OUTPUT	Low Output Voltage[1]	V_{OL}	$R_L = 20k\Omega$		-2.95	-2.6		-2.95	-2.6	V
OUTPUT	High Output Voltage[1]	V_{OH}	$R_L = 200k\Omega$	2.5	2.9		2.5	2.9		V
DYNAMIC	Common Mode Range	CMR			+1.3/-3			+1.3/-3		V
DYNAMIC	Response Time	t	100mV Overdrive, $C_L = 10pF$		5			5		µs
DYNAMIC	Common Mode Rejection Ratio	CMRR	V_{IN} = CMR	75	90		75	90		dB
SUPPLY	Power Supply Rejection Ratio	PSRR		65	80		65	80		dB
SUPPLY	Supply Current	Is	All Inputs Grounded, $R_L = \infty$		210	300		210	300	µA
										T_A = Over Temperature Range
	Input Offset Voltage	V_{OS}				5				mV
	DC Open Loop Voltage Gain	A_{VOL}		10			5			V/mV
	Supply Current	Is	All Inputs Grounded, $R_L = \infty$			350			350	µA

HIGH POWER ELECTRICAL CHARACTERISTICS: Unless Otherwise Stated: $V_S = \pm 15V$, $I_{SET}^2 = 100\mu A$, $R_L = 2M\Omega$, $C_L = 10pF$, $T_A = 25°C$, $T_A = T_J$.

	PARAMETER	SYMBOL	TEST CONDITIONS	UC161A			UC161B/C			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
INPUT	Input Offset Voltage	V_{OS}			1.5	3		1.5	6	mV
INPUT	Input Offset Current	I_{OS}			5	60		5	90	nA
INPUT	Input Bias Current	I_{BT}			100	400		100	800	nA
OUTPUT	DC Open Loop Voltage Gain	A_{VOL}		50	100		30	100		V/mV
OUTPUT	Low Output Voltage1	V_{OL}	$R_L = 20k\Omega$		-14.9	-14.6		-14.9	-14.6	V
OUTPUT	High Output Voltage1	V_{OH}	$R_L = 200k\Omega$	14.5	14.9		14.5	14.9		V
DYNAMIC	Common Mode Range	CMR			+13/-15			+13/-15		V
DYNAMIC	Response Time	t	100mV Overdrive, $C_L = 10pF$		1			1		µs
DYNAMIC	Common Mode Rejection Ratio	CMRR	V_{IN} = CMR	75	90		75	90		dB
SUPPLY	Power Supply Rejection Ratio	PSRR		65	80		65	80		dB
SUPPLY	Supply Current	Is	All Inputs Grounded, $R_L = \infty$		2100	3500		2100	3500	µA

Note 1: The output current drive of the UC161 is non-symmetrical. This facilitates the wire-ORing of two comparator outputs. The output pull-down current capability is typically 75–150 times the pull-up current.

Note 2: Set current (I_{SET}) and supply current (I_{SUPPLY}) can be determined by the following formulas:

$$I_{SET} = \frac{[(+V) - (2V_{BE}) - (-V)]}{R_{SET}} : I_{SUPPLY} = 21 \times I_{SET}.$$

HIGH POWER ELECTRICAL CHARACTERISTICS (Continued): $T_A = T_J$.

T_A = Over Temperature Range

	PARAMETER	SYMBOL	TEST CONDITIONS	UC161A			UC161B/C			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
	Input Offset Voltage	V_{OS}				6				mV
	Input Bias Current	I_{BT}				500				nA
	DC Open Loop Voltage Gain	A_{VOL}		25			15			V/mV
	Supply Current	I_S	All Inputs Grounded $R_L = \infty$			4000			4000	µA

Note 1: The output current drive of the UC161 is non-symmetrical. This facilitates the wire-ORing of two comparator outputs. The output pull-down current capability is typically 75–150 times the pull-up current.

Note 2: Set current (I_{SET}) and supply current (I_{SUPPLY}) can be determined by the following formulas:

$$I_{SET} = \frac{[(+V) - (2V_{BE}) - (-V)]}{R_{SET}} : I_{SUPPLY} = 21 \times I_{SET}.$$

APPLICATION AND OPERATION INFORMATION DESCRIPTION

The UC161 is a monolithic quad micropower comparator with an external control for varying its AC and DC characteristics. The variation of a single programming resistor will simultaneously alter parameters such as supply current, input bias, current slew rate, output drive capability, and gain. By making this resistor large, operation at very small supply current levels and power dissipations is possible. The UC161 is therefore ideal for systems requiring minimum power drain, such as battery-powered instrumentation, aerospace systems, CMOS designs, and remote security systems.

The circuit (see Simplified Schematic) is composed of five major blocks–four comparators and a common bias network. Q_1-Q_6, and D_1 from a darlington differential amplifier with double-to-single ended conversion. Q_6 is a dual current source whose outputs are exactly twice the current flowing through Q_8. The collector current of Q_8 is a function of the current supplied externally to Q_9-Q_{10}, which in turn is known as the set current of I_{SET}. This set current is established by a resistor connected between the I_{SET} terminal and a voltage source, most commonly the positive supply. Q_{11} prevents excessive current from flowing through Q_9 and Q_{10} in the event the I_{SET} terminal is shorted to the positive supply; it has no effect on circuit operation under normal conditions.

SETTING THE SET CURRENT

The set current can be expressed as:

$$I_{SET} = \frac{[(+V) - (2V_{BE}) - (-V)]}{R_{SET}}$$

where +V is the voltage to which the control resistor is connected, -V is the negative supply voltage, V_{BE} is the base emitter drop of Q_9 or Q_{10} (about 0.7V), and R_{SET} is the value of the external control resistor or set resistor. Equation 1 is simply a derivative of ohms law. There is also an analytical relationship between I_{SET} and the total supply current:

I_{SUPPLY} = [I_{SET} *(current sourced by Q_6 to Q_8)*

+2 I_{SET} (current sourced to the differential amplifier by Q_6)

+2 I_{SET} (current sourced to the comparator output by Q_6)

× 4 (the total number of comparators)

+ I_{SET} (current sourced through Q_{11}, Q_{10}, and Q_9 to –V)

$= [I_{SET} + 2\ I_{SET} + 2\ I_{SET}] \times 4 + I_{SET}$

$= 21\ I_{SET}$

The output current pulldown capability (I_{OL}) of the UC161 is about 2 orders of magnitude greater than the high output drive current, (I_{OH}), which allows wire-ORing the outputs. I_{OH} is simply the current sourced by Q_6:

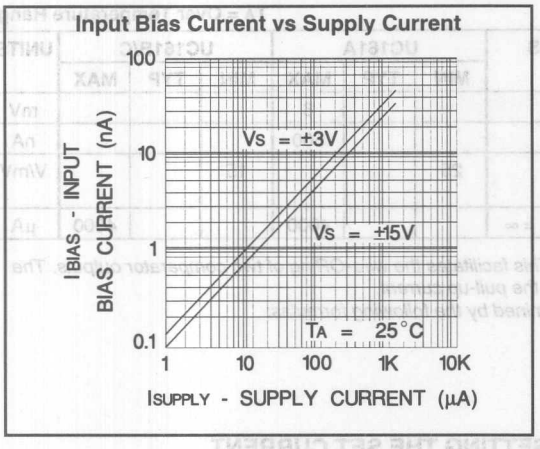
$$I_{OH} = 2 \times I_{SET}$$

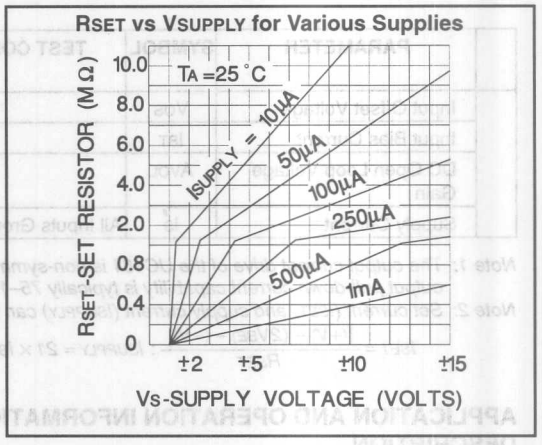
I_{OL} is found by multiplying the current sourced by the collector of Q_6 by the gain Q_7:

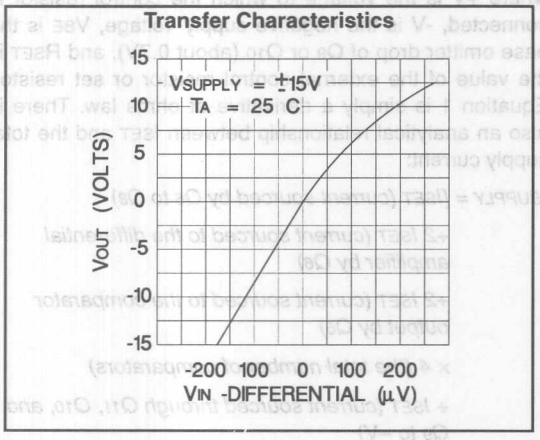
$$I_{OL} = \beta\ (Q_7) \times 2\ I_{SET}$$

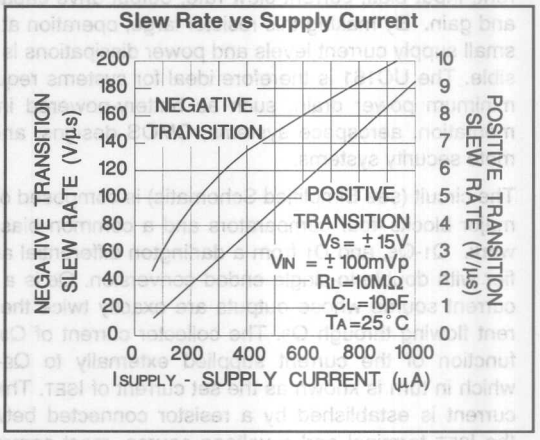
The beta of Q_7 is about 75–150.

APPLICATION AND OPERATION INFORMATION (Continued)









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UNITRODE

Simple Step-Up Fixed Voltage Regulators

FEATURES

- Requires Few External Components
- NPN Output Switches 3.0A, 65V(max)
- Extended Input Voltage Range: 3.0V to 40V
- Current Mode Operation for Improved Transient Response, Line Regulation, and Current Limiting
- Soft Start Function Provides Controlled Startup
- 52kHz Internal Oscillator
- Output Switch Protected by Current Limit, UVLO and Thermal Shutdown
- Improved Replacement for LM2577 Series

DESCRIPTION

The UC2577 family of devices provides all the active functions necessary to implement step-up (boost), flyback, and forward converter switching regulators. Requiring only a few components, these simple regulators efficiently provide fixed output voltages of 12V or 15V as step-up regulators.

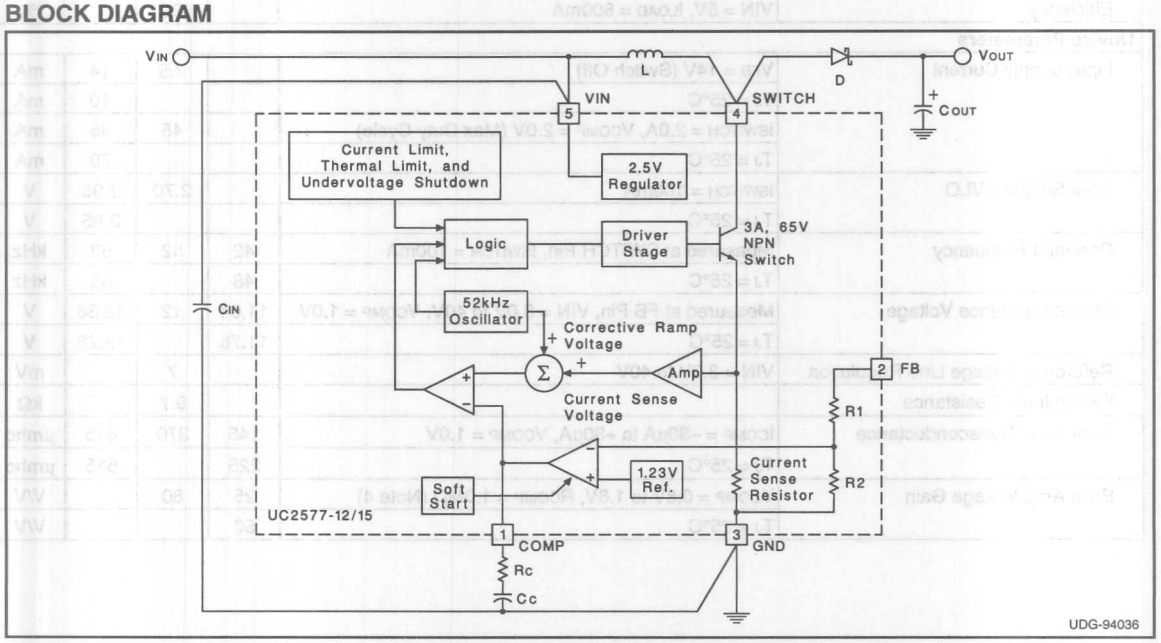
The UC2577 series features a wide input voltage range of 3.0V to 40V. An on-chip 3.0A NPN switch is included with undervoltage lockout, thermal protection circuitry, and current limiting, as well as soft start mode operation to reduce current during startup. Other features include a 52kHz fixed frequency on-chip oscillator with no external components and current mode control for better line and load regulation.

For Applications Information, see the UC2577-ADJ data sheet, Design Note DN-48 "Versatile Low Power SEPIC Converter Accepts Wide Input Voltage Range", and Design Note DN-49 "UC2577 Easy Switcher Controls SEPIC Converter for Automotive Applications".

TYPICAL APPLICATIONS

- Simple Boost and Flyback Converters
- Transformer Coupled Forward Regulators
- SEPIC Topology Permits Input Voltage to be Higher or Lower than Output Voltage
- Multiple Output Designs

BLOCK DIAGRAM



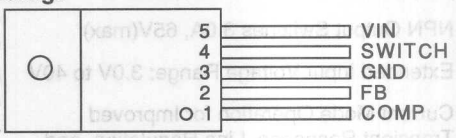
UC2577-12

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage 45V
Output Switch Voltage 65V
Output Switch Current (Note 2) 6.0A
Power Dissipation ..... Internally Limited
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... 260°C
Maximum Junction Temperature ..... 150°C
Minimum ESD Rating (C = 100pF, R = 1.5kΩ) 2kV

CONNECTION DIAGRAM

5-Pin TO-220 (Top View)
T Package



Also available in TO-263 Package (TD).

RECOMMENDED OPERATING RANGE

Supply Voltage ..... 3.0V ≤ VIN ≤ 40V
Output Switch Voltage ..... 0V ≤ VSWITCH ≤ 60V
Output Switch Current ..... ISWITCH ≤ 3.0A
Junction Temperature Range ..... −40°C ≤ TJ ≤ +125°C

ORDERING INFORMATION

UC2577T-12	5 Pin TO-220 Plastic Package
UC2577T-15	5 Pin TO-220 Plastic Package
UC2577TD-12	5 Pin TO-263 Plastic Package
UC2577TD-15	5 Pin TO-263 Plastic Package

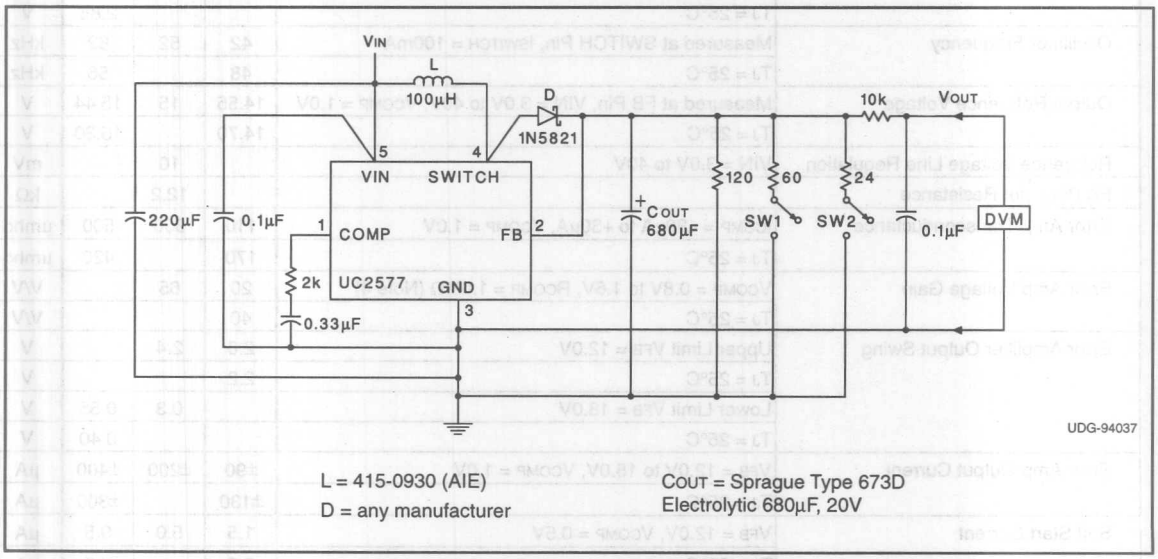
ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply for TA = −40°C to +125°C, VIN = 5V, ISWITCH = 0, and TA = TJ.

		UC2577-12			
PARAMETER	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
System Parameters *Circuit Figure 1* (Note 3)					
Output Voltage	VIN = 5V to 10V, ILOAD = 100mA to 800mA	11.40	12.0	12.60	V
	TJ = 25°C	11.60		12.40	V
Line Regulation	VIN = 3.0V to 12V, ILOAD = 300mA		20	100	mV
	TJ = 25°C			50	mV
Load Regulation	VIN = 5V, ILOAD = 100mA to 800mA		20	100	mV
	TJ = 25°C			50	mV
Efficiency	VIN = 5V, ILOAD = 800mA		80		%
Device Parameters					
Input Supply Current	VFB = 14V (Switch Off)		7.5	14	mA
	TJ = 25°C			10	mA
	ISWITCH = 2.0A, VCOMP = 2.0V (Max Duty Cycle)		45	85	mA
	TJ = 25°C			70	mA
Input Supply UVLO	ISWITCH = 100mA		2.70	2.95	V
	TJ = 25°C			2.85	V
Oscillator Frequency	Measured at SWITCH Pin, ISWITCH = 100mA	42	52	62	kHz
	TJ = 25°C	48		56	kHz
Output Reference Voltage	Measured at FB Pin, VIN = 3.0V to 40V, VCOMP = 1.0V	11.64	12	12.36	V
	TJ = 25°C	11.76		12.26	V
Reference Voltage Line Regulation	VIN = 3.0V to 40V		7		mV
FB Pin Input Resistance			9.7		kΩ
Error Amp Transconductance	ICOMP = −30µA to +30µA, VCOMP = 1.0V	145	370	615	µmho
	TJ = 25°C	225		515	µmho
Error Amp Voltage Gain	VCOMP = 0.8V to 1.6V, RCOMP = 1.0MΩ (Note 4)	25	80		V/V
	TJ = 25°C	50			V/V

ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for T_A = –40°C to +125°C, VIN = 5V, I_{SWITCH} = 0, and T_A = T_J.

		UC2577-12			
PARAMETER	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Device Parameters (cont.)					
Error Amplifier Output Swing	Upper Limit V_{FB} = 10.0V	2.0	2.4		V
	T_J = 25°C	2.2			V
	Lower Limit V_{FB} = 15.0V		0.3	0.55	V
	T_J = 25°C			0.40	V
Error Amp Output Current	V_{FB} = 10.0V to 15.0V, V_{COMP} = 10.0V	±90	±200	±400	µA
	T_J = 25°C	±130		±300	µA
Soft Start Current	V_{FB} = 10.0V, V_{COMP} = 0.5V	1.5	5.0	9.5	µA
	T_J = 25°C	2.5		7.5	µA
Maximum Duty Cycle	V_{COMP} = 1.5V, I_{SWITCH} = 100mA	90	95		%
	T_J = 25°C	93			%
Switch Transconductance			12.5		A/V
Switch Leakage Current	V_{SWITCH} = 65V, V_{FB} = 1.5V (Switch Off)		10	600	µA
	T_J = 25°C			300	µA
Switch Saturation Voltage	I_{SWITCH} = 2.0A, V_{COMP} = 2.0V (Max Duty Cycle)		0.5	0.9	V
	T_J = 25°C			0.7	V
NPN Switch Current Limit	V_{COMP} = 2.0V	3.0	4.3	6.0	A
Thermal Resistance	Junction to Ambient		65		°C/W
	Junction to Case		2		°C/W
COMP Pin Current	V_{COMP} = 0		25	50	µA
	T_J = 25°C			40	µA



L = 415-0930 (AIE)
D = any manufacturer

C_{OUT} = Sprague Type 673D
Electrolytic 680µF, 20V

Figure 1. Circuit Used to Specify System Parameters

UC2577-15

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage 45V
Output Switch Voltage 65V
Output Switch Current (Note 2) 6.0A
Power Dissipation . . . . . Internally Limited
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . 260°C
Maximum Junction Temperature . . . . . 150°C
Minimum ESD Rating (C = 100pF, R = 1.5kΩ) 2kV

RECOMMENDED OPERATING RANGE

Supply Voltage . . . . . 3.0V ≤ VIN ≤ 40V
Output Switch Voltage . . . . . 0V ≤ VSWITCH ≤ 60V
Output Switch Current . . . . . ISWITCH ≤ 3.0A
Junction Temperature Range . . . . . −40°C ≤ TJ ≤ +125°C

See Page 2 of this data sheet for Connection Diagram and Ordering Information.

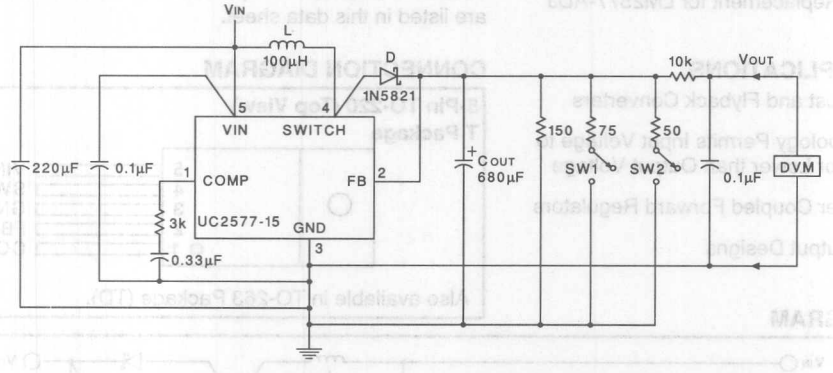
ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply for TA = −40°C to +125°C, VIN = 5V, ISWITCH = 0, and TA = TJ.

		UC2577-15			
PARAMETER	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
System Parameters *Circuit Figure 2* (Note 3)					
Output Voltage	VIN = 5V to 12V, ILOAD = 100mA to 600mA	14.25	15.0	15.75	V
	TJ = 25°C	14.50		15.50	V
Line Regulation	VIN = 3.0V to 12V, ILOAD = 300mA		20	100	mV
	TJ = 25°C			50	mV
Load Regulation	VIN = 5V, ILOAD = 100mA to 600mA		20	100	mV
	TJ = 25°C			50	mV
Efficiency	VIN = 5V, ILOAD = 600mA		80		%
Device Parameters					
Input Supply Current	VFB = 1.5V (Switch Off)		7.5	14	mA
	TJ = 25°C			10	mA
	ISWITCH = 2.0A, VCOMP = 2.0V (Max Duty Cycle)		45	85	mA
	TJ = 25°C			70	mA
Input Supply UVLO	ISWITCH = 100mA		2.70	2.95	V
	TJ = 25°C			2.85	V
Oscillator Frequency	Measured at SWITCH Pin, ISWITCH = 100mA	42	52	62	kHz
	TJ = 25°C	48		56	kHz
Output Reference Voltage	Measured at FB Pin, VIN = 3.0V to 40V, VCOMP = 1.0V	14.55	15	15.44	V
	TJ = 25°C	14.70		15.30	V
Reference Voltage Line Regulation	VIN = 3.0V to 40V		10		mV
FB Pin Input Resistance			12.2		kΩ
Error Amp Transconductance	ICOMP = −30µA to +30µA, VCOMP = 1.0V	110	300	500	µmho
	TJ = 25°C	170		420	µmho
Error Amp Voltage Gain	VCOMP = 0.8V to 1.6V, RCOMP = 1.0MΩ (Note 4)	20	65		V/V
	TJ = 25°C	40			V/V
Error Amplifier Output Swing	Upper Limit VFB = 12.0V	2.0	2.4		V
	TJ = 25°C	2.2			V
	Lower Limit VFB = 18.0V		0.3	0.55	V
	TJ = 25°C			0.40	V
Error Amp Output Current	VFB = 12.0V to 18.0V, VCOMP = 1.0V	±90	±200	±400	µA
	TJ = 25°C	±130		±300	µA
Soft Start Current	VFB = 12.0V, VCOMP = 0.5V	1.5	5.0	9.5	µA
	TJ = 25°C	2.5		7.5	µA
Maximum Duty Cycle	VCOMP = 1.5V, ISWITCH = 100mA	90	95		%
	TJ = 25°C	93			%

ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for T_A = –40°C to +125°C, VIN = 5V, I_{SWITCH} = 0, and T_A = T_J.

		UC2577-15			
PARAMETER	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Device Parameters (cont.)					
Switch Transconductance			12.5		A/V
Switch Leakage Current	V_{SWITCH} = 65V, V_{FB} = 1.5V (Switch Off)		10	600	µA
	T_J = 25°C			300	µA
Switch Saturation Voltage	I_{SWITCH} = 2.0A, V_{COMP} = 2.0V (Max Duty Cycle)		0.5	0.9	V
	T_J = 25°C			0.7	V
NPN Switch Current Limit	V_{COMP} = 2.0V	3.0	4.3	6.0	A
Thermal Resistance	Junction to Ambient		65		°C/W
	Junction to Case		2		°C/W
COMP Pin Current	V_{COMP} = 0		25	50	µA
	T_J = 25°C			40	µA



L = 415-0930 (AIE)*
D = any manufacturer

C_{OUT} = Sprague Type 673D
Electrolytic 680µF, 20V

Figure 2. Circuit Used to Specify System Parameters

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating ratings indicate conditions during which the device is intended to be functional, but device parameter specifications may not be guaranteed under these conditions. For guaranteed specifications and test conditions, see the Electrical Characteristics.

Note 2: Output current cannot be internally limited when the UC2577 is used as a step-up regulator. To prevent damage to the switch, its current must be externally limited to 6.0A. However, output current is internally limited when the UC2577 is used as a flyback or forward converter regulator.

Note 3. External components such as the diode, inductor, input and output capacitors can affect switching regulator performance. When the UC2577 is used as shown in the Test Circuit, system performance will be as specified by the system parameters.

Note 4: A 1.0MΩ resistor is connected to the compensation pin (which is the error amplifier's output) to ensure accuracy in measuring A_{VOL}. In actual applications, this pin's load resistance should be ≥ 10MΩ, resulting in A_{VOL} that is typically twice the guaranteed minimum limit.

**(AIE) is AIE Magnetics, Div. Vernitron Corp., 2801 72nd Street North, St. Petersburg, FL 33710. Tel. (813) 347-2181*

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UNITRODE

Simple Step-Up Voltage Regulator

FEATURES

- Requires Few External Components
- NPN Output Switches 3.0A, 65V(max)
- Extended Input Voltage Range: 3.0V to 40V
- Current Mode Operation for Improved Transient Response, Line Regulation, and Current Limiting
- Soft Start Function Provides Controlled Startup
- 52kHz Internal Oscillator
- Output Switch Protected by Current Limit, Undervoltage Lockout and Thermal Shutdown
- Improved Replacement for LM2577-ADJ Series

TYPICAL APPLICATIONS

- Simple Boost and Flyback Converters
- SEPIC Topology Permits Input Voltage to be Higher or Lower than Output Voltage
- Transformer Coupled Forward Regulators
- Multiple Output Designs

DESCRIPTION

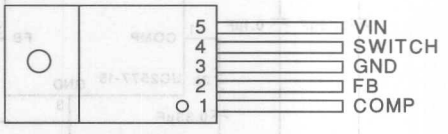
The UC2577-ADJ device provides all the active functions necessary to implement step-up (boost), flyback, and forward converter switching regulators. Requiring only a few components, these simple regulators efficiently provide up to 60V as a step-up regulator, and even higher voltages as a flyback or forward converter regulator.

The UC2577-ADJ features a wide input voltage range of 3.0V to 40V and an adjustable output voltage. An on-chip 3.0A NPN switch is included with undervoltage lockout, thermal protection circuitry, and current limiting, as well as soft start mode operation to reduce current during startup. Other features include a 52kHz fixed frequency on-chip oscillator with no external components and current mode control for better line and load regulation.

A standard series of inductors and capacitors are available from several manufacturers optimized for use with these regulators and are listed in this data sheet.

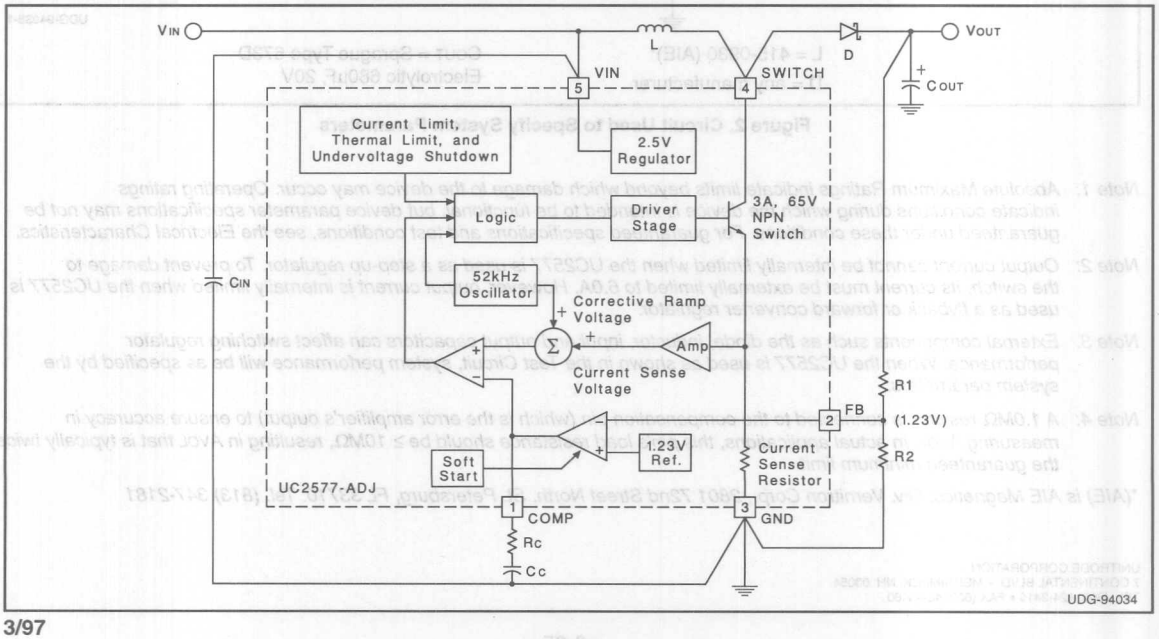
CONNECTION DIAGRAM

5-Pin TO-220 (Top View)
T Package



Also available in TO-263 Package (TD).

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage 45V
Output Switch Voltage 65V
Output Switch Current (Note 2) 6.0A
Power Dissipation . . . . . Internally Limited
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . 260°C
Maximum Junction Temperature . . . . . 150°C
Minimum ESD Rating (C = 100pF, R = 15kΩ) 2kV

RECOMMENDED OPERATING RANGE

Supply Voltage . . . . . 3.0V ≤ VIN ≤ 40V
Output Switch Voltage . . . . . 0V ≤ VSWITCH ≤ 60V
Output Switch Current . . . . . ISWITCH ≤ 3.0A
Junction Temperature Range . . . . . –40°C ≤ TJ ≤ +125°C

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply for TA = –40°C to +125°C, VIN = 5V, VFB = VREF, ISWITCH = 0, and TA = TJ.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
System Parameters *Circuit Figure 1* (Note 3)					
Output Voltage	VIN = 5V to 10V, ILOAD = 100mA to 800mA	11.40	12.0	12.60	V
	TJ = 25°C	11.60		12.40	V
Line Regulation	VIN = 3.0V to 10V, ILOAD = 300mA		20	100	mV
	TJ = 25°C			50	mV
Load Regulation	VIN = 5V, ILOAD = 100mA to 800mA		20	100	mV
	TJ = 25°C			50	mV
Efficiency	VIN = 5V, ILOAD = 800mA		80		%
Device Parameters					
Input Supply Current	VFB = 1.5V (Switch Off)		7.5	14	mA
	TJ = 25°C			10	mA
	ISWITCH = 2.0A, VCOMP = 2.0V (Max Duty Cycle)		45	85	mA
	TJ = 25°C			70	mA
Input Supply UVLO	ISWITCH = 100mA		2.70	2.95	V
	TJ = 25°C			2.85	V
Oscillator Frequency	Measured at SWITCH Pin, ISWITCH = 100mA	42	52	62	kHz
	TJ = 25°C	48		56	kHz
Reference Voltage	Measured at FB Pin, VIN = 3.0V to 40V, VCOMP = 1.0V	1.206	1.230	1.254	V
	TJ = 25°C	1.214		1.246	V
Reference Voltage Line Regulation	VIN = 3.0V to 40V		0.5		mV
Error Amp Input Bias Current	VCOMP = 1.0V		100	800	nA
	TJ = 25°C			300	nA
Error Amp Transconductance	ICOMP = –30µA to +30µA, VCOMP = 1.0V	1600	3700	5800	µmho
	TJ = 25°C	2400		4800	µmho
Error Amp Voltage Gain	VCOMP = 0.8V to 1.6V, RCOMP = 1.0MW (Note 4)	250	800		V/V
	TJ = 25°C	500			V/V
Error Amplifier Output Swing	Upper Limit VFB = 1.0V	2.0	2.4		V
	TJ = 25°C	2.2			V
	Lower Limit VFB = 1.5V		0.3	0.55	V
	TJ = 25°C			0.40	V
Error Amp Output Current	VFB = 1.0V to 1.5V, VCOMP = 1.0V	±90	±200	±400	µA
	TJ = 25°C	±130		±300	µA
Soft Start Current	VFB = 1.0V, VCOMP = 0.5V	1.5	5.0	9.5	µA
	TJ = 25°C	2.5		7.5	µA
Maximum Duty Cycle	VCOMP = 1.5V, ISWITCH = 100mA	90	95		%
	TJ = 25°C	93			%

ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for T_A = –40°C to +125°C, VIN = 5V, V_{FB} = V_{REF}, I_{SWITCH} = 0, and T_A = T_J.

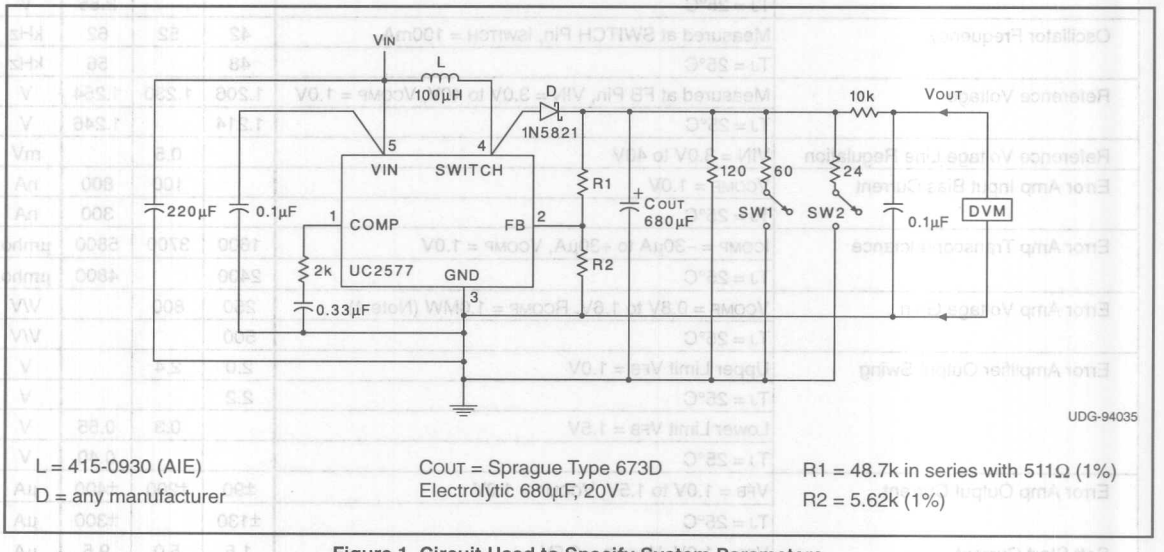
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Device Parameters (cont.)					
Switch Transconductance			12.5		A/V
Switch Leakage Current	V_{SWITCH} = 65V, V_{FB} = 1.5V (Switch Off)		10	600	µA
	T_J = 25°C			300	µA
Switch Saturation Voltage	I_{SWITCH} = 2.0A, V_{COMP} = 2.0V (Max Duty Cycle)		0.5	0.9	V
	T_J = 25°C			0.7	V
NPN Switch Current Limit	V_{COMP} = 2.0V	3.0	4.3	6.0	A
Thermal Resistance	Junction to Ambient		65		°C/W
	Junction to Case		2		°C/W
COMP Pin Current	V_{COMP} = 0		25	50	µA
	T_J = 25°C			40	µA

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating ratings indicate conditions during which the device is intended to be functional, but device parameter specifications may not be guaranteed under these conditions. For guaranteed specifications and test conditions, see the Electrical Characteristics.

Note 2: Output current cannot be internally limited when the UC2577 is used as a step-up regulator. To prevent damage to the switch, its current must be externally limited to 6.0A. However, output current is internally limited when the UC2577 is used as a flyback or forward converter regulator.

Note 3. External components such as the diode, inductor, input and output capacitors can affect switching regulator performance. When the UC2577 is used as shown in the Test Circuit, system performance will be as specified by the system parameters.

Note 4: A 1.0MΩ resistor is connected to the compensation pin (which is the error amplifier's output) to ensure accuracy in measuring A_{VOL}. In actual applications, this pin's load resistance should be ≥ 10MΩ, resulting in A_{VOL} that is typically twice the guaranteed minimum limit.



L = 415-0930 (AIE)
D = any manufacturer

C_{OUT} = Sprague Type 673D Electrolytic 680µF, 20V

R1 = 48.7k in series with 511Ω (1%)
R2 = 5.62k (1%)

Figure 1. Circuit Used to Specify System Parameters

APPLICATIONS INFORMATION

Step-up (Boost) Regulator

The Block Diagram shows a step-up switching regulator utilizing the UC2577. The regulator produces an output voltage higher than the input voltage. The UC2577 turns its switch on and off at a fixed frequency of 52kHz, thus storing energy in the inductor (L). When the NPN switch is on, the inductor current is charged at a rate of VIN/L. When the switch is off, the voltage at the SWITCH terminal of the inductor rises above VIN, discharging the stored current through the output diode (D) into the output capacitor (C_{OUT}) at a rate of (V_{OUT} - VIN)/L. The energy stored in the inductor is thus transferred to the output.

The output voltage is controlled by the amount of energy transferred, which is controlled by modulating the peak inductor current. This modulation is accomplished by feeding a portion of the output voltage to an error amplifier which amplifies the difference between the feedback voltage and an internal 1.23V precision reference voltage. The output of the error amplifier is then compared to a voltage proportional to the switch current, or the inductor current, during the switch on time. A comparator terminates the switch on time when the two voltages are equal and thus controls the peak switch current to maintain a constant output voltage. Figure 2 shows voltage and current waveforms for the circuit. Formulas for calculation are shown in Figure 3.

STEP-UP REGULATOR DESIGN PROCEDURE

Refer to the Block Diagram

Given:

V_{INmin} = Minimum input supply voltage
V_{OUT} = Regulated output voltage

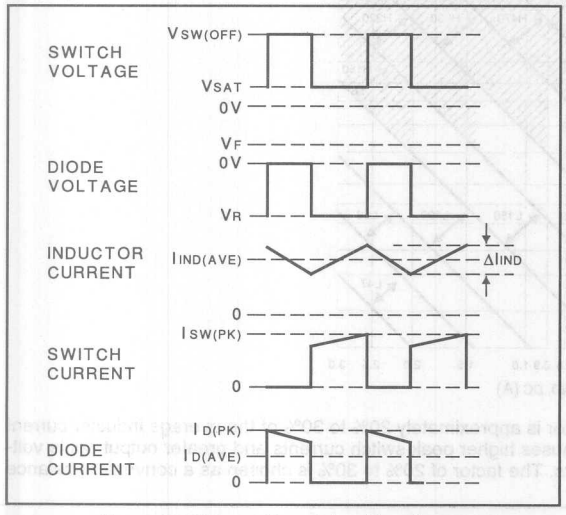


Figure 2. Step-up Regulator Waveforms

Duty Cycle	D	$\frac{V_{OUT} + V_F - V_{IN}}{V_{OUT} + V_F - V_{SAT}} \approx \frac{V_{OUT} - V_{IN}}{V_{OUT}}$
Avg. Inductor Current	$I_{IND(AVG)}$	$\frac{I_{LOAD}}{1 - D}$
Inductor Current Ripple	ΔI_{IND}	$\frac{V_{IN} - V_{SAT}}{L} \bullet \frac{D}{52{,}000}$
Peak Inductor Current	$I_{IND(PK)}$	$\frac{I_{LOAD}}{1-D} + \frac{\Delta I_{IND}}{2}$
Peak Switch Current	$I_{SW(PK)}$	$\frac{I_{LOAD}}{1-D} + \frac{\Delta I_{IND}}{2}$
Switch Voltage when Off	$V_{SW(OFF)}$	$V_{OUT} + V_F$
Diode Reverse Voltage	V_R	$V_{OUT} - V_{SAT}$
Avg. Diode Current	$I_{D(AVG)}$	I_{LOAD}
Peak Diode Current	$I_{D(PK)}$	$\frac{I_{LOAD}}{1-D} + \frac{\Delta I_{IND}}{2}$.
Power Dissipation	P_D	$0.25\Omega \left(\frac{I_{LOAD}}{1-D}\right)^2 D + \frac{I_{LOAD} \bullet D \bullet V_{IN}}{50\,(1-D)}$

V_F = Forward Biased Diode Voltage, I_{LOAD} = Output Load

Figure 3. Step-up Regulator Formulas

First, determine if the UC2577 can provide these values of V_{OUT} and $I_{LOADmax}$ when operating with the minimum value of V_{IN}. The upper limits for V_{OUT} and $I_{LOADmax}$ are given by the following equations.

$$V_{OUT} \le 60V \text{ and}$$
$$V_{OUT} \le 10 \bullet V_{INmin}$$
$$I_{LOADmax} \le \frac{2.1A \bullet V_{INmin}}{V_{OUT}}$$

These limits must be greater than or equal to the values specified in this application.

1. Output Voltage Section

Resistors R1 and R2 are used to select the desired output voltage. These resistors form a voltage divider and present a portion of the output voltage to the error amplifier which compares it to an internal 1.23V reference. Select R1 and R2 such that:

$$\frac{R1}{R2} = \frac{V_{OUT}}{1.23V} - 1$$

APPLICATIONS INFORMATION (cont.)

2. Inductor Selection (L)

A. Preliminary Calculations

To select the inductor, the calculation of the following three parameters is necessary:

Dmax, the maximum switch duty cycle ($0 \le D \le 0.9$):

$$D_{max} = \frac{V_{OUT} + V_F - V_{INmin}}{V_{OUT} + V_F - 0.6V}$$

where typically $V_F = 0.5V$ for Schottky diodes and $V_F = 0.8V$ for fast recovery diodes.

E • T, the product of volts • time that charges the inductor:

$$E \bullet T = \frac{D_{max} \bullet (V_{INmin} - 0.6V)10^6}{52{,}000Hz} (V \bullet \mu s)$$

$I_{IND, DC}$, the average inductor current under full load:

$$I_{IND, DC} = \frac{1.05 \bullet I_{LOADmax}}{1 - D_{max}}$$

B. Identify Inductor Value:

1. From Figure 4, identify the inductor code for the region indicated by the intersection of E • T and $I_{IND, DC}$. This code gives the inductor value in microhenries. The L or H prefix signifies whether the inductor is rated for a maximum E • T of 90Vμs (L) or 250Vμs (H).

2. If $D < 0.85$, go to step C. If $D \ge 0.85$, calculate the minimum inductance needed to ensure the switching regulator's stability:

If L_{min} is smaller than the inductor values found in step B1, go on to step C. Otherwise, the inductor value found in step B1 is too low; an appropriate inductor code should be obtained from the graph as follows:

1. Find the lowest value inductor that is greater than L_{min}.
2. Find where E • T intersects this inductor value to determine if it has an L or H prefix. If E • T intersects both the L and H regions, select the inductor with an H prefix.

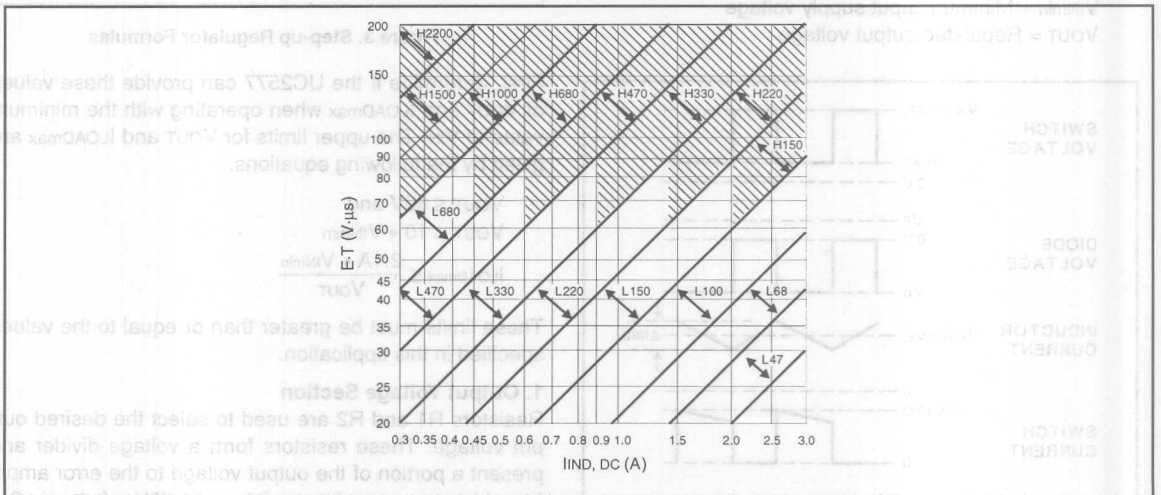
C. Inductor Selection

Select an inductor from the table of Figure 5 which cross references the inductor codes to the part numbers of the three different manufacturers. The inductors listed in this table have the following characteristics:

AIE (ferrite, pot-core inductors): Benefits of this type are low etectromagnetic interference (EMI), small physical size, and very low power dissipation (core loss).

Pulse (powdered iron, toroid core inductors): Benefits are low EMI and ability to withstand E • T and peak current above rated value better than ferrite cores.

Renco (ferrite, bobbin-core inductors): Benefits are low cost and best ability to withstand E • T and peak current above rated value. Be aware that these inductors generate more EMI than the other types, and this may interfere with signals sensitive to noise.



Note: This chart assumes that the inductor ripple current inductor is approximately 20% to 30% of the average inductor current (when the regulator is under full load). Greater ripple current causes higher peak switch currents and greater output ripple voltage. Lower ripple current is achieved with larger value inductors. The factor of 20% to 30% is chosen as a convenient balance between the two extremes.

Figure 4. Inductor Selection Graph

APPLICATIONS INFORMATION (cont.)

Inductor Code	Manufacturer's Part Number		
	AIE	Pulse	Renco
L47	415 - 0932	PE - 53112	RL2442
L68	415 - 0931	PE - 92114	RL2443
L100	415 - 0930	PE - 92108	RL2444
L150	415 - 0953	PE - 53113	RL1954
L220	415 - 0922	PE - 52626	RL1953
L330	415 - 0926	PE - 52627	RL1952
L470	415 - 0927	PE - 53114	RL1951
L680	415 - 0928	PE - 52629	RL1950
H150	415 - 0936	PE - 53115	RL2445
H220	430 - 0636	PE - 53116	RL2446
H330	430 - 0635	PE - 53117	RL2447
H470	430 - 0634	PE - 53118	RL1961
H680	415 - 0935	PE - 53119	RL1960
H1000	415 - 0934	PE - 53120	RL1959
H1500	415 - 0933	PE - 53121	RL1958
H2200	415 - 0945	PE - 53122	RL2448

AIE Magnetics, Div. Vernitron Corp., (813)347-2181
2801 72nd Street North, St. Petersburg, FL 33710
Pulse Engineering, (619)674-8100
12220 World Trade Drive, San Diego, CA 92128
Renco Electronics, Inc., (516)586-5566
60 Jeffryn Blvd. East, Deer Park, NY 11729

Figure 5. Table of Standardized Inductors and Manufacturer's Part Numbers

3. Compensation Network (Rc, Cc) and Output Capacitor (COUT) Selection

The compensation network consists of resistor RC and capacitor CC which form a simple pole-zero network and stabilize the regulator. The values of RC and CC depend upon the voltage gain of the regulator, ILOADmax, the inductor L, and output capacitance COUT. A procedure to calculate and select the values for RC, CC, and COUT which ensures stability is described below. It should be noted, however, that this may not result in optimum compensation. To guarantee optimum compensation a standard procedure for testing loop stability is recommended, such as measuring VOUT transient responses to pulsing ILOAD.

A. Calculate the maximum value for RC.

$$RC \le \frac{750 \bullet I_{LOADmax} \bullet V_{OUT}^2}{V_{INmin}^2}$$

Select a resistor less than or equal to this value, not to exceed 3kΩ.

B. Calculate the minimum value for COUT using the following two equations.

$$C_{OUT} \ge \frac{0.19 \bullet L \bullet RC \bullet I_{LOADmax}}{V_{INmin} \bullet V_{OUT}} \quad \text{and}$$

$$C_{OUT} \ge \frac{V_{INmin} \bullet RC \bullet (V_{INmin} + (3.74 \bullet 10^5 \bullet L))}{487{,}800 \bullet V_{OUT}^3}$$

The larger of these two values is the minimum value that ensures stability.

C. Calculate the minimum value of CC.

$$CC \ge \frac{58.5 \bullet V_{OUT}^2 \bullet C_{OUT}}{RC^2 \bullet V_{INmin}}$$

The compensation capacitor is also used in the soft start function of the regulator. When the input voltage is applied to the part, the switch duty cycle is increased slowly at a rate defined by the compensation capacitor and the soft start current, thus eliminating high input currents. Without the soft start circuitry, the switch duty cycle would instantly rise to about 90% and draw large currents from the input supply. For proper soft starting, the value for CC should be equal or greater than 0.22µF.

Figure 6 lists several types of aluminum electrolytic capacitors which could be used for the output filter. Use the following parameters to select the capacitor.

Working Voltage (WVDC): Choose a capacitor with a working voltage at least 20% higher than the regulator output voltage.

Ripple Current: This is the maximum RMS value of current that charges the capacitor during each switching cycle. For step-up and flyback regulators, the formula for ripple current is:

$$I_{RIPPLErms} = \frac{I_{LOADmax} \bullet D_{max}}{1 - D_{max}}$$

Choose a capacitor that is rated at least 50% higher than this value at 52kHz.

Equivalent Series Resistance (ESR): This is the primary cause of output ripple voltage, and it also affects the values of RC and CC needed to stabilize the regulator. As a result, the preceding calculations for CC and RC are only valid if the ESR does not exceed the maximum value specified by the following equations.

$$ESR \le \frac{0.01 \bullet 15V}{I_{RIPPLE(P-P)}} \quad \text{and} \quad \le \frac{8.7 \bullet 10^{-3} \bullet V_{IN}}{I_{LOADmax}} \quad \text{where}$$

$$I_{RIPPLE(P-P)} = \frac{1.15 \bullet I_{LOADmax}}{1 - D_{max}}$$

Select a capacitor with an ESR, at 52kHz, that is less than or equal to the lower value calculated. Most electrolytic capacitors specify ESR at 120kHz which is 15% to 30% higher than at 52kHz. Also, note that ESR increases by a factor of 2 when operating at –20°C.

In general, low values of ESR are achieved by using large value capacitors (C ≥ 470µF), and capacitors with high WVDC, or by paralleling smaller value capacitors.

APPLICATIONS INFORMATION (cont.)

4. Input Capacitor Selection (C_{IN})

To reduce noise on the supply voltage caused by the switching action of a step-up regulator (ripple current noise), VIN should be bypassed to ground. A good quality 0.1µF capacitor with low ESR should provide sufficient decoupling. If the UC2577 is located far from the supply source filter capacitors, an additional electrolytic (47µF, for example) is required.

Nichicon - Types PF, PX, or PZ
927 East StateParkway, Schaumburg, IL 60173
(708)843-7500

United Chemi-CON - Types LX, SXF, or SXJ
9801 West Higgens, Rosemont, IL 60018
(708)696-2000

Figure 6. Aluminum Electrolytic Capacitors Recommended for Switching Regulators

5. Output Diode Selection (D)

In the step-up regulator, the switching diode must withstand a reverse voltage and be able to conduct the peak output current of the UC2577. Therefore a suitable diode must have a minimum reverse breakdown voltage greater than the circuit output voltage, and should also be rated for average and peak current greater than $I_{LOADmax}$ and I_{Dpk}. Because of their low forward voltage drop (and thus higher regulator efficiencies), Schottky barrier diodes are often used in switching regulators. Refer to Figure 7 for recommended part numbers and voltage ratings of 1A and 3A diodes.

V_{OUTmax}	Schottky		Fast Recovery	
	1A	3A	1A	3A
20V	1N5817 MBR120P	1N5820 MBR320P		
30V	1N5818 MBR130P 11DQ03	1N5821 MBR330P 31DQ03		
40V	1N5819 MBR140P 11DQ04	1N5822 MBR340P 31DQ04		
50V	MBR150 11DQ05	MBR350 31DQ05	1N4933 MUR105	
100V			1N4934 MUR110 10DL1	MR851 30DL1 MR831

MBRxxx and MURxxx are manufactured by Motorola.
1DDxxx, 11Cxx and 31Dxx are manufactured by International Rectifier

Figure 7. Diode Selection Chart

ORDERING INFORMATION

Unitrode Type Number	
UC2577T-ADJ	5 Pin TO-220 Plastic Package
UC2577TD-ADJ	5 Pin TO-263 Plastic Package

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

HID Lamp Controller

FEATURES

- Regulates Lamp Power
- Compensates For Lamp Temperature
- Fixed Frequency Operation
- Current Mode Control
- Overcurrent Protected
- Overvoltage Shutdown
- Open and Short Protected
- High Current FET Drive Output
- Operates Over Wide Battery Voltage Range: 5V to 18V

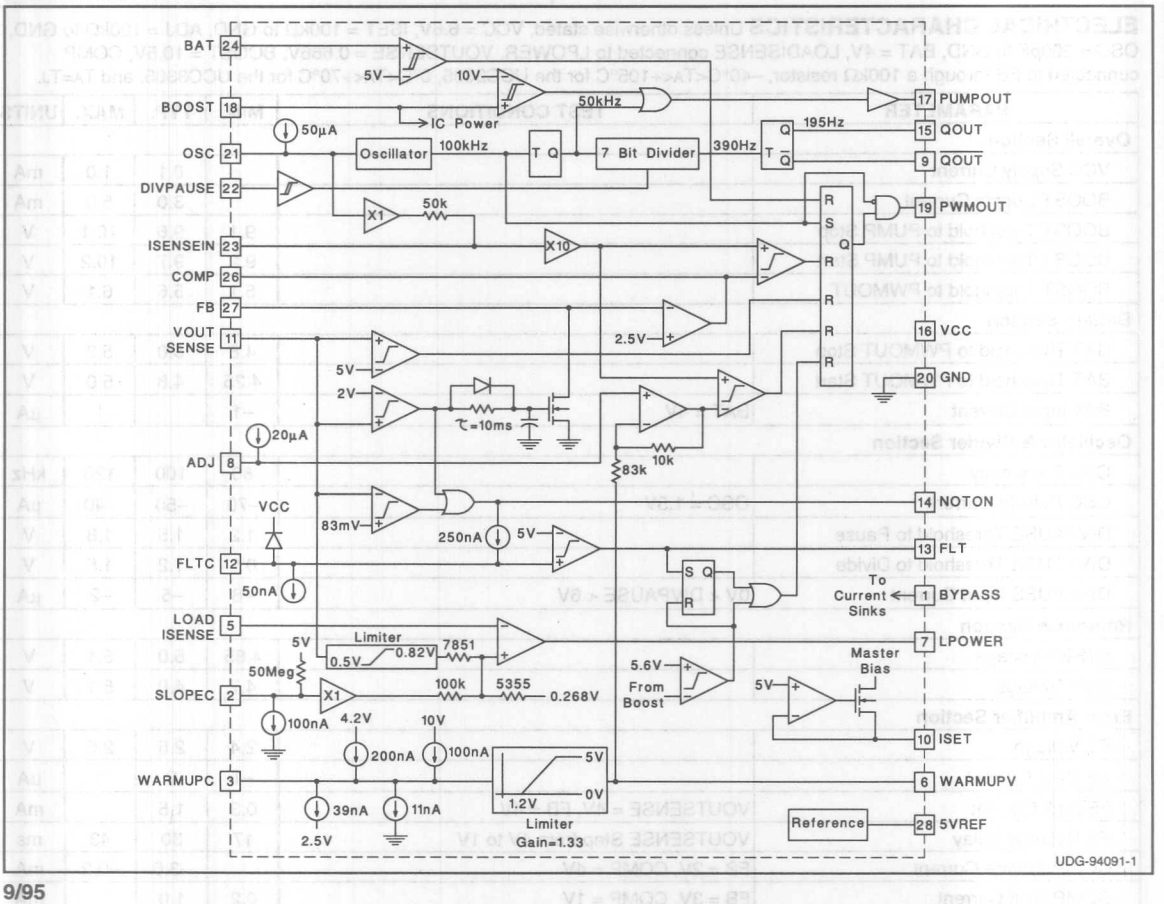
DESCRIPTION

The UCC3305 integrates all of the functions required to control and drive one HID lamp. The UCC3305 is tailored to the demanding, fast turn-on requirements of automobile headlamps, but is also applicable to all other lighting applications where HID lamps are selected. HID lamps are ideal for any lighting applications that can benefit from very high efficiency, blue-white light color, small physical lamp size, and very long life.

The UCC3305 contains a complete current mode pulse width modulator, a lamp power regulator, lamp temperature compensation, and total fault protection. Lamp temperature compensation is critical for automobile headlamps, because without compensation, light output varies dramatically from a cold lamp to one that is fully warmed up.

The UCC2305 is tested for full performance with ambient temperature from –40°C to +105°C while the UCC3305 is tested with ambient temperature from 0°C to +70°C. The UCC3305 is available in a 28 pin small-outline, surface mount plastic package (SOIC).

BLOCK DIAGRAM



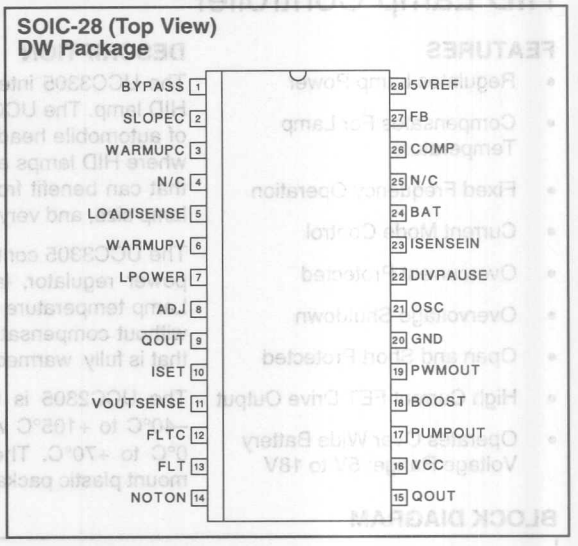
ABSOLUTE MAXIMUM RATINGS

VCC Supply Voltage 8.0V
BOOST Supply Voltage 12.0V
PWMOUT Current, Peak . . . . . ±1.0A
PWMOUT Energy, Capacitive Load. 5.0µJ
Input Voltage, Any Input . . . . . –0.3V to +10.0V
Output Current, QOUT, $\overline{QOUT}$, FLT . . . . . ±10.0mA
Output Current, 5VREF, LPOWER, COMP . . . . . ±10.0mA
ISET Current. . . . . –1.0mA
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature . . . . . +300°C

All voltages with respect to GND. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

SOIC-28 (Top View)
DW Package



ELECTRICAL CHARACTERISTICS

Unless otherwise stated, VCC = 6.6V, ISET = 100kΩ to GND, ADJ = 100kΩ to GND, OSC = 200pF to GND, BAT = 4V, LOADISENSE connected to LPOWER, VOUTSENSE = 0.666V, BOOST = 10.5V, COMP connected to FB through a 100kΩ resistor, –40°C<T_A<+105°C for the UCC2305, 0°C<T_A<+70°C for the UCC3305, and T_A=T_J.

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Overall Section					
VCC Supply Current			0.1	1.0	mA
BOOST Supply Current			3.0	5.0	mA
BOOST Threshold to PUMP Stop		9.1	9.6	10.1	V
BOOST Threshold to PUMP Start		9.2	9.7	10.2	V
BOOST Threshold to PWMOUT		5.1	5.6	6.1	V
Battery Section					
BAT Threshold to PWMOUT Stop		4.8	5.0	5.2	V
BAT Threshold to PWMOUT Start		4.25	4.8	5.0	V
BAT Input Current	BAT = 4V	–1		1	µA
Oscillator & Divider Section					
OSC Frequency		80	100	120	kHz
OSC Pull-Up Current	OSC = 1.5V	–70	–50	–40	µA
DIVPAUSE Threshold to Pause		1.2	1.5	1.8	V
DIVPAUSE Threshold to Divide		0.9	1.2	1.5	V
DIVPAUSE Input Current	0V < DIVPAUSE < 6V	–8	–5	–2	µA
Reference Section					
5VREF Voltage		4.85	5.0	5.1	V
ISET Voltage		4.7	4.8	5.1	V
Error Amplifier Section					
FB Voltage		2.4	2.5	2.6	V
FB Input Current		–1	0	1	µA
FB Sink Current	VOUTSENSE = 4V, FB = 4V	0.3	1.5		mA
FB Release Delay	VOUTSENSE Step from 4V to 1V	17	30	43	ms
COMP Source Current	FB = 2V, COMP = 4V		–3.0	–0.2	mA
COMP Sink Current	FB = 3V, COMP = 1V	0.2	1.0		mA

ELECTRICAL CHARACTERISTICS (cont.) Unless otherwise stated, VCC = 6.6V, ISET = 100kΩ to GND, ADJ = 100kΩ to GND, OSC = 200pF to GND, BAT = 4V, LOADISENSE connected to LPOWER, VOUTSENSE = 0.666V, BOOST = 10.5V, COMP connected to FB through a 100kΩ resistor, –40°C<T_A<+105°C for the UCC2305, 0°C<T_A<+70°C for the UCC3305, and T_A=T_J.

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Load Power Amplifier Section					
LOADISENSE Input Current		–2.5	–0.1	2.5	µA
LPOWER Source Current	LPOWER = 0V		–8.0	–0.4	mA
LPOWER Sink Current	LPOWER = 1V	0.4	1.3		mA
LPOWER Voltage	VOUTSENSE = 0.0V	0.35	0.40	0.45	V
	VOUTSENSE = 0.45V	0.35	0.40	0.45	V
	VOUTSENSE = 0.65V	0.41	0.46	0.51	V
	VOUTSENSE = 0.88V	0.46	0.51	0.56	V
	VOUTSENSE = 2.0V	0.46	0.51	0.56	V
	VOUTSENSE = 0.7V, SLOPEC = 0V	0.29	0.34	0.39	V
Input Current Sense Section					
ISENSEIN Threshold	COMP = 5V, WARMUPC = 0V	0.16	0.21	0.28	V
	COMP = 5V, WARMUPC = 10V	0.13	0.19	0.27	V
	COMP = 1V, WARMUPC = 0V	0.07	0.10	0.2	V
ISENSEIN Bias Current	OSC = 0V	–15	–5	–2	µA
	OSC = 2V	–65	–40	–15	µA
VOUTSENSE Section					
VOUTSENSE Threshold to PWMOUT		4.2	5.0	5.2	V
VOUTSENSE Threshold to FB		1.7	1.9	2.1	V
VOUTSENSE Threshold to NOTON		0.035	0.083	0.140	V
VOUTSENSE Input Current		–1		1	µA
OUTPUTS SECTION					
PWMOUT High Voltage	I_{PWMOUT} = –100mA	9.15	10.0		V
PWMOUT Low Voltage	I_{PWMOUT} = 100mA		0.3	0.5	V
PUMPOUT High Voltage	$I_{PUMPOUT}$ = –10mA	5.3	5.8		V
PUMPOUT Low Voltage	$I_{PUMPOUT}$ = 10mA		1.0	1.8	V
PUMPOUT Frequency	BOOST = 9.5V	35	50	60	kHz
NOTON High Voltage	I_{NOTON} = –1mA	5.0	6.3		V
NOTON Low Voltage	I_{NOTON} = 1mA		0.1	0.3	V
QOUT, $\overline{QOUT}$ High Voltage	I_{QOUT} = –1mA or $I_{\overline{QOUT}}$ = –1mA	5.0	6.3		V
QOUT, $\overline{QOUT}$ Low Voltage	I_{QOUT} = 1mA or $I_{\overline{QOUT}}$ = 1mA		0.1	0.45	V
QOUT, $\overline{QOUT}$ Frequency		175	250	275	Hz
FLT High Voltage	I_{FLT} = –1mA	6.0	6.3		V
FLT Low Voltage	I_{FLT} = 1mA		0.1	0.3	V
Timing Capacitor Section					
FLTC Discharge Current	FLTC = 2.5V	35	60	90	nA
FLTC Charge Current	FLTC = 2.5V	–380	–290	–220	nA
FLTC Threshold to FAULT		4.65	4.9	5.1	V
SLOPEC Charge Current	SLOPEC = 0.5V	–165	–90	–60	nA
	SLOPEC = 2.2	–105	–60	–40	nA
	SLOPEC = 4.2	–35	–20	–10	nA
SLOPEC Voltage	I_{SLOPEC} = –125nA	1.3	1.5	1.7	V
	I_{SLOPEC} = –50nA	2.8	3.0	3.2	V

ELECTRICAL CHARACTERISTICS (cont.) Unless otherwise stated, VCC = 6.6V, ISET = 100kΩ to GND, ADJ = 100kΩ to GND, OSC = 200pF to GND, BAT = 4V, LOADISENSE connected to LPOWER, VOUTSENSE = 0.666V, BOOST = 10.5V, COMP connected to FB through a 100kΩ resistor, –40°C<T_A<+105°C for the UCC2305, 0°C<T_A<+70°C for the UCC3305, and T_A=T_J.

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Timing Capacitor Section (cont.)					
SLOPEC Discharge Current	SLOPEC = 2.2V, VCC = 0V, BOOST = 0V, BYPASS = 8V	40	90	175	nA
WARMUPC Charge Current	WARMUPC = 0V	–515	–375	–275	nA
	WARMUPC = 2V	–450	–375	–300	nA
	WARMUPC = 6V	–170	–120	–75	nA
WARMUPC Voltage, Charging	$I_{WARMUPC}$ = –250nA	3.5	3.8	4.1	V
WARMUPC Discharge Current	WARMUPC = 5V, VCC = 0V, BOOST = 0V, BYPASS = 8V	23	50	108	nA
	WARMUPC = 1V, VCC = 0V, BOOST = 0V, BYPASS = 8V	5	10	20	nA
WARMUPC Voltage, Discharging	$I_{WARMUPC}$ = 25nA, VCC = 0V, BOOST = 0V, BYPASS = 8V	1.5	1.9	2.3	V
ADJ Bias Current	V_{ADJ} = 0V	–38	–20	–12	µA
WARMUPV Voltage	WARMUPC = 1V	0.05	0.125	0.25	V
	WARMUPC = 2V	0.09	0.108	1.27	V
	WARMUPC = 3V	2.3	2.48	2.66	V
	WARMUPC = 5V	4.5	4.8	5.1	V
	WARMUPC = 10V	4.5	4.8	5.1	V
BYPASS Voltage	VCC = 0V	8.8	9.6		V
BYPASS Current	VCC = 0V, BOOST = 0V, BYPASS = 8V		2.5	7	µA

PIN DESCRIPTIONS

5VREF: Circuitry in the UCC3305 uses the internal 5V reference to set currents and thresholds. This reference can also be used for other functions if required.

ADJ: The ratio of cold lamp peak current to warmed-up lamp peak current is controlled by the voltage on ADJ. To select this voltage, connect a resistor from ADJ to GND.

BAT: This input is used to detect excessively high input voltage and shut down the IC if the input exceeds a predetermined level. Connect BAT to a voltage divider across the input supply. The UCC3305 shuts down when this input voltage exceeds 5V. To protect the IC in the event of very high or negative inputs, keep divider impedance higher than 10k.

BOOST: Although the UCC3305 is powered from the VCC input, most functions of the device operate from a supply voltage of approximately 10V connected to BOOST. This 10V supply can be generated by a voltage doubler using PUMPOUT as an AC signal and external diodes as switches.

BYPASS: The UCC3305 compensates for lamp temperature changes by changing the voltage on the SLOPEC and WARMUPC capacitors. These voltages rise as the lamp warms up. An internal calculation determines what power should be applied to the lamp.

When the HID lamp is turned off, power to the lamp and the controller is removed, leaving these two critical capacitors charged to specific voltages. Also, with power off, the lamp will cool down at a controlled rate. It is essential that the two capacitors discharge at a similarly controlled rate so that if the lamp is restarted before the lamp is fully cooled, the controller will have an estimate of new lamp temperature, and can again command the correct power for the lamp.

Power to control the discharge of these capacitors comes from energy stored in a large capacitor connected to BYPASS. The value of the capacitor required can be estimated assuming a maximum BYPASS current of 5µA, a discharge time of 60s, and a maximum allowable droop of 5V by:

$$C = I \bullet \frac{\Delta t}{\Delta V} = 5\mu A \bullet \frac{60s}{5V} = 60\mu F$$

COMP: Differences between commanded lamp power and desired lamp power are amplified by an error amplifier. This amplifier senses the difference between the voltage at FB and 2.5V, and drives COMP with an amplified error voltage. A capacitor is normally connected from COMP to FB to compensate the overall feedback loop so that the system will be stable.

PIN DESCRIPTIONS (cont.)

DIVPAUSE: The QOUT and $\overline{\text{QOUT}}$ outputs can be used to switch lamp polarity in an AC ballast. It is important to stop polarity switching when the lamp is being lit, so that the arc across the electrodes can form in the correct place. Pulling high on DIVPAUSE stops the internal divider which generates the QOUT and $\overline{\text{QOUT}}$ signals, and thereby freezes the QOUT and $\overline{\text{QOUT}}$ signals.

To stop the divider when the lamp is being lit and start after the lamp has lit, connect a resistor from NOTON to DIVPAUSE and a capacitor from DIVPAUSE to GND.

FLTC: The voltage on VOUTSENSE is proportional to lamp voltage. If that voltage is too high or too low, the lamp is either open, shorted, or not yet running. During normal operation, there is a capacitor connected to FLTC, and this capacitor is discharged to 0V by a current source inside the UCC3305.

The UCC3305 monitors the voltage on VOUTSENSE and compares it to an internal 83mV lower threshold and a 2V upper threshold. If the voltage is outside this window, then the IC will pull up on FLTC with a current of approximately 250nA. If the fault remains long enough to charge the external FLTC capacitor over 5V, the controller declares a catastrophic fault and shuts the IC down. The IC will stay shut down until power is removed from BOOST.

If the fault clears before the FLTC capacitor reaches 5V, the capacitor discharges down to 0V. This discharge current is approximately 50nA, representing a five times longer discharge rate than charge rate.

FLT: If the voltage on the FLTC pin exceeds 5V, indicating a severe fault, then a latch in the UCC3305 sets and PWM drive is halted. In addition, the FLT output goes high to VCC, indicating a serious system fault.

FB: Differences between commanded lamp power and desired lamp power are amplified by an error amplifier. This amplifier senses the difference between the voltage at FB and 2.5V, and drives COMP with an amplified error voltage.

GND: Ground for all functions is through this pin.

ISENSEIN: The power regulating algorithm in the UCC3305 HID Controller computes a function of lamp current and lamp voltage and commands the appropriate battery current to keep lamp power constant. This appropriate battery current is sensed by a connection from ISENSEIN to a current sense resistor. This current sensed pulse width modulation scheme is often referred to as current mode control.

In addition to this current regulation, the UCC3305 contains peak input current limiting. This limiting is set to 0.2V across the ISENSEIN resistor during normal operation and 0.4V during starting. The transition from starting to normal operation is accomplished by the rise of the WARMUPC capacitor.

Current mode control has an advantage over voltage mode control in that a current mode loop is easier to compensate. Current mode control has a disadvantage compared to voltage mode control in that the loop can enter into chaotic oscillations at high duty cycles. These chaotic oscillations can be prevented using slope compensation. The UCC3305 contains internal slope compensation in the form of a current proportional to OSC voltage on ISENSEIN. This current combined with an external resistor from ISENSEIN to the current sense resistor creates a voltage drop proportional to OSC voltage, which gives slope compensation.

ISET: Many functions inside the UCC3305 require precise currents to give well controlled performance. These controlled currents are programmed by a resistor from ISET to GND. A resistor of 100k programs the IC to normal operating current. Lower resistor values increase the internal currents. Some of the functions which are influenced by this resistor are WARMUPC charging and discharging, SLOPEC charging and discharging, FLTC charging and discharging, and error amplifier bandwidth

LOADISENSE: Just as ISENSEIN is normally connected to a current sense resistor which monitors battery current, LOADISENSE is normally connected to a resistor which monitors lamp current. Lamp current is then regulated by the controller such that the correct lamp power is supplied at every lamp temperature, in conjunction with the lamp voltage sensed by VOUTSENSE.

LPOWER: LOADISENSE directly drives one input of an op amp in the UCC3305. This amplifier amplifies the difference between the desired load current and the actual load current, and generates an output signal on LPOWER which feeds the error amplifier.

NOTON: While the lamp is in a fault condition, such as excessively high or low lamp voltage, NOTON is pulled high to VCC, indicating that the arc is not yet correct. When the voltage on VOUTSENSE is within the 83mV to 2V window, NOTON is pulled low.

OSC: The fixed frequency PWM in the UCC3305 operates at the frequency programmed by the OSC pin. Typically, a a 200pF capacitor from OSC to GND programs the PWM frequency at 100kHz. In addition, this programs the charge pump at 50kHz and the $\overline{\text{QOUT}}$ and QOUT signals at 192Hz. The actual oscillator frequency is a function of both the capacitor from OSC to GND and the resistor from ISET to GND.

PUMPOUT: Although the UCC3305 is powered from the VCC input, most functions of the device operate from a supply voltage of approximately 10V connected to BOOST. In normal operation, this 10V supply is gener-

PIN DESCRIPTIONS (cont.)

ated by a voltage doubler using the PUMPOUT pin as an AC signal and external diodes as switches. PUMPOUT is a square wave which swings from VCC to GND at half of the OSC frequency.

PWMOUT: The output of the pulse width modulator is a command signal to a power MOSFET switch. This signal appears on PWMOUT. In normal systems, PWMOUT can be directly connected to the gate of an N-channel power MOSFET such as the IRF540. If the lead between the UCC3305 and the MOSFET is longer than a few cm, a 10 ohm resistor from PWMOUT to gate may be required to dampen overshoot and undershoot.

$\overline{\text{QOUT}}$: The UCC3305 is immediately configured for DC HID lamps. To operate with AC HID lamps, it is necessary to add a power H-bridge which will toggle lamp voltage. A practical switching frequency for this toggle function is the OSC frequency divided by 512, or 192Hz for a 100kHz oscillator.

The $\overline{\text{QOUT}}$ pin is a logic output which toggles at the OSC frequency divided by 512, 180 degrees out of phase with the QOUT pin.

QOUT: The QOUT pin is a logic output which toggles at the OSC frequency divided by 512, 180 degrees out of phase with the $\overline{\text{QOUT}}$ pin.

SLOPEC: To track lamp warm-up and cool down, two capacitors connected to the UCC3305 charge and discharge. One is connected to SLOPEC. The other is connected to WARMUPC. The capacitor connected to SLOPEC charges up to 5V with a rate controlled by the resistor from ISET to GND. With a nominal 100k ISET resistor the charging current into SLOPEC is equivalent to the current from a 50Meg resistor to 5V.

When power is removed from VCC, SLOPEC discharges at a constant current, nominally 100nA.

VCC: VCC is the main supply input to the UCC3305. Many functions in the UCC3305 are powered by VCC, while others are powered by BOOST. VCC should be clamped to 6.8V by an external zener diode and kept as close to 6.8V as practical with a low value resistor to the input supply.

VOUT-SENSE: The VOUTSENSE input is used to sense lamp voltage, commonly through a 120:1 voltage divider. For a normal, running HID lamp, the voltage across the lamp is between 60V and 110V. It takes higher than 300V to break down the lamp, and it is desirable to limit the voltage on the starter input to 600V maximum. A lamp voltage less than 10V is indicative of a shorted lamp.

The UCC3305 regulates lamp power by commanding the correct lamp current for a given lamp voltage. In addition, a comparator in the UCC3305 terminates a PWM cycle if VOUTSENSE reaches 5V, corresponding to 600V on the lamp. This regulates lamp voltage at 600V when the lamp is not lit. Comparators in the UCC3305 also compare VOUTSENSE to 83mV corresponding to 10V lamp voltage and 2V, corresponding to a 240V lamp voltage. When the VOUTSENSE voltage is outside this window, the lamp is either not lit, shorted, or open.

WARMUPC: In addition to the capacitor from SLOPEC to GND, lamp temperature is estimated by the voltage on a capacitor from WARMUPC to GND. This capacitor is charged by a 200nA current source to 4.2V and by a 100nA current source from 4.2V to 10V when the lamp is on, and discharged by 39nA current sink to 2.5V and 11nA current sink to GND when the lamp is off.

WARMUPV: The voltage on WARMUPC is used to modulate the signal fed to the error amplifier through FB. However, the impedance on WARMUPC is too high to be directly used. The UCC3305 contains a buffer amplifier which buffers the voltage on WARMUPC and processes it to WARMUPV, making a signal appropriate for driving FB.

APPLICATIONS INFORMATION

Typical Application

This circuit shows the UCC3305 HID Lamp Controller IC in a flyback converter. The output of the converter is regulated at constant power, so that lamp intensity is relatively constant regardless of small lamp manufacturing variations.

Full Bridge Output Stage

The output of the flyback converter is directed to the AC lamp through a full bridge inverter. The full bridge is switched at a low frequency (typically 195Hz), so that the average lamp voltage is zero. The low frequency switching is derived from the PWM oscillator. It is desirable to switch lamp polarity when running, but switching lamp polarity can interfere with clean starting. The UCC3305 has a logic output called NOTON which is high when the lamp is not running (Not On) and low when the lamp is running. This output is connected to the DIVPAUSE input so that the low frequency switching stops until the lamp is fully lit.

The UCC3305 HID Controller IC has two low frequency outputs, QOUT and $\overline{\text{QOUT}}$. These outputs are capable of driving low-side MOSFETs directly at 195Hz, but high-side MOSFETs require a level-shifted drive. This can be

APPLICATIONS INFORMATION (cont.)

as simple as a high voltage transistor and a resistor pull-up, combined with the correct choice of phases.

Regulated Lamp Input Power Gives Constant Intensity

The LPOWER output of the UCC3305 is a voltage roughly proportional to lamp input power. The UCC3305 regulates constant lamp power over a wide range of lamp voltages. The range of lamp voltages which produce constant lamp power is set by the limiting amplifier on VOUTSENSE.

For inputs to VOUTSENSE below 0.5V, such as would occur with a shorted lamp, the loop regulates constant load current. For inputs to VOUTSENSE greater than 0.82V, as might occur with a lamp that is open or not yet lit, the loop also regulates constant load current, but at a lower current than for a shorted lamp. In between those two voltages, the amplifier driving the LPOWER pin will sum the load current and load voltage and produce a signal roughly proportional to load power. The summing amplifier approximates power well enough to hold power within ±10% over a factor of two in lamp voltage.

The UCC3305 HID Controller contains a current mode PWM similar to the industry standard UC3842 and UCC3802 circuits. This controller uses a high gain op amp to regulate the output of the LPOWER circuit. This op amp drives a high speed PWM comparator, which compares converter input current to the output of the op amp and uses this signal to set duty cycle.

Slope Compensation

In addition to a complete current mode PWM, the UCC3305 HID Controller contains internal slope compensation, a valuable function which improves current loop stability for high duty cycles. Slope compensation is accomplished with an on-chip current ramp and an off-chip resistor RSL. Larger values of RSL give more slope compensation and a more stable feedback loop.

Powering The UCC3305

Conventional power MOSFETs require at least 8V of gate drive to ensure high efficiency and low on resistance. Despite this requirement, the UCC3305 HID Controller can be used to build a ballast that will drive power MOSFETs well with input supplies as low as 5V! The UCC3305 does this using a charge pump.

In this typical application, power for the UCC3305 HID Controller IC is derived from a 6.8V zener supply. This zener regulated supply gives the application overvoltage protection, reverse battery protection, low parts count, and low cost. The output of the 6.8V zener supply drives the VCC pin of the UCC3305. VCC is the input to the UCC3305 charge pump. The charge pump generates a regulated 10V supply on the BOOST output. This 10V supply drives all other functions on the UCC3305.

Protection From Over Voltage

The most significant stresses in an automotive environment are the overvoltage conditions which can occur during load dump and double-battery jump start. At these times, the voltage into the ballast can go so high that even the most overdesigned power stage will be damaged. The UCC3305 is inherently immune to damage from this when operated with a zener regulated supply. In addition, the UCC3305 will protect the ballast components by shutting down the PWM in the presence of excessive voltage on the BAT input.

This typical application shows a voltage divider consisting of a 270k resistor and a 100k resistor driving the BAT input. The threshold of the BAT input is approximately 5V, so this divider sets the shutdown voltage at approximately 18.5V.

Programming the UCC3305

All circuitry on the UCC3305 HID Lamp Controller is operated from a bias current set by the resistor from ISET to ground. For best operation, this resistor (RSET) should be between 75k and 150k.

Oscillator Frequency

The UCC3305 HID Lamp Controller PWM oscillator is set by the resistor from ISET to ground and by the capacitor from OSC to ground. Oscillator frequency can be estimated by the equation:

$$F_{OSC} = \frac{2}{R_{SET} \bullet C_{OSC}}$$

For operation at 100kHz, RSET should be 100k and COSC should be 200pF.

The PWM oscillator also determines the low frequency lamp switching rate for AC lamps. The exact lamp switching rate is the PWM frequency divided by 512.

Lamp Temperature Compensation

Automobile headlights must come up to full intensity very quickly, but HID lamps require many minutes to stabilize. The UCC3305 HID Controller contains sophisticated internal circuitry to anticipate lamp temperature and also to compensate for lamp temperature.

The circuits anticipate lamp temperature by monitoring charge on capacitors which charge when the lamp is on and discharge when the lamp is off. The UCC3305 HID Controller compensates for lamp temperature by driving the lamp with a higher lamp power when the lamp is cold and reducing the power to a normal operating level when the lamp is warmed up. The capacitors which set these

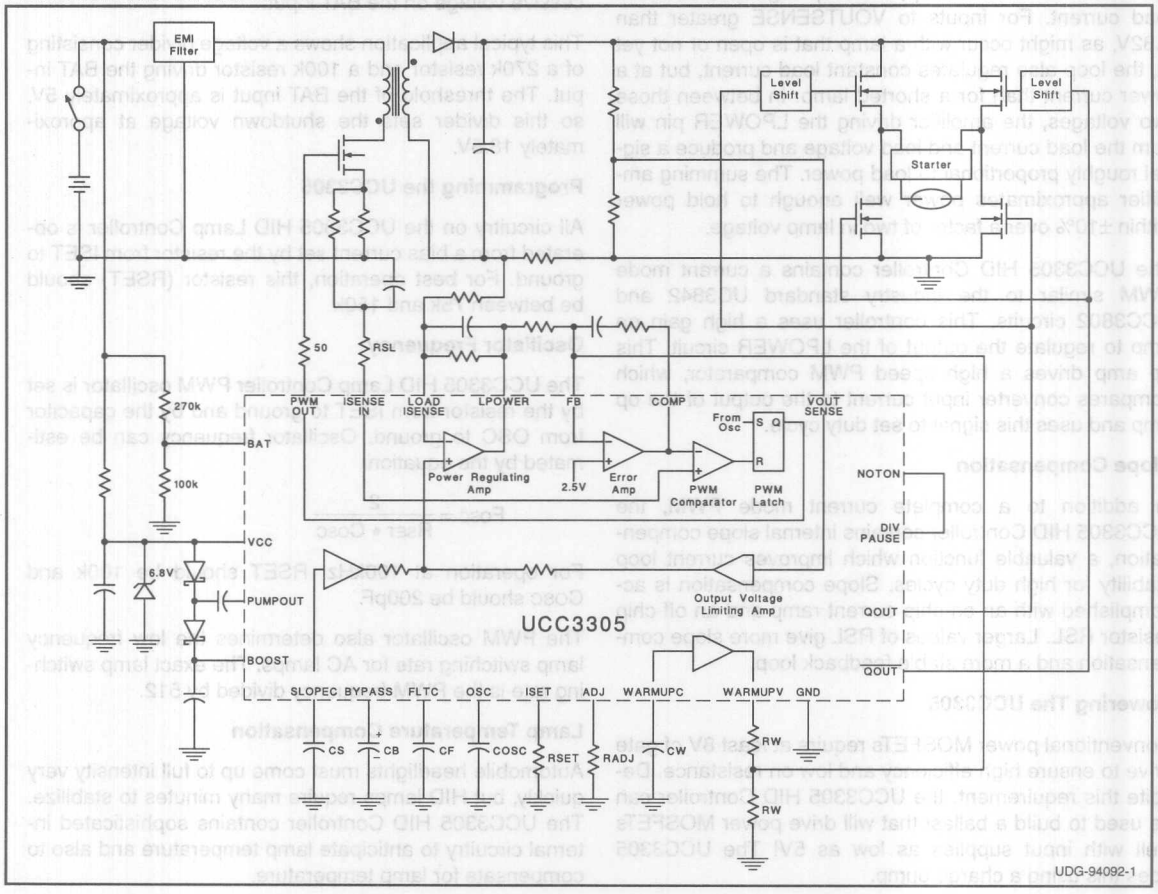
APPLICATIONS INFORMATION (cont.)

time constants are external film capacitors CS and CW, and are connected to SLOPEC and WARMUPC. CS and CW are critical capacitors and must be selected to match the time-temperature relationship of the lamp.

In addition to changing the power regulation point, the WARMUPC capacitor voltage also changes the short circuit lamp current. The ratio of cold short circuit current to warmed-up short circuit current is set by the resistor from ADJ to ground.

When power is removed from the ballast, CS and CW must discharge at a controlled rate. The discharge currents are programmed by current sources on the UCC3305 HID Controller. These current sources are powered by the power supply connected to BYPASS. In a typical application, a non-critical electrolytic capacitor from BYPASS to ground stores energy when the ballast is on and uses this energy to control the discharge rate when the ballast is off.

FLYBACK HID BALLAST



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Advanced Regulating Pulse Width Modulators

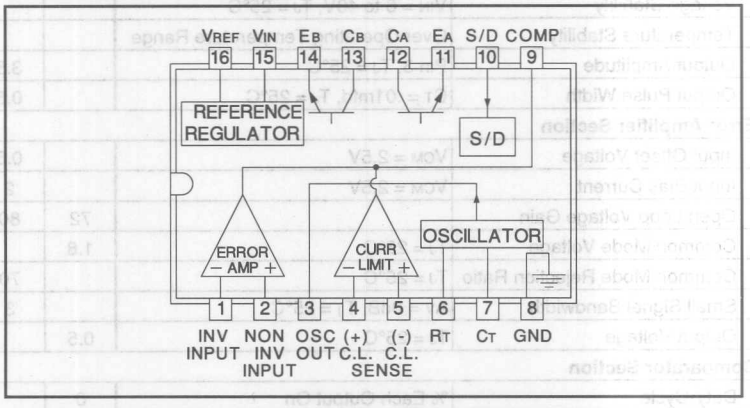
FEATURES

- Complete PWM Power Control Circuitry
- Uncommitted Outputs for Single-ended or Push-pull Applications
- Low Standby Current...8mA Typical
- Interchangeable with SG1524, SG2524 and SG3524, Respectively

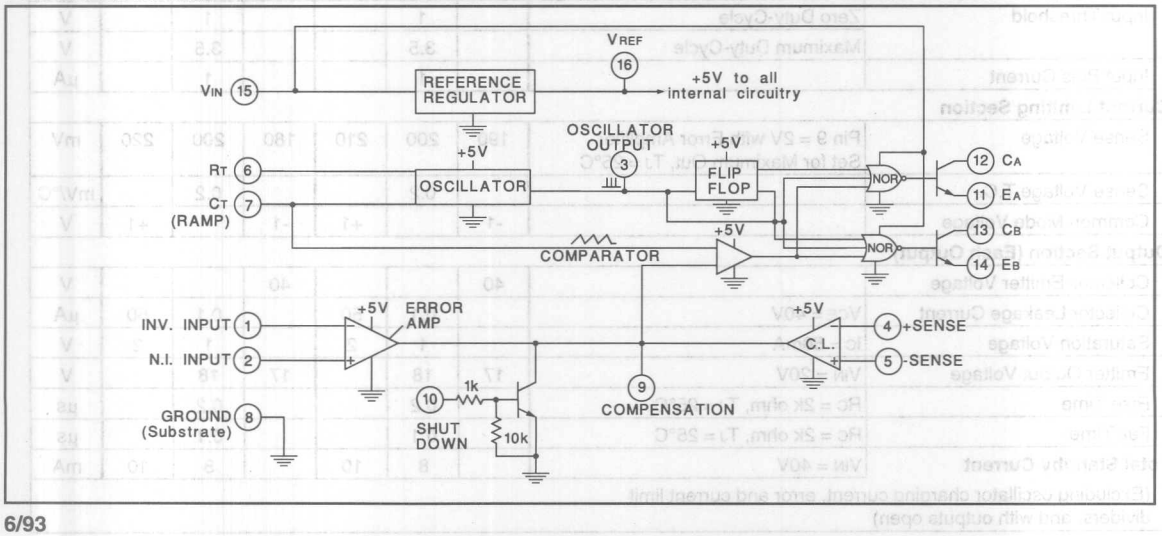
DESCRIPTION

The UC1524, UC2524 and UC3524 incorporate on a single monolithic chip all the functions required for the construction of regulating power supplies, inverters or switching regulators. They can also be used as the control element for high-power-output applications. The UC1524 family was designed for switching regulators of either polarity, transformer-coupled dc-to-dc converters, transformerless voltage doublers and polarity converter applications employing fixed-frequency, pulse-width modulation techniques. The dual alternating outputs allow either single-ended or push-pull applications. Each device includes an on-chip reference, error amplifier, programmable oscillator, pulse-steering flip-flop, two uncommitted output transistors, a high-gain comparator, and current-limiting and shut-down circuitry. The UC1524 is characterized for operation over the full military temperature range of -55°C to +125°C. The UC2524 and UC3524 are designed for operation from -25°C to +85°C and 0° to +70°C, respectively.

CONNECTION DIAGRAM



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, these specifications apply for T_A = –55°C to +125°C for the UC1524, –25°C to +85°C for the UC2524, and 0°C to +70°C for the UC3524, V_{IN} = 20V, and f = 20kHz, T_A=T_J.

PARAMETER	TEST CONDITIONS	UC1524/UC2524			UC3524			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Reference Section								
Output Voltage		4.8	5.0	5.2	4.6	5.0	5.4	V
Line Regulation	V_{IN} = 8 to 40V		10	20		10	30	mV
Load Regulation	I_L = 0 to 20mA		20	50		20	50	mV
Ripple Rejection	f = 120Hz, T_J = 25°C		66			66		dB
Short Circuit Current Limit	V_{REF} = 0, T_J = 25°C		100			100		mA
Temperature Stability	Over Operating Temperature Range		0.3	1		0.3	1	%
Long Term Stability	T_J = 125°C, t = 1000 Hrs.		20			20		mV
Oscillator Section								
Maximum Frequency	C_T = .001mfd, R_T = 2kΩ		300			300		kHz
Initial Accuracy	R_T and C_T Constant		5			5		%
Voltage Stability	V_{IN} = 8 to 40V, T_J = 25°C			1			1	%
Temperature Stability	Over Operating Temperature Range			5			5	%
Output Amplitude	Pin 3, T_J = 25°C		3.5			3.5		V
Output Pulse Width	C_T = .01mfd, T_J = 25°C		0.5			0.5		µs
Error Amplifier Section								
Input Offset Voltage	V_{CM} = 2.5V		0.5	5		2	10	mV
Input Bias Current	V_{CM} = 2.5V		2	10		2	10	µA
Open Loop Voltage Gain		72	80		60	80		dB
Common Mode Voltage	T_J = 25°C	1.8		3.4	1.8		3.4	V
Common Mode Rejection Ratio	T_J = 25°C		70			70		dB
Small Signal Bandwidth	A_V = 0dB, T_J = 25°C		3			3		MHz
Output Voltage	T_J = 25°C	0.5		3.8	0.5		3.8	V
Comparator Section								
Duty-Cycle	% Each Output On	0		45	0		45	%
Input Threshold	Zero Duty-Cycle		1			1		V
	Maximum Duty-Cycle		3.5			3.5		V
Input Bias Current			1			1		µA
Current Limiting Section								
Sense Voltage	Pin 9 = 2V with Error Amplifier Set for Maximum Out, T_J = 25°C	190	200	210	180	200	220	mV
Sense Voltage T.C.			0.2			0.2		mV/°C
Common Mode Voltage		-1		+1	-1		+1	V
Output Section (Each Output)								
Collector-Emitter Voltage		40			40			V
Collector Leakage Current	V_{CE} = 40V		0.1	50		0.1	50	µA
Saturation Voltage	I_C = 50mA		1	2		1	2	V
Emitter Output Voltage	V_{IN} = 20V	17	18		17	18		V
Rise Time	R_C = 2k ohm, T_J = 25°C		0.2			0.2		µs
Fall Time	R_C = 2k ohm, T_J = 25°C		0.1			0.1		µs
Total Standby Current	V_{IN} = 40V		8	10		8	10	mA
(Excluding oscillator charging current, error and current limit dividers, and with outputs open)								

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage, V_{CC} (Notes 2 and 3) 40V
Collector Output Current 100mA
Reference Output Current 50mA
Current Through C_T Terminal . . . . . -5mA
Power Dissipation at T_A = +25°C (Note 4) 1000mW
Power Dissipation at T_C = +25°C (Note 4) 2000mW
Operating Junction Temperature Range . . . . . -55°C to +150°C
Storage Temperature Range . . . . . -65°C to +150°C

Note 1: Over operating free-air temperature range unless otherwise noted.

Note 2: All voltage values are with respect to the ground terminal, pin 8.

Note 3: The reference regulator may be bypassed for operation from a fixed 5V supply by connecting the Vcc and reference output pins both to the supply voltage. In this configuration the maximum supply voltage is 6V.

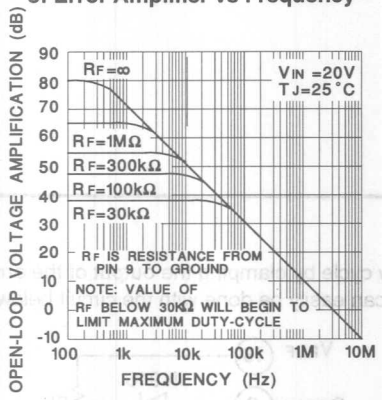
Note 4: Consult packaging section of databook for thermal limitations and considerations of package.

RECOMMENDED OPERATING CONDITIONS

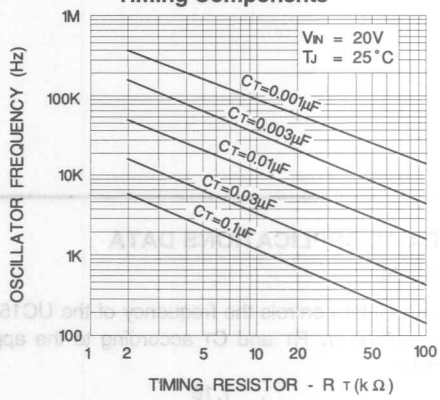
Supply Voltage, V_{CC} . . . . . 8V to 40V
Reference Output Current . . . . . 0 to 20mA
Current through C_T Terminal . . . . . -0.03mA to -2mA
Timing Resistor, R_T . . . . . 1.8kΩ to 100kΩ
Timing Capacitor, C_T . . . . . 0.001µF to 0.1µF
Operating Ambient Temperature Range
UC1524 . . . . . -55°C to +125°C
UC2524 . . . . . -25°C to +85°C
UC3524 . . . . . 0°C to +70°C

TYPICAL CHARACTERISTICS

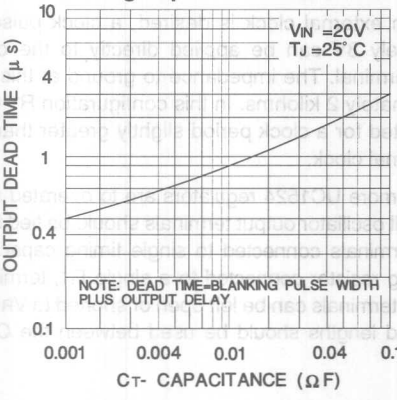
Open-Loop Voltage Amplification of Error Amplifier vs Frequency



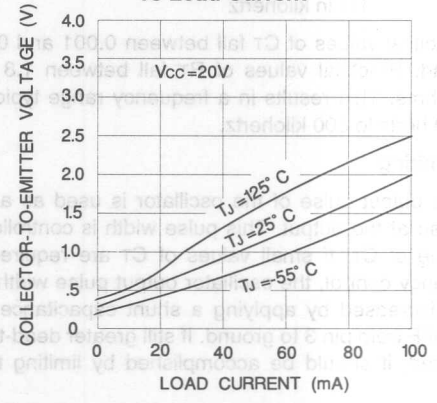
Oscillator Frequency vs Timing Components



Output Dead Time vs Timing Capacitance Value



Output Saturation Voltage vs Load Current



PRINCIPLES OF OPERATION

The UC1524 is a fixed-frequency pulse-width-modulation voltage regulator control circuit. The regulator operates at a frequency that is programmed by one timing resistor (R_T), and one timing capacitor (C_T). R_T establishes a constant charging current for C_T. This results in a linear voltage ramp at C_T, which is fed to the comparator providing linear control of the output pulse width by the error amplifier. The UC1524 contains an on-board 5V regulator that serves as a reference as well as powering the UC1524's internal control circuitry and is also useful in supplying external support functions. This reference voltage is lowered externally by a resistor divider to provide a reference within the common-mode range of the error amplifier or an external reference may be used. The power supply output is sensed by a second resistor divider network to generate a feedback signal to the error amplifier. The amplifier output voltage is then compared to the linear voltage ramp at C_T. The resulting modulated pulse out of the high-gain comparator is then steered to the appropriate output pass transistor (Q_1 or Q_2) by the pulse-steering flip-flop, which is synchronously toggled by the oscillator output. The oscillator output pulse also serves as a blanking pulse to assure both outputs are never on simultaneously during the transition times. The width of the blanking pulse is controlled by the valve of C_T. The outputs may be applied in a push-pull configuration in which their frequency is half that of the base oscillator, or paralleled for single-ended applications in which the frequency is equal to that of the oscillator. The output of the error amplifier shares a common input to the comparator with the current limiting and shutdown circuitry and can be overridden by signals from either of these inputs. This common point is also available externally and may be employed to control the gain of, or to compensate, the error amplifier or to provide additional control to the regulator.

TYPICAL APPLICATIONS DATA

Oscillator

The oscillator controls the frequency of the UC1524 and is programmed by R_T and C_T according to the approximate formula:

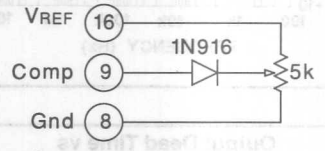
$$f \approx \frac{1.18}{R_T C_T}$$

where R_T is in kilohms
C_T is in microfarads
f is in kilohertz

Practical values of C_T fall between 0.001 and 0.1 microfarad. Practical values of R_T fall between 1.8 and 100 kilohms. This results in a frequency range typically from 120 hertz to 500 kilohertz.

Blanking

The output pulse of the oscillator is used as a blanking pulse at the output. This pulse width is controlled by the value of C_T. If small values of C_T are required for frequency control, the oscillator output pulse width may still be increased by applying a shunt capacitance of up to 100pF from pin 3 to ground. If still greater dead-time is required, it should be accomplished by limiting the maximum duty cycle by clamping the output of the error amplifier. This can easily be done with the circuit below:

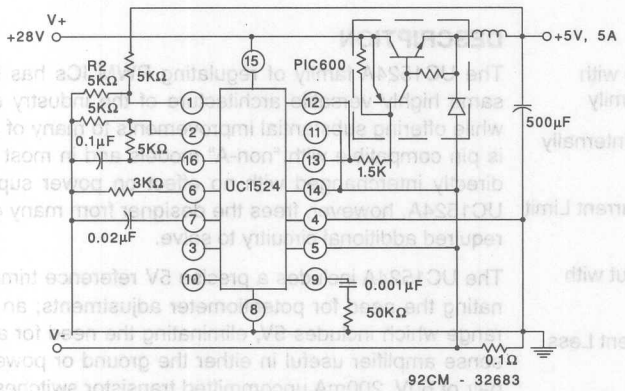


Synchronous Operation

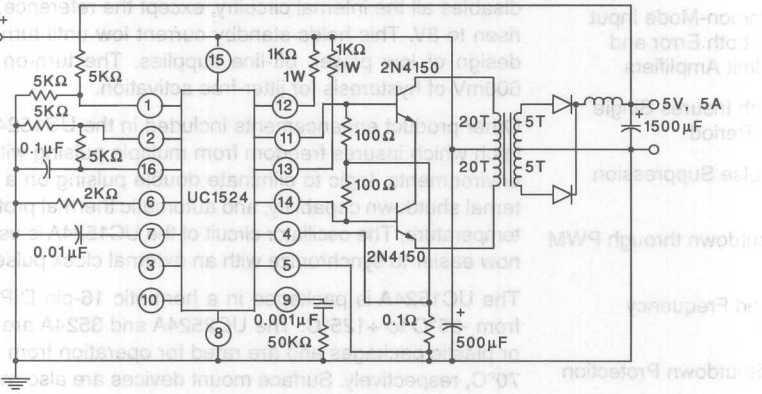
When an external clock is desired, a clock pulse of approximately 3V can be applied directly to the oscillator output terminal. The impedance to ground at this point is approximately 2 kilohms. In this configuration R_T C_T must be selected for a clock period slightly greater than that of the external clock.

If two or more UC1524 regulators are to operated synchronously, all oscillator output terminals should be tied together, all C_T terminals connected to single timing capacitor, and the timing resistor connected to a single R_T, terminal. The other R_T terminals can be left open or shorted to V_{REF}. Minimum lead lengths should be used between the C_T terminals.

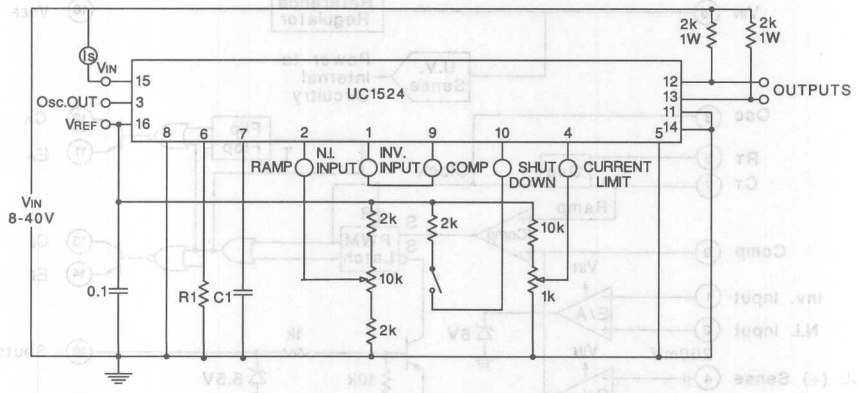
Single-Ended LC Switching Regulator Circuit



Push Pull Transformer Coupled Circuit



Open Loop Test Circuit



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UNITRODE

UC1524A
UC2524A
UC3524A

Advanced Regulating Pulse Width Modulators

FEATURES

- Fully Interchangeable with Standard UC1524 Family
- Precision Reference Internally Trimmed to ±1%
- High-Performance Current Limit Function
- Under-Voltage Lockout with Hysteretic Turn-on
- Start-Up Supply Current Less Than 4mA
- Output Current to 200mA
- 60V Output Capability
- Wide Common-Mode Input Range for both Error and Current Limit Amplifiers
- PWM Latch Insures Single Pulse per Period
- Double Pulse Suppression Logic
- 200ns Shutdown through PWM Latch
- Guaranteed Frequency Accuracy
- Thermal Shutdown Protection

DESCRIPTION

The UC1524A family of regulating PWM ICs has been designed to retain the same highly versatile architecture of the industry standard UC1524 (SG1524) while offering substantial improvements to many of its limitations. The UC1524A is pin compatible with "non-A" models and in most existing applications can be directly interchanged with no effect on power supply performance. Using the UC1524A, however, frees the designer from many concerns which typically had required additional circuitry to solve.

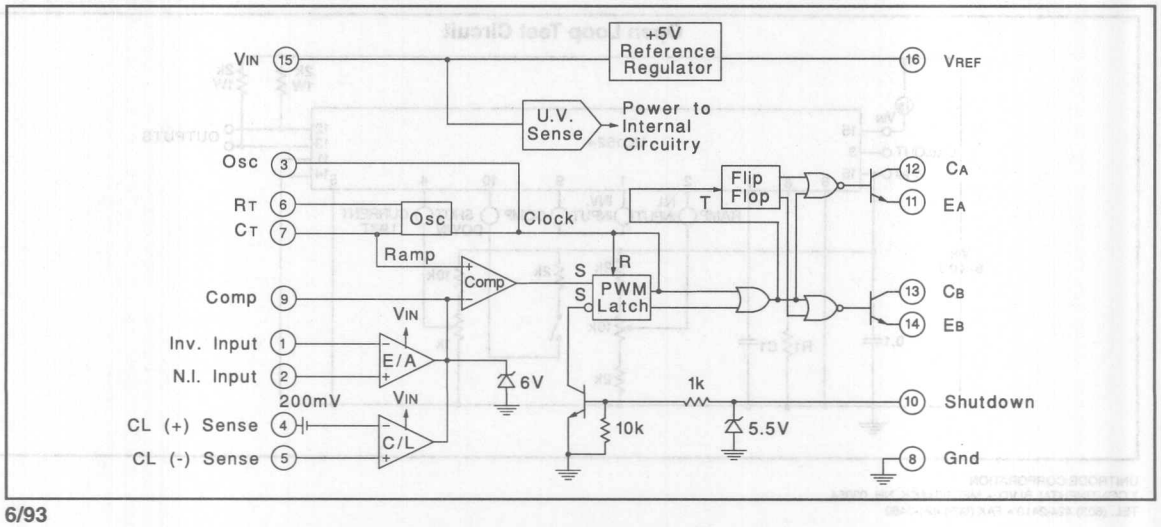
The UC1524A includes a precise 5V reference trimmed to ±1% accuracy, eliminating the need for potentiometer adjustments; an error amplifier with an input range which includes 5V, eliminating the need for a reference divider; a current sense amplifier useful in either the ground or power supply output lines; and a pair of 60V, 200mA uncommitted transistor switches which greatly enhance output versatility.

An additional feature of the UC1524A is an under-voltage lockout circuit which disables all the internal circuitry, except the reference, until the input voltage has risen to 8V. This holds standby current low until turn-on, greatly simplifying the design of low power, off-line supplies. The turn-on circuit has approximately 600mV of hysteresis for jitter-free activation.

Other product enhancements included in the UC1524A's design include a PWM latch which insures freedom from multiple pulsing within a period, even in noisy environments, logic to eliminate double pulsing on a single output, a 200ns external shutdown capability, and automatic thermal protection from excessive chip temperature. The oscillator circuit of the UC1524A is usable beyond 500kHz and is now easier to synchronize with an external clock pulse.

The UC1524A is packaged in a hermetic 16-pin DIP and is rated for operation from -55°C to +125°C. The UC2524A and 3524A are available in either ceramic or plastic packages and are rated for operation from -25°C to +85°C and 0°C to 70°C, respectively. Surface mount devices are also available.

BLOCK DIAGRAM



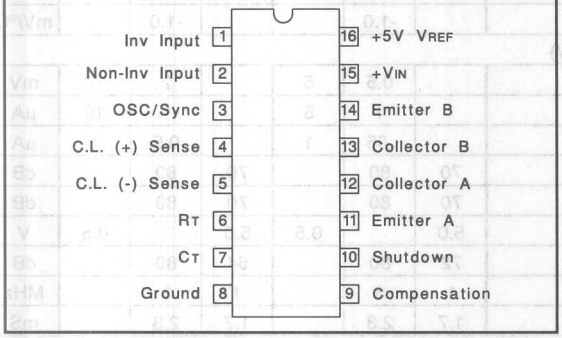
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ABSOLUTE MAXIMUM RATINGS

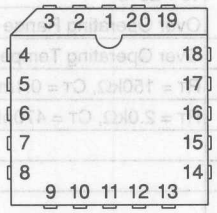
Supply Voltage (V_{IN}) 40V
Collector Supply Voltage (V_C) 60V
Output Current (each Output) 200mA
Maximum Forced Voltage (Pin 9, 10) . . . . . -3 to +5V
Maximum Forced Current (Pin 9, 10) . . . . . ±10mA
Reference Output Current 50mA
Oscillator Charging Current 5mA
Power Dissipation at T_A = +25°C 1000mW
Power Dissipation at T_C = +25°C 2000mW
Operating Temperature Range . . . . . -55°C to +125°C
Storage Temperature Range . . . . . -65°C to +150°C
Lead Temperature, (Soldering, 10 seconds) . . . . . +300°C
Note: Consult packaging section of Databook for thermal limitations and considerations of package.

CONNECTION DIAGRAMS

DIL-16, SOIC-16 (TOP VIEW)
J or N Package, DW Pack-



PLCC-20, LCC-20 (TOP VIEW)



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
Inv. Input	2
Non-Inv. Input	3
OSC/SYNC	4
C.L. (+) sense	5
N/C	6
C.L. (-) sense	7
RT	8
CT	9
Ground	10
N/C	11
Compensation	12
Shutdown	13
Emitter A	14
Collector A	15
N/C	16
Collector B	17
Emitter B	18
+VIN	19
+5V VREF	20

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1524A, -25° to +85°C for the UC2524A, and 0°C to + 70°C for the UC3524A; V_{IN} = V_C = 20V, T_A = T_J.

PARAMETER	TEST CONDITIONS	UC1524A / UC2524A			UC3524A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Turn-on Characteristics								
Input Voltage	Operating Range after Turn-on	8		40	8		40	V
Turn-on Threshold		6.5	7.5	8.5	6.5	7.5	8.5	V
Turn-on Current	V_{IN} = 6V		2.5	4		2.5	4	mA
Operating Current	V_{IN} = 8 to 40V		5	10		5	10	mA
Turn-on Hysteresis*			0.5			0.5		V
Reference Section								
Output Voltage	T_J = 25°C	4.95	5.00	5.05	4.90	5.00	5.10	V
	Over Operating Range	4.9		5.1	4.85		5.15	V
Line Regulation	V_{IN} = 10 to 40V		10	20		10	30	mV
Load Regulation	I_L = 0 to 20 mA		20	25		20	35	mV
Temperature Stability*	Over Operating Range*		20	25		20	35	mV
Short Circuit Current	V_{REF} = 0, 25°C ≤ T_J ≤ 125°C		80	100		80	100	mA
Output Noise Voltage*	10Hz ≤ f ≤ 10kHz, T_J =25°C		40			40		µVrms
Long Term Stability*	T_J =125°C, 1000 Hrs.		20	50		20	50	mV

** These parameters are guaranteed by design but not 100% tested in production.*

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1524A, -25° to +85°C for the UC2524A, and 0°C to + 70°C for the UC3524A; V_{IN} = V_C = 20V, T_A = T_J.

PARAMETER	TEST CONDITIONS	UC1524A / UC2524A			UC3524A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Oscillator Section (Unless otherwise specified, R_T = 2700Ω, C_T = 0.01 mfd)								
Initial Accuracy	T_J = 25°C	41	43	45	39	43	47	kHz
	Over Operating Range	40.2		45.9	38.2		47.9	kHz
Temperature Stability*	Over Operating Temperature Range		1	2		1	2	%
Minimum Frequency	R_T = 150kΩ, C_T = 0.1mfd			140			120	Hz
Maximum Frequency	R_T = 2.0kΩ, C_T = 470pF	500			500			kHz
Output Amplitude*		3	3.5		3	3.5		V
Output Pulse Width*		0.29	0.5	1.0	0.3	0.5	1.0	µs
Ramp Peak		3.3	3.5	3.7	3.3	3.5	3.7	V
Ramp Valley	T_J = 25°C	0.7	0.8	0.9	0.7	0.8	0.9	V
Ramp Valley T.C.			-1.0			-1.0		mV/°C
Error Amplifier Section (Unless otherwise specified, V_{CM} = 2.5V)								
Input Offset Voltage			0.5	5		2	10	mV
Input Bias Current			1	5		1	10	µA
Input Offset Current			.05	1		0.5	1	µA
Common Mode Rejection Ratio	V_{CM} = 1.5 to 5.5V	70	80		70	80		dB
Power Supply Rejection Ratio	V_{IN} = 10 to 40V	70	80		70	80		dB
Output Swing (Note 1)		5.0		0.5	5.0		0.5	V
Open Loop Voltage Gain	ΔV_O= 1 to 4V, $R_L \geq$ 10MΩ	72	80		64	80		dB
Gain-Bandwidth*	T_J = 25°C, A_V = 0dB	1	3		1	3		MHz
DC Transconductance*§	T_J = 25°C, 30kΩ ≤ R_L ≤ 1MΩ	1.7	2.3		1.7	2.3		mS
P.W.M. Comparator (R_T = 2kΩ, C_T = 0.01mfd)								
Minimum Duty Cycle	V_{COMP} = 0.5V			0			0	%
Maximum Duty Cycle	V_{COMP} = 3.8V	45			45			%
Current Limit Amplifier (Unless otherwise specified, Pin 5 = 0V)								
Input Offset Voltage	T_J = 25°C, E/A Set for Maximum Output	190	200	210	180	200	220	mV
	Over Operating Temperature Range	180		220	170		230	mV
Input Bias Current			-1	-10		-1	-10	µA
Common Mode Rejection Ratio	$V_{(pin\ 5)}$ = -0.3V to + 5.5V	50	60		50	60		dB
Power Supply Rejection Ratio	V_{IN} = 10 to 40V	50	60		50	60		dB
Output Swing (Note 1)	Minimum Total Range	5.0		0.5	5.0		0.5	V
Open-Loop Voltage Gain	ΔV_O = 1 to 4V, $R_L \geq$ 10MΩ	70	80		70	80		dB
Delay Time*	Pin 4 to Pin 9, ΔV_{IN} = 300mV		300			300		ns
Output Section (Each Output)								
Collector Emitter Voltage	I_C = 100µA	60	80		60	80		V
Collector Leakage Current	V_{CE} = 50V		.1	20		.1	20	µA

** These parameters are guaranteed by design but not 100% tested in production.*

§ DC transconductance (g_M) relates to DC open-loop voltage gain according to the following equation: $A_V = g_M R_L$ where R_L is the resistance from pin 9 to the common mode voltage.

The minimum g_M specification is used to calculate minimum A_V when the error amplifier output is loaded.

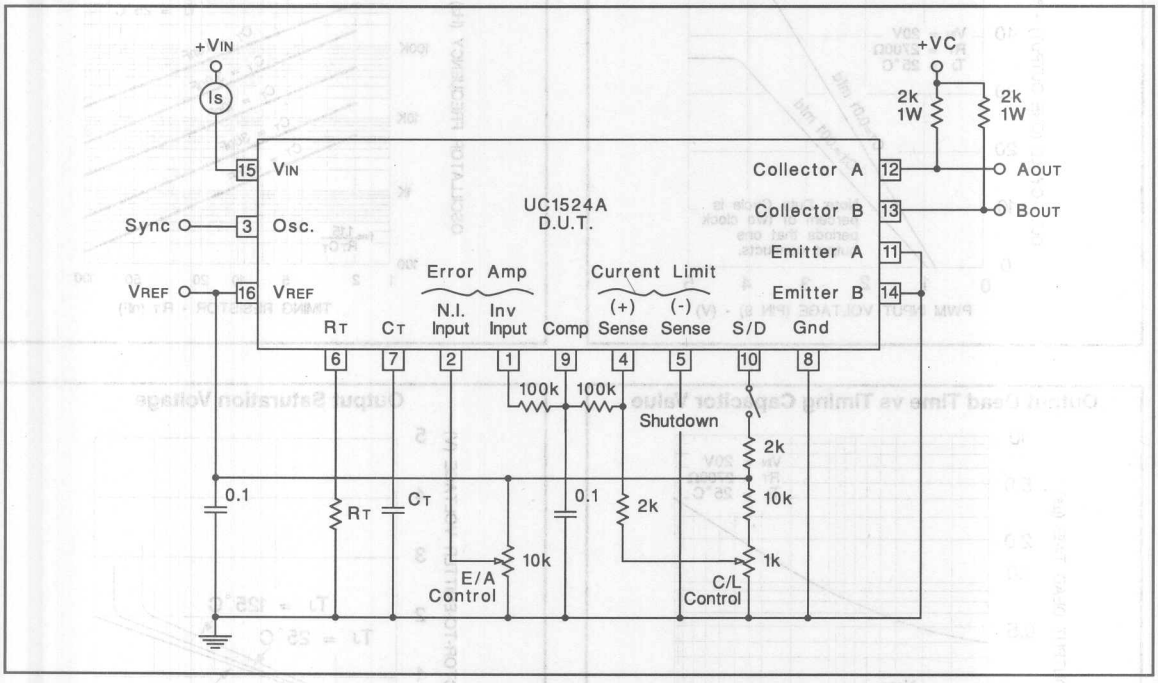
Note 1: Min Limit applies to output high level, max limit applies to output low level.

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1524A, -25° to +85°C for the UC2524A, and 0°C to + 70°C for the UC3524A; V_{IN} = V_C = 20V. T_A = T_J.

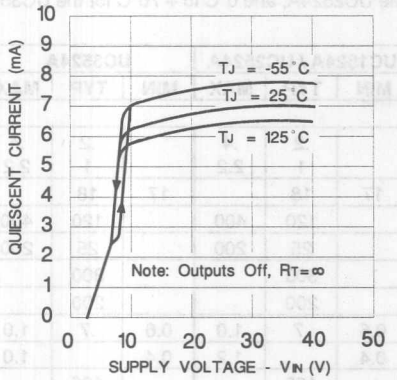
PARAMETER	TEST CONDITIONS	UC1524A / UC2524A			UC3524A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Output Section (cont.) (Each Output)								
Saturation Voltage	I_C = 20mA I_C = 200mA		.2 1	.4 2.2		.2 1	.4 2.2	V V
Emitter Output Voltage	I_E = 50mA	17	18		17	18		V
Rise Time*	T_J = 25°C, R = 2kΩ		120	400		120	400	ns
Fall Time*	T_J = 25°C, R = 2kΩ		25	200		25	200	ns
Comparator Delay*	T_J = 25°C, Pin 9 to output		300			300		ns
Shutdown Delay*	T_J = 25°C, Pin 10 to output		200			200		ns
Shutdown Threshold	T_J = 25°C, R_C = 2kΩ	0.6	.7	1.0	0.6	.7	1.0	V
S/D Threshold Over Temp.	Over Operating Temperature Range	0.4		1.2	0.4		1.0	V
Thermal Shutdown*			165			165		°C

** These parameters are guaranteed by design but not 100% tested in production.*

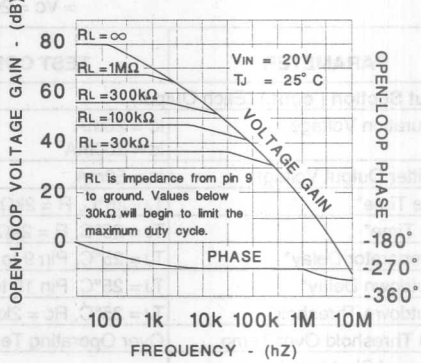
OPEN-LOOP CIRCUIT



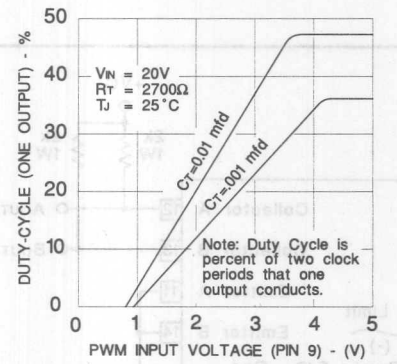
Supply Current vs Voltage



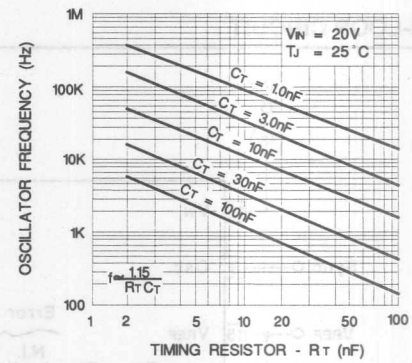
Error Amplifier Voltage Gain and Phase vs Frequency



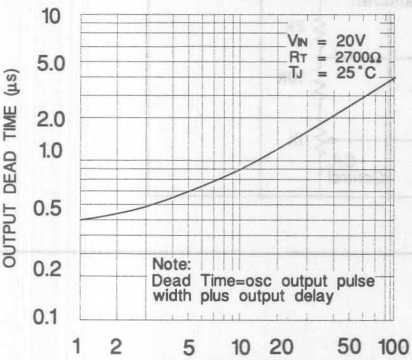
Pulse Width Modulator Transfer Function



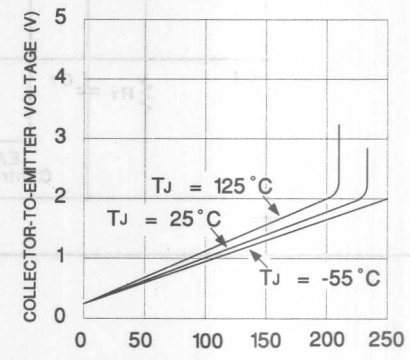
Oscillator Frequency vs Timing Components



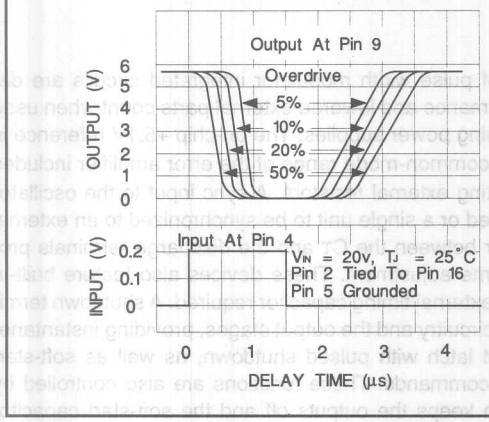
Output Dead Time vs Timing Capacitor Value



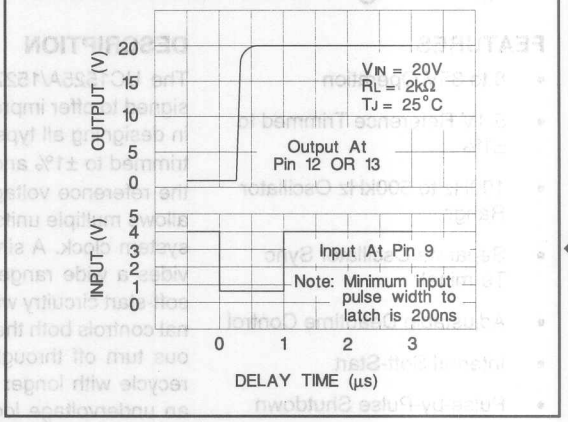
Output Saturation Voltage



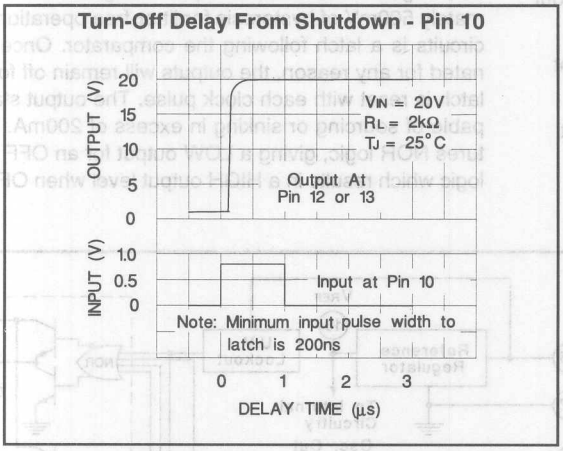
Current Limit Amplifier Delay



Shutdown Delay From PWM Comparator - Pin 9



Turn-Off Delay From Shutdown - Pin 10



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Regulating Pulse Width Modulators

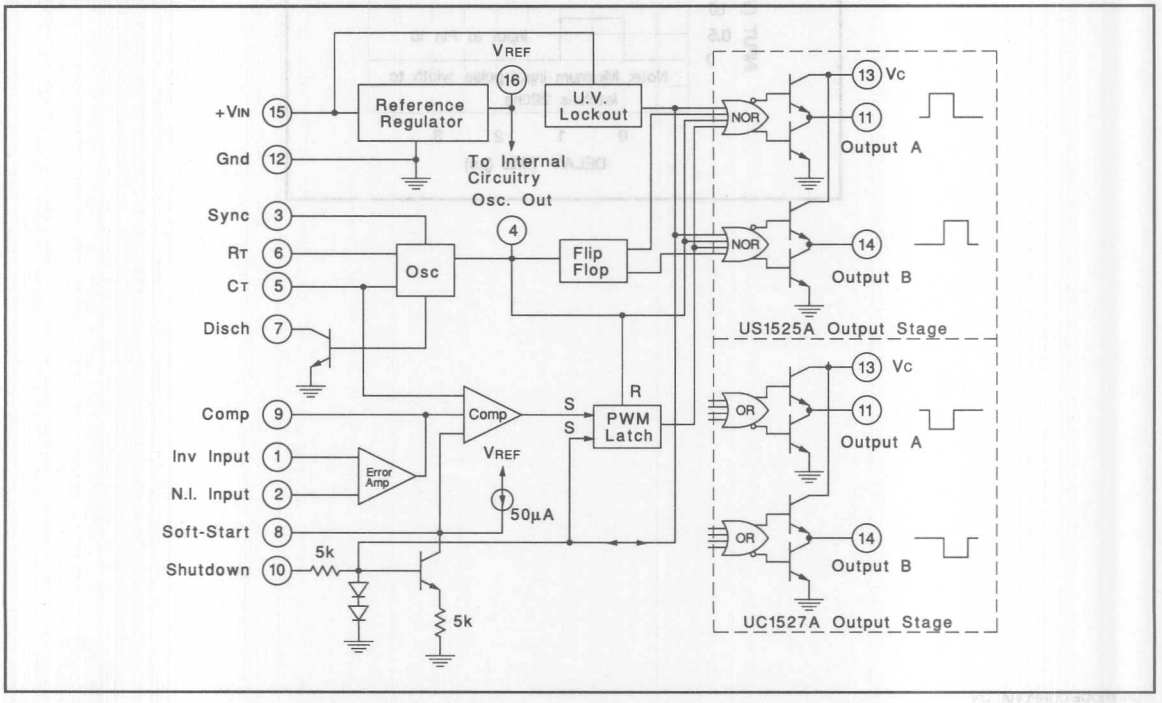
FEATURES

- 8 to 35V Operation
- 5.1V Reference Trimmed to ±1%
- 100Hz to 500kHz Oscillator Range
- Separate Oscillator Sync Terminal
- Adjustable Deadtime Control
- Internal Soft-Start
- Pulse-by-Pulse Shutdown
- Input Undervoltage Lockout with Hysteresis
- Latching PWM to Prevent Multiple Pulses
- Dual Source/Sink Output Drivers

DESCRIPTION

The UC1525A/1527A series of pulse width modulator integrated circuits are designed to offer improved performance and lowered external parts count when used in designing all types of switching power supplies. The on-chip +5.1V reference is trimmed to ±1% and the input common-mode range of the error amplifier includes the reference voltage, eliminating external resistors. A sync input to the oscillator allows multiple units to be slaved or a single unit to be synchronized to an external system clock. A single resistor between the C_T and the discharge terminals provides a wide range of dead-time adjustment. These devices also feature built-in soft-start circuitry with only an external timing capacitor required. A shutdown terminal controls both the soft-start circuitry and the output stages, providing instantaneous turn off through the PWM latch with pulsed shutdown, as well as soft-start recycle with longer shutdown commands. These functions are also controlled by an undervoltage lockout which keeps the outputs off and the soft-start capacitor discharged for sub-normal input voltages. This lockout circuitry includes approximately 500mV of hysteresis for jitter-free operation. Another feature of these PWM circuits is a latch following the comparator. Once a PWM pulse has been terminated for any reason, the outputs will remain off for the duration of the period. The latch is reset with each clock pulse. The output stages are totem-pole designs capable of sourcing or sinking in excess of 200mA. The UC1525A output stage features NOR logic, giving a LOW output for an OFF state. The UC1527A utilizes OR logic which results in a HIGH output level when OFF.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage, (+VIN) . . . . . +40V
Collector Supply Voltage (VC) . . . . . +40V
Logic Inputs . . . . . -0.3V to +5.5V
Analog Inputs . . . . . -0.3V to +VIN
Output Current, Source or Sink 500mA
Reference Output Current 50mA
Oscillator Charging Current 5mA
Power Dissipation at TA = +25°C (Note 2) 1000mW
Power Dissipation at TC = +25°C (Note 2) 2000mW
Operating Junction Temperature . . . . . -55°C to +150°C
Storage Temperature Range . . . . . -65°C to +150°C
Lead Temperature (Soldering, 10 seconds) . . . . . +300°C

Note 1: Values beyond which damage may occur.

Note 2: Consult packaging Section of Databook for thermal limitations and considerations of package.

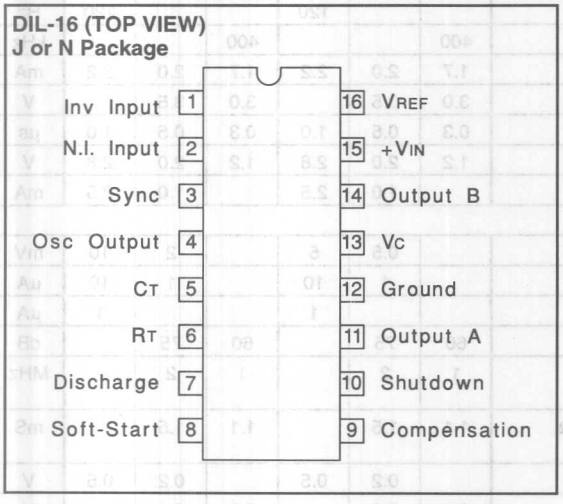
RECOMMENDED OPERATING CONDITIONS (Note 3)

Input Voltage (+VIN) . . . . . +8V to +35V
Collector Supply Voltage (VC) . . . . . +4.5V to +35V
Sink/Source Load Current (steady state) . . . . . 0 to 100mA
Sink/Source Load Current (peak) . . . . . 0 to 400mA
Reference Load Current . . . . . 0 to 20mA
Oscillator Frequency Range . . . . . 100Hz to 400kHz
Oscillator Timing Resistor . . . . . 2kΩ to 150kΩ
Oscillator Timing Capacitor . . . . . .001µF to 0.1µF
Dead Time Resistor Range . . . . . 0 to 500Ω
Operating Ambient Temperature Range
UC1525A, UC1527A . . . . . -55°C to +125°C
UC2525A, UC2527A . . . . . -25°C to +85°C
UC3525A, UC3527A . . . . . 0°C to +70°C

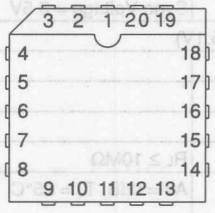
Note 3: Range over which the device is functional and parameter limits are guaranteed.

CONNECTION DIAGRAMS

DIL-16 (TOP VIEW)
J or N Package



PLCC-20, LCC-20 (TOP VIEW)
Q, L Package



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
Inv. Input	2
N.I. Input	3
SYNC	4
OSC. output	5
N/C	6
CT	7
RT	8
Discharge	9
Softstart	10
N/C	11
Compensation	12
Shutdown	13
Output A	14
Ground	15
N/C	16
VC	17
Output B	18
+VIN	19
VREF	20

ELECTRICAL CHARACTERISTICS: +V_{IN} = 20V, and over operating temperature, unless otherwise specified, $T_A = T_J$

PARAMETER	TEST CONDITIONS	UC1525A/UC2525A UC1527A/UC2527A			UC3525A UC3527A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Reference Section								
Output Voltage	T_J = 25°C	5.05	5.10	5.15	5.00	5.10	5.20	V
Line Regulation	V_{IN} = 8 to 35V		10	20		10	20	mV
Load Regulation	I_L = 0 to 20mA		20	50		20	50	mV
Temperature Stability (Note 5)	Over Operating Range		20	50		20	50	
Total Output Variation (Note 5)	Line, Load, and Temperature	5.00		5.20	4.95		5.25	V
Shorter Circuit Current	V_{REF} = 0, T_J = 25°C		80	100		80	100	mA
Output Noise Voltage (Note 5)	10Hz ≤ 10kHz, T_J = 25°C		40	200		40	200	μVrms
Long Term Stability (Note 5)	T_J = 125°C		20	50		20	50	mV
Oscillator Section (Note 6)								
Initial Accuracy (Notes 5 & 6)	T_J = 25°C		± 2	± 6		± 2	± 6	%
Voltage Stability (Notes 5 & 6)	V_{IN} = 8 to 35V		± 0.3	± 1		± 1	± 2	%
Temperature Stability (Note 5)	Over Operating Range		± 3	± 6		± 3	± 6	%
Minimum Frequency	R_T = 200kΩ, C_T = 0.1μF			120			120	Hz
Maximum Frequency	R_T = 2kΩ, C_T = 470pF	400			400			kHz
Current Mirror	I_{RT} = 2mA	1.7	2.0	2.2	1.7	2.0	2.2	mA
Clock Amplitude (Notes 5 & 6)		3.0	3.5		3.0	3.5		V
Clock Width (Notes 5 & 6)	T_J = 25°C	0.3	0.5	1.0	0.3	0.5	1.0	μs
Sync Threshold		1.2	2.0	2.8	1.2	2.0	2.8	V
Sync Input Current	Sync Voltage = 3.5V		1.0	2.5		1.0	2.5	mA
Error Amplifier Section (V_{CM} = 5.1V)								
Input Offset Voltage			0.5	5		2	10	mV
Input Bias Current			1	10		1	10	μA
Input Offset Current				1			1	μA
DC Open Loop Gain	R_L ≥ 10MΩ	60	75		60	75		dB
Gain-Bandwidth Product (Note 5)	A_V = 0dB, T_J = 25°C	1	2		1	2		MHz
DC Transconductance (Notes 5 & 7)	T_J = 25°C, 30kΩ ≤ R_L ≤ 1MΩ	1.1	1.5		1.1	1.5		mS
Output Low Level			0.2	0.5		0.2	0.5	V
Output High Level		3.8	5.6		3.8	5.6		V
Common Mode Rejection	V_{CM} = 1.5 to 5.2V	60	75		60	75		dB
Supply Voltage Rejection	V_{IN} = 8 to 35V	50	60		50	60		dB

Note 5: These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.

Note 6: Tested at f_{OSC} = 40kHz (R_T = 3.6kΩ, C_T = 0.01μF, R_D = 0Ω). Approximate oscillator frequency is defined by:

$$f = \frac{1}{C_T(0.7R_T + 3R_D)}$$

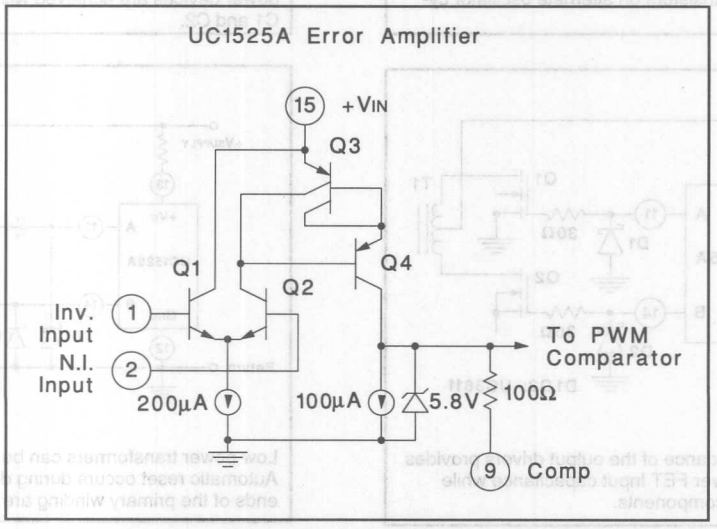
Note 7: DC transconductance (g_M) relates to DC open-loop voltage gain (A_V) according to the following equation: $A_V = g_M R_L$ where R_L is the resistance from pin 9 to ground..

The minimum g_M specification is used to calculate minimum Av when the error amplifier output is loaded.

ELECTRICAL CHARACTERISTICS: +VIN = 20V, and over operating temperature, unless otherwise specified, TA = TJ

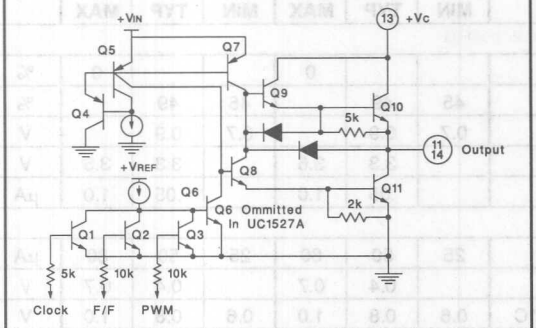
PARAMETER	TEST CONDITIONS	UC1525A/UC2525A UC1527A/UC2527A			UC3525A UC3527A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
PWM Comparator								
Minimum Duty-Cycle				0			0	%
Maximum Duty-Cycle		45	49		45	49		%
Input Threshold (Note 6)	Zero Duty-Cycle	0.7	0.9		0.7	0.9		V
	Maximum Duty-Cycle		3.3	3.6		3.3	3.6	V
Input Bias Current (Note 5)			.05	1.0		.05	1.0	µA
Shutdown Section								
Soft Start Current	VSD = 0V, VSS = 0V	25	50	80	25	50	80	µA
Soft Start Low Level	VSD = 2.5V		0.4	0.7		0.4	0.7	V
Shutdown Threshold	To outputs, VSS = 5.1V, TJ = 25°C	0.6	0.8	1.0	0.6	0.8	1.0	V
Shutdown Input Current	VSD = 2.5V		0.4	1.0		0.4	1.0	mA
Shutdown Delay (Note 5)	VSD = 2.5V, TJ = 25°C		0.2	0.5		0.2	0.5	µs
Output Drivers (Each Output) (VC = 20V)								
Output Low Level	ISINK = 20mA		0.2	0.4		0.2	0.4	V
	ISINK = 100mA		1.0	2.0		1.0	2.0	V
Output High Level	ISOURCE = 20mA	18	19		18	19		V
	ISOURCE = 100mA	17	18		17	18		V
Under-Voltage Lockout	VCOMP and VSS = High	6	7	8	6	7	8	V
VC OFF Current (Note 7)	VC = 35V			200			200	µA
Rise Time (Note 5)	CL = 1nF, TJ = 25°C		100	600		100	600	ns
Fall Time (Note 5)	CL = 1nF, TJ = 25°C		50	300		50	300	ns
Total Standby Current								
Supply Current	VIN = 35V		14	20		14	20	mA

Note 5: These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.
Note 6: Tested at fOSC = 40kHz (RT = 3.6kΩ, CT = 0.01µF, RD = 0Ω).
Note 7: Collector off-state quiescent current measured at pin 13 with outputs low for UC1525A and high for UC1527A.

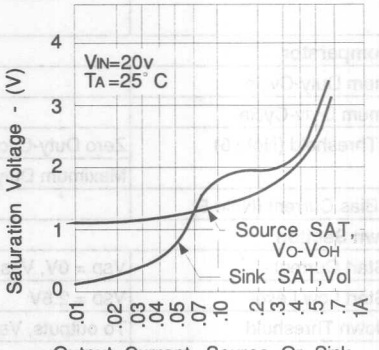


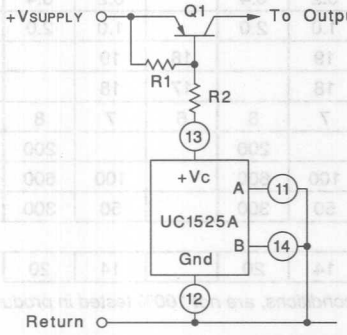
PRINCIPLES OF OPERATION AND TYPICAL CHARACTERISTICS

UC1525A Output Circuit (1/2 Circuit Shown)

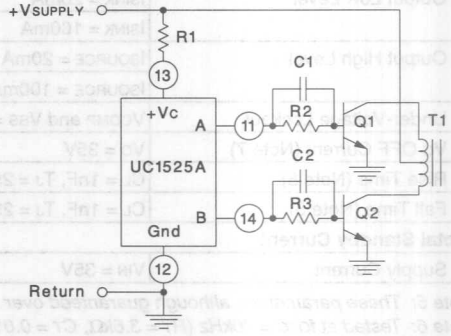


UC1525A Output Saturation Characteristics

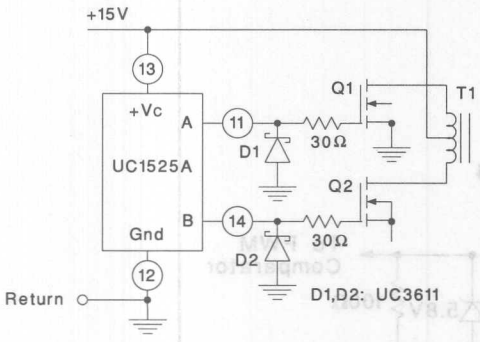




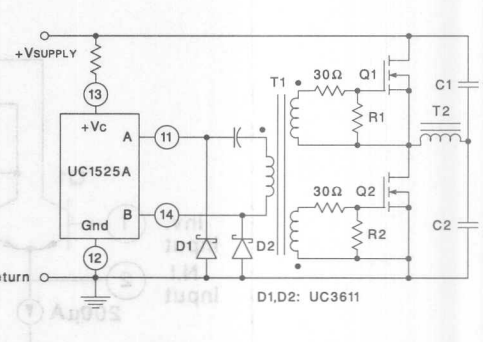
For single-ended supplies, the driver outputs are grounded. The Vc terminal is switched to ground by the totem-pole source transistors on alternate oscillator cycles.



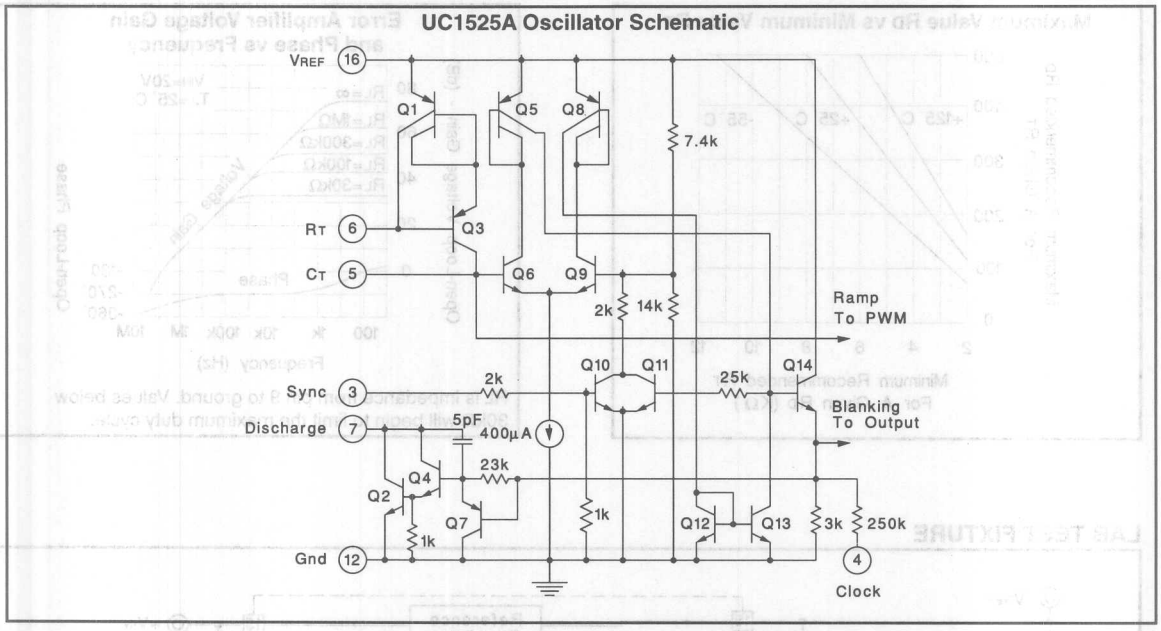
In conventional push-pull bipolar designs, forward base drive is controlled by R1-R3. Rapid turn-off times for the power devices are achieved with speed-up capacitors C1 and C2.



The low source impedance of the output drivers provides rapid charging of power FET Input capacitance while minimizing external components.



Low power transformers can be driven by the UC1525A. Automatic reset occurs during dead time, when both ends of the primary winding are switched to ground.

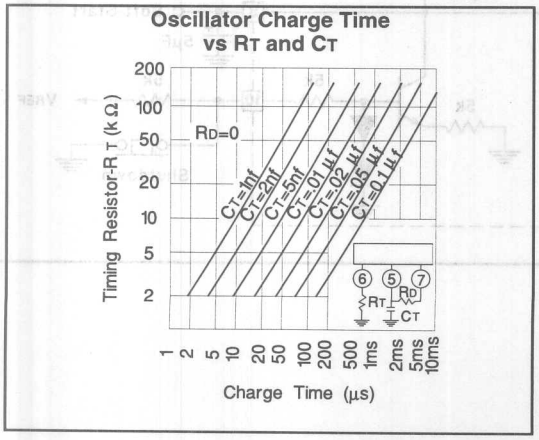


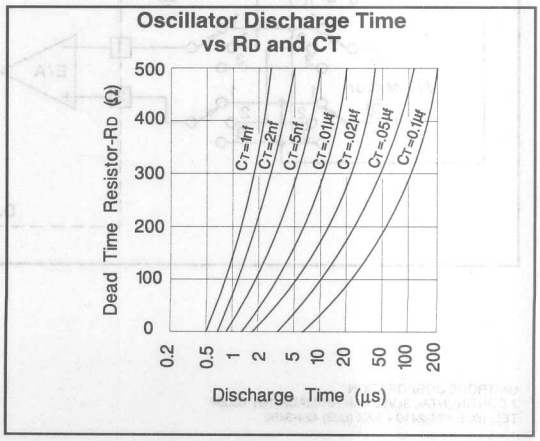
PRINCIPLES OF OPERATION AND TYPICAL CHARACTERISTIC SHUTDOWN OPTIONS
(See Block Diagram)

Since both the compensation and soft-start terminals (Pins 9 and 8) have current source pull-ups, either can readily accept a pull-down signal which only has to sink a maximum of 100µA to turn off the outputs. This is subject to the added requirement of discharging whatever external capacitance may be attached to these pins.

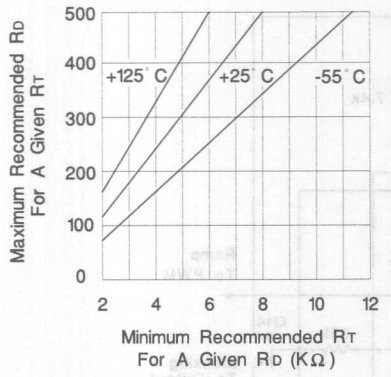
An alternate approach is the use of the shutdown circuitry of Pin 10 which has been improved to enhance the available shutdown options. Activating this circuit by applying a positive signal on Pin 10 performs two functions; the PWM latch is immediately set providing the fastest turn-off signal to the outputs; and a 150µA-current sink begins to discharge the external soft-start capacitor. If the shutdown command is short, the PWM signal is terminated without significant discharge of the soft-start capacitor, thus, allowing, for example, a convenient implementation of pulse-by-pulse current limiting. Holding Pin 10 high for a longer duration, however, will ultimately discharge this external capacitor, recycling slow turn-on upon release.

Pin 10 should not be left floating as noise pickup could conceivably interrupt normal operation.

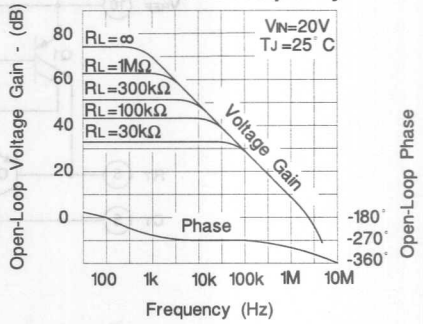




Maximum Value RD vs Minimum Value RT

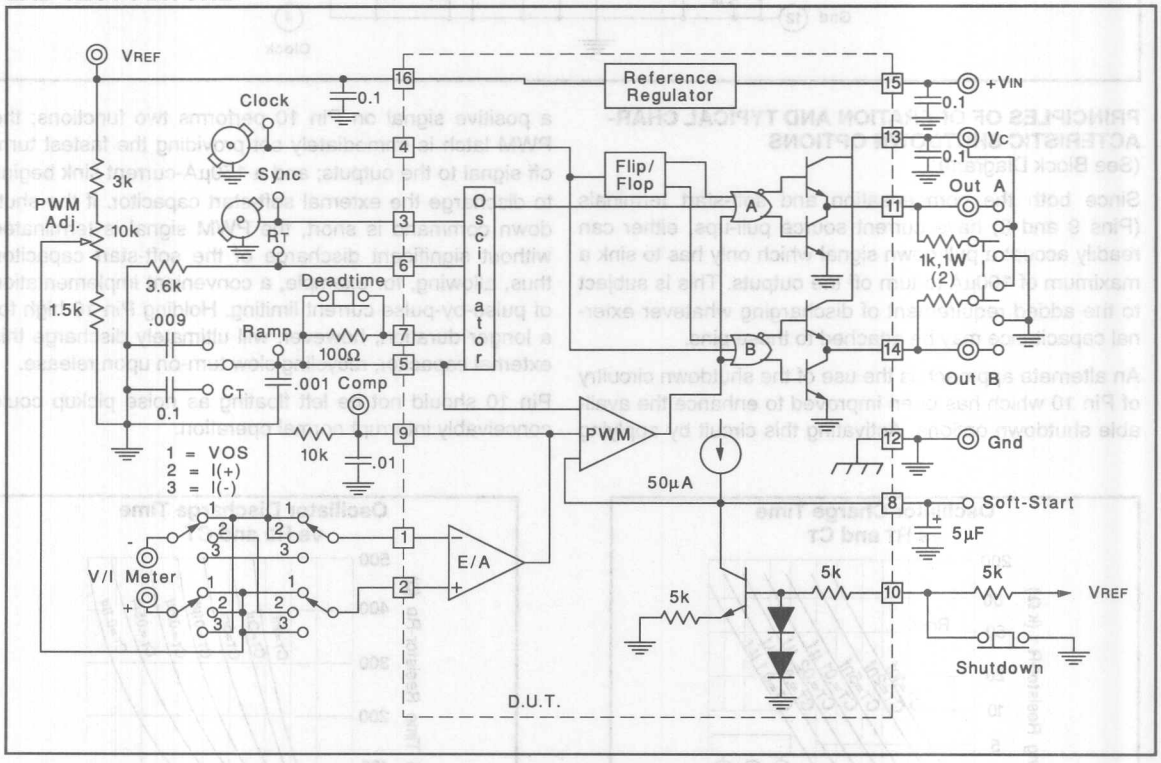


Error Amplifier Voltage Gain and Phase vs Frequency



RL is impedance from pin 9 to ground. Values below 30kΩ will begin to limit the maximum duty cycle.

LAB TEST FIXTURE



UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

UNITRODE

UC1525B UC1527B
UC2525B UC2527B
UC3525B UC3527B

Regulating Pulse Width Modulators

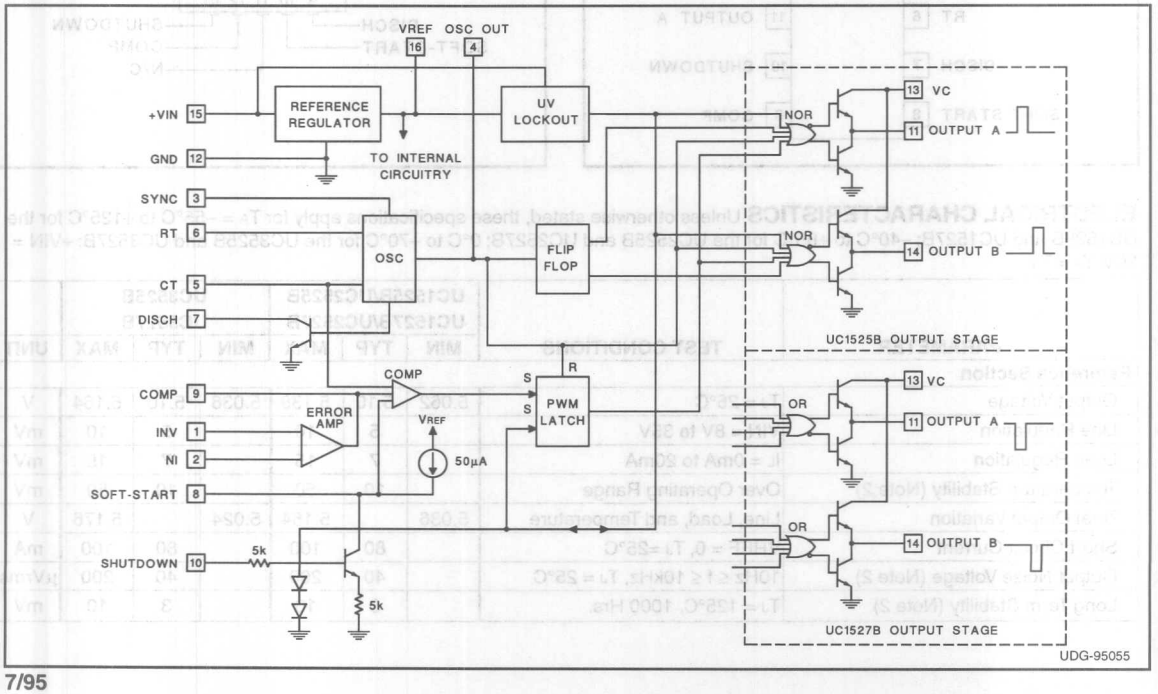
FEATURES

- 8 to 35V Operation
- 5.1V Buried Zener Reference Trimmed to ±0.75%
- 100Hz to 500kHz Oscillator Range
- Separate Oscillator Sync Terminal
- Adjustable Deadtime Control
- Internal Soft-Start
- Pulse-by-Pulse Shutdown
- Input Undervoltage Lockout with Hysteresis
- Latching PWM to Prevent Multiple Pulses
- Dual Source/Sink Output Drivers
- Low Cross Conduction Output Stage
- Tighter Reference Specifications

DESCRIPTION

The UC1525B/1527B series of pulse width modulator integrated circuits are designed to offer improved performance and lowered external parts count when used in designing all types of switching power supplies. The on-chip +5.1V buried zener reference is trimmed to ±0.75% and the input common-mode range of the error amplifier includes the reference voltage, eliminating external resistors. A sync input to the oscillator allows multiple units to be slaved or a single unit to be synchronized to an external system clock. A single resistor between the CT and the discharge terminals provide a wide range of dead time adjustment. These devices also feature built-in soft-start circuitry with only an external timing capacitor required. A shutdown terminal controls both the soft-start circuitry and the output stages, providing instantaneous turn off through the PWM latch with pulsed shutdown, as well as soft-start recycle with longer shutdown commands. These functions are also controlled by an undervoltage lockout which keeps the outputs off and the soft-start capacitor discharged for sub-normal input voltages. This lockout circuitry includes approximately 500mV of hysteresis for jitter-free operation. Another feature of these PWM circuits is a latch following the comparator. Once a PWM pulse has been terminated for any reason, the outputs will remain off for the duration of the period. The latch is reset with each clock pulse. The output stages are totem-pole designs capable of sourcing or sinking in excess of 200mA. The UC1525B output stage features NOR logic, giving a LOW output for an OFF state. The UC1527B utilizes OR logic which results in a HIGH output level when OFF.

BLOCK DIAGRAM



7/95

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, (+VIN) . . . . . +40V
Collector Supply Voltage (VC) . . . . . +40V
Logic Inputs . . . . . –0.3V to +5.5V
Analog Inputs . . . . . –0.3V to VIN
Output Current, Source or Sink 500mA
Reference Output Current 50mA
Oscillator Charging Current 5mA
Power Dissipation at T_A = +25°C 1000mW
Power Dissipation at T_C = +25°C 2000mW
Operating Junction Temperature . . . . . –55°C to +150°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

All currents are positive into, negative out of the specified terminal.
Consult Packaging Section of Databook for thermal limitations and considerations of packages.

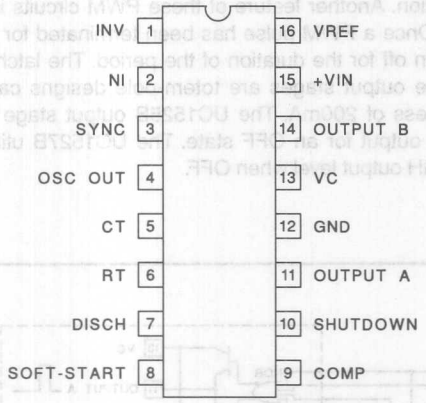
RECOMMENDED OPERATING CONDITIONS (Note 1)

Input Voltage (+VIN) . . . . . +8V to +35V
Collector Supply Voltage (VC) . . . . . +4.5V to +35V
Sink/Source Load Current (steady state) . . . . . 0 to 100mA
Sink/Source Load Current (peak) . . . . . 0 to 400mA
Reference Load Current . . . . . 0 to 20mA
Oscillator Frequency Range . . . . . 100Hz to 400kHz
Oscillator Timing Resistor . . . . . 2kΩ to 150kΩ
Oscillator Timing Capacitor . . . . . 0.001µF to 0.1µF
Dead Time Resistor Range . . . . . 0Ω to 500Ω

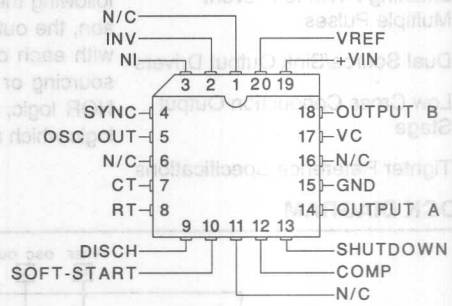
Note 1: Range over which the device is functional and parameter limits are guaranteed.

CONNECTION DIAGRAMS

DIL-16, SOIC-16 (Top View)
J or N Package, DW Package



PLCC-20, LCC-20 (Top View)
Q or L Package



ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply for T_A = –55°C to +125°C for the UC1525B and UC1527B; –40°C to +85°C for the UC2525B and UC2527B; 0°C to +70°C for the UC3525B and UC3527B; +VIN = 20V, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	UC1525B/UC2525B UC1527B/UC2527B			UC3525B UC3527B			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Reference Section								
Output Voltage	T_J = 25°C	5.062	5.10	5.138	5.036	5.10	5.164	V
Line Regulation	VIN = 8V to 35V		5	10		5	10	mV
Load Regulation	I_L = 0mA to 20mA		7	15		7	15	mV
Temperature Stability (Note 2)	Over Operating Range		10	50		10	50	mV
Total Output Variation	Line, Load, and Temperature	5.036		5.164	5.024		5.176	V
Short Circuit Current	VREF = 0, T_J =25°C		80	100		80	100	mA
Output Noise Voltage (Note 2)	10Hz ≤ f ≤ 10kHz, T_J = 25°C		40	200		40	200	µVrms
Long Term Stability (Note 2)	T_J = 125°C, 1000 Hrs.		3	10		3	10	mV

ELECTRICAL CHARACTERISTICS (cont.) Unless otherwise stated, these specifications apply for T_A = –55°C to +125°C for the UC1525B and UC1527B; –40°C to +85°C for the UC2525B and UC2527B; 0°C to +70°C for the UC3525B and UC3527B; +VIN = 20V, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	UC1525B/UC2525B UC1527B/UC2527B			UC3525B UC2527B			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Oscillator Section (Note 3)								
Initial Accuracy (Notes 2 & 3)	T_J = 25°C		±2	±6		±2	±6	%
Voltage Stability (Notes 2 & 3)	VIN = 8V to 35V		±0.3	±1		±1	±2	%
Temperature Stability (Note 2)	Over Operating Range		±3	±6		±3	±6	%
Minimum Frequency	RT = 200kΩ, CT = 0.1µF			120			120	Hz
Maximum Frequency	RT = 2kΩ, CT = 470pF	400			400			kHz
Current Mirror	I_{RT} = 2mA	1.7	2.0	2.2	1.7	2.0	2.2	mA
Clock Amplitude (Notes 2 & 3)		3.0	3.5		3.0	3.5		V
Clock Width (Notes 2 & 3)	T_J = 25°C	0.3	0.5	1.0	0.3	0.5	1.0	µs
Sync Threshold		1.2	2.0	2.8	1.2	2.0	2.8	V
Sync Input Current	Sync Voltage = 3.5V		1.0	2.5		1.0	2.5	mA
Error Amplifier Section (VCM = 5.1V)								
Input Offset Voltage			0.5	5		2	10	mV
Input Bias Current			1	10		1	10	µA
Input Offset Current				1			1	µA
DC Open Loop Gain	RL ≥ 10 MegΩ	60	75		60	75		dB
Gain-Bandwidth Product (Note 2)	Av = 0dB, T_J = 25°C	1	2		1	2		MHz
Output Low Level			0.2	0.5		0.2	0.5	V
Output High Level		3.8	5.6		3.8	5.6		V
Common Mode Rejection	V_{CM} = 1.5V to 5.2V	60	75		60	75		dB
Supply Voltage Rejection	VIN = 8V to 35V	50	60		50	60		dB
PWM Comparator								
Minimum Duty Cycle				0			0	%
Maximum Duty Cycle		45	49		45	49		%
Input Threshold (Note 3)	Zero Duty Cycle	0.7	0.9		0.7	0.9		V
Input Threshold (Note3)	Maximum Duty Cycle		3.3	3.6		3.3	3.6	V
Input Bias Current (Note 2)			0.05	1.0		0.05	1.0	µA
Shutdown Section								
Soft Start Current	$V_{SHUTDOWN}$ = 0V, $V_{SOFTSTART}$ = 0V	25	50	80	25	50	80	µA
Soft Start Low Level	$V_{SHUTDOWN}$ = 2.5V		0.4	0.7		0.4	0.7	V
Shutdown Threshold	To outputs, $V_{SOFTSTART}$ = 5.1V, T_J =25°C	0.6	0.8	1.0	0.6	0.8	1.0	V
Shutdown Input Current	$V_{SHUTDOWN}$ = 2.5V		0.4	1.0		0.4	1.0	mA
Shutdown Delay (Note 2)	$V_{SHUTDOWN}$ = 2.5V, T_J = 25°C		0.2	0.5		0.2	0.5	µs
Output Drivers (Each Output) (VC = 20V)								
Output Low Level	I_{SINK} = 20mA		0.2	0.4		0.2	0.4	V
	I_{SINK} = 100mA		1.0	2.0		1.0	2.0	V
Output HIgh Level	I_{SOURCE} = 20mA	18	19		18	19		V
	I_{SOURCE} = 100mA	17	18		17	18		V
Undervoltage Lockout	V_{COMP} and $V_{SOFTSTART}$ = High	6	7	8	6	7	8	V
Collector Leakage	VC = 35V			200			200	µA

ELECTRICAL CHARACTERISTICS (cont.) Unless otherwise stated, these specifications apply for T_A = –55°C to +125°C for the UC1525B and UC1527B; –40°C to +85°C for the UC2525B and UC2527B; 0°C to +70°C for the UC3525B and UC3527B; +VIN = 20V, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	UC1525B/UC2525B UC1527B/UC2527B			UC3525B UC2527B			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Output Drivers (Each Output) (VC = 20V) (cont.)								
Rise Time (Note 2)	C_L = 1nF, T_J = 25°C		100	600		100	600	ns
Fall Time (Note 2)	C_L = 1nF, T_J = 25°C		50	300		50	300	ns
Cross conduction charge	Per cycle, T_J = 25°C		30			30		nc
Total Standby Current								
Supply Current	VIN = 35V		14	20		14	20	mA

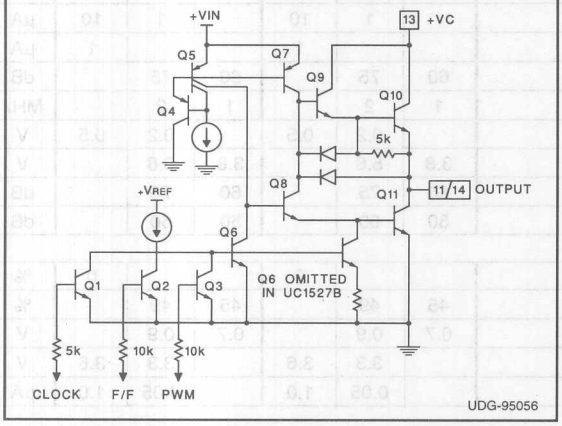
Note 2: Guaranteed by design. Not 100% tested in production.

Note 3. Tested at fosc= 40kHz (R_T = 3.6Ω, C_T = 0.01µF, R_D = 0Ω). Approximate oscillator frequency is defined by:

$$f = \frac{1}{C_T \bullet (0.7 \bullet R_T + 3R_D)}$$

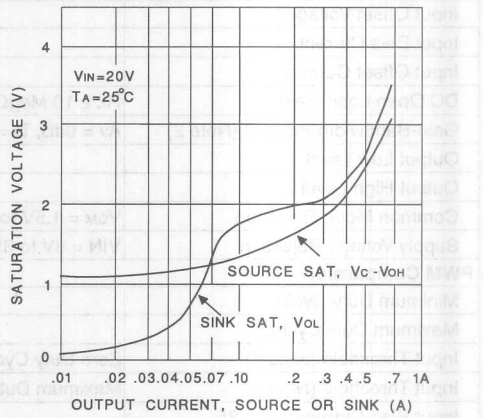
PRINCIPLES OF OPERATION AND TYPICAL CHARACTERISTICS

UC1525B Output Circuit (1/2 Circuit Shown)

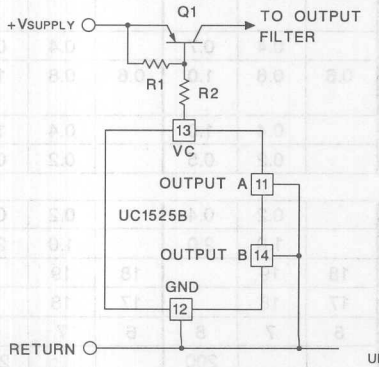


UDG-95056

UC1525B Output Saturation Characteristics

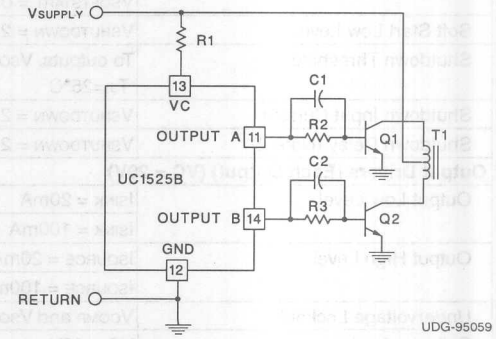


UDG-95057



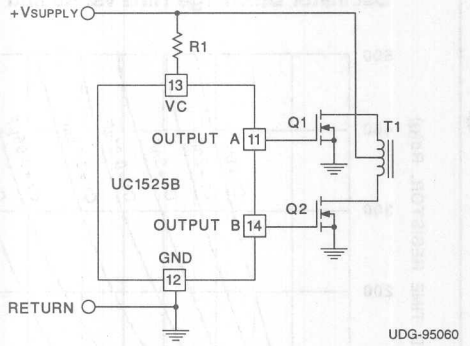
UDG-95058

For single-ended supplies, the driver outputs are grounded. The VC terminal is switched to ground by the totem-pole source transistors on alternate oscillator cycles.

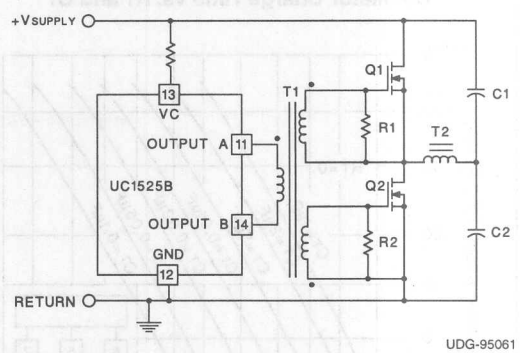


UDG-95059

In conventional push-pull bipolar designs, forward base drive is controlled by R1-R3. Rapid turn-off times for the power devices are achieved with speed-up capacitors C, and C2.



The low source impedance of the output drivers provides rapid charging of power FET input capacitance while minimizing external components.



Low power transformers can be driven directly by the UC1525B. Automatic reset occurs during dead time, when both ends of the primary winding are switched to ground.

PRINCIPLES OF OPERATION AND TYPICAL CHARACTERISTICS

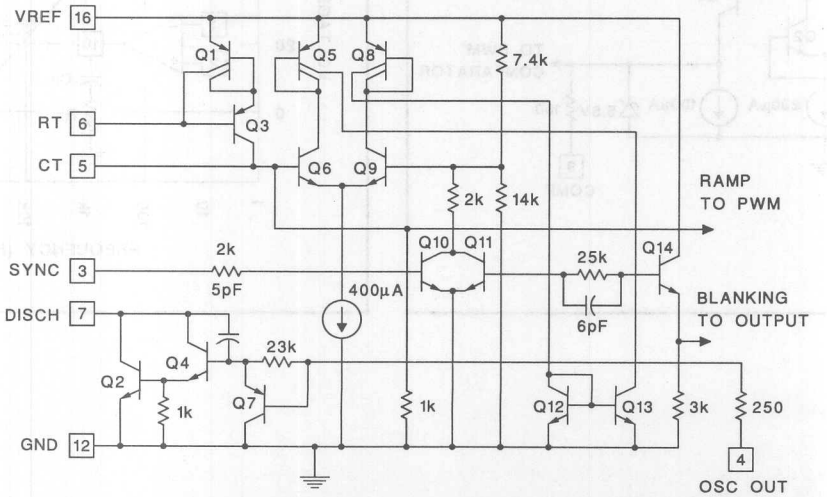
Shutdown Options (See Block Diagram)

Since both the compensation and soft-start terminals (Pins 9 and 8) have current source pull-ups, either can readily accept a pull-down signal which only has to sink a maximum of 100µA to turn off the outputs. This is subject to the added requirement of discharging whatever external capacitance may be attached to these pins.

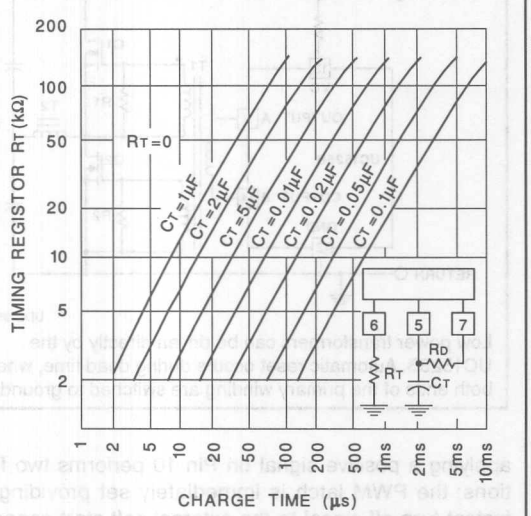
An alternate approach is the use of the shutdown circuitry of Pin 10 which has been improved to enhance the available shutdown options. Activating this circuit by applying a positive signal on Pin 10 performs two functions: the PWM latch is immediately set providing the fastest turn-off signal to the external soft-start capacitor. If the shutdown command is short, the PWM signal is terminated without significant discharge of the soft-start capacitor, thus, allowing, for example, a convenient implementation of pulse-by-pulse current limiting. Holding Pin 10 high for a longer duration, however, will ultimately discharge this external capacitor, recycling slow turn-on upon release.

Pin 10 should not be left floating as noise pickup could conceivably interrupt normal operation.

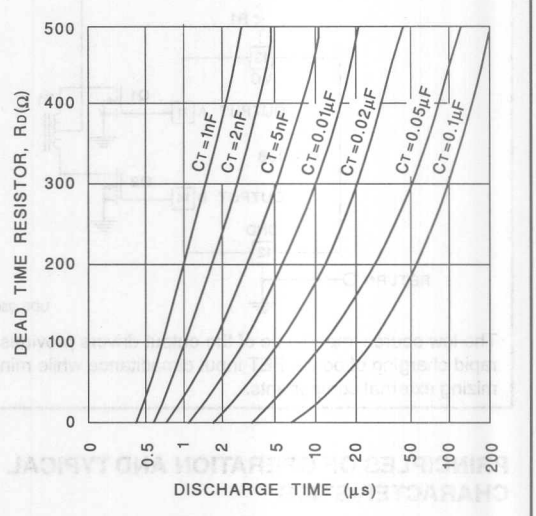
UC1525B Oscillator Schematic



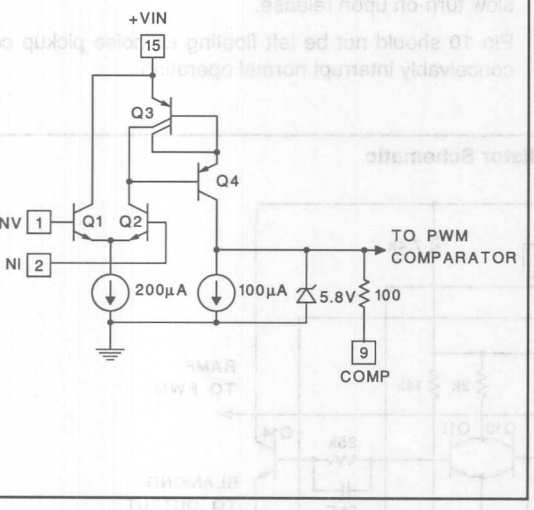
Oscillator Charge Time vs. R_T and C_T



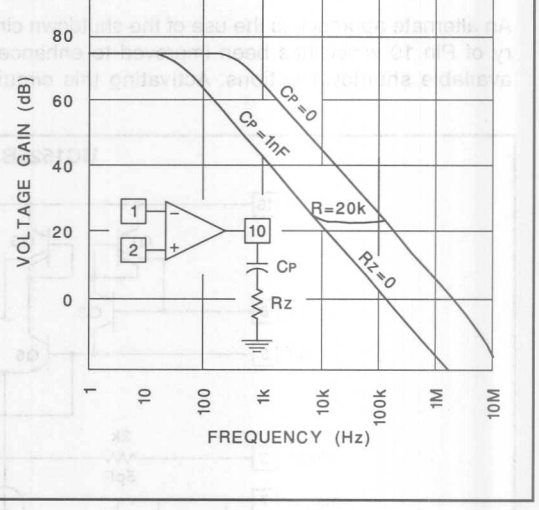
Oscillator Discharge Time vs. R_D and C_T



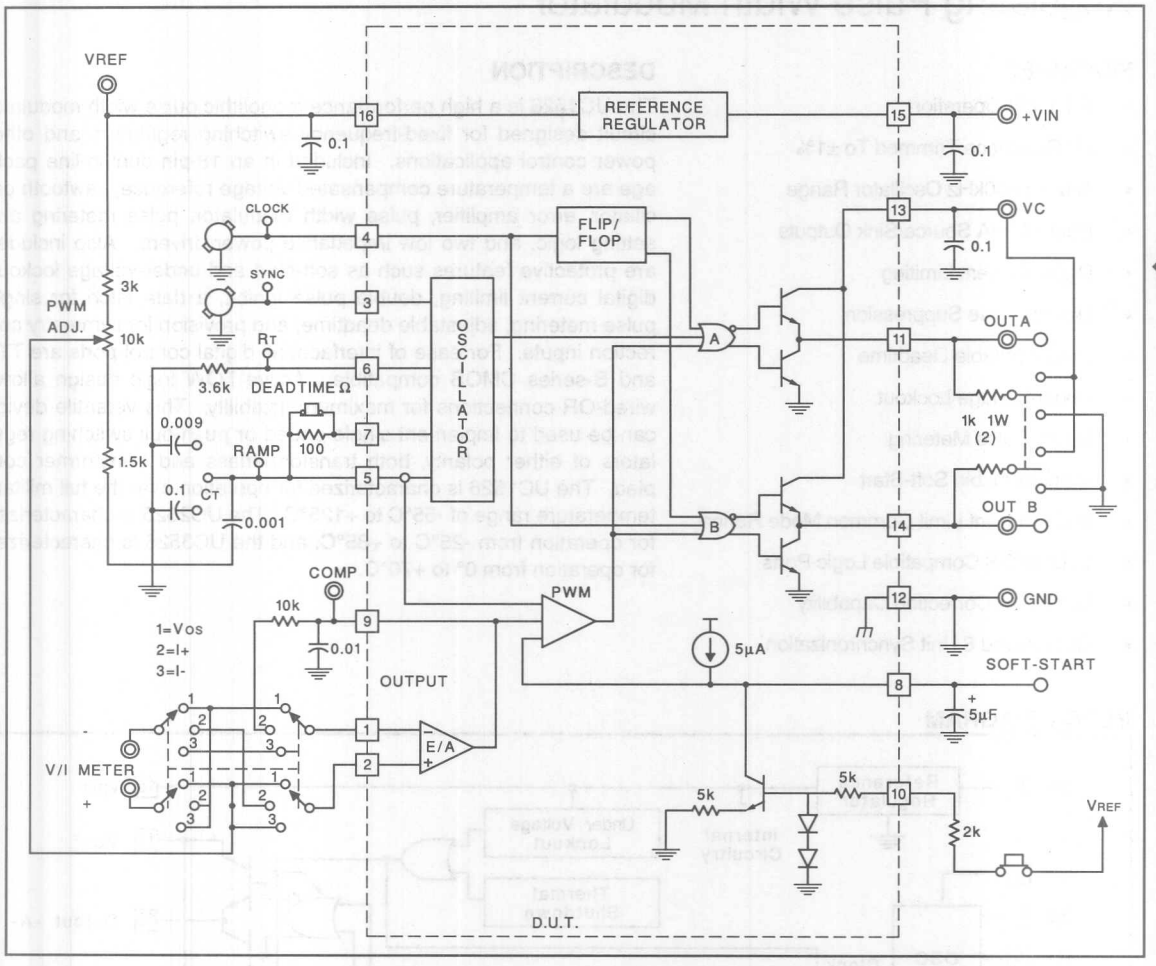
UC1525B Error Amplifier



Error Amplifier Open-Loop Frequency Response



LAB TEST FIXTURE



UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

UNITRODE

UC1526
UC2526
UC3526

Regulating Pulse Width Modulator

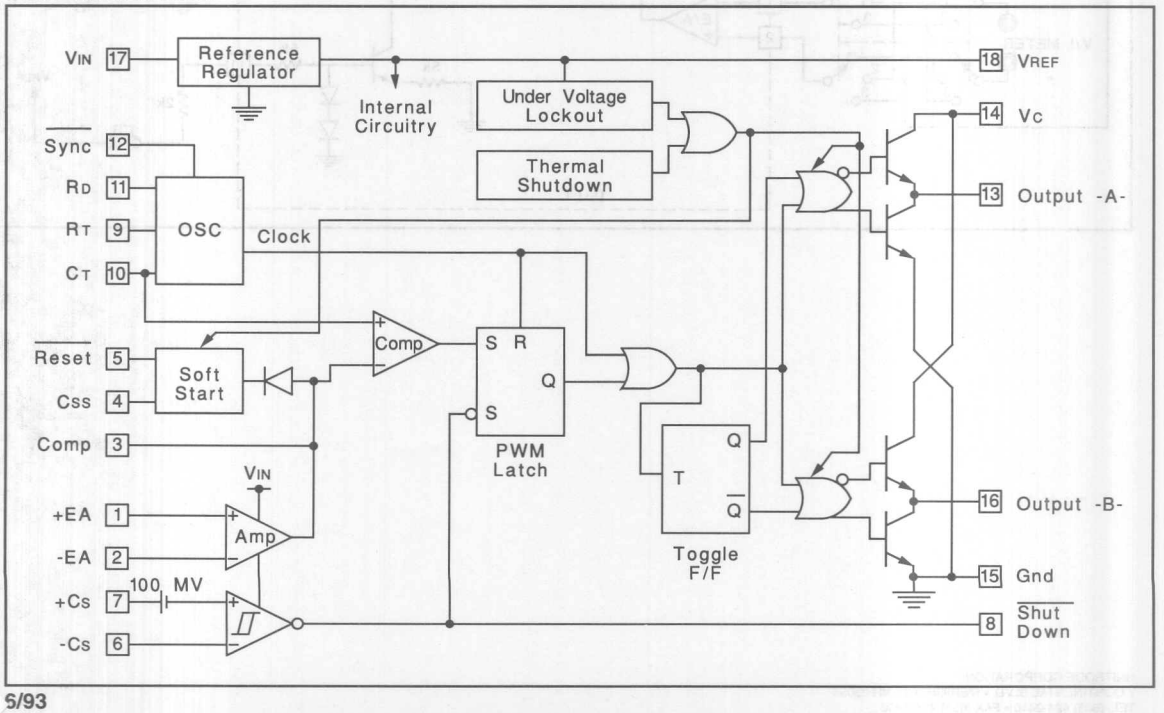
FEATURES

- 8 To 35V Operation
- 5V Reference Trimmed To ±1%
- 1Hz To 400kHz Oscillator Range
- Dual 100mA Source/Sink Outputs
- Digital Current Limiting
- Double Pulse Suppression
- Programmable Deadtime
- Under-Voltage Lockout
- Single Pulse Metering
- Programmable Soft-Start
- Wide Current Limit Common Mode Range
- TTL/CMOS Compatible Logic Ports
- Symmetry Correction Capability
- Guaranteed 6 Unit Synchronization

DESCRIPTION

The UC1526 is a high performance monolithic pulse width modulator circuit designed for fixed-frequency switching regulators and other power control applications. Included in an 18-pin dual-in-line package are a temperature compensated voltage reference, sawtooth oscillator, error amplifier, pulse width modulator, pulse metering and setting logic, and two low impedance power drivers. Also included are protective features such as soft-start and under-voltage lockout, digital current limiting, double pulse inhibit, a data latch for single pulse metering, adjustable deadtime, and provision for symmetry correction inputs. For ease of interface, all digital control ports are TTL and B-series CMOS compatible. Active LOW logic design allows wired-OR connections for maximum flexibility. This versatile device can be used to implement single-ended or push-pull switching regulators of either polarity, both transformerless and transformer coupled. The UC1526 is characterized for operation over the full military temperature range of -55°C to +125°C. The UC2526 is characterized for operation from -25°C to +85°C, and the UC3526 is characterized for operation from 0° to +70°C.

BLOCK DIAGRAM



6/93

ABSOLUTE MAXIMUM RATINGS (Note 1, 2)

Input Voltage (+VIN) ..... +40V
Collector Supply Voltage (+VC) ..... +40V
Logic Inputs ..... -0.3V to +5.5V
Analog Inputs ..... -0.3V to +VIN
Source/Sink Load Current (each output) 200mA
Reference Load Current 50mA
Logic Sink Current 15mA
Power Dissipation at TA = +25°C (Note 2) 1000mW
Power Dissipation at TC = +25°C (Note 2) 3000mW
Operating Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10 seconds) ..... +300°C

Note 1: Values beyond which damage may occur.
Note 2: Consult packaging section of databook for thermal limitations and considerations of package.

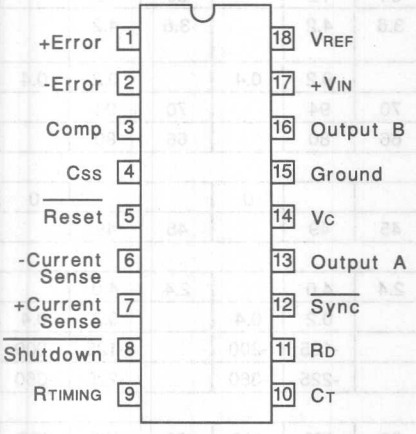
RECOMMENDED OPERATING CONDITIONS (Note 3)

Input Voltage ..... +8V to +35V
Collector Supply Voltage ..... +4.5V to +35V
Sink/Source Load Current (each output) ..... 0 to 100mA
Reference Load Current ..... 0 to 20mA
Oscillator Frequency Range ..... 1Hz to 400kHz
Oscillator Timing Resistor ..... 2kΩ to 150kΩ
Oscillator Timing Capacitor ..... 1nF to 20µF
Available Deadtime Range at 40kHz ..... 3% to 50%
Operating Ambient Temperature Range
UC1526 ..... -55°C to +125°C
UC2526 ..... -25°C to +85°C
UC3526 ..... -0°C to +70°C

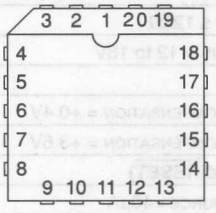
Note 3: Range over which the device is functional and parameter limits are guaranteed.

CONNECTION DIAGRAMS

DIL-18, SOIC-18 (TOP VIEW)
J or N Package, DW Package



PLCC-20, LCC-20
(TOP VIEW)
Q and L Packages



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
+Error	2
-Error	3
Comp.	4
Css	5
Reset	6
- Current Sense	7
+ Current Sense	8
Shutdown	9
RTIMING	10
CT	11
RD	12
Sync	13
Output A	14
VC	15
N/C	16
Ground	17
Output B	18
+VIN	19
VREF	20

ELECTRICAL CHARACTERISTICS: +VIN = 15V, and over operating ambient temperature, unless otherwise specified, TA = TJ.

PARAMETER	TEST CONDITIONS	UC1526 / UC2526			UC3526			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Reference Section (Note 4)								
Output Voltage	TJ = + 25°C	4.95	5.00	5.05	4.90	5.00	5.10	V
Line Regulation	+VIN = 8 to 35V		10	20		10	30	mV
Load Regulation	IL = 0 to 20mA		10	30		10	50	mV
Temperature Stability	Over Operating TJ		15	50		15	50	mV
Total Output Voltage Range	Over Recommended Operating Conditions	4.90	5.00	5.10	4.85	5.00	5.15	V
Short Circuit Current	VREF = 0V	25	50	100	25	50	100	mA
Under -Voltage Lockout								
RESET Output Voltage	VREF = 3.8V		0.2	0.4		0.2	0.4	V
	VREF = 4.8V	2.4	4.8		2.4	4.8		V

Note 4: IL = 0mA.

ELECTRICAL CHARACTERISTICS: +V_{IN} = 15V, and over operating ambient temperature, unless otherwise specified, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	UC1526 / UC2526			UC3526			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Oscillator Section (Note 5)								
Initial Accuracy	T_J = + 25°C		±3	±8		±3	±8	%
Voltage Stability	+V_{IN} = 8 to 35V		0.5	1		0.5	1	%
Temperature Stability	Over Operating T_J		7	10		3	5	%
Minimum Frequency	R_T = 150kΩ, C_T = 20µF			1			1	Hz
Maximum Frequency	R_T = 2kΩ, C_T = 1.0nF	400			400			kHz
Sawtooth Peak Voltage	+V_{IN} = 35V		3.0	3.5		3.0	3.5	V
Sawtooth Valley Voltage	+V_{IN} = 8V	0.5	1.0		0.5	1.0		V
Error Amplifier Section (Note 6)								
Input Offset Voltage	R_S ≤ 2kΩ		2	5		2	10	mV
Input Bias Current			-350	-1000		-350	-2000	nA
Input Offset Current			35	100		35	200	nA
DC Open Loop Gain	R_L ≥ 10MΩ	64	72		60	72		dB
HIGH Output Voltage	V_{PIN1}-V_{PIN2} ≥ 150mV, I_{SOURCE} = 100µA	3.6	4.2		3.6	4.2		V
LOW Output Voltage	V_{PIN2}-V_{PIN1} ≥ 150mV, I_{SINK} = 100µA		0.2	0.4		0.2	0.4	V
Common Mode Rejection	R_S ≤ 12kΩ	70	94		70	94		dB
Supply Voltage Rejection	+V_{IN} = 12 to 18V	66	80		66	80		dB
PWM Comparator (Note 5)								
Minimum Duty Cycle	$V_{COMPENSATION}$ = +0.4V			0			0	%
Maximum Duty Cycle	$V_{COMPENSATION}$ = +3.6V	45	49		45	49		%
Digital Ports ($\overline{SYNC}$, $\overline{SHUTDOWN}$, and $\overline{RESET}$)								
HIGH Output Voltage	I_{SOURCE} =40µA	2.4	4.0		2.4	4.0		V
LOW Output Voltage	I_{SINK} = 3.6mA		0.2	0.4		0.2	0.4	V
HIGH Input Current	V_{IH} = +2.4V		-125	-200		-125	-200	µA
LOW Input Current	V_{IL} = +0.4V		-225	-360		-225	-360	µA
Current Limit Comparator (Note 7)								
Sense Voltage	R_S ≤ 50Ω	90	100	110	80	100	120	mV
Input Bias Current			-3	-10		-3	-10	µA
Soft-Start Section								
Error Clamp Voltage	$\overline{RESET}$ = +0.4V		0.1	0.4		0.1	0.4	V
Cs Charging Current	$\overline{RESET}$ =+2.4V	50	100	150	50	100	150	µA
Output Drivers (Each Output) (Note 8)								
HIGH Output Voltage	I_{SOURCE} = 20mA	12.5	13.5		12.5	13.5		V
	I_{SOURCE} = 100mA	12	13		12	13		V
LOW Output Voltage	I_{SINK} = 20mA		0.2	0.3		0.2	0.3	V
	I_{SINK} = 100mA		1.2	2.0		1.2	2.0	V
Collector Leakage	V_C = 40V		50	150		50	150	µA
Rise Time	C_L = 1000pF		0.3	0.6		0.3	0.6	µs
Fall Time	C_L = 1000pF		0.1	0.2		0.1	0.2	µs
Power Consumption (Note 9)								
Standby Current	$\overline{SHUTDOWN}$ = +0.4V		18	30		18	30	mA

Note 4: I_L = 0mA.
Note 5: F_{OSC} = 40kHz (R_T = 4.12kΩ ± 1%, C_T = 0.1µF ± 1%, R_D = 0Ω)
Note 6: V_{CM} = 0 to +5.2V
Note 8: V_C = +15V
Note 9: +V_{IN} = +35V, R_T = 4.12kΩ

APPLICATIONS INFORMATION

Voltage Reference

The reference regulator of the UC1526 is based on a temperature compensated zener diode. The circuitry is fully active at supply voltages above +8V, and provides up to 20mA of load current to external circuitry at +5.0V. In systems where additional current is required, an external PNP transistor can be used to boost the available current. A rugged low frequency audio-type transistor should be used, and lead lengths between the PWM and transistor should be as short as possible to minimize the risk of oscillations. Even so, some types of transistors may require collector-base capacitance for stability. Up to 1 amp of load current can be obtained with excellent regulation if the device selected maintains high current gain.

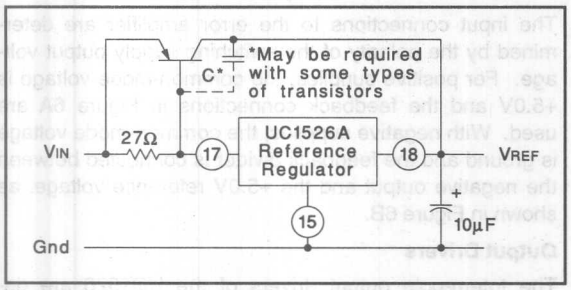


Figure 1. Extending Reference Output Current

Under-Voltage Lockout

The under-voltage lockout circuit protects the UC1526 and the power devices it controls from inadequate supply voltage, If +VIN is too low, the circuit disables the output drivers and holds the $\overline{\text{RESET}}$ pin LOW. This prevents spurious output pulses while the control circuitry is stabilizing, and holds the soft-start timing capacitor in a discharged state.

The circuit consists of a +1.2V bandgap reference and comparator circuit which is active when the reference voltage has risen to 3VBE or +1.8V at 25°C. When the reference voltage rises to approximately +4.4V, the circuit enables the output drivers and releases the $\overline{\text{RESET}}$ pin, allowing a normal soft-start. The comparator has 200mV of hysteresis to minimize oscillation at the trip point. When +VIN to the PWM is removed and the reference drops to +4.2V, the under-voltage circuit pulls $\overline{\text{RESET}}$ LOW again. The soft-start capacitor is immediately discharged, and the PWM is ready for another soft-start cycle.

The UC1526 can operate from a +5V supply by connecting the VREF pin to the +VIN pin and maintaining the supply between +4.8 and +5.2V.

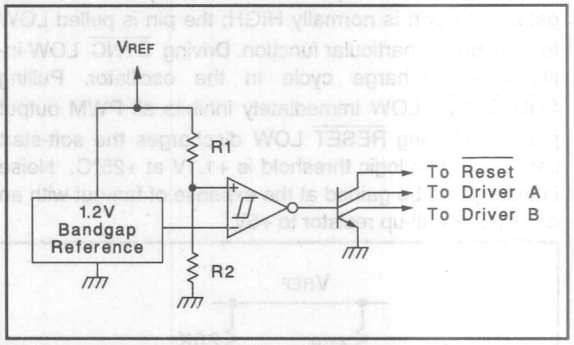


Figure 2. Under-Voltage Lockout Schematic

Soft-Start Circuit

The soft-start circuit protects the power transistors and rectifier diodes from high current surges during power supply turn-on. When supply voltage is first applied to the UC1526, the under-voltage lockout circuit holds $\overline{\text{RESET}}$ LOW with Q3. Q1 is turned on, which holds the soft-start capacitor voltage at zero. The second collector of Q1 clamps the output of the error amplifier to ground, guaranteeing zero duty cycle at the driver outputs. When the supply voltage reaches normal operating range, $\overline{\text{RESET}}$ will go HIGH. Q1 turns off, allowing the internal 100mA current source to charge CS. Q2 clamps the error amplifier output to 1VBE above the voltage on CS. As the soft-start voltage ramps up to +5V, the duty cycle of the PWM linearly increases to whatever value the voltage regulation loop requires for an error null.

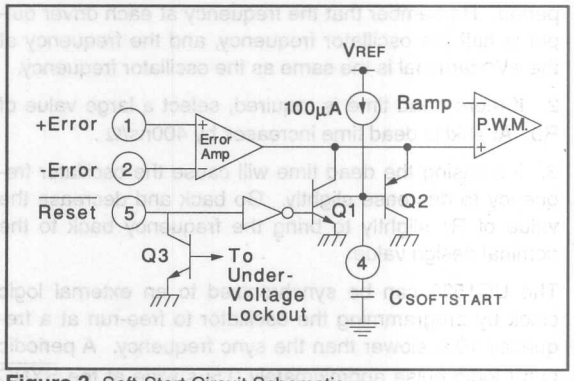


Figure 3. Soft-Start Circuit Schematic

Digital Control Ports

The three digital control ports of the UC1526 are bi-directional. Each pin can drive TTL and 5V CMOS logic directly, up to a fan-out of 10 low-power Schottky gates. Each pin can also be directly driven by open-collector

APPLICATIONS INFORMATION (cont.)

TTL, open-drain CMOS, and open-collector voltage comparators; fan-in is equivalent to 1 low-power Schottky gate. Each port is normally HIGH; the pin is pulled LOW to activate the particular function. Driving $\overline{\text{SYNC}}$ LOW initiates a discharge cycle in the oscillator. Pulling $\overline{\text{SHUTDOWN}}$ LOW immediately inhibits all PWM output pulses. Holding $\overline{\text{RESET}}$ LOW discharges the soft-start capacitor. The logic threshold is +1.1V at +25°C. Noise immunity can be gained at the expense of fan-out with an external 2k pull-up resistor to +5V.

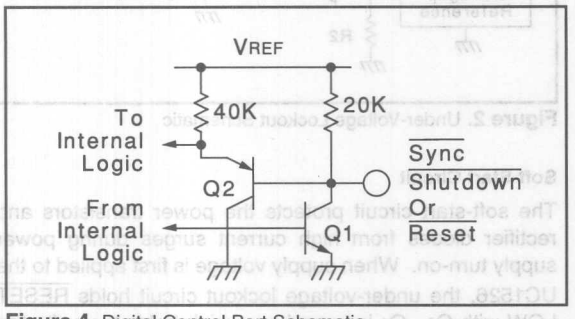


Figure 4. Digital Control Port Schematic

Oscillator

The oscillator is programmed for frequency and dead time with three components: RT, CT and RD. Two waveforms are generated: a sawtooth waveform at pin 10 for pulse width modulation, and a logic clock at pin 12. The following procedure is recommended for choosing timing values:

1. With RD = 0 (pin 11 shorted to ground) select values for RT and CT from Figure 7 to give the desired oscillator period. Remember that the frequency at each driver output is half the oscillator frequency, and the frequency at the +VC terminal is the same as the oscillator frequency.

2. If more dead time is required, select a large value of RD. At 40kHz dead time increases by 400ns/Ω .

3. Increasing the dead time will cause the oscillator frequency to decrease slightly. Go back and decrease the value of RT slightly to bring the frequency back to the nominal design value.

The UC1526 can be synchronized to an external logic clock by programming the oscillator to free-run at a frequency 10% slower than the sync frequency. A periodic LOW logic pulse approximately 0.5µs wide at the $\overline{\text{SYNC}}$ pin will then lock the oscillator to the external frequency.

Multiple devices can be synchronized together by programming one master unit for the desired frequency and then sharing its sawtooth and clock waveforms with the slave units. All CT terminals are connected to the CT pin of the master, and all $\overline{\text{SYNC}}$ terminals are likewise connected to the $\overline{\text{SYNC}}$ pin of the master. Slave RT terminals are left open or connected to VREF. Slave RD terminals may be either left open or grounded.

Error Amplifier

The error amplifier is a transconductance design, with an output impedance of 2MΩ . Since all voltage gain takes place at the output pin, the open-loop gain/frequency characteristics can be controlled with shunt reactance to ground. When compensated for unity-gain stability with 100pF, the amplifier has an open-loop pole at 800Hz.

The input connections to the error amplifier are determined by the polarity of the switching supply output voltage. For positive supplies, the common-mode voltage is +5.0V and the feedback connections in Figure 6A are used. With negative supplies, the common-mode voltage is ground and the feedback divider is connected between the negative output and the +5.0V reference voltage, as shown in Figure 6B.

Output Drivers

The totem-pole output drivers of the UC1526 are designed to source and sink 100mA continuously and 200mA peak. Loads can be driven either from the output pins 13 and 16, or from the +VC, as required.

Since the bottom transistor of the totem-pole is allowed to saturate, there is a momentary conduction path from the +VC terminal to ground during switching. To limit the resulting current spikes a small resistor in series with pin 14 is always recommended. The resistor value is determined by the driver supply voltage, and should be chosen for 200mA peak currents.

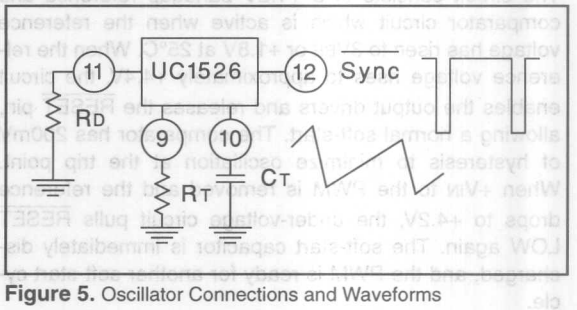


Figure 5. Oscillator Connections and Waveforms

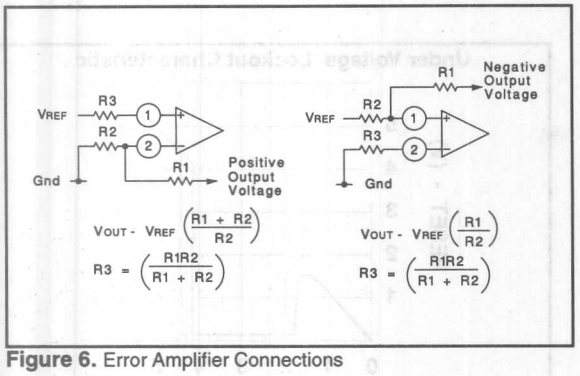


Figure 6. Error Amplifier Connections

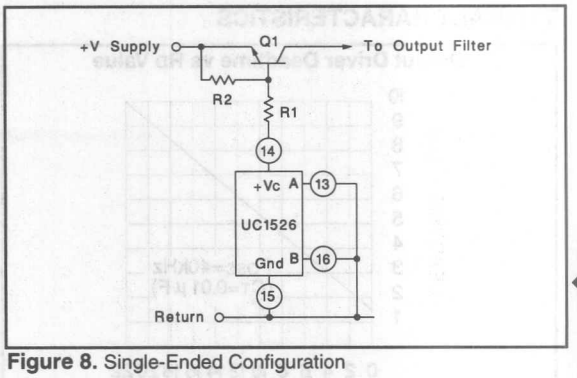


Figure 8. Single-Ended Configuration

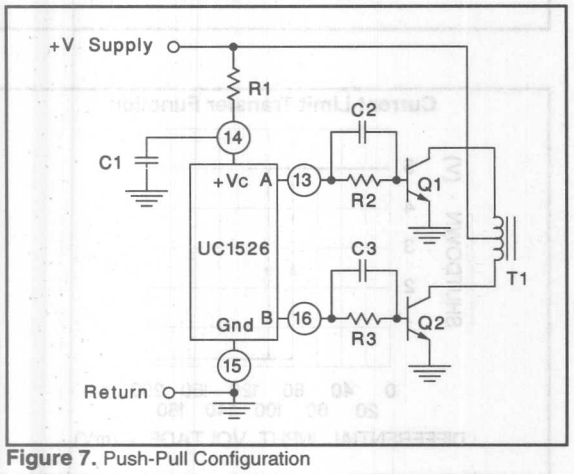


Figure 7. Push-Pull Configuration

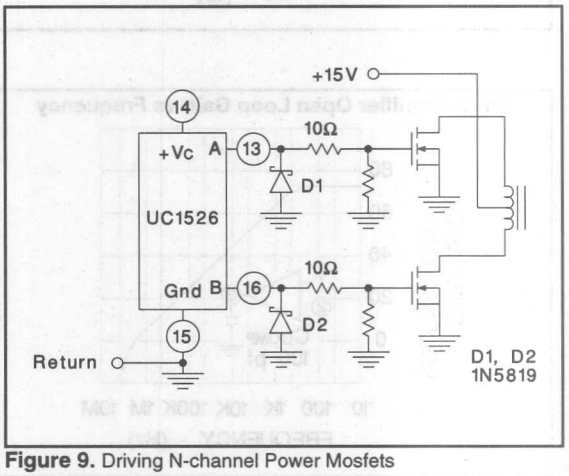
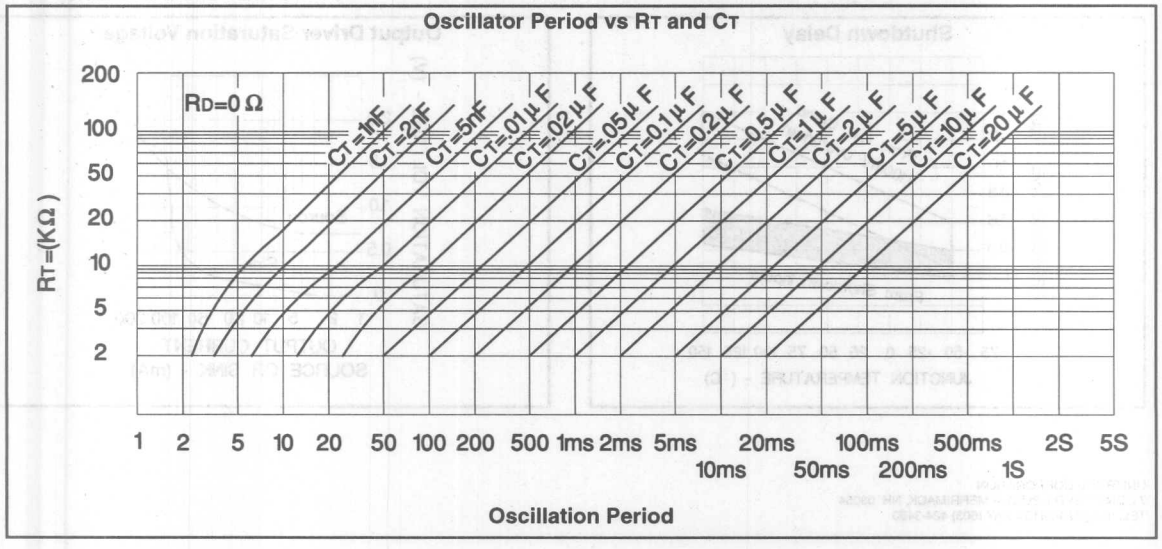


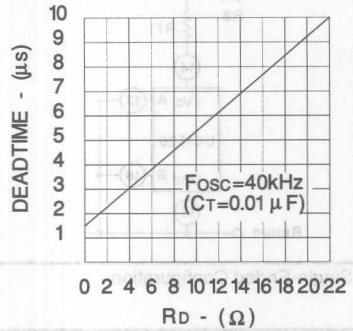
Figure 9. Driving N-channel Power Mosfets

TYPICAL CHARACTERISTICS

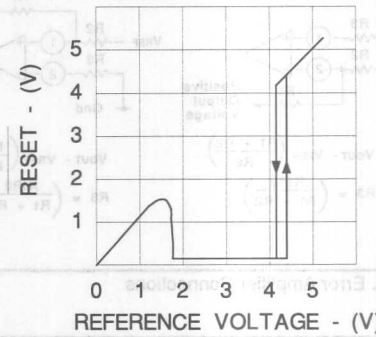


TYPICAL CHARACTERISTICS

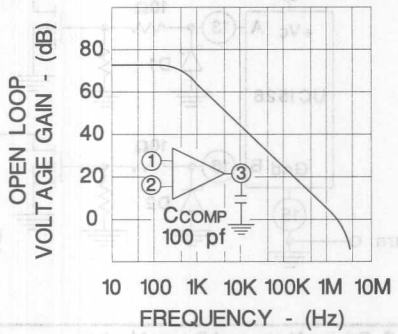
Output Driver Deadtime vs RD Value



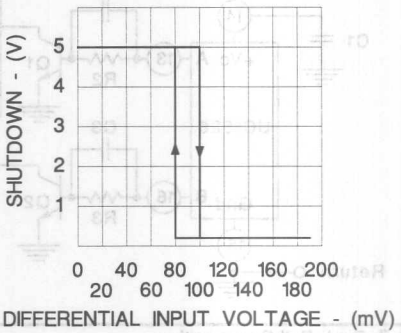
Under Voltage Lockout Characteristic



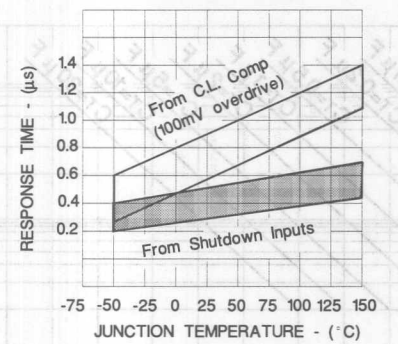
Error Amplifier Open Loop Gain vs Frequency



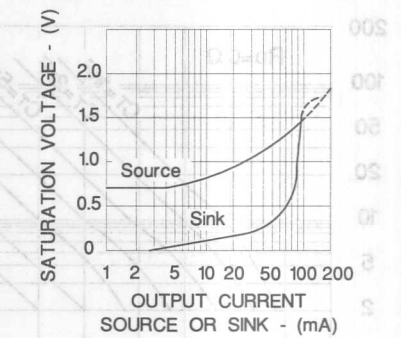
Current Limit Transfer Function



Shutdown Delay



Output Driver Saturation Voltage



UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

Regulating Pulse Width Modulator

FEATURES

- Reduced Supply Current
- Oscillator Frequency to 600kHz
- Precision Band-Gap Reference
- 7 to 35V Operation
- Dual 200mA Source/Sink Outputs
- Minimum Output Cross-Conduction
- Double-Pulse Suppression Logic
- Under-Voltage Lockout
- Programmable Soft-Start
- Thermal Shutdown
- TTL/CMOS Compatible Logic Ports
- 5 Volt Operation (V_{IN} = V_C = V_{REF} = 5.0V)

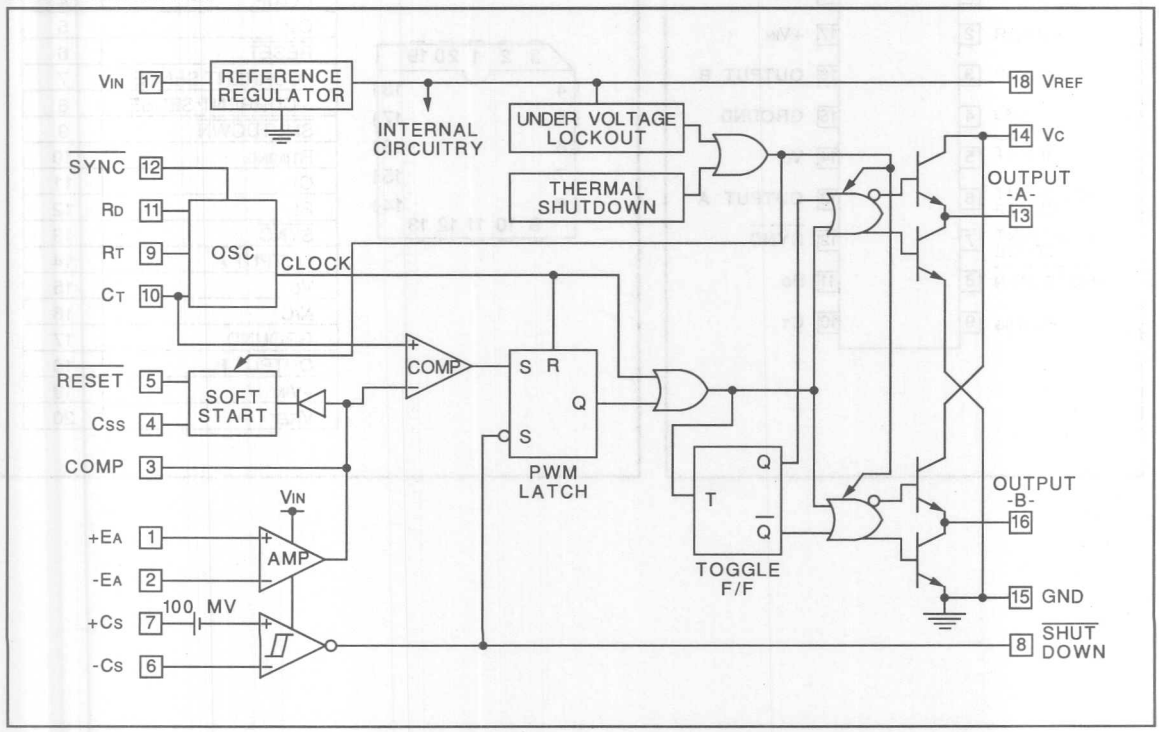
DESCRIPTION

The UC1526A Series are improved-performance pulse-width modulator circuits intended for direct replacement of equivalent non- "A" versions in all applications. Higher frequency operation has been enhanced by several significant improvements including: a more accurate oscillator with less minimum dead time, reduced circuit delays (particularly in current limiting), and an improved output stage with negligible cross-conduction current. Additional improvements include the incorporation of a precision, band-gap reference generator, reduced overall supply current, and the addition of thermal shutdown protection.

Along with these improvements, the UC1526A Series retains the protective features of under-voltage lockout, soft-start, digital current limiting, double pulse suppression logic, and adjustable deadtime. For ease of interfacing, all digital control ports are TTL compatible with active low logic.

Five volt (5V) operation is possible for "logic level" applications by connecting V_{IN}, V_C and V_{REF} to a precision 5V input supply. Consult factory for additional information.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Note 1, 2)

Input Voltage ($+V_{IN}$) ..... +40V
Collector Supply Voltage ($+V_C$) ..... +40V
Logic Inputs ..... -0.3V to +5.5V
Analog Inputs ..... -0.3V to $+V_{IN}$
Source/Sink Load Current (each output) 200mA
Reference Load Current 50mA
Logic Sink Current 15mA
Power Dissipation at T_A = +25°C (Note 2) 1000mW
Power Dissipation at T_C = +25°C (Note 2) 3000mW
Operating Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10 seconds) ..... +300°C

Note 1: Values beyond which damage may occur.
Note 2: Consult packaging Section of Databook for thermal limitations and considerations of package.

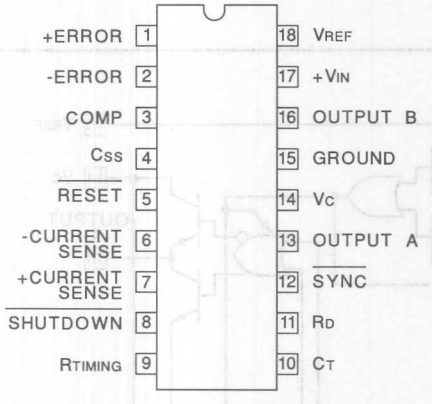
RECOMMENDED OPERATING CONDITIONS

(Note 3)
Input Voltage ..... +7V to +35V
Collector Supply Voltage ..... +4.5V to +35V
Sink/Source Load Current (each output) ..... 0 to 100mA
Reference Load Current ..... 0 to 20mA
Oscillator Frequency Range ..... 1Hz to 600kHz
Oscillator Timing Resistor ..... 2kΩ to 150kΩ
Oscillator Timing Capacitor ..... 400pF to 20μF
Available Deadtime Range at 40kHz ..... 1% to 50%
Operating Ambient Temperature Range
UC1526A ..... -55°C to +125°C
UC2526A ..... -25°C to +85°C
UC3526A ..... 0°C to +70°C

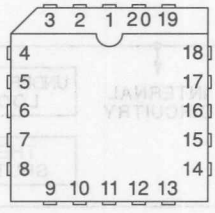
Note 3: Range over which the device is functional and parameter limits are guaranteed.

CONNECTION DIAGRAMS

DIL-18, SOIC-18 (TOP VIEW)
J or N Package, DW Package



PLCC-20, LCC-20
(TOP VIEW)
Q and L Packages



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
+ERROR	2
-ERROR	3
COMP.	4
Css	5
RESET	6
- CURRENT SENSE	7
+ CURRENT SENSE	8
SHUTDOWN	9
RTIMING	10
CT	11
RD	12
SYNC	13
OUTPUT A	14
VC	15
N/C	16
GROUND	17
OUTPUT B	18
+VIN	19
VREF	20

ELECTRICAL CHARACTERISTICS: +V_{IN} = 15V, and over operating ambient temperature, unless otherwise specified T_A = T_J.

PARAMETER	TEST CONDITIONS	UC1526A / UC2526A			UC3526A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Reference Section (Note 4)								
Output Voltage	T_J = +25°C	4.95	5.00	5.05	4.90	5.00	5.10	V
Line Regulation	+V_{IN} = 7 to 35V		2	10		2	15	mV
Load Regulation	I_L = 0 to 20mA		5	20		5	20	mV
Temperature Stability	Over Operating T_J (Note 5)		15	50		15	50	mV
Total Output Voltage Range	Over Recommended Operating Conditions	4.90	5.00	5.10	4.85	5.00	5.15	V
Short Circuit Current	V_{REF} = 0V	25	50	100	25	50	100	mA
Under-Voltage Lockout								
$\overline{\text{RESET}}$ Output Voltage	V_{REF} = 3.8V		0.2	0.4		0.2	0.4	V
	V_{REF} = 4.7V	2.4	4.7		2.4	4.8		V
Oscillator Section (Note 6)								
Initial Accuracy	T_J = +25°C		±3	±8		±3	±8	%
Voltage Stability	+V_{IN} = 7 to 35V		0.5	1		0.5	1	%
Temperature Stability	Over Operating T_J (Note 5)		2	6		1	3	%
Minimum Frequency	R_T = 150kΩ, C_T = 20µF (Note 5)			1			1	Hz
Maximum Frequency	R_T = 2kΩ, C_T = 470pF	550			650			kHz
Sawtooth Peak Voltage	+V_{IN} = 35V		3.0	3.5		3.0	3.5	V
Sawtooth Valley Voltage	+V_{IN} =7V	0.5	1.0		0.5	1.0		V
$\overline{\text{SYNC}}$ Pulse Width	T_J = 25°C, R_L = 2.7kΩ to V_{REF}		1.1			1.1		µs
Error Amplifier Section (Note 7)								
Input Offset Voltage	R_S ≤ 2kΩ		2	5		2	10	mV
Input Bias Current			-350	-1000		-350	-2000	nA
Input Offset Current			35	100		35	200	nA
DC Open Loop Gain	R_L ≥ 10MΩ	64	72		60	72		dB
HIGH Output Voltage	$V_{PIN\ 1}$ - $V_{PIN\ 2}$ ≥ 150mV, I_{SOURCE} = 100µA	3.6	4.2		3.6	4.2		V
LOW Output Voltage	$V_{PIN\ 2}$ - $V_{PIN\ 1}$ ≥ 150mV, I_{SINK} = 100µA		0.2	0.4		0.2	0.4	V
Common Mode Rejection	R_S ≤ 2kΩ	70	94		70	94		dB
Supply Voltage Rejection	+V_{IN} = 12 to 18V	66	80		66	80		dB
PWM Comparator (Note 6)								
Minimum Duty Cycle	$V_{COMPENSATION}$ = +0.4V			0			0	%
Maximum Duty Cycle	$V_{COMPENSATION}$ = +3.6V	45	49		45	49		%
Digital Ports ($\overline{\text{SYNC}}$, $\overline{\text{SHUTDOWN}}$, and $\overline{\text{RESET}}$)								
HIGH Output Voltage	I_{SOURCE} = 40µA	2.4	4.0		2.4	4.0		V
LOW Output Voltage	I_{SINK} = 3.6mA		0.2	0.4		0.2	0.4	V
HIGH Input Current	V_{IH} = +2.4V		-125	-200		-125	-200	µA
LOW Input Current	V_{IL} = +0.4V		-225	-360		-225	-360	µA
Shutdown Delay	From Pin 8, T_J = 25°C		160			160		ns
Current Limit Comparator (Note 8)								
Sense Voltage	R_S ≤ 50Ω	90	100	110	80	100	120	mV
Input Bias Current			-3	-10		-3	-10	µA
Shutdown Delay	From pin 7, 100mV Overdrive, T_J = 25°C		260			260		ns

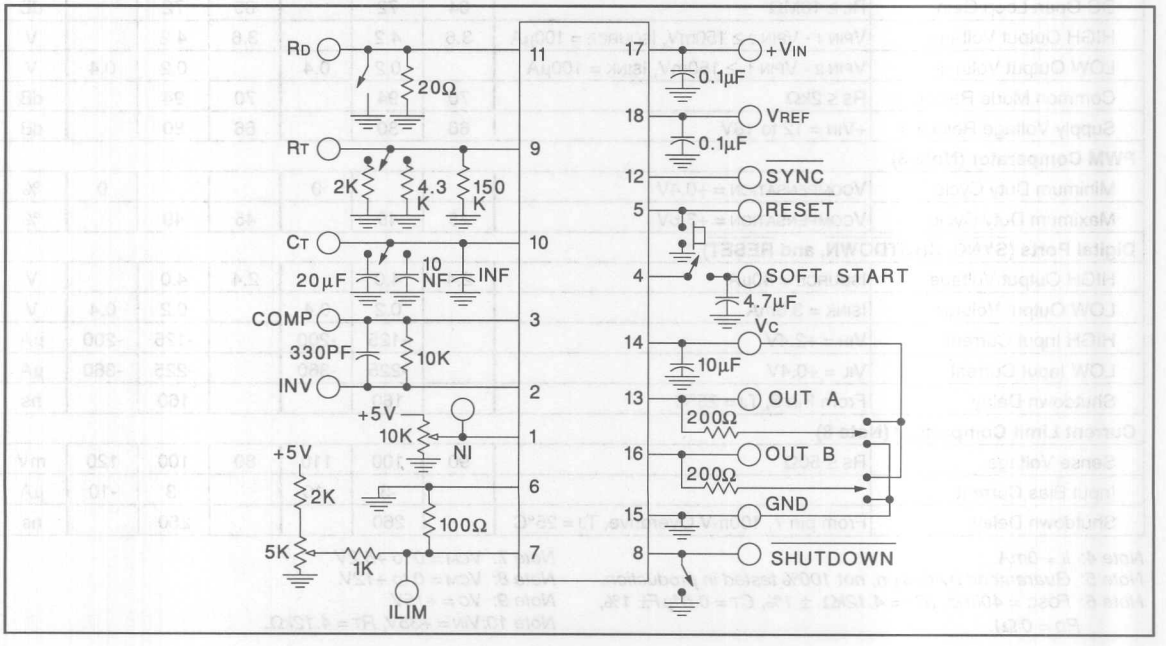
Note 4: I_L = 0mA.
Note 5: Guaranteed by design, not 100% tested in production.
Note 6: F_{OSC} = 40kHz, (R_T = 4.12kΩ ± 1%, C_T = 0.01µF± 1%, R_D = 0 Ω).
Note 7: V_{CM} = 0 to +5.2V
Note 8: V_{CM} = 0 to +12V.
Note 9: V_C = +15V.
Note 10: V_{IN} = +35V, R_T = 4.12kΩ.

ELECTRICAL CHARACTERISTICS: +V_{IN} = 15V, and over operating ambient temperature, unless otherwise specified $T_A = T_J$.

PARAMETER	TEST CONDITIONS	UC1526A UC2526A			UC3526A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Soft-Start Section								
Error Clamp Voltage	$\overline{RESET}$ = +0.4V		0.1	0.4		0.1	0.4	V
Cs Charging Current	$\overline{RESET}$ = +2.4V	50	100	150	50	100	150	µA
Output Drivers (Each Output) (Note 9)								
HIGH Output Voltage	I_{SOURCE} = 20mA	12.5	13.5		12.5	13.5		V
	I_{SOURCE} = 100mA	12	13		12	13		V
LOW Output Voltage	I_{SINK} = 20mA		0.2	0.3		0.2	0.3	V
	I_{SINK} = 100mA		1.2	2.0		1.2	2.0	V
Collector Leakage	V_C = 40V		50	150		50	150	µA
Rise Time	C_L = 1000pF (Note 5)		0.3	0.6		0.3	0.6	µs
Fall Time	C_L = 1000pF (Note 5)		0.1	0.2		0.1	0.2	µs
Cross-Conduction Charge	Per cycle, T_J = 25°C		8			8		nC
Power Consumption (Note 10)								
Standby Current	$\overline{SHUTDOWN}$ = +0.4V		14	20		14	20	mA

Note 4: I_L = 0mA.
Note 5: Guaranteed by design, not 100% tested in production.
Note 6: F_{OSC} = 40kHz, (R_T = 4.12kΩ ± 1%, C_T = 0.01µF± 1%, R_D = 0 Ω).
Note 7: V_{CM} = 0 to +5.2V
Note 8: V_{CM} = 0 to +12V.
Note 9: V_C = +15V.
Note 10: V_{IN} = +35V, R_T = 4.12kΩ.

Open Loop Test Circuit UC1526A



APPLICATIONS INFORMATION

Voltage Reference

The reference regulator of the UC1526A is based on a precision band-gap reference, internally trimmed to ±1% accuracy. The circuitry is fully active at supply voltages above +7V, and provides up to 20mA of load current to external circuitry at +5.0V. In systems where additional current is required, an external PNP transistor can be used to boost the available current. A rugged low frequency audio-type transistor should be used, and lead lengths between the PWM and transistor should be as short as possible to minimize the risk of oscillations. Even so, some types of transistors may require collector-base capacitance for stability. Up to 1 amp of load current can be obtained with excellent regulation if the device selected maintains high current gain.

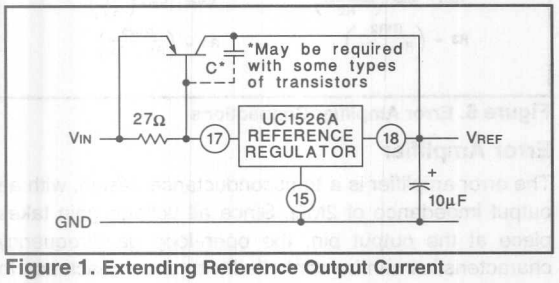


Figure 1. Extending Reference Output Current

Under-Voltage Lockout

The under-voltage lockout circuit protects the UC1526A and the power devices it controls from inadequate supply voltage, If +VIN is too low, the circuit disables the output drivers and holds the $\overline{\text{RESET}}$ pin LOW. This prevents spurious output pulses while the control circuitry is stabilizing, and holds the soft-start timing capacitor in a discharged state.

The circuit consists of a +1.2V bandgap reference and comparator circuit which is active when the reference voltage has risen to 3VBE or +1.8V at 25°C. When the reference voltage rises to approximately +4.4V, the circuit enables the output drivers and releases the $\overline{\text{RESET}}$ pin, allowing a normal soft-start. The comparator has 350mV of hysteresis to minimize oscillation at the trip point. When +VIN to the PWM is removed and the reference drops to +4.2V, the under-voltage circuit pulls $\overline{\text{RESET}}$ LOW again. The soft-start capacitor is immediately discharged, and the PWM is ready for another soft-start cycle.

The UC1526A can operate from a +5V supply by connecting the VREF pin to the +VIN pin and maintaining the supply between +4.8 and +5.2V.

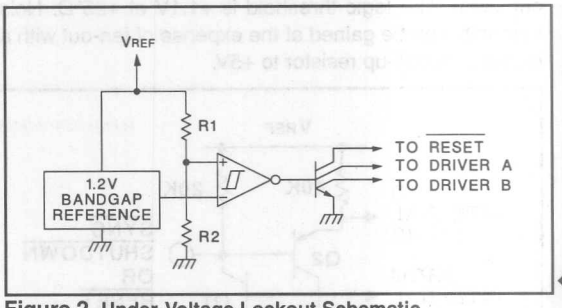


Figure 2. Under-Voltage Lockout Schematic

Soft-Start Circuit

The soft-start circuit protects the power transistors and rectifier diodes from high current surges during power supply turn-on. When supply voltage is first applied to the UC1526A, the under-voltage lockout circuit holds $\overline{\text{RESET}}$ LOW with Q3. Q1 is turned on, which holds the soft-start capacitor voltage at zero. The second collector of Q1 clamps the output of the error amplifier to ground, guaranteeing zero duty cycle at the driver outputs. When the supply voltage reaches normal operating range, $\overline{\text{RESET}}$ will go HIGH. Q1 turns off, allowing the internal 100µA current source to charge Cs. Q2 clamps the error amplifier output to 1VBE above the voltage on Cs. As the soft-start voltage ramps up to +5V, the duty cycle of the PWM linearly increases to whatever value the voltage regulation loop requires for an error null.

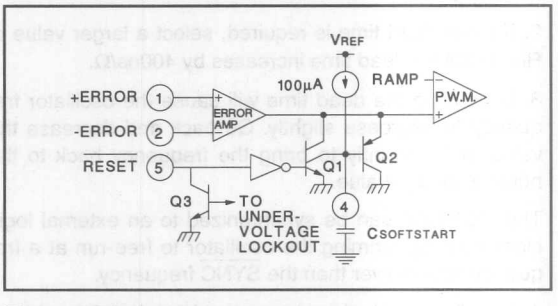


Figure 3. Soft-Start Circuit Schematic

Digital Control Ports

The three digital control ports of the UC1526A are bi-directional. Each pin can drive TTL and 5V CMOS logic directly, up to a fan-out of 10 low-power Schottky gates. Each pin can also be directly driven by open-collector TTL, open-drain CMOS, and open-collector voltage comparators; fan-in is equivalent to 1 low-power Schottky gate. Each port is normally HIGH; the pin is pulled LOW to activate the particular function. Driving $\overline{\text{SYNC}}$ LOW initiates a discharge cycle in the oscillator. Pulling $\overline{\text{SHUTDOWN}}$ LOW immediately inhibits all PWM output pulses. Holding $\overline{\text{RESET}}$ LOW discharges the soft-start

APPLICATIONS INFORMATION (cont.)

capacitor. The logic threshold is +1.1V at +25°C. Noise immunity can be gained at the expense of fan-out with an external 2k pull-up resistor to +5V.

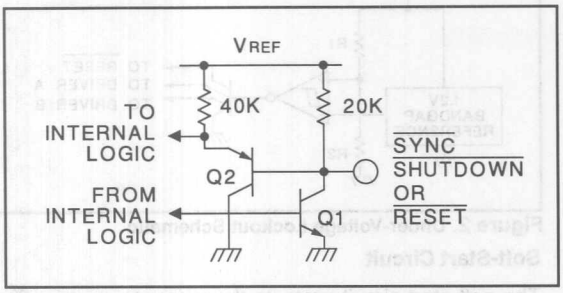


Figure 4. Digital Control Port Schematic

Oscillators

The oscillator is programmed for frequency and dead time with three components: RT, CT and RD. Two waveforms are generated: a sawtooth waveform at pin 10 for pulse width modulation, and a logic clock at pin 12. The following procedure is recommended for choosing timing values:

1. With RD= 0Ω (pin 11 shorted to ground) select values for RT and CT from the graph on page 4 to give the desired oscillator period. Remember that the frequency at each driver output is half the oscillator frequency, and the frequency at the +Vc terminal is the same as the oscillator frequency.

2. If more dead time is required, select a larger value of RD. At 40kHz dead time increases by 400ns/Ω.

3. Increasing the dead time will cause the oscillator frequency to decrease slightly. Go back and decrease the value of RT slightly to bring the frequency back to the nominal design value.

The UC1526A can be synchronized to an external logic clock by programming the oscillator to free-run at a frequency 10% slower than the $\overline{\text{SYNC}}$ frequency.

A periodic LOW logic pulse approximately 0.5µs wide at the $\overline{\text{SYNC}}$ pin will then lock the oscillator to the external frequency.

Multiple devices can be synchronized together by programming one master unit for the desired frequency, and then sharing its sawtooth and clock waveforms with the slave units. All CT terminals are connected to the CT pin of the master and all $\overline{\text{SYNC}}$ terminals are likewise connected to the $\overline{\text{SYNC}}$ pin of the master. Slave RT terminals are left open or connected to VREF. Slave RD terminal may be either left open or grounded.

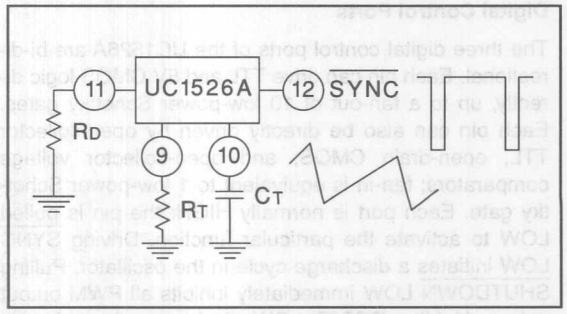


Figure 5. Oscillator Connections and Waveforms

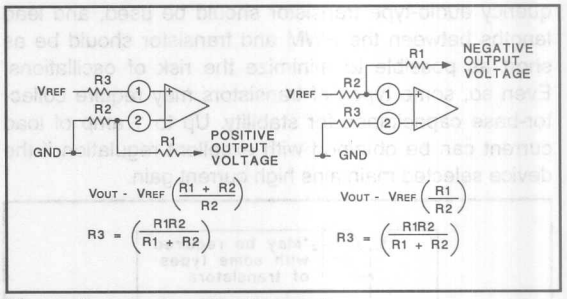


Figure 6. Error Amplifier Connections

Error Amplifier

The error amplifier is a transconductance design, with an output impedance of 2MΩ. Since all voltage gain takes place at the output pin, the open-loop gain/frequency characteristics can be controlled with shunt reactance to ground. When compensated for unity-gain stability with 100pF, the amplifier has an open-loop pole at 800Hz.

The input connections to the error amplifier are determined by the polarity of the switching supply output voltage. For positive supplies, the common-mode voltage is +5.0V and the feedback connections in Figure 6A are used. With negative supplies, the common-mode voltage is ground and the feedback divider is connected between the negative output and the +5.0V reference voltage, as shown in Figure 6B.

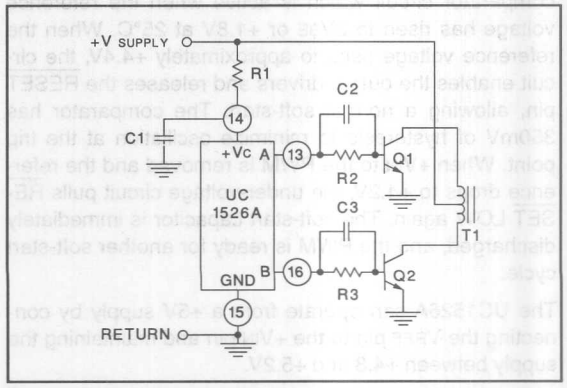


Figure 7. Push-Pull Configuration

APPLICATIONS INFORMATION (cont.)

Output Drivers

The totem pole output drivers of the UC1526A are designed to source and sink 100mA continuously and 200mA peak. Loads can be driven either from the output pins 13 and 16, or from the +Vc, as required.

Since the bottom transistor of the totem-pole is allowed to saturate, there is a momentary conduction path from the +Vc terminal to ground during switching; however, improved design has limited this cross-conduction period to less than 50ns. Capacitor decoupling at Vc is recommended and careful grounding of Pin 15 is needed to insure that high peak sink currents from a capacitive load do not cause ground transients.

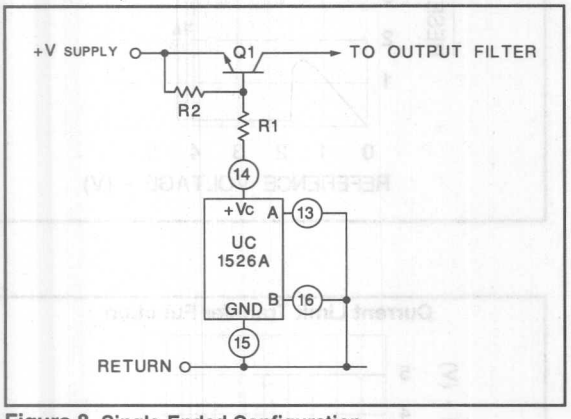


Figure 8. Single-Ended Configuration

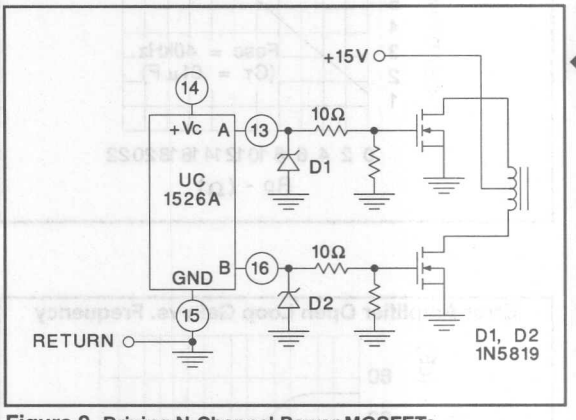
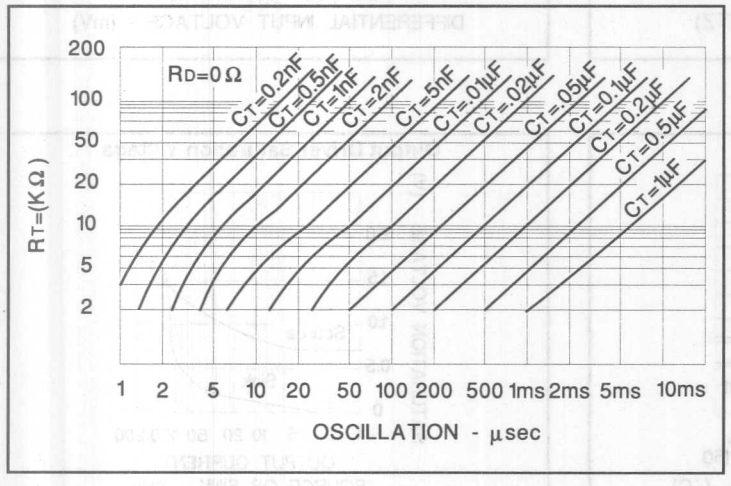


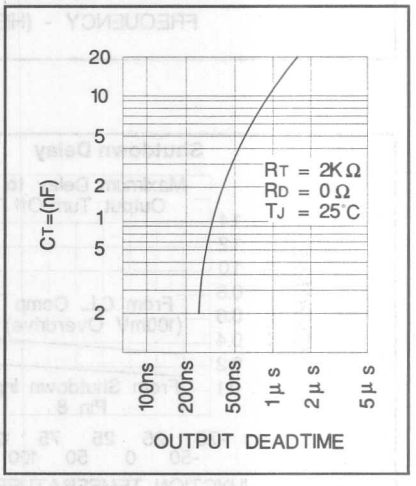
Figure 9. Driving N-Channel Power MOSFETs

TYPICAL CHARACTERISTICS

OSCILLATOR PERIOD vs RT and CT

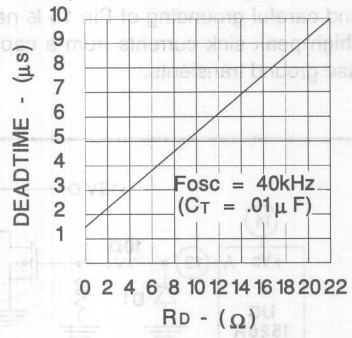


OUTPUT BLANKING

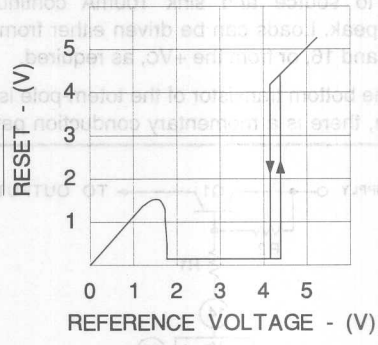


TYPICAL CHARACTERISTICS (Cont.)

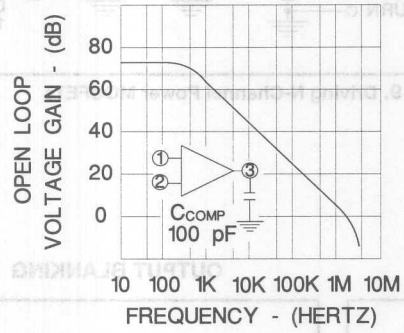
Output Driver Deadtime vs. RD Value



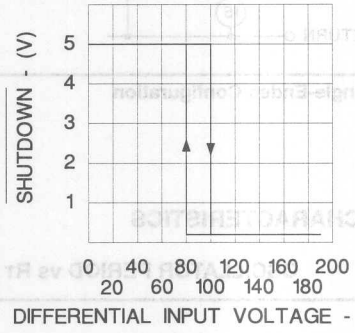
Under Voltage Lockout Characteristic



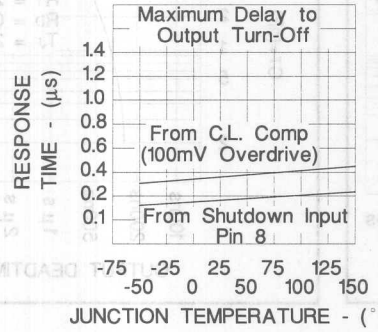
Error Amplifier Open Loop Gain vs. Frequency



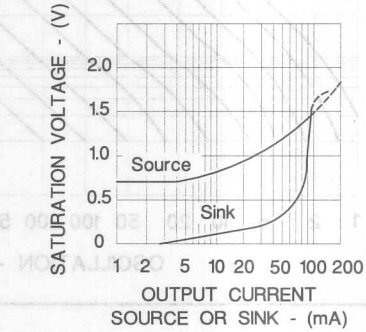
Current Limit Transfer Function



Shutdown Delay



Output Driver Saturation Voltage



UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

Power Supply Supervisory Circuit

FEATURES

- Includes Over-voltage, Under-voltage, And Current Sensing Circuits
- Internal 1% Accurate Reference
- Programmable Time Delays
- SCR "Crowbar" Drive Of 300mA
- Remote Activation Capability
- Optional Over-voltage Latch
- Uncommitted Comparator Inputs For Low Voltage Sensing (UC1544 Series Only)

DESCRIPTION

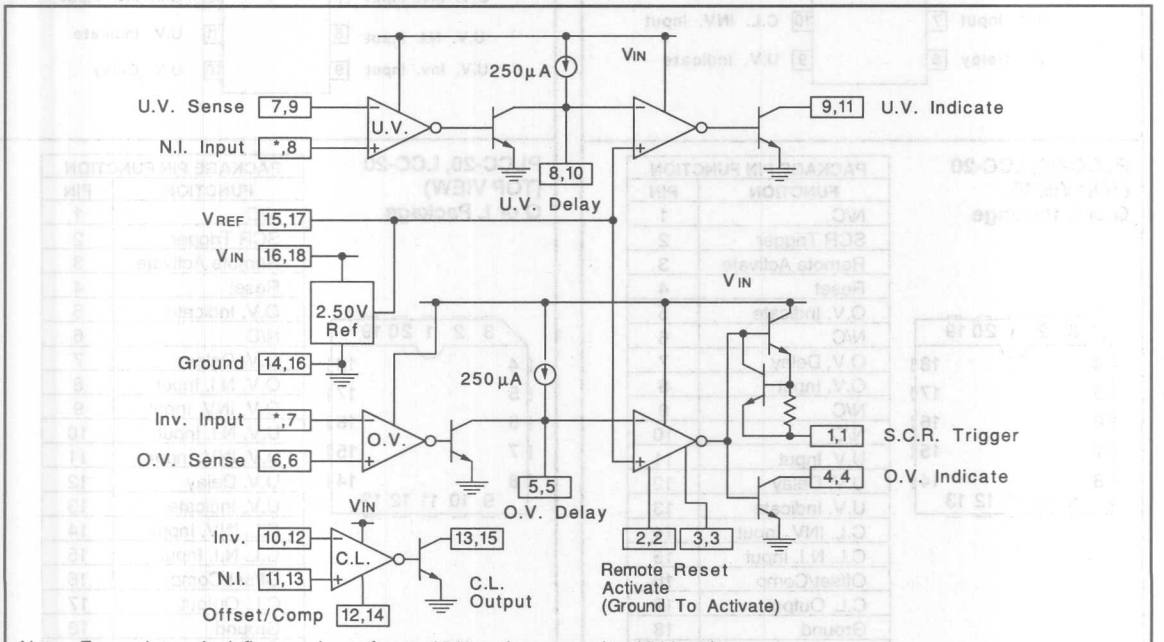
The monolithic integrated circuits contain all the functions necessary to monitor and control the output of a sophisticated power supply system. Over-voltage (O.V.) sensing with provision to trigger an external SCR "crowbar" shutdown; an under-voltage (U.V.) circuit which can be used to monitor either the output or to sample the input line voltage; and a third op amp/comparator usable for current sensing (C.L.) are all included in this IC, together with an independent, accurate reference generator.

Both over- and under-voltage sensing circuits can be externally programmed for minimum time duration of fault before triggering. All functions contain open collector outputs which can be used independently or wire-or'ed together, and although the SCR trigger is directly connected only to the over-voltage sensing circuit, it may be optionally activated by any of the other outputs, or from an external signal. The O.V. circuit also includes an optional latch and external reset capability.

The UC1544/2544/3544 devices have the added versatility of completely uncommitted inputs to the voltage sensing comparators so that levels less than 2.5V may be monitored by dividing down the internal reference voltage. The current sense circuit may be used with external compensation as a linear amplifier or as a high-gain comparator. Although nominally set for zero input offset, a fixed threshold may be added with an external resistor. Instead of current limiting, this circuit may also be used as an additional voltage monitor.

The reference generator circuit is internally trimmed to eliminate the need for external potentiometers and the entire circuit may be powered directly from either the output being monitored or from a separate bias voltage.

BLOCK DIAGRAM



Note: For each terminal, first number refers to 1543 series, second to 1544 series.
** On 1543 series, this function is internally connected to VREF.*

4/97

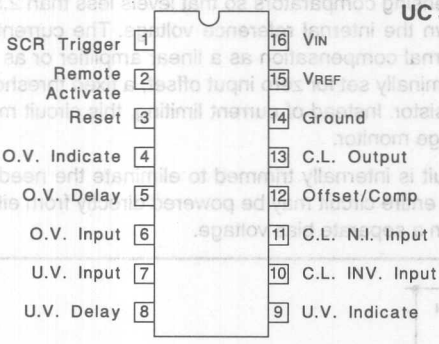
ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage, V_{IN} 40V
Sense Inputs, Voltage Range . . . . . 0 to V_{IN}
SCR Trigger Current (Note 1) . . . . . -600mA
Indicator Output Voltage 40V
Indicator Output Sink Current 50mA
Power Dissipation (Package Limitation) 1000mW
Operating Temperature Range
UC1543, UC1544 . . . . . -55°C to +125°C
UC2543, UC2544 . . . . . -25°C to +85°C
UC3543, UC3544 . . . . . 0°C to +70°C
Storage Temperature Range . . . . . -65°C to +150°C

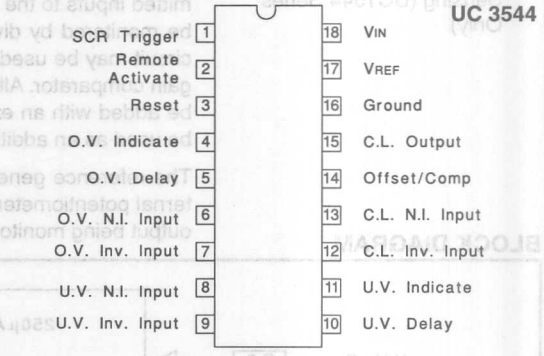
Note 1: At higher input voltages, a dissipation limiting resistor, RG, is required.
Note 2: Currents are positive-into, negative-out of the specified terminal. Consult Packaging section of Databook for thermal limitations and considerations of package.

CONNECTION DIAGRAMS

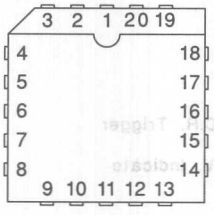
DIL-16, SOIC-16 (TOP VIEW)
J or N, DW Package
UC 1543
UC 2543
UC 3543



DIL-18, SOIC-18 (TOP VIEW)
J or N, DW Package
UC 1544
UC 2544
UC 3544

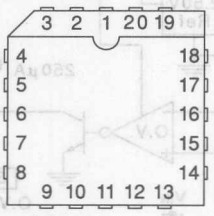


PLCC-20, LCC-20
(TOP VIEW)
Q or L Package



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
SCR Trigger	2
Remote Activate	3
Reset	4
O.V. Indicate	5
N/C	6
O.V. Delay	7
O.V. Input	8
N/C	9
N/C	10
U.V. Input	11
U.V. Delay	12
U.V. Indicate	13
C.L. INV. Input	14
C.L. N.I. Input	15
Offset/Comp	16
C.L. Output	17
Ground	18
V_{REF}	19
V_{IN}	20

PLCC-20, LCC-20
(TOP VIEW)
Q or L Package

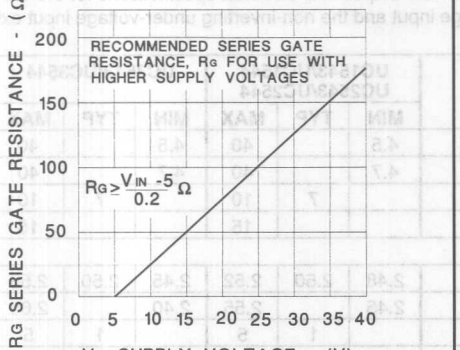


PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
SCR Trigger	2
Remote Activate	3
Reset	4
O.V. Indicate	5
N/C	6
O.V. Delay	7
O.V. N.I. Input	8
O.V. INV. Input	9
U.V. N.I. Input	10
U.V. INV. Input	11
U.V. Delay	12
U.V. Indicate	13
C.L. INV. Input	14
C.L. N.I. Input	15
Offset/Comp	16
C.L. Output	17
Ground	18
V_{REF}	19
V_{IN}	20

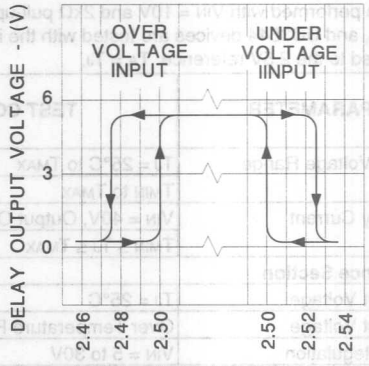
ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1543 and UC1544; -25°C to +85°C for the UC2543 and UC2544; and 0°C to +70°C for the UC3543 and UC3544. Electrical tests are performed with V_{IN} = 10V and 2kΩ pull-up resistors on all indicator outputs. All electrical specifications for the UC1544, UC2544, and UC3544 devices are tested with the inverting over-voltage input and the non-inverting under-voltage input externally connected to the 2.5V reference. $T_A = T_J$.

PARAMETER	TEST CONDITIONS	UC1543/UC1544 UC2543/UC2544			UC3543/UC3544			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Voltage Range	T_J = 25°C to T_{MAX}	4.5		40	4.5		40	V
	T_{MIN} to T_{MAX}	4.7		40	4.7		40	V
Supply Current	V_{IN} = 40V, Output Open, T_J = 25°C		7	10		7	10	mA
	$T_{MIN} \le T_J \le T_{MAX}$			15			15	mA
Reference Section								
Output Voltage	T_J = 25°C	2.48	2.50	2.52	2.45	2.50	2.55	V
Output Voltage	Over Temperature Range	2.45		2.55	2.40		2.60	V
Line Regulation	V_{IN} = 5 to 30V		1	5		1	5	mV
Load Regulation	I_{REF} = 0 to 10mA		1	10		1	10	mV
Short Circuit Current	V_{REF} = 0	-10	-20	-40	-12	-20	-40	mA
Temperature Stability			50			50		ppm/°C
SCR Trigger Section								
Peak Output Current	V_{IN} = 5V, R_G = 0, V_O = 0	-100	-300	-600	-100	-300	-600	mA
Peak Output Voltage	V_{IN} = 15V, I_O = -100mA	12	13		12	13		V
Output Off Voltage	V_{IN} = 40V		0	0.1		0	0.1	V
Remote Activate Current	R/A Pin = Gnd		-0.4	-0.8		-0.4	-0.8	mA
Remote Activate Voltage	R/A Pin Open		2	6		2	6	V
Reset Current	Reset = Gnd, R/A = Gnd		-0.4	-0.8		-0.4	-0.8	mA
Reset Voltage	Reset open, R/A = Gnd		2	6		2	6	V
Output Current Rise Time	R_L = 50Ω, T_J = 25°C, C_D = 0		400			400		mA/µs
Prop. Delay from R/A	R_L = 50Ω, T_J = 25°C, C_D = 0		300			300		ns
Prop. Delay from O/V input	R_L = 50Ω, T_J = 25°C, C_D = 0		500			500		ns
Comparator Section								
Input Threshold (Input voltage rising on O.V. and falling on U.V.)	T_J = 25°C	2.45	2.50	2.55	2.40	2.50	2.60	V
	Over Temperature Range	2.40		2.60	2.35		2.65	V
Input Hysteresis			25			25		mV
Input Bias Current	Sense Input = 0V		-0.3	-1.0		-0.3	-1.0	µA
Delay Saturation			0.2	0.5		0.2	0.5	V
Delay High Level			6	7		6	7	V
Delay Charging Current	V_O = 0	-200	-250	-300	-200	-250	-300	µA
Indicate Saturation	I_L = 10mA		0.2	0.5		0.2	0.5	V
Indicate Leakage	V_{IND} = 40V		.01	1.0		.01	1.0	µA
Propagation Delay	Input Over Drive = 200mV, T_J = 25°C, C_D = 0		400			400		ns
	Input Over Drive = 200mV, T_J = 25°C, C_D = 1µF		10			10		ms
Current Limit Section								
Input Voltage Range		0		V_{IN}-3V	0		V_{IN}-3V	V
Input Bias Current	Offset Pin Open, V_{CM} = 0		-0.3	-1.0		-0.3	-1.0	µA
Input Offset Voltage	Offset Pin Open, V_{CM} = 0		0	10		0	10	mV
	10kΩ from Offset Pin to Gnd	80	100	120	80	100	120	mV
CMRR	0 ≤ V_{CM} ≤ 12V, V_{IN} = 15V	60	70		60	70		dB
AVOL	Offset Pin Open, V_{CM} = 0V, R_L = 10k to 15kΩ, ΔV_{OUT} = 1 to 6V	72	80		72	80		dB
Output Saturation	I_L = 10mA		0.2	0.5		0.2	0.5	V
Output Leakage	V_{IND} = 40V		.01	1.0		.01	1.0	µA
Small Signal Bandwidth	A_V = 0dB, T_J = 25°C		5			5		MHz
Propagation Delay	$V_{OVERDRIVE}$ = 100mV, T_J = 25°C		200			200		ns

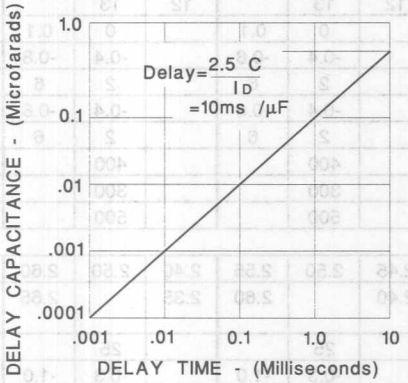
SCR Trigger Power Limiting



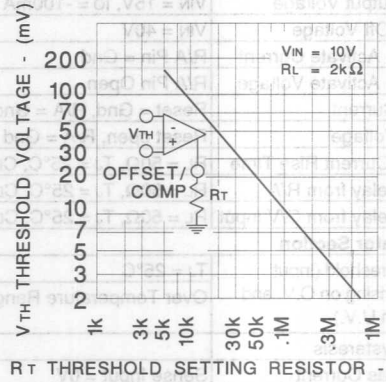
Comparator Input Hysteresis



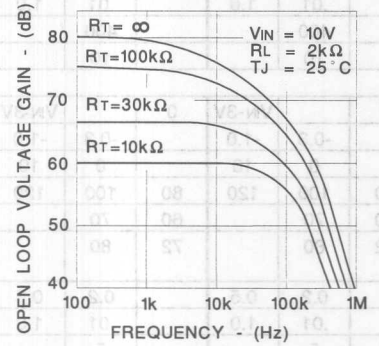
Activation Delay vs Capacitor Value



Current Limit Input Threshold

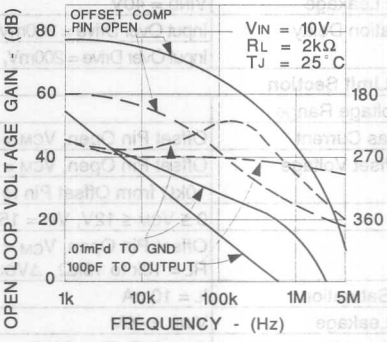


Current Limit Amplifier Gain



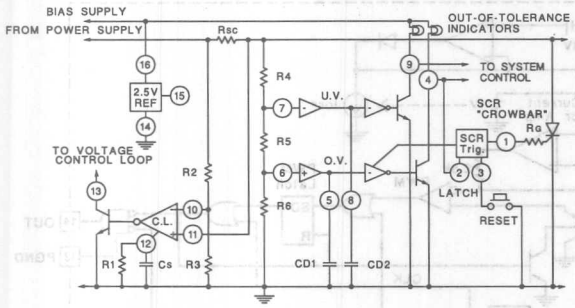
Note: RT is connected from Offset Pin to Gnd. Values of RT below 5.0k may cause Amplifier Cutoff at -55°C.

Current Limit Amplifier Frequency Response



APPLICATIONS (Pin numbers given for UC1543 series devices)

Typical Application



The values for the external components are determined as follows:

Current limit input threshold, $V_{TH} = \frac{1000}{R_1}$

CS is determined by the current loop dynamics

Peak current to load, $I_P \cong \frac{V_{TH}}{R_{SC}} + \frac{V_O}{R_{SC}}\left(\frac{R_2}{R_2 + R_3}\right)$

Short Circuit Current, $I_{SC} = \frac{V_{TH}}{R_{SC}}$

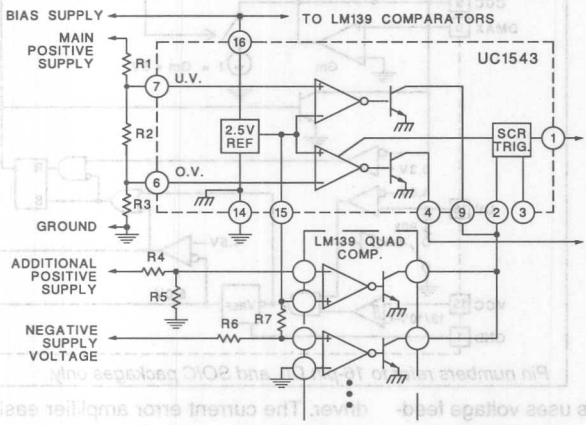
Low output voltage limit, $V_O\ (Low) = \frac{2.5\,(R_4 + R_5 + R_6)}{R_5 + R_6}$

High output voltage limit, $V_O\ (High) = \frac{2.5\,(R_4 + R_5 + R_6)}{R_6}$

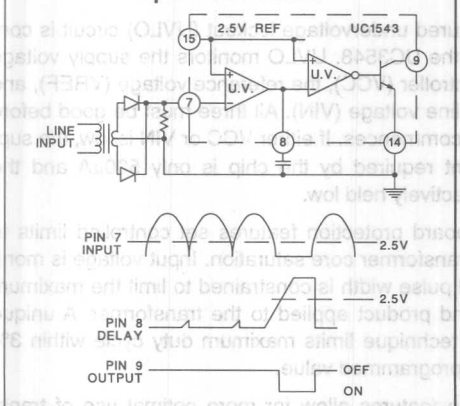
Voltage sensing delay, $t_D = 10{,}000C_D$

SCR trigger power limiting resistor, $R_G > \frac{V_{IN} - 5}{0.2}$

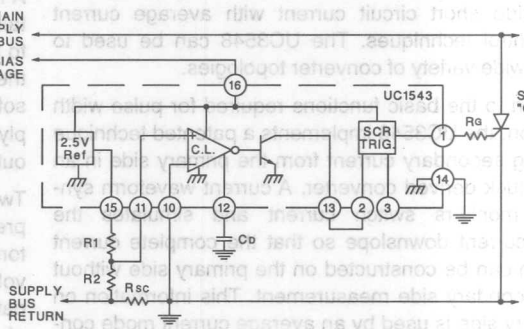
Sensing Multiple Supply Voltages



Input Line Monitor



Overcurrent Shutdown



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7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
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UNITRODE

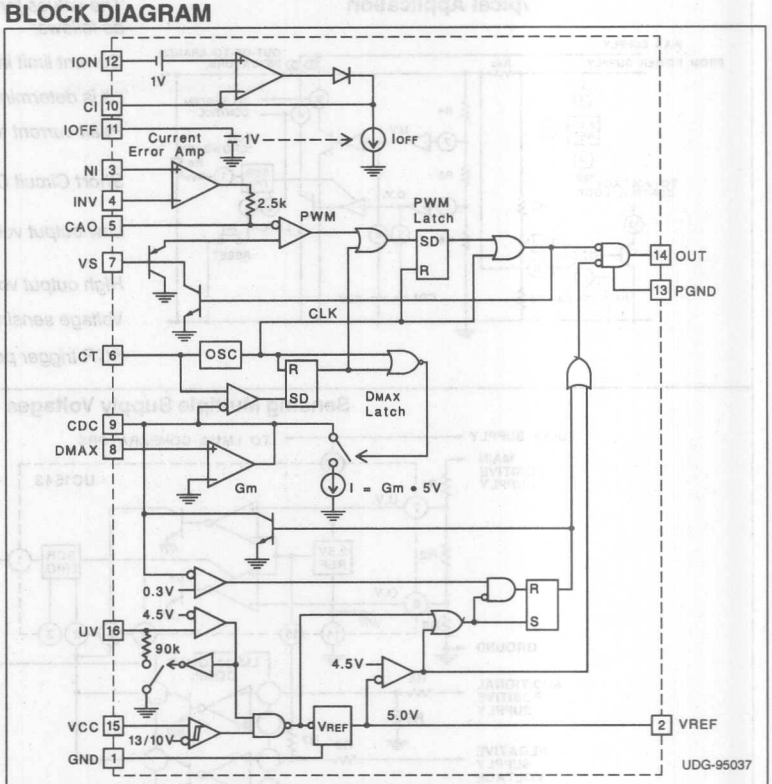
UC1548
UC2548
UC3548

Primary Side PWM Controller

FEATURES

- Primary Side Voltage Feed-forward Control of Isolated Power Supplies
- Accurate DC Control of Secondary Side Short Circuit Current using Primary Side Average Current Mode Control
- Accurate Programmable Maximum Duty Cycle Clamp
- Maximum Volt-Second Product Clamp to Prevent Core Saturation
- Practical Operation Up to 1MHz
- High Current (2A Pk) Totem Pole Output Driver
- Wide Bandwidth (8MHz) Current Error Amplifier
- Undervoltage Lockout Monitors VCC, VIN and VREF
- Output Active Low During UVLO
- Low Startup Current (500µA)

BLOCK DIAGRAM



Pin numbers refer to 16-pin DIL and SOIC packages only.

DESCRIPTION

The UC3548 family of PWM control ICs uses voltage feed-forward control to regulate the output voltage of isolated power supplies. The UC3548 resides on the primary side and has the necessary features to accurately control secondary side short circuit current with average current mode control techniques. The UC3548 can be used to control a wide variety of converter topologies.

In addition to the basic functions required for pulse width modulation, the UC3548 implements a patented technique of sensing secondary current from the primary side in an isolated buck derived converter. A current waveform synthesizer monitors switch current and simulates the inductor current downslope so that the complete current waveform can be constructed on the primary side without actual secondary side measurement. This information on the primary side is used by an average current mode control circuit to accurately limit maximum output current.

The UC3548 circuitry includes a precision reference, a wide bandwidth error amplifier for average current control, an oscillator to generate the system clock, latching PWM comparator and logic circuits, and a high current output driver. The current error amplifier easily interfaces with an optoisolator from a secondary side voltage sensing circuit.

A full featured undervoltage lockout (UVLO) circuit is contained in the UC3548. UVLO monitors the supply voltage to the controller (VCC), the reference voltage (VREF), and the input line voltage (VIN). All three must be good before soft start commences. If either VCC or VIN is low, the supply current required by the chip is only 500µA and the output is actively held low.

Two on board protection features set controlled limits to prevent transformer core saturation. Input voltage is monitored and pulse width is constrained to limit the maximum volt-second product applied to the transformer. A unique patented technique limits maximum duty cycle within 3% of a user programmed value.

These two features allow for more optimal use of transformers and switches, resulting in reduced system size and cost.

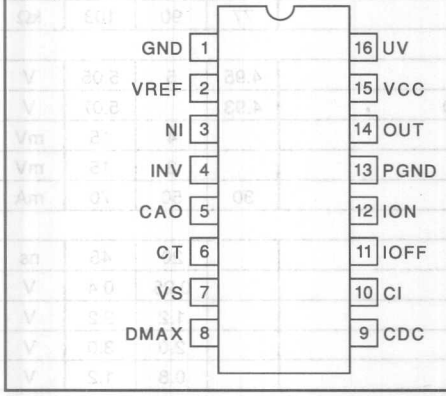
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Pin 15) 22V
Output Current, Source or Sink (Pin 14)
DC 0.5A
Pulse (0.5µs) 2.2A
Power Ground to Ground (Pin 1 to Pin 13) . . . . . ±0.2V
Analog Input Voltages
(Pins 3, 4, 7, 8, 12, 16) . . . . . -0.3 to 7V
Analog Input Currents, Source or Sink
(Pins 3, 4, 7, 8, 11, 12, 16) 1mA
Analog Output Currents, Source or Sink (Pins 5 & 10) . . . 5mA
Power Dissipation at T_A = 60°C 1W
Storage Temperature Range. . . . . –65°C to +150°C
Lead Temperature (Soldering 10 seconds) . . . . . +300°C

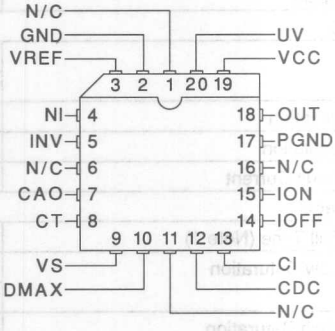
Notes: All voltages are with respect to ground (DIL and SOIC pin 1). Currents are positive into the specified terminal. Pin numbers refer to the 16 pin DIL and SOIC packages. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAMS

DIL-16, SOIC-16 (Top View)
J, N, or DW Packages



PLCC-20 & LCC-20 (Top View)
Q & L Packages



ELECTRICAL CHARACTERISTICS

Unless otherwise stated, all specifications are over the junction temperature range of –55°C to +125°C for the UC1548, –40°C to +85°C for the UC2548, and 0°C to +70°C for the UC3548. Test conditions are: VCC = 12V, CT = 400pF, CI = 100pF, IOFF = 100µA, CDC = 100nF, Cvs = 100pF, and Ivs = 400µA, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Real Time Current Waveform Synthesizer					
Ion Amplifier					
Offset Voltage		0.95	1	1.05	V
Slew Rate (Note 1)		20	25		V/µs
Iib			-2	-20	µA
IOFF Current Mirror					
Input Voltage		0.95	1	1.05	V
Current Gain		0.9	1	1.1	A/A
Current Error Amplifier					
AVOL		60	100		dB
Vio	12V ≤ VCC ≤ 20V, 0V ≤ VCM ≤ 5V			10	mV
Iib			-0.5	-3	µA
Voh	Io = –200µA	3.1	3.3	3.5	V
Vol	Io = 200µA		0.3	0.6	V
Source Current	Vo = 1V	1.4	1.6	2.0	mA
GBW Product	f = 200kHz	5	8		MHz
Slew Rate (Note 1)		8	10		V/µs
Oscillator					
Frequency	T_A = 25°C	240	250	260	kHz
		235		265	kHz

ELECTRICAL CHARACTERISTICS (cont.): Unless otherwise stated, all specifications are over the junction temperature range of –55°C to +125°C for the UC1548, –40°C to +85°C for the UC2548, and 0°C to +70°C for the UC3548. Test conditions are: VCC = 12V, CT = 400pF, CI = 100pF, IOFF = 100µA, CDC = 100nF, Cvs = 100pF, and Ivs = 400µA, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Duty Cycle Clamp					
Max Duty Cycle	V(DMAX) = 0.75 • VREF	73.5	76.5	79.5	%
VCC Comparator					
Turn-on Threshold			13	14	V
Turn-off Threshold		9	10		V
Hysteresis		2.5	3	3.5	V
UV Comparator					
Turn-on Threshold		4.1	4.35	4.6	V
RHYSTERESIS	Vuv = 4.2V	77	90	103	kΩ
Reference					
VREF	T_A = 25°C	4.95	5	5.05	V
	0 < Io < 10mA, 12 < VCC < 20	4.93		5.07	V
Line Regulation	12V < VCC < 20V		4	15	mV
Load Regulation	0 < Io < 10mA		3	15	mV
Short Circuit Current	VREF = 0V	30	50	70	mA
Output Stage					
Rise & Fall Time (Note 1)	CI = 1nF		20	45	ns
Output Low Saturation	Io = 20mA		0.25	0.4	V
	Io = 200mA		1.2	2.2	V
Output High Saturation	Io = -200mA		2.0	3.0	V
UVLO Output Low Saturation	Io = 20mA		0.8	1.2	V
Icc					
ISTART	VCC = 12V		0.2	0.4	mA
ICC (pre-start)	VCC = 15V, V(UV) = 0		0.5	1	mA

Note 1: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

CAO: Output of the current error amplifier. Also the resistor load for the collector of an optocoupler.

CDC: Connect a charge balance integration capacitor from CDC to GND to achieve an accurate duty cycle clamp. This capacitor also sets the soft start time.

CI: Output of the inductor current waveform synthesizer. Requires a capacitor to ground.

CT: A capacitor from CT to GND sets the oscillator frequency.

DMAX: Programs maximum duty cycle with a resistive divider from VREF to DMAX to GND.

GND: Signal ground.

INV: Inverting input of the current error amplifier.

IOFF: Programs the discharge slope of the capacitor on CI to emulate the down slope of the inductor current waveform.

ION: Input pin to inductor current waveform synthesizer. Apply a voltage proportional to switch current to this pin.

NI: Noninverting input of the current error amplifier.

OUT: Output driver for the gate of a power FET.

PGND: Power ground pin for the output driver. This ground circuit should be connected to GND at a single point.

UV: Line voltage sense pin to insure the chip only operates with sufficient line voltage. Program with a resistive divider from the converter input voltage to UV to GND.

VCC: Chip supply voltage. Bypass with a 1µF ceramic capacitor to PGND.

VREF: Precision voltage reference. Bypass with a 1µF ceramic capacitor to GND.

VS: Volt second clamp programming pin and feedforward ramp waveform for the pulse width

UNDERVOLTAGE LOCKOUT

The undervoltage lockout block diagram is shown in Figure 1. The VCC comparator monitors chip supply voltage. Hysteretic thresholds are set at 13V and 10V to facilitate off-line applications. If the VCC comparator is low, ICC is low (<500µA) and the output is low.

The UV comparator monitors input line voltage (VIN). A pair of resistors divides the input line to UV. Hysteretic input line thresholds are programmed by Rv1 and Rv2. The thresholds are

$V_{IN(on)} = 4.35V \bullet (1 + Rv1/Rv2')$ and

$V_{IN(off)} = 4.35V \bullet (1 + Rv1/Rv2)$ where

$Rv2' = Rv2 \| 90k$.

The resulting hysteresis is

$V_{IN(hys)} = 4.35V \bullet Rv1 / 90k$.

When the UV comparator is low, Icc is low (<500µA) and the output is low.

When both the UV and VCC comparators are high, the internal bias circuitry for the remainder of the chip is activated. The CDC pin (see discussion on Maximum Duty Cycle Control and Soft Start) and the Output are held low until VREF exceeds the 4.5V threshold of the VREF comparator. When VREF is good, control of the output driver is transferred to the PWM circuitry and CDC is allowed to charge.

If any of the three UVLO comparators go low, the UVLO latch is set, the output is held low, and CDC is discharged. This state will be maintained until all three comparators are high and the CDC pin is fully discharged.

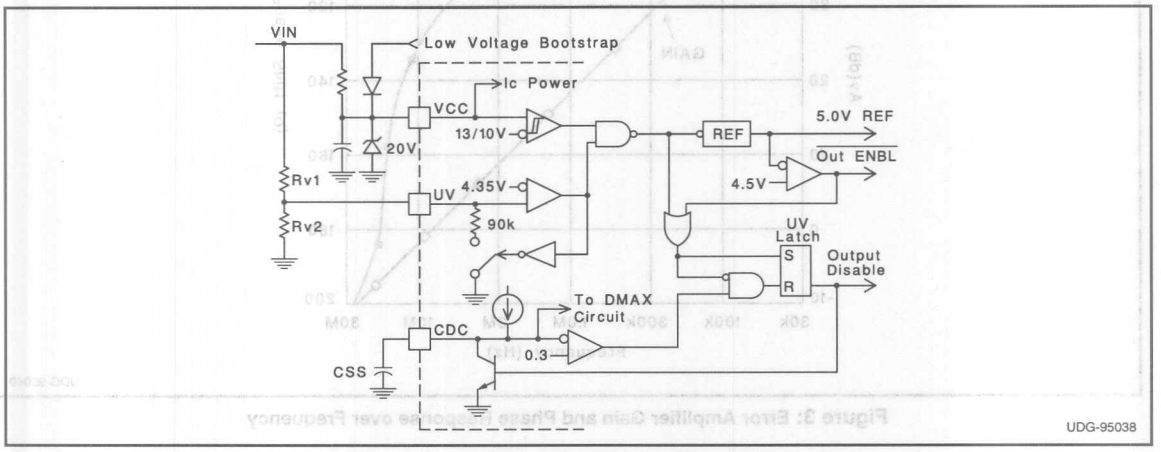


Figure 1: Undervoltage Lockout

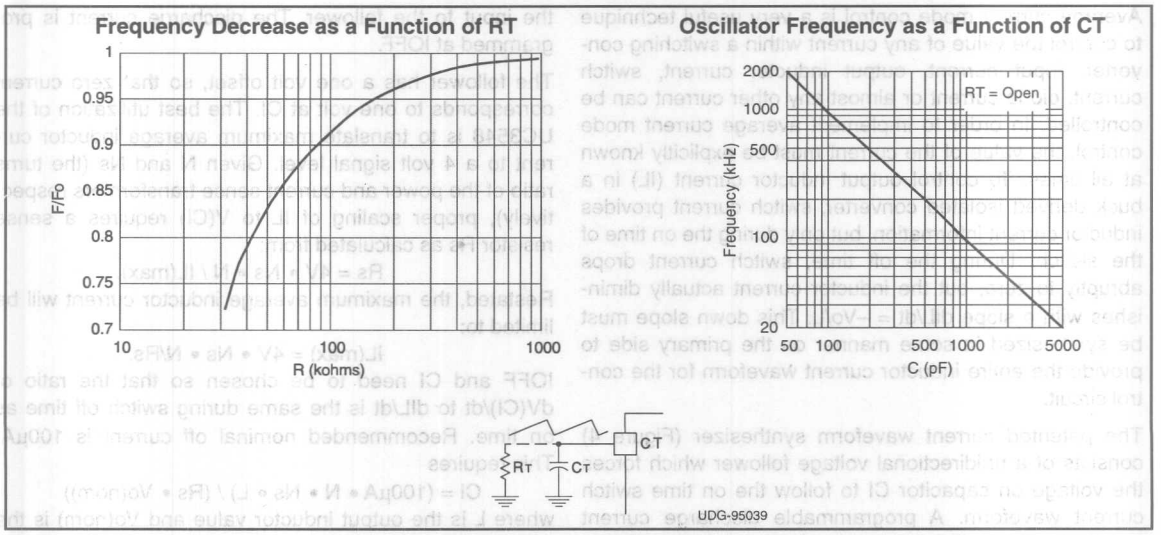


Figure 2: Oscillator Frequency

OSCILLATOR

A capacitor from the CT pin to GND programs oscillator frequency, as shown in Figure 2. Frequency is determined by:

$$F = 1 / (10k \bullet CT).$$

The sawtooth wave shape is generated by a charging current of 200µA and a discharge current of 1800µA. The discharge time of the sawtooth is guaranteed dead time for the output driver. If the maximum duty cycle control is defeated by connecting DMAX to VREF, the maximum duty cycle is limited by the oscillator to 90%. If an adjustment is required, an additional trim resistor RT from CT to ground can be used to adjust the oscillator frequency. RT should not be less than 40kohms. This will allow up to a 22% decrease in frequency.

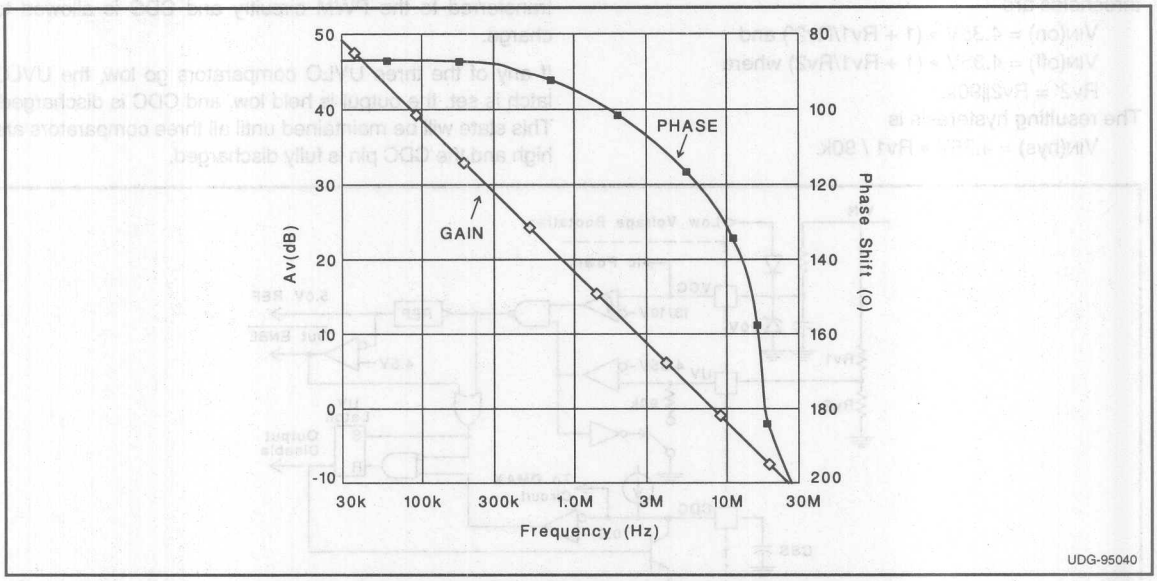


Figure 3: Error Amplifier Gain and Phase Response over Frequency

INDUCTOR CURRENT WAVEFORM SYNTHESIZER

Average current mode control is a very useful technique to control the value of any current within a switching converter. Input current, output inductor current, switch current, diode current or almost any other current can be controlled. In order to implement average current mode control, the value of the current must be explicitly known at all times. To control output inductor current (IL) in a buck derived isolated converter, switch current provides inductor current information, but only during the on time of the switch. During the off time, switch current drops abruptly to zero, but the inductor current actually diminishes with a slope dIL/dt = –Vo/L. This down slope must be synthesized in some manner on the primary side to provide the entire inductor current waveform for the control circuit.

The patented current waveform synthesizer (Figure 4) consists of a unidirectional voltage follower which forces the voltage on capacitor CI to follow the on time switch current waveform. A programmable discharge current synthesizes the off time portion of the waveform. ION is the input to the follower. The discharge current is programmed at IOFF.

The follower has a one volt offset, so that zero current corresponds to one volt at CI. The best utilization of the UC3548 is to translate maximum average inductor current to a 4 volt signal level. Given N and Ns (the turns ratio of the power and current sense transformers respectively), proper scaling of IL to V(CI) requires a sense resistor Rs as calculated from:

$$Rs = 4V \bullet Ns \bullet N / IL(max).$$

Restated, the maximum average inductor current will be limited to:

$$IL(max) = 4V \bullet Ns \bullet N/Rs.$$

IOFF and CI need to be chosen so that the ratio of dV(CI)/dt to dIL/dt is the same during switch off time as on time. Recommended nominal off current is 100µA. This requires

$$CI = (100\mu A \bullet N \bullet Ns \bullet L) / (Rs \bullet Vo(nom))$$

where L is the output inductor value and Vo(nom) is the converter regulated output voltage.

INDUCTOR CURRENT WAVEFORM SYNTHESIZER (cont.)

There are several methods to program IOFF. If accurate maximum current control is required, IOFF must track output voltage. The method shown in Figure 4 derives a voltage proportional to VIN • D (where D = duty cycle). In a buck converter, output voltage is proportional to VIN • D. A resistively loaded diode connection to the bootstrap winding yields a square wave whose amplitude is proportional to VIN and is duty cycle modulated by the control circuit. Averaging this waveform with a filter generates a primary side replica of secondary regulated Vo. A single pole filter is shown, but in practice a two or three pole filter provides better transient response. Filtered voltage is converted by ROFF to a current to the IOFF pin to control CI downslope.

If accurate system maximum current is not a critical requirement, Figure 5 shows the simplest method of downslope generation: a single resistor (ROFF = 40k) from IOFF to VREF. The discharge current is then 100µA. The disadvantage to this approach is that the synthesizer continues to generate a down slope when the switch is off even during short circuit conditions. Actual inductor downslope is closer to zero during a short circuit. The penalty is that the average current is understated by an amount approximately equal to the nominal inductor ripple current. Output short circuit is therefore higher than the designed maximum output current.

A third method of generating IOFF is to add a second winding to the output inductor core (Figure 6). When the power switch is off and inductor current flows in the free wheeling diode, the voltage across the inductor is equal to the output voltage plus the diode drop. This voltage is then transformed by the second winding to the primary side of the converter. The advantages to this approach are its inherent accuracy and bandwidth. Winding the second coil on the output inductor core while maintaining the required isolation makes this a more costly solution. In the example, ROFF = Vo / 100µA. The 4 • ROFF resistor is added to compensate the one volt input level of the IOFF pin. Without this compensation, a minor current foldback behavior will be observed.

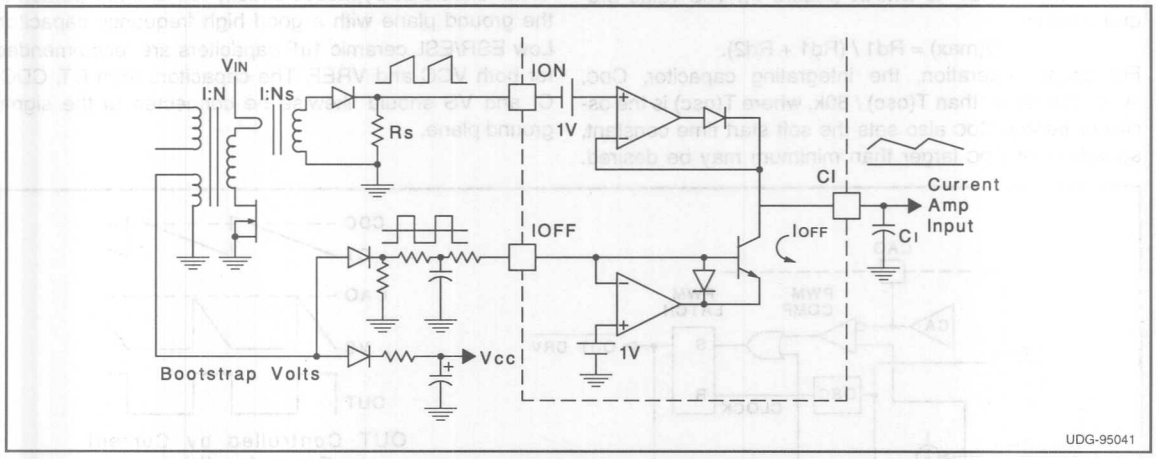


Figure 4: Inductor Current Waveform Synthesizer

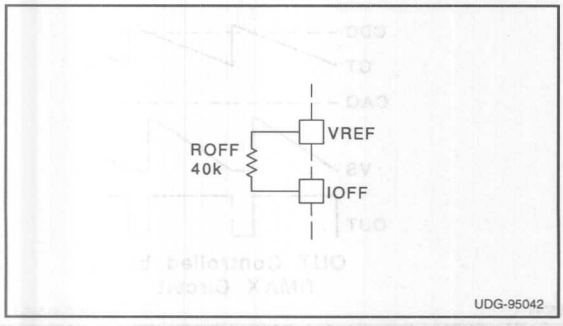


Figure 5: Fixed IOFF

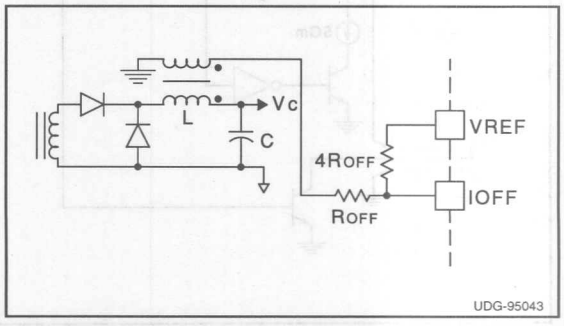


Figure 6: Second Inductor Winding Generation of IOFF

FEED FORWARD PULSE WIDTH MODULATION

Pulse width modulation is achieved by comparing the output of the current error amplifier to the feed forward ramp generated at VS (Figure 7). The charge slope of the ramp is determined by a resistor (RVS) from VS to VIN and a capacitor (CVS) from VS to GND. In the event that CAO is at its maximum voltage, typically 3.3V, the UC3548 will limit the power stage to a volt-second product of:

$$V_{IN} \bullet T_{ON}(max) = 3.3V \bullet Rvs \bullet Cvs.$$

An isolated voltage control loop can be implemented with a secondary side reference, error amplifier and an optoisolator. The optoisolator can be used to override the current amplifier output which is current limited by a 2.5k resistor. In overcurrent situations, the voltage loop turns the optoisolator off and the current error amplifier then assumes duty cycle control resulting in accurately limited maximum output current.

MAXIMUM DUTY CYCLE AND SOFT START

A patented technique is used to accurately program maximum duty cycle. Programming is accomplished by a divider from VREF to DMAX (Figure 7). The value programmed is:

$$D(max) = Rd1 / (Rd1 + Rd2).$$

For proper operation, the integrating capacitor, C_{DC}, should be larger than T(osc) / 80k, where T(osc) is the oscillator period. C_{DC} also sets the soft start time constant, so values of C_{DC} larger than minimum may be desired. The soft start time constant is approximately:

$$T(ss) = 20k \bullet C_{DC}.$$

GROUND PLANES

The output driver on the UC3548 is capable of 2A peak currents. Careful layout is essential for correct operation of the chip. A ground plane must be employed (Figure 8). A unique section of the ground plane must be designated for high di/dt currents associated with the output stage. This point is the power ground to which to PGND pin is connected. Power ground can be separated from the rest of the ground plane and connected at a single point, although this is not strictly necessary if the high di/dt paths are well understood and accounted for. VCC should be bypassed directly to power ground with a good high frequency capacitor. The source of the power MOSFET should connect to power ground as should the return connection for input power to the system and the bulk input capacitor. The output should be clamped with a high current Schottky diode to both VCC and PGND. Nothing else should be connected to power ground.

VREF should be bypassed directly to the signal portion of the ground plane with a good high frequency capacitor. Low ESR/ESL ceramic 1µF capacitors are recommended for both VCC and VREF. The capacitors from CT, CDC, CI and VS should likewise be connected to the signal ground plane.

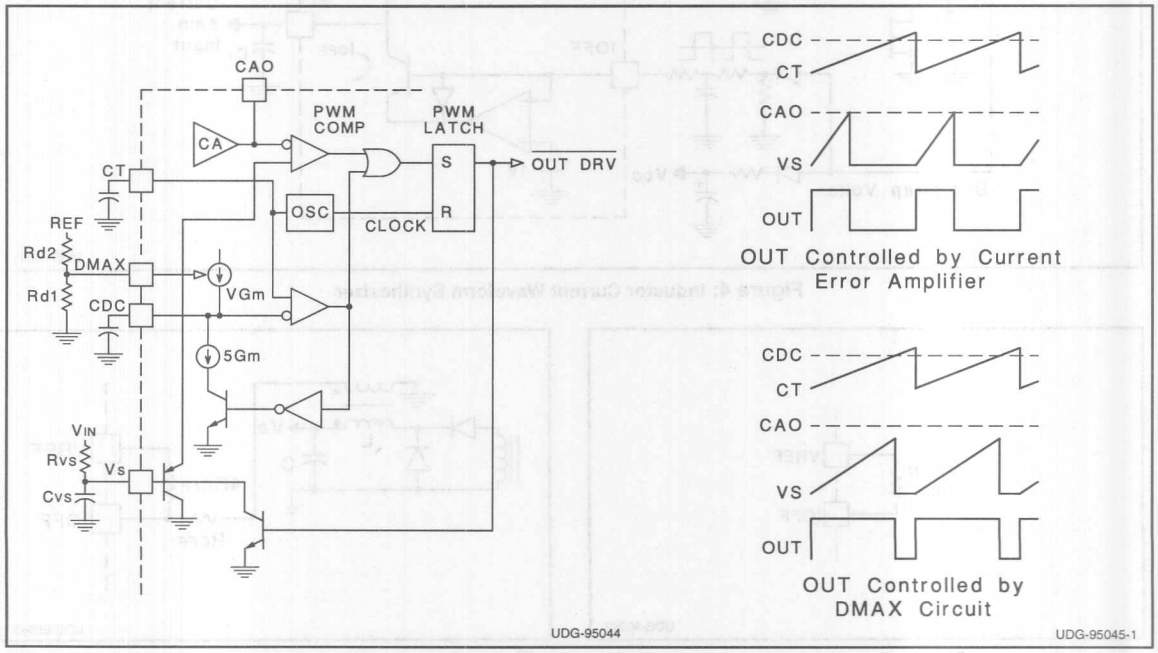


Figure 7: Duty Cycle Control

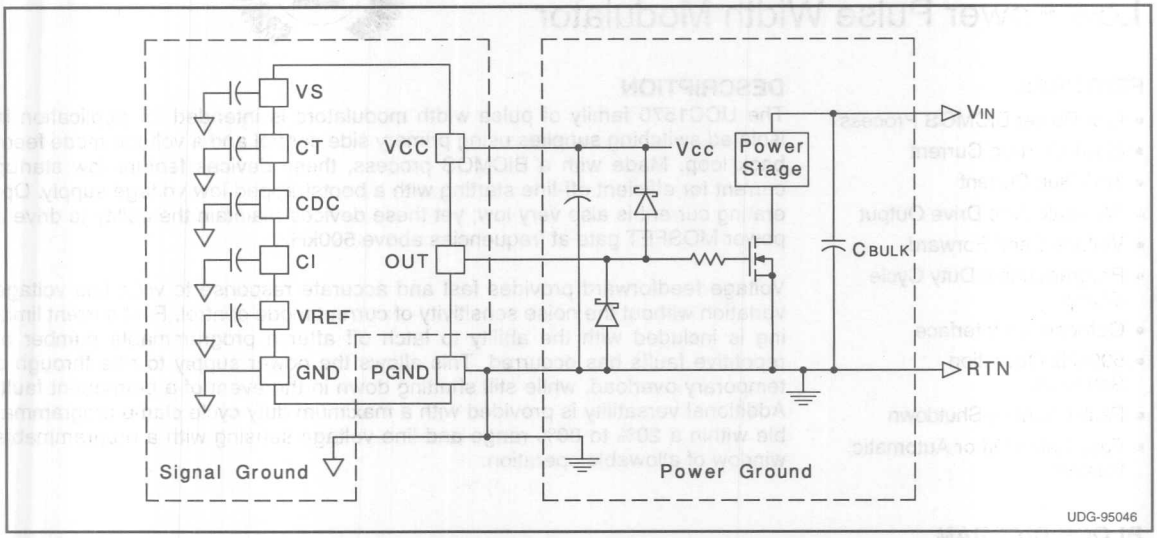


Figure 8: Ground Plane Considerations

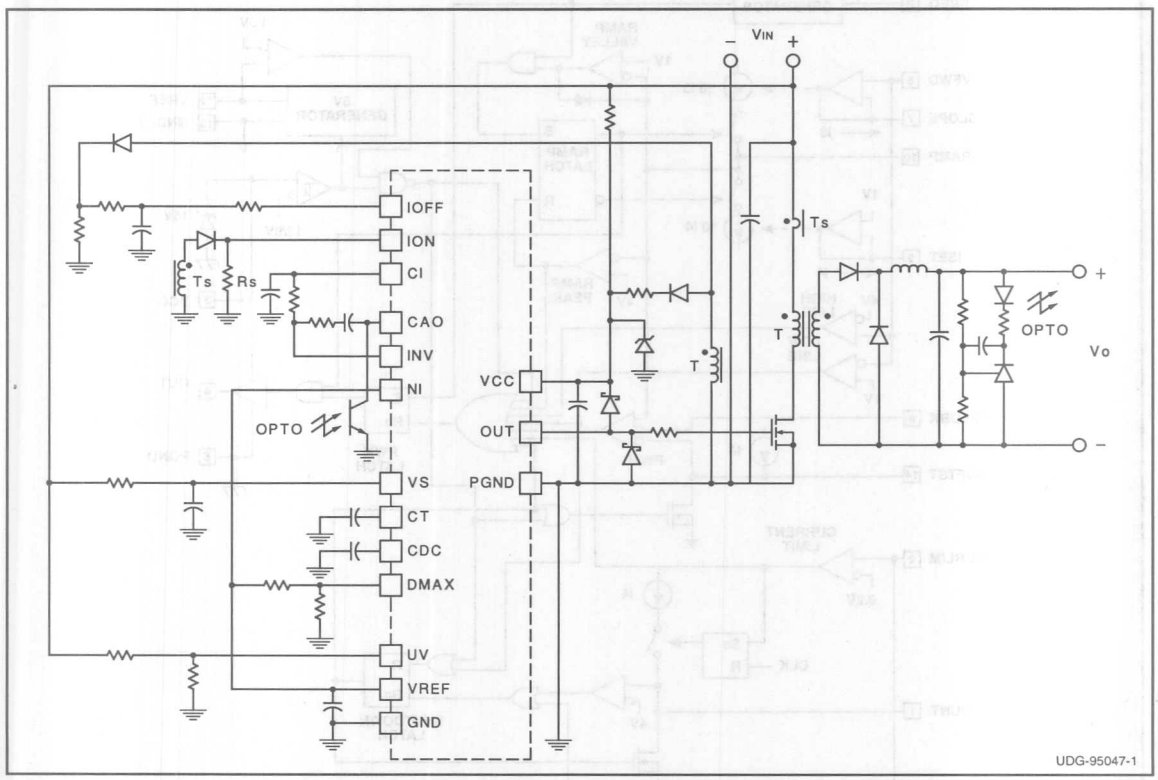


Figure 9: Typical Application - Voltage Feedforward Control Isolated Forward Converter with Average Current Limiting

UNITRODE CORPORATION
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UNITRODE

Low Power Pulse Width Modulator

FEATURES

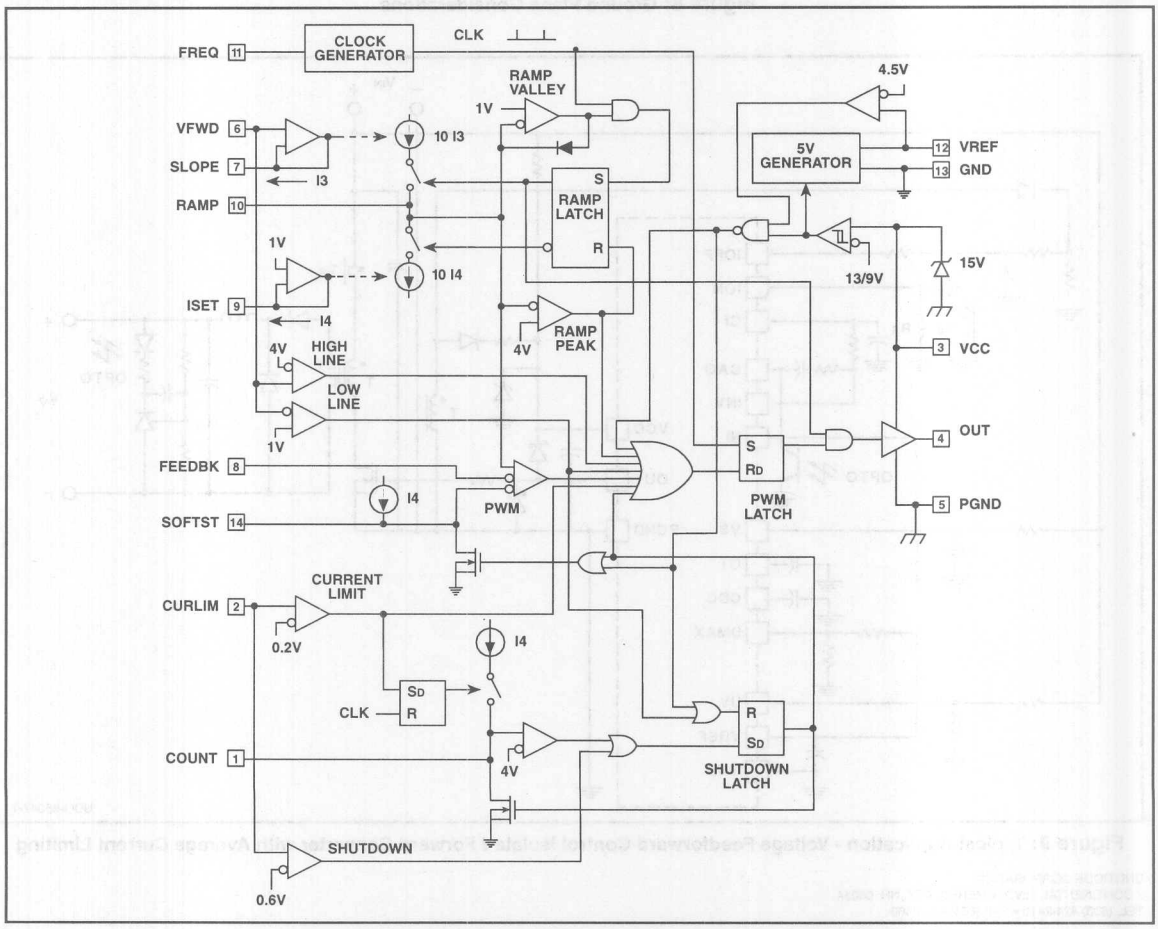
- Low Power BiCMOS Process
- 85µA Start-up Current
- 1mA Run Current
- 1A Peak Gate Drive Output
- Voltage Feed Forward
- Programmable Duty Cycle Clamp
- Optocoupler Interface
- 500kHz Operation Soft Start
- Fault Counting Shutdown
- Fault Latch Off or Automatic Restart

DESCRIPTION

The UCC1570 family of pulse width modulators is intended for application in isolated switching supplies using primary side control and a voltage mode feedback loop. Made with a BiCMOS process, these devices feature low startup current for efficient off-line starting with a bootstrapped low voltage supply. Operating current is also very low; yet these devices maintain the ability to drive a power MOSFET gate at frequencies above 500kHz.

Voltage feedforward provides fast and accurate response to wide line voltage variation without the noise sensitivity of current mode control. Fast current limiting is included with the ability to latch off after a programmable number of repetitive faults has occurred. This allows the power supply to ride through a temporary overload, while still shutting down in the event of a permanent fault. Additional versatility is provided with a maximum duty cycle clamp programmable within a 20% to 80% range and line voltage sensing with a programmable window of allowable operation.

BLOCK DIAGRAM



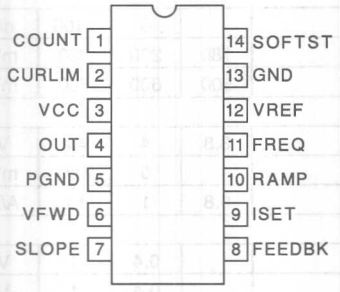
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Limit Supply Current to 20mA) ..... Self Limiting at 15 V
Supply Current ..... +20mA
Analog Inputs (CURLIM, VFWD, FEEBK) 6V
Programming Current (I (SLOPE), I (ISET)) ..... -1mA
Output Current (I (OUT)) ..... DC ..... ±180mA
..... Pulse (0.5ms) ..... ±1.2A

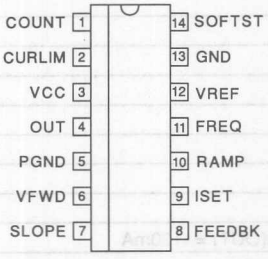
Note: *All voltages are with respect to GND. Currents are positive into the specified terminal.*

CONNECTION DIAGRAMS

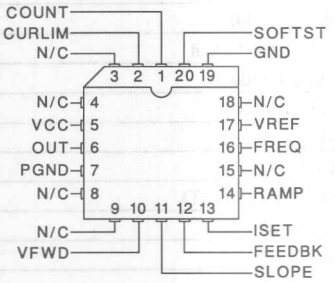
DIL-14 (TOP VIEW)
N or J PACKAGE



SOIC-14 (TOP VIEW)
D PACKAGE



PLCC-20 (TOP VIEW)
L Or Q PACKAGE



ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply for T_A = 0 to 70°C for the UCC3570, T_A= -40 to 85°C for the UCC2570, T_A=-55 to 125°C for the UCC1570, R(ISET)=100k, R(SLOPE)=121k, C(FREQ)=180pF, C(RAMP)=150pF, VCC=11V and T_A=T_J.

PARAMETER	TEST CONDITIONS	Min	Typ	Max	Units
Reference					
VREF	VCC=10 to 13V, I(VREF) = 0 to 2mA	4.9	5	5.1	V
Line Regulation	VCC = 10 to 13V		2	10	mV
Load Regulation	I(VREF) = 0 to 2mA		2	10	mV
Short Circuit Current	VREF = 0		10	50	mA
VCC					
Vth (On)		12	13		V
Vth (Off)		8	9	10	V
Hysteresis		3	4	5	V
VCC	I(VCC) = 10mA	13.5	15	16	V
I(VCC) Start	VCC = 11V, VCC Comparator Off		85	150	µA
I(VCC) Run	VCC Comparator On		1	1.5	mA
Line Sense					
Vth High Line Comparator		3.9	4	4.1	V
Vth Low Line Comparator		0.96	1	1.04	V
Iib (VFWD)			0	±100	nA
Oscillator					
Frequency		90	100	110	kHz
Ramp Generator					
I(RAMP)/I(SLOPE)		9	10	11	A/A
-I(RAMP)/I(ISET)		9	10	11	A/A
Peak Ramp Voltage		3.8	4	4.2	V
Valley Ramp Voltage		0.95	1	1.05	V
ISET Voltage Level		0.95	1	1.05	V

ELECTRICAL CHARACTERISTICS (cont.)

Unless otherwise stated, these specifications apply for T_A = 0 to 70°C for the UCC3570, T_A= -40 to 85°C for the UCC2570, T_A=-55 to 125°C for the UCC1570, R(ISET)=100k, R(SLOPE)=121k, C(FREQ)=180pF, C(RAMP)=150pF, VCC=11V and T_A=T_J.

PARAMETER	TEST CONDITIONS	Min	Typ	Max	Units
Soft Start					
Saturation	VCC = 11V, VCC Comparator Off		25	100	mV
I(SOFTST)/I(ISET)		0.8	1	1.2	A/A
Pulse Width Modulator					
lib(FEEDBK)			0	±100	n A
FEEDBK	Zero Duty Cycle	0.9	1	1.1	V
	Maximum Duty Cycle, Note 1	3.8	4	4.2	V
Current Limit					
lib(CURLIM)			0	±100	nA
Vth Current Limit		180	200	220	mV
Vth Shutdown		500	600	700	mV
Fault Counter					
Vth		3.8	4	4.2	V
Vsat			0	100	mV
I(COUNT)/I(ISET)		0.8	1	1.2	A/A
Output Driver					
Vsat High	I(OUT) = -100mA		0.4	1	V
Vsat Low	I(OUT) = 100mA		0.4	1	V
Rise/Fall Time	C(OUT) = 1nF, Note 1		20	100	ns

Note 1: *This parameter guaranteed by design but not 100% tested in production.*

PIN DESCRIPTION

VCC: Chip supply voltage pin. Bypass to PGND with a low ESL/ESR 0.1µF capacitor plus a capacitor for gate charge storage. Lead lengths must be minimum.

PGND: Ground pin for the output driver. Keep connections less than 2cm. Carefully maintain low impedance path for high current return.

OUT: Gate drive output pin. Connect to the gate of a power MOSFET with a resistor greater than 2 ohms. Keep connection lengths under 2cm.

VFWD: Voltage Feed Forward and Line Sense pin. Connect to input DC line using a resistive divider.

SLOPE: Program the charging current for RAMP with a resistor from this pin to GND. This pin will follow VFWD.

FEEDBK: Input to the pulse width modulator comparator. Drive this pin with an optocoupler to GND and a resistor to VREF. Modulation input range is from 1V to 4V.

ISET: A resistor from this pin to GND programs RAMP discharge current, FREQ current, SOFTST current, and COUNT current.

RAMP: Ramp Pin. Connect a capacitor to GND. Rising slope is programmed by current in SLOPE. This slope is compared to FEEDBK for pulse width modulation. The falling slope is programmed by the current in ISET and used to limit maximum duty cycle.

FREQ: Oscillator pin. Program the frequency with a capacitor to GND.

VREF: Precision 5V reference, and bypass point for internal circuitry. Bypass this pin with a 1µF minimum capacitor to GND.

GND: Analog ground. Connect to a low impedance ground plane containing all analog low current returns.

SOFTST: Soft start pin. Program with a capacitor to GND.

COUNT: Program the time that fault events will be tolerated before shutdown occurs with a capacitor and resistor to GND.

CURLIM: Current Limit Sense pin. Terminates OUT gate drive pulse for inputs over 0.2V. Enables fault counting function (COUNT). For inputs over 0.6V, the shutdown latch is activated.

FUNCTIONAL DESCRIPTION

(Note: Refer to Typical Application for external component names.) All the equations given below should be considered as first order approximations with final values determined empirically for a specific application.

Power Sequencing

VCC normally connects through a high impedance (R5) to the rectified line, with an additional path (R6) to a low voltage, bootstrap winding on the power transformer. VFWD normally connects to a divider (R1 and R2) from the rectified line. For circuit activation, all of the following conditions are required:

1. VFWD between 1V and 4V
2. VCC has been under 9V (to reset the shutdown latch)
3. VCC over 13V

FUNCTIONAL DESCRIPTION (cont.)

At this time, the circuit will activate. I(VCC) will increase from its start up value of 85µA to its run value of 1mA. The capacitor on SOFTST is charged with a current determined by

$$-I(SOFTST) = 1V/R4.$$

When SOFTST rises above 1V, output pulses will begin and I(VCC) will further rise to a level dictated by gate charge requirements as I(VCC) ≈ 1mA + Q_{Tfs}. With output pulses, the low voltage bootstrap winding should now power the controller. If VCC falls below 9V, the controller will turn off and the start sequence will reset and retry.

Vcc Clamp

An internal shunt regulator clamps V_{CC} so that it will not exceed 15V.

Output Inhibit

During normal operation, OUT is driven high at the start of a clock period and back low when RAMP either crosses FEEDBK or equals 4V. If, however, any of the following occur, OUT is immediately driven low for the remainder of the clock period:

1. VFWD is outside the range of 1V to 4V
2. CURLIM is greater than 0.2V
3. FEEDBK or SOFTST is less than 1V

Normal output pulses will not resume until the beginning of the next clock period in which none of the above conditions exist.

Current Limiting

CURLIM is monitored by two internal comparators. The current limit comparator threshold is 0.2V. If the current limit comparator is triggered, OUT is immediately driven low and held low for the remainder of the clock cycle, providing pulse-by-pulse overcurrent control for excessive loads. This comparator also causes C_F to be charged for the remainder of the clock cycle. The charging current is

$$-I(COUNT) = 1V/R4$$

If repetitive cycles are terminated by the current limit comparator causing COUNT to rise above 4V, the shutdown latch is set. The COUNT integration delay feature will be bypassed by the shutdown comparator which has a 0.6V threshold. The shutdown comparator immediately sets the shutdown latch. R_F in parallel with C_F resets the COUNT integrator following transient faults. R_F must be greater than (4 * R4.)/(1-D_{MAX})

Latched Shutdown

If CURLIM rises above 0.6V, or COUNT rises to 4V, the shutdown latch will be set. This will force OUT low, discharge SOFTST and COUNT, and reduce I(VCC) to approximately 1 mA. When, and if, VCC falls below 9V, the shutdown latch will reset and I(VCC) will fall to 85µA, allowing the circuit to restart. If VCC remains above 9V, an alternate restart will occur if VFWD is momentarily reduced below 1V. External shutdown commands from any source may be added into either the COUNT or CURLIM pins.

Deadtime Control

The voltage waveform on RAMP has independently controlled rising and falling edges. At the start of the clock period, RAMP is at 1V and rises to 4V. It then discharges back to 1V and awaits the next clock period. OUT can only be high during the rising part of the waveform, while it is positively blanked off during the falling portion. Setting the -dV/dt slope by R4 from ISET to GND establishes a minimum deadtime as:

$$td = 0.3 * R4 * C_R.$$

Choose R4 between 20k and 200k and C_R greater than 50pF. In order to have a pulse at OUT in the next clock period, RAMP must fall to 1V prior to the end of the current period. If it does not, OUT will remain low for the entire next clock period.

Voltage Feedforward

The +dV/dt on RAMP is made proportional to line voltage. The slope is:

$$dV/dt = 10 * VFWD / (R3 * C_R),$$

where VFWD is line voltage scaled by R1 and R2. Therefore, a changing line voltage will accomplish an immediate proportionate pulse width change without any action from the feedback amplifier. This will result in constant volt-second drive to the power transformer providing both international voltage operation, and excellent dynamic line regulation. VFWD is intended to operate over a 4:1 range (1V to 4V) with undervoltage and overvoltage sensors designed to drive OUT low if this range is exceeded. Choose R3 between 20k and 200k.

Frequency Set

A capacitor from FREQ to GND will determine a constant clock frequency. Frequency is:

$$F = 1.8/(R4 * C_T).$$

If required, frequency can be trimmed down from the above equation by the addition of R_T from FREQ to GND. The reduction in frequency is a function of the ratio of R_T/R4. R_T should be greater than 2.4 * R4 for reliable operation.

External synchronization can be accomplished by coupling a narrow pulse to a resistor inserted in series with the ground side of C_T. The value should be less than R4/200 and the synchronizing pulse width should be less than 5% of the oscillator period.

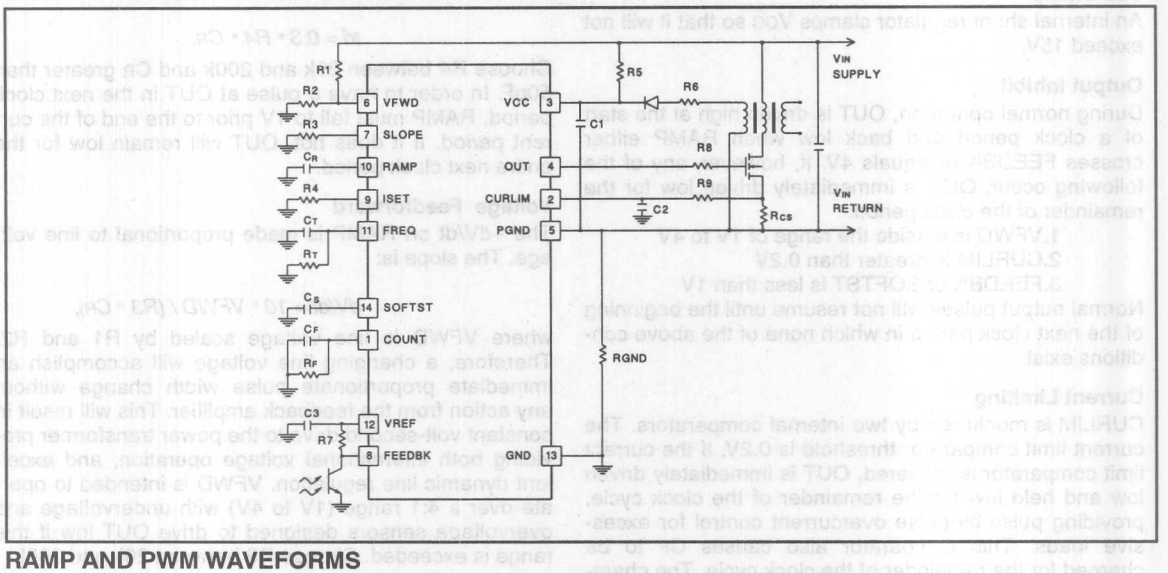
FUNCTIONAL DESCRIPTION (cont.)

External synchronization can also be accomplished by driving FREQ with an CMOS inverter. The inverter must be able to sink 4 * I4 with at a voltage less than the 3.5V upper threshold of the oscillator. It must also be able to source 36 * I4 at a voltage greater than the 1.5V lower threshold of the oscillator. As long as FREQ is held high, the output is guaranteed to be low.

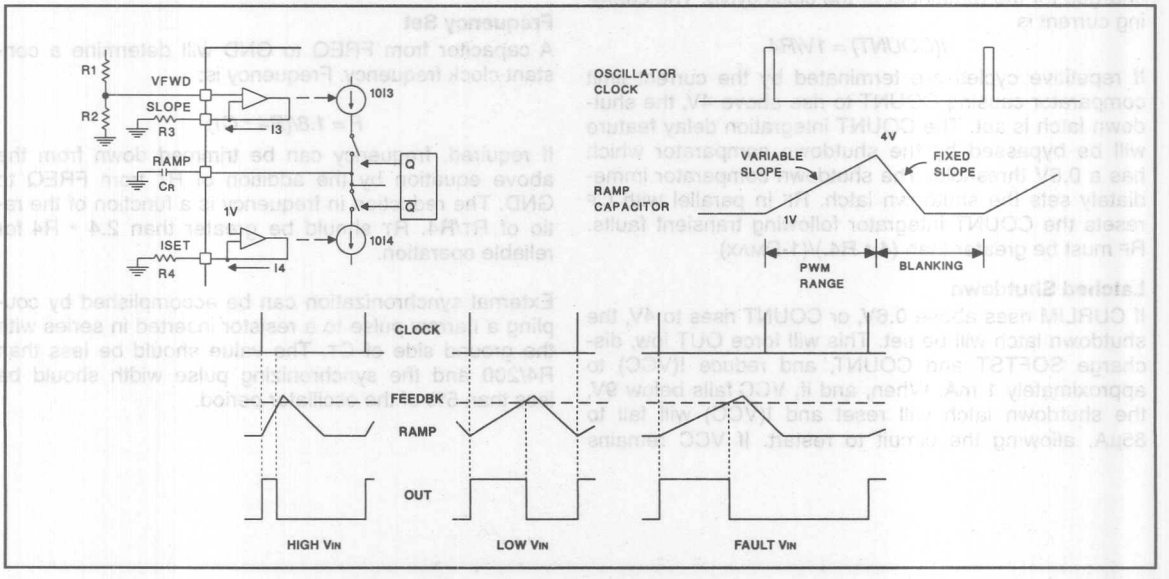
Gate Drive Output

The UCC1570 is capable of 1A peak output current. Bypass VCC with at least 0.1µF directly to PGND. Use a capacitor with low equivalent series resistance and inductance. The connection from OUT to the MOSFET gate should have a 2 ohm or greater damping resistor and the length should be minimized. A low impedance connection must be established between the MOSFET source (or the ground side of the current sense resistor), the VCC bypass capacitor and PGND. PGND should then be connected by a single path (shown as RGND in the application) to GND.

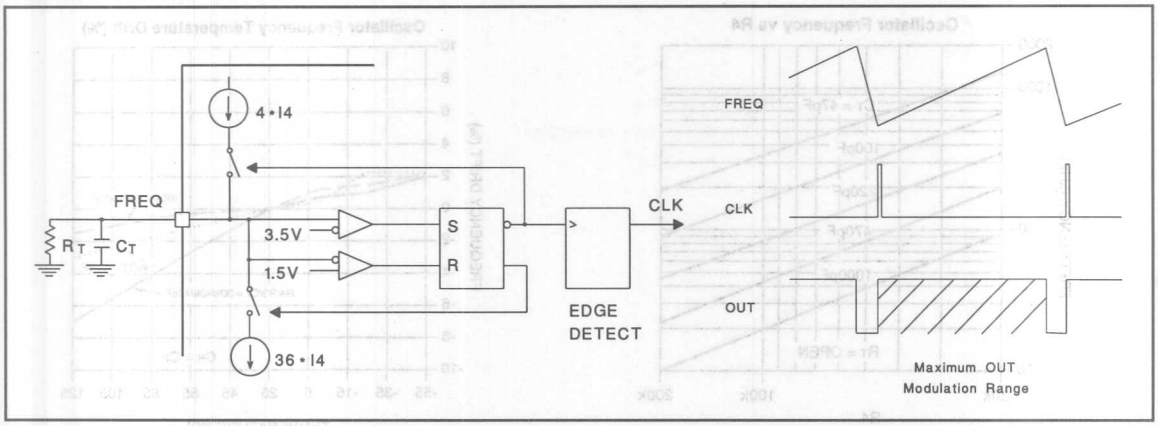
UCC1570 TYPICAL APPLICATION



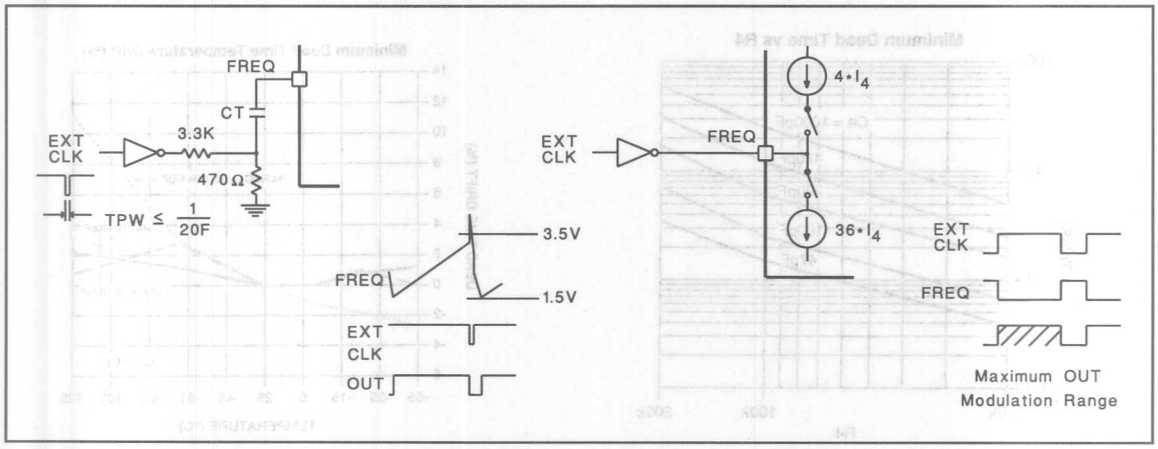
RAMP AND PWM WAVEFORMS



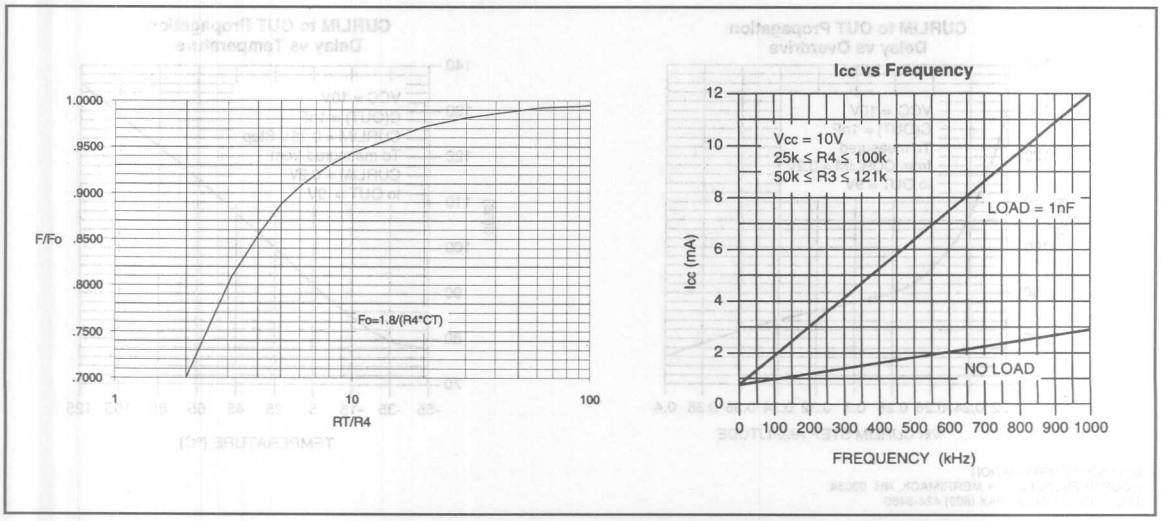
CLOCK GENERATOR



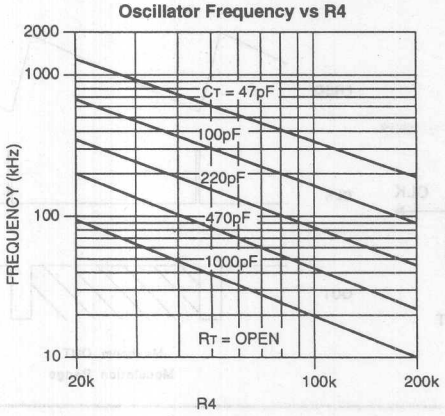
EXTERNAL CLOCK SYNCHRONIZATION



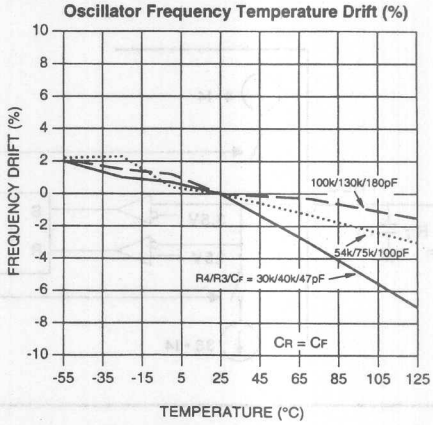
FREQUENCY DEPENDENCE ON RT/ R4 RATIO



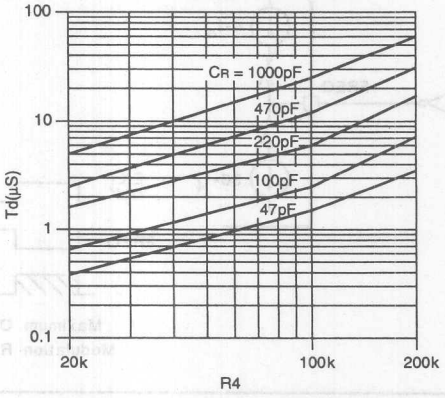
Oscillator Frequency vs R4



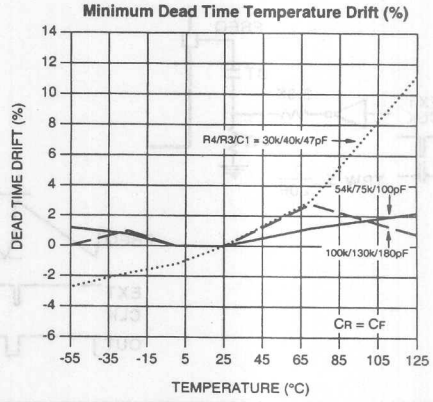
Oscillator Frequency Temperature Drift (%)



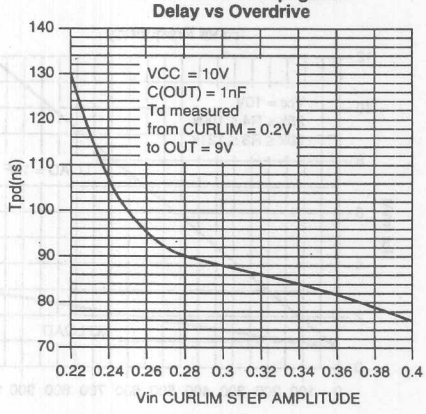
Minimum Dead Time vs R4



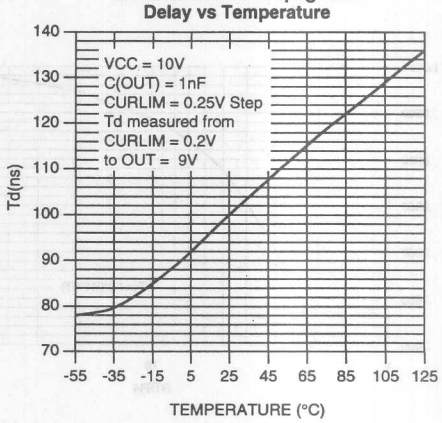
Minimum Dead Time Temperature Drift (%)



CURLIM to OUT Propagation Delay vs Overdrive



CURLIM to OUT Propagation Delay vs Temperature



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Negative Output Flyback Pulse Width Modulator

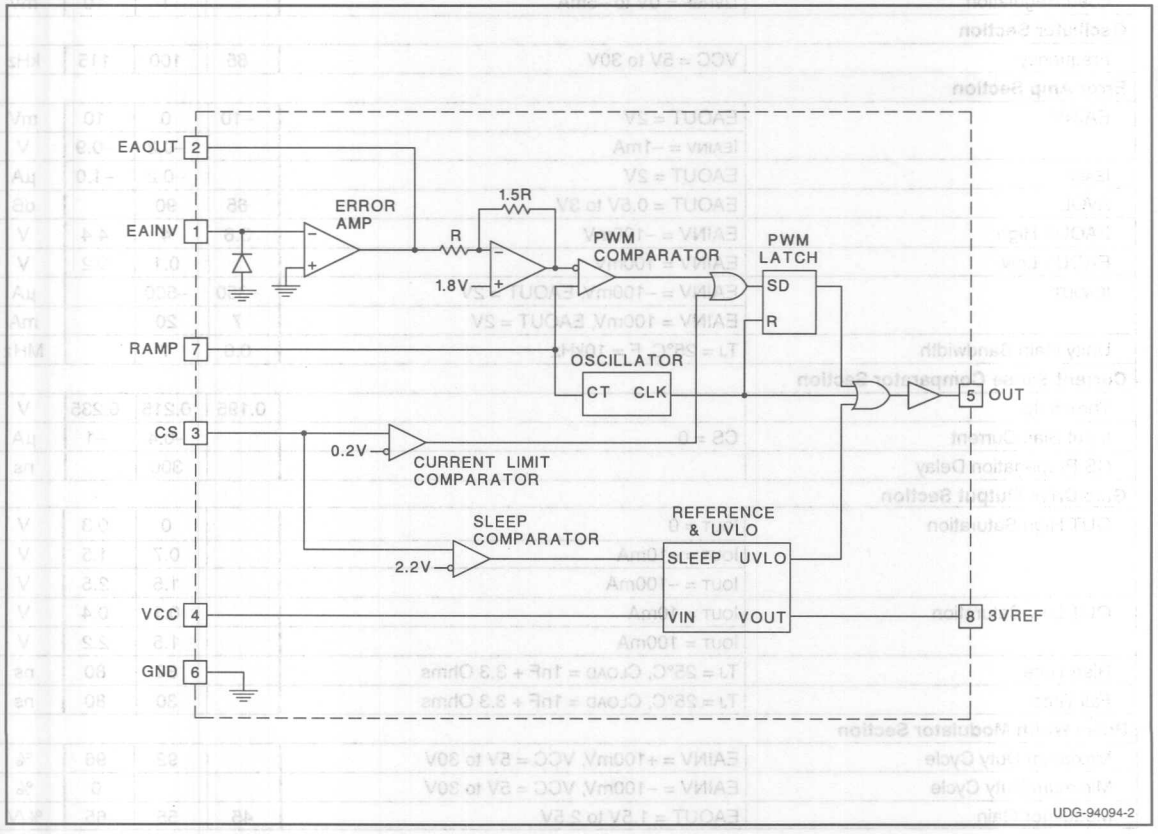
FEATURES

- Simple Single Inductor Flyback PWM for Negative Voltage Generation
- Drives External PMOS Switch
- Contains UVLO Circuit
- Includes Pulse-by-Pulse Current Limit
- Low 50µA Sleep Mode Current

DESCRIPTION

The UC3572 is a negative output flyback pulse width modulator which converts a positive input voltage to a regulated negative output voltage. The chip is optimized for use in a single inductor negative flyback switching converter employing an external PMOS switch. The block diagram consists of a precision reference, an error amplifier configured for voltage mode operation, an oscillator, a PWM comparator with latching logic, and a 0.5A peak gate driver. The UC3572 includes an undervoltage lockout circuit to insure sufficient input supply voltage is present before any switching activity can occur, and a pulse-by-pulse current limit. Output current can be sensed and limited to a user determined maximum value. The UVLO circuit turns the chip off when the input voltage is below the UVLO threshold.In addition, a sleep comparator interfaces to the UVLO circuit to turn the chip off. This reduces the supply current to only 50µA, making the UC3572 ideal for battery powered applications.

BLOCK DIAGRAM



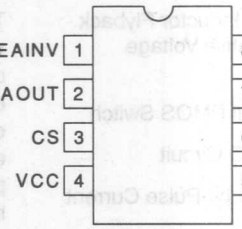
ABSOLUTE MAXIMUM RATINGS

VCC 35V
EAINV .....–0.6V to VCC
I_{EAOUT} 25mA
RAMP .....–0.3V to 4V
CS .....–0.3V to VCC
I_{OUT} .....–0.7A to 0.7A
I_{3VREF} .....–15mA
Storage Temperature .....–65°C to +150°C
Junction Temperature .....–65°C to +150°C
Lead Temperature (Soldering, 10 sec.) .....+300°C

Currents are positive into, negative out of the specified terminal.
Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAMS

DIL-8, SOIC-8 (TOP VIEW)
J or N, D Packages



ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these parameters apply for T_A = – 55°C to +125°C for the UC1572, – 40°C to +85°C for the UC2572, and 0°C to +70°C for the UC3572, VCC = 5V, CT = 680pF, T_A = T_J.

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
Reference Section					
3VREF		2.94	3	3.06	V
Line Regulation	VCC = 4.75 TO 30V		1	10	mV
Load Regulation	I_{3VREF} = 0V to –5mA		1	10	mV
Oscillator Section					
Frequency	VCC = 5V to 30V	85	100	115	kHz
Error Amp Section					
EAINV	EAOUT = 2V	–10	0	10	mV
	I_{EAINV} = –1mA		–0.2	–0.9	V
I_{EAINV}	EAOUT = 2V		–0.2	–1.0	µA
AVOL	EAOUT = 0.5V to 3V	65	90		dB
EAOUT High	EAINV = –100mV	3.6	4	4.4	V
EAOUT Low	EAINV = 100mV		0.1	0.2	V
I_{EAOUT}	EAINV = –100mV, EAOUT = 2V	–350	–500		µA
	EAINV = 100mV, EAOUT = 2V	7	20		mA
Unity Gain Bandwidth	T_J = 25°C, F = 10kHz	0.6	1		MHz
Current Sense Comparator Section					
Threshold		0.195	0.215	0.235	V
Input Bias Current	CS = 0		–0.4	–1	µA
CS Propagation Delay			300		ns
Gate Drive Output Section					
OUT High Saturation	I_{OUT} = 0		0	0.3	V
	I_{OUT} = –10mA		0.7	1.5	V
	I_{OUT} = –100mA		1.5	2.5	V
OUT Low Saturation	I_{OUT} = 10mA		0.1	0.4	V
	I_{OUT} = 100mA		1.5	2.2	V
Rise Time	T_J = 25°C, C_{LOAD} = 1nF + 3.3 Ohms		30	80	ns
Fall Time	T_J = 25°C, C_{LOAD} = 1nF + 3.3 Ohms		30	80	ns
Pulse Width Modulator Section					
Maximum Duty Cycle	EAINV = +100mV, VCC = 5V to 30V		92	96	%
Minimum Duty Cycle	EAINV = –100mV, VCC = 5V to 30V			0	%
Modulator Gain	EAOUT = 1.5V to 2.5V	45	55	65	%/V

ELECTRICAL CHARACTERISTICS (cont.) Unless otherwise stated, these parameters apply for T_A = – 55°C to +125°C for the UC1572, – 40°C to +85°C for the UC2572, and 0°C to +70°C for the UC3572, VCC = 5V, CT = 680pF, T_A = T_J.

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
Undervoltage Lockout Section					
Start Threshold		3.5	4.2	4.7	V
Hysteresis		100	200	300	mV
Sleep Mode Section					
Threshold		1.8	2.2	2.6	V
Supply Current Section					
Ivcc	VCC = 5V, 30V		9	12	mA
	VCC = 30, CS = 3V		50	150	µA

PIN DESCRIPTIONS

3VREF: Precision 3V reference. Bypass with 100nF capacitor to GND.

CS: Current limit sense pin. Connect to a ground referenced current sense resistor in series with the flyback inductor. OUT will be held high (PMOS switch off) if CS exceeds 0.2V.

EAINV: Inverting input to error amplifier. Summing junction for 3VREF and VOUT sense. The non-inverting input of the error amplifier is internally connected to GND.

EAOUT: Output of error amplifier. Use EAOUT and EAINV for loop compensation components.

GND: Circuit Ground.

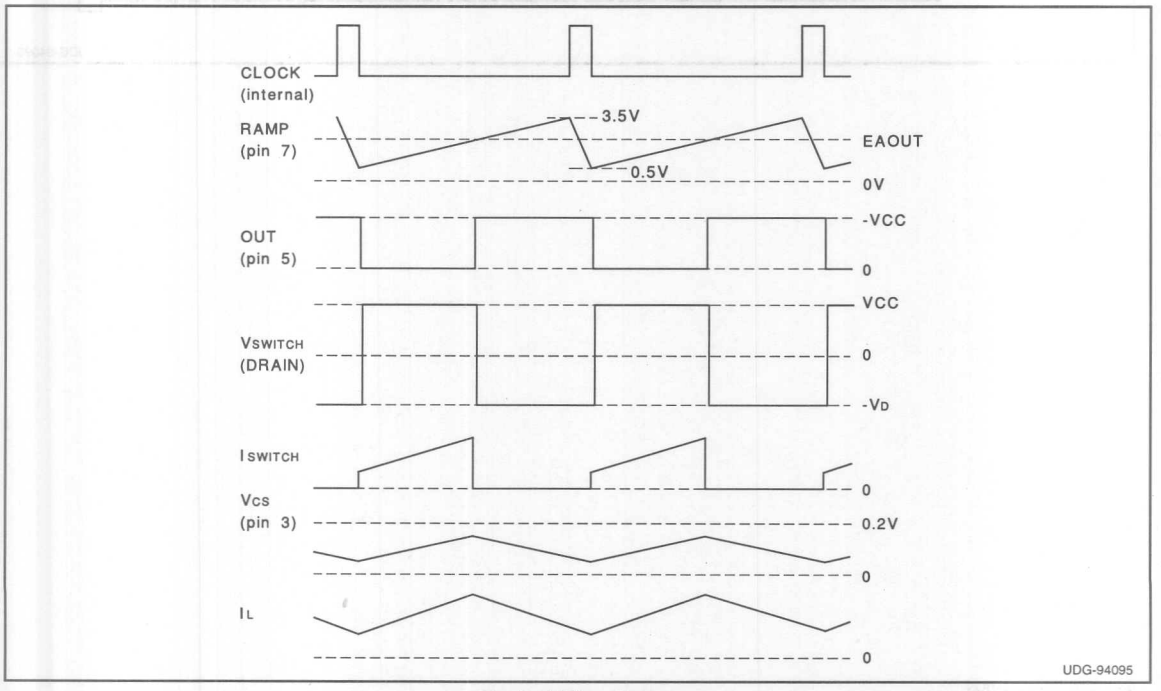
OUT: Gate drive for external PMOS switch connected between VCC and the flyback inductor. OUT drives the gate of the PMOS switch between VCC and GND.

RAMP: Oscillator and ramp for pulse width modulator. Frequency is set by a capacitor to GND by the equation

$$F = \frac{1}{15k \bullet C_{RAMP}}$$

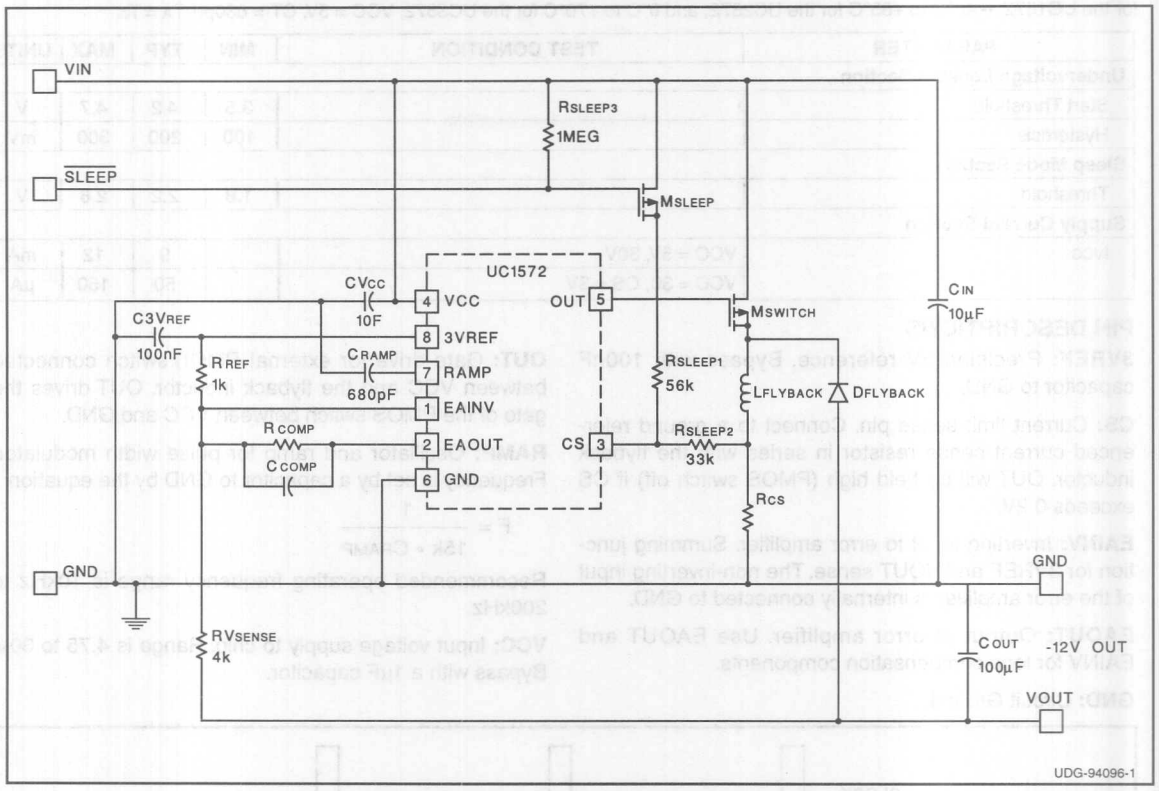
Recommended operating frequency range is 10kHz to 200kHz.

VCC: Input voltage supply to chip. Range is 4.75 to 30V. Bypass with a 1µF capacitor.



Typical Waveforms

TYPICAL APPLICATION : +5V TO -12V FLYBACK CONVERTER



UNITRODE CORPORATION
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TEL. 603-424-2410 • FAX 603-424-3460

Buck Pulse Width Modulator Stepdown Voltage Regulator

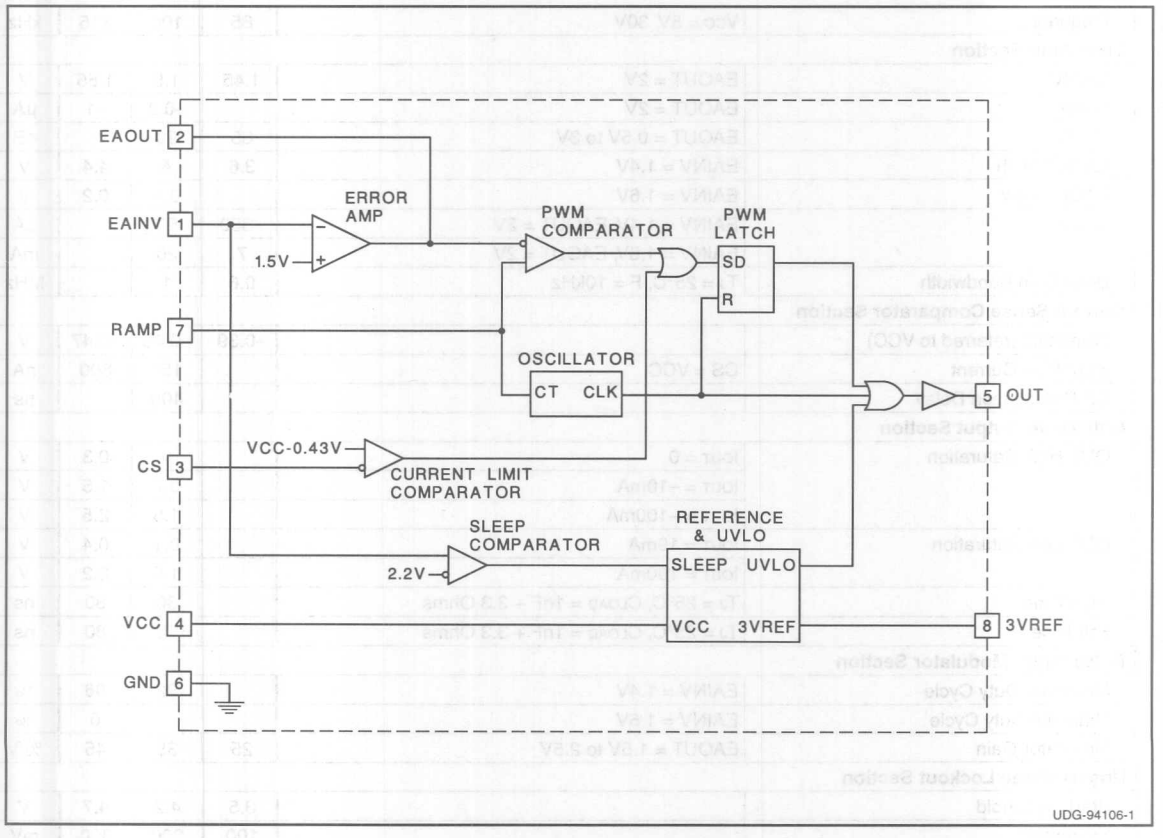
FEATURES

- Simple Single Inductor Buck PWM Stepdown Voltage Regulation
- Drives External PMOS Switch
- Contains UVLO Circuit
- Includes Pulse-by-Pulse Current Limit
- Low 50µA Sleep Mode Current

DESCRIPTION

The UC3573 is a Buck pulse width modulator which steps down and regulates a positive input voltage. The chip is optimized for use in a single inductor buck switching converter employing an external PMOS switch. The block diagram consists of a precision reference, an error amplifier configured for voltage mode operation, an oscillator, a PWM comparator with latching logic, and a 0.5A peak gate driver. The UC3573 includes an undervoltage lockout circuit to insure sufficient input supply voltage is present before any switching activity can occur, and a pulse-by-pulse current limit. Input current can be sensed and limited to a user determined maximum value. In addition, a sleep comparator interfaces to the UVLO circuit which turns the chip off when the input voltage is below the UVLO threshold. This reduces the supply current to only 50µA, making the UC3573 ideal for battery powered applications.

BLOCK DIAGRAM



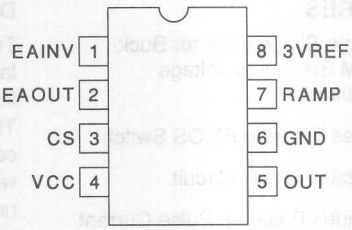
ABSOLUTE MAXIMUM RATINGS

VCC 35V
EAINV . . . . . .–0.6V to VCC
I_{EAOUT} 25mA
RAMP . . . . . .–0.3V to 4V
CS . . . . . .–0.3V to VCC
I_{OUT} . . . . . .–0.7A to 0.7A
I_{3VREF} . . . . . .–15mA
Storage Temperature . . . . . .–65°C to +150°C
Junction Temperature . . . . . .–65°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . .+300°C

Currents are positive into, negative out of the specified terminal.
Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAMS

DIL-8, SOIC-8 (TOP VIEW)
J or N, D Packages



ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these parameters apply for T_A = –55°C to +125°C for the UC1573, –40°C to +85°C for the UC2573, and 0°C to +70°C for the UC3573, VCC = 5V, CT = 680pF, $T_A = T_J$.

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
Reference Section					
3VREF		2.94	3	3.06	V
Line Regulation	VCC = 4.75 to 30V		1	10	mV
Load Regulation	I_{3VREF} = 0 to –5mA		1	10	mV
Oscillator Section					
Frequency	V_{CC} = 5V, 30V	85	100	115	kHz
Error Amp Section					
EAINV	EAOUT = 2V	1.45	1.5	1.55	V
I_{EAINV}	EAOUT = 2V		–0.2	–1	µA
AVOL	EAOUT = 0.5V to 3V	65	90		dB
EAOUT High	EAINV = 1.4V	3.6	4	4.4	V
EAOUT Low	EAINV = 1.6V		0.1	0.2	V
I_{EAOUT}	EAINV = 1.4V, EAOUT = 2V	–350	–500		µA
	EAINV = 1.6V, EAOUT = 2V	7	20		mA
Unity Gain Bandwidth	T_J = 25°C, F = 10kHz	0.6	1		MHz
Current Sense Comparator Section					
Threshold (referred to VCC)		–0.39	–0.43	–0.47	V
Input Bias Current	CS = VCC		150	800	nA
CS Propagation Delay			400		ns
Gate Drive Output Section					
OUT High Saturation	I_{OUT} = 0		0	0.3	V
	I_{OUT} = –10mA		0.7	1.5	V
	I_{OUT} = –100mA		1.5	2.5	V
OUT Low Saturation	I_{OUT} = 10mA		0.1	0.4	V
	I_{OUT} = 100mA		1.5	2.2	V
Rise Time	T_J = 25°C, C_{LOAD} = 1nF + 3.3 Ohms		30	80	ns
Fall Time	T_J = 25°C, C_{LOAD} = 1nF + 3.3 Ohms		30	80	ns
Pulse Width Modulator Section					
Maximum Duty Cycle	EAINV = 1.4V		92	96	%
Minimum Duty Cycle	EAINV = 1.6V			0	%
Modulator Gain	EAOUT = 1.5V to 2.5V	25	35	45	%/V
Undervoltage Lockout Section					
Start Threshold		3.5	4.2	4.7	V
Hysteresis		100	200	300	mV

ELECTRICAL CHARACTERISTICS (cont.) Unless otherwise stated, these parameters apply for T_A = –55°C to +125°C for the UC1573, –40°C to +85°C for the UC2573, and 0°C to +70°C for the UC3573, VCC = 5V, CT = 680pF, T_A = T_J.

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
Sleep Mode Section					
Threshold		1.8	2.2	2.6	V
Supply Current Section					
Ivcc	VCC = 30V		9	12	mA
Ivcc	VCC = 30V, EAINV = 3V		50	150	µA

PIN DESCRIPTIONS

3VREF: Precision 3V reference. Bypass with 100nF capacitor.

CS: Peak current limit sense pin. Senses the current across a current sense resistor placed between VCC and source of the PMOS Buck switch. OUT will be held high (PMOS buck switch off) if VCC – CS exceeds 0.4V.

EAINV: Inverting input to error amplifier. VOUT sense feedback connected to this pin. The non-inverting input of the error amplifier is internally connected to

$$\frac{3VREF}{2} \text{ volts.}$$

Connecting the EAINV pin to an external voltage greater than 2.6V commands the chip to go into a low current sleep mode.

EAOUT: Output of error amplifier. Use EAOUT and EAINV for loop compensation components.

GND: Circuit Ground.

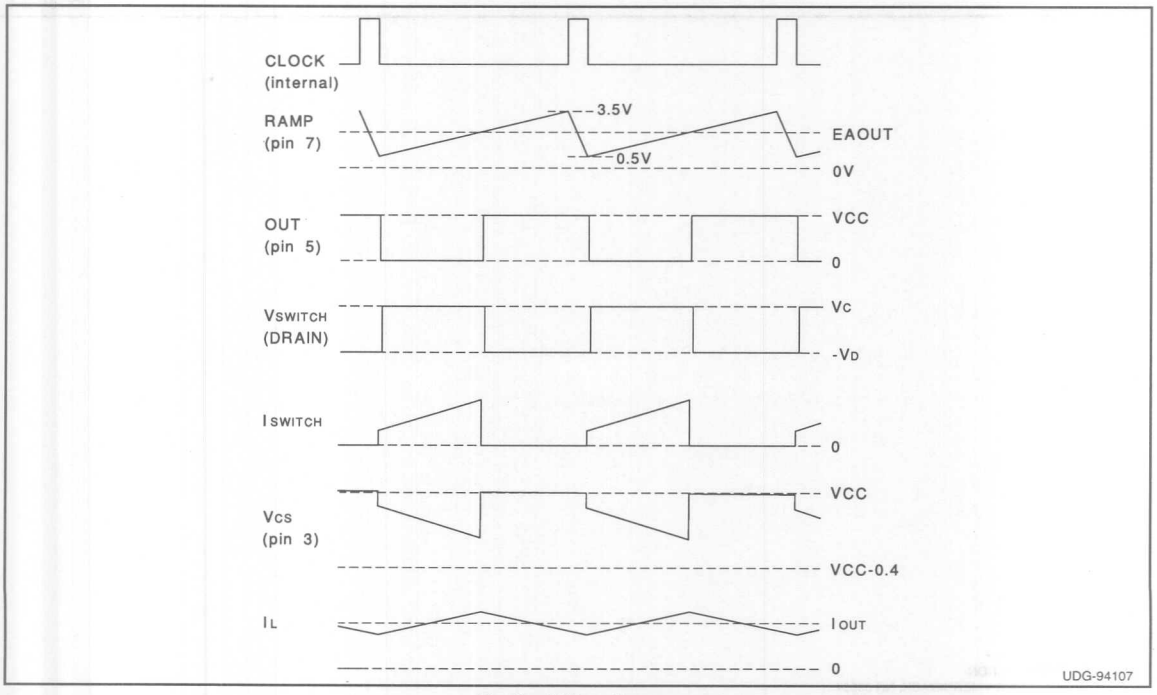
OUT: Gate drive for external PMOS switch connected between VCC and the flyback inductor. OUT drives the gate of the PMOS switch between VCC and GND.

RAMP: Oscillator and ramp for pulse width modulator. Frequency is set by a capacitor to GND by the equation

$$F = \frac{1}{15k \bullet C_{RAMP}}$$

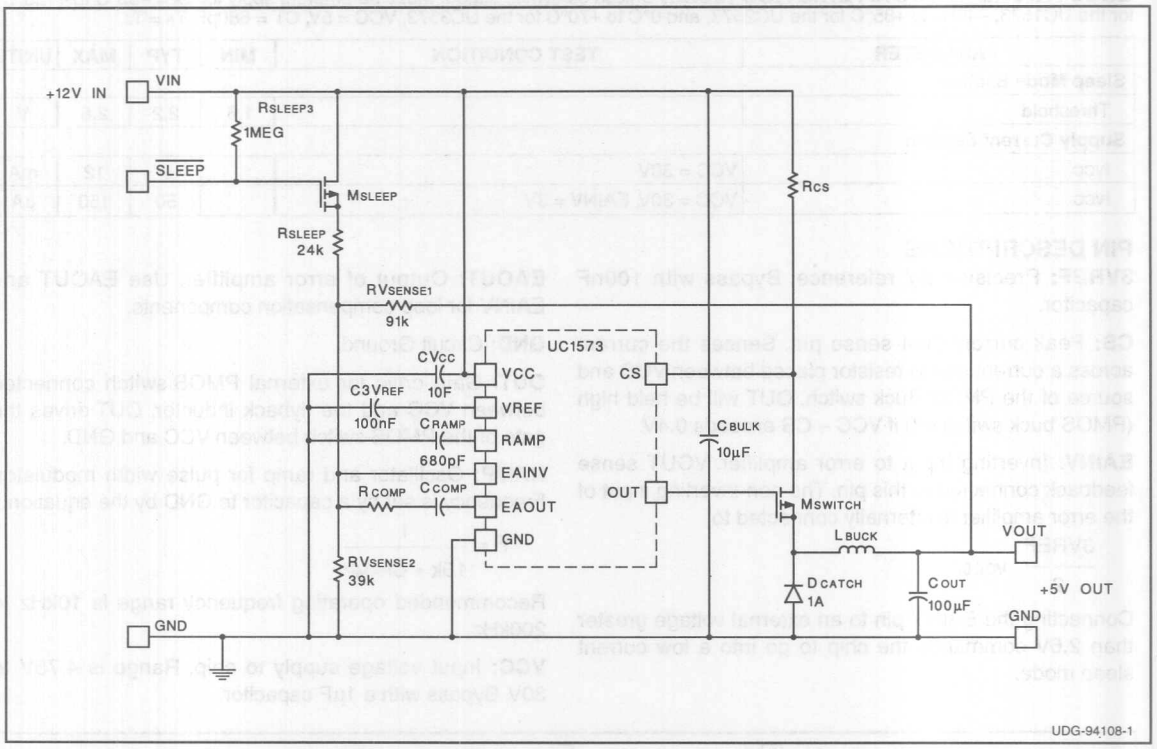
Recommended operating frequency range is 10kHz to 200kHz.

VCC: Input voltage supply to chip. Range is 4.75V to 30V. Bypass with a 1µF capacitor.



Typical Waveforms

TYPICAL APPLICATION: 12V TO 5V BUCK CONVERTER



UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

Buck Pulse Width Modulator Stepdown Voltage Regulator

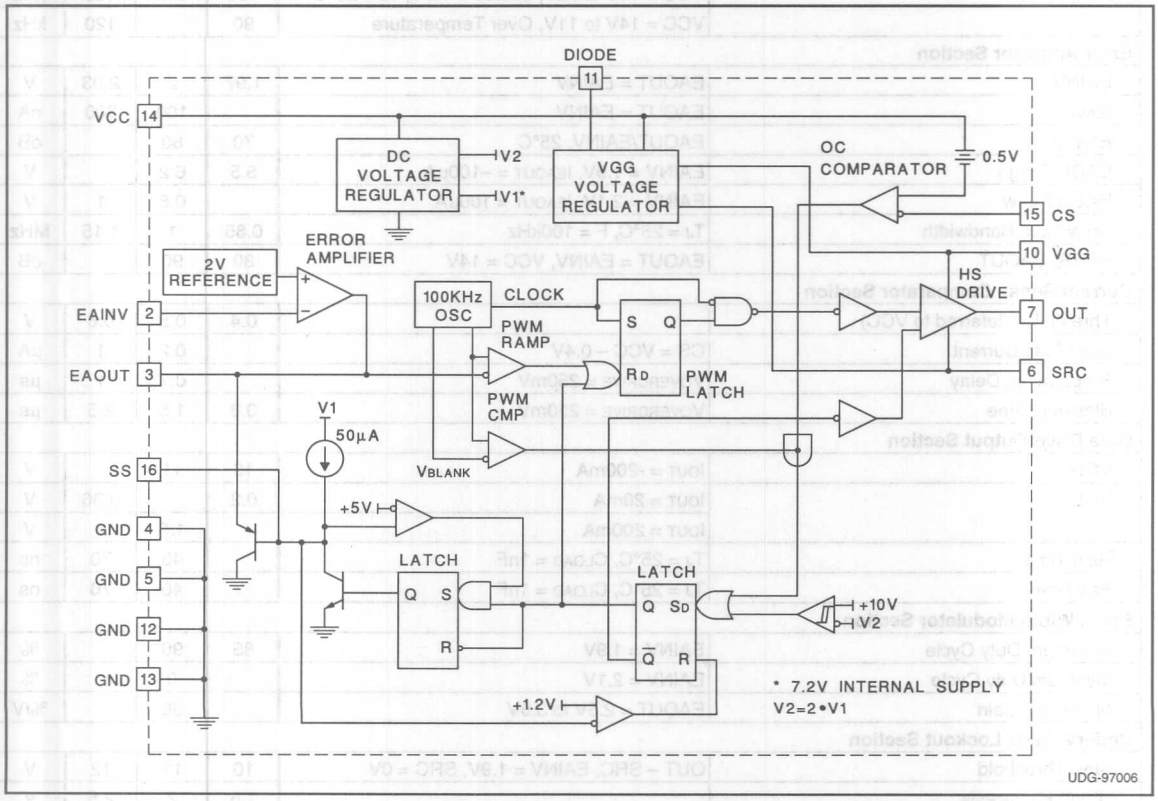
FEATURES

- Provides Simple Single Inductor Buck PWM Step-Down Voltage Regulation
- Drives External High Side NMOS Switch
- 14V to 72V Input Voltage Operating Range
- Contains 100kHz Internal Oscillator, 2V Reference and UVLO
- Includes Soft Start on Power Up
- Includes Overcurrent Shutdown Followed by Soft Start

DESCRIPTION

The UC3578 is a high side buck pulse width modulator with a floating gate driver which steps down and regulates a positive input voltage. The chip is optimized for use in a single inductor buck switching converter employing an external NMOS switch. The block diagram consists of a precision reference, an error amplifier configured for voltage mode operation, a 100kHz oscillator, a PWM comparator with latching logic and a high current gate driver. The UC3578 includes an under voltage lockout circuit to insure sufficient input supply voltage is present before any switching activity can occur, and overcurrent shutdown followed by soft start. Input current can be sensed and limited to a user defined maximum.

BLOCK DIAGRAM



1/97

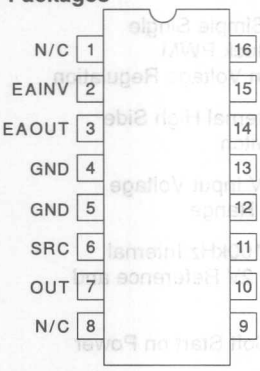
ABSOLUTE MAXIMUM RATINGS

VCC ..... +72V
EAINV ..... –0.3V to +10V
EAOUT ..... –0.3V to +10V
SS ..... –0.3V to +10V
DIODE ..... –0.3V to VCC
VGG ..... –0.3V to VCC + 14V
CS ..... VCC – 5V to VCC + 0.6V
IOUT Pulsed ..... –0.6A to 0.8A
SRC ..... –0.6V to VCC
Storage Temperature ..... –65°C to +150°C
Junction Temperature ..... –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

Currents are positive into, negative out of the specified terminal.
Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

DIL-16.SOIC-16(Top View)
N or DP Packages



ELECTRICAL CHARACTERISTICS

Unless otherwise specified, –40°C to 85°C for the UC2578, and 0°C to 70°C for the UC3578, VCC = 14V, VGG = 14V, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator Section					
Frequency	VCC = 14V to 72V, EAINV = 1.9V, T_J = 25°C	100	110	120	kHz
	VCC = 14V to 11V, Over Temperature	90		120	kHz
Error Amplifier Section					
EAINV	EAOUT = EAINV	1.97	2	2.03	V
I_{EAINV}	EAOUT = EAINV		100	300	nA
EAVOL	EAOUT/EAINV, 25°C	70	80		dB
EAOUT High	EAINV = 1.9V, I_{EAOUT} = –100µA	5.5	6.2		V
EAOUT Low	EAINV = 2.1V, I_{EAOUT} = 100µA		0.8	1	V
Unity Gain Bandwidth	T_J = 25°C, F = 100kHz	0.85	1	1.15	MHz
PSRR, EAOUT	EAOUT = EAINV, VCC = 14V	80	90		dB
Current Sense Comparator Section					
Threshold (Referred to VCC)		0.4	0.5	0.6	V
Input Bias Current	CS = VCC – 0.4V		0.2	1	µA
Propagation Delay	$V_{OVERDRIVE}$ = 250mV		0.7	1	µs
Blanking Time	$V_{OVERDRIVE}$ = 250mV	0.8	1.5	2.5	µs
Gate Drive Output Section					
VOH	I_{OUT} = -200mA	10	11		V
VOL	I_{OUT} = 20mA	0.2		0.36	V
	I_{OUT} = 200mA		1.5	2	V
Rise Time	T_J = 25°C, C_{LOAD} = 1nF		40	70	ns
Fall Time	T_J = 25°C, C_{LOAD} = 1nF		40	70	ns
Pulse Width Modulator Section					
Maximum Duty Cycle	EAINV = 1.9V	85	90		%
Minimum Duty Cycle	EAINV = 2.1V		0		%
Modulator Gain	EAOUT = 2.5V to 3.5V		30		%/V
Undervoltage Lockout Section					
Start Threshold	OUT – SRC, EAINV = 1.9V, SRC = 0V	10	11	12	V
UVLO Hysteresis		1.5	2	2.5	V

ELECTRICAL CHARACTERISTICS (cont.) Unless otherwise specified, –40°C to 85°C for the UC2578, and 0°C to 70°C for the UC3578, VCC = 14V, VGG = 14V, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VGG Regulator Section					
VGG – SRC	VCC = 72V	14.5	15.25	16	V
	VCC = 50V, SRC = 0V, I_{VGG} = –7mA	14	14.75	15.5	V
	VCC = 15V, SRC = 0V, I_{VGG} = –7mA	13	13.75	14.5	V
	VCC = 11V, SRC = 0V, I_{VGG} = –7mA	9.5	10	10.5	V
Soft Start Ramp Section					
Soft Start Ramp Current		–30	–45		µA
Supply Current Section					
I_{VCC}	EAINV = 2.1V, SRC = 0V		10	14	mA
I_{VGG}	EAINV = 2.1V, SRC = 0V		7	10.5	mA

PIN DESCRIPTIONS

CS: Peak current limit sense pin. Senses the current across a current sense resistor placed between VCC and the drain of the NMOS buck switch. OUT will be held low (NMOS buck switch off) if VCC – CS exceeds 0.5V.

DIODE: An external small signal diode (1N4148 typical) is connected here, anode to VCC and cathode to DIODE, to implement the VGG regulator function.

EAINV: Inverting input to error amplifier. V_{OUT} sense feedback is connected to this pin. The non-inverting input of the error amplifier is internally connected to 2V.

EAOUT: Output of the error amplifier. Use EAOUT and EAINV for loop compensation components.

GND: Circuit Ground.

OUT: Gate drive for the external NMOS switch connected between VCC and the buck inductor.

SRC: This pin is connected to the junction of the external NMOS switch source, the floating voltage source capacitor, the free-wheeling diode cathode, and buck inductor.

SS: The external soft start capacitor is connected to this pin.

VGG: An external capacitor connected from VGG to SRC completes the floating voltage source for the floating gate driver. A 1µF capacitor is recommended.

VCC: Input supply voltage. This pin supplies an internal ground referenced voltage regulator that supplies the IC and an on-chip regulated floating voltage source (VGG – SRC) used by the floating driver to drive the external NMOS buck switch. This pin should be bypassed with a high quality ceramic capacitor.

APPLICATION INFORMATION

The UC3578 Floating Buck Controller is a high frequency switching regulator with a floating driver which provides PWM control for non-isolated buck converters. The controller operates at a fixed 100 kHz switching frequency, and in voltage mode control. The duty cycle range of the PWM output is 0% to 90% allowing for a wide range of input voltages (14V minimum with transients to 72V). The regulator features an undervoltage lockout threshold of 11V with approximately 2V hysterisis as well as soft start capability. A typical application circuit is shown in Figure 2 for a 15V to 40V input and a 12V at 3A output.

As shown in Figure 2 for proper operation of the floating driver an external capacitor (1µF ceramic) must be connected from VGG to SRC the source of the external MOSFET. This capacitor provides the energy for the high side driver. The gate drive voltage to the MOSFET is internally regulated to 14V. A diode (1N4148) is required from the input voltage to DIODE. This allows the floating drive capacitor to charge during conduction of the output rectifier but prevents its discharge back into the supply rail. A 1µF ceramic capacitor is recommended from VCC to ground to provide high frequency decoupling. Additional decoupling of this pin could be accomplished by a low value resistor between VCC and V_{IN} and a 1µF capacitor from VCC to GND as shown in the schematic.

CURRENT LIMIT

The current sense pin provides overcurrent shutdown. As can be seen from the block diagram, the overcurrent comparator is wire ANDed with the oscillator after an internally set blanking time. The I_{LIMIT} threshold level is set by the current sense resistor from R_{SENSE}.

$$I_{LIMIT} = \frac{0.5V}{R_{SENSE}}$$

APPLICATION INFORMATION (cont.)

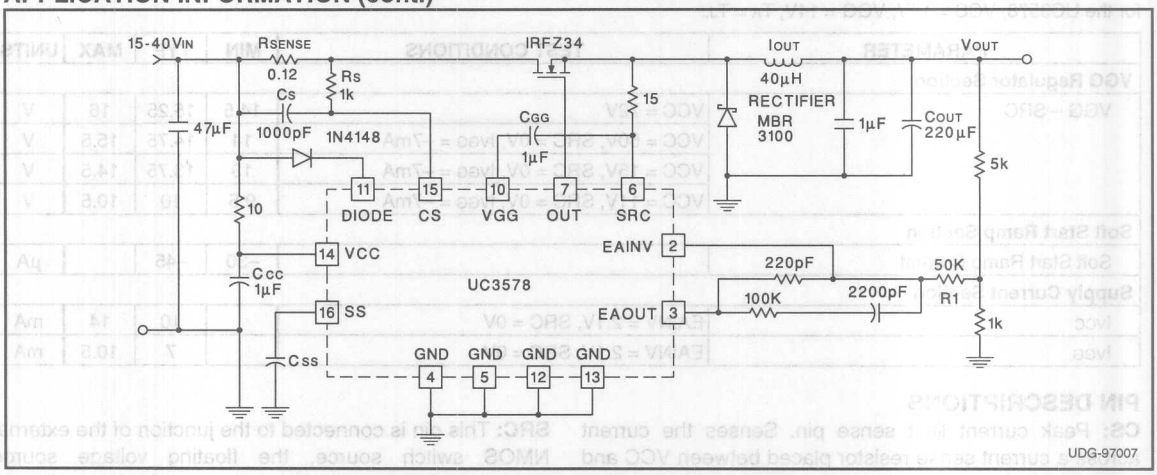


Figure 2. Typical Application

An optional filter can be added (RsCs) from the current sense resistor to CS to provide high frequency filtering of the current sense signal if necessary.

During a current limit condition, the soft start capacitor on SS is discharged until its voltage level reaches 1.2V. During this time, a duty cycle clamp is activated to approximately 0.6V above the voltage level on the SS capacitor. This condition persist until the SS capacitor is discharged to 1.2V, thus disabling the output driver. At this time, the SS capacitor is allowed to charge to 5V through the 50µA current source and normal operation resumes when the SS capacitor reaches 5V. During the condition described, the regulator enters a hiccup current limit mode of operation which limits the power dissipation in the MOSFET and output rectifier under a short circuit condition.

ERROR AMPLIFIER

The onboard error amplifier of the UC3578 is a voltage amplifier with its non-inverting input tied to an internal 2V reference. As usual, loop compensation can be added from the inverting input of EAINV to the error amplifier output at EAOUT. Consideration must be given when choosing the values of the compensation components around the amplifier so that the output swing of the amplifier is not restricted. The output of the amplifier can source 100µA typically.

GENERAL

As in any buck converter, when the switch is off, the MOSFET's source flies low due to the conduction of the free-wheeling rectifier. The source (SRC) is pulled below ground by an amount determined by the forward voltage drop of the rectifier and by any transient voltage spike from inductance in this path. The occurrence of this condition could result in erratic operation of the IC during this period if the negative excursion is not limited. This is because of conduction of current in the substrate of the IC due to the source pin being pulled below ground and forward biasing the internal substrate PN junction. To limit this effect, a small resistor (15Ω) can be placed in series between the MOSFET source and the SRC pin as shown in Figure 2. Too large a resistor will limit the drive to the MOSFET and result in startup problems with the regulator. A Schottky rectifier is used for the free-wheeling diode to limit the negative excursion of the source. This will also limit the reverse recovery current thus limiting the inductive voltage spike.

In applications where transient load excursions may result in a no load condition, it is necessary that the output of the regulator be loaded with a small load current (10mA to 15mA). This will prevent the output voltage from going unregulated at no load. This small load current is necessary for proper operation of the floating driver since the source must fly low to charge up the floating driver capacitance.

THERMAL CONSIDERATIONS

For proper operation and reliability of the UC3578, proper thermal management is essential. It is important that the designer keep in mind that with surface mount packages, a significant amount of their heat that the device generates is conducted out through the lead frame. Because of this, the PCB design becomes a critical part of the thermal management system. Worst case junction-to-ambient thermal resistance for different package

APPLICATION INFORMATION (cont.)

configurations are given in a table in the data book in the package information section.

The maximum ambient operating temperature is an important factor in determining what the maximum operating voltage can be for a particular application. For example, if we assume a maximum operating ambient temperature of 70°C we can determine what the maximum allowable input voltage can be given other parameters such as package thermal impedance and MOSFET total gate charge by following the procedure outlined below;

$$T_{JMAX} - T_A = 125°C - 70°C = 55°C \quad (1)$$

$$Pd = \frac{55°C}{58°C/W} = 0.95W \quad (2)$$

where 58°C/W is the worst case theta j-a for the 16 pin DP package and Pd is the package power dissipation.

$$Pd = (Qg \times 100kHz + 19mA) \bullet V_{IN} \quad (3)$$

where Qg is the total MOSFET gate charge and 19mA is the maximum quiescent current for the UC3578 (I_{CC} + I_{GG}) from the data sheet. The switching frequency of the buck converter is 100kHz.

The gate charge can be determined from the MOSFET-data sheet. As an example, for a IRFZ34 which has a total gate charge of 46nC, substituting for Pd in equation 3:

$$0.95W = (46nC \times 100\ kHz + 19mA)\ V_{IN}$$

$$V_{IN\ MAX} = \frac{0.95W}{0.0236A} = 40V$$

Therefore, at 70°C using a IRFZ34 MOSFET the maximum input voltage is limited to 40V to maintain a maximum junction temperature of 125°C in the 16 pin DP package.

Higher input voltages can be achieved by choosing a MOSFET with a lower total gate charge or by a reduced ambient operating temperature or by reducing the theta j-a of the package by improving the PCB mounting method. It is recommended that the four GND pins (4,5,12 and 13) be connected to a ground plane to provide a low resistance thermal path. If a ground plane is not available, a heat spreader on a double sided PC board is recommended.

Note: Thermal impedance number is based on device mounted to 5 square inch FR4 PC board with one ounce copper. From Unitrode 95-96 data book Table 1, page 9-8, when resistance range is given, lower thermal impedance values are for 5 square inch aluminum PC board.

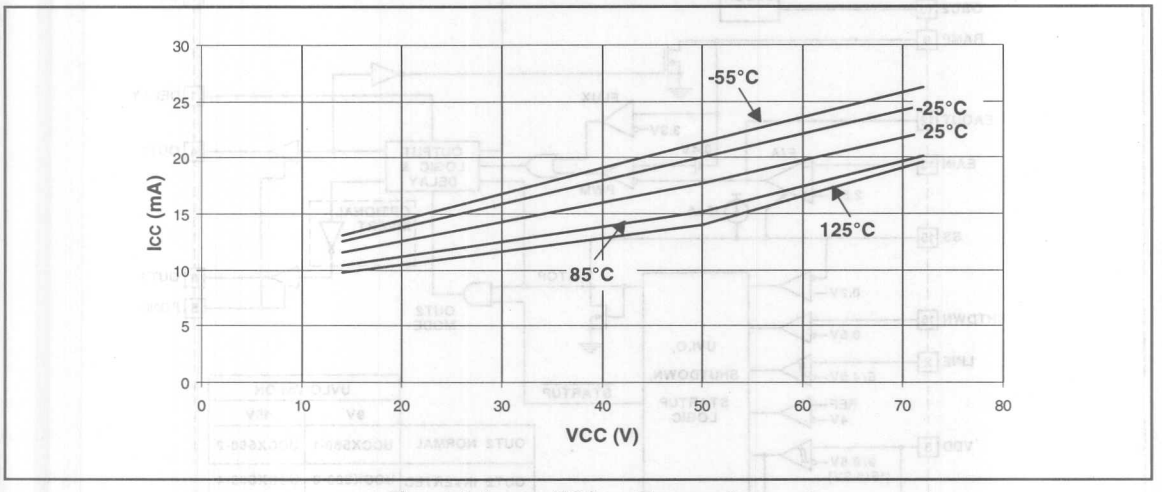


Figure 3. Icc vs. VCC vs. Temperature

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

Single Ended Active Clamp/Reset PWM

FEATURES

- Provides Auxiliary Switch Activation Complementary to Main Power Switch Drive
- Programmable deadtime (Turn-on Delay) Between Activation of Each Switch
- Voltage Mode Control with Feedforward Operation
- Programmable Limits for Both Transformer Volt-Second Product and PWM Duty Cycle
- High Current Gate Driver for Both Main and Auxiliary Outputs
- Multiple Protection Features with Latched Shutdown and Soft Restart
- Low Supply Current (100µA Startup, 1.5mA Operation)

DESCRIPTION

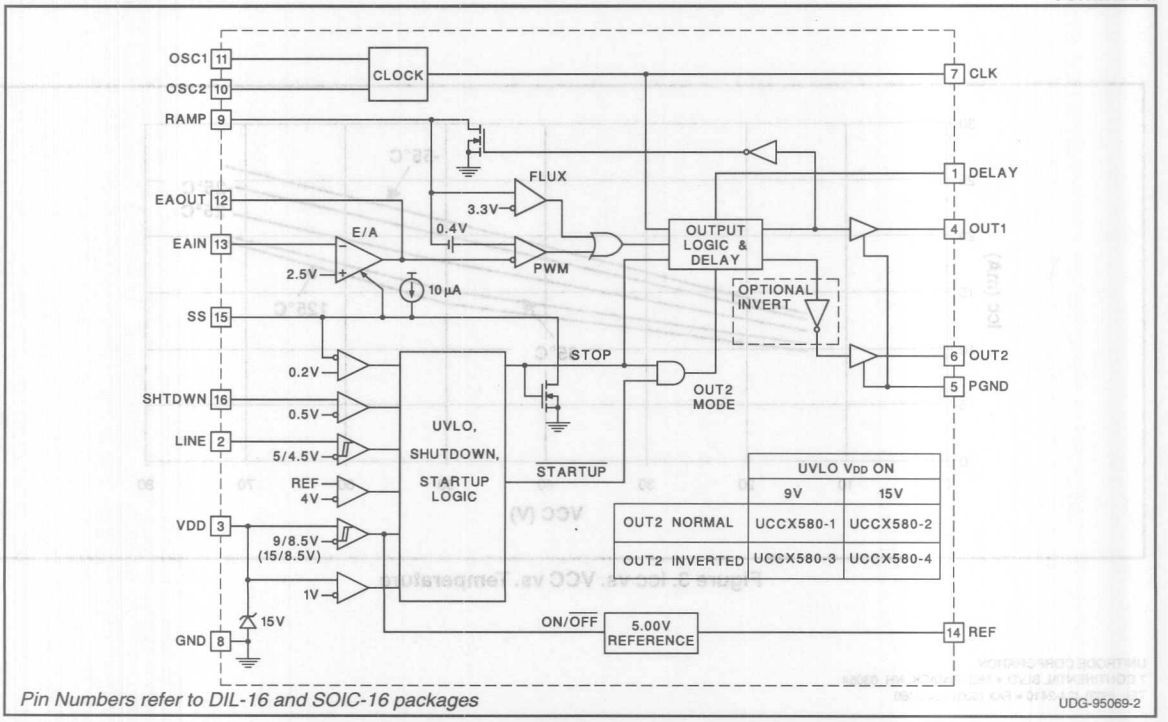
The UCC3580 family of PWM controllers is designed to implement a variety of active clamp/reset and synchronous rectifier switching converter topologies. While containing all the necessary functions for fixed frequency, high performance pulse width modulation, the additional feature of this design is the inclusion of an auxiliary switch driver which complements the main power switch, and with a programmable deadtime or delay between each transition. The active clamp/reset technique allows operation of single ended converters beyond 50% duty cycle while reducing voltage stresses on the switches, and allows a greater flux swing for the power transformer. This approach also allows a reduction in switching losses by recovering energy stored in parasitic elements such as leakage inductance and switch capacitance.

The oscillator is programmed with two resistors and a capacitor to set switching frequency and maximum duty cycle. A separate synchronized ramp provides a voltage feedforward pulse width modulation and a programmed maximum volt-second limit. The generated clock from the oscillator contains both frequency and maximum duty cycle information.

The main gate drive output (OUT1) is controlled by the pulse width modulator. The second output (OUT2) is intended to activate an auxiliary switch during the off time of the main switch, except that between each transition there is deadtime where both switches are off, programmed by a single external resistor. This design offers two options for OUT2, normal and inverted. In the -1 and -2 versions, OUT2 is normal and can be used to drive PMOS FETs. In the -3

continued

BLOCK DIAGRAM



Pin Numbers refer to DIL-16 and SOIC-16 packages

UDG-95069-2

DESCRIPTION (cont.)

and -4 versions, OUT2 is inverted and can be used to drive NMOS FETs. In all versions, both the main and auxiliary switches are held off prior to startup and when the PWM command goes to zero duty cycle. During fault conditions, OUT1 is held off while OUT2 operates at maximum duty cycle with a guaranteed off time equal to the sum of the two deadtimes.

Undervoltage lockout monitors supply voltage (VDD), the precision reference (REF), input line voltage (LINE), and the shutdown comparator (SHTDWN). If after any of these four have sensed a fault condition, recovery to full operation is initiated with a soft start. VDD thresholds, on and off, are 15V and 8.5V for the -2 and -4 versions, 9V and 8.5V for the -1 and -3 versions.

The UCC1580-x is specified for operation over the military temperature range of –55°C to 125°C. The UCC2580-x is specified from –40°C to 85°C. The UCC3580-x is specified from 0°C to 70°C. Package options include 16-pin surface mount or dual in-line, and 20-pin plastic leadless chip carrier.

Prospective users of this IC are advised that, while use in certain applications could potentially violate patent rights of one or more third parties, this product has been licensed for use in flyback power supply applications as described by U.S. Patent 5,402,329 from Technical Witts, Inc. Unitrode disclaims any other liability and suggests that users consult their own legal advisors.

ABSOLUTE MAXIMUM RATINGS

VDD 16V
I_{VDD} 25mA
LINE, RAMP ..... –0.3V to VDD + 1V
I_{LINE}, I_{RAMP} 5mA
DELAY 5.3V
I_{DELAY} ..... –5mA
I_{OUT1} (tpw < 1µs and Duty Cycle < 10%) ..... –0.6A to 1.2A
I_{OUT2} (tpw < 1µs and Duty Cycle < 10%) ..... –0.4A to 0.4A
I_{CLK} ..... –100mA to 100mA
OSC1, OSC2, SS, SHTDWN, EAIN .... –0.3V to REF + 0.3V
I_{EAOUT} ..... –5mA to 5mA
I_{REF} ..... –30mA
PGND ..... –0.2V to 0.2V
Storage Temperature ..... –65°C to +150°C
Junction Temperature ..... –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

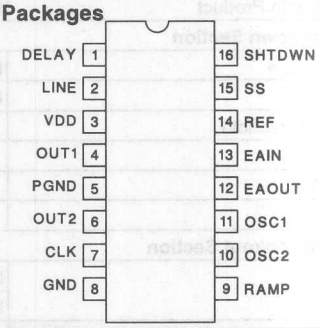
All voltages are with respect to ground unless otherwise stated. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

ORDER INFORMATION

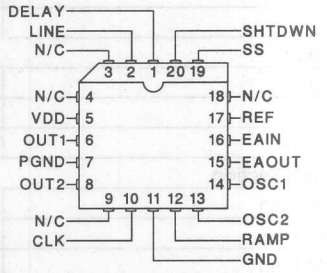
UCC☐580☐-☐
- ☐ — UVLO On Threshold/OUT2 Options
- ☐ — Package
- ☐ — Temperature Range

CONNECTION DIAGRAMS

DIL-16, SOIC-16 (Top View)
J, N, or D Packages



PLCC-20 (Top View)
Q Packages



ELECTRICAL CHARACTERISTICS

Unless otherwise stated, all specifications are over the full temperature range, VDD = 12V, R1 = 18.2k, R2 = 4.41k, C_T = 100pF, R3 = 100k, C_{OUT1} = 0, C_{OUT2} = 0. T_A = 0°C to 70°C for the UCC3580, –40°C to 85°C for the UCC2580, –55°C to 125°C for the UCC1580, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator Section					
Frequency		370	400	430	kHz
CLK Pulse Width		650	750	850	ns
CLK V_{OH}	I_{CLK} = –3mA	4.3	4.7		V
CLK V_{OL}	I_{CLK} = 3mA		0.3	0.5	V

ELECTRICAL CHARACTERISTICS (cont.) Unless otherwise stated, all specifications are over the full temperature range, VDD = 12V, R1 = 18.2k, R2 = 4.41k, C_T = 100pF, R3 = 100k, C_{OUT1} = 0, C_{OUT2} = 0. T_A = 0°C to 70°C for the UCC3580, –40°C to 85°C for the UCC2580, –55°C to 125°C for the UCC1580, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Ramp Generator Section					
Ramp V_{OL}	I_{RAMP} = 100µA		50	100	mV
Flux Comparator Vth		3.16	3.33	3.50	V
Pulse Width Modulator Section					
Minimum Duty Cycle	OUT1, EAOUT = VOL			0	%
Maximum Duty Cycle	OUT1, EAIN = 2.6V	63	66	69	%
PWM Comparator Offset		0.2	0.4	0.6	V
Error Amplifier Section					
EAIN	EAOUT = EAIN	2.46	2.5	2.54	V
I_{EAIN}	EAOUT = EAIN		150	400	nA
EAOUT, VOL	EAIN = 2.6V, I_{EAOUT} = 100µA		0.3	0.5	V
EAOUT, VOH	EAIN = 2.4V, I_{EAOUT} = –100µA	4	5	5.5	V
AVOL		70	80		dB
Gain Bandwidth Product	f = 100kHz (Note 1)	2	6		MHz
Softstart/Shutdown Section					
Start Duty Cycle	EAIN = 2.4V		0		%
SS V_{OL}	I_{SS} = 100µA		100	350	mV
SS Restart Threshold			300	500	mV
I_{SS}			–20	–35	µA
SHTDWN Vth		0.4	0.5	0.6	V
I_{SHTDWN}			50	150	nA
Undervoltage Lockout Section					
VDD On	UCC3580-2,-4	14	15	16	V
	UCC3580-1,-3	8	9	10	V
VDD Off		7.5	8.5	9.5	V
LINE On		4.7	5	5.3	V
LINE Off		4.2	4.5	4.8	V
I_{LINE}	LINE = 6V		50	150	nA
Supply Section					
VDD Clamp	I_{VDD} = 10mA	14	15	16	V
I_{VDD} Start	VDD < VDD On		160	250	µA
I_{VDD} Operating	No Load		2.5	3.5	mA
Output Drivers Section					
OUT1 V_{SAT} High	I_{OUT1} = –50mA		0.4	1.0	V
OUT1 V_{SAT} Low	I_{OUT1} =100mA		0.4	1.0	V
OUT2 V_{SAT} High	I_{OUT2} = –30mA		0.4	1.0	V
OUT2 V_{SAT} Low	I_{OUT2} = 30mA		0.4	1.0	V
OUT1 Fall Time	C_{OUT1} = 1nF		20	40	ns
OUT1 Rise Time	C_{OUT1} = 1nF		40	80	ns
OUT2 Fall Time	C_{OUT2} = 300pF		20	40	ns
Output Drivers Section (cont.)					
OUT2 Rise Time	C_{OUT2} = 300pF		20	40	ns
Delay 1 OUT2 to OUT1	R3 = 100k, C_{OUT1} = C_{OUT2} = 15pF	90	110	130	ns
Delay 2 OUT1 to OUT2	R3 = 100k, C_{OUT1} = C_{OUT2} = 15pF	140	170	200	ns

ELECTRICAL CHARACTERISTICS (cont.): Unless otherwise stated, all specifications are over the full temperature range, VDD = 12V, R1 = 18.2k, R2 = 4.41k, C_T = 100pF, R3 = 100k, C_{OUT1} = 0, C_{OUT2} = 0. T_A = 0°C to 70°C for the UCC3580, –40°C to 85°C for the UCC2580, –55°C to 125°C for the UCC1580, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Reference Section					
REF	I_{REF} = 0	4.875	5	5.125	V
Load Regulation	I_{REF} = 0mA to 1mA		1	20	mV
Line Regulation	VDD = 10V to 14V		1	20	mV

Note 1: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

CLK: Oscillator clock output pin from a low impedance CMOS driver. CLK is high during guaranteed off time. CLK can be used to synchronized up to five other UCC3580 PWMs.

DELAY: A resistor from DELAY to GND programs the nonoverlap delay between OUT1 and OUT2. The delay times, Delay1 and Delay2, are shown in Figure 1 and are as follows:

Delay 1 = 1.1pF • R3.
Delay 2 is designed to be larger than Delay 1 by a ratio shown in Figure 2.

EAIN: Inverting input to the error amplifier. The noninverting input of the error amplifier is internally set to 2.5V. EAIN is used for feedback and loop compensation.

EAOUT: Output of the error amplifier and input to the PWM comparator. Loop compensation components connect from EAOUT to EAIN.

GND: Signal Ground.

LINE: Hysteretic comparator input. Thresholds are 5.0V and 4.5V. Used to sense input line voltage and turn off OUT1 when the line is low.

OSC1 & OSC2: Oscillator programming pins. A resistor connects each pin to a timing capacitor. The resistor connected to OSC1 sets maximum on time. The resistor connected to OSC2 controls guaranteed off time. The combined total sets frequency with the timing capacitor. Frequency and maximum duty cycle are approximately given by:

$$\text{Frequency} = \frac{1}{(R1 + 1.25 \bullet R2) \bullet C_T}$$

$$\text{Maximum Duty Cycle} = \frac{R1}{R1 + 1.25 \bullet R2}$$

Maximum Duty Cycle for OUT1 will be slightly less due to Delay1 which is programmed by R3.

OUT1: Gate drive output for the main switch capable of sourcing up to 0.5A and sinking 1A.

OUT2: Gate drive output for the auxiliary switch with ±0.3A drive current capability.

PGND: Ground connection for the gate drivers. Connect PGND to GND at a single point so that no high frequency components of the output switching currents are in the ground plane on the circuit board.

RAMP: A resistor (R4) from RAMP to the input voltage and a capacitor (CR) from RAMP to GND programs the feedforward ramp signal. RAMP is discharged to GND when CLK is high and allowed to charge when CLK is low. RAMP is the line feedforward sawtooth signal for the PWM comparator. Assuming the input voltage is much greater than 3.3V, the ramp is very linear. A flux comparator compares the ramp signal to 3.3V to limit the maximum allowable volt-second product:

Volt-Second Product Clamp = 3.3 • R4 • CR.

REF: Precision 5.0V reference pin. REF can supply up to 5mA to external circuits. REF is off until VDD exceeds 9V (-1 and -3 versions) or activates the 15V clamp (-2 and -4 versions) and turns off again when VDD droops below 8.5V. Bypass REF to GND with a 1µF capacitor.

SHTDWN: Comparator input to stop the chip. The threshold is 0.5V. When the chip is stopped, OUT1 is low and OUT2 continues to oscillate with guaranteed off time equal to two non-overlap delay times.

SS: A capacitor from SS to ground programs the soft start time. During soft start, EAOUT follows the amplitude of SS's slowly increasing waveform until regulation is achieved.

VDD: Chip power supply pin. VDD should be bypassed to PGND. The -1 and -3 versions require VDD to exceed 9V to start and remain above 8.5V to continue running. A shunt clamp from VDD to GND limits the supply voltage to 15V. The -2 and -4 versions do not start until the shunt clamp threshold is reached and operation continues as long as VDD is greater than 8.5V.

APPLICATION INFORMATION

UVLO and Startup

For self biased off-line applications, -2 and -4 versions (UVLO on and off thresholds of 15V and 8.5V typical) are recommended. For all other applications, -1 and -3 versions provide the lower on threshold of 9V. The IC requires a low startup current of only 160µA when VDD is under the UVLO threshold, enabling use of a large trickle charge resistor (with corresponding low power dissipation) from the input voltage. VDD has an internal clamp at 15V which can sink up to 10mA. Measures should be taken not to exceed this current. For -2 and -4 versions, this clamp must be activated as an indication of reaching the UVLO on threshold. The internal reference (REF) is brought up when the UVLO on threshold is crossed. The startup logic ensures that LINE and REF are above and SHTDWN is below their respective thresholds before outputs are asserted. LINE input is useful for monitoring actual input voltage and shutting off the IC if it falls below a programmed value. A resistive divider should be used to connect the input voltage to the LINE input. This feature can protect the power supply from excessive currents at low line voltages.

The soft start pin provides an effective means to start the IC in a controlled manner. An internal current of 20µA begins charging a capacitor connected to SS once the startup conditions listed above have been met. The voltage on SS effectively controls maximum duty cycle on OUT1 during the charging period. OUT2 is also controlled during this period (see Figure 1). Negation of any of the startup conditions causes SS to be immediately discharged. Internal circuitry ensures full discharge of SS (to 0.3V) before allowing charging to begin again, provided all the startup conditions are again met.

Oscillator

Simplified oscillator block diagram and waveforms are shown in Figure 3. OSC1 and OSC2 pins are used to program the frequency and maximum duty cycle. Capacitor CT is alternately charged through R1 and discharged through R2 between levels of 1V and 3.5V. The charging and discharging equations for CT are given by

$$Vc(charge) = REF - 4.0 \bullet e^{-t/\tau_1}$$

$$Vc(discharge) = 3.5 \bullet e^{-t/\tau_2}$$

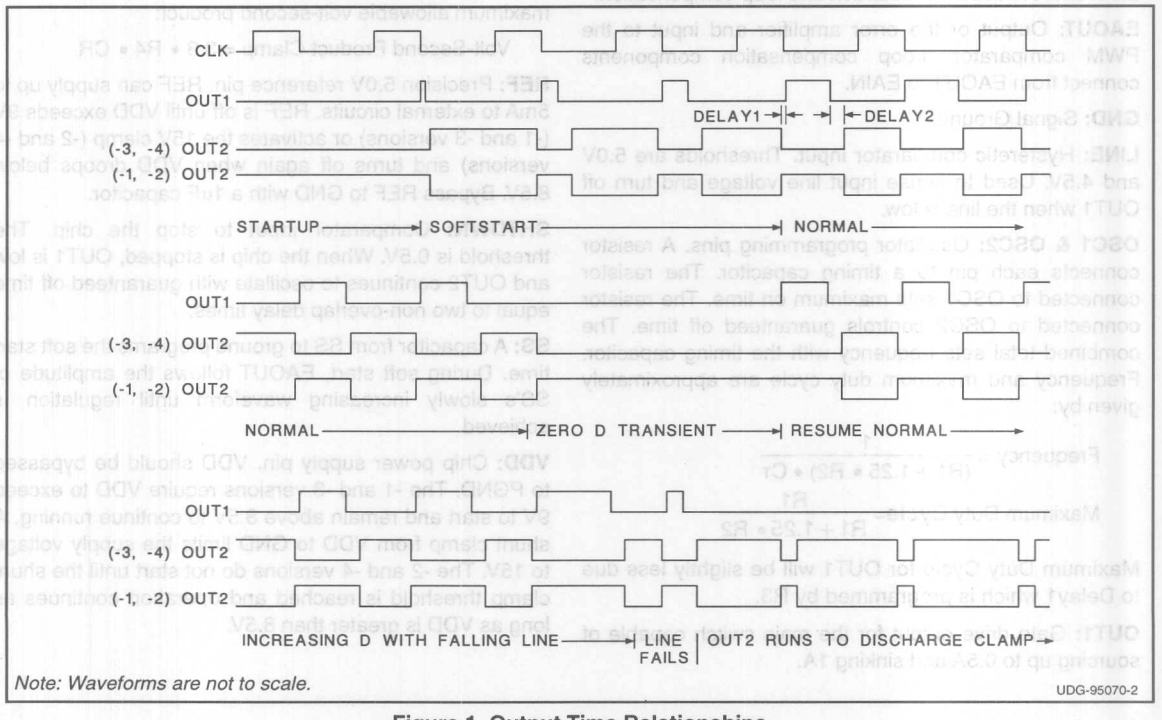


Figure 1. Output Time Relationships

APPLICATION INFORMATION (cont.)

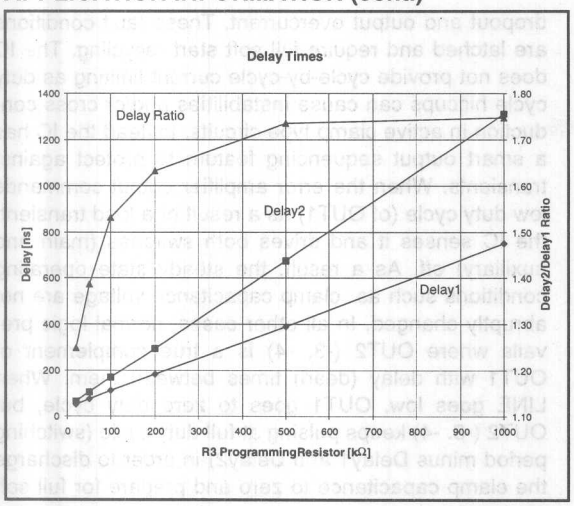


Figure 2. Delay Times

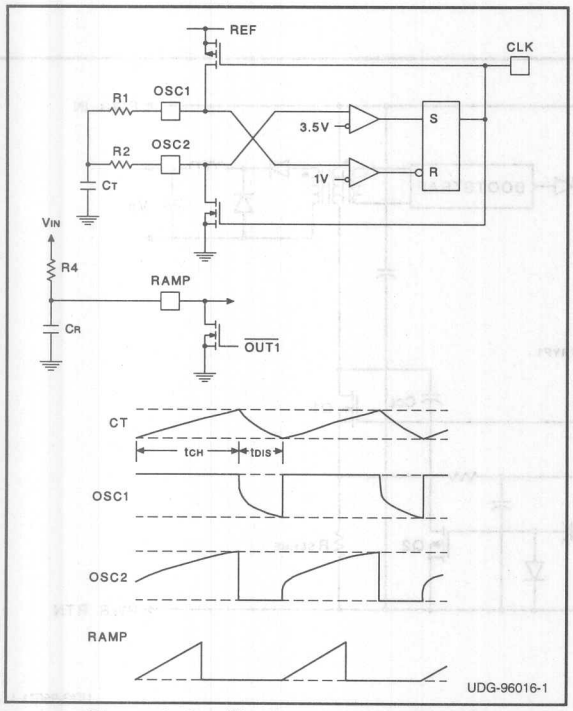


Figure 3. Oscillator and Ramp Circuits

where $\tau_1 = R1 \bullet CT$ and $\tau_2 = R2 \bullet CT$. The charge time and discharge time are given by

$t_{CH} = R1 \bullet C_T$ and $t_{DIS} = 1.25 \bullet R2 \bullet C_T$

The CLK output is high during the discharge period. It blanks the output to limit the maximum duty cycle of OUT1. The frequency and maximum duty cycle are given by

$$\text{Frequency} = \frac{1}{(R1 + 1.25 \bullet R2) \bullet C_T}$$

$$\text{Maximum Duty Cycle} = \frac{R1}{R1 + 1.25 \bullet R2}$$

Maximum Duty Cycle for OUT1 will be slightly less due to Delay1 which is programmed by R3.

Voltage Feedforward and Volt-Second Clamp

UCC3580 has a provision for input voltage feedforward. As shown in Figure 3, the ramp slope is made proportional to input line voltage by converting it into a charging current for CR. This provides a first order cancellation of the effects of line voltage changes on converter performance. The maximum volt-second clamp is provided to protect against transient saturation of the transformer core. It terminates the OUT1 pulse when the RAMP voltage exceeds 3.3V. If the feedforward feature is not used, the ramp can be generated by tying R4 to REF. However, the linearity of ramp suffers and in this case the maximum volt-second clamp is no longer available.

Output Configurations

The UCC3580 family of ICs is designed to provide control functions for single ended active clamp circuits. For different implementations of the active clamp approach, different drive waveforms for the two switches (main and auxiliary) are required. The -3 and -4 versions of the IC supply complementary non-overlapping waveforms (OUT1 and OUT2) with programmable delay which can be used to drive the main and auxiliary switches. Most active clamp configurations will require one of these outputs to be transformer coupled to drive a floating switch (e.g. Figure 5). The -1 and -2 versions have the phase of OUT2 inverted to give overlapping waveforms. This configuration is suitable for capacity coupled driving of a ground referenced p-channel auxiliary switch with the OUT2 drive while OUT1 is directly driving an n-channel main switch (e.g. Figure 4).

The programmable delay can be judiciously used to get zero voltage turn-on of both the main and auxiliary switches in the active clamp circuits. For the UCC3580, a single pin is used to program the delays between OUT1 and OUT2 on both sets of edges. Figure 1 shows the relationships between the outputs. Figure 2 gives the ratio between the two delays. During the transition from main to auxiliary switch, the delay is not

APPLICATION INFORMATION (cont.)

very critical for ZVS turn-on. For the first half of OUT1 off-time, the body diode of the auxiliary switch conducts and OUT2 can be turned on any time. The transition from auxiliary to main switch is more critical. Energy stored in the parasitic inductance(s) at the end of the OUT2 pulse is used to discharge the parasitic capacitance across the main switch during the delay time. The delay (Delay 1) should be optimally programmed at 1/4 the resonant period determined by parasitic capacitance and the resonant inductor (transformer leakage and/or magnetizing inductances, depending on the topology). However, depending on other circuit parasitics, the resonant behavior can change, and in some cases, ZVS turn-on may not be obtainable. It can be shown that the optimum delay time is independent of operating conditions for a specific circuit and should be determined specifically for each circuit.

Output Behavior During Fault Modes

The UCC3580 family is designed to protect power converter components against faults such as input line dropout and output overcurrent. These fault conditions are latched and require full soft start recycling. The IC does not provide cycle-by-cycle current limiting as duty cycle hiccups can cause instabilities and/or cross conduction in active clamp type circuits. Instead the IC has a smart output sequencing feature to protect against transients. When the error amplifier output commands low duty cycle (of OUT1) as a result of a load transient, the IC senses it and drives both switches (main and auxiliary) off. As a result, the steady state operating conditions such as clamp capacitance voltage are not abruptly changed. In all other cases, normal logic prevails where OUT2 (-3, -4) is a true complement of OUT1 with delay (dead) times between them. When LINE goes low, OUT1 goes to zero duty cycle, but OUT2 (-3. -4) keeps pulsing at full duty cycle (switching period minus Delay1 and Delay2) in order to discharge the clamp capacitance to zero and prepare for full soft start cycle.

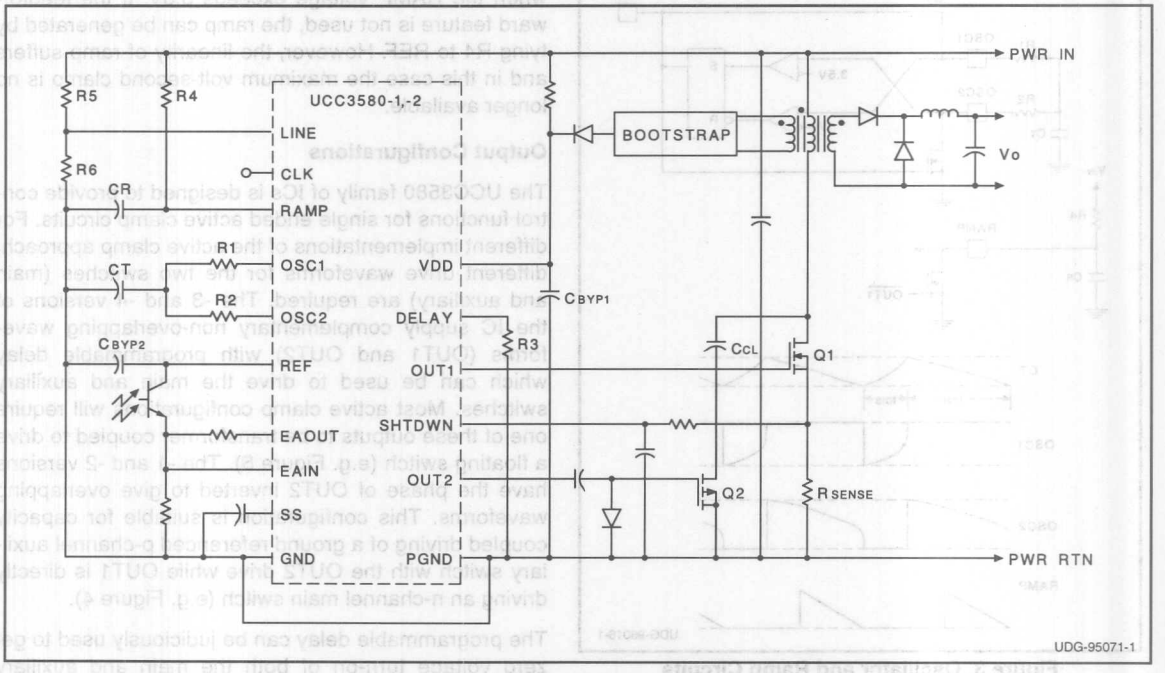


Figure 4. Active Clamp Forward Converter

APPLICATION INFORMATION (cont.)

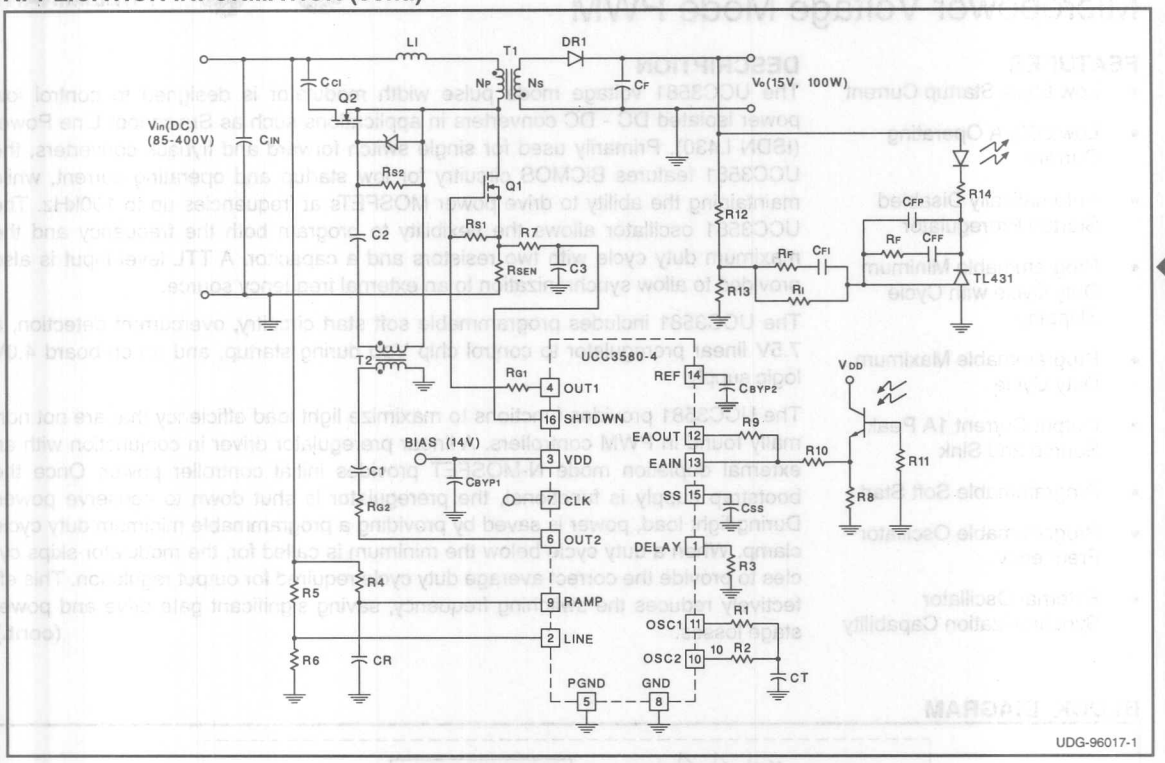


Figure 5. Off-line Active Clamp Flyback Converter

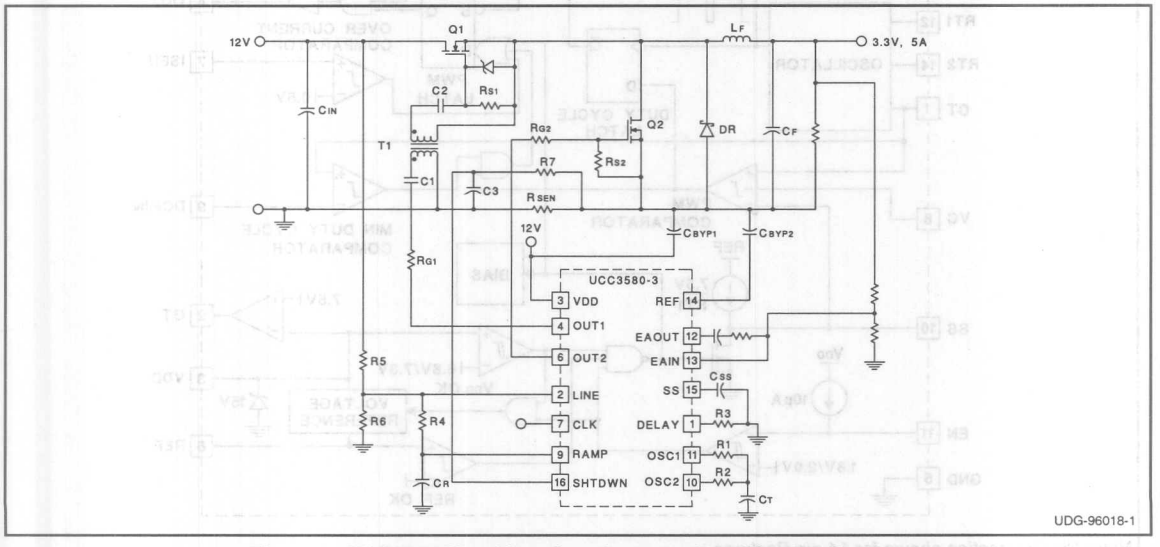


Figure 6. UCC3580 Used in a Synchronous Rectifier Application

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

Micropower Voltage Mode PWM

PRELIMINARY

FEATURES

- Low 85µA Startup Current
- Low 300µA Operating Current
- Automatically Disabled Startup Preregulator
- Programmable Minimum Duty Cycle with Cycle Skipping
- Programmable Maximum Duty Cycle
- Output Current 1A Peak Source and Sink
- Programmable Soft Start
- Programmable Oscillator Frequency
- External Oscillator Synchronization Capability

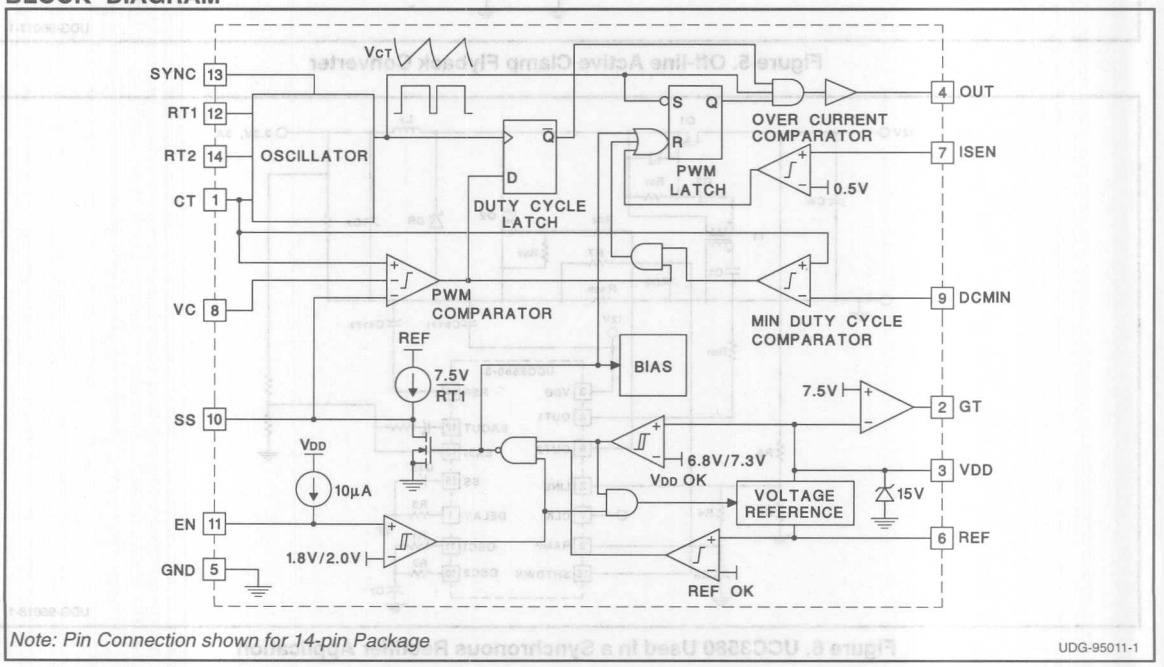
DESCRIPTION

The UCC3581 voltage mode pulse width modulator is designed to control low power isolated DC - DC converters in applications such as Subscriber Line Power (ISDN I.430). Primarily used for single switch forward and flyback converters, the UCC3581 features BiCMOS circuitry for low startup and operating current, while maintaining the ability to drive power MOSFETs at frequencies up to 100kHz. The UCC3581 oscillator allows the flexibility to program both the frequency and the maximum duty cycle with two resistors and a capacitor. A TTL level input is also provided to allow synchronization to an external frequency source.

The UCC3581 includes programmable soft start circuitry, overcurrent detection, a 7.5V linear preregulator to control chip V_{DD} during startup, and an on-board 4.0V logic supply.

The UCC3581 provides functions to maximize light load efficiency that are not normally found in PWM controllers. A linear preregulator driver in conjunction with an external depletion mode N-MOSFET provides initial controller power. Once the bootstrap supply is functional, the preregulator is shut down to conserve power. During light load, power is saved by providing a programmable minimum duty cycle clamp. When a duty cycle below the minimum is called for, the modulator skips cycles to provide the correct average duty cycle required for output regulation. This effectively reduces the switching frequency, saving significant gate drive and power stage losses. **(cont.)**

BLOCK DIAGRAM



Note: Pin Connection shown for 14-pin Package

UDG-95011-1

DESCRIPTION (cont.)

The UCC3581 family is available in 14-pin plastic and ceramic dual-in-line packages, in a 14-pin narrow body small outline IC package (SOIC), and in 20-pin plastic and ceramic leadless chip carriers (PLCC and LCC). The UCC1581 is specified for operation from –55°C to +125°C, the UCC2581 is specified for operation from –40°C to +85°C, and the UCC3581 is specified for operation from 0°C to +70°C.

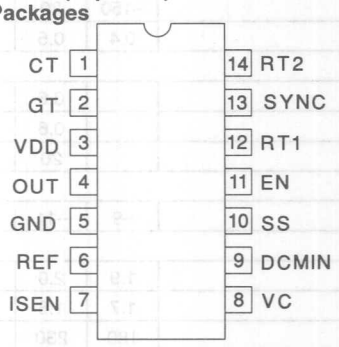
ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($I_{DD} \leq 10mA$) 15V
Supply Current 30mA
V_{REF} Current ..... –10mA
OUT Current ..... ±1A
Analog Inputs
EN ..... –0.3V to (VDD + 0.3V)
VC, ISEN, SYNC, DCMIN ..... –0.3V to (V_{REF} + 0.3V)
Power Dissipation at T_D = 25°C
(N, J, Q, L Package) 1W
(D Package) 0.65W
Storage Temperature ..... –65°C to +150°C
Junction Temperature ..... –55C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

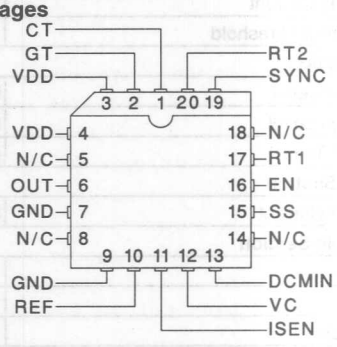
Unless otherwise specified, all voltages are with respect to Ground. Currents positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAMS

DIL-14, SOIC-14 (Top View)
N or J, D Packages



PLCC-20, LCC-20 (Top View)
Q, L Packages



ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = –55°C to 125°C for UCC1581, –40°C to 85°C for UCC2581, and 0°C to 70°C for UCC3581. VDD = 10V, 0.1µF capacitor from VDD to GND, 1.0µF capacitor from REF to GND, RT1 = 680kΩ, RT2 = 12kΩ, CT = 750pF, T_A = TJ.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Reference Section					
Output Voltage	I = –0.2mA	3.94	4.0	4.06	V
Load Regulation	–5.0mA < I < –0.2mA		10	30	mV
Undervoltage Lockout Section					
Start Threshold		6.7	7.3	7.9	V
Minimum Operating Voltage After Start		6.2	6.8	7.4	V
Hysteresis		0.2	0.5	0.8	V
Linear Preregulator Section					
Regulated VDD Voltage		7.0	7.5	8.0	V
Regulated VDD to UVLO Delta		100	230	360	mV
VDD Override Threshold				8.2	V

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = –55°C to 125°C for UCC1581, –40°C to 85°C for UCC2581, and 0°C to 70°C for UCC3581. VDD = 10V, 0.1µF capacitor from VDD to GND, 1.0µF capacitor from REF to GND, RT1 = 680kΩ, RT2 = 12kΩ, CT = 750pF, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator Section					
Frequency	25°C	18.6	19.7	20.8	kHz
Temperature Stability	(Note 1)		3.0		%
CT Peak Voltage	(Note 1)		2.5		V
CT Valley Voltage	(Note 1)		1.0		V
SYNC VIH		1.9	2.1	2.3	V
SYNC VIL	(Note 1)		1.8		V
PWM SECTION					
Maximum Duty Cycle		80	83	86	%
Minimum Duty Cycle	(VC < 1.0V) DCMIN = 0V			0	%
	(VC > 1.0V at start of cycle) DCMIN = 1.18V	8	10	12	%
Input Bias Current	(DC minimum)	–150	20	150	nA
	(VC minimum)	–150	20	150	nA
Current Sense Section					
Input Bias Current		–150	20	150	nA
Overcurrent Threshold		0.4	0.5	0.6	V
Output Section					
OUT Low Level	I = 100mA		0.6	1.2	V
OUT High Level	I = –100mA, VDD - OUT		0.6	1.2	V
Rise/Fall Time	(Note 1)		20	100	ns
Soft start Section					
Soft start Current	SS = 2V	–9	–11	–13	µA
Chip Enable Section					
VIH		1.9	2.0	2.1	V
VIL		1.7	1.8	1.9	V
Hysteresis		180	230	280	mV
Source Current		5	10	15	µA
Overall Section					
Start-Up Current	VDD < Start Threshold		85	120	µA
Operating Supply Current	VC = 0V		300	600	µA
VDD Zener Shunt Voltage	I_{CC} = 10mA	13.5	15	16.5	V
I_{DD} Stand-by Shunt Voltage	EN = 0V		100	150	µA

Note 1: Guaranteed by design. Not 100% tested in production

PIN DESCRIPTIONS

CT: Oscillator timing capacitor pin. Minimum value is 100pF.

DCMIN: Input for programming minimum duty cycle where pulse skipping begins. This pin can be grounded to disable minimum duty cycle feature and pulse skipping.

EN: Enable input. This pin has an internal 10µA pull-up. A logic low input inhibits the PWM output and causes the soft start capacitor to be discharged.

GND: Circuit ground.

GT: Pin for controlling the gate of an external depletion mode N-MOSFET for the startup supply. The external N-MOSFET regulates VDD to 7.5V until the bootstrap supply comes up, then GT goes low.

ISEN: Input for overcurrent comparator. This function can be used for pulse-by-pulse current limiting. The threshold is 0.5V nominal.

PIN DESCRIPTIONS (cont.)

OUT: Gate drive output to external N-MOSFET.

REF: 4.0V reference output. A minimum value bypass capacitor of 1.0µF is required for stability.

RT1: Resistor pin to program oscillator charging current. The oscillator charging current is $9.2 \bullet \frac{2.0V}{R_{RT1}}$.

See Application Diagram Figure 1.

The current in RT1 is $\frac{2.0V}{R_{RT1}}$.

The value of R_{RT1} should be between 220k and 1MΩ.

RT2: Resistor pin to program oscillator discharge time. The minimum value of R_{RT2} is 10kΩ. See Application Diagram Figure 1.

SS: Soft start capacitor pin. The charging current out of SS is 3.75X the current in R_{RT1}.

SYNC: Oscillator synchronization pin. Rising edge triggered CMOS/TTL compatible input with a 2.1V threshold. SYNC should be grounded if not used. The minimum pulse width of the SYNC signal is 100ns.

VC: Control voltage input to PWM comparator. The nominal control range of VC is 1.0V to 2.5V.

VDD: Chip input power with an 15V internal clamp. VDD is regulated by startup FET to 7.5V until the bootstrap voltage comes up. VDD should be bypassed at the chip with a 0.1µF minimum capacitor.

APPLICATION INFORMATION

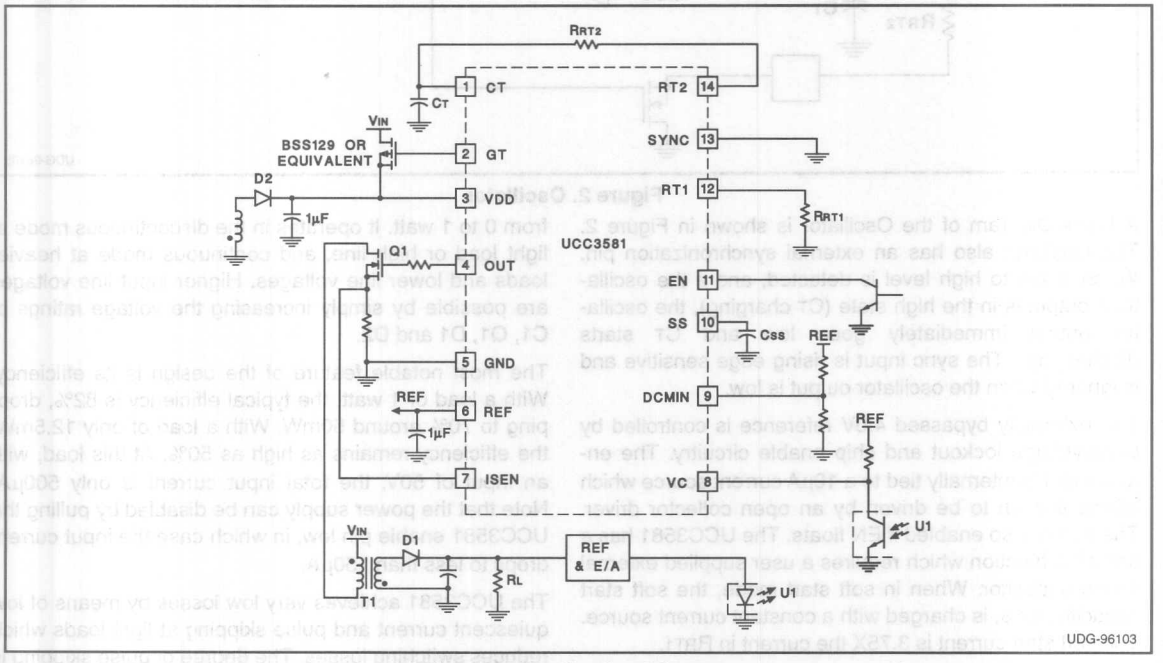


Figure 1. Application Diagram

The UCC3581's oscillator allows the user the flexibility to program the frequency and the duty cycle by adjusting two resistors and a capacitor. Application Diagram Figure 1 shows these components as R_{RT1}, R_{RT2}, and C_T. R_{RT1} programs the timing capacitor charging current which results in a linear ramp charging C_T. Discharge of C_T is accomplished though R_{RT2} which results in a standard RC discharge waveform. The oscillator on-time (C_T charging) is calculated by the formula $t_{ON} = 0.082 \bullet R_{RT1} \bullet C_T$.

The off-time (C_T discharging) is calculated by the formula $t_{OFF} = 0.95 \bullet R_{RT2} \bullet C_T$.

Resistor R_{RT1} programs the charging current. The current in R_{RT1} is

$$\frac{2.0V}{R_{RT1}}.$$

CT charging current is 9.2 times the current in R_{RT1}. R_{RT1} can range from 220kΩ to 1MΩ. Minimum capacitor size is 100pF, and minimum R_{RT2} size is 10k.

APPLICATION INFORMATION (cont.)

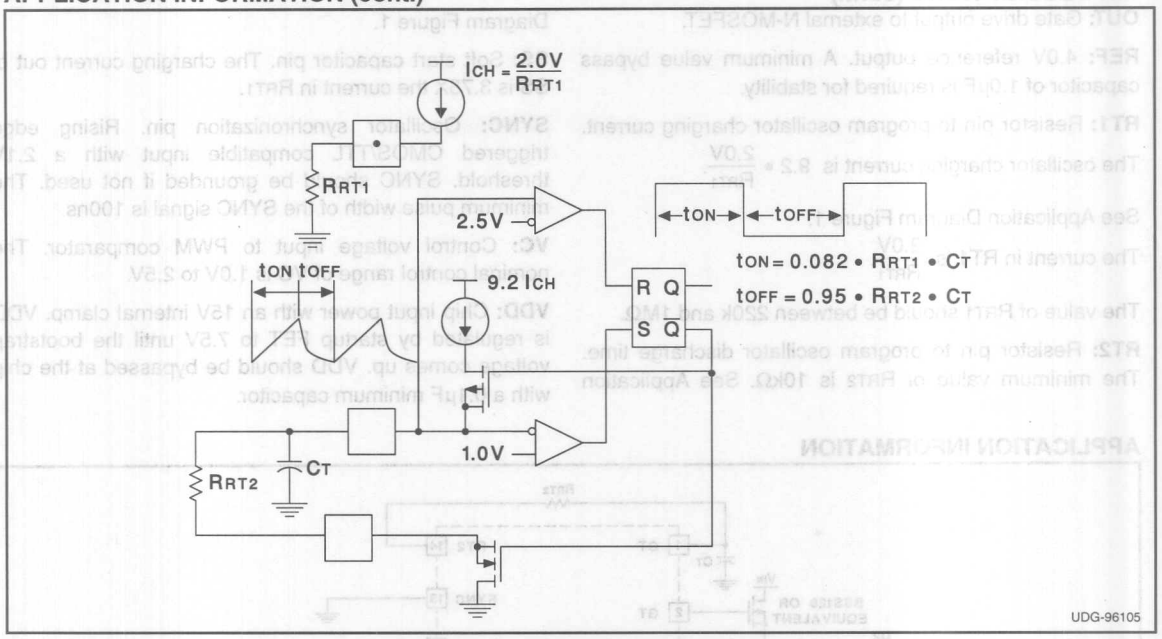


Figure 2. Oscillator

A Block Diagram of the Oscillator is shown in Figure 2. The oscillator also has an external synchronization pin. When a low to high level is detected, and if the oscillator's output is in the high state (C_T charging), the oscillator output immediately goes low and C_T starts discharging. The sync input is rising edge sensitive and is ignored when the oscillator output is low.

The externally bypassed 4.0V reference is controlled by undervoltage lockout and chip enable circuitry. The enable input is internally tied to a 10µA current source which allows the pin to be driven by an open collector driver. The part is also enabled if EN floats. The UCC3581 has a soft start function which requires a user supplied external timing capacitor. When in soft start mode, the soft start capacitor, C_{SS}, is charged with a constant current source. The soft start current is 3.75X the current in R_{RT1}.

There is an on-chip control amplifier, which when driving the gate of an external depletion mode N-MOSFET, acts as a 7.5V linear preregulator supplying VDD directly from the primary input power line. The preregulator may subsequently be fully disabled by a tertiary bootstrap winding providing a minimum of 8.2V to the VDD pin.

The circuit shown in Figure 3 illustrates the use of the UCC3581 in a micropower application. The isolated 5V flyback power supply uses a minimum of parts and operates over an 8:1 input voltage range (15VDC to 120VDC) while delivering a regulated 5V output with a load swing from 0 to 1 watt. It operates in the discontinuous mode at light load or high line, and continuous mode at heavier loads and lower line voltages. Higher input line voltages are possible by simply increasing the voltage ratings of C1, Q1, D1 and D2.

The most notable feature of the design is its efficiency. With a load of 1 watt, the typical efficiency is 82%, dropping to 70% around 50mW. With a load of only 12.5mW, the efficiency remains as high as 50%. At this load, with an input of 50V, the total input current is only 500µA. Note that the power supply can be disabled by pulling the UCC3581 enable pin low, in which case the input current drops to less than 150µA.

The UCC3581 achieves very low losses by means of low quiescent current and pulse skipping at light loads which reduces switching losses. The degree of pulse skipping is controlled by programming the minimum duty cycle. In this example, the frequency is 35kHz at maximum load and drops to <2kHz at 12.5mW load (minimum pulse width of around 6µsec, or 21% duty cycle at 35kHz). Another way losses are reduced is operating with a VDD of around 10V rather than the more common 12V to 16V. At such light primary currents, the MOSFET remains in full saturation with a gate drive voltage well below 10V.

Gate drive losses are minimized by choosing a MOSFET with low total gate charge, in this case only 8nC maximum. By choosing a large gate drive resistor, EMI is

APPLICATION INFORMATION (cont.)

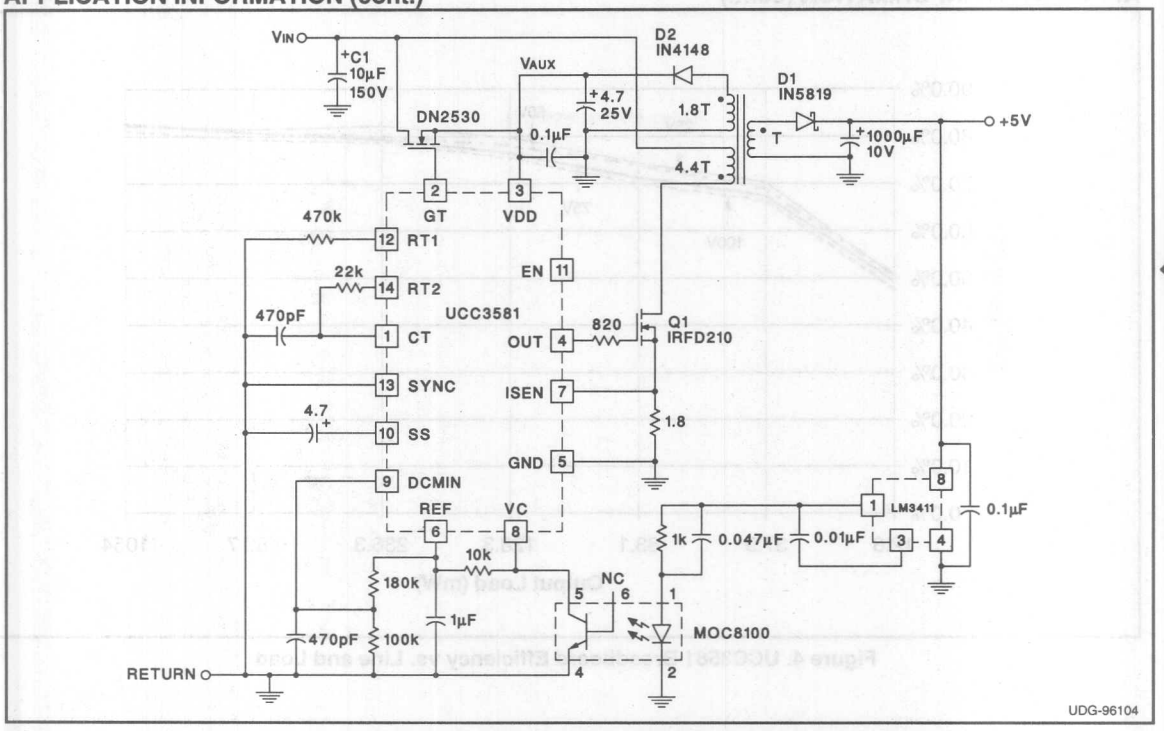


Figure 3. Micropower Power Supply with 50% Efficiency at 12.5mW Load

minimized by reducing peak currents. Due to pulse skipping, switching times are less critical for efficiency at light load.

The shunt regulator (LM3411) and optocoupler (MOC8100) are also key to the efficiency at such light loads, and were chosen for their low operating current. The LM3411 has a quiescent current of only 150µA maximum (compared to 1mA for the more common TL431). In addition, because it is not a three terminal device, the LM3411's quiescent current does not flow in the optocoupler LED. Since this bias current is not in the feedback control path, a higher value pull-up resistor can be used on the optocoupler output transistor, further reducing losses.

A rather large soft start capacitor was chosen to give a startup time of several hundred milliseconds, reducing the input surge current while the output is coming up.

Note that for stability, the UCC3581 V_{REF} bypass capacitor needs to be at least 1µF. The V_{DD} supply also needs some capacitance to hold it up between pulses at light load and high line, where the frequency may drop to less than 1kHz due to pulse skipping. Otherwise it may drop low enough for the startup MOSFET to be biased on, lowering efficiency.

If the sync input is used, it should not be left in a high impedance state where noise could cause false triggering. If unused, it should be grounded.

The transformer was designed with a standard Magnetics RM8 ferrite core using P material, gapped for an A_L of 1600mH/1000Turn^2. The primary consists of 44 turns, while the 5V secondary has 10 turns and the bootstrap winding 18 turns. For simplicity, all the windings can be #28 AWG. A two section bobbin was used to provide high primary to secondary isolation. A much smaller design, with reduced isolation, could have been done for this low power level.

APPLICATION INFORMATION (cont.)

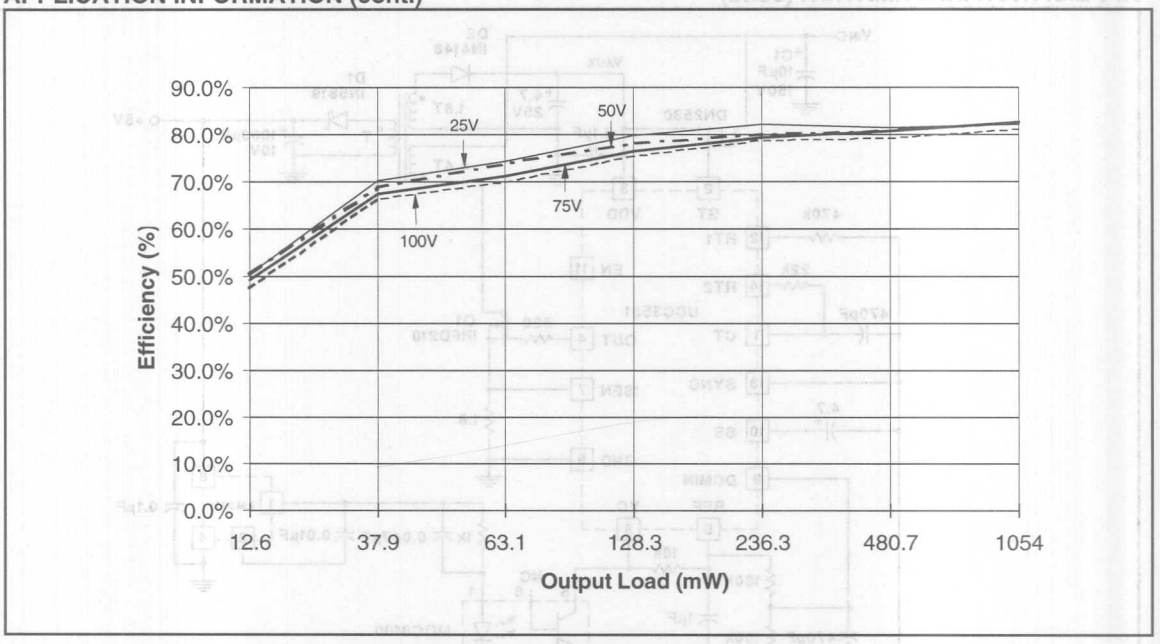


Figure 4. UCC3581 Breadboard Efficiency vs. Line and Load

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

High Efficiency Synchronous, Step Down Controller

PRELIMINARY

FEATURES

- BiCMOS Voltage Mode PWM Controller
- 4.5V to 7V Input Voltage Range
- Output Voltages as low as 1.25V
- Sleep Mode (Ic = 15µA typ)
- Lossless Short Circuit Current Limiting
- >90% Typical Efficiency
- 0% to 100% Duty Cycle Range
- 8-Pin Surface Mount Package

DESCRIPTION

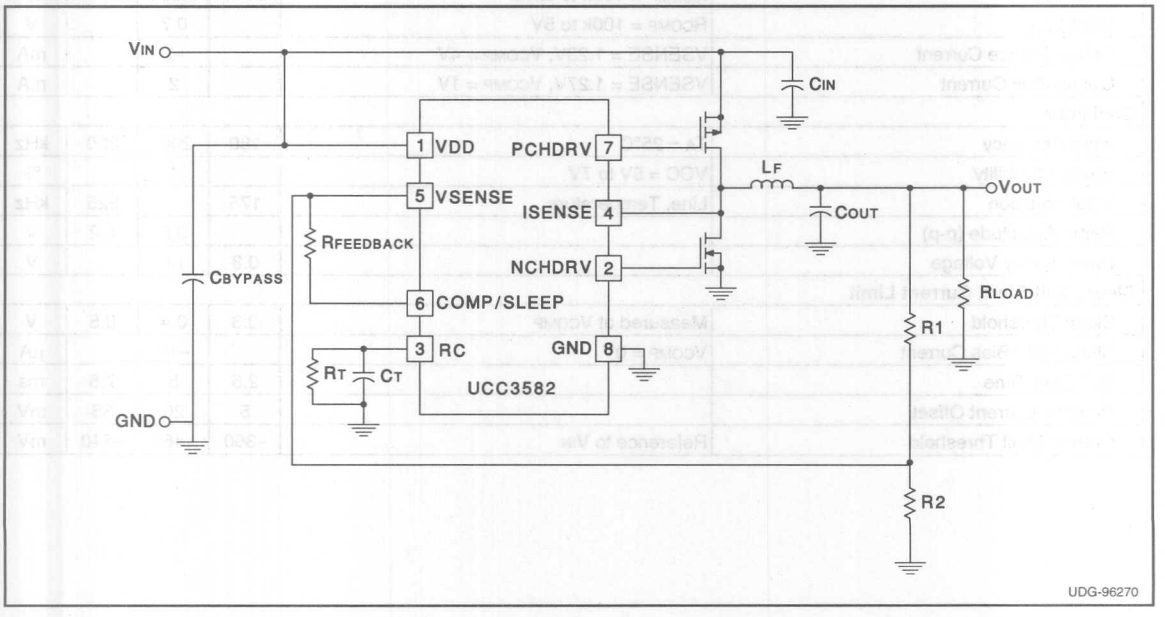
The UCC3582 family of synchronous step-down (Buck) regulators provides accurate high efficiency power conversion from input voltages ranging from 4.5V to 7V volts. Using few external components, the UCC3582 in an 8-pin surface mount package is especially suited for low voltage, battery powered applications where cost, small size and high efficiency are critical. A high level of integration and novel design allow this 8-pin controller to provide a complete control solution. High efficiency is obtained through the use of synchronous rectification.

Synchronous regulators replace the catch diode in the standard buck converter with a low RDS(on) N-channel MOSFET switch allowing for significant efficiency improvements. The external high side switch is a P-channel MOSFET, negating the need for a charge pump and a complex high side driver. The UCC3582 provides the out of phase and non-overlapping gate drive signals needed to drive the external MOSFETs. The P-channel MOSFET voltage drop during conduction is sensed for lossless short circuit current limiting.

100% duty cycle operation allows the UCC3582 to operate as a low dropout regulator in the event of a low battery condition. A low power sleep mode can be commanded by externally forcing the COMP pin below 0.5V. Quiescent supply current in sleep mode is typically less than 15µA. The internal 5ms soft start provides for controlled ramp up of the output voltage with minimal overshoot. The undervoltage lockout threshold is set at 4.5V with 200mV of hysteresis.

Available packages include the 8-pin SOIC and Plastic and Ceramic Dips.

TYPICAL APPLICATION



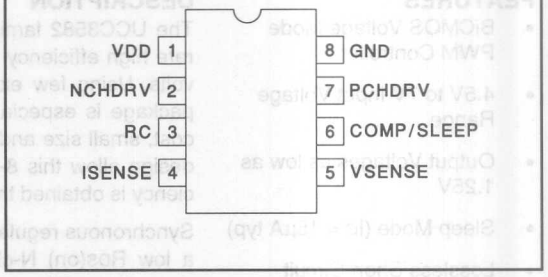
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (VDD) 7V
Output Drivers (PCHDRV, NCHDRV) Currents
Continuous . . . . . ±0.25A
Peak. . . . . ±500mA
Inputs (VSENSE,COMP/SLEEP, RC, ISENSE) . . –0.3V to 7V
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature . . . . . +300°C

All voltages with respect to GND. Currents are positive into, negative out of the specified terminal. Pulsed is defined as a less than 10% duty cycle with a maximum duration of 500ns. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

DIL-8, SOIC-8
D, N and J Packages



ELECTRICAL CHARACTERISTICS:

Unless otherwise specified, VCC = 5V, CT = 470pF, RT = 10k, TA = -55°C to 125°C for UCC1582, –25°C to 85°C for UCC2582, 0°C to 70°C for UCC3582, TA = TJ.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Overall					
Supply Current, Sleep	VCOMP = 0V		14	25	µA
Supply Current, Operating			1.5	3	mA
VCC Turn-on Threshold			4.5	4.75	V
VCC Turn-off Threshold		4	4.3		V
Error Amplifier					
Input Voltage		1.23	1.25	1.27	V
VSENSE Bias Current		–500	25	500	nA
Open Loop Gain	VCOMP = 1V to 3V	70	100		dB
VOUT High	RCOMP = 100k to GND		4.3		V
VOUT Low	RCOMP = 100k to 5V		0.7		V
Output Source Current	VSENSE = 1.23V, VCOMP = 4V		–2		mA
Output Sink Current	VSENSE = 1.27V, VCOMP = 1V		2		mA
Oscillator					
Initial Accuracy	TA = 25°C	180	200	220	kHz
Voltage Stability	VCC = 5V to 7V		1		%
Total Variation	Line, Temperature	175		225	kHz
Ramp Amplitude (p-p)			3.6	4.2	V
Ramp Valley Voltage		0.8	1.5		V
Sleep, Soft Start, Current Limit					
Sleep Threshold	Measured at VCOMP	0.3	0.4	0.5	V
Sleep Input Bias Current	VCOMP = 0V		–10		µA
Soft Start Time		2.5	5	7.5	ms
Reverse Current Offset		5	20	35	mV
Current Limit Threshold	Reference to VIN	–360	–450	–540	mV

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, VCC = 5V, CT = 470pF, RT = 10k, TA = -55°C to 125°C for UCC1582, –25°C to 85°C for UCC2582, 0°C to 70°C for UCC3582, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
N-Channel and P-Channel Driver Outputs					
Output High Voltage	I_{OUT} = –50mA	4.0	4.5		V
Output Low Voltage	I_{OUT} = 50mA		0.5		V
Output Resistance	I_{OUT} = 100mA		15		Ω
Output Low (UVLO)	I_{OUT} = 10mA, VCC = 0V		0.9		V
Output Rise Time	C_{OUT} = 1nF		30		ns
Output Fall Time	C_{OUT} = 1nF		30		ns
Output Dead Time	C_{OUT} = 1nF		200		ns
Overcurrent Blank Time			300		ns
Reverse Current Blank Time			300		ns

PIN DESCRIPTIONS

COMP/SLEEP: This is the output of the voltage amplifier. The voltage at this output is inverted internally and connected to the non-inverting input of the PWM comparator. A lead-lag network around the voltage amplifier compensates for the two pole LC filter characteristic inherent to voltage mode control, and is required in order to optimize the dynamic performance of the voltage mode control loop. Sleep mode is invoked if COMP is pulled and held below 0.5V which can be accomplished by an external gate or transistor. Sleep mode supply current is 15µA typical.

GND: All voltages are measured with respect to this pin. All bypass and timing capacitors connected to GND should have leads as short and direct as possible.

ISENSE: This input is connected to the junction between the two external power MOSFET transistors. The voltage drop across the upper P-channel device is monitored by ISENSE during conduction, and forms the current limit signal. When this drop exceeds 450mV the overcurrent comparator and logic sets the PWM latch and terminates the output pulse. The controller stops switching and goes through a soft start sequence. This prevents excess power dissipation in the NMOSFET during a short circuit. The reverse current comparator senses the drop across the lower N-channel MOSFET and disables the drive signal if a small positive voltage is present. A positive voltage is indicative of either P-channel conduction or reverse inductor current. To disable the overcurrent comparator, connect ISENSE to VDD.

PCHDRV, NCHDRV: The output drivers are rated for 0.5A peak currents. The PWM circuitry provides complementary drive signals to the output stages. Cross conduction of the external MOSFETs is prevented by monitoring the voltage on the P-channel and N-channel driver pins in conjunction with a time delay optimized for FET turn-off characteristics.

RC: A parallel capacitor and resistor combination from RC to GND sets the PWM oscillator frequency according to the following equation:

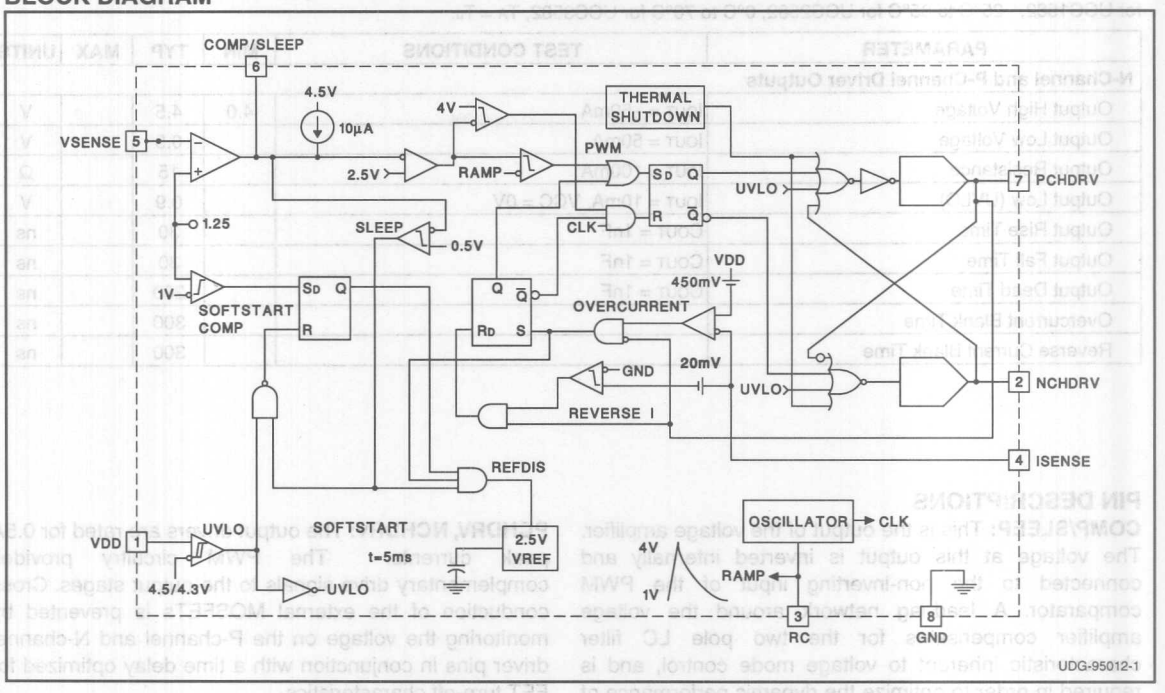
$$F \approx \frac{0.72}{RC}$$

Use a high quality ceramic capacitor with low ESL and ESR for best results. A minimum C_T value of 200pF ensures good accuracy and less susceptibility to circuit layout parasitics. The waveform on RC has a fast linear charge and slow RC exponential discharge characteristic. The exponential characteristic improves converter response to input line voltage changes. The oscillator and PWM are designed to provide practical operation to 500kHz.

VDD: Positive supply rail for the IC. Bypass this pin to GND with a 0.1 to 1µF low ESL/ESR ceramic capacitor.

VSENSE: This pin is the inverting input of the voltage amplifier and serves as the output voltage feedback point for the Buck converter. It senses the output voltage through an external divider.

BLOCK DIAGRAM



UNITRODE CORPORATION
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TEL. (603) 424-2410 • FAX (603) 424-3460

Switch Mode Secondary Side Post Regulator

FEATURES

- Precision Secondary Side Post Regulation for Multiple Output Power Supplies
- Useful for Both Single Ended and Center Tapped Secondary Circuits
- Ideal Replacement for Complex Magnetic Amplifier Regulated Circuits
- Leading Edge Modulation
- Does Not Require Gate Drive Transformer
- High Frequency (>500kHz) Operation
- Applicable for Wide Range of Output Voltages
- High Current Gate Driver (0.5A Sink/1.5A Source)
- Average Current Limiting Loop

DESCRIPTION

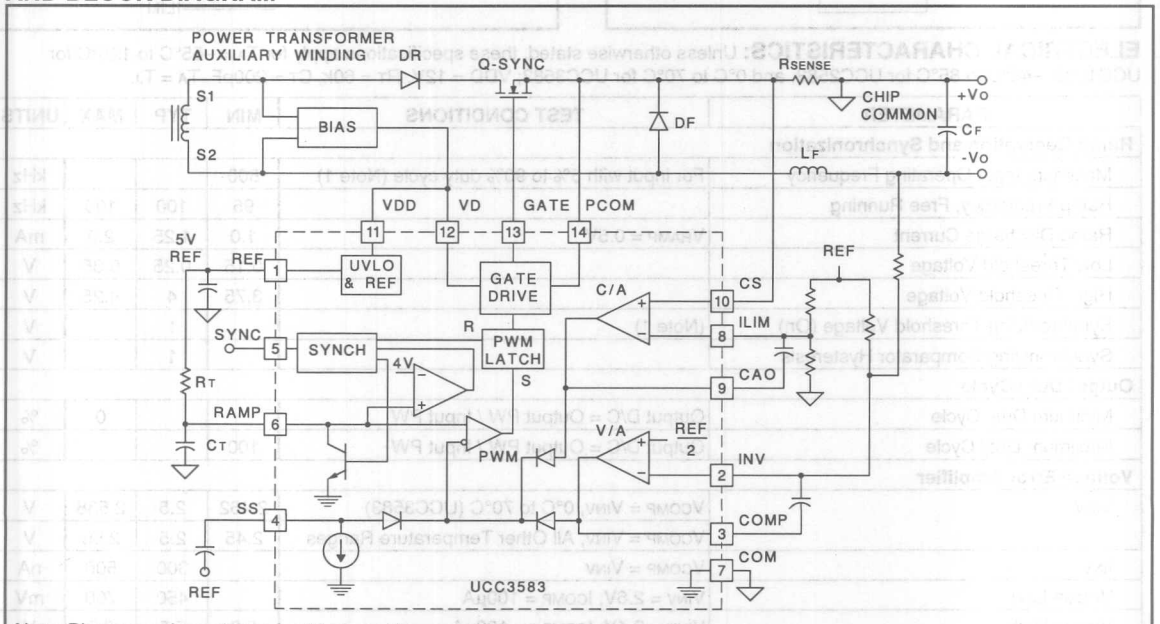
The UCC3583 is a synchronizable secondary side post regulator for precision regulation of the auxiliary outputs of multiple output power supplies. It contains a leading edge pulse width modulator, which generates the gate drive signal for a FET power switch connected in series with the rectifying diode. The turn-on of the power switch is delayed from the leading edge of the secondary power pulse to regulate the output voltage. The UCC3583 contains a ramp generator slaved to the secondary power pulse, a voltage error amplifier, a current error amplifier, a PWM comparator and associated logic, a gate driver, a precision reference, and protection circuitry.

The ramp discharge and termination of the gate drive signal are triggered by the synchronization pulse, typically derived from the falling edge of the transformer secondary voltage. The ramp starts charging again once its low threshold is reached. The gate drive signal is turned on when the ramp voltage exceeds the control voltage. This leading edge modulation technique prevents instability when the UCC3583 is used in peak current mode primary controlled systems.

The controller operates from a floating power supply referenced to the output voltage being controlled. It features an undervoltage lockout (UVLO) circuit, a soft start circuit, and an averaging current limit amplifier. The current limit can be programmed to be proportional to the output voltage, thus achieving foldback operation to minimize the dissipation under short circuit conditions.

The UCC1583 is specified for operation over the military temperature range of –55°C to 125°C. The UCC2583 is specified from –40°C to 85°C. The UCC3583 is specified from 0°C to 70°C. Package options include 14-pin surface mount or dual in-line and 20-pin plastic leadless chip carrier.

TYPICAL APPLICATION AND BLOCK DIAGRAM



Note: Pin connections shown for 14-pin packages.

UDG-96201-2

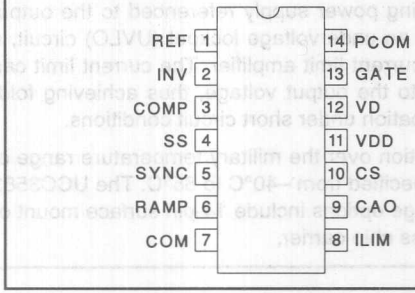
ABSOLUTE MAXIMUM RATINGS

V_{DD} 15V
I_{VDD} 15mA
RAMP ..... –0.3V to V_{DD} + 1V
I_{RAMP} 5mA
I_{REF} ..... –30mA
P_{COM} ..... –0.2V to 0.2V
I_{GATE} (twp < 1µS and Duty Cycle < 10%) ..... –0.8A to 1.8A
I_{COMP} ..... –5mA to 5mA
I_{CAO} ..... –5mA to 5mA
V_{SYNC} ..... –0.6V to V_{REF} +0.3V
I_{SYNC} ..... –05mA to 5mA
INV, SS, ILIM, ISENSE ..... –0.3V to VREF + 0.3V
Storage Temperature ..... –65°C to +150°C
Junction Temperature ..... –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

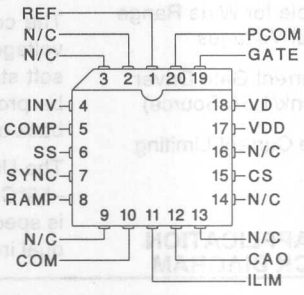
All voltages are with respect to the COM terminal unless otherwise stated. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAMS

DIL-14, SOIC-14 (Top View)
J, N, or D Packages



PLCC-20 (Top View)
Q Package



ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = –55°C to 125°C for UCC1583, –40°C to 85°C for UCC2583, and 0°C to 70°C for UCC3583; VDD = 12V, R_T = 60k, C_T = 200pF, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Ramp Generation and Synchronization					
Maximum Input Operating Frequency	For input with 5% to 90% duty cycle (Note 1)	500			kHz
Ramp Frequency, Free Running		95	100	105	kHz
Ramp Discharge Current	V_{RAMP} = 0.5V	1.0	1.25	2.0	mA
Low Threshold Voltage		0.15	0.25	0.35	V
High Threshold Voltage		3.75	4	4.25	V
Synchronizing Threshold Voltage (On)	(Note 1)		1		V
Synchronizing Comparator Hysteresis			1		V
Output Duty Cycle					
Minimum Duty Cycle	Output D/C = Output PW / Input PW			0	%
Maximum Duty Cycle	Output D/C = Output PW / Input PW	100			%
Voltage Error Amplifier					
V_{INV}	V_{COMP} = V_{INV}, 0°C to 70°C (UCC3583)	2.462	2.5	2.538	V
	V_{COMP} = V_{INV}, All Other Temperature Ranges	2.45	2.5	2.55	V
I_{INV}	V_{COMP} = V_{INV}		300	500	nA
V_{COMP} Low	V_{INV} = 2.6V, I_{COMP} = 100µA		450	700	mV
V_{COMP} High	V_{INV} = 2.4V, I_{COMP} = –100µA	5.0	5.5	6.0	V

ELECTRICAL CHARACTERISTICS (cont.): Unless otherwise stated, these specifications apply for T_A = –55°C to 125°C for UCC1583, –40°C to 85°C for UCC2583, and 0°C to 70°C for UCC3583. VDD = 12V, R_T = 60k, C_T = 200pF, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Voltage Error Amplifier (cont.)					
AVOL	No Load	80	100		dB
GBW Product	At f = 100kHz, T_A = 25°C (Note 1)	3	5		MHz
Current Error Amplifier					
Input CM Low	Common Mode for CS and ILIM (Note 1)			0	V
Input CM High	Common Mode for CS and ILIM (Note 1)	2			V
V_{CAO} Low	V_{+IN} = 0V, V_{-IN} = 0.1V, I_{CAO} = 100µA		250	500	mV
V_{CAO} High	V_{+IN} = 0V, V_{-IN} = 0.1V, I_{CAO} = –100µA	5.0	5.5	6.0	V
Input Current (ILIM and CS Pins)		–50	0	50	nA
AVOL	No Load	80	100		dB
GBW Product	At f = 100kHz, T_A = 25°C	2	4		MHz
Soft Start Current			10	25	µA
UVLO					
VDD On Threshold Voltage		8.5	9.0	9.5	V
VDD Off Threshold Voltage		7.9	8.4	8.9	V
UVLO Hysteresis		0.3	0.6	0.9	V
Bias Supply					
Supply Clamp Voltage		13	14	15	V
Supply Current (VDD)	f = 100kHz With No Gate Output Load		3	5	mA
Output Driver					
V_{SAT} High	I_{GATE} = –150mA		0.6	1.0	V
V_{SAT} Low	I_{GATE} = 50mA		0.4	0.75	V
Rise Time	C_{GATE} = 1nF		50	75	ns
Fall Time	C_{GATE} = 330pF		20	40	ns
Reference					
V_{REF}	I_{REF} = 0, 0°C to 70°C (UCC3583)	4.925	5	5.075	V
	I_{REF} = 0, All Other Temperature Ranges	4.900	5	5.100	V
Line Regulation	VDD = 10V to 14V		2	30	mV
Load Regulation	I_{REF} = 0mA to 2mA		1	20	mV

Note 1: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

CAO: Output of the current error amplifier. Averaging of the sensed current signal is provided by connecting an integrating capacitor between ILIM and CAO. CAO feeds into the PWM comparator input and controls the loop when its voltage is higher than the voltage at COMP (output of the voltage error amplifier).

COM: Signal ground for the chip. It is connected to the positive terminal of the output voltage being regulated by the IC.

COMP: Output of the voltage error amplifier fed into the PWM comparator. Loop compensation components are connected between COMP and INV.

CS: Non-inverting input of the current error amplifier. The sensed current signal from the current sense resistor is connected to this pin. By making the signal at CS proportional to the output voltage, effective current foldback limiting can be provided.

GATE: Gate drive output for the power switch FET. The drive pin has a 0.5A sink/1.5A source capability and very low output off-state impedance.

ILIM: Inverting input of the current error amplifier. It sets the DC limit for the output current.

INV: Inverting input of the voltage error amplifier. The feedback signal is connected to this pin using a resistive divider between REF and –Vo.

PCOM: Power ground for the chip. It is connected to the source terminal of the MOSFET being regulated by the IC.

PIN DESCRIPTIONS (cont.)

RAMP: This pin is the input to the PWM comparator and provides a ramp signal for generation of the PWM signal. A capacitor to COM and a resistor to REF set the charging rate for the ramp. An internal current source of 1mA discharges RAMP when synchronization signal appears or when RAMP crosses a 4V threshold. In the intended mode of operation, the switching frequency is determined by the secondary power pulse. The RC components at RAMP should be selected to give an appropriately sized ramp signal. In the absence of a synchronizing pulse, these RC components determine the free running frequency of the controller.

REF: Precision 5V reference pin. REF stays off until VDD exceeds 9V and turns off again when VDD drops below 8.4V. Bypass REF to COM.

SS: This pin provides a soft start function. A capacitor to REF programs the soft start time. During soft start, the PWM comparator is controlled by the soft start voltage resulting in a slow increase in output duty cycle. Once the soft start capacitor is discharged, output control is dictated by the larger of the output at CAO or COMP.

SYNC: Synchronization input pin. It is connected to a signal representative of the secondary power pulse. One possible implementation is to use a resistive divider between terminal S2 of the secondary winding shown in Figure 1 and REF for generating the input to the SYNC pin. The synchronizing comparator is referenced to 0.5V and has 1V of hysteresis.

VD: Power supply for the output driver. VD should be tied to VDD in the application.

VDD: Power supply for the chip. VDD should be bypassed to COM. VDD has to be 9V for the IC to start and 8.4V for it to remain operational. A shunt clamp from VDD to COM limits the supply voltage to 14V.

APPLICATION INFORMATION

Power Stage Circuit Configuration

The UCC3583 is designed for use in a post regulator application for tightly regulating auxiliary outputs in a multiple output converter. The post regulation is applied to the secondary side power pulse of a power transformer where the power pulse is controlled by the feedback signal from the main output. In order to simplify the application of the UCC3583, it is required that the IC be referenced to the positive output terminal and the output filter inductor be placed in the return path. The placement of the inductor in the return path facilitates better EMI performance, in addition to making magnetic designs and terminations easier to implement. Typical set-up and circuit waveforms of the UCC3583 system application are shown in Figure 1. Figure 2 shows waveforms for a single ended output rectifier application of the UCC3583 shown on page 1. The UCC3583 can also be used in half bridge rectifier applications as shown by the circuit and waveforms depicted in Figures 3 and 4. Referencing the IC to the positive output terminal creates a requirement for a floating bias voltage for the IC which can be referenced to the same positive voltage terminal. Possible implementations of deriving the floating bias voltage are shown in Figure 5.

For the circuit shown in Figure 5a, CC1 is charged when the transformer voltage is positive and the synchronous switch is on. During the off period of Q-SYNC, the charge is transferred to CC2 through diode DC2. Diode DC3 charges CC2 during the blocking interval of Q-SYNC. This method is preferable when the transformer positive voltage is high enough to generate the required bias voltage. For the circuit shown in Figure 5b, CC1 is charged during the period when reverse (reset) voltage appears across the secondary. The charge on CC1 is transferred to CC2 through DC2 when Q-SYNC turns on. This method is preferable when the reverse voltage is high enough to generate the required bias voltage. The series resistor should be chosen to handle the required voltage drop at full IC operating current when the zener clamp across VDD and COM is activated.

The following is a description of the major functional blocks of the UCC3583. Refer to Figure 6 (Typical Application Circuit) for component designations.

UVLO and Start Up

The UCC3583 has an internal undervoltage lockout circuit which keeps the internal circuitry inactive until VDD exceeds the upper threshold (9V). Once the chip is activated, VDD has to be above the lower UVLO threshold (8.4V) for it to remain functional. The IC requires a low startup current of only 100µA when VDD is under the UVLO threshold. VDD has an internal clamp of 14V which can sink up to 10mA. Measures must be taken not to exceed this current. The internal reference (REF) is brought up when the UVLO on threshold is exceeded.

The soft start pin provides an effective means to start the IC in a controlled manner. An internal current of 10µA starts discharging a capacitor connected to SS

APPLICATION INFORMATION (cont.)

when the UVLO conditions have been removed. The voltage on SS controls the duty cycle of the output during the discharge period.

Synchronizing Circuit and Oscillator

UCC3583 is primarily intended for synchronizable operation where its switching frequency is determined by the secondary pulse of the power transformer. However, it has an internal oscillator which allows it to operate in free-running mode when an external synchronization pulse is not available. The switching frequency is determined by resistor R_T connected between REF and RAMP and capacitor C_T connected from RAMP to GND. The frequency is given by:

$$freq = \frac{1}{t_{CH} + t_{DIS}} \text{ where } t_{CH} = 1.56 \bullet R_T \bullet C_T \text{ and}$$

$$t_{DIS} = \frac{C_T \bullet V_{RAMP\ (p-p)}}{I_{RAMP\ (dis)}} \approx 3000 \bullet C_T$$

The values of R_T and C_T are also dictated by the fact that the ramp is discharged through an internal impedance of 2k. The value of R_T needs to be at least 50k to ensure that the internal discharge current is the current through R_T during the entire discharge period. This results in making the value of C_T relatively small for a desired frequency of operation.

When the synchronizing signal is available, the oscillator frequency should be programmed to be lower than the synchronizing frequency to ensure proper operation. A large difference in self-running and synchronizing frequencies leads to smaller ramp amplitude and higher noise sensitivity. The ramp capacitor is discharged when the synchronization signal arrives and begins charging when the low threshold is crossed.

There are two methods to synchronize to the secondary pulse. One method is to use the rising edge of the secondary pulse, which reduces the maximum duty cycle available. Subsequently, the post regulator switch cannot be turned on during the C_T discharge time. The other method is to use the falling edge of the secondary pulse for synchronization. This method is preferable because it allows a slower discharge of the ramp capacitor without affecting the maximum available duty cycle of the post regulator. The UCC3583 SYNC input needs to exceed a fixed threshold (0.5V typical) for synchronization to take effect. Hence the IC is usable with either method of synchronization. However, the UCC3583 oscillator configuration is better suited for synchronization to the falling edge. A recommended method to implement the synchronization is shown in Figure 6. By connecting SYNC to a resistive divider between REF and the secondary terminal S2, the synchronization is achieved whenever the voltage on S2 goes from a negative value to zero. R_A and R_B should be selected so that at the lowest negative voltage on S2 (during the primary pulse on period), the voltage on SYNC does not exceed the threshold voltage of 0.5V. Placement of a Schottky diode from SYNC to COM prevents the voltage at SYNC from going negative.

PWM Comparator

The UCC3583 uses a leading edge PWM scheme. In a leading edge PWM, the output pulse (gate signal) is turned on when the error amplifier crosses the PWM ramp and turned off by the clock/oscillator. Leading edge modulation is naturally provided by magamp type post regulators and is an essential feature for post regulators. Without the leading edge modulation in a multiple output converter with post regulation on one or more outputs, the primary current shape does not remain monotonic and can lead to instability when the primary current is used for current mode control or current limiting. When compared to conventional trailing edge PWMs, the leading edge modulation leads to a phase inversion that needs to be accounted for in the feedback loop. For the UCC3583, this inversion is automatically provided since the sensed voltage at the power supply output negative terminal has a negative polarity with respect to the chip common. Thus, UCC3583 does not require inverting buffers which would otherwise be needed.

Error Signal Generation and Current Limiting

The PWM comparator in the UCC3583 is controlled by three parallel loops with only one of them in effect at a time. During normal operation, the voltage error amplifier output is fed to the PWM comparator. The voltage error amplifier can be compensated using commonly used feedback techniques to achieve the desired dynamic performance. The ouput drive capability of the voltage amplifier is limited to 100µA, so appropriately high impedances should be used to utilize the full output swing of the amplifier. During startup, the soft start capacitor controls the pulse width. The third control loop is provided by the average current amplifier. By sensing the instantaneous inductor current and filtering/averaging it with the current error amplifier, accurate current limiting is achieved. This loop is in effect only during the overcurrent mode and provides a more accurate and noise free control of the maximum output current com-

APPLICATION INFORMATION (cont.)

pared to conventional peak current limiting circuits. The current limit is set by programming the voltage at ILIM based on the current sense resistor chosen. In addition, the current limit can be made proportional to the output voltage in order to limit the power dissipation under short circuit conditions. This is implemented by inserting a bias voltage on CS which is proportional to the output voltage.

Gate Drive Circuit

The gate drive circuit of the UCC3583 provides high current drive capability and is very easy to implement as a result of tying the chip common to the source of the switching device. Turn on current is higher (1.5A) as fast turn on is essential for low losses and effective operation. During the turn off, the drain voltage disappears, so turn off time can be slower without increasing switching losses.

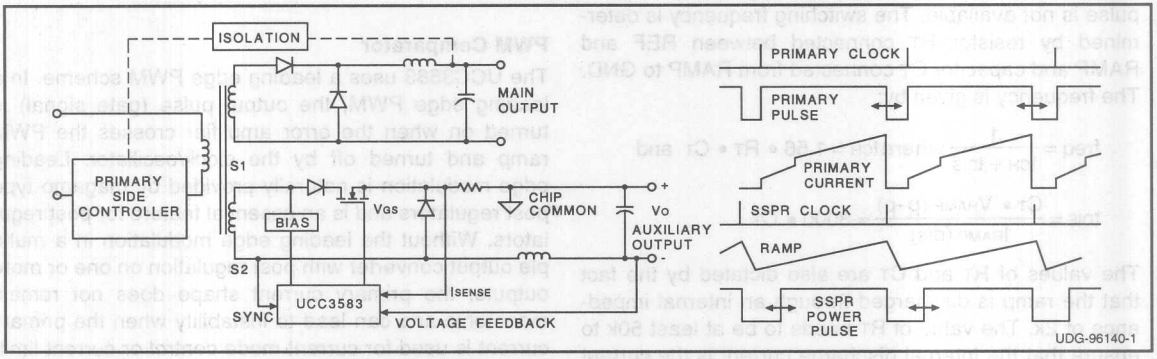


Figure 1. UCC3583 SSPR System Application and Typical Waveforms

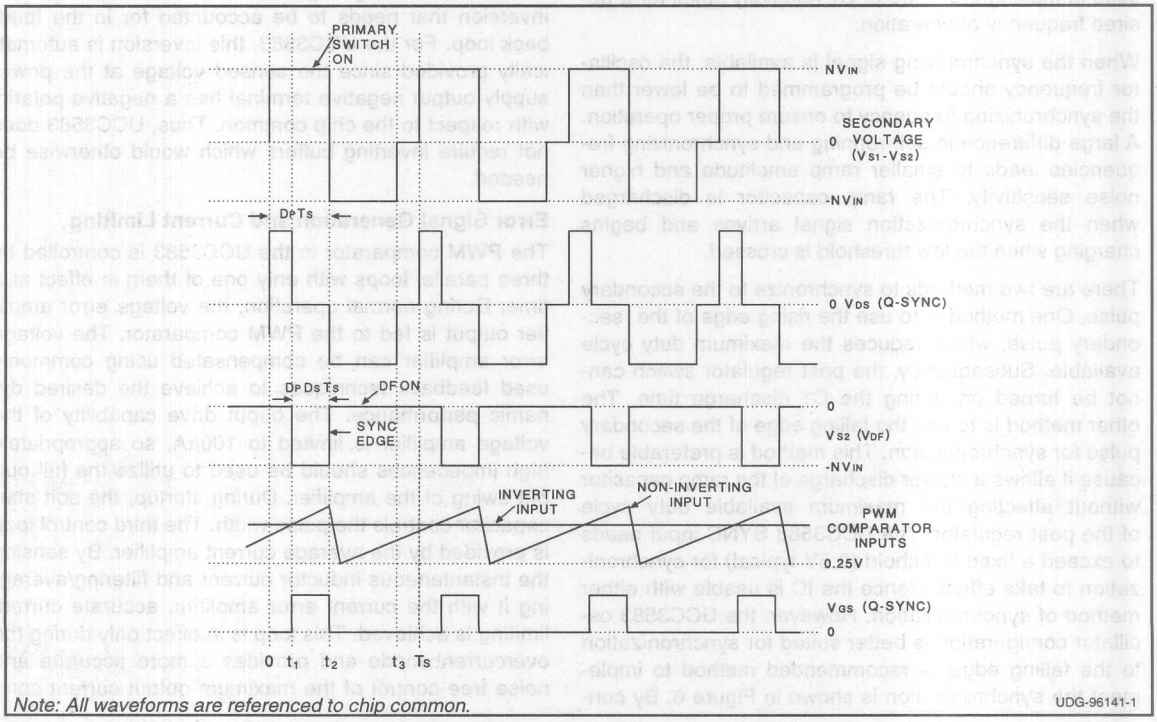


Figure 2. Single Ended Post Regulator Waveforms

APPLICATION INFORMATION (cont.)

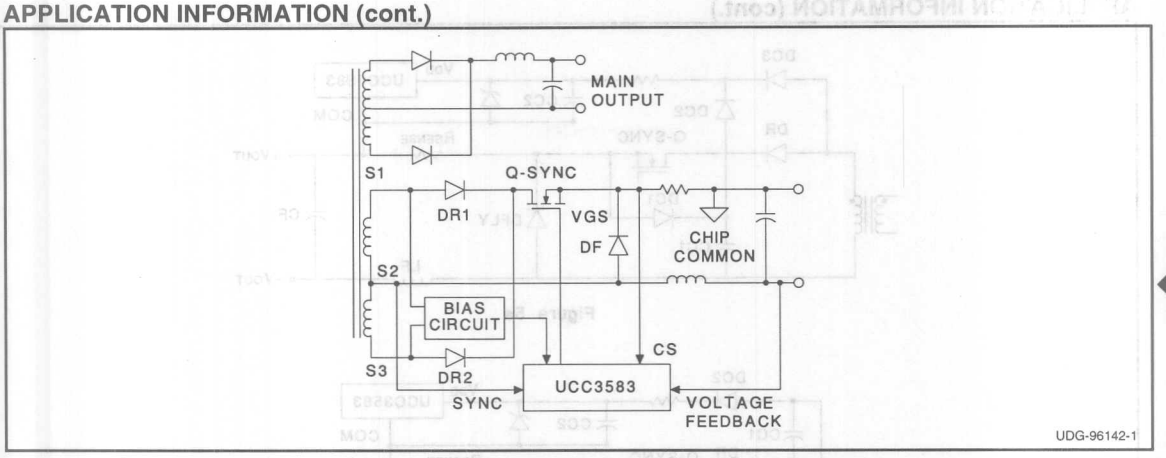


Figure 3. Half-Bridge Synchronous Post Regulator Application

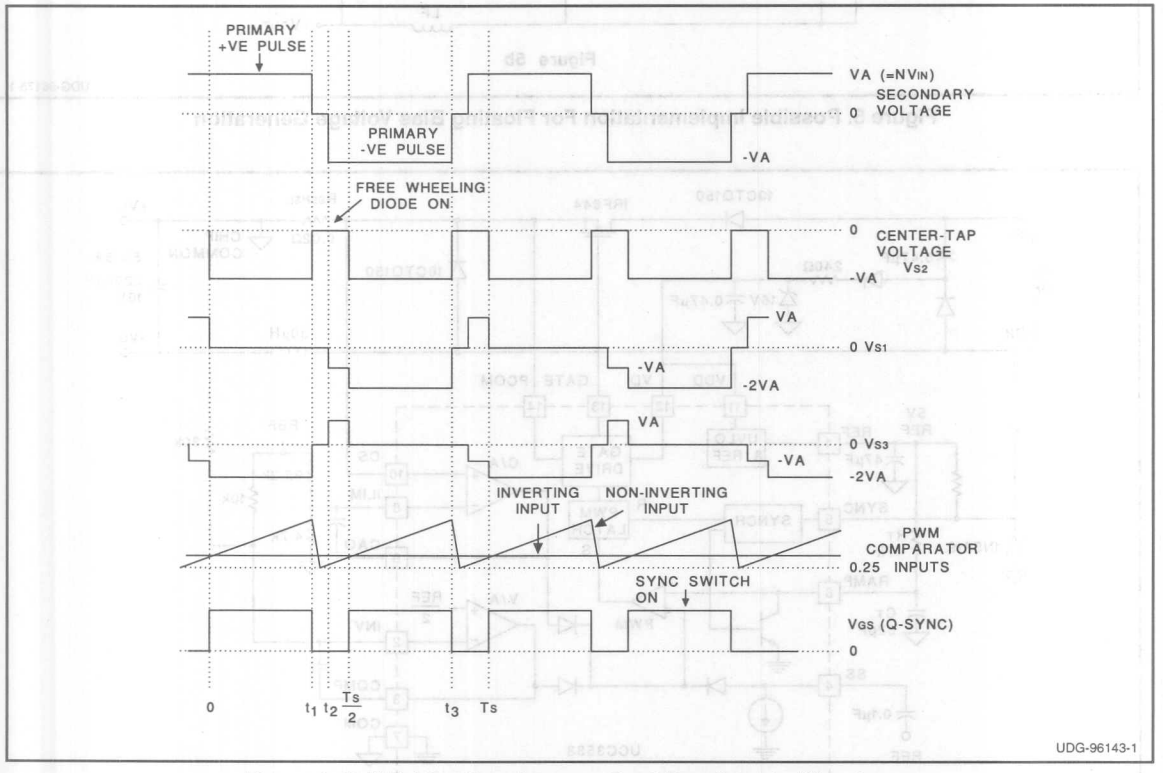


Figure 4. Half-Bridge Synchronous Post Regulator to Waveforms

APPLICATION INFORMATION (cont.)

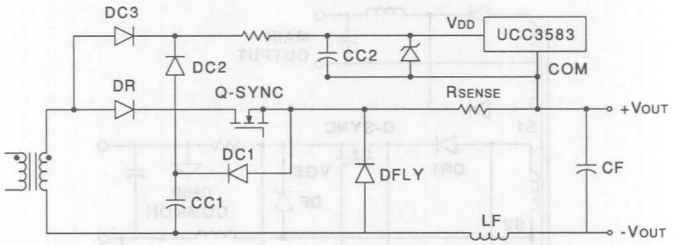


Figure 5a

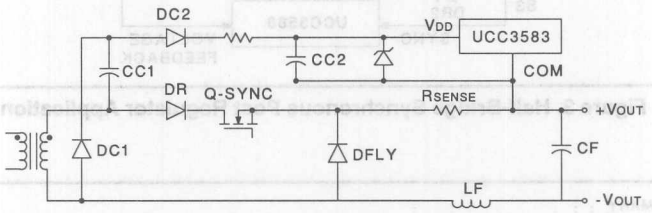
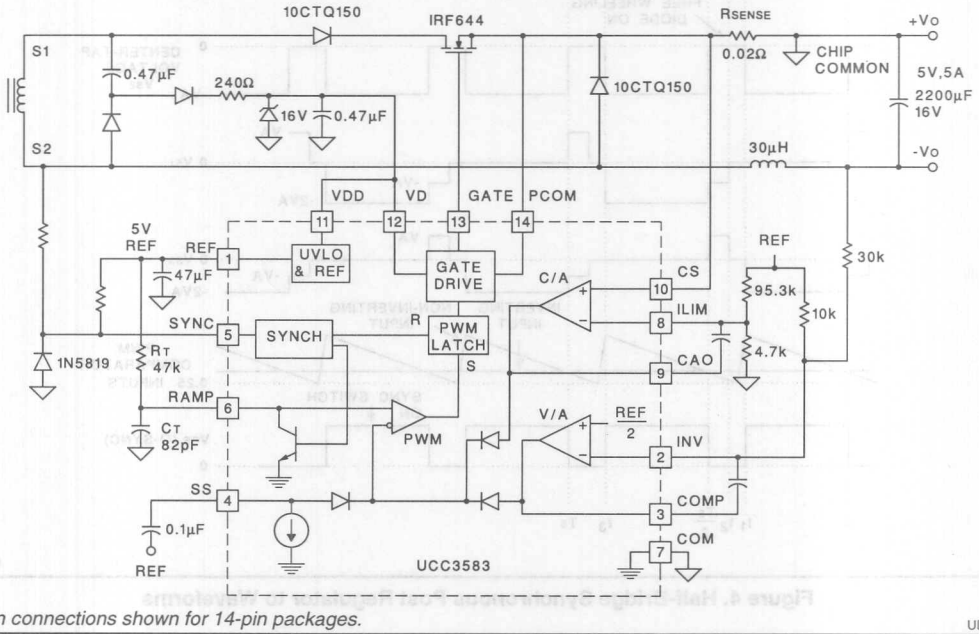


Figure 5b

UDG-96175-1

Figure 5. Possible Implementation For Floating Bias Voltage Generation



Note: Pin connections shown for 14-pin packages.

UDG-96072-2

Figure 6. Typical Application Circuit for UCC3583

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Secondary Side Synchronous Post Regulator

FEATURES

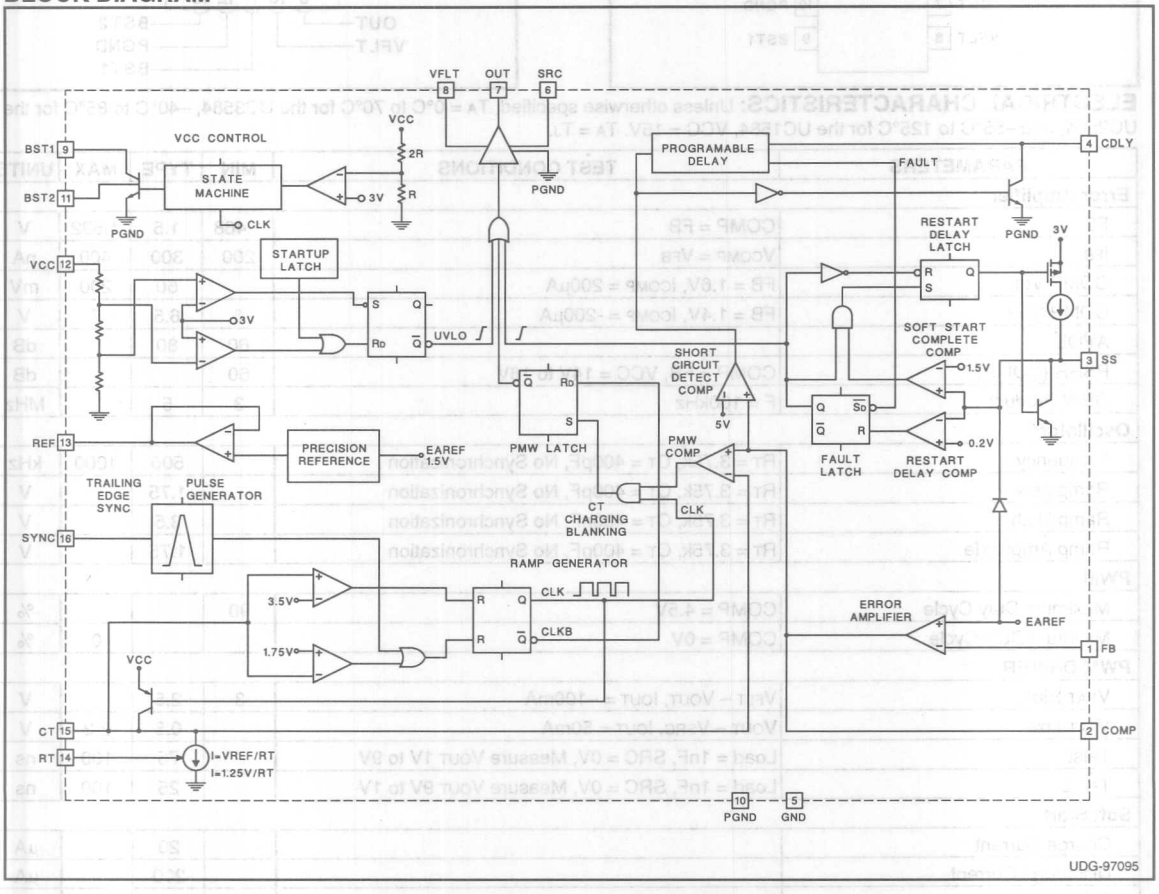
- Practical Operation at Switching Frequencies up to 1MHz
- Wide Band Error Amplifier
- Undervoltage Lockout with Hysteresis
- Output Active Low During UVLO
- Soft Start/Maximum Duty Cycle Control
- Trimmed Bandgap Reference
- Internally Regulated 15V Boost Supply

DESCRIPTION

The UC3584 is a low voltage, Secondary Side Synchronous Post Regulator. It is intended to be used for auxiliary output voltage regulation in single secondary winding, multiple output power supplies (for more details refer to the Application Section of this Data sheet). The UC3584 is most suited for systems where the main output is regulated between 5V and 14V. Output voltages regulated by the UC3584 can range from virtually 0V up to the output voltage of the main output.

Auxiliary output voltage regulation with the UC3584 uses leading edge modulation making it compatible to primary side peak current or voltage mode control. The UC3584 clock circuit is synchronized to the switching frequency utilizing the trailing edge of the transformer's secondary winding waveform.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

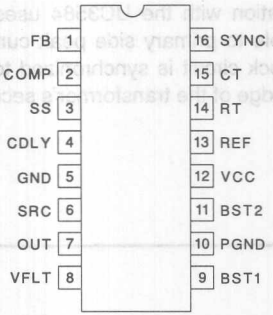
Supply Voltage 20V
V_{FLT} Voltage . . . . . 50V, 30V at 2A
Supply Current 50mA
Analog Inputs . . . . . –0.3 to 20V
PWM Driver, I_{OUT} . . . . . ±300mA
PWM Driver, I_{OUT} (Peak) . . . . . ±1.5A
Power Dissipation at TA = 60°C 1W

Storage Temperature . . . . . –65°C to 150°C
Junction Temperature . . . . . –55°C to 150°C
Lead Temperature (Soldering, 10 sec.) . . . . . 300°C

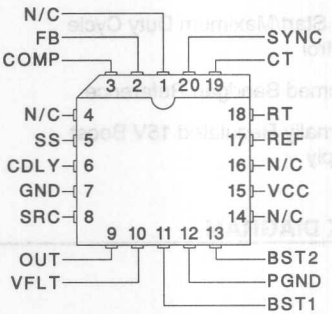
Currents are positive into, negative out of specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

DIL-16, SOIC-16 (Top View)
J, N or DW Packages



PLCC-20 (Top View)
Q Package



ELECTRICAL CHARACTERISTICS:

Unless otherwise specified, T_A = 0°C to 70°C for the UC3584, –40°C to 85°C for the UC2584, and –55°C to 125°C for the UC1584, VCC = 15V. T_A = T_J.

PARAMETERS	TEST CONDITIONS	MIN	TYPE	MAX	UNITS
Error Amplifier					
FB	COMP = FB	1.468	1.5	1.532	V
I_{FB}	V_{COMP} = V_{FB}	200	300	400	nA
COMP V_{OL}	FB = 1.6V, I_{COMP} = 200µA		50	200	mV
COMP V_{OH}	FB = 1.4V, I_{COMP} = -200µA	6	6.5	7	V
AVOL		60	80		dB
PSRR (COMP)	COMP = FB, VCC = 14V to 16V	60			dB
GBW Product	F = 100kHz	3	5		MHz
Oscillator					
Frequency	R_T = 3.75k, C_T = 400pF, No Synchronization		500	1000	kHz
Ramp Low	R_T = 3.75k, C_T = 400pF, No Synchronization		1.75		V
Ramp High	R_T = 3.75k, C_T = 400pF, No Synchronization		3.5		V
Ramp Amplitude	R_T = 3.75k, C_T = 400pF, No Synchronization		1.75		V
PWM					
Maximum Duty Cycle	COMP = 4.5V	90			%
Minimum Duty Cycle	COMP = 0V			0	%
PWM DRIVER					
V_{SAT} High	V_{FLT} – V_{OUT}, I_{OUT} = –100mA	3	2.5		V
V_{SAT} Low	V_{OUT} – V_{SRC}, I_{OUT} = 50mA		0.8	2.2	V
T_{RISE}	Load = 1nF, SRC = 0V, Measure V_{OUT} 1V to 9V		75	100	ns
T_{FALL}	Load = 1nF, SRC = 0V, Measure V_{OUT} 9V to 1V		25	100	ns
Soft Start					
Charge Current			20		µA
Discharge Current			200		µA
SS Delay	C_{SS} = 500nF		50		ms

ELECTRICAL CHARACTERISTICS (cont.): Unless otherwise specified, T_A = 0°C to 70°C for the UC3584, –40°C to 85°C for the UC2584, and –55°C to 125°C for the UC1584, VCC = 15V. $T_A = T_J$.

PARAMETERS	TEST CONDITIONS	MIN	TYPE	MAX	UNITS
Fault Latch					
Charge Current			20		µA
Discharge Current			200		µA
Fault Latch Delay	CDLY = 500nF		50		ms
UVLO					
VCC On			10		V
VCC Off			8.8		V
Hysteresis			1.2		V
Voltage Reference					
REF	I_{REF} = 0mA to 1mA	4.9		5.1	V
VCC Regulator					
VCC	Boost inductor connected to 5V	14	15	16	V
Ivcc	No Load, Boost Circuitry Active		25		mA

PIN DESCRIPTIONS

BST1: Collector of the boost switch. This is the connection point of the external boost inductor and boost diode. The boost converter generates the bias supply for the UC3584 from the regulated 5V output.

BST2: See BST1. BST2 must be connected externally to BST1 pin.

CDLY: Delay Set. External CDLY capacitor sets the delay from the time Short Circuit condition is detected and Fault Condition is asserted.

COMP: Output of the Voltage Error Amplifier.

CT: Connect the Timing Capacitor between CT and GND.

FB: Inverting Input of the Voltage Error Amplifier.

GND: Analog System Ground.

OUT: Output of the floating driver for an external, N-channel MOSFET.

PGND: Power Ground. This is the reference node for the boost bias supply regulator. PGND and GND must be connected externally.

REF: Output of the internal 5V reference. Must be decoupled to GND.

RT: A Timing Resistor connected between RT and GND sets the discharge current of the timing capacitor.

SRC: Source connection of the floating driver to the external switch.

SS: Soft Start. An external capacitor is connected between SS and GND to set the duration of the Soft Start cycle.

SYNC: Synchronization Pin. The UC3584 is synchronized from the falling edge of the transformer's secondary winding.

VCC: Bias supply of the chip, approximately 15V. This is also the output of the boost regulator. The VCC pin must be decoupled to PGND.

VFLT: Positive rail of the floating driver's bias supply. Decouple to SRC using a high frequency (ceramic) capacitor.

APPLICATION INFORMATION

Biasing the UC3584

Bias supply for the UC3584 is generated from the main output of the power supply by a boost regulator. This part of the UC3584 is operational from 4.5V on the VCC pin. The inductor, diode and capacitor of the boost converter are external components, while the boost switch is internal to the chip. The boost converter operates in a burst mode with a built-in hysteresis of approximately 1V. When VCC drops below a certain voltage, the boost switch is enabled and the boost converter brings back the voltage on VCC to a regulated level. The boost switch is synchronized to the oscillator of the UC3584 and it has a fixed duty ratio of 0.75.

Undervoltage Detection

The UVLO circuit of the UC3584 monitors the voltage on VCC. During power up and power down, the pulse width modulator and the output driver are disabled and OUT is held active low. Operation is enabled when VCC reaches 10V. The UVLO circuitry has a built-in hysteresis of 1.2V (10V to 8.8V) thus VCC must drop below 8.8V in order to assert UVLO again.

APPLICATION INFORMATION

Precision Reference

An internal precision bandgap reference provides accurate voltages to the error amplifier and other control sections of the IC. A buffered 5V reference voltage is also available for external circuitry on REF terminal. This pin must be decoupled to the signal GND connection by a good quality high frequency capacitor.

Oscillator and Trailing Edge Synchronization

The UC3584 is outfitted with a synchronizable oscillator which also generates a ramp signal across the C_T capacitor for the PWM comparator. For easy implementation of the leading edge pulse width modulation technique, the oscillator has an inverted ramp waveform as shown in Figure 1. The free running oscillator frequency is determined by the timing components, R_T and C_T, according to the following equations:

$$R_T = \frac{1.5 \bullet D}{0.0065 \bullet (1 - D_{MAX})}$$

$$C_T = \frac{0.6 \bullet D_{MAX}}{R_T \bullet f_{OSC}}$$

where

R_T is the timing resistor, its value should be between 1kΩ and 100kΩ,

C_T is the timing capacitor,

D_{MAX} is the desired maximum duty cycle, and

f_{OSC} is the free running oscillator frequency.

During normal operation the oscillator must be synchronized to the trailing (falling) edge of the transformer secondary waveform. Synchronization is achieved by connecting SYNC to the secondary winding via a resistor divider. The resistor divider must be chosen to provide a SYNC pin voltage in excess of 3V at the lowest operating voltage on the transformer secondary winding. The UC3584 will generate a narrow synchronization pulse which will synchronize the oscillator to the switching frequency of the main converter.

PWM and Output Driver

The UC3584 employs leading edge modulation technique to set the required on time of its output. Leading edge modulation is preferred for secondary side regulation in multiple output converters to prevent ambiguity in the primary current waveform. In fact, this is the only feasible technique to preserve compatibility with primary side peak current mode control.

As Figure 1 depicts the UC3584 utilizes voltage mode control to regulate output voltage. The output pulse width (the on-time of the MOSFET switch) is determined on a cycle-by-cycle basis by comparing the output of the voltage error amplifier and the ramp waveforms across the timing capacitor. OUT is high when the voltage on COMP exceeds the voltage on CT. There are three more conditions which must be satisfied to obtain an active high on the OUT pin. These conditions are:

1. VCC within normal range (UVLO is inactive),
2. No fault condition is detected,
3. C_T is discharging.

During the fast charging time of the C_T capacitor is held low.

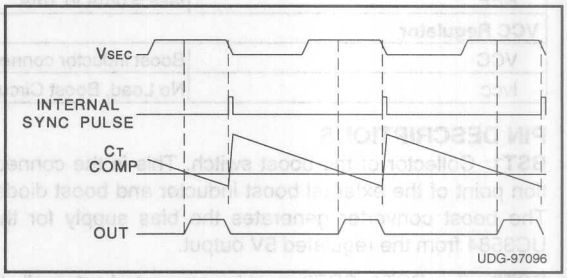


Figure 1. Trailing Edge Synchronization, Leading

Ultimately, the output of the PWM circuitry controls the conduction interval of an external N-channel MOSFET switch in the power supply. The UC3584 employs an on-board, floating gate driver circuit to interface to the external switch. An external capacitor connected between FLT and SRC acts as a floating power supply for the driver during the on-time of the switch. Charge is being replenished to the bootstrap capacitor during the off-time of the switch through the bootstrap diode connected between VCC and FLT, as shown in the typical application diagram.

Soft Start

The UC3584 Soft Start circuitry is designed to implement closed loop startup of the power supply output. During Soft Start, the reference to the noninverting input of the error amplifier is controlled by the voltage across the soft start capacitor on SS. As this voltage rises during soft start, it provides an increasing reference to the error amplifier. Once the soft start capacitor charges above the 1.5V precision reference of the error amplifier, SS gets disconnected from the noninverting input of the error amplifier. This technique allows the error amplifier to stay in its linear mode and to regulate the output voltage of the power supply according to the gradually increasing reference voltage on its noninverting input. Further advantage of the closed loop start up scheme is the absence of output voltage overshoot during power up of the power supply output.

APPLICATION INFORMATION (cont.)

Fault Detection

Fault Detection feature is implemented to detect excessive over load conditions. Under these conditions the error amplifier output goes high to command the maximum duty cycle. As soon as the error amplifier's output exceeds 5V, the fault delay capacitor connected to the CDLY pin starts charging. If CDLY capacitor voltage reaches 2V before the error amplifier output falls back below 5V, a fault condition is declared, the PWM output is disabled and soft start cycle is initiated. Under persistent fault conditions the UC3584 will continuously cycle through soft start sequence, attempting to bring the output to its regulated, nominal voltage. The value of CDLY capacitor should be chosen large enough to delay the activation of the fault sequence in case of load transients which can also cause the error amplifier output to go high temporarily.

Error Amplifier

The Error Amplifier of the UC3584 is used to regulate the voltage of an auxiliary output in a power supply. The noninverting input of the error amplifier is connected to an internal, 1.5V reference. The inverting input (FB pin) is tied to an output voltage divider. The compensation network of the negative feedback loop is connected between the amplifier's output (COMP pin) and FB. The noninverting input of the error amplifier is also connected to the SS node through a diode. This arrangement allows closed loop soft start for the output of a power supply regulated by the UC3584. Closed loop soft start assures that the error amplifier is kept in active mode and the output voltage of the converter follows the reference voltage on its noninverting input as it ramps up (following the SS node). If a fault condition is detected, SS node gets pulled to ground, forcing the error amplifier's reference, consequently the output voltage of the converter to go to ground.

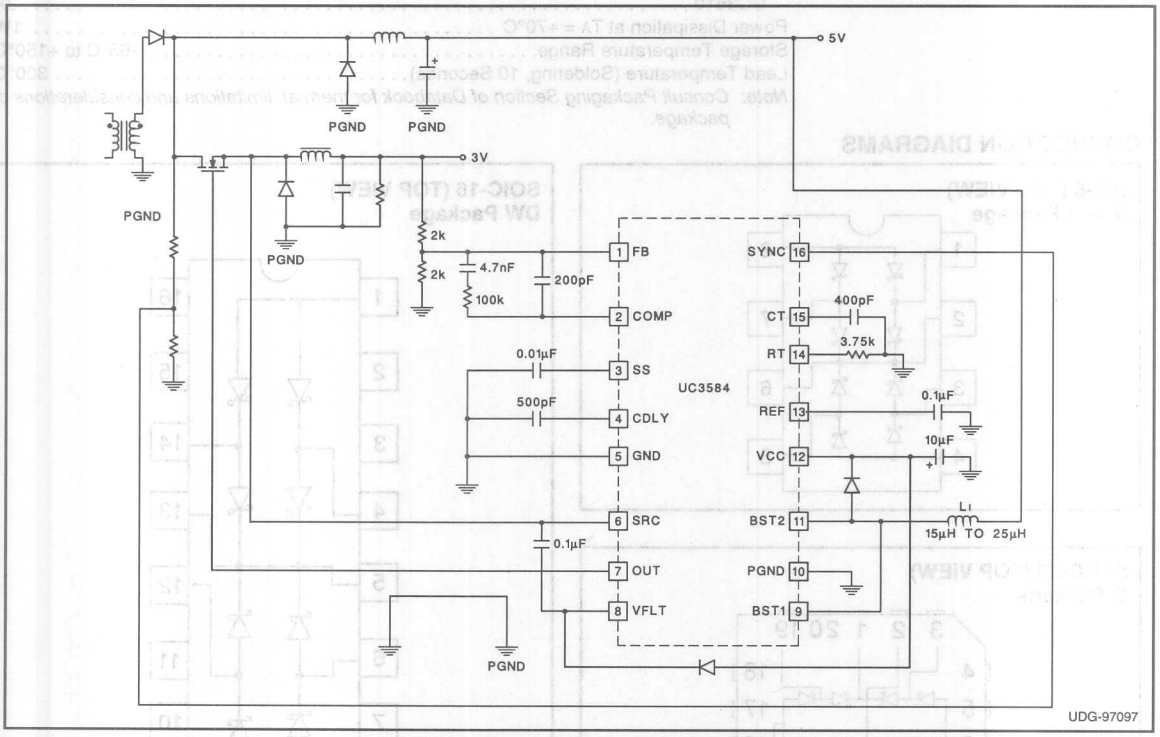


Figure 2. System Application Diagram

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Dual Schottky Diode Bridge

FEATURES

- Monolithic Eight-Diode Array
- Exceptional Efficiency
- Low Forward Voltage
- Fast Recovery Time
- High Peak Current
- Small Size

DESCRIPTION

This eight-diode array is designed for high-current, low duty-cycle applications typical of flyback voltage clamping for inductive loads. The dual bridge connection makes this device particularly applicable to bipolar driven stepper motors.

The use of Schottky diode technology features high efficiency through lowered forward voltage drop and decreased reverse recovery time.

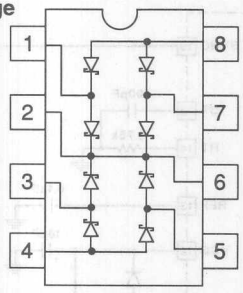
This single monolithic chip is fabricated in both hermetic CERDIP and copper-leaded plastic packages. The UC1610 in ceramic is designed for -55°C to +125°C environments but with reduced peak current capability. The UC2610 in plastic and ceramic is designed for -25°C to +125°C environments also with reduced peak current capability; while the UC3610 in plastic has higher current rating over a 0°C to +70°C temperature range.

ABSOLUTE MAXIMUM RATINGS

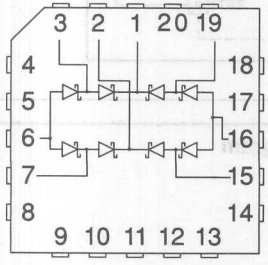
Peak Inverse Voltage (per diode) 50V
Peak Forward Current
UC1610 . . . . . 1A
UC2610 . . . . . 1A
UC3610 . . . . . 3A
Power Dissipation at T_A = +70°C 1W
Storage Temperature Range. . . . . -65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) . . . . . 300°C
Note: Consult Packaging Section of Databook for thermal limitations and considerations of package.

CONNECTION DIAGRAMS

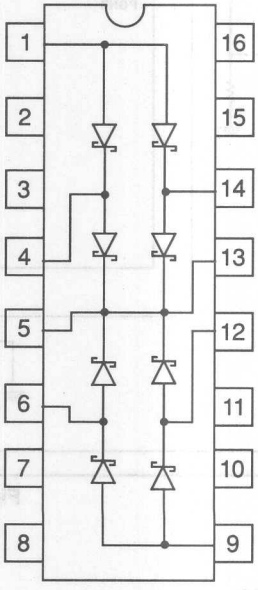
DIL-8 (TOP VIEW)
N or J Package



PLCC-20 (TOP VIEW)
Q Package



SOIC-16 (TOP VIEW)
DW Package

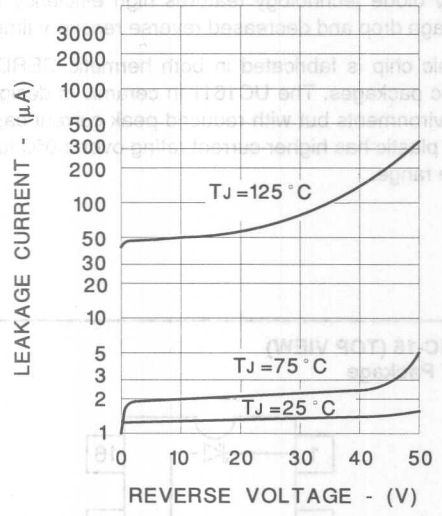


ELECTRICAL CHARACTERISTICS: All specifications apply to each individual diode. T_J = 25°C except as noted. $T_A = T_J$.

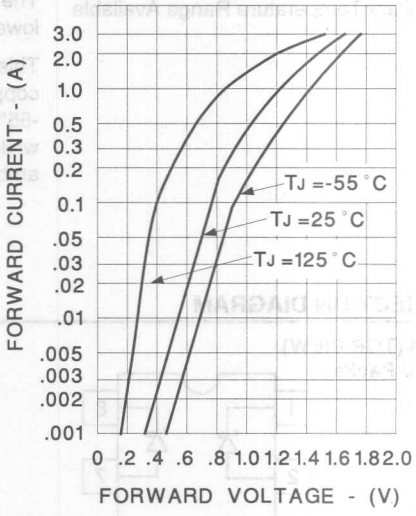
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward Voltage Drop	I_F = 100mA	0.35	0.5	0.7	V
	I_F = 1A	0.8	1.0	1.3	V
Leakage Current	V_R = 40V		.01	0.1	mA
	V_R = 40V, T_J = +100°C		0.1	1.0	mA
Reverse Recovery	0.5A Forward to 0.5A Reverse		15		ns
Forward Recovery	1A Forward to 1.1V Recovery		30		ns
Junction Capacitance	V_R = 5V		70		pF

Note: At forward currents of greater than 1.0A a parasitic current of approximately 10mA may be collected by adjacent diodes.

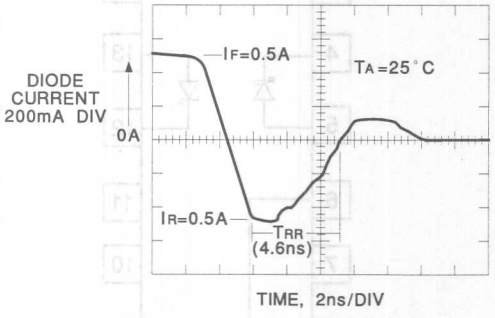
Reverse Current vs Voltage



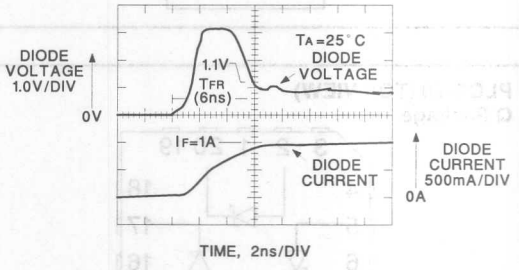
Forward Current vs Voltage



Reverse Recovery Characteristics



Forward Recovery Characteristics



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Quad Schottky Diode Array

FEATURES

- Matched, Four-Diode Monolithic Array
- High Peak Current
- Low-Cost MINIDIP Package
- Low-Forward Voltage
- Parallelable for Lower V_F or Higher I_F
- Fast Recovery Time
- Military Temperature Range Available

DESCRIPTION

This four-diode array is designed for general purpose use as individual diodes or as a high-speed, high-current bridge. It is particularly useful on the outputs of high-speed power MOSFET drivers where Schottky diodes are needed to clamp any negative excursions caused by ringing on the driven line.

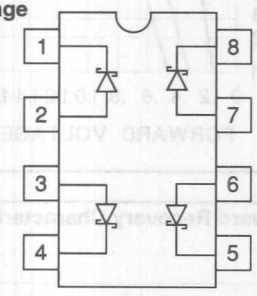
These diodes are also ideally suited for use as voltage clamps when driving inductive loads such as relays and solenoids, and to provide a path for current free-wheeling in motor drive applications.

The use of Schottky diode technology features high efficiency through lowered forward voltage drop and decreased reverse recovery time.

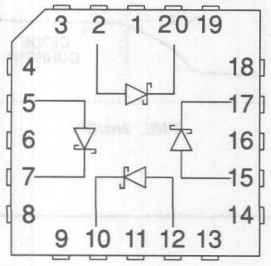
This single monolithic chip is fabricated in both hermetic CERDIP and copper-leaded plastic packages. The UC1611 in ceramic is designed for -55°C to +125°C environments but with reduced peak current capability: while the UC3611 in plastic has higher current rating over a 0°C to +70°C ambient temperature range.

CONNECTION DIAGRAM

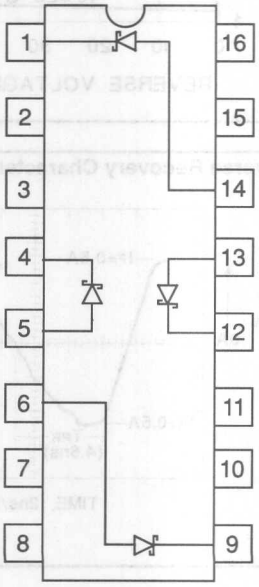
DIL-8 (TOP VIEW)
N or J Package



PLCC-20 (TOP VIEW)
Q Package



SOIC-16 (TOP VIEW)
DW Package



ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage (per Diode) 50V
Diode-to-Diode Voltage 80V
Peak Forward Current
UC1611 . . . . . 1A
UC3611 . . . . . 3A
Power Dissipation at TA = +70°C 1W
Storage Temperature Range . . . . . -65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) . . . . . +300°C

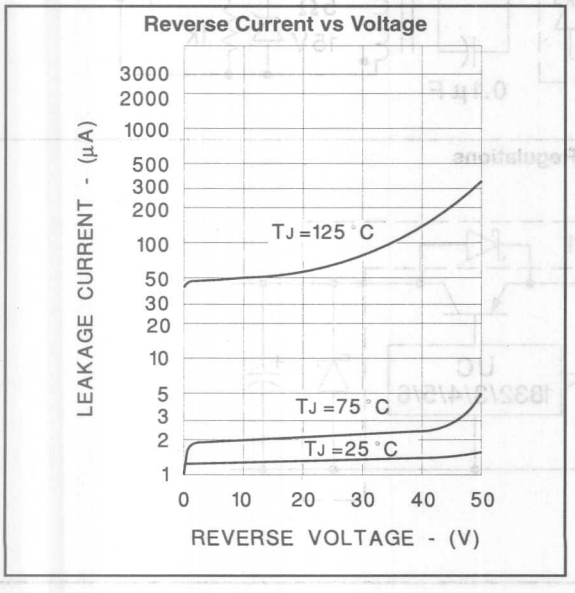
Note: Please consult Packaging Section of Databook for thermal limitations and considerations of package.

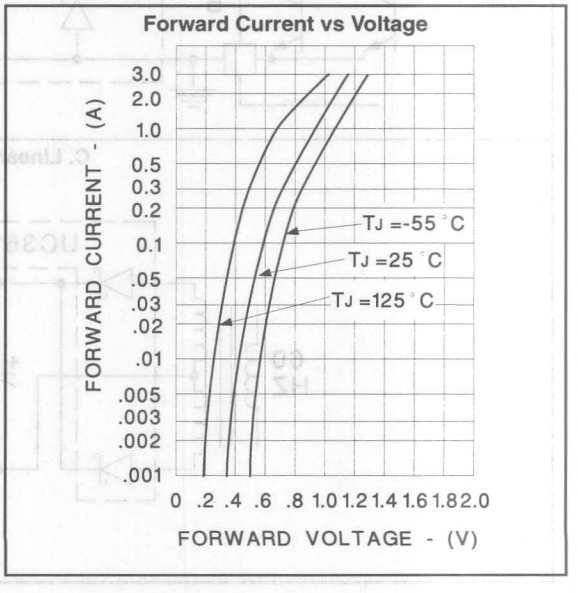
ELECTRICAL CHARACTERISTICS:

All specifications apply to each individual diode. T_J = +25°C except as noted. $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Forward Voltage Drop	I_F = 100mA	0.3	0.4	0.7	V
	I_F = 1A		0.9	1.2	V
Leakage Current	V_R = 40V		0.01	0.1	mA
	V_R = 40V, T_J = +100°C		0.1	1.0	mA
Reverse Recovery	0.5A Forward to 0.5A Reverse		20		ns
Forward Recovery	1A Forward to 1.1V Recovery		40		ns
Junction Capacitance	V_R = 5V		100		pF

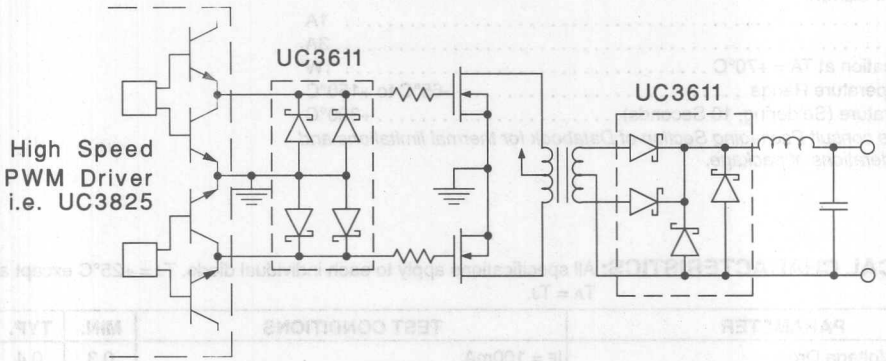
Note: At Forward currents of greater than 1.0A, a parasitic current of approximately 10mA may be collected by adjacent diodes.



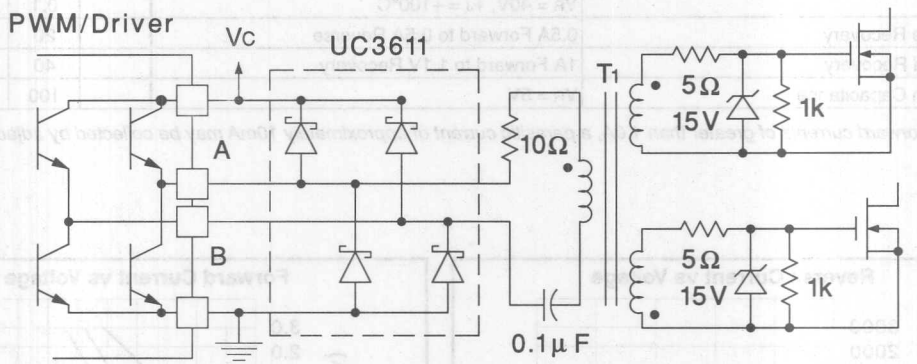


TYPICAL APPLICATIONS

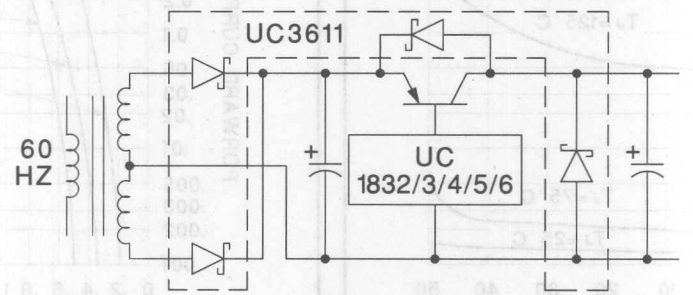
A. Clamp Diodes - PWMS and Drivers



B. Transformer Coupled Drive Circuits



C. Linear Regulations



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UNITRODE

Dual Schottky Diode

FEATURES

- Monolithic Two Diode Array
- Exceptional Efficiency
- Low Forward Voltage
- Fast Recovery Time
- High Peak Current
- Small Size

DESCRIPTION

The two-diode array is designed for high-current, low duty-cycle applications typical of flyback voltage clamping for inductive loads.

The use of Schottky diode technology features high efficiency through lowered forward voltage drop and decreased reverse recovery time.

This single monolithic chip is fabricated in hermetic CERDIP as well as copper leaded plastic MINIDIP and SOIC surface mount power pack. The UC1612 in ceramic is designed for –55°C to +125°C environments, but with reduced peak current capability; while the UC3612 has higher current rating over a 0°C to +70°C ambient temperature range.

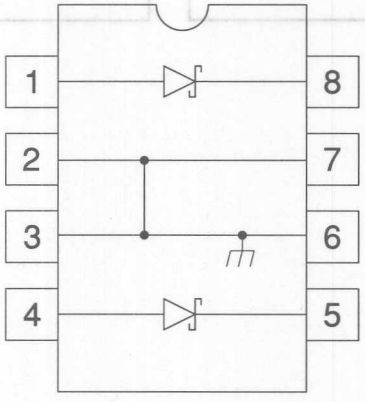
ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage (per diode) 50V
Peak Forward Current, UC3612 . . . . . .3A
Peak Forward Current, UC1612 . . . . . .1A
Storage Temperature Range . . . . . .–65°C to +150°C
Junction Temperature . . . . . .–55°C to +150°C
Lead Temperature (Soldering, 10 seconds) . . . . . .300°C

Currents are positive into, negative out of the specified terminal.
Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

DIL-8, SOIC-8
(Top View)
J, N, or DP Package



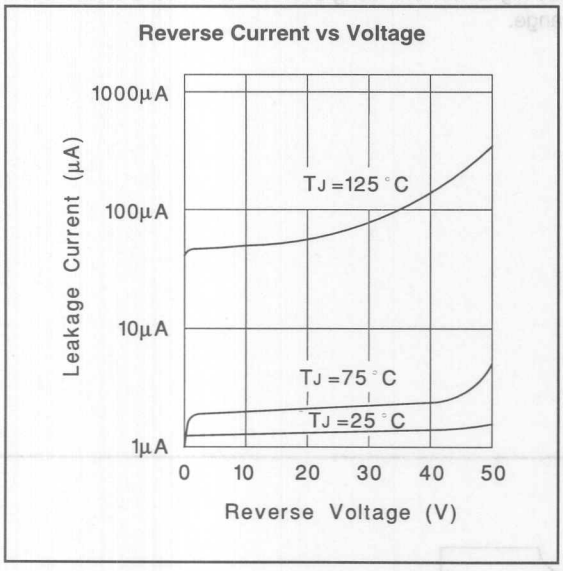
Pins 2, 3, 6, 7 are connected to substrate and must be electrically isolated.

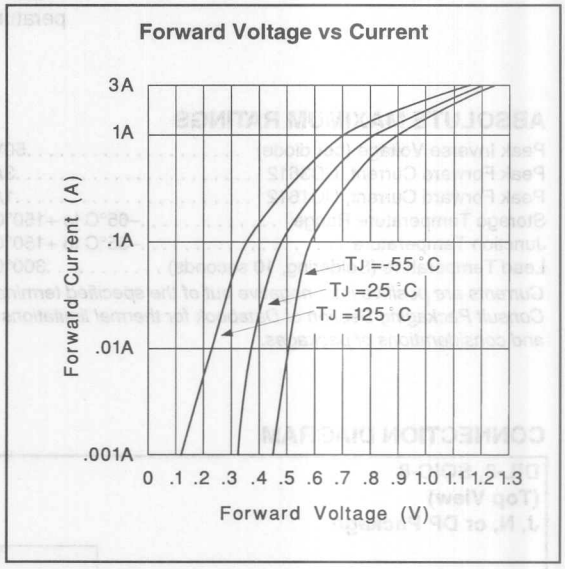
ELECTRICAL CHARACTERISTICS

All specifications apply to each individual diode. T_J = 25°C except as noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward Leakage Drop	I_F = 100mA		0.49	0.55	V
	I_F = 1A		0.9	1.0	V
Leakage Current	V_R = 40V		.01	0.1	mA
	V_R = 40V, T_J = 100°C		0.1	1.0	mA
Reverse Recovery	0.5A Forward to 0.5A Reverse		15		ns
Forward Recovery	1A Forward to 1.1V Recovery		30		ns
Junction Capacitance	V_R = 5V		70		pF

Note: At forward currents of greater than 1.0A, a parasitic current of approximately 10mA may be collected by adjacent diodes.





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Thermal Monitor

FEATURES

- On-Chip Temperature Transducer
- Temperature Comparator Gives Threshold Temperature Alarm
- Power Reference Permits Airflow Diagnostics
- Precision 2.5V Power Reference Permits Airflow Diagnostics
- Transducer Output is Easily Scaled for Increased Sensitivity
- Low 2.5mA Quiescent Current

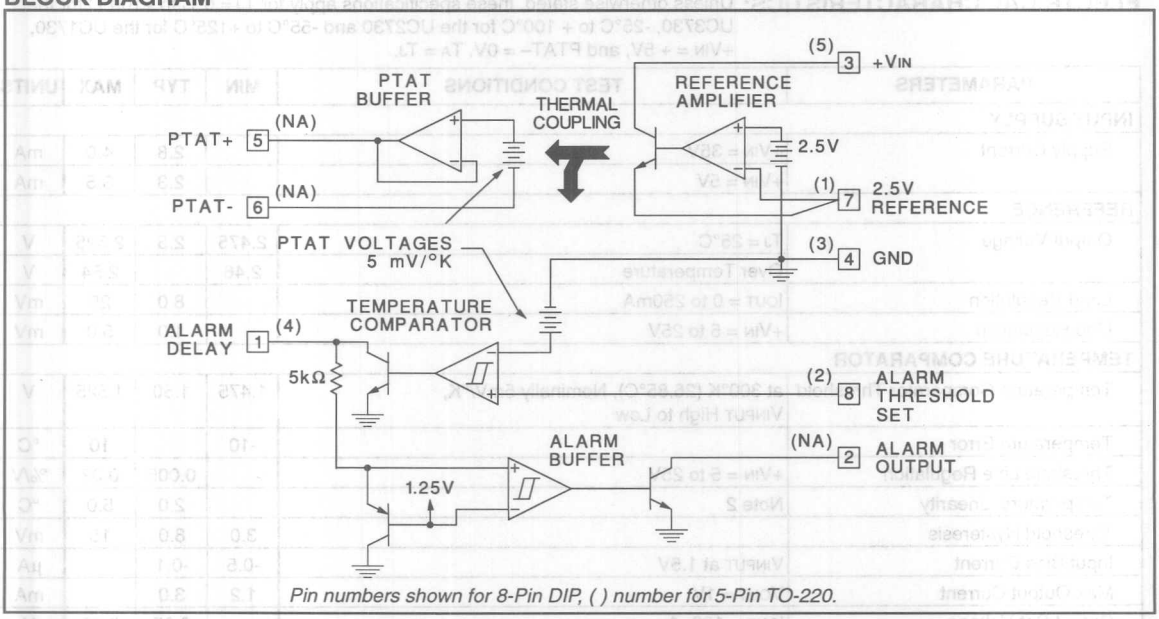
DESCRIPTION

The UC1730 family of integrated circuit devices are designed to be used in a number of thermal monitoring applications. Each IC combines a temperature transducer, precision reference, and temperature comparator allowing the device to respond with a logic output if temperatures exceed a user programmed level. The reference on these devices is capable of supplying in excess of 250mA of output current – by setting a level of power dissipation the rise in die temperature will vary with airflow past the package, allowing the IC to respond to airflow conditions

These devices come in an 8-Pin DIP, plastic or ceramic, a 5-Pin TO-220 or a PLCC-20 version. In the 8-Pin version, a PTAT (proportional to absolute temperature) output reports die temperature directly. This output is configured such that its output level can be easily scaled up with two external gain resistors. A second PTAT source is internally referenced to the temperature comparator. The other input to this comparator can then be externally programmed to set a temperature threshold. When this temperature threshold is exceeded an alarm delay output is activated. Following the activation of the delay output, a separate open collector output is turned on. The delay pin can be programmed with an external RC to provide a time separation between activation of the delay pin and the alarm pin, permitting shutdown diagnostics in applications where the open collector outputs of multiple parts are wire OR'ed together.

The 5-Pin version in the TO-220 package is well suited for monitoring heatsink temperatures. Enhanced airflow sensitivities can be obtained with this package by mounting the device to a small heatsink in the airstream. This version of the device does not include the PTAT output or the open collector alarm output.

BLOCK DIAGRAM



Pin numbers shown for 8-Pin DIP, ( ) number for 5-Pin TO-220.

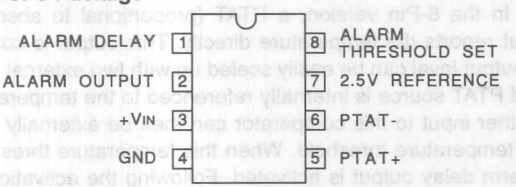
10/94

Input Supply Voltage, (+VIN) 40V
Alarm Output Voltage (8-Pin Version Only) 40V
Alarm Delay Voltage 10V
Alarm Threshold Set Voltage 10V
2.5V Reference Output Current ..... -400 mA
Alarm Output Current (8-Pin Version Only) ..... 0 mA
Power Dissipation at TA = 25°C (Note 2) ..... 1000 mW
Power Dissipation at TC = 25°C (Note 2) ..... 2000 mW
Thermal Resistance Junction to Ambient
N, 8-Pin Plastic DIP ..... 110°C/W
J, 8-Pin Ceramic DIP ..... 110°C/W
T, 5-Pin Plastic DIP TO-220 ..... 65°C/W
Thermal Resistance Junction to Case
N, 8-Pin Plastic DIP ..... 60°C/W
J, 8-Pin Ceramic DIP ..... 40°C/W
T, 5-Pin Plastic TO-220 ..... 5°C/W
Operating Junction Temperature ..... -55°C to +150°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

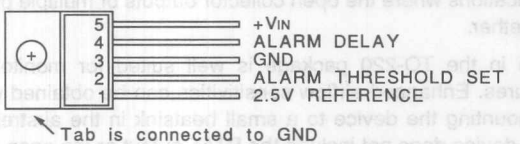
Note 1: Voltages are referenced to ground. Currents are positive into, negative out of, the specified terminals.
Note 2: Consult Packaging section of Databook for thermal limitations and considerations of package.

CONNECTION DIAGRAMS

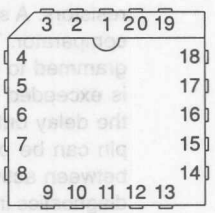
DIL-8 (TOP VIEW)
N or J Package



5-PIN TO-220 (TOP VIEW)
T Package



PLCC-20 (TOP VIEW)
Q Package



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1-3
ALARM DELAY	4
ALARM OUTPUT	5
+VIN	6
GND	7
N/C	8-13
PTAT+	14
PTAT-	15
2.5V REFERENCE	16
2.5V REFERENCE	17
ALARM THRESHOLD SET	18
N/C	19-20

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, these specifications apply for TJ = 0°C to +100°C for the UC3730, -25°C to + 100°C for the UC2730 and -55°C to +125°C for the UC1730, +VIN = + 5V, and PTAT– = 0V. TA = TJ.

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY					
Supply Current	+VIN = 35V		2.8	4.0	mA
	+VIN = 5V		2.3	3.5	mA
REFERENCE					
Output Voltage	TJ = 25°C	2.475	2.5	2.525	V
	Over Temperature	2.46		2.54	V
Load Regulation	IOUT = 0 to 250mA		8.0	25	mV
Line Regulation	+VIN = 5 to 25V		1.0	5.0	mV
TEMPERATURE COMPARATOR					
Temperature Comparator Threshold	at 300°K (26.85°C), Nominally 5mV/°K, VINPUT High to Low	1.475	1.50	1.525	V
Temperature Error		-10		10	°C
Threshold Line Regulation	+VIN = 5 to 25V		0.005	0.02	%/V
Temperature Linearity	Note 2		2.0	5.0	°C
Threshold Hysteresis		3.0	8.0	15	mV
Input Bias Current	VINPUT at 1.5V	-0.5	-0.1		µA
Max Output Current	VOUT = 1V	1.2	3.0		mA
Output Sat Voltage	IOUT = 100µA		0.05	0.25	V

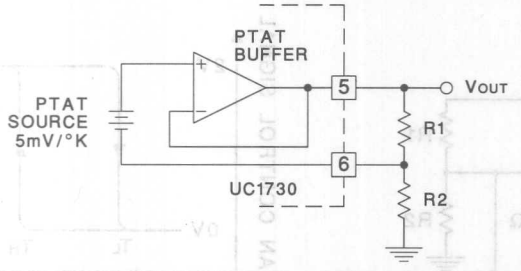
ELECTRICAL CHARACTERISTICS (cont): Unless otherwise stated, these specifications apply for T_J = 0°C to +100°C for the UC3730, -25°C to + 100°C for the UC2730 and -55°C to +125°C for the UC1730, $+V_{IN}$ = + 5V, and PTAT– = 0V. $T_A = T_J$.

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
TEMPERATURE COMPARATOR (cont.)					
Output Leakage Current	V_{OUT} = 1V		0.01	1.0	µA
PTAT BUFFER (8-Pin N, or J Version Only)					
Output Voltage	at 300°K (26.85°C), Nominally 5mV/°K	1.460	1.50	1.54	V
	In 10X Config. + V_{IN} = 25V	14.6	15	15.4	V
Temperature Error		-12		12	°C
Temperature Linearity (Note 2)			2.0	5.0	°C
Line Regulation	+V_{IN} = 5 to 25V		0.02	0.04	%/V
Load Regulation	I_{OUT} = 0 to 2mA		1.0	3.0	mV
Dropout Voltage	PTAT + TO +V_{IN}		1.9	2.5	V
Input Bias Current at PTAT– Input		-3.0	-1.0		µA
ALARM BUFFER COMPARATOR (8-Pin N, or J Version Only)					
Threshold Voltage (V_{TH})	Alarm Delay Input Low to High	1.1	1.2	1.3	V
Threshold Hysteresis Voltage	Alarm Delay Voltage > V_{TH}		100	250	mV
Input Bias Current	Alarm Delay Voltage < V_{TH}		0.1	0.5	µA
Max Output Current	V_{OUT} = 1V	7.0	15		mA
Output Sat Voltage	I_{OUT} = 3mA		0.25	0.45	V
Output Leakage	V_{OUT} = 35V		0.1	2.0	µA

Note 2: This parameter is guaranteed by design and is not tested in production.

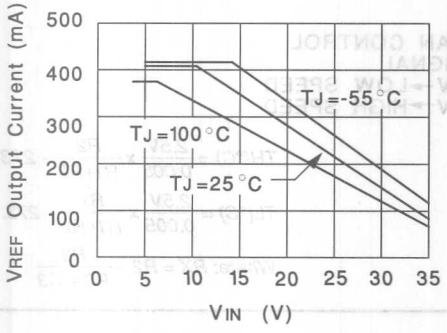
APPLICATIONS AND OPERATION INFORMATION

Scaling the PTAT Output (8 Pin Version Only)

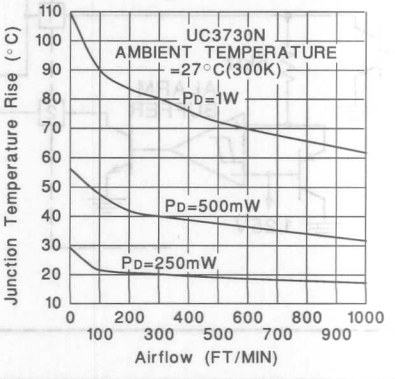


$$V_{OUT} = 5 \times \left(1 + \frac{R2}{R1}\right) mV/°K$$

(Recommended Range for R1 is 2k to 4k)



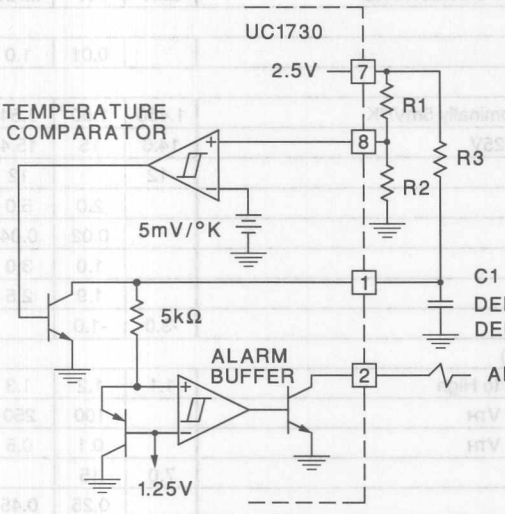
V_{REF} Maximum Output Current vs Input Supply



Junction Temperature Rise vs Airflow UC3730N (8-Pin Plastic Dip)

APPLICATIONS AND OPERATION INFORMATION (Cont.)

Setting a Temperature Threshold

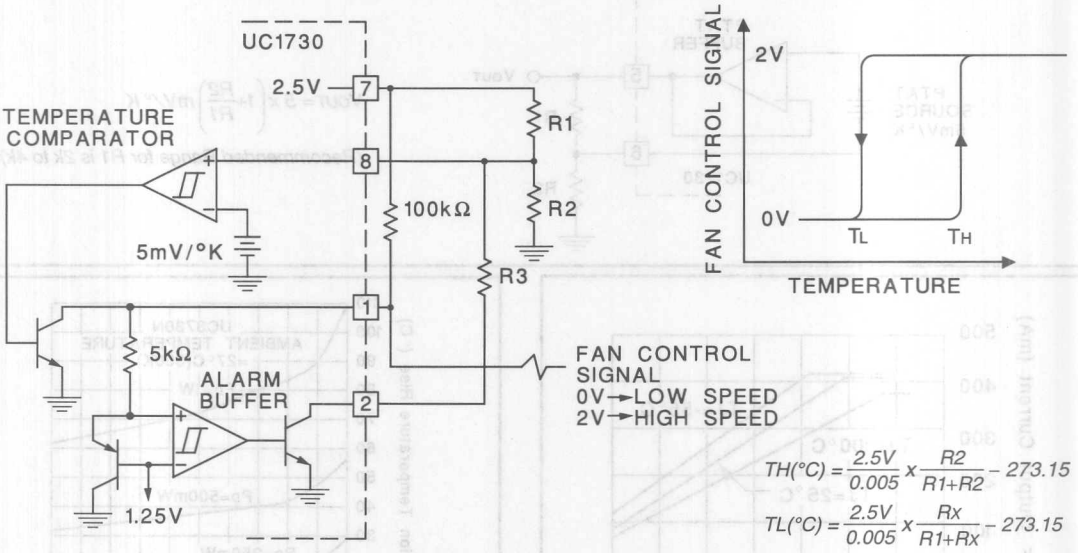


Temperature Threshold (°C)

$$= \left(\frac{2.5V}{0.005}\right) x \frac{R2}{R1+R2} - 273.15$$

Note: For airflow monitoring a power dissipation level can be set with a resistive load, R_L, on the reference output. $P_D = (+ V_{IN} - 2.5V)^2/R_L$.

Dual Speed Fan Control



$$TH(°C) = \frac{2.5V}{0.005} x \frac{R2}{R1+R2} - 273.15$$

$$TL(°C) = \frac{2.5V}{0.005} x \frac{Rx}{R1+Rx} - 273.15$$

$$\text{Where: } RX = R2 \times \frac{R3}{R2+R3}$$

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Source Ringer Controller

FEATURES

- Provides Control for Flyback Based Four Quadrant Amplifier Topology
- Onboard Sine Wave Reference with Low THD
- Selectable Ringing Frequency for Different Phone Systems (20Hz, 25Hz and 50Hz)
- Programmable Output Amplitude and DC Offset
- AC Current Limiting Supports Off Hook Detection
- DC Current Limiting for Short Circuit Protection
- Secondary Side Voltage Mode Control
- Operates from a Single 5V Supply

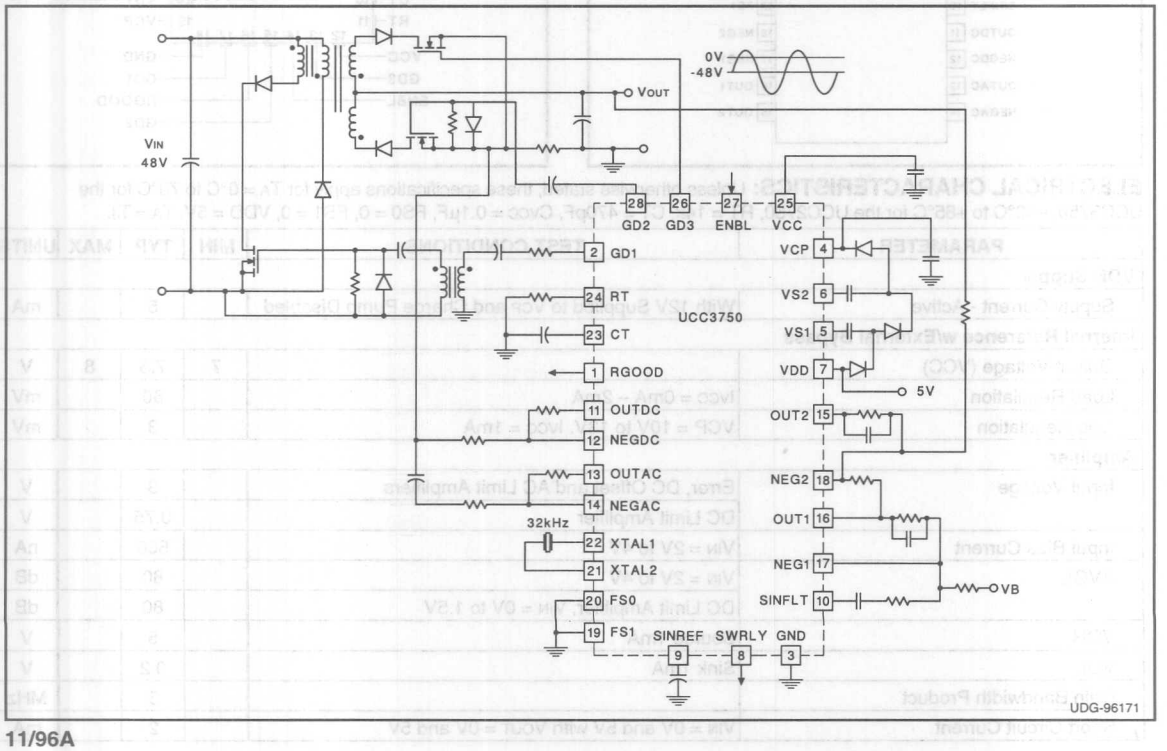
DESCRIPTION

The UCC3750 Source Ringer Controller provides a complete control and drive solution for a four quadrant flyback-based ring generator circuit. The IC controls a primary side switch, which is modulated when power transfer is taking place from input to output. It also controls two secondary switches which act as synchronous rectifier switches during positive power flow. These switches are pulse-width-modulated when the power is being delivered back to the source.

The UCC3750 has an onboard sine wave reference with programmable frequencies of 20Hz, 25Hz and 50Hz. The reference is derived from a high-frequency (32kHz) crystal connected externally. Two frequency-select pins control an internal divider to give a sinusoidal output at 20Hz, 25Hz or 50Hz. A capacitor connected at SINREF provides sufficient harmonic reduction. The ring generator can also be used at other frequencies by supplying externally generated sine-waves to the chip or by clocking the crystal input at the desired frequency.

Other features included in the UCC3750 are programmable AC and DC current limits (with buffer amplifiers), a charge-pump circuit for gate drive voltage, internal 3V and 7.5V references, a triangular clock oscillator and a buffer amplifier for adding programmable DC offset to the output voltage.

TYPICAL APPLICATION



11/96A

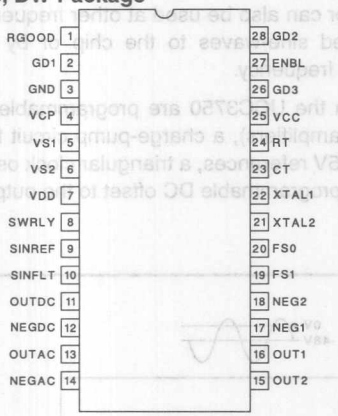
ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage
VDD 7.5V
Maximum Forced Voltage
VCP ..... –0.3V to 13.2V
VS1, VS2 ..... –0.3V to 5V
OUT1, OUT2, OUTAC, OUTDC
Maximum Forced Voltage ..... –0.3V to 7.5V
Maximum Forced Current ..... Internally Limited
NEG1, NEG2, NEGAC, NEGDC
Maximum Forced Voltage ..... –0.3V to 7.5V
SINREF, SINFLT
Maximum Forced Voltage ..... –0.3V to 7.5V
Logic Inputs
Maximum Forced Voltage ..... –0.3V to 7.5V
Reference Output Current (VCC) ..... Internally Limited
Output Current (GD1, GD2, GD3)
Pulsed 1.5A
Storage Temperature ..... –65°C to +150°C
Junction Temperature ..... –55°C to +150°C
Lead Temperature (Soldering, 10 Sec.) ..... +300°C

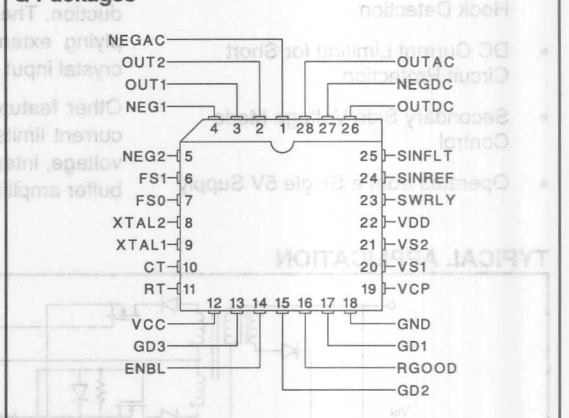
Unless otherwise indicated, voltages are reference to ground and currents are positive into, negative out of the specified terminal. Pulsed is defined as a less than 10% duty cycle with a maximum duration of 500ns. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAMS

DIL-28, SOIC- 28 (Top View)
N Package, DW Package



PLCC-28 (Top View)
Q Packages



ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C for the UCC3750, –40°C to +85°C for the UCC2750, RT = 14k, CT = 470pF, C_{VCC} = 0.1µF, FS0 = 0, FS1 = 0, VDD = 5V. $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VDD Supply					
Supply Current - Active	With 12V Supplied to V_{CP} and Charge Pump Disabled		5		mA
Internal Reference w/External Bypass					
Output Voltage (VCC)		7	7.5	8	V
Load Regulation	I_{VCC} = 0mA – 2mA		60		mV
Line Regulation	VCP = 10V to 13V, I_{VCC} = 1mA		3		mV
Amplifier					
Input Voltage	Error, DC Offset and AC Limit Amplifiers		3		V
	DC Limit Amplifier		0.75		V
Input Bias Current	V_{IN} = 2V to 4V		500		nA
AVOL	V_{IN} = 2V to 4V		80		dB
	DC Limit Amplifier, V_{IN} = 0V to 1.5V		80		dB
VOH	Source 1mA		5		V
VOL	Sink 1mA		0.2		V
Gain Bandwidth Product			3		MHz
Short Circuit Current	V_{IN} = 0V and 5V with V_{OUT} = 0V and 5V		2		mA

ELECTRICAL CHARACTERISTICS (cont.): Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C for the UCC3750, –40°C to +85°C for the UCC2750, RT = 14k, CT = 470pF, C_{VCC} = 0.1µF, FS0 = 0, FS1 = 0, VDD = 5V. T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Sine Reference					
Accuracy	T_J = 25°C, Program Frequency - Reference Frequency	–1	0	1	Hz
Total Harmonic Distortion	(Note 1)	–2		2	%
Amplitude			0.066		VCC
Offset			0.4		VCC
Oscillator					
Accuracy		108	128	148	kHz
Peak Voltage			4.75		V
Valley Voltage			3		V
Charge Pump					
Switch Pull Up Resistance (VS1, VS2)			15	30	Ω
Switch Pull Down Resistance (VS1, VS2)			15	30	Ω
Output Voltage (VCP)	VDD = 5V, I_{VCP} = 10mA		12		V
Output Drivers					
Pull Up Resistance			9	15	Ω
Pull Down Resistance			9	15	Ω
Rise Time	CL = 3nF		50	100	ns
Fall Time	CL = 3nF		50	100	ns
Current Limit					
AC Threshold Limit 1	With External Gain at 1		1.25		V
	Sine Input Attenuation		25		%
AC Threshold Limit 2	With External Gain at 1		1.5		V
	Sine Input Attenuation		50		%
AC Threshold Limit 3	With External Gain at 1		1.75		V
	Sine Input Attenuation		75		%
DC Threshold Voltage Positive	With External Gain at 3		0.5		V
DC Threshold Voltage Negative	With External Gain at 3		–0.5		V
Duty Cycle					
Maximum PWM Duty Cycle				50	%
Rectifier Duty Cycle			50		%

Note 1: Guaranteed by measuring the steps of the PWL Sine Wave.

State	% VCC	Value for VCC = 7.5	State	% VCC	Value for VCC = 7.5
0	0.3333	2.5	5	0.4255	3.191
1	0.3384	2.538	6	0.4471	3.353
2	0.3528	2.646	7	0.4616	3.462
3	0.3745	2.808	8	0.4666	3.5
4	0.4	3			

PIN DESCRIPTIONS

CT: This pin programs the internal PWM oscillator frequency. Capacitor from CT to GND sets the charge and discharge time of the oscillator.

ENBL: Logic input which enables the outputs and the charge pump when high. ENBL should be pulled low to turn the outputs off.

FS0, FS1: Frequency select pins for the internal sine-wave generator. Table 1 provides the SINREF frequencies as a function of FS0 and FS1 when a 32kHz crystal is used at the crystal inputs (XTAL1, XTAL2). Other proportional frequencies can be obtained with a different crystal. Inputs FS0 and FS1 are TTL compatible.

FS0	FS1	SINREF (Hz)
0	0	20
1	0	25
0	1	50
1	1	High Impedence

Table 1.

PIN DESCRIPTIONS (cont.)

GD1: Output driver that controls the primary side switch in a flyback converter through a gate drive transformer. The output signal on this pin is PWM during positive power transfer modes and zero during negative power transfer modes.

GD2: Output driver that controls the p-channel secondary side switch in the flyback converter. The output signal on this pin is PWM during mode 4 (Figure 2) when the reference signal is negative and power is being returned to the input. This pin functions as a synchronous rectifier output during mode 1 with positive reference signal and positive power transfer. This output is logically inverted to provide the correct polarity drive signal for a p-channel switch.

GD3: Output driver that controls the n-channel secondary side switch in the flyback converter. The output signal on this pin is PWM during mode 2 (Figure 2) when the reference signal is positive and power is being returned to the input. This pin functions as a synchronous rectifier output during mode 3 with a negative reference signal and positive power transfer.

GND: Reference point for the internal reference and all thresholds. Also provides the signal return path for all other pins.

NEG1: Inverting input of the buffer amplifier that acts as a summing junction for the DC (battery) offset voltage and sinewave reference.

NEG2: Inverting input of the error amplifier where the ringer output voltage and the reference signal with the desired offset are applied with a weighted sum. Feedback compensation is connected between NEG2 and OUT2.

NEGAC: Inverting input of the amplifier used to set the AC current limit level.

NEGDC: Inverting input of the amplifier used for DC current limiting.

OUT1: Output of the buffer amplifier that provides scaling and filtering for the reference signal before feeding it into the error amplifier. This output is also used internally to select the PWM mode for the flyback converter.

OUT2: Output of the error amplifier. Used to connect compensation components. This voltage determines the duty cycle of the PWM pulse.

OUTAC: Output node for AC current limit circuit. The AC current limit is activated and the output of SINFLT attenuated when voltage on this pin differs by more than 1.25V from the V_{CM}.

OUTDC: Output of the DC current limit amplifier. The DC current limit is activated when this pin is above 4.5V or below 1.5V.

RGOOD: Logic output that indicates that the error amplifier output is within range ($0 < D < 0.5$).

RT: Resistor from RT to GND helps set the oscillator frequency. RT programs the charge and discharge currents of CT.

SINFLT: This signal is the buffered version of SINREF. Under AC limit conditions (such as off-hook detection period), the reference signal amplitude is attenuated. This signal is summed with the DC offset level with appropriate scaling.

SINREF: This pin is the output of the sine-wave reference generator. It has a high output impedance (≈ 25kΩ). A 0.01µF capacitor to GND is recommended to provide smoothing of the sinewave. When FS0 and FS1 are both set high, the sine reference generator is disabled allowing this pin to accept an external sinewave input.

SWRLY: Logic output that leads the battery offset crossings (by typically 5ms) to allow "zero voltage" relay switching.

XTAL1: Crystal connection for external crystal.

XTAL2: Crystal connection for external crystal. This pin can be also used to clock the internal sine wave generator when XTAL1 is connected to VDD/2.

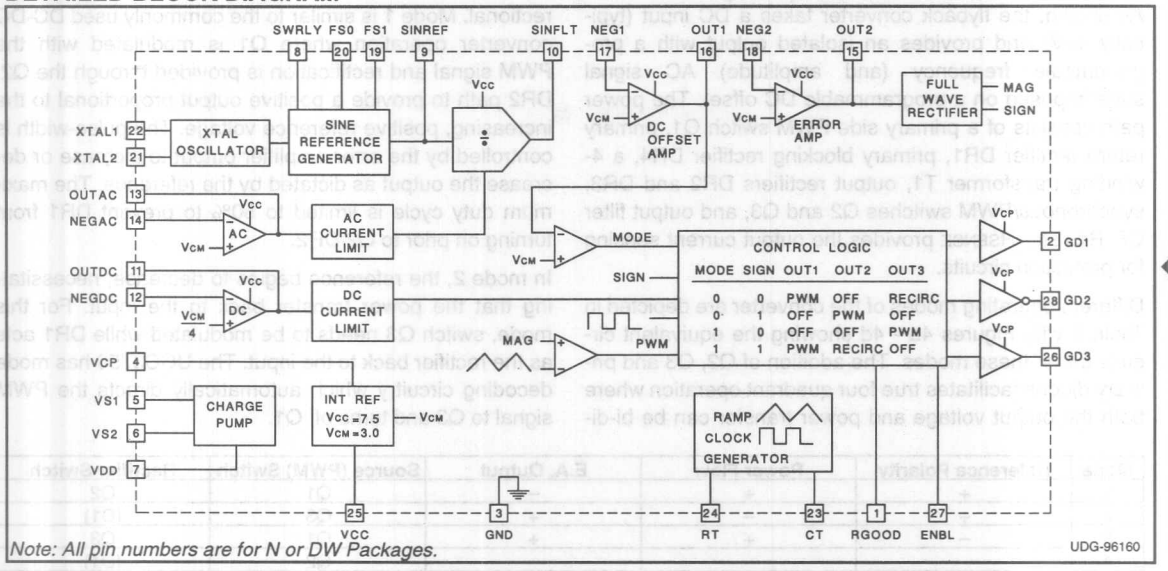
VCC: Internal 7.5V reference. For best results, bypass to GND with a ceramic capacitor(>0.1µF).

VCP: External connection for charge pump storage capacitor. A capacitance ≥ 2.2µF is recommended for low charge pump output ripple. The voltage at this pin is used by the output drivers for gate drive voltages. Alternatively, a regulated gate drive voltage can be connected at this pin while leaving the charge pump circuit at nodes VS1, VS2 disconnected.

VDD: External supply input used to bias internal logic functions. Typically a regulated 5V supply is connected between this pin and GND. It also is the input voltage for the voltage tripler circuit to generate the gate drive voltage.

VS1, VS2: Voltage switches for the voltage tripler (charge pump circuit). They provide different voltage levels to external capacitors in order to pump up the voltage from VDD to VCP.

DETAILED BLOCK DIAGRAM



Note: All pin numbers are for N or DW Packages.

APPLICATION INFORMATION

The UCC3750 provides complete control and protection functions for a four quadrant flyback converter used to generate ring signals for telephone circuits. A typical application circuit for a 15 REN ring generator is shown in Figure 1.

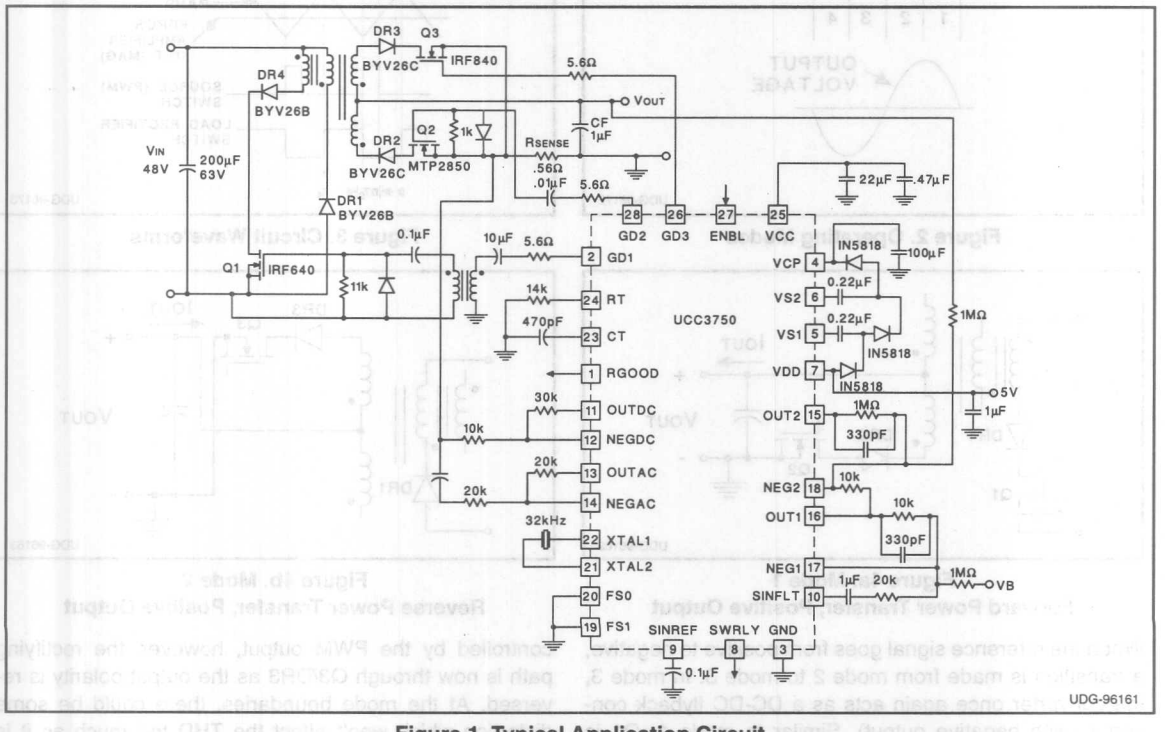


Figure 1. Typical Application Circuit

APPLICATION INFORMATION (cont.)

As shown, the flyback converter takes a DC input (typically 48V) and provides an isolated output with a programmable frequency (and amplitude) AC signal superimposed on a programmable DC offset. The power path consists of a primary side PWM switch Q1, primary return rectifier DR1, primary blocking rectifier DR4, a 4-winding transformer T1, output rectifiers DR2 and DR3, synchronous/PWM switches Q2 and Q3, and output filter CF. Resistor R_{SENSE} provides the output current sensing for protection circuits.

Different operating modes of the converter are depicted in Table 2 with Figures 4a - 4d showing the equivalent circuits under these modes. The addition of Q2, Q3 and primary diodes facilitates true four quadrant operation where both the output voltage and power transfer can be bi-directional. Mode 1 is similar to the commonly used DC-DC converter operation where Q1 is modulated with the PWM signal and rectification is provided through the Q2, DR2 path to provide a positive output proportional to the increasing, positive reference voltage. The pulse-width is controlled by the error amplifier output to increase or decrease the output as dictated by the reference. The maximum duty cycle is limited to 50% to prevent DR1 from turning on prior to Q2/DR2.

In mode 2, the reference begins to decrease, necessitating that the power transfer back to the input. For this mode, switch Q3 needs to be modulated while DR1 acts as the rectifier back to the input. The UCC3750 has mode decoding circuitry which automatically directs the PWM signal to Q3 and turns off Q1.

Mode	Reference Polarity	Power Flow	E.A. Output	Source (PWM) Switch	Rectifier Switch
1	+	+	–	Q1	Q2
2	+	–	+	Q3	(D1)
3	–	+	+	Q1	Q3
4	–	–	–	Q2	(D1)

Table 2.

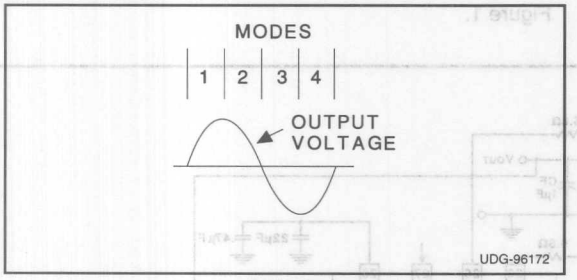


Figure 2. Operating Modes

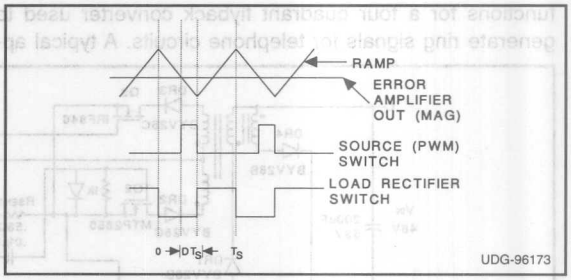


Figure 3. Circuit Waveforms

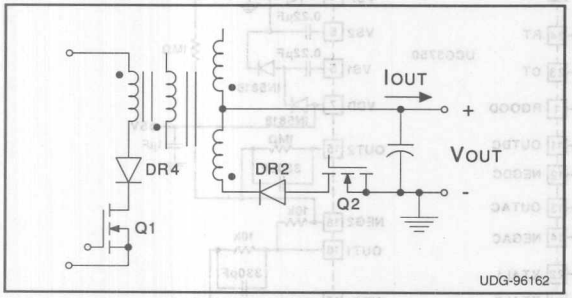


Figure 4a. Mode 1
Forward Power Transfer, Positive Output

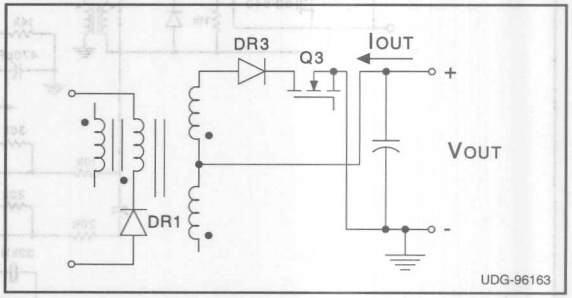


Figure 4b. Mode 2
Reverse Power Transfer, Positive Output

When the reference signal goes from positive to negative, a transition is made from mode 2 to mode 3. In mode 3, the converter once again acts as a DC-DC flyback converter (with negative output). Similar to mode 1, Q1 is controlled by the PWM output, however, the rectifying path is now through Q3/DR3 as the output polarity is reversed. At the mode boundaries, there could be some distortion which won't affect the THD too much as it is

APPLICATION INFORMATION (cont.)

near zero crossings. Finally, as the reference signal starts increasing towards zero, the direction of power transfer is again reversed and Q2 is PWMed in mode 4.

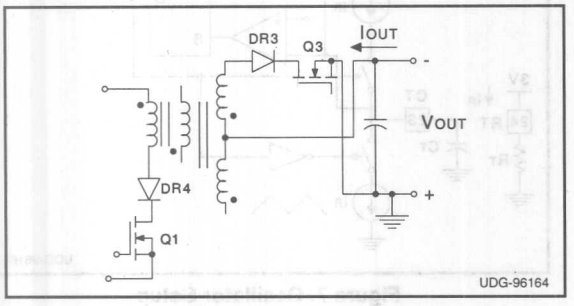


Figure 4c. Mode 3
Forward Power Transfer, Negative Output

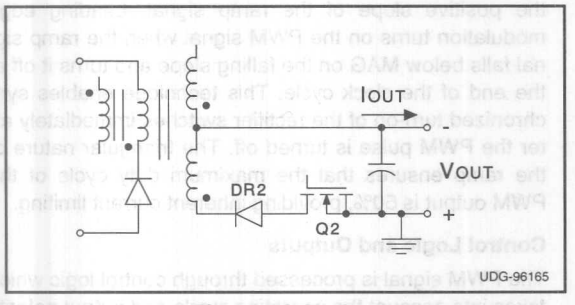


Figure 4d. Mode 4
Reverse Power Transfer, Negative Output

It should be noted that in modes 2 and 3 when the reference is decreasing, the phase of the feedback path is inverted compared to the other two modes. Traditional PWM methods will result in instability due to this characteristic. The UCC3750 separates the error signal magnitude and polarity and determines the correct PWM signal based on a separate mode determination circuit.

UCC3750 FUNCTIONAL BLOCKS

Sine Reference Generator

The IC has a versatile low frequency sinewave reference generator with low harmonic distortion and good frequency accuracy. In its intended mode as shown in Figure 5, the reference generator will take an input from a 32kHz crystal (connected between XTAL1 and XTAL2) and generate a sine-wave at 20Hz, 25Hz or 50Hz based on the programming of pins FS0 and FS1 (See Table 2). If the crystal frequency is changed, the output frequencies will be appropriately shifted. C-2 type Quartz crystals are recommended for this application. If the frequency accuracy is not a major concern, the more common and

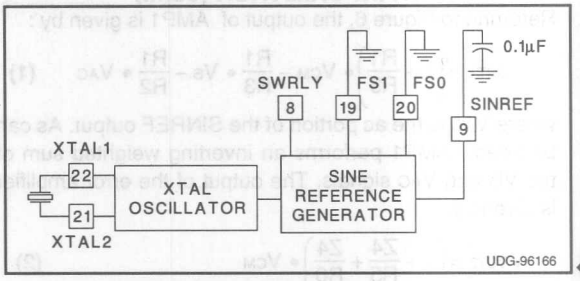


Figure 5. Sine-Wave Generator

less expensive clock crystal (C-type) at 32.768kHz can be used with a minor output frequency offset (20.5Hz instead of 20Hz). Additionally, the XTAL2 input can be clocked at a desired frequency to get a different set of output frequencies at the sine-wave output (with divide ratios of 1600, 1280 and 640). The sine-wave output is centered around an internal reference of 3V. A capacitor from SINREF to GND helps provide smoothing of the sine wave reference. Recommended value is at least 0.01µF and maximum of 0.05µF. When FS0 and FS1 are both 1 (high), the sine reference is disabled and external sine-wave can be fed into the SINREF pin. This signal should have the same DC offset as the internal sine-wave (3V).

Reference and Error Amplifier

The recommended circuit connections for these circuits are shown in Figure 6. The sine-wave reference is passed through a processing stage that attenuates it in presence of a temporary overload (such as off-hook) condition. The sine-wave is added to a DC offset to create the composite reference signal for the error amplifier. The DC reference can vary over a wide range. For pure AC outputs it is zero, while in many common applications, it is the talk battery voltage (–48V). The UCC3750 accomplishes this task by summing the two signals weighted by resisting R2 and R3. The output of AMP1 also helps determine the mode of the circuit.

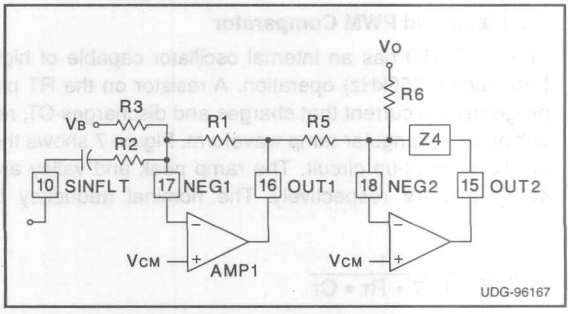


Figure 6. Error Amplifier Setup

APPLICATION INFORMATION (cont.)

Referring to Figure 6, the output of AMP1 is given by :

$$V_{OUT1} = \left(1 + \frac{R1}{R3}\right) \bullet V_{CM} - \frac{R1}{R3} \bullet V_B - \frac{R1}{R2} \bullet V_{AC} \quad (1)$$

where V_{AC} is the ac portion of the SINREF output. As can be seen, AMP1 performs an inverting weighted sum of the VB and V_{AC} signals. The output of the error amplifier is given by:

$$V_{OUT2} = \left(1 + \frac{Z4}{R5} + \frac{Z4}{R6}\right) \bullet V_{CM} \quad (2)$$

$$- \frac{Z4}{R5} \bullet V_{OUT1} - \frac{Z4}{R6} \bullet V_O$$

Substituting equation 1 into equation 2 and forcing:

$$\left(\frac{R6 \bullet R1}{R5 \bullet R3} = 1\right)$$

leads to:

$$V_O = V_B + \frac{R3}{R2} \bullet V_{AC} + \frac{R6}{Z4} \bullet (V_{CM} - V_{OUT2}) \quad (3)$$

From euation 3, it can be seen that R6 should be made low compared to Z4 to minimize effects of V_{CM} on V_O. Also, values of R1, R2 and R3 should be chosen so that signal at OUT1 is within the common mode range of AMP1.

The error amplifier compares the reference signal with the output voltage by way of weighted sum at its inverting input. The error signal is further processed to separate its polarity and magnitude. An absolute value circuit (precision full-wave rectifier) is used to get the magnitude information. The polarity is used along with the reference signal polarity to determine the mode information. The absolute value circuit provides phase inversion when appropriate for modes 2 and 3 to maintain the correct loop gain polarity. While the output of the error amplifier swings around 3V, the full-wave rectifier output (MAG) converts it into a signal above 3V. This signal is compared to the oscillator ramp to generate the PWM output.

Oscillator and PWM Comparator

The UCC3750 has an internal oscillator capable of high frequency (>250kHz) operation. A resistor on the RT pin programs the current that charges and discharges CT, resulting in a triangular ramp waveform. Figure 7 shows the oscillator hook-up circuit. The ramp peak and valley are 4.75V and 3V respectively. The nominal frequency is given by:

$$f_{OSC} = \frac{1}{1.17 \bullet R_T \bullet C_T}$$

The ramp waveform and the rectified output of the error amplifier are compared by the PWM comparator to generate the PWM signal. The PWM action is disabled on the positive slope of the ramp signal. Leading edge modulation turns on the PWM signal when the ramp signal falls below MAG on the falling slope and turns it off at the end of the clock cycle. This technique enables synchronized turn-on of the rectifier switches immediately after the PWM pulse is turned off. The triangular nature of the ramp ensures that the maximum duty cycle of the PWM output is 50%, providing inherent current limiting.

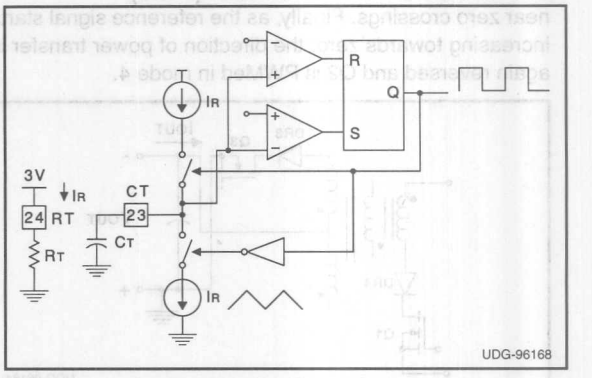


Figure 7. Oscillator Setup

Control Logic and Outputs

The PWM signal is processed through control logic which takes into account the operating mode and output polarity to determine which output to modulate. The logic table for the outputs is given in Table 2. For example, assume that the reference signal is in the first quadrant (positive and increasing). The output will lag the reference by a certain delay and hence the error amp output will be positive, resulting in SIGN = 0. The logic table indicates that GD1 is modulated during this phase allowing power transfer to increase the output voltage to keep up with the reference. Increasing error (MAG) will result in larger duty cycle and enable the output to increase and catch up with the reference. If the output becomes higher than the reference (as is likely in the second quadrant when the reference is dropping), the SIGN becomes 1 and GD3 is modulated to decrease the output level by transferring power to the input. At the boundary of the first and second quadrant, there may be some switching back and forth between modes as the reference slope crosses through zero. Some of this switching can be eliminated by judicious selection of error amplifier filtering and compensation components. In the first quadrant, when PWM is applied to Q1, Q2 is turned on in the rectifier mode by the clock signal to allow the flyback transformer flux to reset (and to transfer power to the output). Operation in quadrants 3

APPLICATION INFORMATION (cont.)

and 4 is symmetrical to the first two quadrants with Q2 and Q3 interchanged. Note that the output signal for Q2 is logically inverted to allow for driving the p-channel switch. An n-channel switch can also be used for Q2, but the drive circuit must be transformer isolated and the polarity inverted. The outputs are designed for high peak current drive and low internal impedance. In isolated systems, GD1 must be coupled to Q1 using a gate-drive transformer.

AC and DC Current Limits

In a typical ring generator application, the load increases significantly when the phone goes off-hook. Under these conditions, it is desired to maintain the output offset level and the sinusoidal shape of the AC component. To limit power consumption the amplitude of the AC signal is allowed to drop. The UCC3750 implements a unique technology to attentuate the ring signal under overload conditions while maintaining the same offset level. The amplifier titled AC tracks the AC part of the current sense signal (as shown in Figure 8) and provides some high frequency filtering. The output of this amplifier (ACOUT) is compared to internal thresholds to determine the attenuation level (if any) for the sinusoidal signal. If this output is within a ± 1.25V window of VCM, there is no attenuation of the sine-wave reference and the output is at the externally programmed AC and DC levels. Once the ACOUT goes outside 1.25V of VCM, the sine-wave reference is attenuated 25% to reduce the AC level of the output accordingly. When this pin deviates by 1.5V, the output is attenuated 50% and when ACOUT deviates beyond 1.75V, output is attenuated 75%. By programming the gain of the AC amplifier, this circuit can be made to work with any sense resistor value and is independent of DC level current limiting. The decoupling capacitor CAC provides DC decoupling and presents the AC current waveform biased around VCM to the AC amplifier. The DC current limit function provides protection against short circuit conditions by limiting the maximum current level and shutting off the PWM function when the limit point is reached.

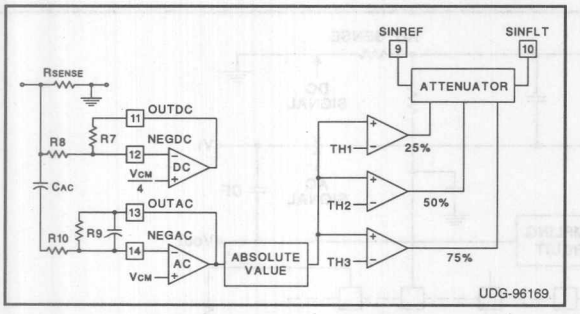


Figure 8. Current Limiting

The DC limit is activated when DC out is below 0.5 VCM or above 1.5 • VCM. The DC current limit can be programmed by setting

$$\frac{R7}{R8} = 3.$$

With this ratio, a symmetric DC limit with thresholds of ±0.5V is obtained. For other ratios, the positive and negative voltage thresholds for current sense signal are given by

$$V_{SENSE(POS)} = \frac{V_{CM}}{4} \bullet \left(1 - \frac{R8}{R7}\right)$$

$$V_{SENSE(NEG)} = \frac{V_{CM}}{4} \bullet \left(1 - \frac{5R8}{R7}\right)$$

Charge Pump and Reference

The UCC3750 is designed to work on the secondary side of an isolated power supply. It requires a 5V power supply with respect to its GND pin to operate. Note that the GND pin of the IC is also the reference point of the ring signal that is generated by the converter. If the converter output is connected in series with any other voltage, it should be ensured that the available supply voltage is referenced to the converter output return. The IC along with its associated charge pump componnents shown in Figure 9 generates all the other voltages the system requires. The UCC3750 typically requires about 5mA to operate without any loads on the drive outputs. The charge pump capacitor should be high enough to keep the VCP fairly constant when driving Q1-Q3 in the converter.

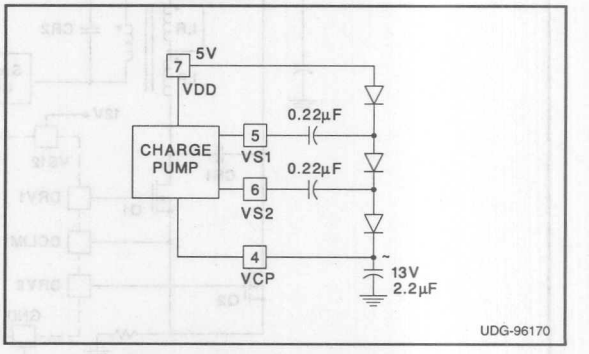


Figure 9. Charge Pump Circuits

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Single Line Ring Generator Controller

FEATURES

- Controls Novel Topology for Low Cost, Efficient Generation of Ring Voltage
- Provides DC Offset and "Talk Battery" Voltage for Off-Hook Conditions
- Selectable 20Hz, 25Hz and 50Hz Ring Frequency
- Output Current Sensing Allows Removal of AC Voltage Under Off-Hook Conditions
- Primary Current Limiting to Turn Power Stage Off Under Fault Conditions
- Operates From a Single 12V Supply

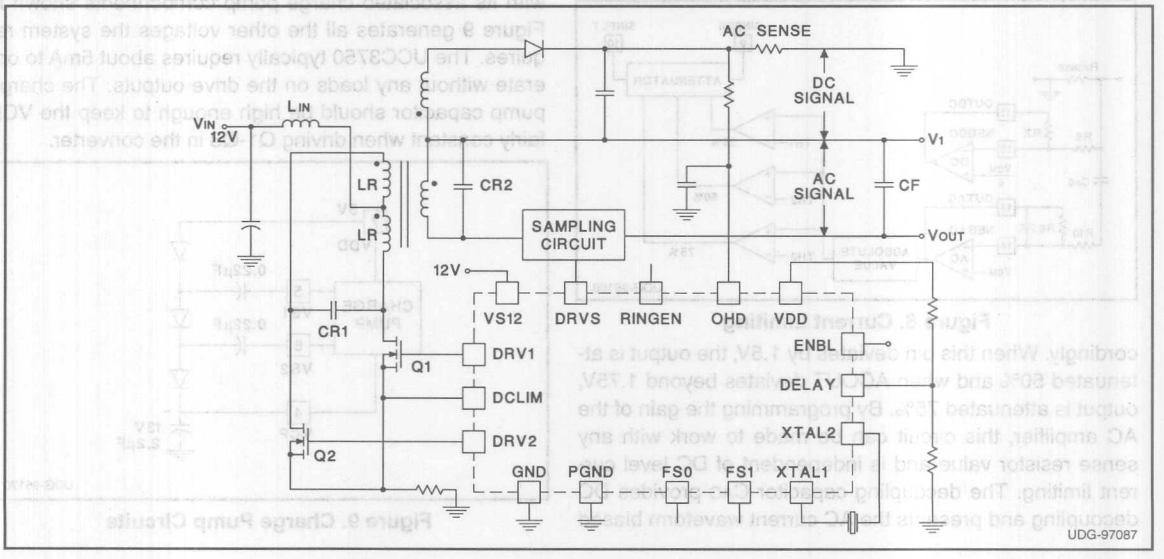
DESCRIPTION

The UCC3751 controller is designed for driving a power stage that generates low frequency, high voltage sinusoidal signals for telephone ringing applications. The controller and the power stage are most suitable for single line applications where low cost, high efficiency and minimum parts count are critical. In addition to providing the sinusoidal ringing signal, the controller and the power stage are designed to provide the required DC voltage across the output when the phone goes off-hook. The DC voltage is also added as the offset to the ringing signal. This feature eliminates the need to have a separate talk battery voltage power supply as well as relays and drivers to switch between the ringing voltage and the talk battery.

The UCC3751 directly drives primary side switches used to implement a push-pull resonant converter topology and transformer coupled sampling switches located on the secondary of the converter. For normal ring signal generation, the primary switching frequency and secondary sampling frequency are precisely offset from each other by the ringing frequency to produce a high voltage low frequency alias signal at the output. The off-hook condition is detected by sensing the output current and when a set threshold is exceeded, the sampling frequency is set to be equal to the primary switching frequency to produce a "pure" DC output. The RINGEN pin has to be asserted again to resume ringing.

The drive signal frequencies are derived from a high frequency (3579545Hz) crystal. The primary switching frequency is 89.488kHz and the sampling frequency is 20Hz, 25Hz and 50Hz less depending on the status of frequency select pins FS0 and FS1.

TYPICAL APPLICATION



UNITRODE CORPORATION
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Low-Power BiCMOS Current-Mode PWM

FEATURES

- 100µA Typical Starting Supply Current
- 500µA Typical Operating Supply Current
- Operation to 1MHz
- Internal Soft Start
- Internal Fault Soft Start
- Internal Leading-Edge Blanking of the Current Sense Signal
- 1 Amp Totem-Pole Output
- 70ns Typical Response from Current-Sense to Gate Drive Output
- 1.5% Tolerance Voltage Reference
- Same Pinout as UC3842 and UC3842A

DESCRIPTION

The UCC1800/1/2/3/4/5 family of high-speed, low-power integrated circuits contain all of the control and drive components required for off-line and DC-to-DC fixed frequency current-mode switching power supplies with minimal parts count.

These devices have the same pin configuration as the UC1842/3/4/5 family, and also offer the added features of internal full-cycle soft start and internal leading-edge blanking of the current-sense input.

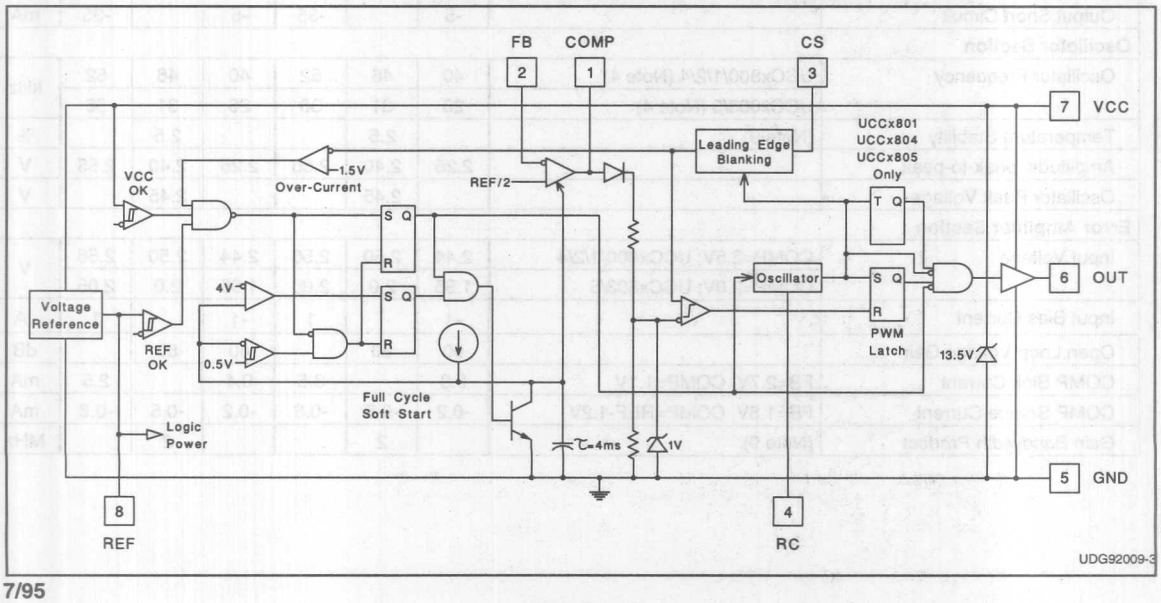
The UCC1800/1/2/3/4/5 family offers a variety of package options, temperature range options, choice of maximum duty cycle, and choice of critical voltage levels. Lower reference parts such as the UCC1803 and UCC1805 fit best into battery operated systems, while the higher reference and the higher UVLO hysteresis of the UCC1802 and UCC1804 make these ideal choices for use in off-line power supplies.

The UCC180x series is specified for operation from -55°C to +125°C, the UCC280x series is specified for operation from -40°C to +85°C, and the UCC380x series is specified for operation from 0°C to +70°C.

ORDERING INFORMATION

Part Number	Maximum Duty Cycle	Reference Voltage	Turn-On Threshold	Turn-Off Threshold
UCCx800	100%	5V	7.2V	6.9V
UCCx801	50%	5V	9.4V	7.4V
UCCx802	100%	5V	12.5V	8.3V
UCCx803	100%	4V	4.1V	3.6V
UCCx804	50%	5V	12.5V	8.3V
UCCx805	50%	4V	4.1V	3.6V

BLOCK DIAGRAM



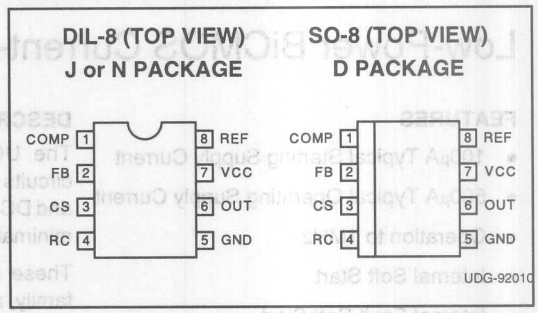
ABSOLUTE MAXIMUM RATINGS (Note 1)

VCC Voltage (Note 2) 12.0V
VCC Current 30.0mA
OUT Current ..... ±1.0A
OUT Energy (Capacitive Load) 20.0µJ
Analog Inputs (FB, CS) ..... -0.3V to 6.3V
Power Dissipation at Ta < +25°C (N or J Package) 1.0W
Power Dissipation at Ta < +25°C (D Package) 0.65W
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) ..... +300°C

Note 1: All voltages are with respect to GND. All currents are positive into the specified terminal. Consult Unitrode Integrated Circuits databook for information regarding thermal specifications and limitations of packages.

Note 2: In normal operation VCC is powered through a current limiting resistor. Absolute maximum of 12V applies when VCC is driven from a low impedance source such that ICC does not exceed 30mA.

CONNECTION DIAGRAM



ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply for -55°≤Ta≤+125°C for UCC180x; -40°≤Ta≤+85°C for UCC280x; 0°C≤Ta≤+70°C for UCC380x; VCC=10V (Note 3); RT=100k from REF to RC; CT=330pF from RC to GND; 0.1µF capacitor from VCC to GND; 0.1µF capacitor from VREF to GND. Ta=Tj.

PARAMETER	TEST CONDITIONS	UCC180X UCC280X			UCC380X			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Reference Section								
Output Voltage	Tj=+25°C, I=0.2mA, UCCx800/1/2/4	4.925	5.00	5.075	4.925	5.00	5.075	V
	Tj=+25°C, I=0.2mA, UCCx803/5	3.94	4.00	4.06	3.94	4.00	4.06	
Load Regulation	0.2mA<I<5mA		10	30		10	25	mV
Total Variation	UCCx800/1/2/4 (Note 7)	4.88	5.00	5.10	4.88	5.00	5.10	V
	UCCx803/5 (Note 7)	3.90	4.00	4.08	3.90	4.00	4.08	V
Output Noise Voltage	10Hz≤f≤10kHz, Tj=+25°C (Note 9)		70			70		µV
Long Term Stability	Ta=+125°C, 1000 Hours (Note 9)		5			5		mV
Output Short Circuit		-5		-35	-5		-35	mA
Oscillator Section								
Oscillator Frequency	UCCx800/1/2/4 (Note 4)	40	46	52	40	46	52	kHz
	UCCx803/5 (Note 4)	26	31	36	26	31	36	
Temperature Stability	(Note 9)		2.5			2.5		%
Amplitude peak-to-peak		2.25	2.40	2.55	2.25	2.40	2.55	V
Oscillator Peak Voltage			2.45			2.45		V
Error Amplifier Section								
Input Voltage	COMP=2.5V; UCCx800/1/2/4	2.44	2.50	2.56	2.44	2.50	2.56	V
	COMP=2.0V; UCCx803/5	1.95	2.0	2.05	1.95	2.0	2.05	
Input Bias Current		-1		1	-1		1	µA
Open Loop Voltage Gain		60	80		60	80		dB
COMP Sink Current	FB=2.7V, COMP=1.1V	0.3		3.5	0.4		2.5	mA
COMP Source Current	FB=1.8V, COMP=REF-1.2V	-0.2	-0.5	-0.8	-0.2	-0.5	-0.8	mA
Gain Bandwidth Product	(Note 9)		2			2		MHz

ELECTRICAL CHARACTERISTICS (cont.) Unless otherwise stated, these specifications apply for -55°≤Ta≤+125°C for UCC180x; -40°≤Ta≤+85°C for UCC280x; 0°C≤Ta≤+70°C for UCC380x; VCC=10V (Note 3); RT=100k from REF to RC; CT=330pF from RC to GND; 0.1µF capacitor from VCC to GND; 0.1µF capacitor from VREF to GND. Ta=Tj.

PARAMETER	TEST CONDITIONS	UCC180X UCC280X			UCC380X			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
PWM Section								
Maximum Duty Cycle	UCCx800/2/3	97	99	100	97	99	100	%
	UCCx801/4/5	48	49	50	48	49	50	
Minimum Duty Cycle	COMP=0V			0			0	%
Current Sense Section								
Gain	(Note 5)	1.10	1.65	1.80	1.10	1.65	1.80	V/V
Maximum Input Signal	COMP=5V (Note 6)	0.9	1.0	1.1	0.9	1.0	1.1	V
Input Bias Current		-200		200	-200		200	nA
CS Blank Time		50	100	150	50	100	150	ns
Over-Current Threshold		1.42	1.55	1.68	1.42	1.55	1.68	V
COMP to CS Offset	CS=0V	0.45	0.90	1.35	0.45	0.90	1.35	V
Output Section								
OUT Low Level	I=20mA, all parts		0.1	0.4		0.1	0.4	V
	I=200mA, all parts		0.35	0.90		0.35	0.90	
	I=50mA, VCC=5V, UCCx803/5		0.15	0.40		0.15	0.40	
	I=20mA, VCC=0V, all parts		0.7	1.2		0.7	1.2	
OUT High V_{SAT} (Vcc-OUT)	I=-20mA, all parts		0.15	0.40		0.15	0.40	V
	I=-200mA, all parts		1.0	1.9		1.0	1.9	
	I=-50mA,VCC=5V, UCCx803/5		0.4	0.9		0.4	0.9	
Rise Time	C_L=1nF		41	70		41	70	ns
Fall Time	C_L=1nF		44	75		44	75	ns
Undervoltage Lockout Section								
Start Threshold (Note 8)	UCCx800	6.6	7.2	7.8	6.6	7.2	7.8	V
	UCCx801	8.6	9.4	10.2	8.6	9.4	10.2	
	UCCx802/4	11.5	12.5	13.5	11.5	12.5	13.5	
	UCCx803/5	3.7	4.1	4.5	3.7	4.1	4.5	
Stop Threshold (Note 8)	UCCx1800	6.3	6.9	7.5	6.3	6.9	7.5	V
	UCCx1801	6.8	7.4	8.0	6.8	7.4	8.0	
	UCCx802/4	7.6	8.3	9.0	7.6	8.3	9.0	
	UCCx803/5	3.2	3.6	4.0	3.2	3.6	4.0	
Start to Stop Hysteresis	UCCx800	0.12	0.3	0.48	0.12	0.3	0.48	V
	UCCx801	1.6	2	2.4	1.6	2	2.4	
	UCCx802/4	3.5	4.2	5.1	3.5	4.2	5.1	
	UCCx803/5	0.2	0.5	0.8	0.2	0.5	0.8	
Soft Start Section								
COMP Rise Time	FB=1.8V, Rise from 0.5V to REF-1V		4			4		ms

ELECTRICAL CHARACTERISTICS (cont.) Unless otherwise stated, these specifications apply for -55°≤Ta≤+125°C for UCC180x; -40°≤Ta≤+85°C for UCC280x; 0°C≤Ta≤+70°C for UCC380x; VCC=10V (Note 3); RT=100k from REF to RC; CT=330pF from RC to GND; 0.1µF capacitor from VCC to GND; 0.1µF capacitor from VREF to GND. Ta=Tj.

PARAMETER	TEST CONDITIONS	UCC180X UCC280X			UCC380X			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Overall Section								
Start-up Current	VCC<Start Threshold		0.1	0.2		0.1	0.2	mA
Operating Supply Current	FB=0V, CS=0V, RC=0V		0.5	1.0		0.5	1.0	mA
VCC Internal Zener Voltage	ICC=10mA (Note 8)	12	13.5	15	12	13.5	15	V
VCC Internal Zener Voltage Minus Start Threshold Voltage	UCCx802/4	0.5	1.0		0.5	1.0		V

Note 3: Adjust VCC above the start threshold before setting at 10V.

Note 4: Oscillator frequency for the UCCx800, UCCx802 and UCCx803 is the output frequency. Oscillator frequency for the UCCx801, UCCx804 and UCCx805 is twice the output frequency.

Note 5: Gain is defined by: $A = \frac{\Delta V_{COMP}}{\Delta V_{CS}}$ $0 \le V_{CS} \le 0.8V$.

Note 6: Parameter measured at trip point of latch with Pin 2 at 0V.

Note 7: Total Variation includes temperature stability and load regulation.

Note 8: Start Threshold, Stop Threshold and Zener Shunt Thresholds track one another.

Note 9: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

COMP: COMP is the output of the error amplifier and the input of the PWM comparator.

Unlike other devices, the error amplifier in the UCC3800 family is a true, low output-impedance, 2MHz operational amplifier. As such, the COMP terminal can both source and sink current. However, the error amplifier is internally current limited, so that you can command zero duty cycle by externally forcing COMP to GND.

The UCC3800 family features built-in full cycle Soft Start. Soft Start is implemented as a clamp on the maximum COMP voltage.

FB: FB is the inverting input of the error amplifier. For best stability, keep FB lead length as short as possible and FB stray capacitance as small as possible.

CS: CS is the input to the current sense comparators. The UCC3800 family has two different current sense comparators: the PWM comparator and an over-current comparator.

The UCC3800 family contains digital current sense filtering, which disconnects the CS terminal from the current sense comparator during the 100ns interval immediately following the rising edge of the OUT pin. This digital filtering, also called leading-edge blanking, means that in most applications, no analog filtering (RC filter) is required on CS. Compared to an external RC filter technique, the leading-edge blanking provides a smaller effective CS to OUT propagation delay. Note, however, that the minimum non-zero On-Time of the OUT signal is directly affected by the leading-edge-blanking and the CS to OUT propagation delay.

The over-current comparator is only intended for fault sensing, and exceeding the over-current threshold will cause a soft start cycle.

RC: RC is the oscillator timing pin. For fixed frequency operation, set timing capacitor charging current by connecting a resistor from REF to RC. Set frequency by connecting a timing capacitor from RC to GND. For best performance, keep the timing capacitor lead to GND as short and direct as possible. If possible, use separate ground traces for the timing capacitor and all other functions.

The frequency of oscillation can be estimated with the following equations:

UCCx800/1/2/4: $F = \frac{1.5}{R \times C}$

UCCx803, UCCx805: $F = \frac{1.0}{R \times C}$

where frequency is in Hz, resistance is in ohms, and capacitance is in farads. The recommended range of timing resistors is between 10k and 200k and timing capacitor is 100pF to 1000pF. Never use a timing resistor less than 10k.

GND: GND is reference ground and power ground for all functions on this part.

OUT: OUT is the output of a high-current power driver capable of driving the gate of a power MOSFET with peak

PIN DESCRIPTIONS (cont.)

currents exceeding ±750mA. OUT is actively held low when VCC is below the UVLO threshold.

The high-current power driver consists of FET output devices, which can switch all of the way to GND and all of the way to VCC. The output stage also provides a very low impedance to overshoot and undershoot. This means that in many cases, external schottky clamp diodes are not required.

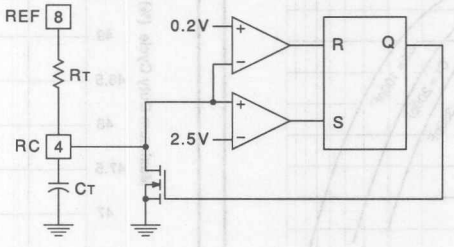
VCC: VCC is the power input connection for this device. In normal operation VCC is powered through a current limiting resistor. Although quiescent VCC current is very low, total supply current will be higher, depending on OUT current. Total VCC current is the sum of quiescent VCC current and the average OUT current. Knowing the operating frequency and the MOSFET gate charge (Qg), average OUT current can be calculated from: $I_{OUT} = Q_g \times F$.

To prevent noise problems, bypass VCC to GND with a ceramic capacitor as close to the VCC pin as possible. An electrolytic capacitor may also be used in addition to the ceramic capacitor.

REF: REF is the voltage reference for the error amplifier and also for many other functions on the IC. REF is also used as the logic power supply for high speed switching logic on the IC.

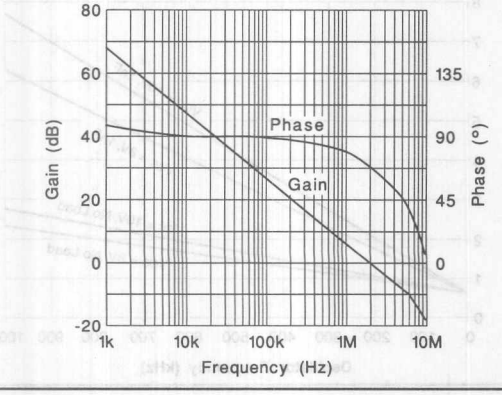
When VCC is greater than 1V and less than the UVLO threshold, REF is pulled to ground through a 5k ohm resistor. This means that REF can be used as a logic output indicating power system status. It is important for reference stability that REF is bypassed to GND with a ceramic capacitor as close to the pin as possible. An electrolytic capacitor may also be used in addition to the ceramic capacitor. A minimum of 0.1µF ceramic is required. Additional REF bypassing is required for external loads greater than 2.5mA on the reference.

OSCILLATOR

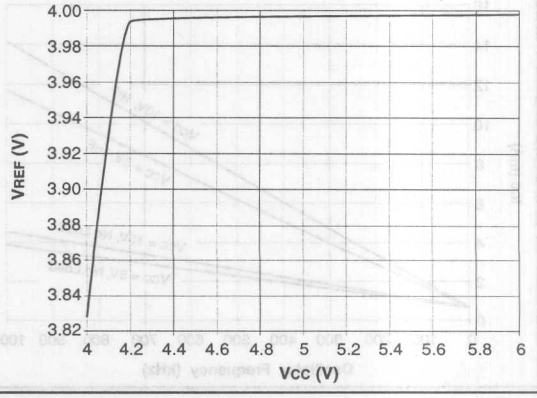


The UCC3800/1/2/3/4/5 oscillator generates a sawtooth waveform on RC. The rise time is set by the time constant of RT and CT. The fall time is set by CT and an internal transistor on-resistance of approximately 125Ω. During the fall time, the output is off and the maximum duty cycle is reduced below 50% or 100% depending on the part number. Larger timing capacitors increase the discharge time and reduce the maximum duty cycle and frequency.

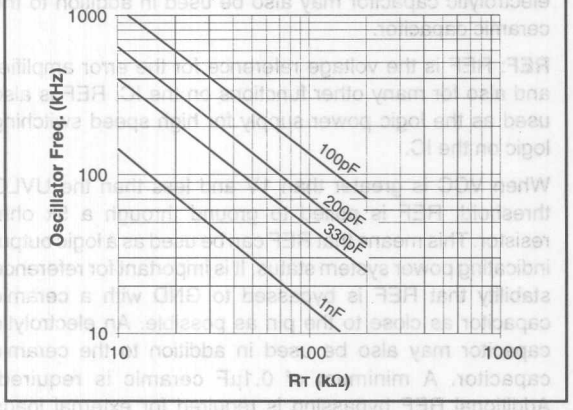
Error Amplifier Gain/Phase Response



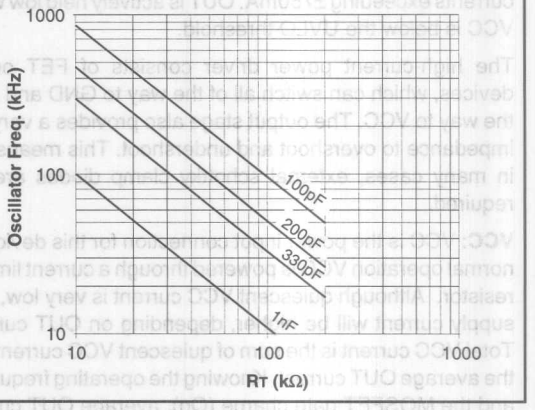
UCC1803/5 VREF vs. VCC; ILOAD = 0.5mA



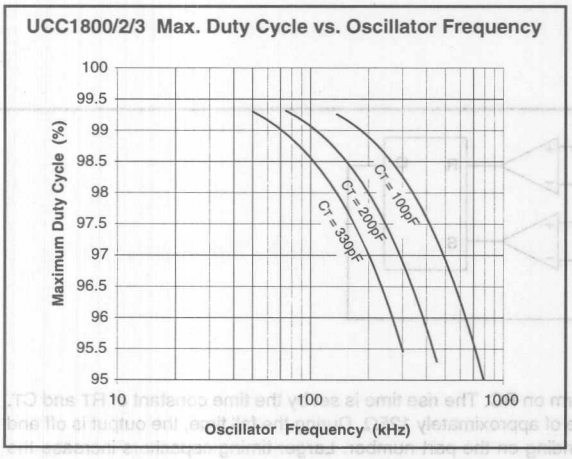
UCC1800/1/2/4 Oscillator Frequency vs. RT and CT



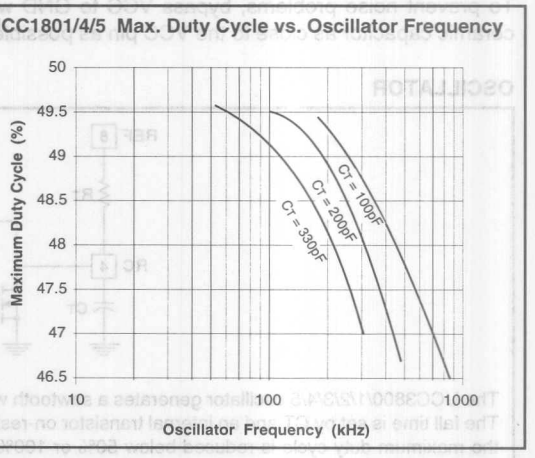
UCC1803/5 Oscillator Frequency vs. RT and CT



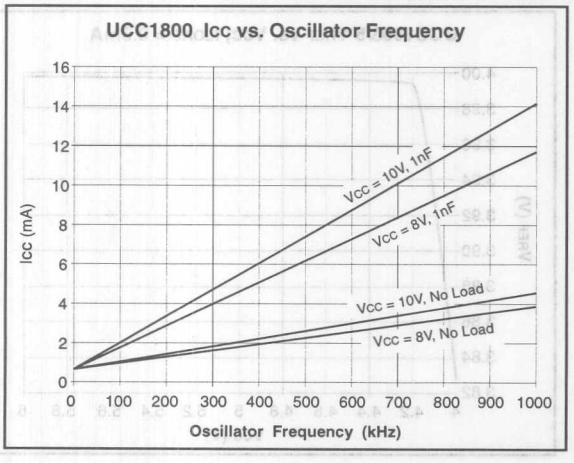
UCC1800/2/3 Max. Duty Cycle vs. Oscillator Frequency



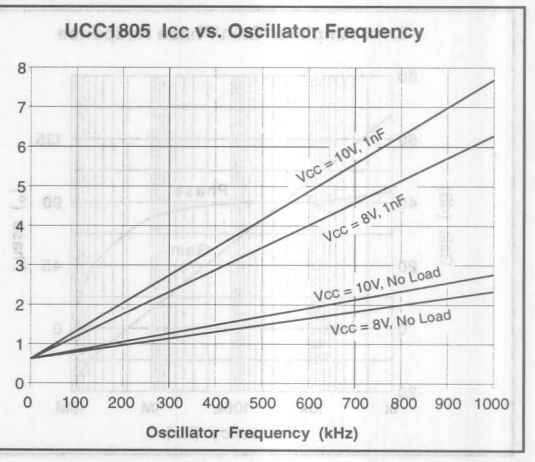
UCC1801/4/5 Max. Duty Cycle vs. Oscillator Frequency

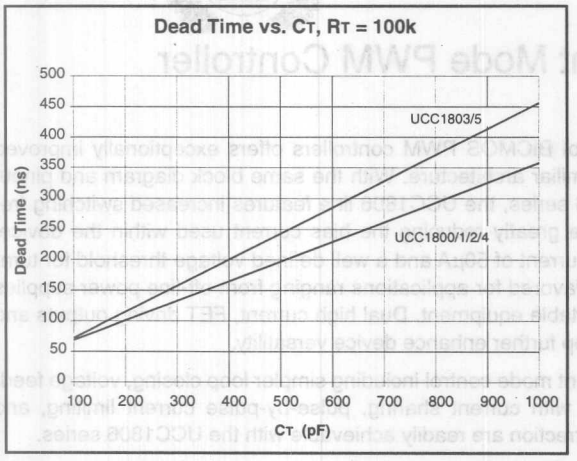


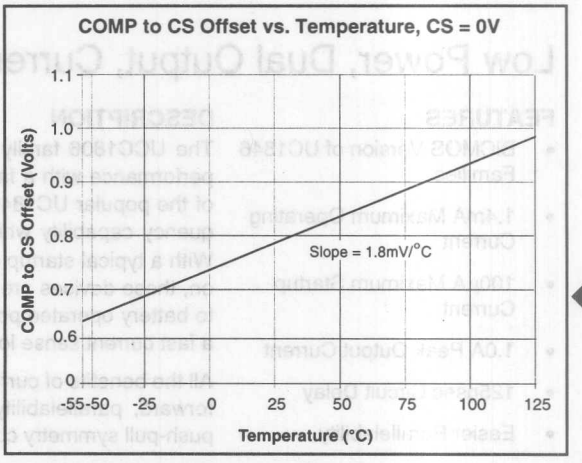
UCC1800 Icc vs. Oscillator Frequency

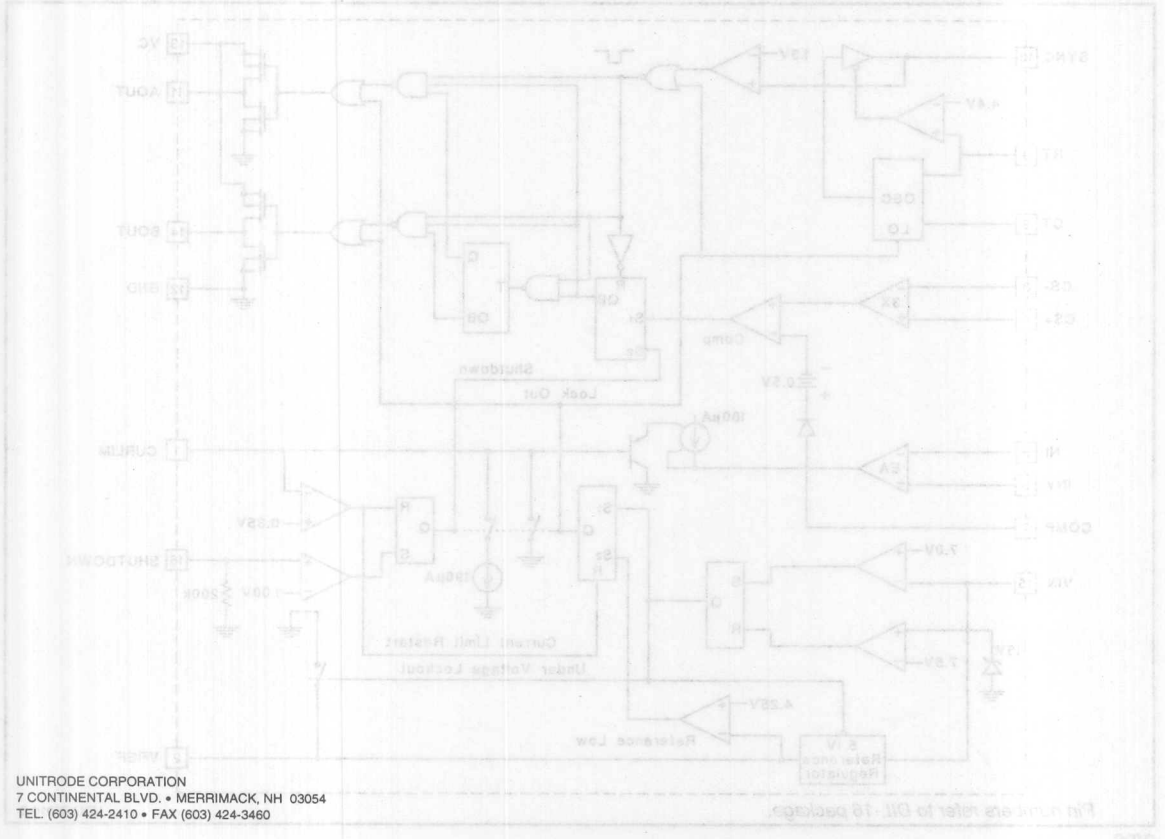


UCC1805 Icc vs. Oscillator Frequency









UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
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UNITRODE

UCC1806
UCC2806
UCC3806

Low Power, Dual Output, Current Mode PWM Controller

FEATURES

- BiCMOS Version of UC1846 Families
- 1.4mA Maximum Operating Current
- 100µA Maximum Startup Current
- 1.0A Peak Output Current
- 125nsec Circuit Delay
- Easier Parallelability
- Improved Benefits of Current Mode Control

DESCRIPTION

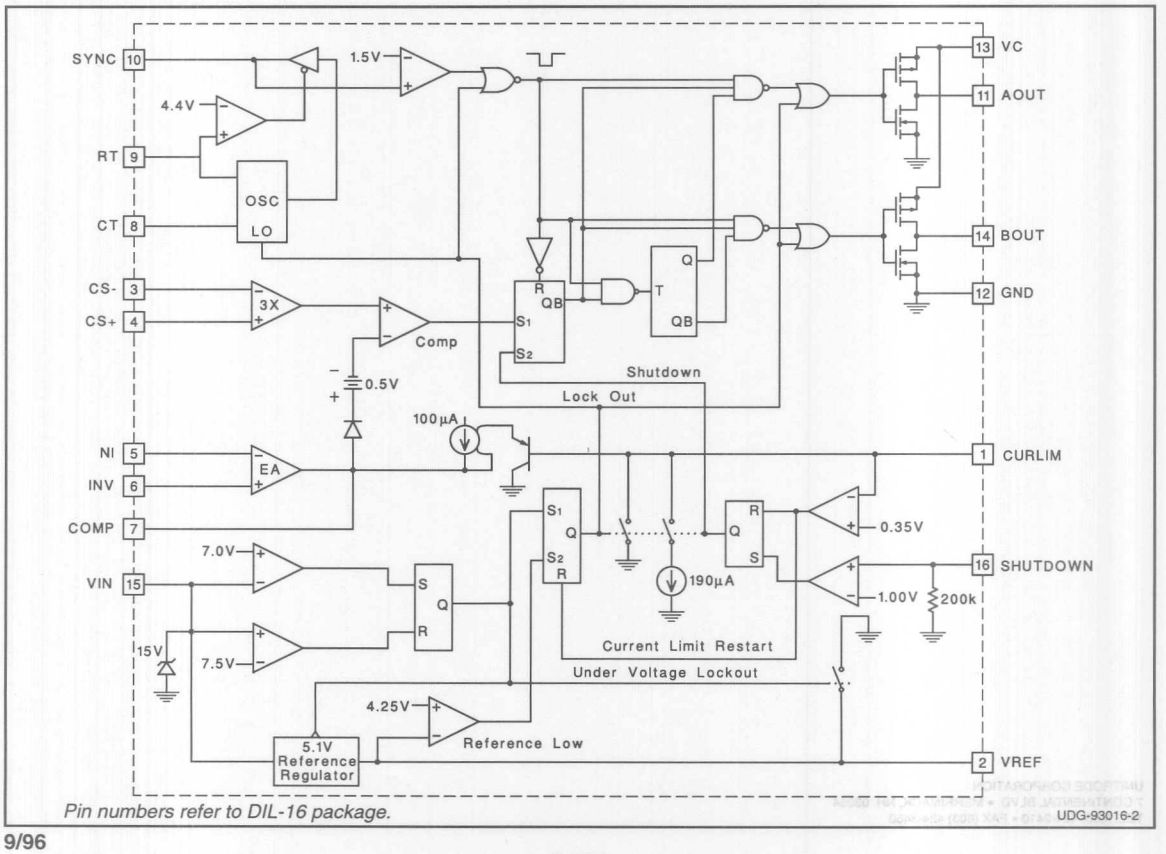
The UCC1806 family of BiCMOS PWM controllers offers exceptionally improved performance with a familiar architecture. With the same block diagram and pinout of the popular UC1846 series, the UCC1806 line features increased switching frequency capability while greatly reducing the bias current used within the device. With a typical startup current of 50µA and a well defined voltage threshold for turn-on, these devices are favored for applications ranging from off-line power supplies to battery operated portable equipment. Dual high current, FET driving outputs and a fast current sense loop further enhance device versatility.

All the benefits of current mode control including simpler loop closing, voltage feed-forward, parallelability with current sharing, pulse-by-pulse current limiting, and push-pull symmetry correction are readily achievable with the UCC1806 series.

These devices are available with multiple package options for both through-hole and surface mount applications; and in commercial, industrial, and military temperature ranges. Contact factory for availability.

The UCC1806 is specified for operation from –55°C to +125°C, the UCC2806 is specified for operation from –40°C to +85°C, and the UCC3806 is specified for operation from 0°C to +70°C. The part is available in DIP and SOIC packages.

BLOCK DIAGRAM



Pin numbers refer to DIL-16 package.

UDG-93016-2

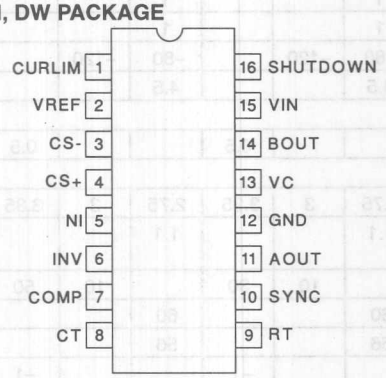
ABSOLUTE MAXIMUM RATINGS

Supply Voltage, Low Impedance (Pin 15) . . . . . +15V
Supply Current, High Impedance (Pin 15) . . . . . +25mA
Output Supply Voltage (Pin 13) . . . . . +18V
Output Current, Continuous Source or Sink. . . . . ±200mA
Output Current, Gate Drive. . . . . ±500mA
Analog Input Voltage (Pin 3, 4, 5, 6, 16). . . –0.3V to +VIN + 0.3V
Sync Output Current (Pin 10) . . . . . ±30mA
Error Amplifier Output Current (Pin 7) . +10mA/– is Self Limiting
Power Dissipation at TA = 25°C (Note 3) 1000mW
Power Dissipation at TC = 25°C (Note 3) 2000mW
Storage Temperature Range. . . . . -65°C to +150°C
Lead Temperature (soldering, 10 seconds) . . . . . +300°C

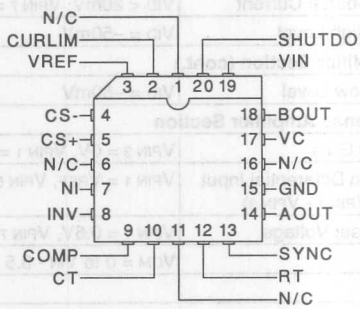
Note 1. All voltages are with respect to Ground, Pin 12.
Note 2. Currents are positive into, negative out of the specified terminal.
Note 3. Consult packaging section of databook for thermal limitations and considerations of package.
Note 4. Pin numbers refer to DIL-16 package.

CONNECTION DIAGRAMS

DIL-16 (Top View)
J or N, DW PACKAGE



PLCC-20, LCC-20 (Top View)
Q, L PACKAGE



ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications hold for TA = –55°C to +125°C for the UCC1806, –40°C to +85°C for the UCC2806, and 0°C to +70°C for the UCC3806; VIN = 12V, RT = 33k, CT = 330pF, CBYPASS on VREF = 0.01µF, TA = TJ.

PARAMETER	TEST CONDITION	UCC1806 / UCC2806			UCC3806			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Reference Section								
Output Voltage	TJ = 25°C, IO = 0.2mA	5.02	5.10	5.17	5.00	5.10	5.20	V
Load Regulation	0.2mA < IO < 5mA		3	25		3	25	mV
Temperature Stability	Note 5		0.2	0.6		0.2	0.6	mV/°C
Total Output Variation	Line, Load, Temperature (Note 7)	–150		150	–150		150	mV
Output Noise Voltage	10Hz ≤ f ≤ 10kHz, TJ = 25°C (Note 5)		70			70		µV
Long Term Stability	TA = 125°C, 1000 Hours (Note 5)		5	25		5	25	mV
Output Short Circuit		–10		–30	–10		–30	mA
Oscillator Section								
Initial Accuracy	TJ = 25°C	42	47	52	42	47	52	kHz
Temperature Stability	TMIN < TA < TMAX (Note 5)		2			2		%
Amplitude			2.35			2.35		V
Sync Delay to Outputs	Pin 8 = 0V, Pin 9 = VREF, VSYNC = 0.8V to 2.0V		50	100		50	100	ns
Discharge Current	TJ = 25°C, VPIN 8 = 2.0V		2			2		mA
Sync, VOL	IOUT = +1mA			0.4			0.4	V
Sync, VOH	IOUT = –5mA	2.4			2.4			V
Sync, VIL	Pin 8 = 0V, Pin 9 = VREF			0.8			0.8	V
Sync, VIH	Pin 8 = 0V, Pin 9 = VREF	2.0			2.0			V
Sync Input Current		–1		+1	–1		+1	µA

ELECTRICAL CHARACTERISTICS (cont.) Unless otherwise stated, these specifications hold for T_A = −55°C to +125°C for the UCC1806, −40°C to +85°C for the UCC2806, and 0°C to +70°C for the UCC3806; V_{IN} = 12V, R_T = 33k, C_T = 330pF, C_{BYPASS} on V_{REF} = 0.01µF, T_A = T_J.

PARAMETER	TEST CONDITION	UCC1806 / UCC2806			UCC3806			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Error Amplifier Section								
Input Offset Voltage				5			10	mV
Input Bias Current				−1			−1	µA
Input Offset Current				500			500	nA
Common Mode Range		0		V_{IN}−2	0		V_{IN}−2	V
Open Loop Gain	V_O = 1.0 to 4.0	80	100		80	100		dB
Unity Gain Bandwidth		1			1			MHz
Output Sink Current	V_{ID} < −20mV, $V_{PIN\ 7}$ = 1.0V	1			1			mA
Output Source Current	V_{ID} < 20mV, $V_{PIN\ 7}$ = 3.0V	−80	−120		−80	−120		µA
Output High Level	V_{ID} = −50mV	4.5			4.5			V
Error Amplifier Section (cont.)								
Output Low Level	V_{ID} = −50mV			0.5			0.5	V
Current Sense Amplifier Section								
Amplifier Gain	$V_{PIN\ 3}$ = 0V, $V_{PIN\ 1}$ = V_{REF} (Notes 3,4)	2.75	3	3.35	2.75	3	3.35	V/V
Maximum Differential Input Signal ($V_{PIN\ 4}$ - $V_{PIN\ 3}$)	$V_{PIN\ 1}$ = V_{REF}, $V_{PIN\ 5}$ = V_{REF}, $V_{PIN\ 6}$ = 0V	1.1			1.1			V
Input Offset Voltage	$V_{PIN\ 1}$ = 0.5V, $V_{PIN\ 7}$ = open		10	30		10	50	mV
CMRR	V_{CM} = 0 to V_{IN} - 3.5	60			60			dB
PSRR		56			56			dB
Input Bias Current	$V_{PIN\ 1}$ = 0.5V, Pin 7 open (Note 3)			−1			−1	µA
Input Offset Current	$V_{PIN\ 1}$ = 0.5V, Pin 7 open (Note 3)			1			1	µA
Delay to Outputs	$V_{PIN\ 5}$ = V_{REF}, Pin 6 = 0, Pin 4 - Pin 3 = 0 to 1.5V step (Note 6)		125	175		125	175	ns
Current Limit Adjust Section								
Current Limit Offset	$V_{PIN\ 3}$ = 0, $V_{PIN\ 4}$ = 0, Pin 7 = open	0.40	0.50	0.60	0.40	0.50	0.60	mV
Input Bias Current				1			1	µA
Shutdown Terminal Section								
Threshold Voltage		0.94	1.00	1.06	0.9	1.0	1.1	V
Input Voltage Range		0		V_{IN}	0		V_{IN}	V
Minimum Latching Current		300	200		300	200		µA
Maximum Non-Latching Current			200	80		200	80	µA
Delay to Outputs	$V_{PIN\ 16}$ = 0 to 1.3V		50	120		50	110	ns
Output Section								
Output Supply Voltage		2.5		15	2.5		15	V
Output Low Level	I_{SINK} = 20mA		100	200		100	200	mV
	I_{SINK} = 100mA		0.40	1.1		0.40	1.1	V
Output High Level	I_{SOURCE} = −20mA	11.6	11.9		11.6	11.9		V
	I_{SOURCE} = −100mA	11	11.6		11	11.6		V
Rise Time	T_J = 25°C, C_{LOAD} = 1000pF		35	65		35	65	ns
Fall Time	T_J = 25°C, C_{LOAD} = 1000pF		35	65		35	65	ns

ELECTRICAL CHARACTERISTICS (cont.) Unless otherwise stated, these specifications hold for T_A = –55°C to +125°C for the UCC1806, –40°C to +85°C for the UCC2806, and 0°C to +70°C for the UCC3806; V_{IN} = 12V, R_T = 33k, C_T = 330pF, C_{BYPASS} on V_{REF} = 0.01µF, T_A = T_J.

PARAMETER	TEST CONDITION	UCC1806 / UCC2806			UCC3806			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Under Voltage Lockout Section								
Startup Current	V_{IN} < Start Threshold		50	100		50	100	µA
Operating Supply Current			1	1.4		1	1.4	mA
V_{IN} Shunt Voltage	I_{VIN} = 10mA	15		17.5	15		17.5	V
Startup Threshold		6.5	7.5	8	6.5	7.5	8	V
Threshold Hysteresis			0.75			0.75		V

Note 1: All voltages are with respect to Ground, Pin 12.

Note 2: Currents are positive into, negative out of the specified terminal.

Note 3: Parameters measured at trip point of latch with $V_{PIN\ 5}$ = V_{REF}, $V_{PIN\ 6}$ = 0V.

Note 4: Amplifier gain defined as:
G = delta change at Pin 7/delta change forced at Pin 4
delta voltage at Pin 4 = 0 to 1V.

Note 5: Guaranteed by design. Not 100% tested in production.

Note 6: Current Sense Amp output is slew rate limited to provide noise immunity.

Note 7: Line Range = 9 to 15V,
Load Range = 0.2 to 5mA.

PIN DESCRIPTIONS

AOUT and BOUT: AOUT and BOUT provide alternating high current gate drive for the external MOSFETs. Duty cycle can be varied from 0 to 50% where minimum dead time is a function of CT. Both outputs use MOS transistor switches with inherent anti-parallel body diodes to clamp voltage swings to the supply rails, allowing operation without the use of clamp diodes.

COMP: COMP is the output of the error amplifier and the input of the PWM comparator. The error amplifier is a low output impedance, 2MHz operational amplifier which allows sinking or sourcing of current at the COMP pin. The error amplifier is internally current limited, so that zero duty cycle can be commanded by externally forcing COMP to GND.

CS-: CS- is the inverting input of the 3X, differential current sense amplifier.

CS+: CS+ is the non-inverting input of the 3X, differential current sense amplifier.

CT: CT is the oscillator timing capacitor connection point, which is charged by the current set by RT. CT is discharged to GND through a 2.6mA current sink. This causes a linear discharge of CT to zero volts which then initiates the next switching cycle. Dead time occurs during the discharge of CT, forcing AOUT and BOUT low. Switching frequency (fs) and dead time (td) are approximated by:

$$fs = \frac{1}{2 \bullet RT \bullet CT + td} \text{ and } td = 961 \bullet CT.$$

CURLIM: CURLIM programs the primary current limit threshold and determines whether the device will latch off or retry after an overcurrent condition. When a shutdown signal is generated, a 190µA current source to ground pulls down on CURLIM. If the voltage on the pin remains above 350mV the device remains latched and the power must be cycled to restart. If the voltage on the pin falls below 350mV, the device attempts a restart. The voltage threshold is typically set by a resistor divider from VREF to ground. To calculate the current limit adjust voltage threshold the following equations can be used;

Current Limit Adjust Latching Mode Voltage:

$$V = \frac{VREF - (R1 \bullet 300\mu A)}{1 + \frac{R1}{R2}} > 350mV$$

CurrentLimitAdjustNon-LatchingModeVoltage:

$$V = \frac{VREF - (R1 \bullet 80\mu A)}{1 + \frac{R1}{R2}} < 350mV$$

where R1 is the resistance from the VREF to CURLIM and R2 is the resistance from CURLIM to GND.

GND: GND is the reference ground and power ground for all functions of this part. Bypass and timing capacitors should be connected as close as possible to GND.

INV: INV is the inverting input of the error amplifier and has a common mode range from 0V to VIN - 2V.

NI: NI is the non-inverting input of the error amplifier and has a common mode range from 0V to VIN - 2V.

RT: RT is the connection point for the oscillator timing resistor. It has a low impedance input and is nominally at 1.25V. The current through RT is mirrored to the timing capacitor pin, CT. This causes a linear charging of CT from 0V to 2.35V. Note that the current mirror is limited to a maximum of 100µA so RT must be greater than 12.5k.

PIN DESCRIPTIONS (cont.)

SHUTDOWN: The SHUTDOWN pin is provided for enhanced protection. When SHUTDOWN is driven above 1V, AOUT and BOUT are forced low.

SYNC: SYNC is a bi-directional pin, allowing or providing external synchronization with TTL compatible thresholds. In a typical application RT is connected through a timing resistor to GND which allows the internal oscillator to free run. In this mode SYNC outputs a TTL compatible pulse during the oscillator dead time (when CT is being discharged). If RT is forced above 4.4V, SYNC acts as an input with TTL compatible thresholds and the internal oscillator is disabled. When SYNC is high, greater than 2V the outputs are held active low. When SYNC returns low, the outputs may be high until the on-time is terminated by the normal peak current signal, a fault seen at SHUTDOWN or the next high assertion of SYNC. Multiple UCC3806s can be synchronized by a single master UCC3806 or external clock.

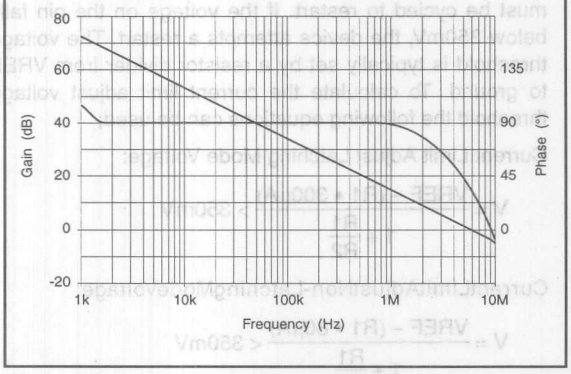
VC: VC is the input supply connection for the FET drive outputs and has an input range of 2.5V to 15V. VC should be capacitively bypassed for proper operation.

VIN: VIN is the input supply connection for this device. The UCC1806 has a maximum startup threshold of 8V and internally limited by means of a 15V shunt regulator. The shunted supply current must be limited to 2.5mA. For proper operation, VIN must be bypassed to GND with at least a 0.01µF ceramic capacitor.

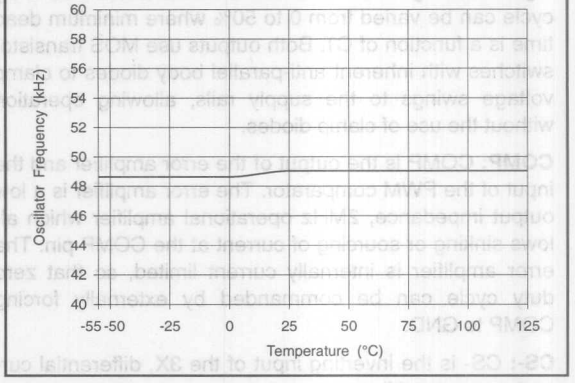
VREF: VREF is a 5.1V ±1% trimmed reference output with a 5mA maximum available current. VREF must be bypassed to GND with at least a 0.1µF ceramic capacitor for proper operation.

TYPICAL CHARACTERISTICS

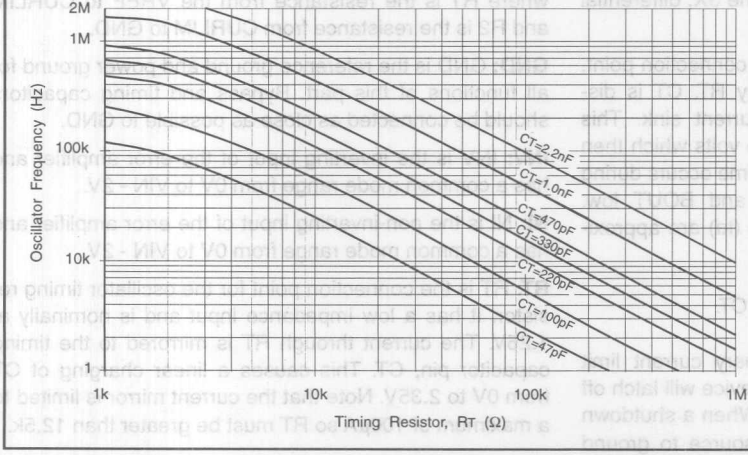
Error Amplifier Gain and Phase Response



Oscillator Frequency vs. Temperature



Oscillator Frequency vs. RT and CT



Design Equations for Oscillator:

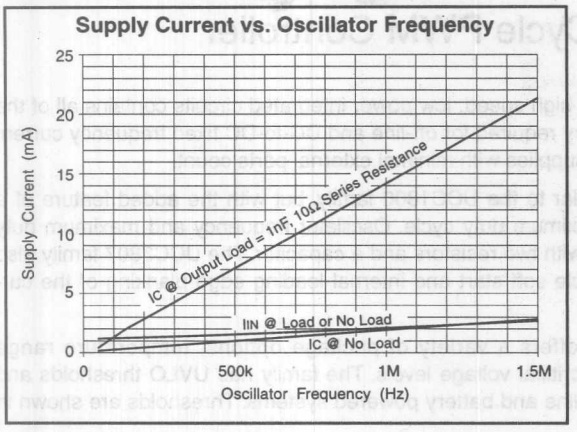
$$F_{OSC} = \frac{1}{T_{RAMP} + T_{FALL}}$$

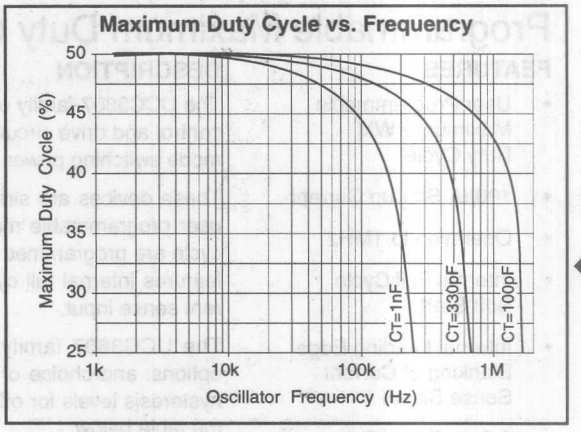
$$T_{RAMP} = 1.92 \bullet RT \bullet CT$$

$$T_{FALL} = \frac{2.4 \bullet C_T}{0.002 - \frac{1.25}{R_T}}$$

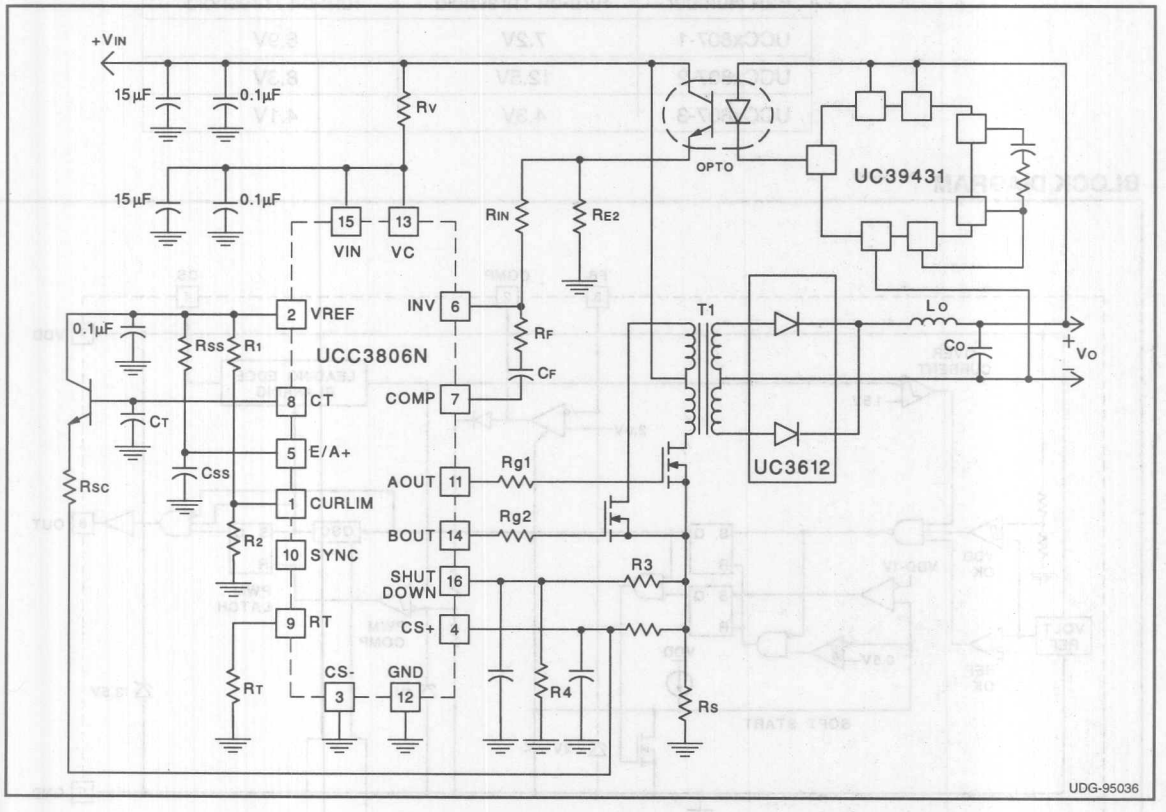
Dead Time = T_{FALL}

TYPICAL CHARACTERISTICS (cont.)





TYPICAL APPLICATION



UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
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UNITRODE

UCC1807-1/-2/-3
UCC2807-1/-2/-3
UCC3807-1/-2/-3
PRELIMINARY

Programmable Maximum Duty Cycle PWM Controller

FEATURES

- User Programmable Maximum PWM Duty Cycle
- 100µA Startup Current
- Operation to 1MHz
- Internal Full Cycle Soft Start
- Internal Leading Edge Blanking of Current Sense Signal
- 1 Amp Totem Pole Output

DESCRIPTION

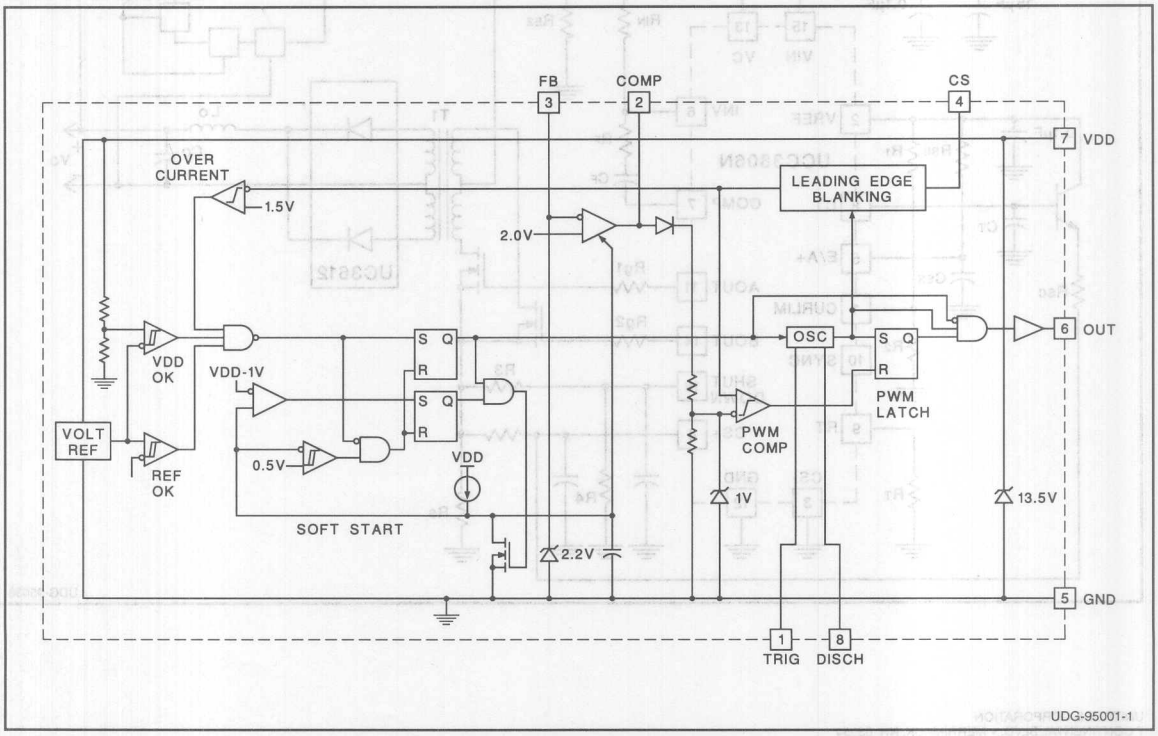
The UCC3807 family of high speed, low power integrated circuits contains all of the control and drive circuitry required for off-line and DC-to-DC fixed frequency current mode switching power supplies with minimal external parts count.

These devices are similar to the UCC1800 family, but with the added feature of a user programmable maximum duty cycle. Oscillator frequency and maximum duty cycle are programmed with two resistors and a capacitor. The UCC3807 family also features internal full cycle soft start and internal leading edge blanking of the current sense input.

The UCC3807 family offers a variety of package options, temperature range options, and choice of critical voltage levels. The family has UVLO thresholds and hysteresis levels for off-line and battery powered systems. Thresholds are shown in the table below.

Part Number	Turn-on Threshold	Turn-off Threshold
UCCx807-1	7.2V	6.9V
UCCx807-2	12.5V	8.3V
UCCx807-3	4.3V	4.1V

BLOCK DIAGRAM

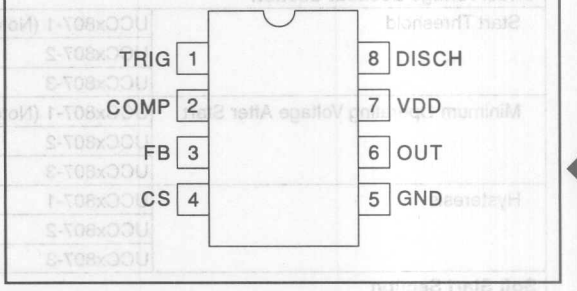


ABSOLUTE MAXIMUM RATINGS

Supply Voltage (I_{DD} ≤ 10mA) 13.5V
Supply Current 30mA
OUT Current . . . . . .±1A
Analog Inputs (FB, CS) . . . . . .–0.3V to (VDD + 0.3V)
Power Dissipation at T_A +25°C (N or J packages) 1W
Power Dissipation at T_A +25°C (D package) 0.65W
Storage Temperature . . . . . .–65°C to +150°C
Junction Temperature . . . . . .–65°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . .+300°C
All currents are positive into, negative out of the specified terminal.
Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

DIL-8, SOIC-8 (Top View)
J or N, D Packages



ORDERING INFORMATION

UCC□ 807□ – □
- UVLO Threshold
- Package
- Temperature Range

ELECTRICAL CHARACTERISTICS

Unless otherwise stated these specifications apply for T_A = –55°C to +125°C for UCC1807-1/-2/-3; –40°C to +85°C for UCC2807-1/-2/-3; and 0°C to +70°C for UCC3807-1/-2/-3; VDD = 10V, R_A = 12kΩ, R_B = 4.7kΩ, CT = 330pF, 1.0µF capacitor from VDD to GND, T_A = T_J. See Note 6.

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
Oscillator Section					
Frequency		175	202	228	kHz
Temperature Stability	(Note 5)		2.5		%
Amplitude	(Note 1)		1/3VDD		V
Error Amplifier Section					
Input Voltage	COMP = 2.0V	1.95	2.00	2.05	V
Input Bias Current		–1		1	µA
Open Loop Voltage Gain		60	80		dB
COMP Sink Current	FB = 2.2V, COMP = 1.0V	0.3	2.5		mA
COMP Source Current	FB = 1.3V, COMP = 4.0V	–0.2	–0.5		mA
PWM Section					
Maximum Duty Cycle		75	78	81	%
Minimum Duty Cycle	COMP = 0V			0	%
Current Sense Section					
Gain	(Note 2)	1.1	1.65	1.8	V/V
Maximum Input Signal	COMP = 5.0V (Note 3)	0.9	1.0	1.1	V
Input Bias Current		–200		200	nA
CS Blank Time		50	100	150	ns
Overcurrent Threshold		1.4	1.5	1.6	V
COMP to CS Offset	CS = 0V	0.55	1.1	1.65	V
Output Section					
OUT Low Level	I = 100mA		0.4	1	V
OUT High Level	I = –100mA, VDD – OUT		0.4	1	V
Rise/Fall Time	CL = 1nF (Note 5)		20	100	ns

ELECTRICAL CHARACTERISTICS (cont.) Unless otherwise stated these specifications apply for TA = −55°C to +125°C for UCC1807-1/-2/-3; −40°C to +85°C for UCC2807-1/-2/-3; and 0°C to +70°C for UCC3807-1/-2/-3; VDD = 10V, RA = 12kΩ, RB = 4.7kΩ, CT = 330pF, 1.0µF capacitor from VDD to GND, TA = TJ. See Note 6.

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
Undervoltage Lockout Section					
Start Threshold	UCCx807-1 (Note 4)	6.6	7.2	7.8	V
	UCCx807-2	11.5	12.5	13.5	V
	UCCx807-3	4.1	4.3	4.5	V
Minimum Operating Voltage After Start	UCCx807-1 (Note 4)	6.3	6.9	7.5	V
	UCCx807-2	7.6	8.3	9.0	V
	UCCx807-3	3.9	4.1	4.3	V
Hysteresis	UCCx807-1	0.1	0.3	0.5	V
	UCCx807-2	3.5	4.2	5.1	V
	UCCx807-3	0.1	0.2	0.3	V
Soft Start Section					
COMP Rise Time	FB = 1.8V, From 0.5V to 4.0V		4		ms
Overall Section					
Startup Current	VDD < Start Threshold (UCCx807-1,-3)		0.1	0.2	mA
	VDD < Start Threshold (UCCx807-2)		0.15	0.25	mA
Operating Supply Current	FB = 0V, CS = 0V, No Load (Note 7)		1.3	2.1	mA
VDD Zener Shunt Voltage	IDD = 10mA	12.0	13.5	15.0	V
Shunt to Start Difference		0.5	1.0		V

Note 1: Measured at TRIG; signal minimum = 1/3 VDD, maximum = 2/3 VDD.

Note 2: Gain is defined by: $A = \frac{\Delta V_{COMP}}{\Delta V_{CS}}$, $0 \le V_{CS} \le 0.8V$

Note 3: Parameter measured at trip point of latch with FB at 0V.
Note 4: Start Threshold and Zener Shunt thresholds track one another.
Note 5: Guaranteed by design. Not 100% tested in production.
Note 6: Adjust VDD above the start threshold before setting at 10V.
Note 7: Does not include current in external timing RC network.

PIN DESCRIPTIONS

COMP: COMP is the output of the error amplifier and the input of the PWM comparator. The error amplifier in the UCC3807 is a low output impedance, 2MHz operational amplifier. COMP can both source and sink current. The error amplifier is internally current limited, which allows zero duty cycle by externally forcing COMP to GND.

The UCC3807 family features built-in full cycle soft start. Soft start is implemented as a clamp on the maximum COMP voltage.

CS: Current sense input. There are two current sense comparators on the chip, the PWM comparator and an overcurrent comparator.

The UCC3807 also contains a leading edge blanking circuit, which disconnects the external CS signal from the current sense comparator during the 100ns interval immediately following the rising edge of the signal at the OUT pin. In most applications, no analog filtering is required on CS. Compared to an external RC filtering technique, leading edge blanking provides a smaller effective CS to OUT propagation delay. Note, however, that the minimum non-zero on-time of the OUT signal is directly affected by the leading edge blanking and the CS to OUT propagation delay.

The overcurrent comparator is only intended for fault sensing. Exceeding the overcurrent threshold causes a soft start cycle.

FB: The inverting input to the error amplifier. For best stability, keep connections to FB as short as possible and stray capacitance as small as possible.

GND: Reference ground and power ground for all functions of the part.

OUT: The output of a high current power driver capable of driving the gate of a power MOSFET with peak currents exceeding 1A. OUT is actively held low when VDD is below the UVLO threshold.

The high current power driver consists of MOSFET output devices in a totem pole configuration. This allows the output to switch from VDD to GND. The output stage also provides a very low impedance which minimizes overshoot and undershoot. In most cases, external Schottky clamp diodes are not required.

PIN DESCRIPTIONS (cont.)

TRIG/DISCH: Oscillator control pins. TRIG is the oscillator timing input, which has an RC-type charge/discharge signal controlling the chip's internal oscillator. DISCH is the pin which provides the low impedance discharge path for the external RC network during normal operation. Oscillator frequency and maximum duty cycle are computed as follows:

$$\text{frequency} \approx \frac{1.4}{(R_A + 2R_B)C_T}$$

$$\text{duty cycle} \approx \frac{R_A + R_B}{R_A + 2R_B}$$

as shown in Figure 1.

For best performance, keep the lead from C_T to GND as short as possible. A separate ground connection for C_T is desirable. The minimum value of R_A is 10kΩ, the minimum value of R_B is 2.2kΩ, and the minimum value of C_T is 47pF.

VDD: The power input connection for this device. Total VDD current is the sum of quiescent current and the average OUT current. Knowing the operating frequency and the MOSFET gate charge (Qg), average OUT current can be calculated from

$$I_{OUT} = Qg \bullet F, \text{ where F is frequency.}$$

To prevent noise problems, bypass VDD to GND with a ceramic capacitor as close to the chip as possible in parallel with an electrolytic capacitor.

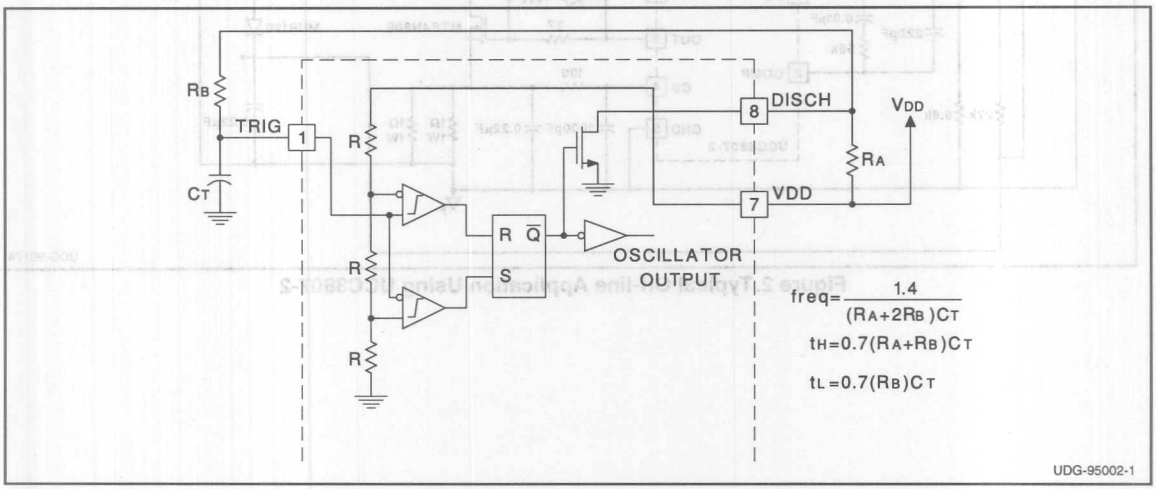


Figure 1. Oscillator Block Diagram

APPLICATIONS INFORMATION

The circuit shown in Figure 2 illustrates the use of the UCC3807 in a typical off-line application. The 100W, 200kHz, universal input forward converter produces a regulated 12VDC at 8 Amps. The programmable maximum duty cycle of the UCC3807 allows operation down to 80VRMS and up to 265VRMS with a simple RCD clamp to limit the MOSFET voltage and provide core reset. In this application the maximum duty cycle is set to about 65%. Another feature of the design is the use of a flyback winding on the output filter choke for both bootstrapping and voltage regulation. This method of loop closure eliminates the optocoupler and secondary side regulator, common to most off-line designs, while providing good line and load regulation.

T1:	
Core:	Magnetics Inc. #P-42625-UG (ungapped)
Primary:	28 turns of 2x #26AWG
Secondary:	6 turns of 50x0.2mm Litz wire
L1:	
Core:	Magnetics Inc. #P-42625-SG-37 (0.020" gap)
Main Winding:	13 turns of 2x #18AWG
Second Winding:	11 turns of #26AWG
Magnetics Inc.	
900 E. Butler Road P.O. Box 391 Butler, PA 16003 Tel: (412) 282-8282 Fax: (412) 282-6955	

APPLICATIONS INFORMATION (cont.)

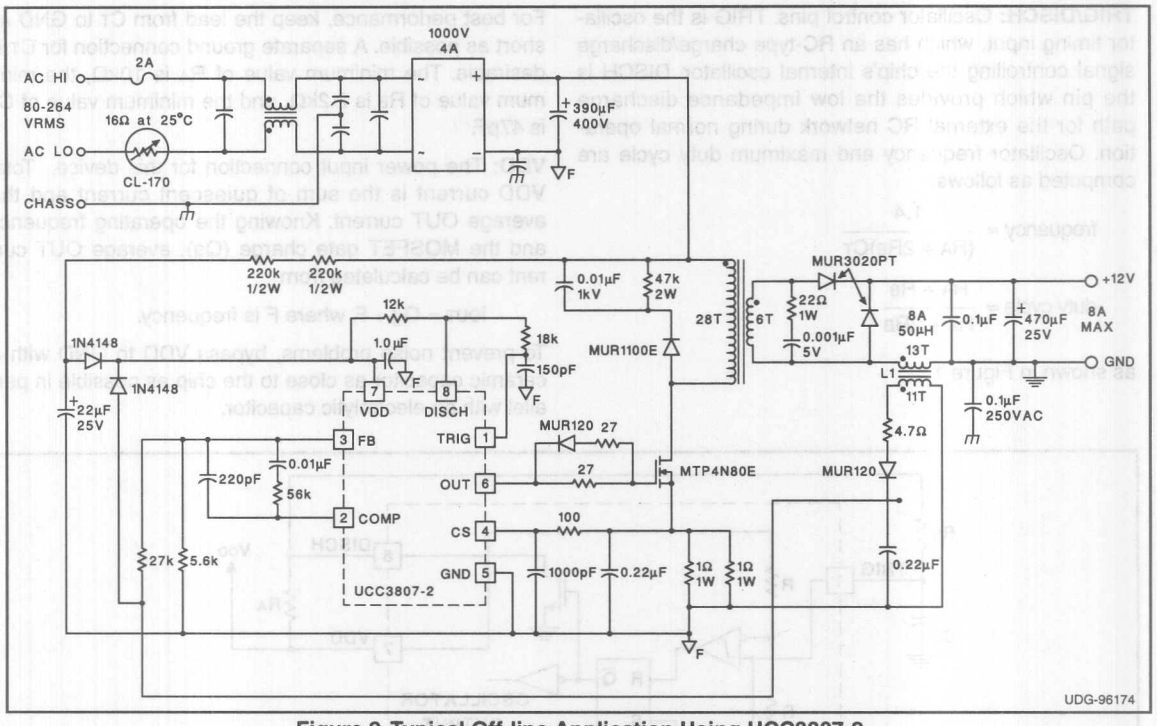


Figure 2. Typical Off-line Application Using UCC3807-2

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

UNITRODE

UCC1808-1/-2
UCC2808-1/-2
UCC3808-1/-2

PRELIMINARY

Low Power Current Mode Push-Pull PWM

FEATURES

- 130µA Typical Starting Current
- 1mA Typical Run Current
- Operation to 1MHz
- Internal Soft Start
- On Chip Error Amplifier With 2MHz Gain Bandwidth Product
- On Chip VDD Clamping
- Dual Output Drive Stages In Push-Pull Configuration
- Output Drive Stages Capable Of 500mA Peak Source Current, 1A Peak Sink Current

DESCRIPTION

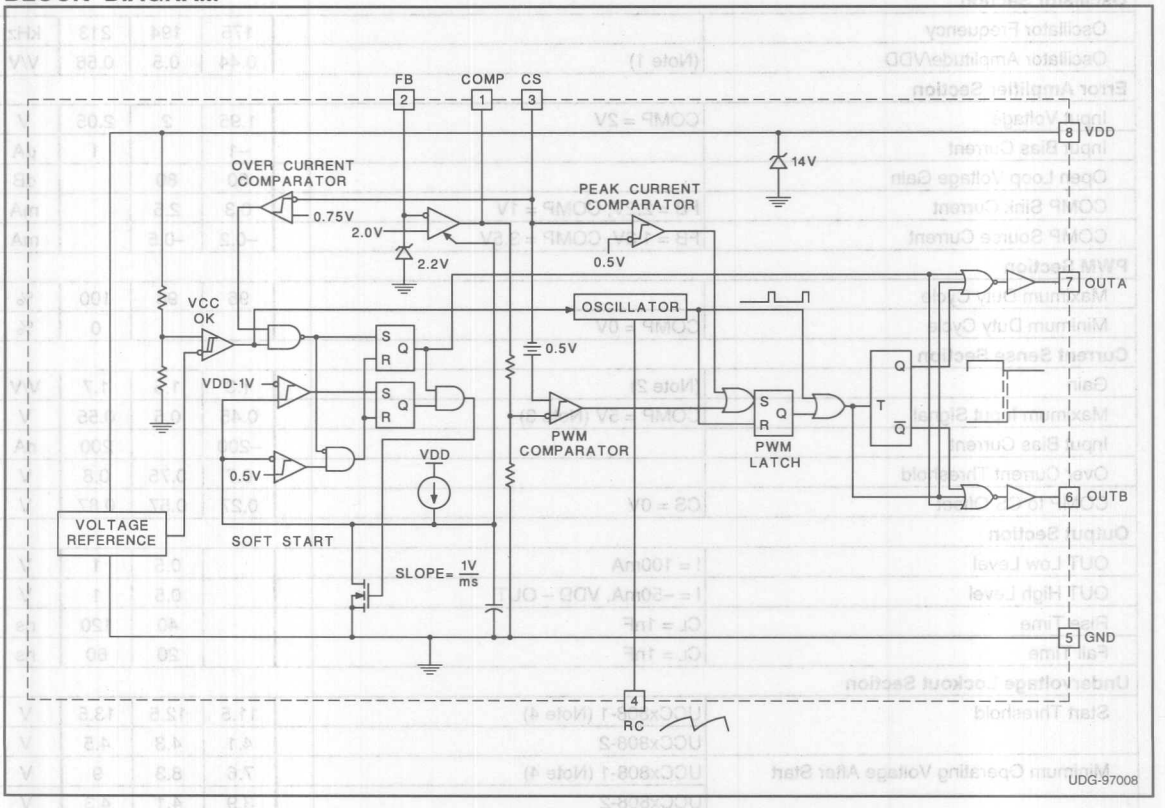
The UCC3808 is a family of BiCMOS push-pull, high-speed, low power, pulse width modulators. The UCC3808 contains all of the control and drive circuitry required for off-line or DC-to-DC fixed frequency current-mode switching power supplies with minimal external parts count.

The UCC3808 dual output drive stages are arranged in a push-pull configuration. Both outputs switch at half the oscillator frequency. A toggle flip-flop divides the oscillator frequency, thus limiting each output stage duty cycle to less than 50%.

The UCC3808 family offers a variety of package options temperature range options, and choice of undervoltage lockout levels. The family has UVLO thresholds and hysteresis options for off-line and battery powered systems. Thresholds are shown in the table below.

Part Number	Turn on Threshold	Turn off Threshold
UCCx808-1	12.5V	8.3V
UCCx808-2	4.3V	4.1V

BLOCK DIAGRAM



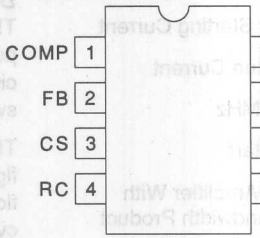
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (IDD ≤ 10mA) 15V
Supply Current 20mA
OUTA/OUTB Source Current . . . . . –500mA
OUTA/OUTB Sink Current 1000mA
Analog Inputs (FB, CS) –0.3V to VDD+0.3V, not to exceed 6V
Power Dissipation at T_A = 25°C (N Package) 1W
Power Dissipation at T_A = 25°C (D Package) 650mW
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10sec.) . . . . . +300°C

Currents are positive into, negative out of the specified terminal.
Consult Packaging Section of Databook for thermal limitations and considerations of package.

CONNECTION DIAGRAM

DIL-8, SOIC-8 (Top View)
J or N Package, D Package



ORDER INFORMATION

UCC ☐ 808 ☐ - ☐
- UVLO THRESHOLD
- PACKAGE
- TEMPERATURE RANGE

ELECTRICAL CHARACTERISTICS:

Unless otherwise specified, T_A = 0°C to 70°C for UCC3808-X, –40°C to 85°C for UCC2808-X and –55°C to 125°C UCC1808-X, VDD = 10V, 0.1µF capacitor from VDD to GND, Oscillator R = 22kΩ, C = 330pF. T_A = T_J. (Note 6)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator Section					
Oscillator Frequency		175	194	213	kHz
Oscillator Amplitude/VDD	(Note 1)	0.44	0.5	0.56	V/V
Error Amplifier Section					
Input Voltage	COMP = 2V	1.95	2	2.05	V
Input Bias Current		–1		1	µA
Open Loop Voltage Gain		60	80		dB
COMP Sink Current	FB = 2.2V, COMP = 1V	0.3	2.5		mA
COMP Source Current	FB = 1.3V, COMP = 3.5V	–0.2	–0.5		mA
PWM Section					
Maximum Duty Cycle		96	98	100	%
Minimum Duty Cycle	COMP = 0V			0	%
Current Sense Section					
Gain	(Note 2)	1.3	1.5	1.7	V/V
Maximum Input Signal	COMP = 5V (Note 3)	0.45	0.5	0.55	V
Input Bias Current		–200		200	nA
Over Current Threshold		0.7	0.75	0.8	V
COMP to CS Offset	CS = 0V	0.27	0.57	0.87	V
Output Section					
OUT Low Level	I = 100mA		0.5	1	V
OUT High Level	I = –50mA, VDD – OUT		0.5	1	V
Rise Time	C_L = 1nF		40	120	ns
Fall Time	C_L = 1nF		20	60	ns
Undervoltage Lockout Section					
Start Threshold	UCCx808-1 (Note 4)	11.5	12.5	13.5	V
	UCCx808-2	4.1	4.3	4.5	V
Minimum Operating Voltage After Start	UCCx808-1 (Note 4)	7.6	8.3	9	V
	UCCx808-2	3.9	4.1	4.3	V
Hysteresis	UCCx808-1	3.5	4.2	5.1	V
	UCCx808-2	0.1	0.2	0.3	V

ELECTRICAL CHARACTERISTICS (cont): Unless otherwise specified, T_A = 0°C to 70°C for UCC3808-X, –40°C to 85°C for UCC2808-X and –55°C to 125°C UCC1808-X, VDD = 10V, 0.1µF capacitor from VDD to GND, Oscillator R = 22kΩ, C = 330pF. $T_A = T_J$. (Note 6)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Soft Start Section					
COMP Rise Time	FB = 1.8V, Rise from 0.5V to 4V		3.5		ms
Overall Section					
Startup Current	VDD < Start Threshold		130	260	µA
Operating Supply Current	FB = 0V, CS = 0V (Note 5 and 6)		1	2	mA
VDD Zener Shunt Voltage	IDD = 10mA	13	14	15	V

Note 1: Measured at RC. Signal amplitude tracks VDD.
Note 2: Gain is defined by

$$A = \frac{\Delta V_{COMP}}{\Delta V_{CS}},\ 0 \le V_{CS} \le 0.4V.$$

Note 3: Parameter measured at trip point of latch with FB at 0V.
Note 4: Start threshold and Zener Shunt threshold track one another.
Note 5: Does not include current in the external oscillator network.
Note 6: For UCCx808-1, set VDD above the start threshold before setting at 10V.

PIN DESCRIPTIONS

COMP: COMP is the output of the error amplifier and the input of the PWM comparator. The error amplifier in the UCC3808 is a true low-output impedance, 2MHz operational amplifier. As such, the COMP pin can both source and sink current. However, the error amplifier is internally current limited, so that zero duty cycle can be externally forced by pulling COMP to GND.

The UCC3808 family features built-in full cycle soft start. Soft start is implemented as a clamp on the maximum COMP voltage.

CS: The input to the PWM and overcurrent comparators. The overcurrent comparator is only intended for fault sensing. Exceeding the overcurrent threshold will cause a soft start cycle.

FB: The inverting input to the error amplifier. For best stability, keep FB lead length as short as possible and FB stray capacitance as small as possible.

GND: Reference ground and power ground for all functions on the part.

OUTA and OUTB: Alternating high current output stages. Both stages are capable of driving the gate of a power MOSFET. Each stage is capable of 500mA peak source current, and 1A peak sink current.

The output stages switch at half the oscillator frequency, in a push/pull configuration. When the voltage on the RC pin is rising, one of the two outputs is high, but during fall time, both outputs are off. This "dead time" between the two outputs, along with a slower output rise time than fall time, insures that the two outputs can not be on at the same time. This dead time is typically 60ns to 200ns and is depended upon the values of the timing capacitor and resistor.

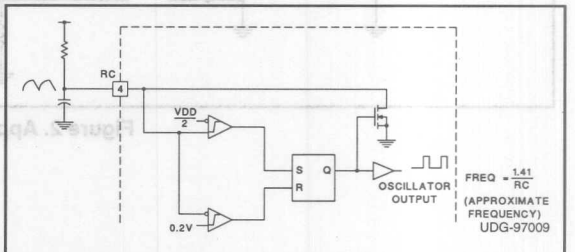
The high-current output drivers consist of MOSFET output devices, which can switch from VDD to GND. Each output stage also provides a very low impedance to overshoot and undershoot. This means that in many cases, external schottky clamp diodes are not required.

RC: The oscillator programming pin. The UCC3808's oscillator tracks VDD and GND internally, so that variations in power supply rails minimally affect frequency stability. Figure 1 shows the oscillator block diagram.

Only two components are required to program the oscillator, a resistor (tied to the VDD and RC), and a capacitor (tied to the RC and GND). The approximate oscillator frequency is determined by the simple formula

$$f_{OSCILLATOR} = \frac{1.41}{RC}$$

where frequency is in Hertz, resistance in Ohms, and ca-



The oscillator generates a sawtooth waveform on RC. During the RC rise time, the output stages alternate on time, but both stages are off during the RC fall time.

The output stages switch at 1/2 the oscillator frequency, with guaranteed duty cycle of < 50% for both ouputs.

Figure 1. Block Diagram for Oscillator

PIN DESCRIPTION (cont.)

pacitance in Farads. The recommended range of timing resistors is between 10kΩ and 200kΩ and range of timing capacitors is between 100pF and 1000pF. Timing resistors less than 10kΩ must never be used.

For best performance, keep the timing capacitor lead to GND as short as possible, the timing resistor lead from VDD as short as possible, and the leads between timing components and RC as short as possible. Separate ground and VDD traces to the external timing network are encouraged.

VDD: The power input connection for this device. Although quiescent VDD current is very low, total supply current will be higher, depending on OUTA and OUTB current, and the programmed oscillator frequency. Total VDD current is the sum of quiescent VDD current and the average OUT current. Knowing the operating frequency and the MOSFET gate charge (Qg), average OUT current can be calculated from

$$I_{OUT} = Qg \bullet F, \text{ where F is frequency.}$$

To prevent noise problems, bypass VDD to GND with a ceramic capacitor as close to the chip as possible along with an electrolytic capacitor.

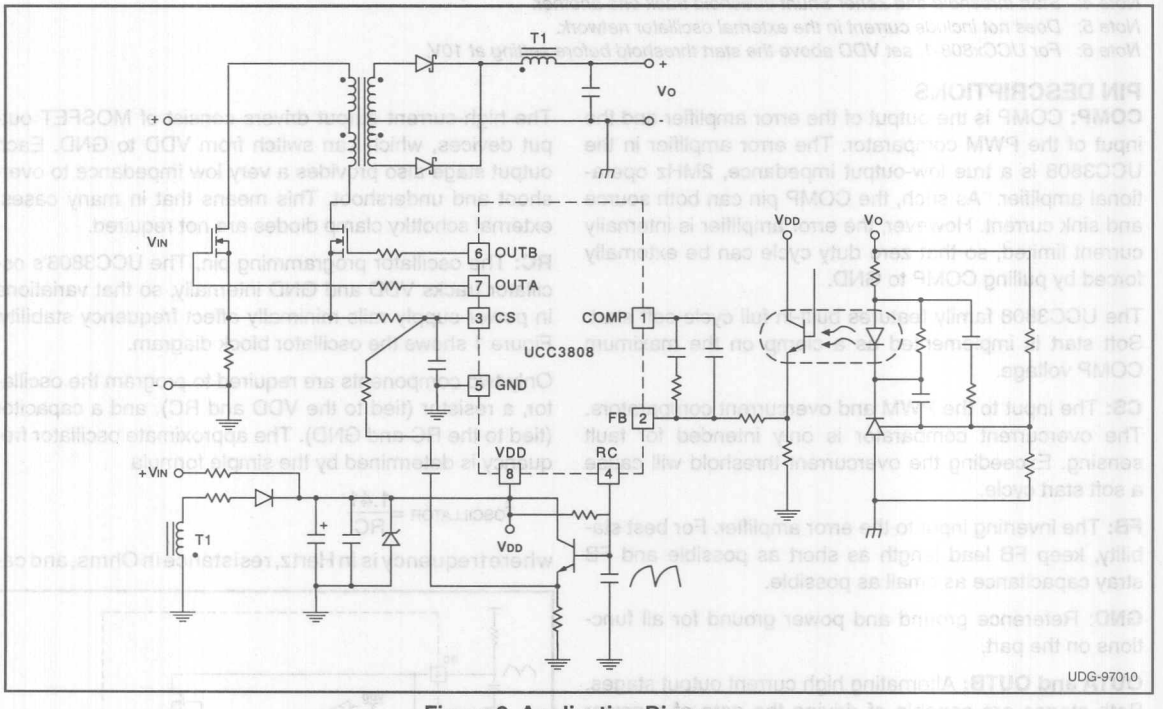


Figure 2. Application Diagram

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UNITRODE

UCC1809-1/-2
UCC2809-1/-2
UCC3809-1/-2

PRELIMINARY

Economy Primary Side Controller

FEATURES

- User Programmable Soft Start With Active Low Shutdown
- User Programmable Maximum Duty Cycle
- Accessible 5V Reference
- Undervoltage Lockout
- Operation to 1MHz
- 0.4A Source/1A Sink FET Driver
- Low 100µA Startup Current

DESCRIPTION

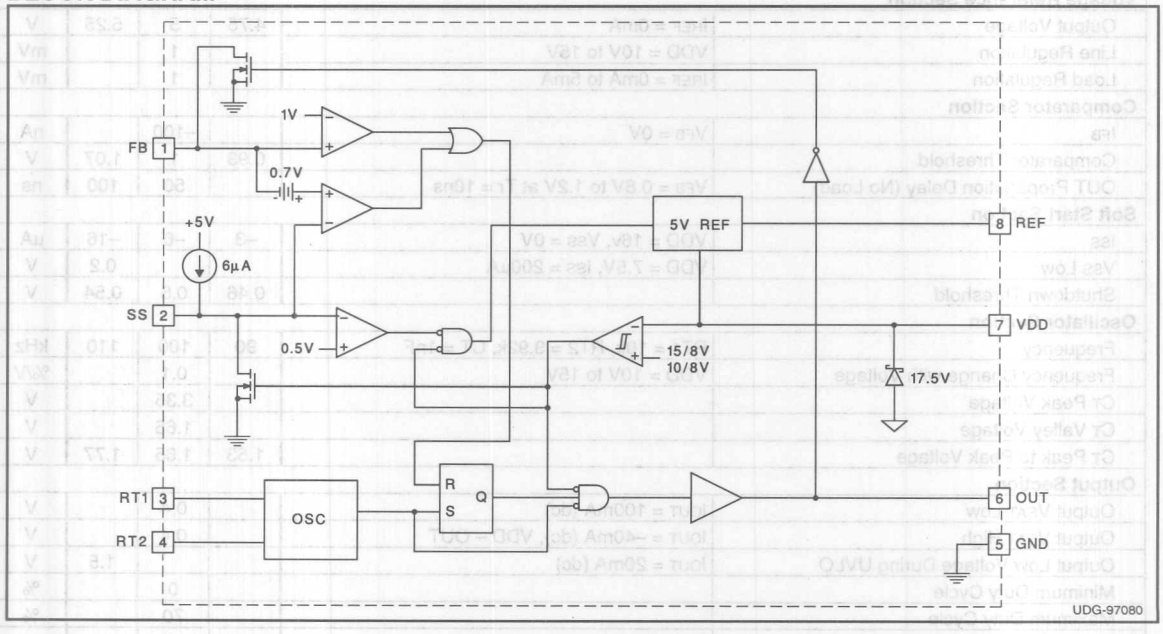
The UCC3809 family of BCDMOS economy low power integrated circuits contains all the control and drive circuitry required for off-line and isolated DC-to-DC fixed frequency current mode switching power supplies with minimal external parts count. Internally implemented circuits include undervoltage lockout featuring startup current less than 100µA, a user accessible voltage reference, logic to ensure latched operation, a PWM comparator, and a complementary output stage to sink or source peak current. The output stage, suitable for driving N-Channel MOSFETs, is low in the off state.

Oscillator frequency and maximum duty cycle are programmed with two resistors and a capacitor. The UCC3809 family also features full cycle soft start.

The family has UVLO thresholds and hysteresis levels for off-line and DC-to-DC systems as shown in the table below.

PART NUMBER	TURN ON THRESHOLD	TURN OFF THRESHOLD
UCCX809-1	10V	8V
UCCX809-2	15V	8V

BLOCK DIAGRAM



3

GENERAL POWER SUPPLY

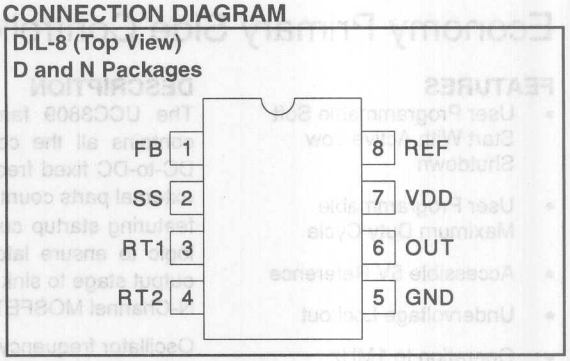
ABSOLUTE MAXIMUM RATINGS

VDD 17.5V
IVDD 25mA
IOUT (tpw < 1µs and Duty Cycle < 10%) ..... –0.4A to 1.0A
RT1, RT2, SS ..... -0.3V to REF + 0.3V
IREF ..... –15mA
Storage Temperature ..... –65°C to +150°C
Junction Temperature ..... –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

All voltages are with respect to ground unless otherwise stated. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

DIL-8 (Top View)
D and N Packages



ELECTRICAL CHARACTERISTICS: Unless otherwise specified, TA = 0°C to 70°C for the UCC3809-1/-2, –40°C to 85°C for the 2809-1/-2 and –55°C to 125°C for the UCC1809-1/-2. TA = TJ.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Section					
VDD Clamp	IVDD = 10mA	16	17.5	19	V
IVDD	No Load		500		µA
IVDD Starting				100	µA
Undervoltage Lockout Section					
Start Threshold (UCCx809-1)		9.5	10	10.5	V
UVLO Hysteresis (UCCx809-1)		1.9	2		V
Start Threshold (UCC3809-2)		14.2	15	15.8	V
UVLO Hysteresis (UCCx809-2)		6.6	7		V
Voltage Reference Section					
Output Voltage	IREF = 0mA	4.75	5	5.25	V
Line Regulation	VDD = 10V to 15V		1		mV
Load Regulation	IREF = 0mA to 5mA		1		mV
Comparator Section					
IFB	VFB = 0V		–100		nA
Comparator Threshold		0.93	1	1.07	V
OUT Propagation Delay (No Load)	VFB = 0.8V to 1.2V at Tr = 10ns		50	100	ns
Soft Start Section					
ISS	VDD = 16v, VSS = 0V	–3	–6	–16	µA
VSS Low	VDD = 7.5V, ISS = 200µA			0.2	V
Shutdown Threshold		0.46	0.5	0.54	V
Oscillator Section					
Frequency	RT1 = 10k, RT2 = 3.92k, CT = 1nF	90	100	110	kHz
Frequency Change with Voltage	VDD = 10V to 15V		0.1		%/V
CT Peak Voltage			3.35		V
CT Valley Voltage			1.65		V
CT Peak to Peak Voltage		1.53	1.65	1.77	V
Output Section					
Output VSAT Low	IOUT = 100mA (dc)		0.4		V
Output VSAT High	IOUT = –40mA (dc), VDD – OUT		0.4		V
Output Low Voltage During UVLO	IOUT = 20mA (dc)			1.5	V
Minimum Duty Cycle			0		%
Maximum Duty Cycle			70		%
Rise Time	COUT = 1nF		35		ns
Fall Time	COUT = 1nF		15		ns

PIN DESCRITPTION

FB: This pin is the summing node for current sense feedback, voltage sense feedback (by opto coupler) and slope compensation. Slope compensation is derived from the rising voltage at the timing capacitor and can be buffered with an external small signal NPN transistor. External high frequency filter capacitance applied from this node to GND is discharged by an internal 250Ω on resistance NMOS FET during PWM off time and offers effective leading edge blanking set by the RC time constant of the feed back resistance from current sense resistor to FB input and the high frequency filter capacitor capacitance at this node to GND.

GND: Reference ground and power ground for all functions.

OUT: This pin is the high current power driver output.

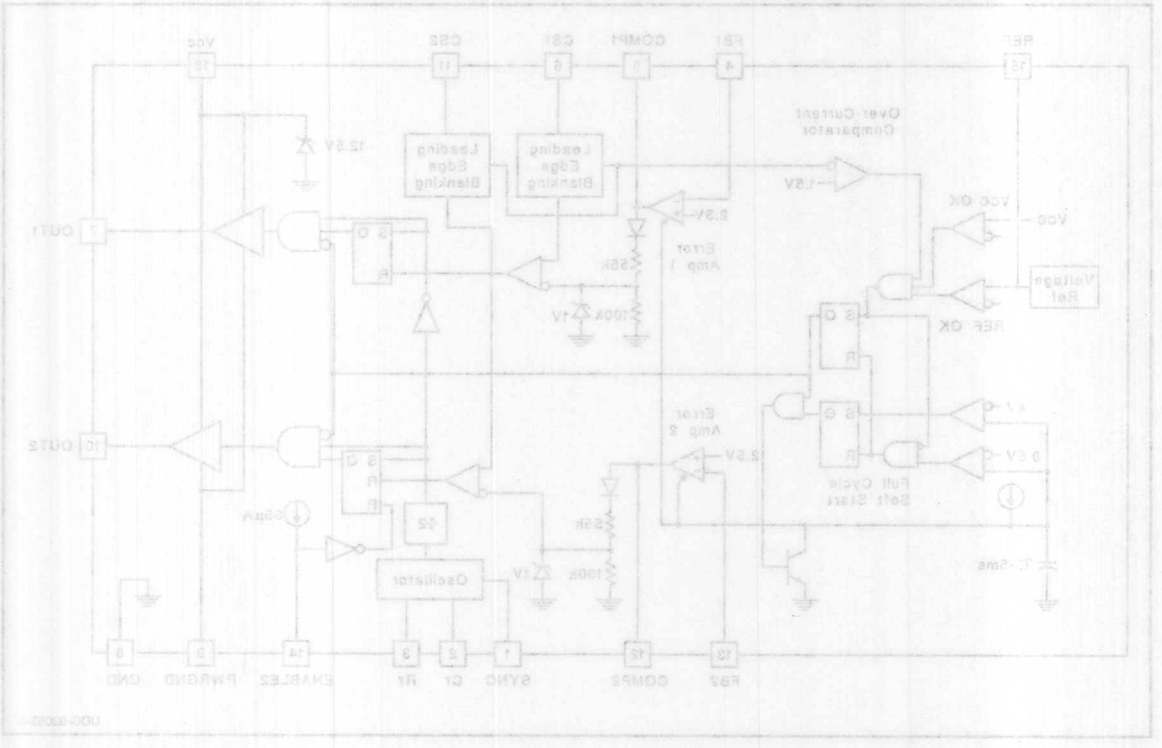
REF: The internal 5V reference output. This reference is buffered and is available on the REF pin.

RT1: This pin connects to timing resistor RT1 and controls the positive ramp time of the internal oscillator (Tr = 0.69 * RT1 * CT). The positive threshold of the internal oscillator is sensed through inactive timing resistor RT2 which connects to pin RT2 and timing capacitor CT.

RT2: This pin connects to timing resistor RT2 and controls the negative ramp time of the internal oscillator (Tf = 0.69 * RT2 * CT). The negative threshold of the internal oscillator is sensed through inactive timing resistor RT1 which connects to pin RT1 and timing capacitor CT.

SS: This pin serves two functions. The soft start timing capacitor connects to SS and is charged by an internal 20μA current source. Under normal soft start SS is discharged to at least 0.4V and then ramps positive to 0.7V during which time the output driver is held low. As SS charges from 0.7V to 1.7V soft start is implemented by an increasing output duty cycle. If SS is taken below 0.5V, the output driver is inhibited and held low. The user accessible 5V voltage reference also goes low and I_{VDD} < 100μA.

VDD: The power input connection for this device. This pin is shunt regulated at 17.5V which is sufficiently below the voltage rating of the DMOS output driver stage.



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UNITRODE

UCC1810
UCC2810
UCC3810

Dual Channel Synchronized Current Mode PWM

PRELIMINARY

FEATURES

- Single Oscillator Synchronizes Two PWMs
- 150µA Startup Supply Current
- 2mA Operating Supply Current
- Operation to 1MHz
- Internal Soft Start
- Full-Cycle Fault Restart
- Internal Leading Edge Blanking of the Current Sense Signal
- 1 Amp Totem Pole Outputs
- 75ns Typical Response from Current Sense to Output
- 1.5% Tolerance Voltage Reference

DESCRIPTION

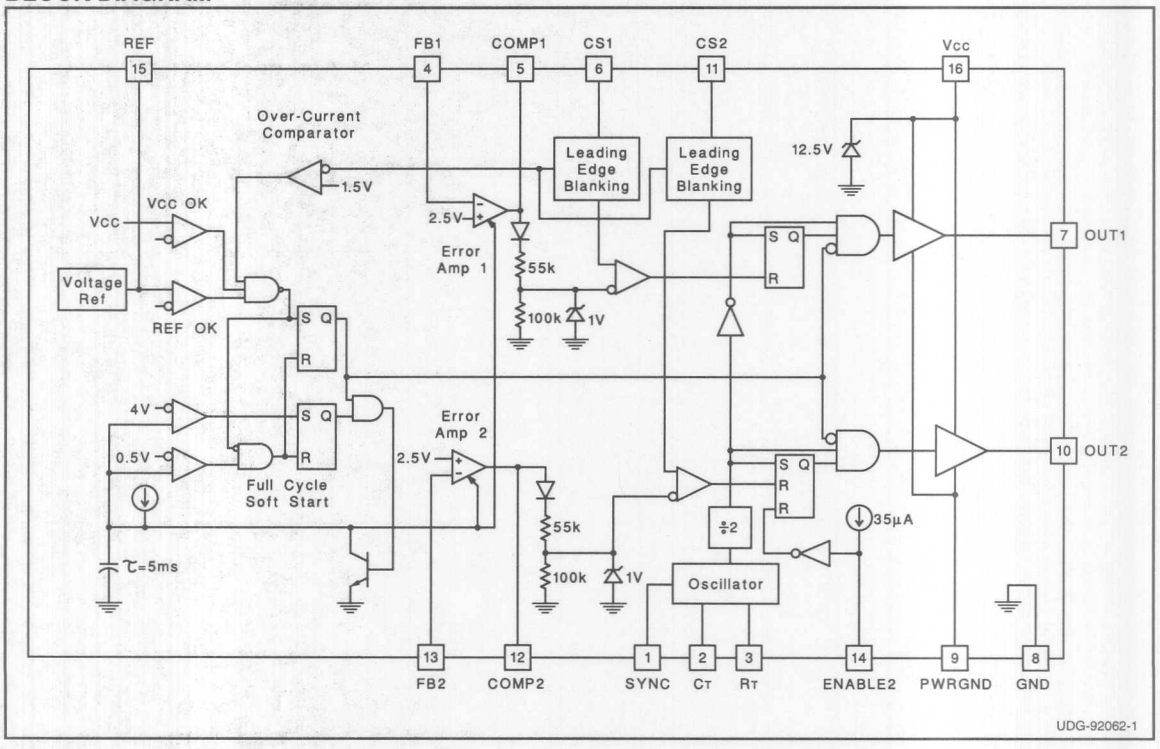
The UCC3810 is a high-speed BiCMOS integrated circuit which implements two synchronized pulse width modulators for use in off-line and DC-to-DC power supplies.

The UCC3810 provides perfect synchronization between two PWMs by using the same oscillator. The oscillator's sawtooth waveform can be used for slope compensation if required.

Using a toggle flip flop to alternate between modulators, the UCC3810 ensures that one PWM will not slave, interfere, or otherwise affect the other PWM. This toggle flip flop also ensures that each PWM will be limited to 50% maximum duty cycle, insuring adequate off-time to reset magnetic elements.

This IC contains many of the same elements of the UC3842 current mode controller family, combined with the enhancements of the UCC3802. This minimizes power supply parts count. Enhancements include leading edge blanking of the current sense signals, full cycle fault restart, CMOS output drivers, and outputs which remain low even when the supply voltage is removed.

BLOCK DIAGRAM



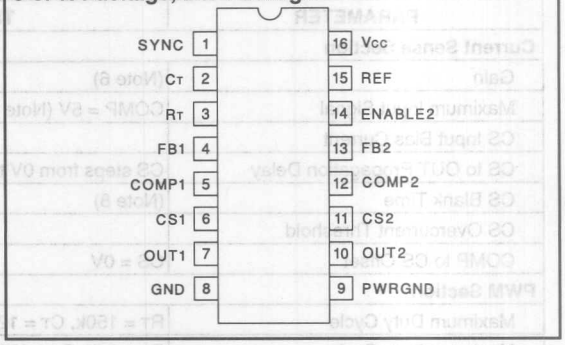
ABSOLUTE MAXIMUM RATINGS

Vcc Voltage (Note 3) 11V
Vcc Current 20mA
OUT1, OUT2 Current, Peak, 5% Duty Cycle ..... ±1A
OUT1, OUT2 Energy (Capacitive Load) 20µJ
Analog Inputs (FB1, FB2, CS1, CS2, SYNC) .... -0.3V to 6.3V
Operating Junction Temperature ..... +150°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 10 seconds) ..... 300°C

Note 1: All voltages are with respect to GND. All currents are positive into the specified terminals.
Note 2: Consult Unitrode Integrated Circuits Product & Applications Handbook for information regarding thermal specifications and limitations of packages.
Note 3: In normal operation, Vcc is powered through a current limiting resistor. Absolute maximum of 11V applies when driven from a low impedance such that the Vcc current does not exceed 20mA.

CONNECTION DIAGRAM

DIL-16, SOIC-16 (TOP VIEW)
J or N Package, DW Package



ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply for –55°C ≤ TA ≤ 125°C for UCC1810; –40°C ≤ TA ≤ 85°C for UCC2810; 0°C ≤ TA ≤ 70°C for UCC3810; Vcc = 10V (Note 4); RT = 150k; CT = 120pF; No Load; TA = TJ. All parameters are the same for both channels.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Reference Section					
Output Voltage	TJ = 25°C	4.925	5.000	5.075	V
Load Regulation	0mA < IREF < 5mA		5	25	mV
Line Regulation	UVLO Stop Threshold Voltage+0.5V < Vcc < Shunt Voltage		12		mV
Output Voltage	Full temperature range, 0mA < IREF < 5mA	4.88	5.00	5.10	V
Output Noise Voltage	10Hz < f < 10kHz, TJ = +25°C (Note 10)		235		µV
Long Term Stability	TA = +125°C, 1000 Hours (Note 10)		5		mV
Output Short Circuit Current			–8	–25	mA
Oscillator Section					
Oscillator Frequency	RT = 30k, CT = 120pF (Note 5)	880	980	1080	kHz
Oscillator Frequency	RT = 150k, CT = 120pF (Note 5)	200	220	240	kHz
Temperature Stability	(Note 10)		2.5		%
Peak Voltage			2.5		V
Valley Voltage			0.05		V
Peak-to-Peak Amplitude		2.25	2.45	2.65	V
SYNC Threshold		0.80	1.65	2.00	V
SYNC Input Current	SYNC = 5V		30		µA
Error Amplifier Section					
FB Input Voltage	COMP = 2.5V	2.44	2.50	2.56	V
FB Input Bias Current				±1	µA
Open Loop Voltage Gain		60	73		dB
Unity Gain Bandwidth	(Note 10)		2		MHz
COMP Sink Current	FB = 2.7V, COMP = 1V	0.3	1.4	3.5	mA
COMP Source Current	FB = 1.8V, COMP = 4V	–0.2	–0.5	–0.8	mA
Minimum Duty Cycle	COMP = 0V			0	%
COMP Soft Start Rise Time	FB = 1.8V, Rise from 0.5V to REF-1V		5		ms

ELECTRICAL CHARACTERISTICS (cont.)

Unless otherwise stated, these specifications apply for $-55^{\circ}C \le T_A \le 125^{\circ}C$ for UCC1810; $-40^{\circ}C \le T_A \le 85^{\circ}C$ for UCC2810; $0^{\circ}C \le T_A \le 70^{\circ}C$ for UCC3810; V_{CC} = 10V (Note 4); R_T = 150k; C_T = 120pF; No Load; $T_A = T_J$. All parameters are the same for both channels.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Current Sense Section					
Gain	(Note 6)	1.30	1.55	1.80	V/V
Maximum Input Signal	COMP = 5V (Note 7)	0.9	1.0	1.1	V
CS Input Bias Current				±200	nA
CS to OUT Propagation Delay	CS steps from 0V to 1.2V, COMP = 2.5V		75		ns
CS Blank Time	(Note 8)		55		ns
CS Overcurrent Threshold		1.35	1.55	1.75	V
COMP to CS Offset	CS = 0V	0.65	0.95	1.4	V
PWM Section					
Maximum Duty Cycle	R_T = 150k, C_T = 120pF (Note 10)	45	49	50	%
Maximum Duty Cycle	R_T = 30k, C_T = 120pF (Note 10)	40	45	48	%
Minimum On Time	CS =1.2V, COMP = 5V		130		ns
Output Section					
OUT Low Level	I_{OUT} = 20mA		0.12	0.42	V
	I_{OUT} = 200mA		0.48	1.10	V
	I_{OUT} = 20mA, V_{CC} = 0V		0.7	1.20	V
OUT High Level (V_{CC} - OUT)	I_{OUT} = –20mA		0.15	0.42	V
	I_{OUT} = –200mA		1.20	2.10	V
OUT Rise Time	C_{OUT} = 1nF		20	50	ns
OUT Fall Time	C_{OUT} = 1nF		30	60	ns
Undervoltage Lockout Section					
Start Threshold		10.5	11.3	13.2	V
Stop Threshold		7.5	8.3	9.5	V
Start to Stop Hysteresis		1.7	3.0	4.7	V
ENABLE2 Input Bias Current	ENABLE2 = 0V	–20	–35	–55	µA
ENABLE2 Input Threshold Voltage		0.80	1.53	2.00	V
Overall Section					
Startup Current	V_{CC} < Start Threshold Voltage		0.15	0.25	mA
Operating Supply Current, Outputs Off	V_{CC} = 10V, FB = 2.75V		2.0	3.0	mA
Operating Supply Current, Outputs On	V_{CC} = 10V, FB = 0V, CS = 0V, R_T = 150k		3.2	5.1	mA
Operating Supply Current, Outputs On	V_{CC} = 10V, FB = 0V, CS = 0V, R_T = 30k		8.5	14.5	mA
V_{CC} Internal Zener Voltage	I_{CC} = 10mA (Note 9)	11.0	12.9	14.0	V
V_{CC} Internal Zener Voltage Minus Start Threshold Voltage		0.4	1.2		V

Note 4: Adjust Vcc above the start threshold before setting at 10V.

Note 5: Oscillator frequency is twice the output frequency. $Fosc \approx \frac{4}{R_T \times C_T}$

Note 6: Current Sense Gain A is defined by: $A = \frac{\Delta V_{COMP}}{\Delta V_{CS}}$ $0 \le V_{CS} \le 0.8V$.

Note 7: Parameter measured at trip point of latch with FB = 0V.

Note 8: CS Blank Time is measured as the difference between the minimum non-zero on-time and the CS to OUT delay.

Note 9: Start Threshold Voltage and Vcc Internal Zener Voltage track each other.

Note 10: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

COMP1, COMP2: The low impedance outputs of the error amplifiers.

CS1, CS2: The current sense inputs to the PWM comparators. These inputs have leading edge blanking. For most applications, no input filtering is required. Leading edge blanking disconnects the CS inputs from all internal circuits for the first 55ns of each PWM cycle. When used with very slow diodes or in other applications where the current sense signal is unusually noisy, a small current sense RC filter may be required.

CT: The timing capacitor of the oscillator. Recommended values of CT are between 100pF and 1nF. Connect the timing capacitor directly across CT and GND.

ENABLE2: A logic input which disables PWM 2 when low. This input has no effect on PWM 1. This input is internally pulled high. In most applications it can be left floating. In unusually noisy applications, the input should be bypassed with a 1nF ceramic capacitor. This input has TTL compatible thresholds.

FB1, FB2: The high impedance inverting inputs of the error amplifiers.

GND: To separate noise from the critical control circuits, this part has two different ground connections: GND and PWRGND. GND and PWRGND must be electrically connected together. However, use care to avoid coupling noise into GND.

OUT1, OUT2: The high current push-pull outputs of the PWM are intended to drive power MOSFET gates through a small resistor. This resistor acts as both a current limiting resistor and as a damping impedance to minimize ringing and overshoot.

PWRGND: To separate noise from the critical control circuits, this part has two different ground connections: GND and PWRGND. GND and PWRGND must be electrically connected together.

REF: The output of the 5V reference. Bypass REF to GND with a ceramic capacitor ≥0.01µF for best performance.

RT: The oscillator charging current is set by the value of the resistor connected from RT to GND. This pin is regulated to 1V, but the actual charging current is 10V/RT. Recommended values of RT are between 10k and 470k. For a given frequency, higher timing resistors give higher maximum duty cycle and slightly lower overall power consumption. Supply current decreases with increased RT by the relationship:

$$\Delta Icc = \frac{11\,V}{RT}$$

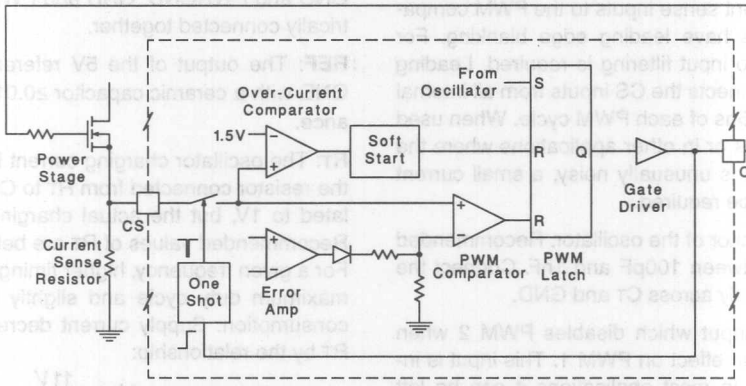
For more information, see the detailed oscillator block diagram.

SYNC: This logic input can be used to synchronize the oscillator to a free running oscillator in another part. This pin is edge triggered with TTL thresholds, and requires at least a 10ns wide pulse. If unused, this pin can be grounded, open circuited, or connected to REF.

VCC: The power input to the IC. This pin supplies current to all functions including the high current output stages and the precision reference. Therefore, it is critical that VCC be directly bypassed to PWRGND with an 0.1µF ceramic capacitor.

DETAILED BLOCK DIAGRAMS

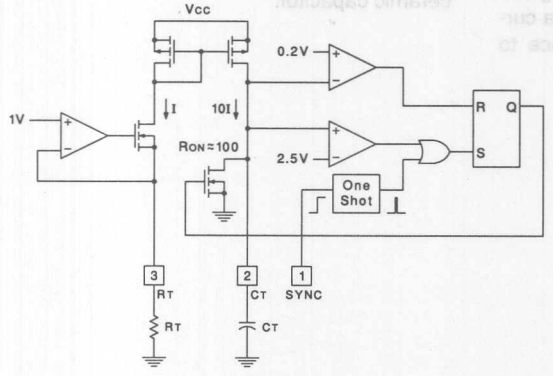
LEADING EDGE BLANKING and CURRENT SENSE



This diagram shows how an external power stage is connected to the UCC3810. The gate of an external power N-channel MOSFET is connected to OUT through a small current limiting resistor. For most applications, a 10Ω resistor is adequate to limit peak current and also practical at damping resonances between the gate driver and the MOSFET input reactance. Long gate lead length increases gate capacitance and mandates a higher series gate resistor to damp the RLC tank formed by the lead, the MOSFET input reactance, and the UCC3810 driver output resistance.

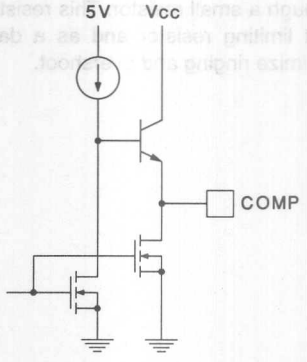
The UCC3810 features internal leading edge blanking of the current sense signal on both current sense inputs. The blank time starts when OUT rises and continues for 55ns. During that 55ns period, the signal on CS is ignored. For most PWM applications, this means that the CS input can be connected to the current sense resistor as shown above. However, high speed grounding practices and short lead lengths are still required for good performance.

OSCILLATOR



The UCC3810 oscillator generates a sawtooth wave at CT. The sawtooth rise time is set by the resistor from RT to GND. Since RT is biased at 1V, the current in RT is 1V/RT. The actual charging current is 10 times higher. The fall time is set by an internal transistor on-resistance of approximately 100Ω. During the fall time, all outputs are off and the maximum duty cycle is reduced below 50%. Larger timing capacitors increase the discharge time and reduce frequency. However, the percentage maximum duty cycle is only a function of the timing resistor RT and the internal 100Ω discharge resistance.

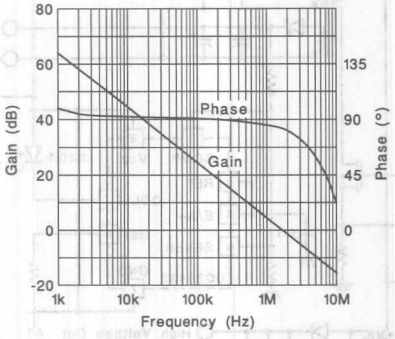
ERROR AMP OUTPUT STAGE



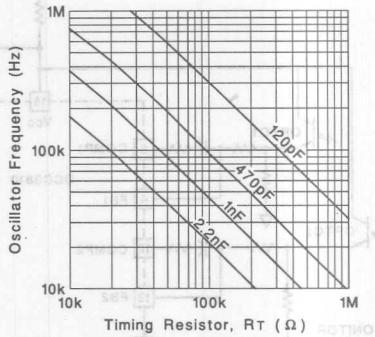
The UCC3810 error amplifiers are operational amplifiers with low output resistance and high input resistance. The output stage of one error amplifier is shown above. This output stage allows the error amplifier output to swing close to GND and as high as one diode drop below 5V with little loss in amplifier performance.

TYPICAL CHARACTERISTICS

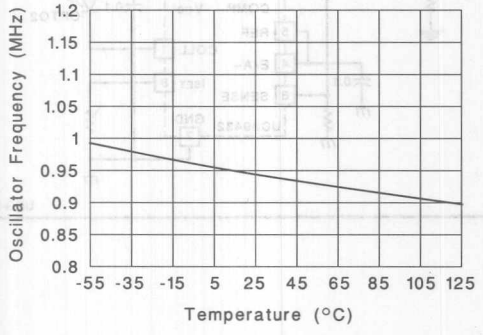
Error Amp and Gain Phase Response



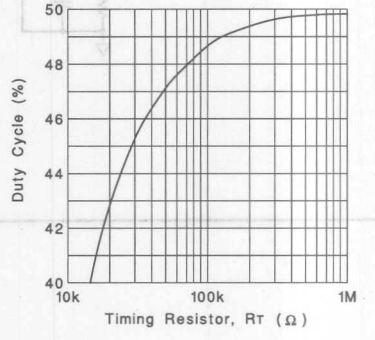
Oscillator Frequency vs RT and CT



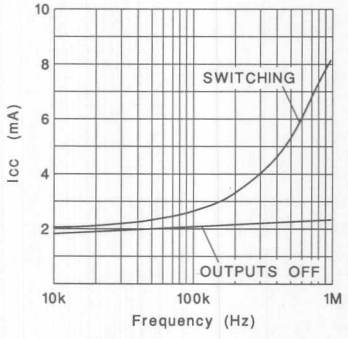
Oscillator Frequency vs Temperature



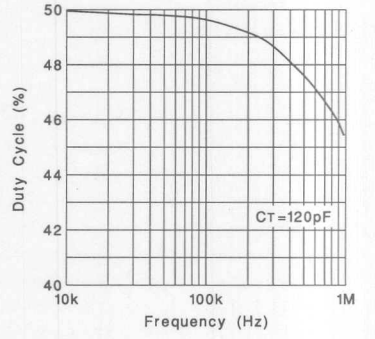
Maximum Duty Cycle vs RT



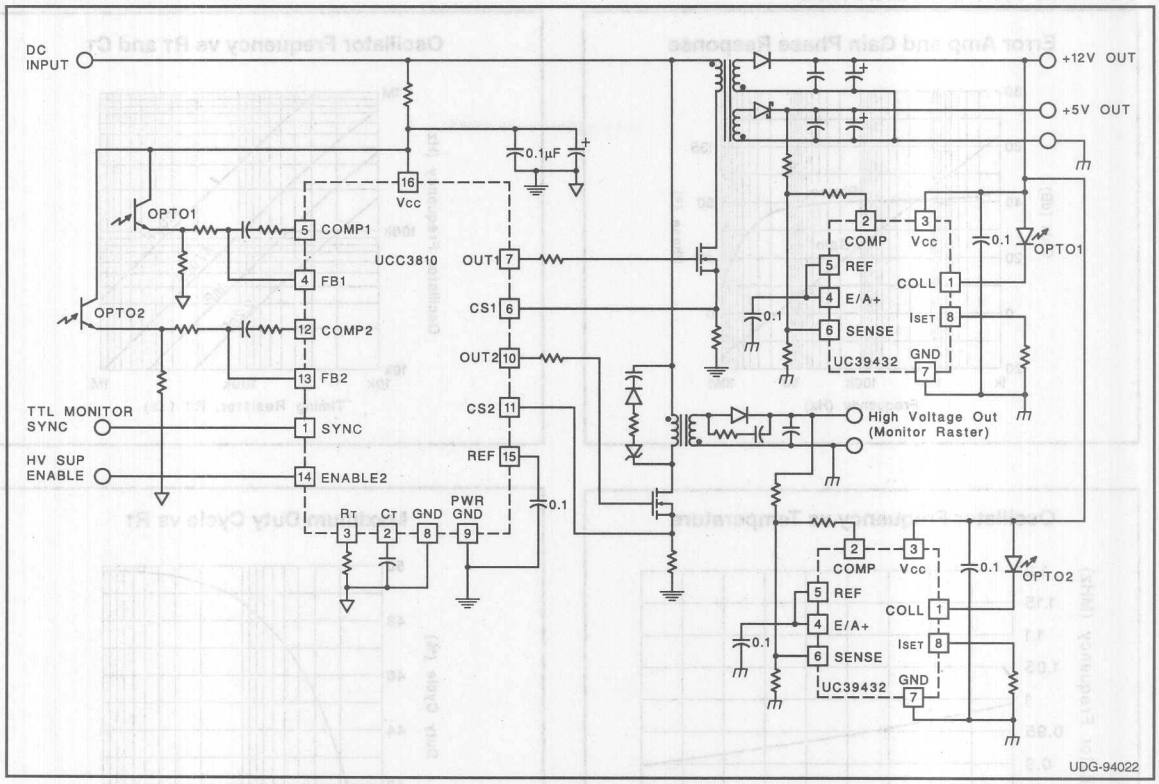
ICC vs Oscillator Frequency



Maximum Duty Cycle vs Frequency



TYPICAL APPLICATION



UNITRODE CORPORATION
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12V Boost Regulator

ADVANCED INFORMATION

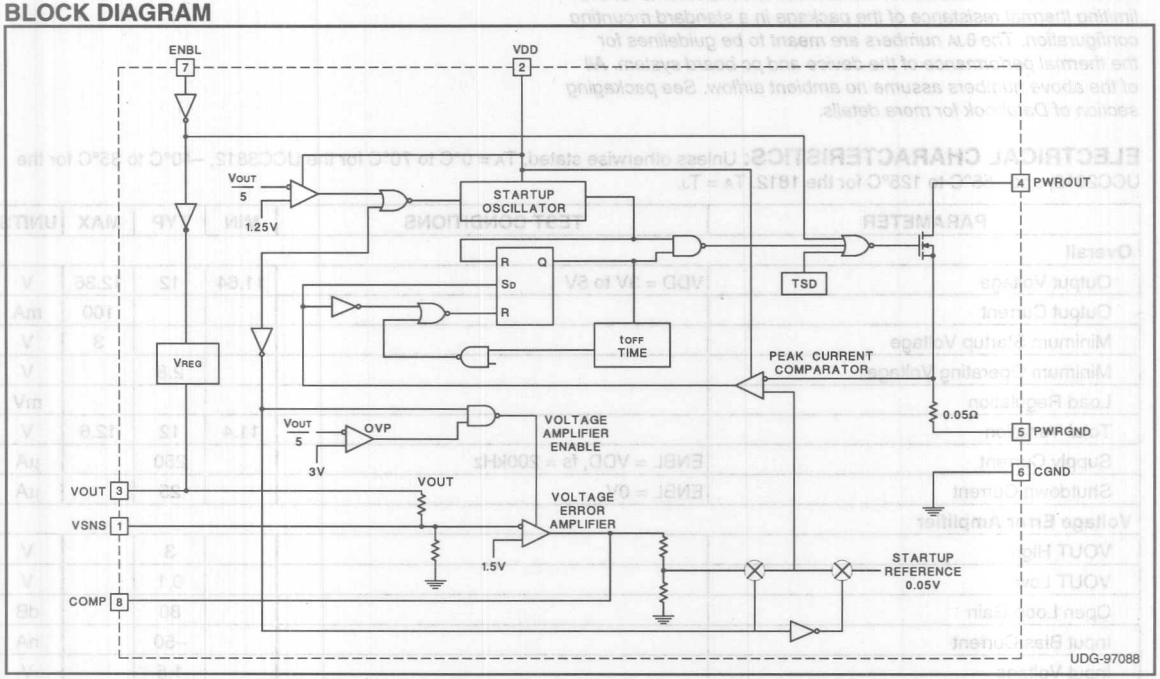
FEATURES

- 3V to 5V Input Voltage Range
- Peak Current Limited PWM Control
- 250µA Operating Supply Current
- 25µA Shutdown Supply Current
- 12V/100mA Output
- Available in 8 Pin DIL and SOIC Packages

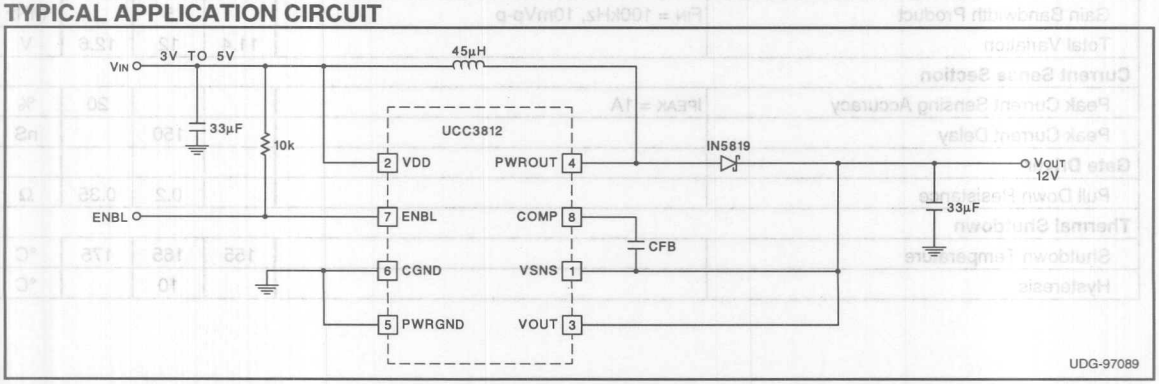
DESCRIPTION

The UCC3812 is a low power boost regulator that takes a 3V to 5V input and outputs a regulated 12V at 100mA. The part uses peak current sensing with a fixed 1µs off time for the current control. An internal power FET with an $R_{DS(ON)}$ of 200mΩ allows peak input currents up to 1A.

BLOCK DIAGRAM



TYPICAL APPLICATION CIRCUIT



4/97

ABSOLUTE MAXIMUM RATINGS

Input Voltage 6.5V
Power Dissapation 0.4W
Storage Temperature ..... –65°C to +150°C
Junction Temperature ..... –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

THERMAL DATA

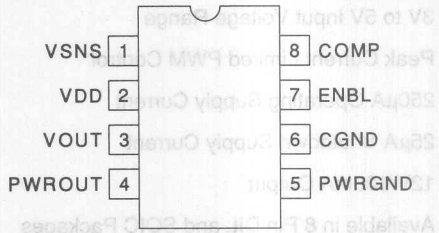
8 Pin SOIC (D)

Thermal Resistance Junction to Case θ_{JC} ..... 42°C/W
Thermal Resistance Junction to Ambient θ_{JA} ..... 160°C/W

Note: The above numbers for θ_{JA} and θ_{JC} are maximums for the limiting thermal resistance of the package in a standard mounting configuration. The θ_{JA} numbers are meant to be guidelines for the thermal performance of the device and pc board system. All of the above numbers assume no ambient airflow. See packaging section of Databook for more details.

CONNECTION DIAGRAM

DIP-8, SOIC-8 (Top View)
J Package, D Package



ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, T_A = 0°C to 70°C for the UCC3812, –40°C to 85°C for the UCC2812, and –55°C to 125°C for the 1812. $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Overall					
Output Voltage	VDD = 3V to 5V	11.64	12	12.36	V
Output Current				100	mA
Minimum Startup Voltage				3	V
Minimum Operating Voltage			2.8		V
Load Regulation					mV
Total Variation		11.4	12	12.6	V
Supply Current	ENBL = VDD, fs = 200kHz		250		µA
Shutdown Current	ENBL = 0V		25		µA
Voltage Error Amplifier					
VOUT High			3		V
VOUT Low			0.1		V
Open Loop Gain			80		dB
Input Bias Current			–50		nA
Input Voltage			1.5		V
Gain Bandwidth Product	F_{IN} = 100kHz, 10mVp-p		5		MHz
Total Variation		11.4	12	12.6	V
Current Sense Section					
Peak Current Sensing Accuracy	I_{PEAK} = 1A			20	%
Peak Current Delay			150		nS
Gate Driver					
Pull Down Resistance			0.2	0.35	Ω
Thermal Shutdown					
Shutdown Temperature		155	165	175	°C
Hysteresis			10		°C

PIN DESCRIPTION

CGND: Low power ground for reference and other part functions.

COMP: Output of the voltage error amplifier.

ENBL: A logic level input used to switch the device in and out of the low current shutdown mode. Pulling ENBL low puts the part in shutdown mode.

PWRGND: Power ground for high current DMOS output section.

PWROUT: Drain of an internal DMOS device with its source connected through a sense resistor to PWRGND. This device has a peak current limit of 1A.

VDD: The power supply input connection for the device connected to a voltage of 3V to 5V.

VOUT: Voltage feedback from the regulated 12V to the non-inverting input of the voltage error amplifier. This input is also used to bootstrap the gate drive to the power DMOS device.

VSNS: The inverting input to the voltage amplifier.

APPLICATION INFORMATION

The UCC3812 is a boost controller IC with an integrated MOSFET. The control is provided by a constant off time current loop with an outer voltage loop for output voltage regulation. The advantage of the constant off time current loop is that it provides cycle by cycle current limiting and all the benefits of current mode control such as easy compensation of the voltage loop, while being inherently stable and therefore not requiring ramp compensation. The UCC3812 takes an input voltage in the range of 3V to 5V and boosts it up to a regulated 12V output. With the MOSFET and current sensing circuitry internal to the IC, the design of the converter is very straight forward. For a maximum load current of 100mA and minimum input voltage of 3V the average input current will be 400mA. The inductor current ripple (ΔI) can be chosen to be half IIN. Therefore, the inductor required is:

$$L \approx \frac{V_{IN\ MIN} \bullet T_{ON\ MAX}}{\Delta I}$$

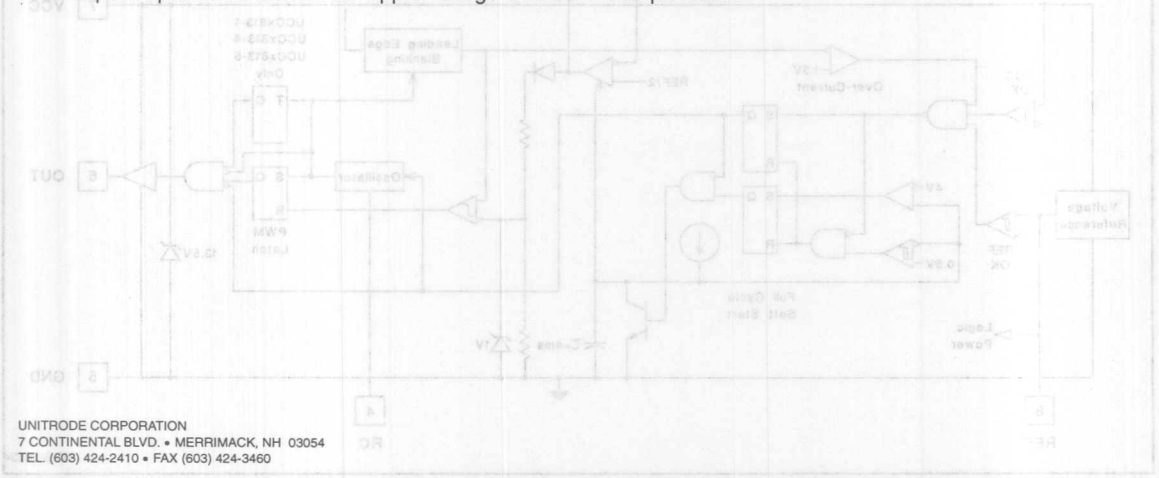
For V_{IN} = 3V, $t_{ON\ MIN}$ = 3µS. Therefore, the inductance required is 45µH.

The output capacitor is chosen for ripple voltage and it's allowable ripple current. In general a low ESR capacitor is suggested to limit the ripple voltage. In this application an ESR of approximately 200mΩ will limit the ripple voltage (neglecting capacitive discharge) to 100mV. Several capacitors are appropriate here, a 33µF OsCON or a 220µF, low ESR electrolytic capacitor would be acceptable.

The diode is chosen to handle the load current. A schottky rectifier is a good choice for its low voltage drop. A 1N5819, or equivalent is appropriate here.

Compensation

Compensation of the converter can be accomplished with simple dominate pole compensation. For the case where 33µF output capacitor is used, a 680pF capacitor in the feedback loop will give a 600Hz cross over frequency with a phase margin of 50°C (if the 220µF capacitor is used a 6.8nF feedback capacitor will result in a cross over frequency of 60Hz and phase margin of about 60°C). If higher bandwidth is required or faster transient response, a zero-pole pair can be used for compensation.



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UNITRODE

Low Power Economy BiCMOS Current Mode PWM

FEATURES

- 100µA Typical Starting Supply Current
- 500µA Typical Operating Supply Current
- Operation to 1MHz
- Internal Soft Start
- Internal Fault Soft Start
- Internal Leading-Edge Blanking of the Current Sense Signal
- 1 Amp Totem-Pole Output
- 70ns Typical Response from Current-Sense to Gate Drive Output
- 1.5% Tolerance Voltage Reference
- Same Pinout as UCC3802, UC3842, and UC3842A

DESCRIPTION

The UCC3813-0/-1/-2/-3/-4/-5 family of high-speed, low-power integrated circuits contain all of the control and drive components required for off-line and DC-to-DC fixed frequency current-mode switching power supplies with minimal parts count.

These devices have the same pin configuration as the UC3842/3/4/5 family, and also offer the added features of internal full-cycle soft start and internal leading-edge blanking of the current-sense input.

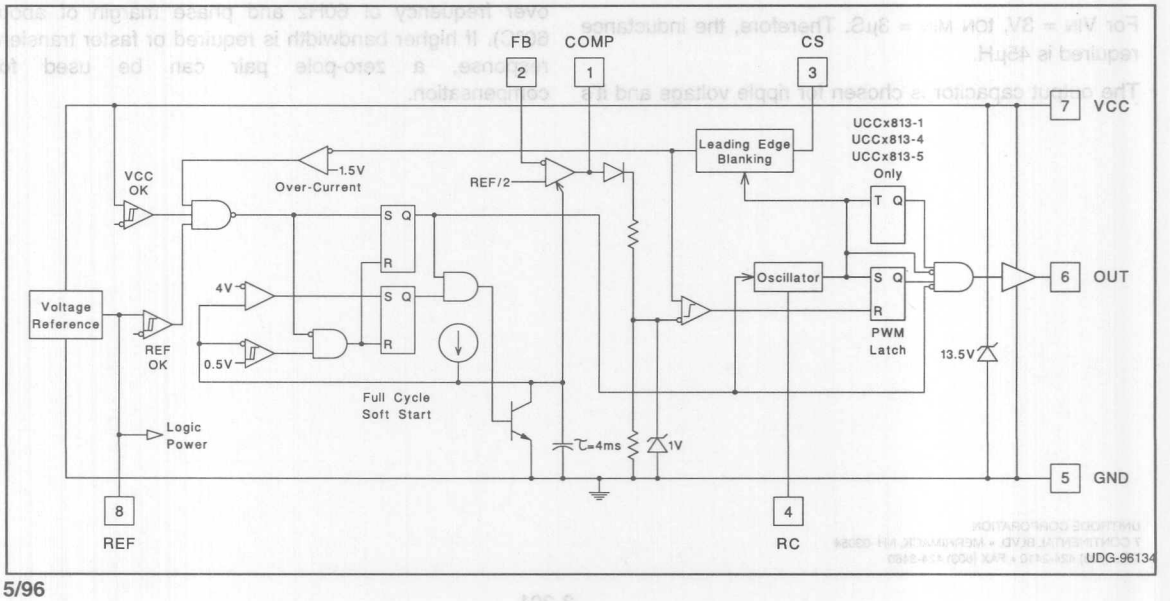
The UCC3813-0/-1/-2/-3/-4/-5 family offers a variety of package options, temperature range options, choice of maximum duty cycle, and choice of critical voltage levels. Lower reference parts such as the UCC3813-3 and UCC3813-5 fit best into battery operated systems, while the higher reference and the higher UVLO hysteresis of the UCC3813-2 and UCC3813-4 make these ideal choices for use in off-line power supplies.

The UCC2813-x series is specified for operation from –40°C to +85°C and the UCC3813-x series is specified for operation from 0°C to +70°C.

ORDERING INFORMATION

Part Number	Maximum Duty Cycle	Reference Voltage	Turn-On Threshold	Turn-Off Threshold
UCCx813-0	100%	5V	7.2V	6.9V
UCCx813-1	50%	5V	9.4V	7.4V
UCCx813-2	100%	5V	12.5V	8.3V
UCCx813-3	100%	4V	4.1V	3.6V
UCCx813-4	50%	5V	12.5V	8.3V
UCCx813-5	50%	4V	4.1V	3.6V

BLOCK DIAGRAM



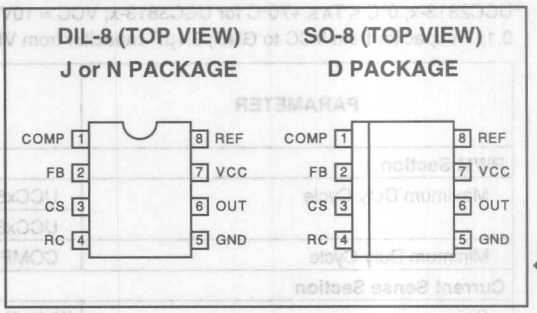
ABSOLUTE MAXIMUM RATINGS (Note 1)

VCC Voltage (Note 2) 12.0V
VCC Current 30.0mA
OUT Current ..... ±1.0A
OUT Energy (Capacitive Load) 20.0µJ
Analog Inputs (FB, CS) ..... -0.3V to 6.3V
Power Dissipation at T_A < +25°C (N or J Package) 1.0W
Power Dissipation at T_A < +25°C (D Package) 0.65W
Storage Temperature ..... –65°C to +150°C
Junction Temperature ..... –55°C to +150°C
Lead Temperature (Soldering, 10 Seconds) ..... +300°C

Note 1: All voltages are with respect to GND. All currents are positive into the specified terminal. Consult Unitrode Integrated Circuits databook for information regarding thermal specifications and limitations of packages.

Note 2: In normal operation VCC is powered through a current limiting resistor. Absolute maximum of 12V applies when VCC is driven from a low impedance source such that ICC does not exceed 30mA.

CONNECTION DIAGRAM



ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply for –40° ≤ T_A ≤ +85°C for UCC2813-x; 0°C ≤ T_A ≤ +70°C for UCC3813-x; VCC = 10V (Note 3); RT = 100k from REF to RC; CT=330pF from RC to GND; 0.1µF capacitor from VCC to GND; 0.1µF capacitor from VREF to GND. T_A = T_J.

PARAMETER	TEST CONDITIONS	UCC2813-x UCC3813-x			UNITS
		MIN	TYP	MAX	
Reference Section					
Output Voltage	T_J = +25°C, I = 0.2mA, UCCx813-0/-1/-2/-4	4.925	5.00	5.075	V
	T_J = +25°C, I = 0.2mA, UCCx813-5	3.94	4.00	4.06	
Load Regulation	0.2mA < I < 5mA		10	30	mV
Total Variation	UCCx813-1/-2/-4 (Note 7)	4.84	5.00	5.10	V
	UCCx813-5 (Note 7)	3.84	4.00	4.08	V
Output Noise Voltage	10Hz ≤ f ≤ 10kHz, T_J = +25°C (Note 9)		70		µV
Long Term Stability	T_A = +125°C, 1000 Hours (Note 9)		5		mV
Output Short Circuit		–5		–35	mA
Oscillator Section					
Oscillator Frequency	UCCx813-0/-1/-2/-4 (Note 4)	40	46	52	kHz
	UCCx813-5 (Note 4)	26	31	36	
Temperature Stability	(Note 9)		2.5		%
Amplitude Peak-to-Peak		2.25	2.40	2.55	V
Oscillator Peak Voltage			2.45		V
Error Amplifier Section					
Input Voltage	COMP = 2.5V; UCCx813-0/-1/-2/-4	2.42	2.50	2.56	V
	COMP = 2.0V; UCCx813-3/-5	1.92	2.0	2.05	
Input Bias Current		–2		2	µA
Open Loop Voltage Gain		60	80		dB
COMP Sink Current	FB = 2.7V, COMP = 1.1V	0.4		2.5	mA
COMP Source Current	FB = 1.8V, COMP = REF - 1.2V	–0.2	–0.5	–0.8	mA
Gain Bandwidth Product	(Note 9)		2		MHz

ELECTRICAL CHARACTERISTICS (cont.) Unless otherwise stated, these specifications apply for –40° ≤ TA ≤ +85°C for UCC2813-x; 0°C ≤ TA ≤ +70°C for UCC3813-x; VCC = 10V (Note 3); RT = 100k from REF to RC; CT=330pF from RC to GND; 0.1µF capacitor from VCC to GND; 0.1µF capacitor from VREF to GND. TA = TJ.

PARAMETER	TEST CONDITIONS	UCC2813-x UCC3813-x			UNITS
		MIN	TYP	MAX	
PWM Section					
Maximum Duty Cycle	UCCx813-0/-2/-3	97	99	100	%
	UCCx813-1/-4/-5	48	49	50	
Minimum Duty Cycle	COMP = 0V			0	%
Current Sense Section					
Gain	(Note 5)	1.10	1.65	1.80	V/V
Maximum Input Signal	COMP = 5V (Note 6)	0.9	1.0	1.1	V
Input Bias Current		–200		200	nA
CS Blank Time		50	100	150	ns
Over-Current Threshold		1.32	1.55	1.70	V
COMP to CS Offset	CS = 0V	0.45	0.90	1.35	V
Output Section					
OUT Low Level	I = 20mA, all parts		0.1	0.4	V
	I = 200mA, all parts		0.35	0.90	
	I = 50mA, VCC = 5V, UCCx813-3/-5		0.15	0.40	
	I = 20mA, VCC = 0V, all parts		0.7	1.2	
OUT High V_{SAT} (Vcc-OUT)	I = –20mA, all parts		0.15	0.40	V
	I = –200mA, all parts		1.0	1.9	
	I = –50mA,VCC = 5V, UCCx813-3/-5		0.4	0.9	
Rise Time	C_L = 1nF		41	70	ns
Fall Time	C_L = 1nF		44	75	ns
Undervoltage Lockout Section					
Start Threshold (Note 8)	UCCx813-0	6.6	7.2	7.8	V
	UCCx813-1	8.6	9.4	10.2	
	UCCx813-2/-4	11.5	12.5	13.5	
	UCCx813-3/-5	3.7	4.1	4.5	
Stop Threshold (Note 8)	UCC1813-0	6.3	6.9	7.5	V
	UCC1813-1	6.8	7.4	8.0	
	UCCx813-2/-4	7.6	8.3	9.0	
	UCCx813-3/-5	3.2	3.6	4.0	
Start to Stop Hysteresis	UCCx813-0	0.12	0.3	0.48	V
	UCCx813-1	1.6	2	2.4	
	UCCx813-2/-4	3.5	4.2	5.1	
	UCCx813-3/-5	0.2	0.5	0.8	
Soft Start Section					
COMP Rise Time	FB = 1.8V, Rise from 0.5V to REF-1V		4		ms

ELECTRICAL CHARACTERISTICS (cont.) Unless otherwise stated, these specifications apply for $-40° \le T_A \le +85°C$ for UCC2813-x; $0°C \le T_A \le +70°C$ for UCC3813-x; VCC = 10V (Note 3); RT = 100k from REF to RC; CT=330pF from RC to GND; 0.1µF capacitor from VCC to GND; 0.1µF capacitor from VREF to GND. $T_A = T_J$.

PARAMETER	TEST CONDITIONS	UCC2813-x UCC3813-x			UNITS
		MIN	TYP	MAX	
Overall Section					
Start-up Current	VCC < Start Threshold		0.1	0.23	mA
Operating Supply Current	FB = 0V, CS = 0V, RC = 0V		0.5	1.2	mA
VCC Internal Zener Voltage	ICC = 10mA (Note 8)	12	13.5	15	V
VCC Internal Zener Voltage Minus Start Threshold Voltage	UCCx813-2/-4	0.5	1.0		V

Note 3: Adjust VCC above the start threshold before setting at 10V.
Note 4: Oscillator frequency for the UCCx813-0, UCCx813-2 and UCCx813-3 is the output frequency.
Oscillator frequency for the UCCx813-1, UCCx813-4 and UCCx813-5 is twice the output frequency.

Note 5: Gain is defined by: $A = \frac{\Delta V_{COMP}}{\Delta V_{CS}}$ $0 \le V_{CS} \le 0.8V$.

Note 6: Parameter measured at trip point of latch with Pin 2 at 0V.
Note 7: Total Variation includes temperature stability and load regulation.
Note 8: Start Threshold, Stop Threshold and Zener Shunt Thresholds track one another.
Note 9: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

COMP: COMP is the output of the error amplifier and the input of the PWM comparator.

Unlike other devices, the error amplifier in the UCC3813 family is a true, low output-impedance, 2MHz operational amplifier. As such, the COMP terminal can both source and sink current. However, the error amplifier is internally current limited, so that you can command zero duty cycle by externally forcing COMP to GND.

The UCC3813 family features built-in full cycle Soft Start. Soft Start is implemented as a clamp on the maximum COMP voltage.

FB: FB is the inverting input of the error amplifier. For best stability, keep FB lead length as short as possible and FB stray capacitance as small as possible.

CS: CS is the input to the current sense comparators. The UCC3813 family has two different current sense comparators: the PWM comparator and an over-current comparator.

The UCC3813 family contains digital current sense filtering, which disconnects the CS terminal from the current sense comparator during the 100ns interval immediately following the rising edge of the OUT pin. This digital filtering, also called leading-edge blanking, means that in most applications, no analog filtering (RC filter) is required on CS. Compared to an external RC filter technique, the leading-edge blanking provides a smaller effective CS to OUT propagation delay. Note, however, that the minimum non-zero On-Time of the OUT signal is directly affected by the leading-edge-blanking and the CS to OUT propagation delay.

The over-current comparator is only intended for fault sensing, and exceeding the over-current threshold will cause a soft start cycle.

RC: RC is the oscillator timing pin. For fixed frequency operation, set timing capacitor charging current by connecting a resistor from REF to RC. Set frequency by connecting a timing capacitor from RC to GND. For best performance, keep the timing capacitor lead to GND as short and direct as possible. If possible, use separate ground traces for the timing capacitor and all other functions.

The frequency of oscillation can be estimated with the following equations:

UCCx813-0/-1/-2/-4: $F = \frac{1.5}{R \times C}$

UCCx813-3, UCCx813-5: $F = \frac{1.0}{R \times C}$

where frequency is in Hz, resistance is in ohms, and capacitance is in farads. The recommended range of timing resistors is between 10k and 200k and timing capacitor is 100pF to 1000pF. Never use a timing resistor less than 10k.

GND: GND is reference ground and power ground for all functions on this part.

OUT: OUT is the output of a high-current power driver capable of driving the gate of a power MOSFET with peak

PIN DESCRIPTIONS (cont.)

currents exceeding ±750mA. OUT is actively held low when VCC is below the UVLO threshold.

The high-current power driver consists of FET output devices, which can switch all of the way to GND and all of the way to VCC. The output stage also provides a very low impedance to overshoot and undershoot. This means that in many cases, external schottky clamp diodes are not required.

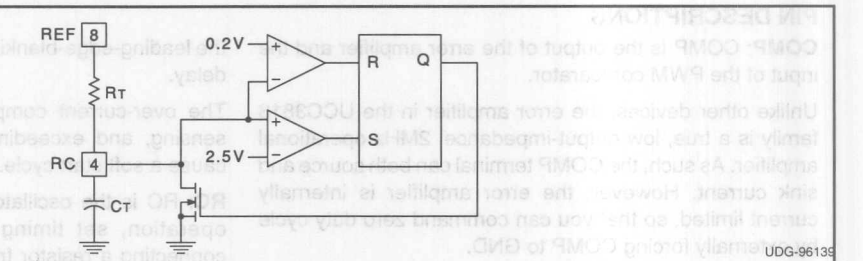
VCC: VCC is the power input connection for this device. In normal operation VCC is powered through a current limiting resistor. Although quiescent VCC current is very low, total supply current will be higher, depending on OUT current. Total VCC current is the sum of quiescent VCC current and the average OUT current. Knowing the operating frequency and the MOSFET gate charge (Qg), average OUT current can be calculated from: $I_{OUT} = Q_g \times F$.

To prevent noise problems, bypass VCC to GND with a ceramic capacitor as close to the VCC pin as possible. An electrolytic capacitor may also be used in addition to the ceramic capacitor.

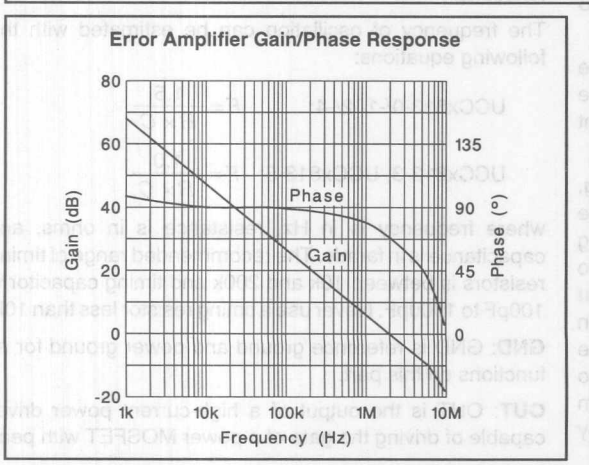
REF: REF is the voltage reference for the error amplifier and also for many other functions on the IC. REF is also used as the logic power supply for high speed switching logic on the IC.

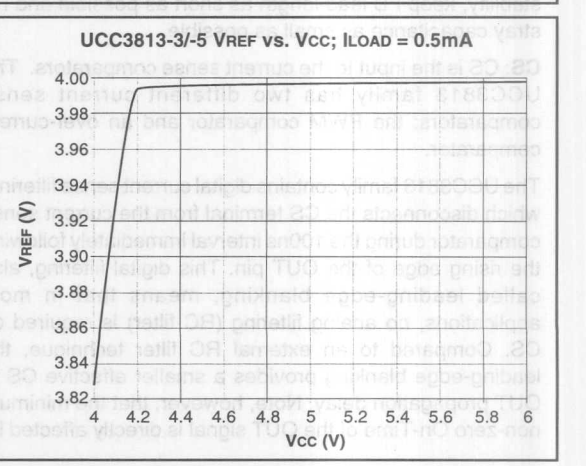
When VCC is greater than 1V and less than the UVLO threshold, REF is pulled to ground through a 5k ohm resistor. This means that REF can be used as a logic output indicating power system status. It is important for reference stability that REF is bypassed to GND with a ceramic capacitor as close to the pin as possible. An electrolytic capacitor may also be used in addition to the ceramic capacitor. A minimum of 0.1µF ceramic is required. Additional REF bypassing is required for external loads greater than 2.5mA on the reference.

OSCILLATOR

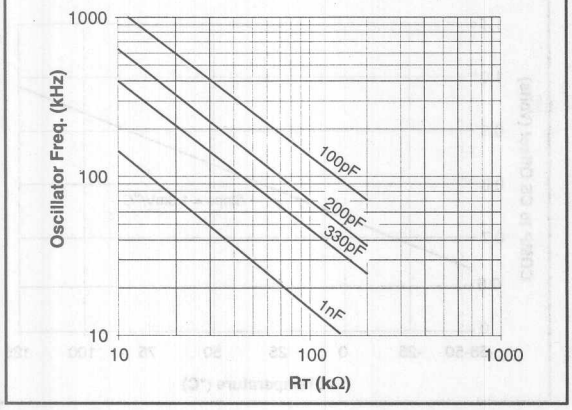


The UCC3813-0/-1/-2/-3/-4/-5 oscillator generates a sawtooth waveform on RC. The rise time is set by the time constant of RT and CT. The fall time is set by CT and an internal transistor on-resistance of approximately 125Ω. During the fall time, the output is off and the maximum duty cycle is reduced below 50% or 100% depending on the part number. Larger timing capacitors increase the discharge time and reduce the maximum duty cycle and frequency.

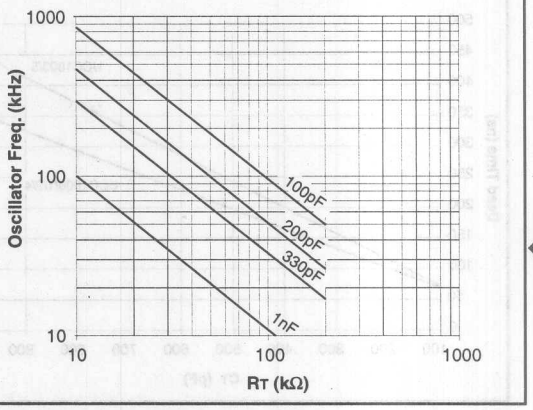




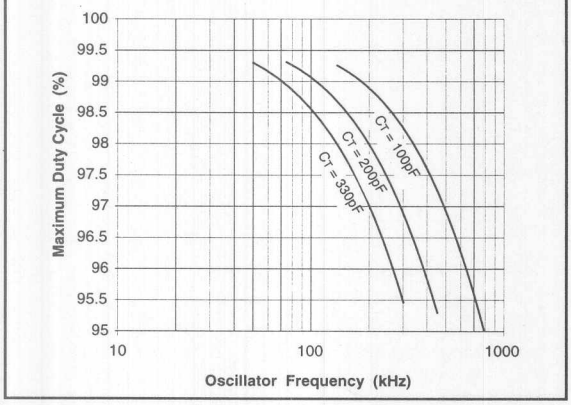
UCC3813-0/-1/-2/-4 Oscillator Frequency vs. RT and CT



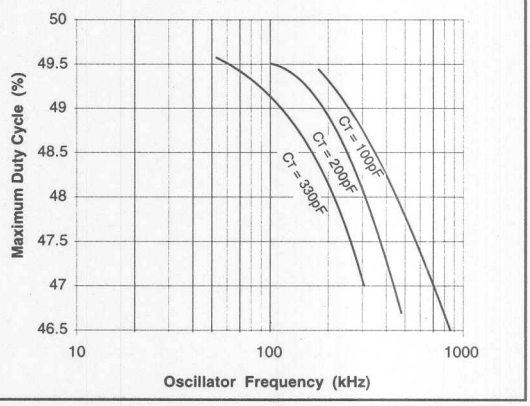
UCC3813-3/-5 Oscillator Frequency vs. RT and CT



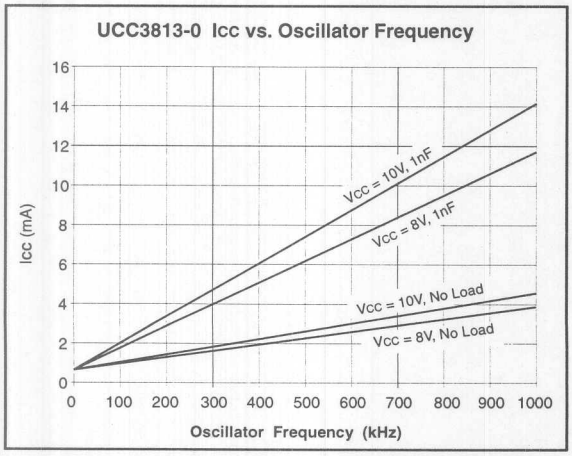
UCC3813-0/-2/-3 Max. Duty Cycle vs. Oscillator Frequency



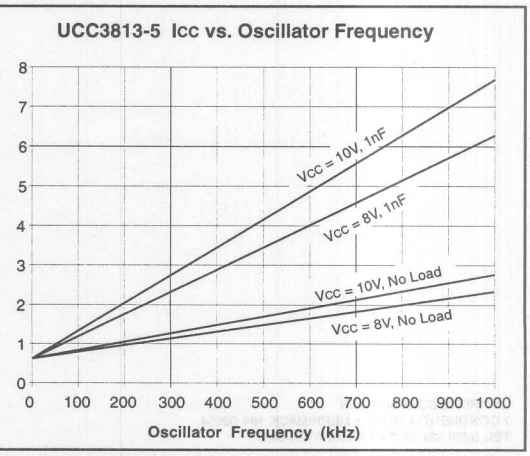
UCC3813-1/-4/-5 Max. Duty Cycle vs. Oscillator Frequency

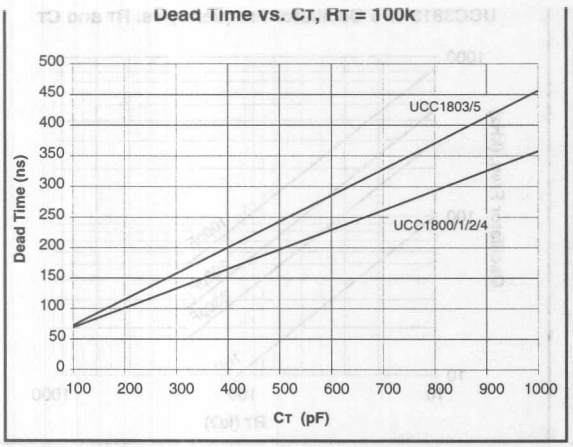


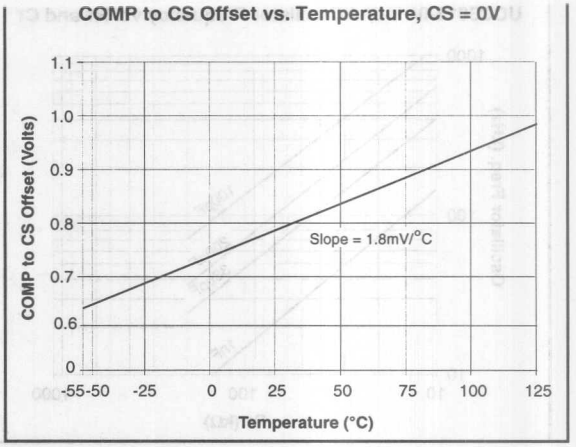
UCC3813-0 Icc vs. Oscillator Frequency



UCC3813-5 Icc vs. Oscillator Frequency







UNITRODE CORPORATION
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UNITRODE

UC1823
UC2823
UC3823

High Speed PWM Controller

FEATURES

- Compatible with Voltage or Current-Mode Topologies
- Practical Operation @ Switching Frequencies to 1.0MHz
- 50ns Propagation Delay to Output
- High Current Totem Pole Output (1.5A peak)
- Wide Bandwidth Error Amplifier
- Fully Latched Logic with Double Pulse Suppression
- Pulse-by-Pulse Current Limiting
- Soft Start/Max. Duty Cycle Control
- Under-Voltage Lockout with Hysteresis
- Low Start Up Current (1.1mA)
- Trimmed Bandgap Reference (5.1V ±1%)

DESCRIPTION

The UC1823 family of PWM control ICs is optimized for high frequency switched mode power supply applications. Particular care was given to minimizing propagation delays through the comparators and logic circuitry while maximizing bandwidth and slew rate of the error amplifier. This controller is designed for use in either current-mode or voltage-mode systems with the capability for input voltage feed-forward.

Protection circuitry includes a current limit comparator, a TTL compatible shutdown port, and a soft start pin which will double as a maximum duty cycle clamp. The logic is fully latched to provide jitter free operation and prohibit multiple pulses at the output. An under-voltage lockout section with 800mV of hysteresis assures low start up current. During under-voltage lockout, the output is high impedance. The current limit reference (pin 11) is a DC input voltage to the current limit comparator. Consult specifications for details.

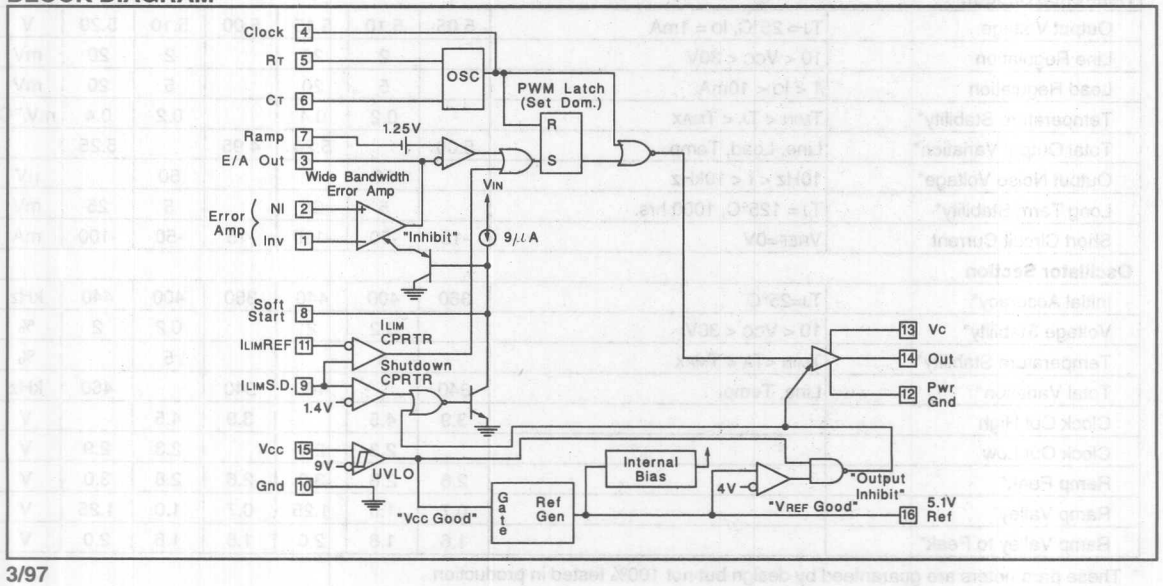
These devices feature a totem pole output designed to source and sink high peak currents from capacitive loads, such as the gate of a power MOSFET. The on state is defined as a high level.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Pins 15, 13) 30V
Output Current, Source or Sink (Pin14)
DC 0.5A
Pulse (0.5µs) 2.0A
Analog Inputs (Pins 1, 2, 7, 8, 9, 11) ..... -0.3V to +6V
Clock Output Current (Pin 4) ..... -5mA
Error Amplifier Output Current (Pin 3) 5mA
Soft Start Sink Current (Pin 8) 20mA
Oscillator Charging Current (Pin 5) ..... -5mA
Power Dissipation at T_A = 60 °C 1W
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10 seconds) ..... 300°C

Note: All voltages are with respect to ground, Pin 10.
Currents are positive into the specified terminal.
Consult Packaging Section of Databook for thermal limitations and considerations of packages.

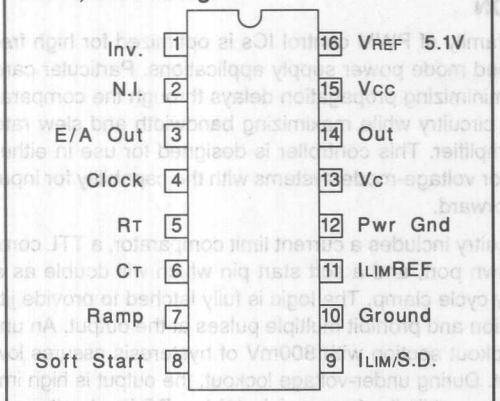
BLOCK DIAGRAM



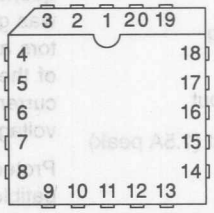
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CONNECTION DIAGRAMS

DIL-16, SOIC-16 (TOP VIEW)
J or N, DW Package



PLCC-20, LCC-20 (TOP VIEW)
Q, L Package



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
Inv.	2
N.I.	3
E/A Out	4
Clock	5
N/C	6
RT	7
CT	8
Ramp	9
Soft start	10
N/C	11
ILIM/S.D.	12
Ground	13
ILIM REF	14
PWR Gnd	15
N/C	16
Vc	17
OUT	18
Vcc	19
VREF 5.1V	20

ELECTRICAL CHARACTERISTICS: Unless otherwise noted, these specifications apply for R_T = 3.65k, C_T = 1nF, V_{CC} = 15V, 0°C < T_A < +70°C for the UC3823, -25°C < T_A < +85°C for the UC2823, and -55°C < T_A < +125°C for the UC1823, T_A = T_J.

PARAMETER	TEST CONDITIONS	UC1823 UC2823			UC3823			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Reference Section								
Output Voltage	T_J = 25°C, Io = 1mA	5.05	5.10	5.15	5.00	5.10	5.20	V
Line Regulation	10 < V_{CC} < 30V		2	20		2	20	mV
Load Regulation	1 < Io < 10mA		5	20		5	20	mV
Temperature Stability*	T_{MIN} < T_A < T_{MAX}		0.2	0.4		0.2	0.4	mV/°C
Total Output Variation*	Line, Load, Temp.	5.00		5.20	4.95		5.25	
Output Noise Voltage*	10Hz < f < 10kHz		50			50		µV
Long Term Stability*	T_J = 125°C, 1000 hrs.		5	25		5	25	mV
Short Circuit Current	V_{REF}=0V	-15	-50	-100	-15	-50	-100	mA
Oscillator Section								
Initial Accuracy*	T_J=25°C	360	400	440	360	400	440	kHz
Voltage Stability*	10 < V_{CC} < 30V		0.2	2		0.2	2	%
Temperature Stability*	T_{MIN} <T_A < T_{MAX}		5			5		%
Total Variation*	Line, Temp.	340		460	340		460	kHz
Clock Out High		3.9	4.5		3.9	4.5		V
Clock Out Low			2.3	2.9		2.3	2.9	V
Ramp Peak*		2.6	2.8	3.0	2.6	2.8	3.0	V
Ramp Valley*		0.7	1.0	1.25	0.7	1.0	1.25	V
Ramp Valley to Peak*		1.6	1.8	2.0	1.6	1.8	2.0	V

* These parameters are guaranteed by design but not 100% tested in production.

ELECTRICAL CHARACTERISTICS: Unless otherwise noted, these specifications apply for R_T = 3.65k, C_T = 1nF, V_{CC} = 15V, 0°C < T_A < +70°C for the UC3823, -25°C < T_A < +85°C for the UC2823, and -55°C < T_A < +125°C for the UC1823, T_A = T_J.

PARAMETER	TEST CONDITIONS	UC1823 UC2823			UC3823			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Error Amplifier Section								
Input Offset Voltage				10			15	mV
Input Bias Current			0.6	3		0.6	3	µA
Input Offset Current			0.1	1		0.1	1	µA
Open Loop Gain	1 < V_O < 4V	60	95		60	95		dB
CMRR	1.5 < V_{CM} < 5.5V	75	95		75	95		dB
PSRR	10 < V_{CC} < 30V	85	110		85	110		dB
Output Sink Current	$V_{PIN\ 3}$ =1V	1	2.5		1	2.5		mA
Output Source Current	$V_{PIN\ 3}$ = 4V	-0.5	-1.3		-0.5	-1.3		mA
Output High Voltage	$I_{PIN\ 3}$ = –0.5mA	4.0	4.7	5.0	4.0	4.7	5.0	V
Output Low Voltage	$I_{PIN\ 3}$ = 1mA	0	0.5	1.0	0	0.5	1.0	V
Unity Gain Bandwidth*		3	5.5		3	5.5		MHz
Slew Rate*		6	12		6	12		V/µS
PWM Comparator Section								
Pin 7 Bias Current	$V_{PIN\ 7}$ = 0V		-1	-5		-1	-5	µA
Duty Cycle Range		0		80	0		85	%
Pin 3 Zero D.C. Threshold	$V_{PIN\ 7}$ = 0V	1.1	1.25		1.1	1.25		V
Delay to Output*			50	80		50	80	ns
Soft-Start Section								
Charge Current	$V_{PIN\ 8}$ = 0.5V	3	9	20	3	9	20	µA
Discharge Current	$V_{PIN\ 8}$ = 1V	1			1			mA
Current Limit/Shutdown Section								
Pin 9 Bias Current	0 < $V_{PIN\ 9}$ < 4V			±10			±10	µA
Current Limit Offset	$V_{PIN\ 11}$ = 1.1V			15			15	mV
Current Limit Common Mode Range ($V_{PIN\ 11}$)		1.0		1.25	1.0		1.25	V
Shutdown Threshold		1.25	1.40	1.55	1.25	1.40	1.55	V
Delay to Output*			50	80		50	80	ns
Output Section								
Output Low Level	I_{OUT} = 20mA		0.25	0.40		0.25	0.40	V
	I_{OUT} = 200mA		1.2	2.2		1.2	2.2	V
Output High Level	I_{OUT} = –20mA	13.0	13.5		13.0	13.5		V
	I_{OUT} = –200mA	12.0	13.0		12.0	13.0		V
Collector Leakage	V_C = 30V		100	500		100	500	µA
Rise/Fall Time*	C_L = 1nF		30	60		30	60	ns
Under-Voltage Lockout Section								
Start Threshold		8.8	9.2	9.6	8.8	9.2	9.6	V
UVLO Hysteresis		0.4	0.8	1.2	0.4	0.8	1.2	V
Supply Current								
Start Up Current	V_{CC} = 8V		1.1	2.5		1.1	2.5	mA
I_{CC}	$V_{PIN\ 1}$, $V_{PIN\ 7}$, $V_{PIN\ 9}$ =0V, $V_{PIN\ 2}$ = 1V		22	33		22	33	mA

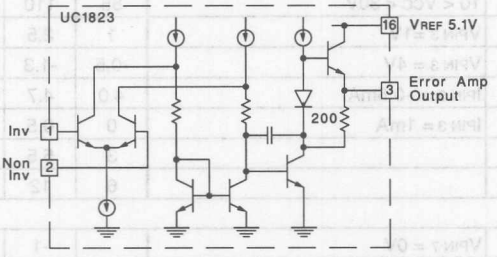
* These parameters are guaranteed by design but not 100% tested in production.

UC1823 PRINTED CIRCUIT BOARD LAYOUT CONSIDERATIONS

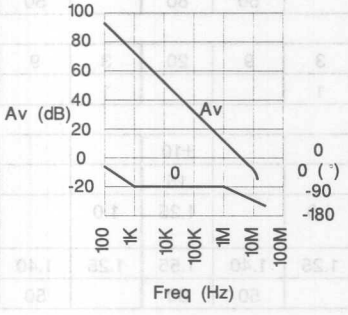
High speed circuits demand careful attention to layout and component placement. To assure proper performance of the UC1823, follow these rules. 1) Use a ground plane. 2) Damp or clamp parasitic inductive kick energy from the gate of driven MOSFET. Don't allow the output pins to ring below ground. A series gate resistor or a shunt 1 Amp Schottky diode at the output pin will serve this purpose. 3) Bypass V_{CC}, V_C, and V_{REF}. Use 0.1µF monolithic ceramic capacitors with low equivalent series inductance. Allow less than 1 cm of total lead length for each capacitor between the bypassed pin and the ground plane. 4) Treat the timing capacitor, C_T, like a bypass capacitor.

ERROR AMPLIFIER CIRCUIT

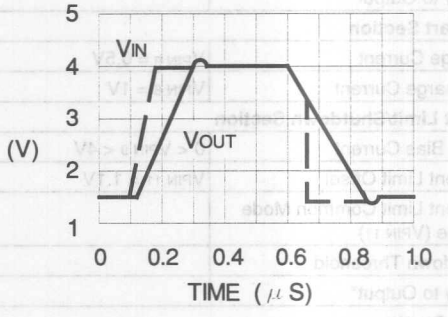
Simplified Schematic



Open Loop Frequency Response

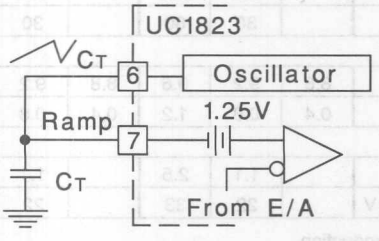


Unity Gain Slew Rate

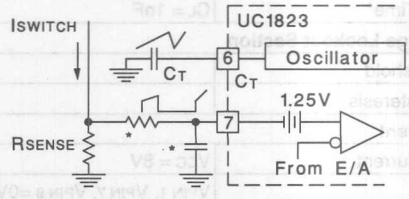


PWM APPLICATIONS

Conventional (Voltage Mode)

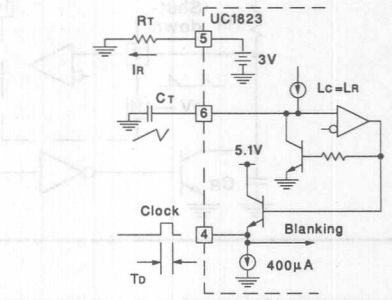


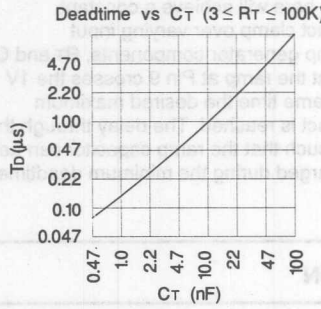
Current-Mode

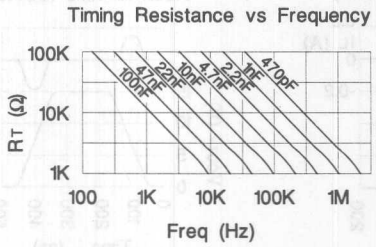


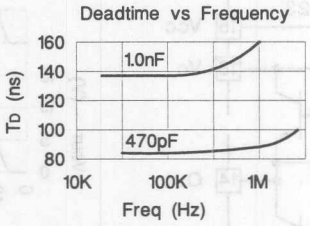
* A small filter may be required to suppress switch

OSCILLATOR CIRCUIT



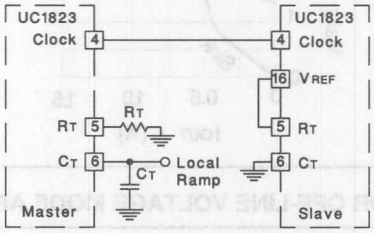




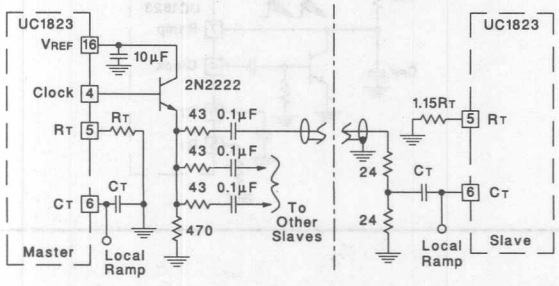


SYNCHRONIZED OPERATION

Two Units in Close Proximity

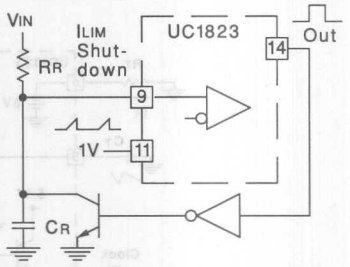


Generalized Synchronization

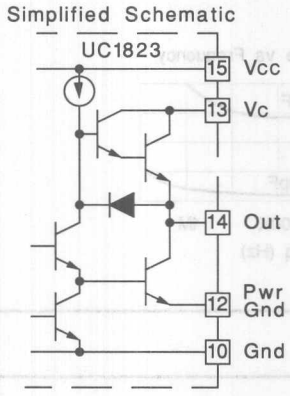


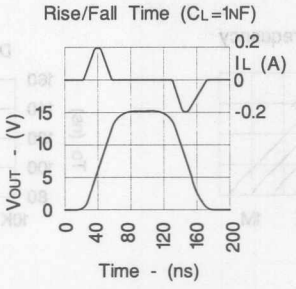
CONSTANT VOLT-SECOND CLAMP CIRCUIT

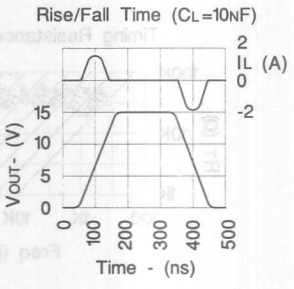
The circuit shown here will achieve a constant volt-second product clamp over varying input voltages. The ramp generator components, R_T and C_R are chosen so that the ramp at Pin 9 crosses the 1V threshold at the same time the desired maximum volt-second product is reached. The delay through the inverter must be such that the ramp capacitor can be completely discharged during the minimum deadtime.

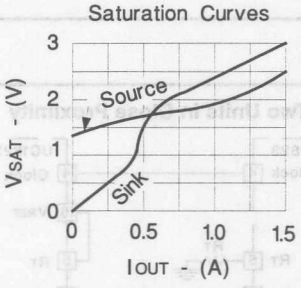


OUTPUT SECTION

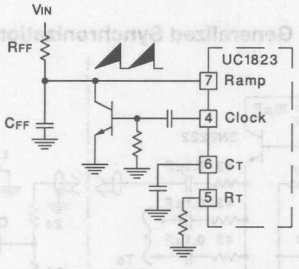








FEED FORWARD TECHNIQUE FOR OFF-LINE VOLTAGE MODE APPLICATION



UNITRODE CORPORATION
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High Speed PWM Controller

FEATURES

- Improved versions of the UC3823/UC3825 PWMs
- Compatible with Voltage or Current-Mode Topologies
- Practical Operation at Switching Frequencies to 1MHz
- 50ns Propagation Delay to Output
- High Current Dual Totem Pole Outputs (2A Peak)
- Trimmed Oscillator Discharge Current
- Low 100µA Startup Current
- Pulse-by-Pulse Current Limiting Comparator
- Latched Overcurrent Comparator With Full Cycle Restart

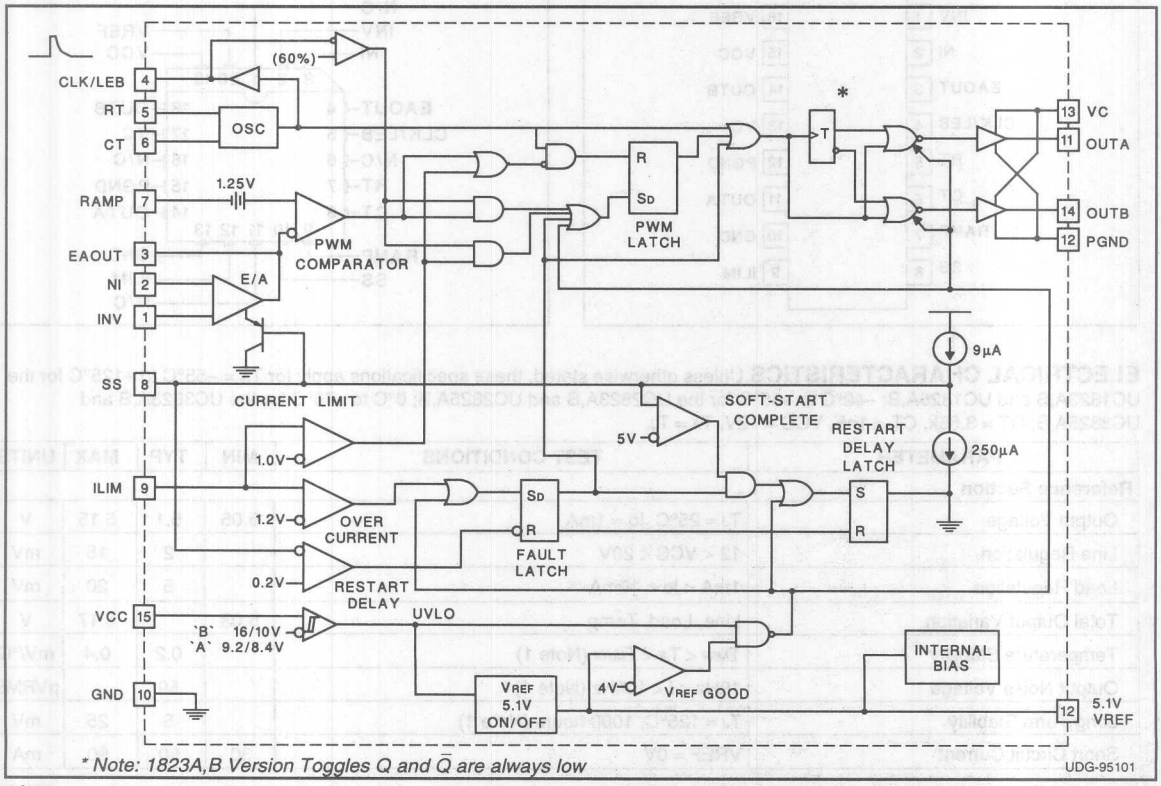
DESCRIPTION

The UC3823A & B and the UC3825A & B family of PWM control ICs are improved versions of the standard UC3823 & UC3825 family. Performance enhancements have been made to several of the circuit blocks. Error amplifier gain bandwidth product is 12MHz while input offset voltage is 2mV. Current limit threshold is guaranteed to a tolerance of 5%. Oscillator discharge current is specified at 10mA for accurate dead time control. Frequency accuracy is improved to 6%. Startup supply current, typically 100µA, is ideal for off-line applications. The output drivers are redesigned to actively sink current during UVLO at no expense to the startup current specification. In addition each output is capable of 2A peak currents during transitions.

Functional improvements have also been implemented in this family. The UC3825 shutdown comparator is now a high-speed overcurrent comparator with a threshold of 1.2V. The overcurrent comparator sets a latch that ensures full discharge of the soft start capacitor before allowing a restart. While the fault latch is set, the outputs are in the low state. In the event of continuous faults, the soft start capacitor is fully charged before discharge to insure that the fault frequency does not exceed the designed soft start period. The UC3825 Clock pin has become CLK/LEB. This pin combines the functions of clock output and leading edge blanking adjustment and has been buffered for easier interfacing.

continued

BLOCK DIAGRAM



DESCRIPTION (cont.)

The UC3825A,B has dual alternating outputs and the same pin configuration of the UC3825. The UC3823A,B outputs operate in phase with duty cycles from zero to less than 100%. The pin configuration of the UC3823A,B is the same as the UC3823 except pin 11 is now an output pin instead of the reference pin to the current limit comparator. "A" version parts have UVLO thresholds identical to the original UC3823/25. The "B" versions have UVLO thresholds of 16 and 10V, intended for ease of use in off-line applications.

Consult Application Note U-128 for detailed technical and applications information. Contact the factory for further packaging and availability information.

Device	UVLO	DMAX
UC3823A	9.2V/8.4V	< 100%
UC3823B	16V/10V	< 100%
UC3825A	9.2V/8.4V	< 50%
UC3825B	16V/10V	< 50%

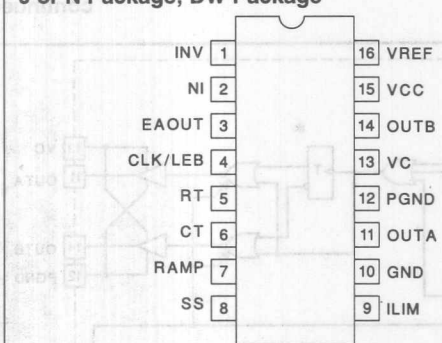
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (VC, VCC) 22V
Output Current, Source or Sink (Pins OUTA, OUTB)
DC 0.5A
Pulse (0.5µs) 2.2A
Power Ground (PGND) ..... ±0.2V
Analog Inputs
(INV, NI, RAMP) ..... –0.3V to 7V
(ILIM, SS) ..... –0.3V to 6V
Clock Output Current (CLK/LEB) ..... –5mA
Error Amplifier Output Current (EAOUT) 5mA
Soft Start Sink Current (SS) 20mA
Oscillator Charging Current (RT) ..... –5mA
Power Dissipation at TA = 60°C 1W
Storage Temperature Range ..... –65°C to +150°C
Junction Temperature ..... –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

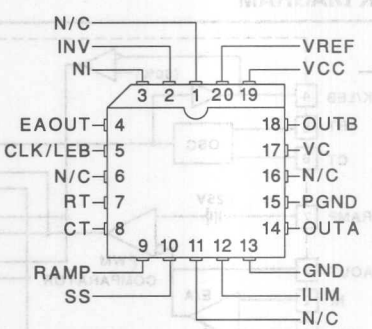
All currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAMS

DIL-16, SOIC-16, (Top View)
J or N Package; DW Package



PLCC-20, LCC-20, (Top View)
Q, L Packages



ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply for TA = –55°C to +125°C for the UC1823A,B and UC1825A,B; –40°C to +85°C for the UC2823A,B and UC2825A,B; 0°C to +70°C for the UC3823A,B and UC3825A,B; RT = 3.65k, CT = 1nF, VCC = 12V, TA = TJ.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Reference Section					
Output Voltage	TJ = 25°C, Io = 1mA	5.05	5.1	5.15	V
Line Regulation	12 < VCC < 20V		2	15	mV
Load Regulation	1mA < Io < 10mA		5	20	mV
Total Output Variation	Line, Load, Temp	5.03		5.17	V
Temperature Stability	TMIN < TA < TMAX (Note 1)		0.2	0.4	mV/°C
Output Noise Voltage	10Hz < f < 10kHz (Note 1)		50		µVRMS
Long Term Stability	TJ = 125°C, 1000 hours (Note 1)		5	25	mV
Short Circuit Current	VREF = 0V	30	60	90	mA

ELECTRICAL CHARACTERISTICS (cont.) Unless otherwise stated, these specifications apply for T_A = –55°C to +125°C for the UC1823A,B and UC1825A,B; –40°C to +85°C for the UC2823A,B and UC2825A,B; 0°C to +70°C for the UC3823A,B and UC3825A,B; RT = 3.65k, CT = 1nF, VCC = 12V, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator Section					
Initial Accuracy	T_J = 25°C (Note 1)	375	400	425	kHz
Total Variation	Line, Temperature (Note 1)	350		450	kHz
Voltage Stability	12V < VCC < 20V			1	%
Temperature Stability	T_{MIN} < T_A < T_{MAX} (Note 1)		5		%
Initial Accuracy	RT = 6.6k, CT = 220pF T_A = 25°C (Note 1)	0.9	1	1.1	MHz
Total Variation	RT = 6.6k, CT = 220pF (Note 1)	0.85		1.15	MHz
Clock Out High		3.7	4		V
Clock Out Low			0	0.2	V
Ramp Peak		2.6	2.8	3	V
Ramp Valley		0.7	1	1.25	V
Ramp Valley to Peak		1.6	1.8	2	V
Oscillator Discharge Current	RT = Open, V_{CT} = 2V	9	10	11	mA
Error Amplifier Section					
Input Offset Voltage			2	10	mV
Input Bias Current			0.6	3	µA
Input Offset Current			0.1	1	µA
Open Loop Gain	1V < Vo < 4V	60	95		dB
CMRR	1.5V < V_{CM} < 5.5V	75	95		dB
PSRR	12V < VCC < 20V	85	110		dB
Output Sink Current	V_{EAOUT} = 1V	1	2.5		mA
Output Source Current	V_{EAOUT} = 4V	–0.5	–1.3		mA
Output High Voltage	I_{EAOUT} = –0.5mA	4.5	4.7	5	V
Output Low Voltage	I_{EAOUT} = 1mA	0	0.5	1	V
Gain Bandwidth Product	F = 200kHz	6	12		MHz
Slew Rate	(Note 1)	6	9		V/µs
PWM Comparator					
RAMP Bias current	V_{RAMP} = 0V		–1	–8	µA
Minimum Duty Cycle				0	%
Maximum Duty Cycle		85			%
Leading Edge Blanking	R = 2k, C = 470pF	300	375	450	ns
LEB Resistor	$V_{CLK/LEB}$ = 3V	8.5	10	11.5	kohm
EAOUT Zero D.C. Threshold	V_{RAMP} = 0V	1.1	1.25	1.4	V
Delay to Output	V_{EAOUT} = 2.1V, V_{RAMP} = 0 to 2V Step (Note 1)		50	80	ns
Current Limit/Start Sequence/Fault Section					
Soft Start Charge Current	V_{SS} = 2.5V	8	14	20	µA
Full Soft Start Threshold		4.3	5		V
Restart Discharge Current	V_{SS} = 2.5V	100	250	350	µA
Restart Threshold			0.3	0.5	V
ILIM Bias Current	0 < V_{ILIM} < 2V			15	µA
Current Limit Threshold		0.95	1	1.05	V

ELECTRICAL CHARACTERISTICS (cont.) Unless otherwise stated, these specifications apply for T_A = –55°C to +125°C for the UC1823A,B and UC1825A,B; –40°C to +85°C for the UC2823A,B and UC2825A,B; 0°C to +70°C for the UC3823A,B and UC3825A,B; RT = 3.65k, CT = 1nF, VCC = 12V, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Current Limit/Start Sequence/Fault Section (cont.)					
Over Current Threshold		1.14	1.2	1.26	V
ILIM Delay to Output	V_{ILIM} = 0 to 2V Step (Note 1)		50	80	ns
Output Section					
Output Low Saturation	I_{OUT} = 20mA		0.25	0.4	V
	I_{OUT} = 200mA		1.2	2.2	V
Output High Saturation	I_{OUT} = 20mA		1.9	2.9	V
	I_{OUT} = 200mA		2	3	V
UVLO Output Low Saturation	I_O = 20mA		0.8	1.2	V
Rise/Fall Time	C_L = 1nF (Note 1)		20	45	ns
UnderVoltage Lockout					
Start Threshold	UCX823B and X825B only		16	17	V
Stop Threshold	UCX823B and X825B only	9	10		V
UVLO Hysteresis	UCX823B and X825B only	5	6	7	V
Start Threshold	UCX823A and X825A only	8.4	9.2	9.6	V
UVLO Hysteresis	UCX823A and X825A only	0.4	0.8	1.2	V
Supply Current					
Startup Current	VC = VCC = V_{TH}(start) - 0.5V		100	300	µA
Icc			28	36	mA

Note 1: Guaranteed by design. Not 100% tested in production.

APPLICATIONS INFORMATION

OSCILLATOR

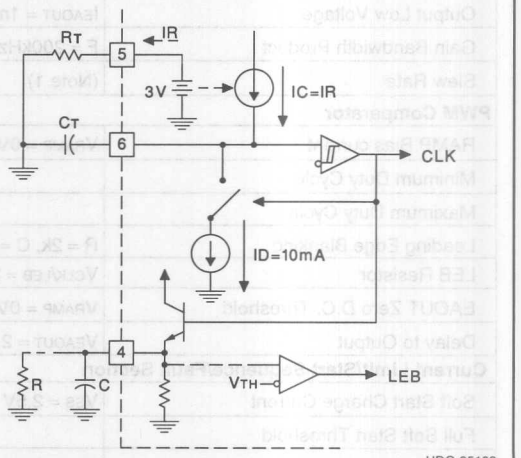
The UC3823A,B/3825A,B oscillator is a saw tooth. The rising edge is governed by a current controlled by the RT pin and value of capacitance at the CT pin. The falling edge of the sawtooth sets dead time for the outputs. Selection of RT should be done first, based on desired maximum duty cycle. CT can then be chosen based on desired frequency, RT, and D_{MAX}. The design equations are:

$$RT = \frac{3V}{(10mA)(1 - D_{MAX})}$$

$$CT = \frac{(1.6 \bullet D_{MAX})}{(RT \bullet F)}$$

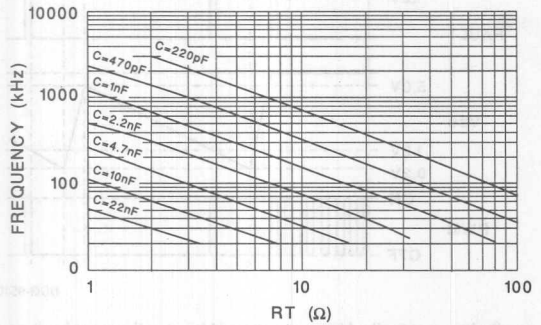
Recommended values for RT range from 1k to 100k. Control of D_{MAX} less than 70% is not recommended.

Oscillator



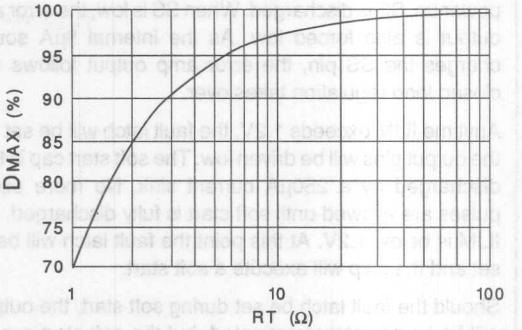
OSCILLATOR (cont.)

Oscillator Frequency vs. RT and CT Curve



UDG-95103

Maximum Duty Cycle vs RT Curve



UDG-95104

LEADING EDGE BLANKING

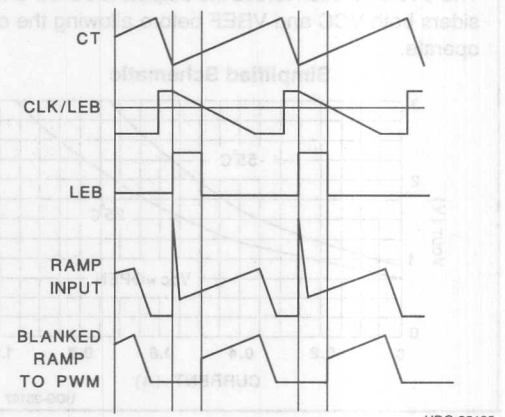
The UC3823A,B/3825A,B performs fixed frequency pulse width modulation control. The UC3823A,B outputs operate together at the switching frequency and can vary from 0 to some value less than 100%. The UC3825A,B outputs are alternately controlled. During every other cycle, one output will be off. Each output then, switches at one-half the oscillator frequency, varying in duty cycle from 0 to less than 50%.

To limit maximum duty cycle, the internal clock pulse blanks both outputs low during the discharge time of the oscillator. On the falling edge of the clock, the appropriate output(s) is driven high. The end of the pulse is controlled by the PWM comparator, current limit comparator, or the overcurrent comparator.

Normally the PWM comparator will sense a ramp crossing a control voltage (error amp output) and terminate the pulse. Leading edge blanking (LEB) causes the PWM comparator to be ignored for a fixed amount of time after the start of the pulse. This allows noise inherent with switched mode power conversion to be rejected. The PWM ramp input may not require any filtering as result of leading edge blanking.

To program a Leading Edge Blanking period, connect a capacitor, C, to CLK/LEB. The discharge time set by C and the internal 10k resistor will determine the blanked interval. The 10k resistor has a 10% tolerance. For more accuracy, an external 2k 1% resistor, R, can be added, resulting in an equivalent resistance of 1.66k with a tolerance of 2.4%. The design equation is:

LEB Operational Waveforms



UDG-95105

$$t_{LEB} = 0.5 \bullet (R \mid\mid 10k) \bullet C.$$

Values of R less than 2k should not be used

Leading edge blanking is also applied to the current limit comparator. After LEB, if the ILIM pin exceeds the one volt threshold, the pulse is terminated. The over current comparator, however, is not blanked. It will catch catastrophic over current faults without a blanking delay. Any time the ILIM pin exceeds 1.2V, the fault latch will be set and the outputs driven low. For this reason, some noise filtering may be required on the ILIM pin.

APPLICATIONS INFORMATION (cont.)

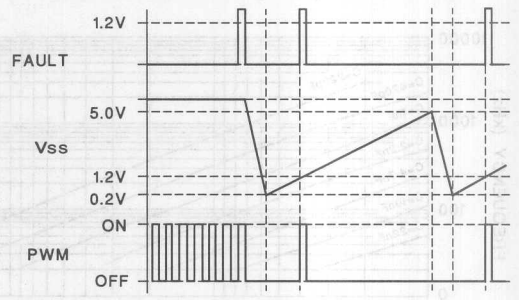
UVLO, SOFT START AND FAULT MANAGEMENT

Soft start is programmed by a capacitor on the SS pin. At power up, SS is discharged. When SS is low, the error amp output is also forced low. As the internal 9µA source charges the SS pin, the error amp output follows until closed loop regulation takes over.

Anytime ILIM exceeds 1.2V, the fault latch will be set and the output pins will be driven low. The soft start cap is then discharged by a 250µA current sink. No more output pulses are allowed until soft start is fully discharged, and ILIM is below 1.2V. At this point the fault latch will be reset and the chip will execute a soft start.

Should the fault latch be set during soft start, the outputs will be immediately terminated, but the soft start cap will not be discharged until it has been fully charged. This results in a controlled hiccup interval for continuous fault conditions.

Soft Start and Fault Waveforms

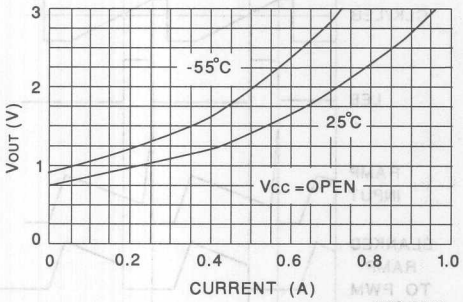


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ACTIVE LOW OUTPUTS DURING UVLO

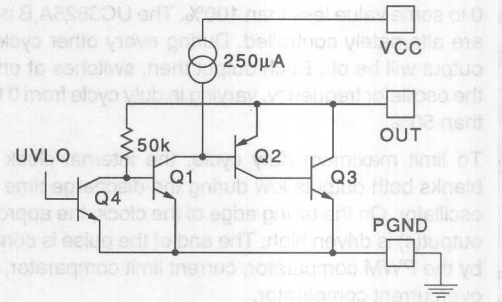
The UVLO function forces the outputs to be low and considers both VCC and VREF before allowing the chip to operate.

Simplified Schematic



UDG-95107

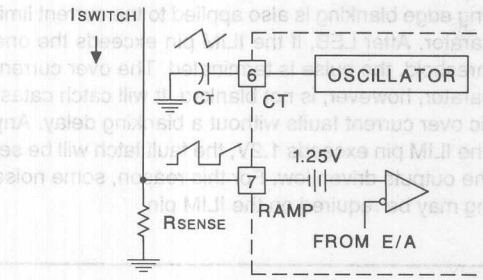
Output V and I During UVLO



UDG-95108

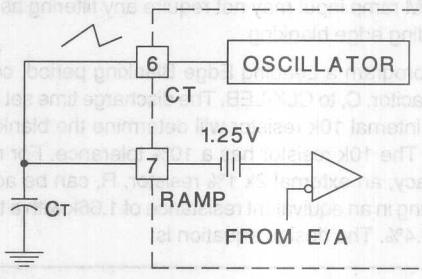
PWM APPLICATIONS

Current Mode



UDG-95109

Voltage Mode



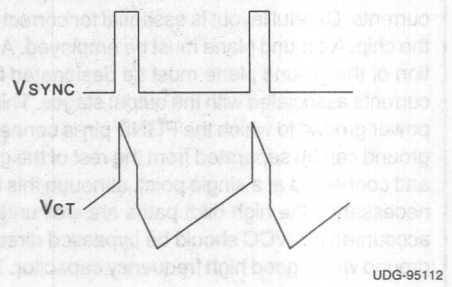
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APPLICATIONS INFORMATION (cont.)

SYNCHRONIZATION

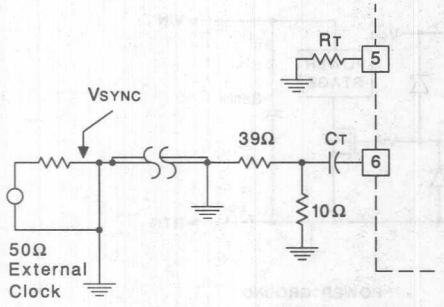
The oscillator can be synchronized by an external pulse inserted in series with the timing capacitor. Program the free running frequency of the oscillator to be 10 to 15% slower than the desired synchronous frequency. The pulse width should be greater than 10ns and less than half the discharge time of the oscillator. The rising edge of the CLK/LEB pin can be used to generate a synchronizing pulse for other chips. Note that, the CLK/LEB pin will no longer accept an incoming synchronizing signal.

Operational Waveforms



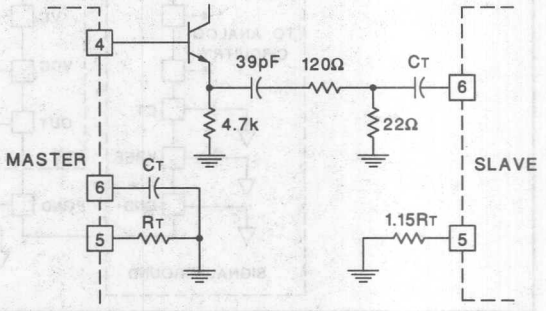
UDG-95112

General Oscillator Synchronization



UDG-95111

Two Units



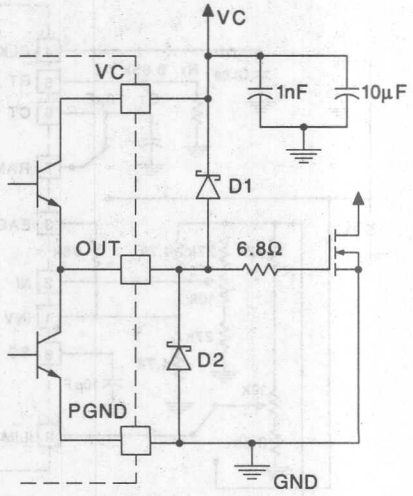
UDG-95113

HIGH CURRENT OUTPUTS

Each totem pole output of the UC3823A,B and UC3825A,B can deliver a 2 amp peak current into a capacitive load. The output can slew a 1000pF capacitor 15 volts in approximately 20 nanoseconds. Separate collector supply (VC) and power ground (PGND) pins help decouple the IC's analog circuitry from the high power gate drive noise. The use of 3 Amp Schottky diodes (1N5120, USD245 or equivalent) as shown in the figure from each output to both VC and PGND are recommended. The diodes clamp the output swing to the supply rails, necessary with any type of inductive/capacitive load, typical of a MOSFET gate. Schottky diodes must be used because a low forward voltage drop is required. DO NOT USE standard silicon diodes.

Although a "single ended" device, two output drivers are available on the UC3823A,B devices. These can be "paralleled" by the use of a one-half ohm (noninductive) resistor connected in series with each output for a combined peak current of 4 Amps.

Power MOSFET Drive Circuit



D1, D2 = 1N5820

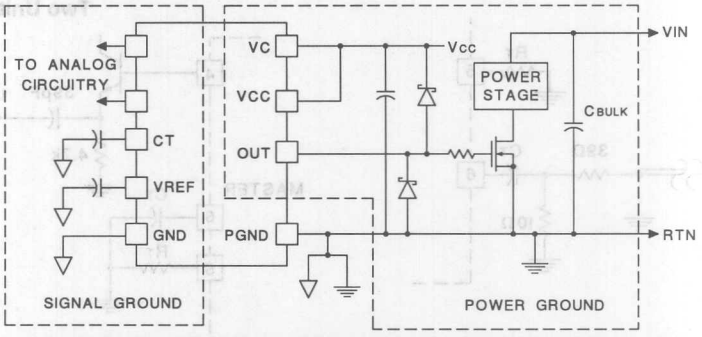
UDG-95114

APPLICATIONS INFORMATION (cont.)

GROUND PLANES

Each output driver of these devices is capable of 2A peak currents. Careful layout is essential for correct operation of the chip. A ground plane must be employed. A unique section of the ground plane must be designated for high di/dt currents associated with the output stages. This point is the power ground to which the PGND pin is connected. Power ground can be separated from the rest of the ground plane and connected at a single point, although this is not strictly necessary if the high di/dt paths are well understood and accounted for. VCC should be bypassed directly to power ground with a good high frequency capacitor. The sources of the power MOSFET should connect to power ground as should the return connection for input power to the system and the bulk input capacitor. The output should be clamped with a high current Schottky diode to both VCC and PGND. Nothing else should be connected to power ground.

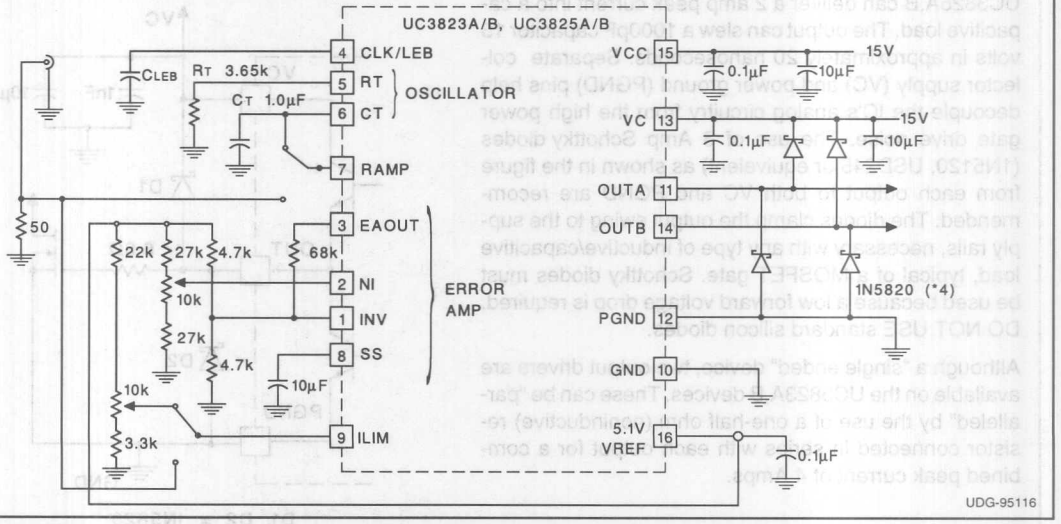
VREF should be bypassed directly to the signal portion of the ground plane with a good high frequency capacitor. Low ESR/ESL ceramic 1µF capacitors are recommended for both VCC and VREF. All analog circuitry should likewise be bypassed to the signal ground plane.



UDG-95115

Open Loop Test Circuit

This test fixture is useful for exercising many of the UC3823A,B, UC3825A,B functions and measuring their specifications. As with any wideband circuit, careful grounding and bypass procedures should be followed. The use of a ground plane is highly recommended.



UDG-95116

UNITRODE CORPORATION
7 CONTINENTAL BLVD.• MERRIMACK, NH 03054
TEL.(603) 424-2410 • FAX (603) 424-3460

High Speed PWM Controller

FEATURES

- Complementary Outputs
- Practical Operation Switching Frequencies to 1MHz
- 50ns Propagation Delay to Output
- High Current Dual Totem Pole Outputs (1.5A Peak)
- Wide Bandwidth Error Amplifier
- Fully Latched Logic with Double Pulse Suppression
- Pulse-by-Pulse Current Limiting
- Soft Start / Max. Duty Cycle Control
- Under-Voltage Lockout with Hysteresis
- Low Start Up Current (1.1 mA)
- Trimmed Bandgap Reference (5.1V ± 1%)

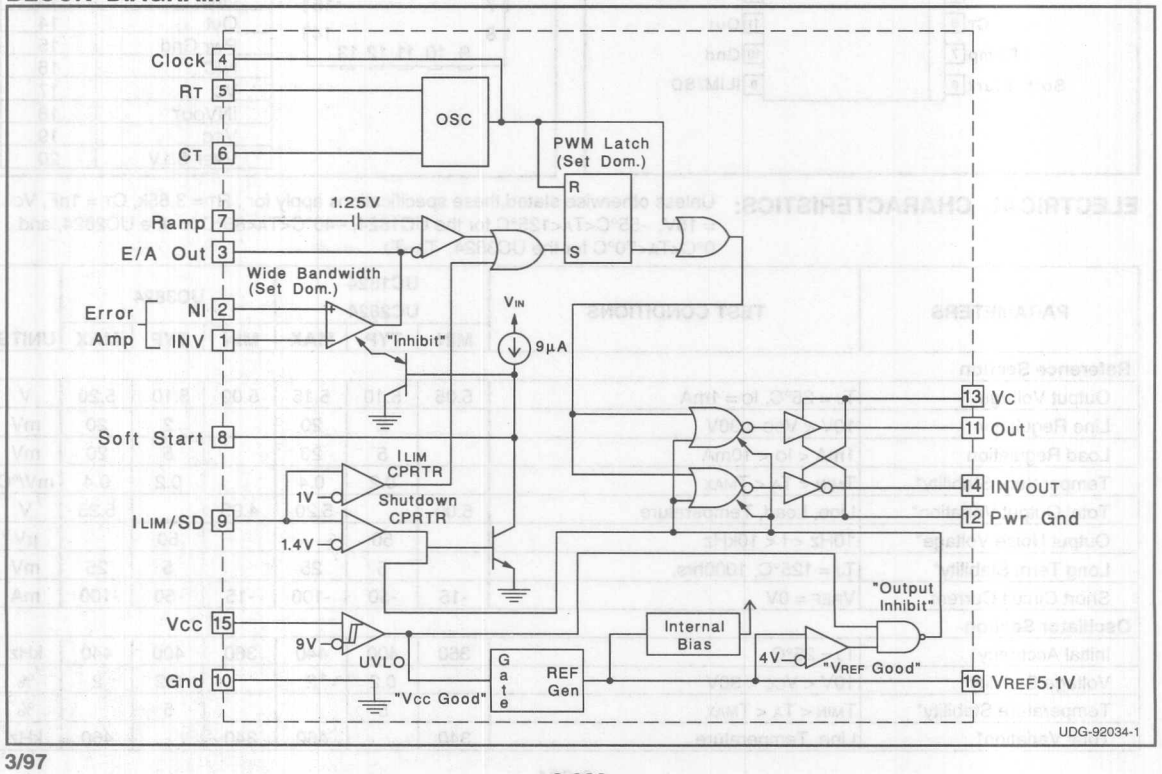
DESCRIPTION

The UC1824 family of PWM control ICs is optimized for high frequency switched mode power supply applications. Particular care was given to minimizing propagation delays through the comparators and logic circuitry while maximizing bandwidth and slew rate of the error amplifier. This controller is designed for use in either current-mode or voltage mode systems with the capability for input voltage feed-forward.

Protection circuitry includes a current limit comparator with a 1V threshold, a TTL compatible shutdown port, and a soft start pin which will double as a maximum duty cycle clamp. The logic is fully latched to provide jitter free operation and prohibit multiple pulses at an output. An under-voltage lockout section with 800mV of hysteresis assures low start up current. During under-voltage lockout, the outputs are high impedance.

These devices feature totem pole outputs designed to source and sink high peak currents from capacitive loads, such as the gate of a power MOSFET. The on state is designed as a high level.

BLOCK DIAGRAM



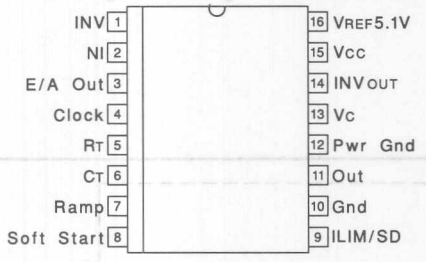
ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (Pins 13, 15) 30V
Output Current, Source or Sink (Pins 11, 14)
DC. 0.5A
Pulse (0.5µs) 2.0A
Analog Inputs
(Pins 1, 2, 7) . . . . . -0.3V to 7V
(Pin 8, 9) . . . . . -0.3V to 6V
Clock Output Current (Pin 4) . . . . . -5mA
Error Amplifier Output Current (Pin 3) 5mA
Soft Start Sink Current (Pin 8) 20mA
Oscillator Charging Current (Pin 5) . . . . . -5mA
Power Dissipation 1W
Storage Temperature Range . . . . . -65°C to +150°C
Lead Temperature (Soldering, 10 seconds) . . . . . 300°C

Note 1: All voltages are with respect to GND (Pin 10); all currents are positive into, negative out of part; pin numbers refer to DIL-16 package.

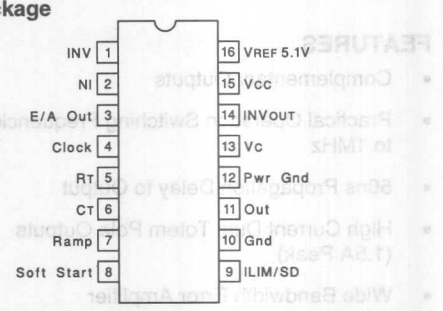
Note 3: Consult Unitrode Integrated Circuit Databook for thermal limitations and considerations of package.

SOIC-16 (Top View)
DW Package

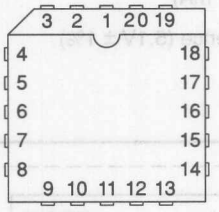


CONNECTION DIAGRAMS

DIL-16 (Top View)
J Or N Package



PLCC-20 & LCC-20
(Top View)
Q & L Packages



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
INV	2
NI	3
E/A Out	4
Clock	5
N/C	6
RT	7
CT	8
Ramp	9
Soft Start	10
N/C	11
ILIM/SD	12
Gnd	13
Out	14
Pwr Gnd	15
N/C	16
VC	17
INVOUT	18
VCC	19
VREF 5.1V	20

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, these specifications apply for , R_T = 3.65k, C_T = 1nF, V_{CC} = 15V, -55°C<T_A<125°C for the UC1824, –40°C<T_A<85°C for the UC2824, and 0°C<T_A<70°C for the UC3824, T_A=T_J.

PARAMETERS	TEST CONDITIONS	UC1824 UC2824			UC3824			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Reference Section								
Output Voltage	T_J = 25°C, I_O = 1mA	5.05	5.10	5.15	5.00	5.10	5.20	V
Line Regulation	10V < V_{CC} < 30V		2	20		2	20	mV
Load Regulation	1mA < I_O < 10mA		5	20		5	20	mV
Temperature Stability*	T_{MIN} < T_A < T_{MAX}		0.2	0.4		0.2	0.4	mV/°C
Total Output Variation*	Line, Load, Temperature	5.00		5.20	4.95		5.25	V
Output Noise Voltage*	10Hz < f < 10kHz		50			50		µV
Long Term Stability*	T_J = 125°C, 1000hrs.		5	25		5	25	mV
Short Circuit Current	V_{REF} = 0V	-15	-50	-100	-15	-50	-100	mA
Oscillator Section								
Initial Accuracy*	T_J = 25°C	360	400	440	360	400	440	kHz
Voltage Stability*	10V < V_{CC} < 30V		0.2	2		0.2	2	%
Temperature Stability*	T_{MIN} < T_A < T_{MAX}		5			5		%
Total Variation*	Line, Temperature	340		460	340		460	kHz

ELECTRICAL CHARACTERISTICS (cont.)

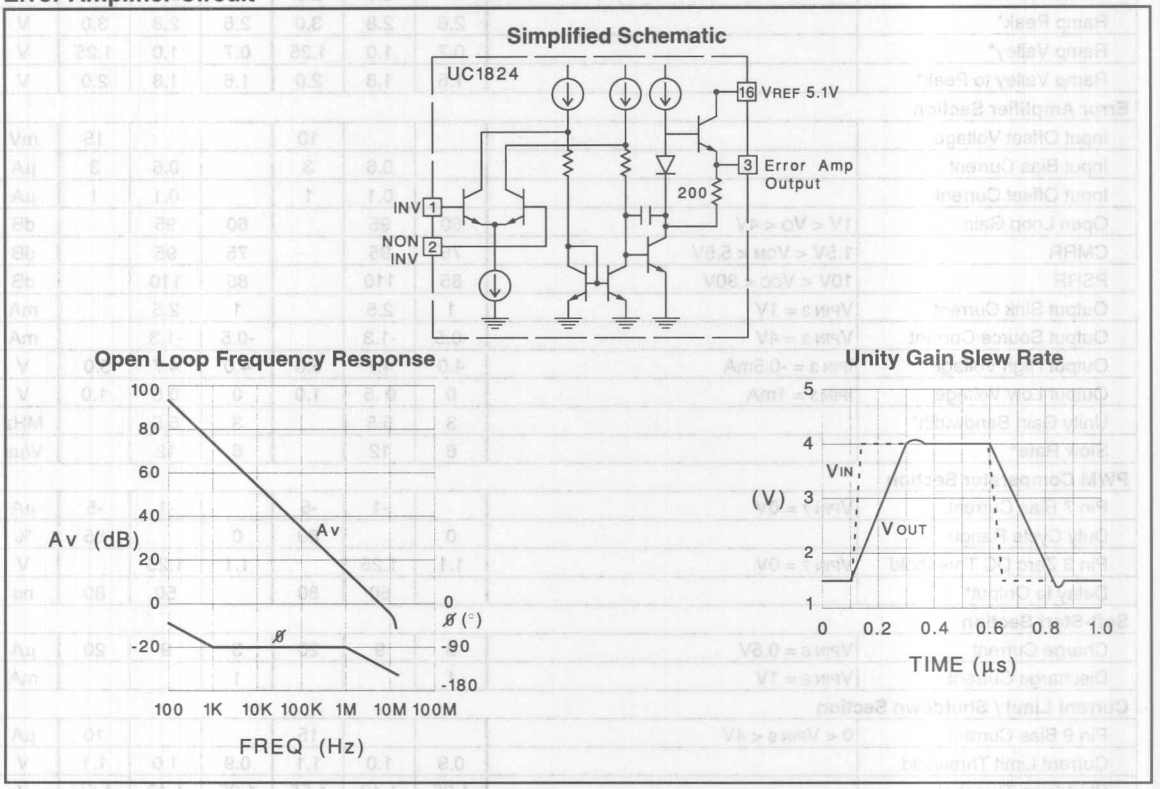
Unless otherwise stated,these specifications apply for , R_T = 3.65k, C_T = 1nF, V_{CC} = 15V, -55°C<T_A<125°C for the UC1824, –40°C<T_A<85°C for the UC2824, and 0°C<T_A<70°C for the UC3824, T_A=T_J.

PARAMETERS	TEST CONDITIONS	UC1824 UC2824			UC3824			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Oscillator Section (cont.)								
Clock Out High		3.9	4.5		3.9	4.5		V
Clock Out Low			2.3	2.9		2.3	2.9	V
Ramp Peak*		2.6	2.8	3.0	2.6	2.8	3.0	V
Ramp Valley*		0.7	1.0	1.25	0.7	1.0	1.25	V
Ramp Valley to Peak*		1.6	1.8	2.0	1.6	1.8	2.0	V
Error Amplifier Section								
Input Offset Voltage				10			15	mV
Input Bias Current			0.6	3		0.6	3	µA
Input Offset Current			0.1	1		0.1	1	µA
Open Loop Gain	1V < V_O < 4V	60	95		60	95		dB
CMRR	1.5V < V_{CM} < 5.5V	75	95		75	95		dB
PSRR	10V < V_{CC} < 30V	85	110		85	110		dB
Output Sink Current	$V_{PIN\ 3}$ = 1V	1	2.5		1	2.5		mA
Output Source Current	$V_{PIN\ 3}$ = 4V	-0.5	-1.3		-0.5	-1.3		mA
Output High Voltage	$I_{PIN\ 3}$ = -0.5mA	4.0	4.7	5.0	4.0	4.7	5.0	V
Output Low Voltage	$I_{PIN\ 3}$ = 1mA	0	0 .5	1.0	0	0.5	1.0	V
Unity Gain Bandwidth*		3	5.5		3	5.5		MHz
Slew Rate*		6	12		6	12		V/µs
PWM Comparator Section								
Pin 7 Bias Current	$V_{PIN\ 7}$ = 0V		-1	-5		-1	-5	µA
Duty Cycle Range		0		80	0		85	%
Pin 3 Zero DC Threshold	$V_{PIN\ 7}$ = 0V	1.1	1.25		1.1	1.25		V
Delay to Output*			50	80		50	80	ns
Soft-Start Section								
Charge Current	$V_{PIN\ 8}$ = 0.5V	3	9	20	3	9	20	µA
Discharge Current	$V_{PIN\ 8}$ = 1V	1			1			mA
Current Limit / Shutdown Section								
Pin 9 Bias Current	0 < $V_{PIN\ 9}$ < 4V			15			10	µA
Current Limit Threshold		0.9	1.0	1.1	0.9	1.0	1.1	V
Shutdown Threshold		1.25	1.40	1.55	1.25	1.40	1.55	V
Delay to Output			50	80		50	80	ns
Output Section								
Output Low Level	I_{OUT} = 20mA		0.25	0.40		0.25	0.40	V
	I_{OUT} = 200mA		1.2	2.2		1.2	2.2	V
Output High Level	I_{OUT} = -20mA	13.0	13.5		13.0	13.5		V
	I_{OUT} = -200mA	12.0	13.0		12.0	13.0		V
Collector Leakage	V_C = 30V		100	500		10	500	µA
Rise/Fall Time*	CL = 1nF		30	60		30	60	ns
Under-Voltage Lockout Section								
Start Threshold		8.8	9.2	9.6	8.8	9.2	9.6	V
UVLO Hysteresis		0.4	0.8	1.2	0.4	0.8	1.2	V
Supply Current Section								
Start Up Current	V_{CC} = 8V		1.1	2.5		1.1	2.5	mA
ICC	$V_{PIN\ 1}$, $V_{PIN\ 7}$, $V_{PIN\ 9}$ = 0V; $V_{PIN\ 2}$ = 1V		22	33		22	33	mA

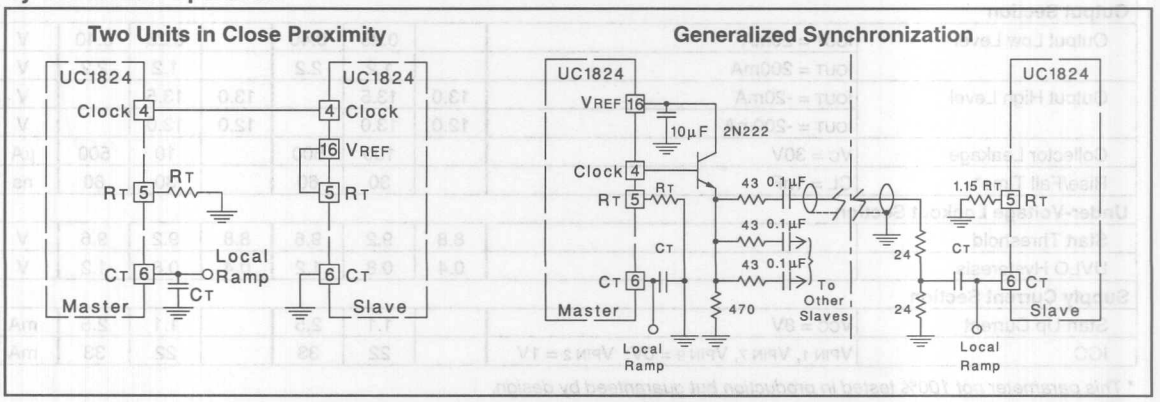
** This parameter not 100% tested in production but guaranteed by design.*

High speed circuits demand careful attention to layout and component placement. To assure proper performance of the UC1824 follow these rules: 1) Use a ground plane. 2) Damp or clamp parasitic inductive kick energy from the gate of driven MOSFETs. Do not allow the output pins to ring below ground. A series gate resistor or a shunt 1 Amp Schottky diode at the output pin will serve this purpose. 3) Bypass V_{CC}, V_C, and V_{REF}. Use 0.1µF monolithic ceramic capacitors with low equivalent series inductance. Allow less than 1 cm of total lead length for each capacitor between the bypassed pin and the ground plane. 4) Treat the timing capacitor, C_T, like a bypass capacitor.

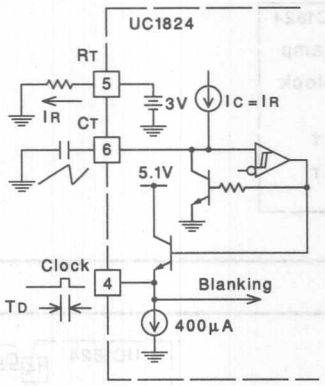
Error Amplifier Circuit



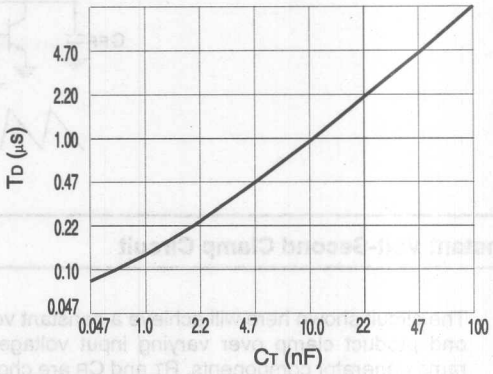
Synchronized Operation



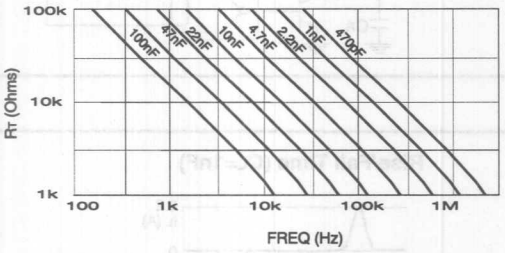
Oscillator Circuit



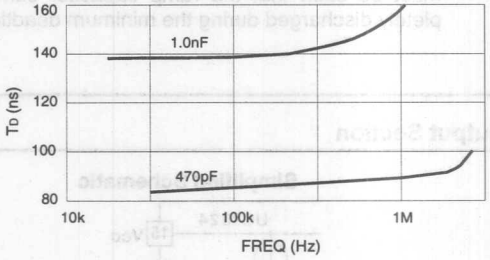
Primary Output Deadtime vs CT (3k ≤ RT ≤ 100k)



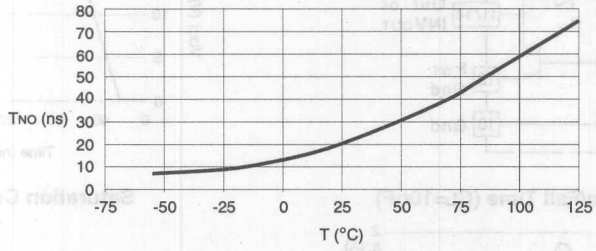
Timing Resistance vs Frequency



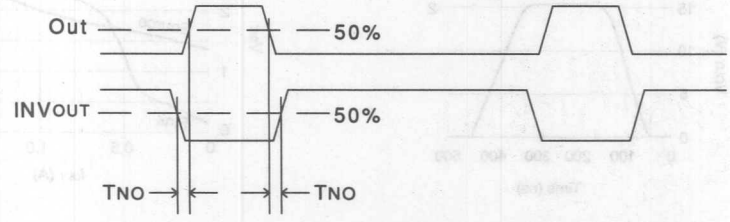
Primary Output Deadtime vs Frequency



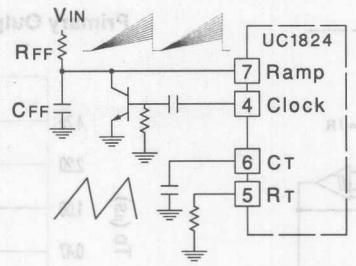
Typical Non-Overlap Time (TNO) Over Temperature



Non-Overlap Time (TNO)

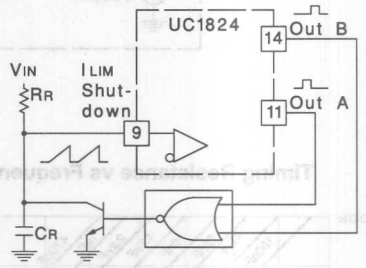


Forward Technique for Off-Line Voltage Mode Application



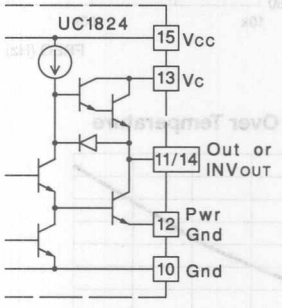
Constant Volt-Second Clamp Circuit

The circuit shown here will achieve a constant volt-second product clamp over varying input voltages. The ramp generator components, RT and CR are chosen so that the ramp at Pin 9 crosses the 1V threshold at the same time the desired maximum volt-second product is reached. The delay through the functional nor block must be such that the ramp capacitor can be completely discharged during the minimum deadtime.

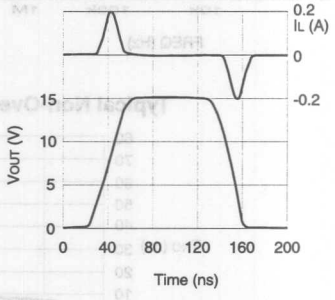


Output Section

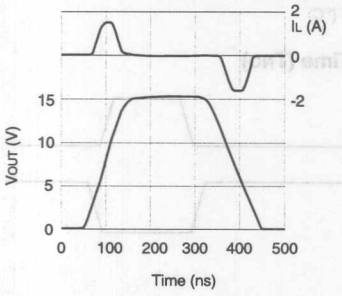
Simplified Schematic



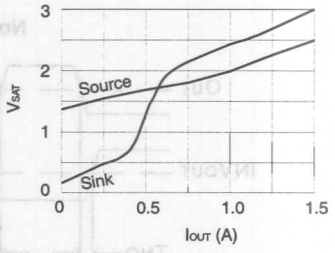
Rise/Fall Time (CL=1nF)



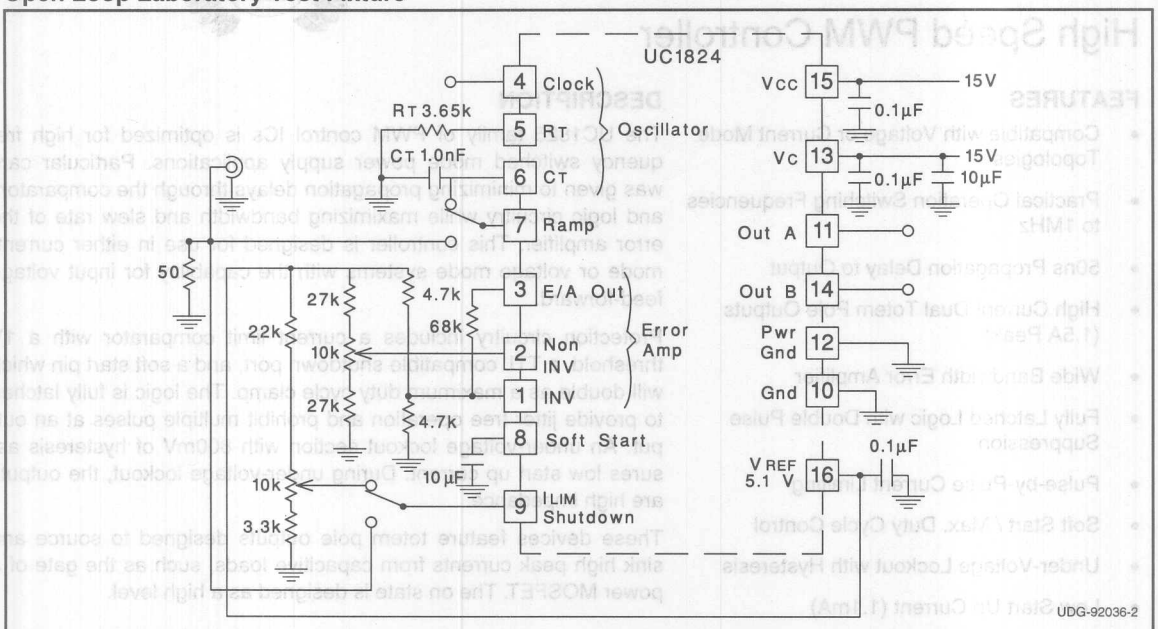
Rise/Fall Time (CL=10nF)



Saturation Curves



Open Loop Laboratory Test Fixture



This test fixture is useful for exercising many of the UC1824's functions and measuring their specifications.

As with any wideband circuit, careful grounding and bypass procedures should be followed. The use of a ground plane is highly recommended.

UNITRODE CORPORATION
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High Speed PWM Controller

FEATURES

- Compatible with Voltage or Current Mode Topologies
- Practical Operation Switching Frequencies to 1MHz
- 50ns Propagation Delay to Output
- High Current Dual Totem Pole Outputs (1.5A Peak)
- Wide Bandwidth Error Amplifier
- Fully Latched Logic with Double Pulse Suppression
- Pulse-by-Pulse Current Limiting
- Soft Start / Max. Duty Cycle Control
- Under-Voltage Lockout with Hysteresis
- Low Start Up Current (1.1mA)
- Trimmed Bandgap Reference (5.1V ±1%)

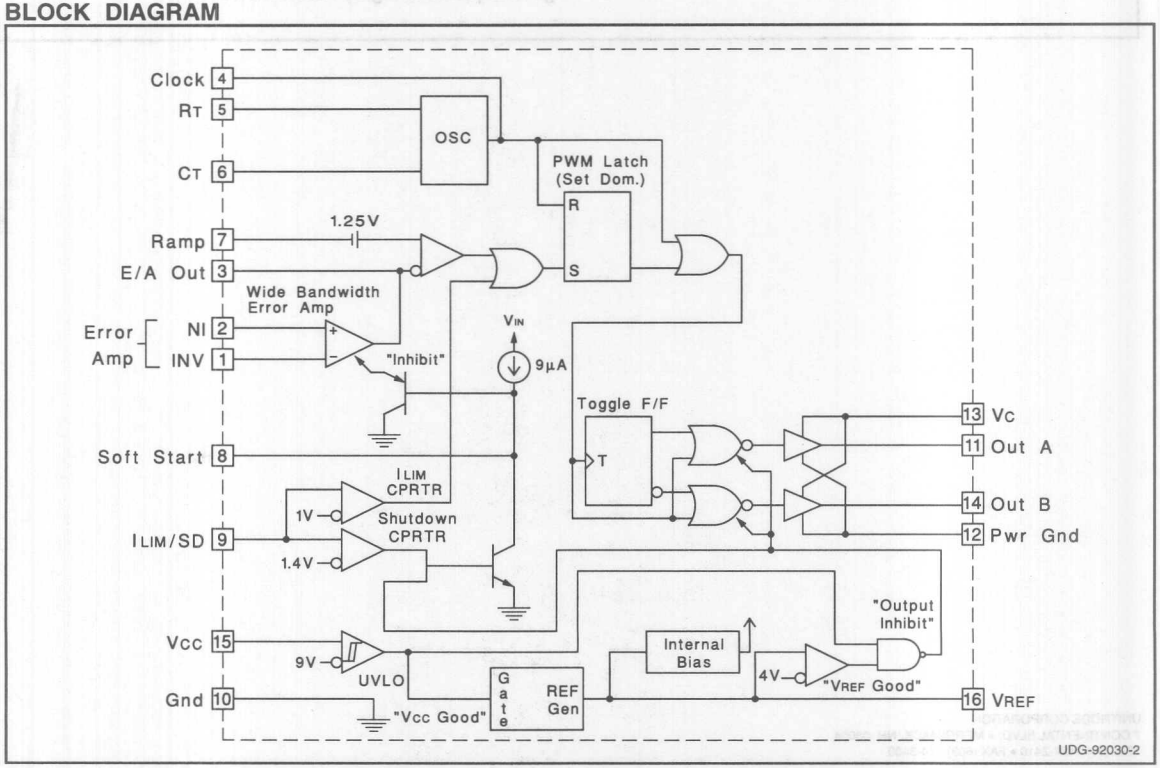
DESCRIPTION

The UC1825 family of PWM control ICs is optimized for high frequency switched mode power supply applications. Particular care was given to minimizing propagation delays through the comparators and logic circuitry while maximizing bandwidth and slew rate of the error amplifier. This controller is designed for use in either current-mode or voltage mode systems with the capability for input voltage feed-forward.

Protection circuitry includes a current limit comparator with a 1V threshold, a TTL compatible shutdown port, and a soft start pin which will double as a maximum duty cycle clamp. The logic is fully latched to provide jitter free operation and prohibit multiple pulses at an output. An under-voltage lockout section with 800mV of hysteresis assures low start up current. During under-voltage lockout, the outputs are high impedance.

These devices feature totem pole outputs designed to source and sink high peak currents from capacitive loads, such as the gate of a power MOSFET. The on state is designed as a high level.

BLOCK DIAGRAM



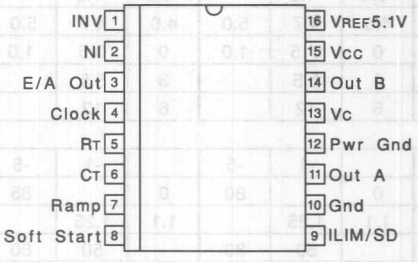
ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (Pins 13, 15) 30V
Output Current, Source or Sink (Pins 11, 14)
DC. 0.5A
Pulse (0.5µs) 2.0A
Analog Inputs
(Pins 1, 2, 7) . . . . . -0.3V to 7V
(Pin 8, 9) . . . . . -0.3V to 6V
Clock Output Current (Pin 4) . . . . . -5mA
Error Amplifier Output Current (Pin 3) 5mA
Soft Start Sink Current (Pin 8) 20mA
Oscillator Charging Current (Pin 5) . . . . . -5mA
Power Dissipation 1W
Storage Temperature Range . . . . . -65°C to +150°C
Lead Temperature (Soldering, 10 seconds) . . . . . 300°C

Note 1: All voltages are with respect to GND (Pin 10); all currents are positive into, negative out of part; pin numbers refer to DIL-16 package.

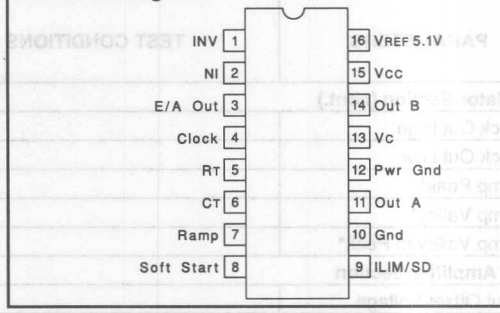
Note 3: Consult Unitrode Integrated Circuit Databook for thermal limitations and considerations of package.

SOIC-16 (Top View)
DW Package

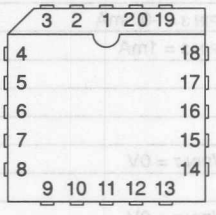


CONNECTION DIAGRAMS

DIL-16 (Top View)
J Or N Package



PLCC-20 & LCC-20
(Top View)
Q & L Packages



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
INV	2
NI	3
E/A Out	4
Clock	5
N/C	6
RT	7
CT	8
Ramp	9
Soft Start	10
N/C	11
ILIM/SD	12
Gnd	13
Out A	14
Pwr Gnd	15
N/C	16
Vc	17
Out B	18
Vcc	19
VREF 5.1V	20

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated,these specifications apply for , R_T = 3.65k, C_T = 1nF, Vcc = 15V, -55°C<T_A<125°C for the UC1825, –40°C<T_A<85°C for the UC2825, and 0°C<T_A<70°C for the UC3825, T_A=T_J.

PARAMETERS	TEST CONDITIONS	UC1825 UC2825			UC3825			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Reference Section								
Output Voltage	T_J = 25°C, Io = 1mA	5.05	5.10	5.15	5.00	5.10	5.20	V
Line Regulation	10V < Vcc < 30V		2	20		2	20	mV
Load Regulation	1mA < Io < 10mA		5	20		5	20	mV
Temperature Stability*	T_{MIN} < T_A < T_{MAX}		0.2	0.4		0.2	0.4	mV/°C
Total Output Variation*	Line, Load, Temperature	5.00		5.20	4.95		5.25	V
Output Noise Voltage*	10Hz < f < 10kHz		50			50		µV
Long Term Stability*	T_J = 125°C, 1000hrs.		5	25		5	25	mV
Short Circuit Current	V_{REF} = 0V	-15	-50	-100	-15	-50	-100	mA
Oscillator Section								
Initial Accuracy*	T_J = 25°C	360	400	440	360	400	440	kHz
Voltage Stability*	10V < Vcc < 30V		0.2	2		0.2	2	%
Temperature Stability*	T_{MIN} < T_A < T_{MAX}		5			5		%
Total Variation*	Line, Temperature	340		460	340		460	kHz

ELECTRICAL CHARACTERISTICS (cont.)

Unless otherwise stated,these specifications apply for , R_T = 3.65k, C_T = 1nF, V_{CC} = 15V, -55°C<T_A<125°C for the UC1825, –40°C<T_A<85°C for the UC2825, and 0°C<T_A<70°C for the UC3825, T_A=T_J.

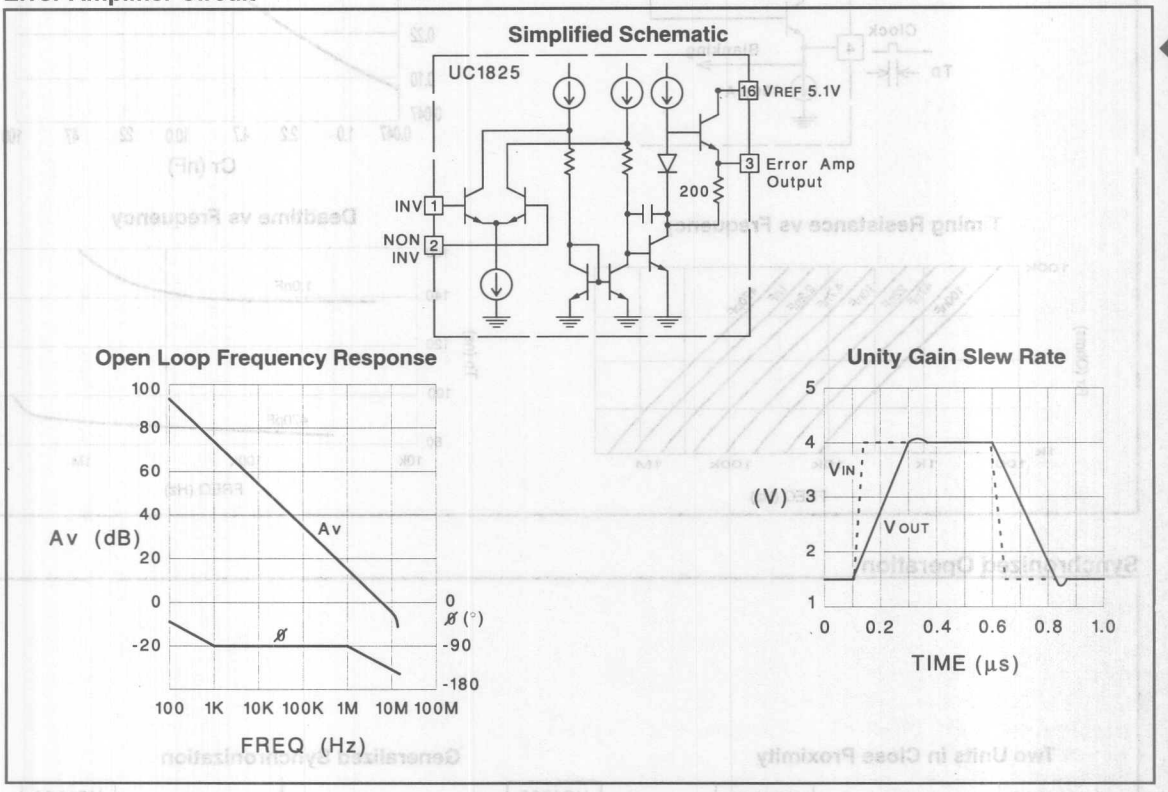
PARAMETERS	TEST CONDITIONS	UC1825 UC2825			UC3825			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Oscillator Section (cont.)								
Clock Out High		3.9	4.5		3.9	4.5		V
Clock Out Low			2.3	2.9		2.3	2.9	V
Ramp Peak*		2.6	2.8	3.0	2.6	2.8	3.0	V
Ramp Valley*		0.7	1.0	1.25	0.7	1.0	1.25	V
Ramp Valley to Peak*		1.6	1.8	2.0	1.6	1.8	2.0	V
Error Amplifier Section								
Input Offset Voltage				10			15	mV
Input Bias Current			0.6	3		0.6	3	µA
Input Offset Current			0.1	1		0.1	1	µA
Open Loop Gain	1V < V_O < 4V	60	95		60	95		dB
CMRR	1.5V < V_{CM} < 5.5V	75	95		75	95		dB
PSRR	10V < V_{CC} < 30V	85	110		85	110		dB
Output Sink Current	$V_{PIN\ 3}$ = 1V	1	2.5		1	2.5		mA
Output Source Current	$V_{PIN\ 3}$ = 4V	-0.5	-1.3		-0.5	-1.3		mA
Output High Voltage	$I_{PIN\ 3}$ = -0.5mA	4.0	4.7	5.0	4.0	4.7	5.0	V
Output Low Voltage	$I_{PIN\ 3}$ = 1mA	0	0 .5	1.0	0	0.5	1.0	V
Unity Gain Bandwidth*		3	5.5		3	5.5		MHz
Slew Rate*		6	12		6	12		V/µs
PWM Comparator Section								
Pin 7 Bias Current	$V_{PIN\ 7}$ = 0V		-1	-5		-1	-5	µA
Duty Cycle Range		0		80	0		85	%
Pin 3 Zero DC Threshold	$V_{PIN\ 7}$ = 0V	1.1	1.25		1.1	1.25		V
Delay to Output*			50	80		50	80	ns
Soft-Start Section								
Charge Current	$V_{PIN\ 8}$ = 0.5V	3	9	20	3	9	20	µA
Discharge Current	$V_{PIN\ 8}$ = 1V	1			1			mA
Current Limit / Shutdown Section								
Pin 9 Bias Current	0 < $V_{PIN\ 9}$ < 4V			15			10	µA
Current Limit Threshold		0.9	1.0	1.1	0.9	1.0	1.1	V
Shutdown Threshold		1.25	1.40	1.55	1.25	1.40	1.55	V
Delay to Output			50	80		50	80	ns
Output Section								
Output Low Level	I_{OUT} = 20mA		0.25	0.40		0.25	0.40	V
	I_{OUT} = 200mA		1.2	2.2		1.2	2.2	V
Output High Level	I_{OUT} = -20mA	13.0	13.5		13.0	13.5		V
	I_{OUT} = -200mA	12.0	13.0		12.0	13.0		V
Collector Leakage	V_C = 30V		100	500		10	500	µA
Rise/Fall Time*	CL = 1nF		30	60		30	60	ns
Under-Voltage Lockout Section								
Start Threshold		8.8	9.2	9.6	8.8	9.2	9.6	V
UVLO Hysteresis		0.4	0.8	1.2	0.4	0.8	1.2	V
Supply Current Section								
Start Up Current	V_{CC} = 8V		1.1	2.5		1.1	2.5	mA
ICC	$V_{PIN\ 1}$, $V_{PIN\ 7}$, $V_{PIN\ 9}$ = 0V; $V_{PIN\ 2}$ = 1V		22	33		22	33	mA

** This parameter not 100% tested in production but guaranteed by design.*

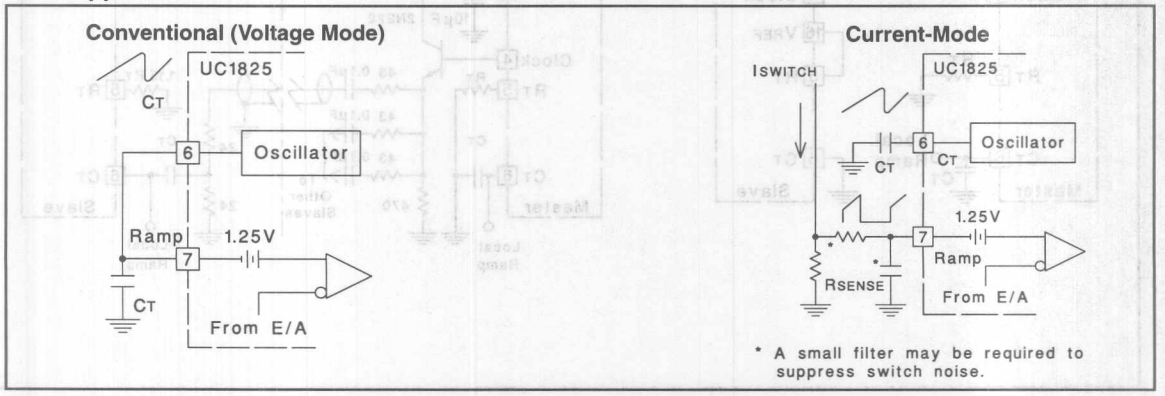
Printed Circuit Board Layout Considerations

High speed circuits demand careful attention to layout and component placement. To assure proper performance of the UC1825 follow these rules: 1) Use a ground plane. 2) Damp or clamp parasitic inductive kick energy from the gate of driven MOSFETs. Do not allow the output pins to ring below ground. A series gate resistor or a shunt 1 Amp Schottky diode at the output pin will serve this purpose. 3) Bypass V_{CC}, V_C, and V_{REF}. Use 0.1µF monolithic ceramic capacitors with low equivalent series inductance. Allow less than 1 cm of total lead length for each capacitor between the bypassed pin and the ground plane. 4) Treat the timing capacitor, C_T, like a bypass capacitor.

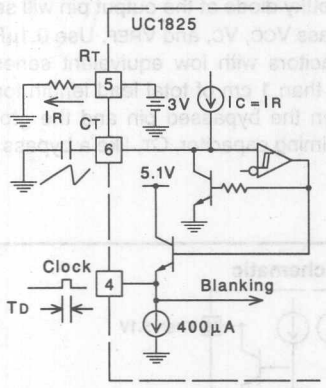
Error Amplifier Circuit

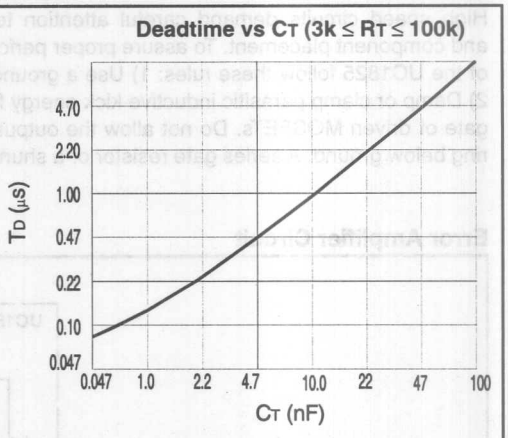


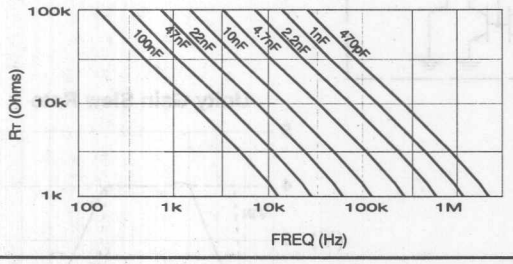
PWM Applications

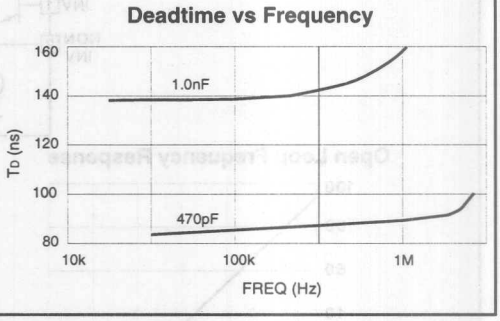


Oscillator Circuit



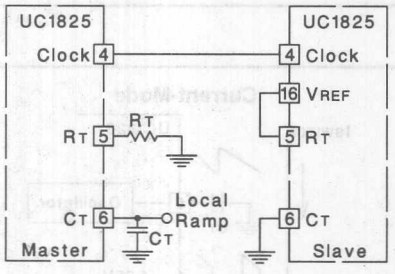




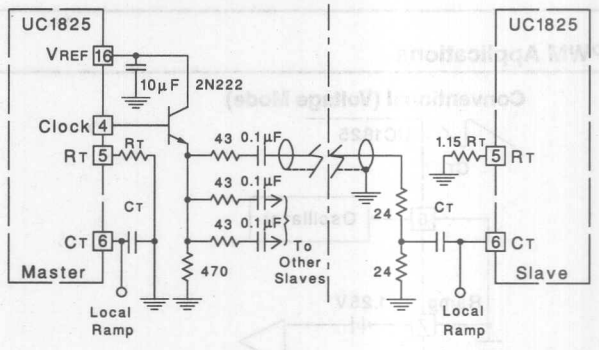


Synchronized Operation

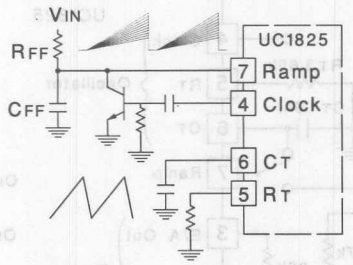
Two Units in Close Proximity



Generalized Synchronization

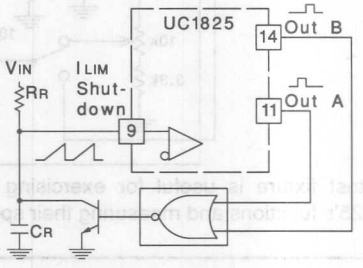


Forward Technique for Off-Line Voltage Mode Application



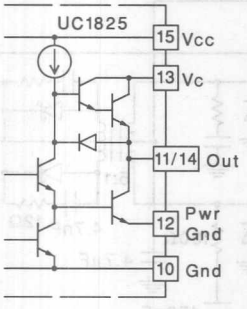
Constant Volt-Second Clamp Circuit

The circuit shown here will achieve a constant volt-second product clamp over varying input voltages. The ramp generator components, RT and CR are chosen so that the ramp at Pin 9 crosses the 1V threshold at the same time the desired maximum volt-second product is reached. The delay through the functional nor block must be such that the ramp capacitor can be completely discharged during the minimum deadtime.

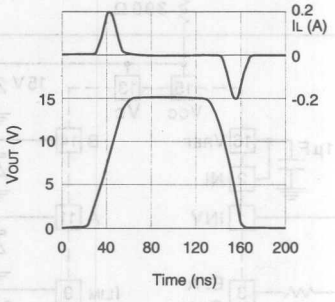


Output Section

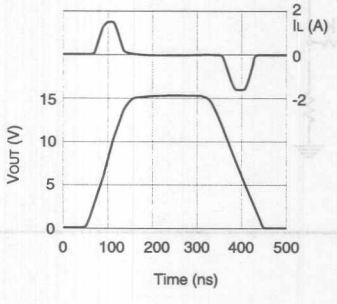
Simplified Schematic



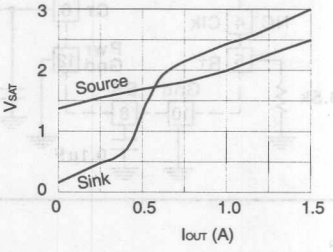
Rise/Fall Time (CL=1nF)



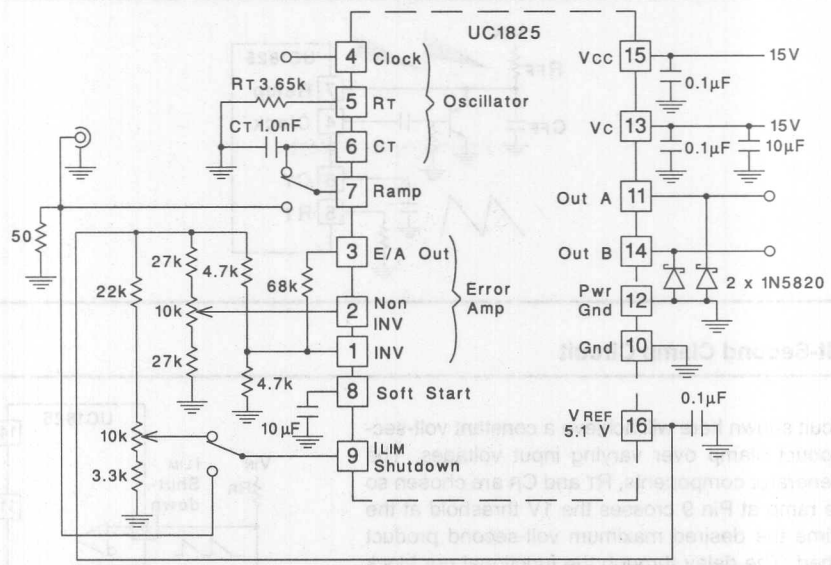
Rise/Fall Time (CL=10nF)



Saturation Curves



Open Loop Laboratory Test Fixture

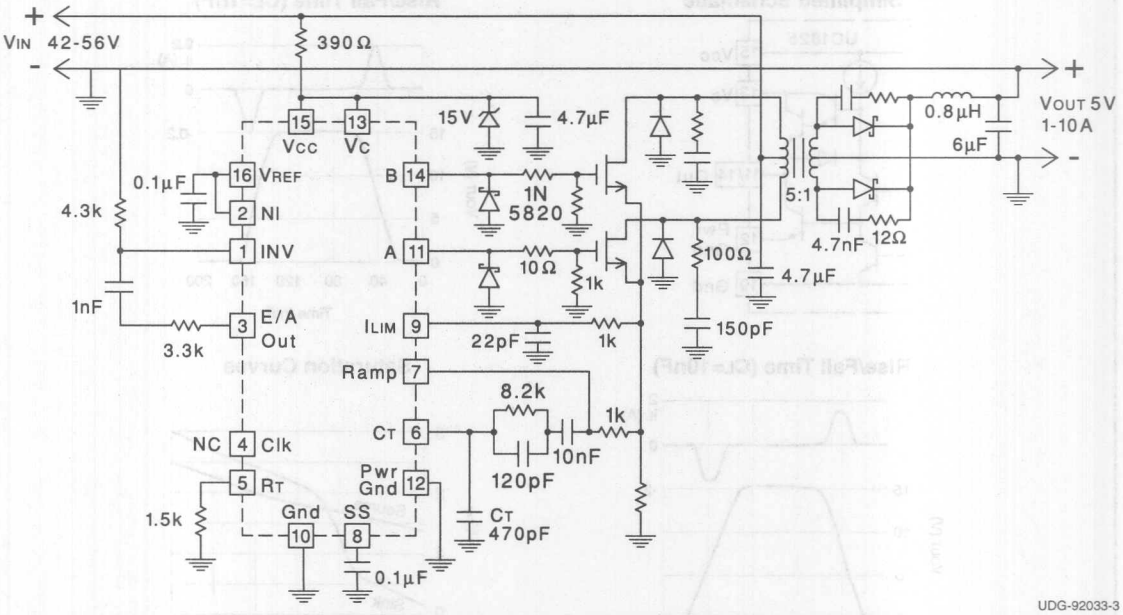


UDG-92032-2

This test fixture is useful for exercising many of the UC1825's functions and measuring their specifications.

As with any wideband circuit, careful grounding and bypass procedures should be followed. The use of a ground plane is highly recommended.

Design Example: 50W, 48V to 5V DC to DC Converter - 1.5MHz Clock Frequency



UDG-92033-3

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

Secondary Side Average Current Mode Controller

FEATURES

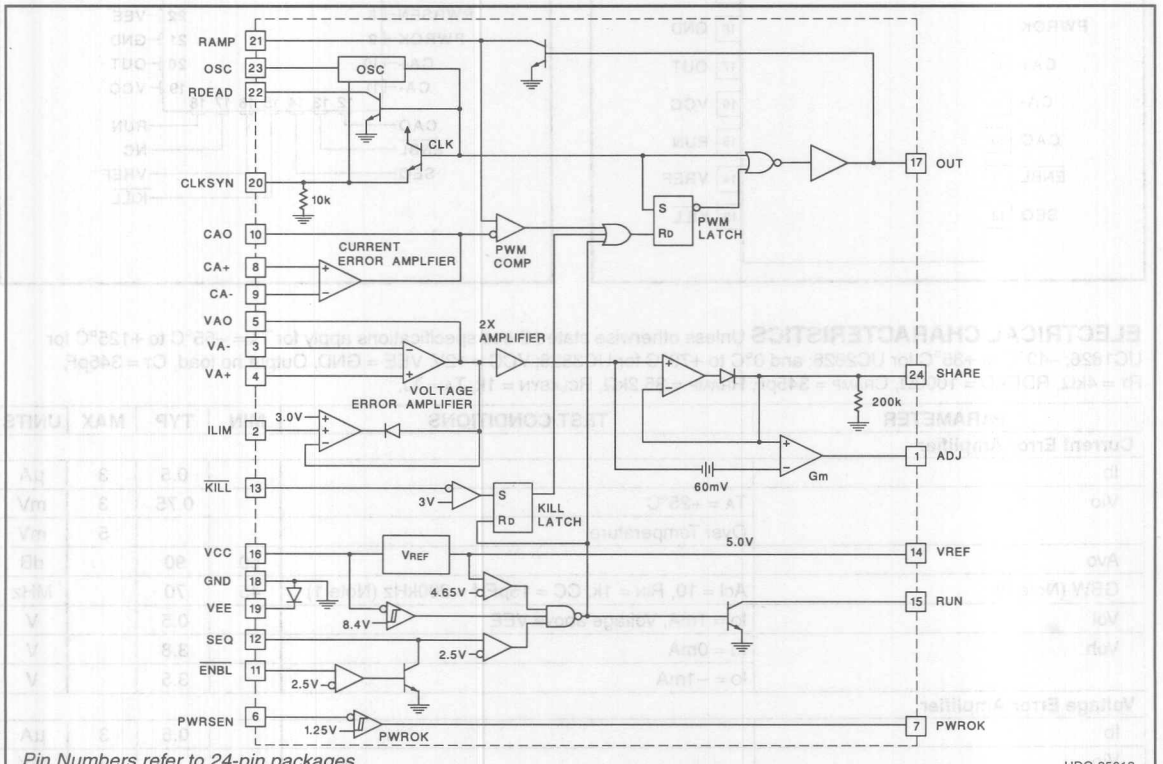
- Practical Secondary Side Control of Isolated Power Supplies
- 1MHz Operation
- Tailored Loop Bandwidth Provides Excellent Noise Immunity
- Voltage Feedforward Provides Superior Transient Response
- Accurate Programmable Maximum Duty Cycle
- Multiple Chips Can be Synchronized to Fastest Oscillator
- Wide Gain Bandwidth Product (70MHz, Acl>10) Current Error Amplifier
- Up to Ten Devices Can Easily Share a Common Load

DESCRIPTION

The UC1826 family of average current mode controllers accurately accomplishes secondary side average current mode control. The secondary side output voltage is regulated by sensing the output voltage and differentially sensing the AC switching current. The sensed output voltage drives a voltage error amplifier. The AC switching current, monitored by a current sense resistor, drives a high bandwidth, low offset current error amplifier. The output of the voltage error amplifier can be used to drive the current amplifier which filters the measured inductor current. Fast transient response is accomplished by utilizing voltage feedforward in generating the PWM ramp.

The UC1826 features load share, oscillator synchronization, undervoltage lockout, and programmable output control. Multiple chip operation can be achieved by connecting up to ten UC1826 chips in parallel. The SHARE bus and CLKSYN bus provide load sharing and synchronization to the fastest oscillator respectively. With its tailored bandwidth, the UC1826 provides excellent noise immunity and is an ideal controller to achieve high power, secondary side average current mode control.

BLOCK DIAGRAM



Pin Numbers refer to 24-pin packages.

UDG-95013

7/95

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (VCC) 20V
Output Current Source or Sink 0.3A
Analog Input Voltages . . . . . .–0.3V to 7V
ILIM, $\overline{KILL}$, SEQ, $\overline{ENBL}$, RUN, PWRSEN, PWROK . . . .–0.3V to 7V
CLKSYN Current Source 20mA
RUN Current Sink 20mA
SEQ Current Sink 20mA
RDEAD Current Sink 20mA
RAMP Current Sink 20mA
Share Bus Voltage (voltage with respect to GND) . . .0V to 6.2V
ADJ Voltage (voltage with respect to GND) . . . . . .0.9V to 6.3V
VEE (voltage with respect to GND) . . . . . .–1.5V
Storage Temperature . . . . . .–65°C to +150°C
Junction Temperature . . . . . .–65°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . .+300°C

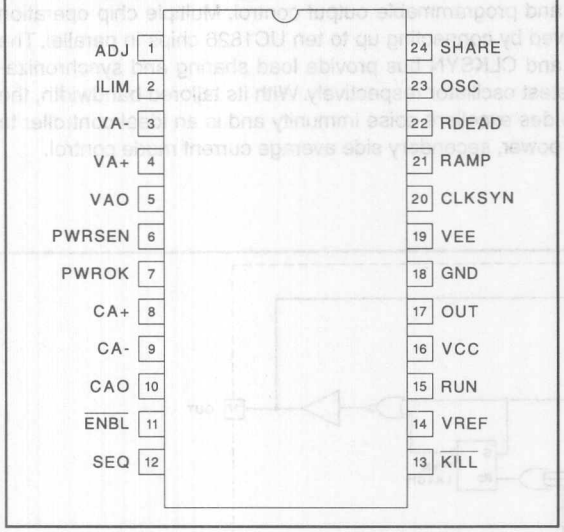
All voltages with respect to VEE except where noted; all currents are positive into, negative out of the specified terminal.
Consult Packaging Section of Databook for thermal limitations and considerations of packages.

RECOMMENDED OPERATING CONDITIONS

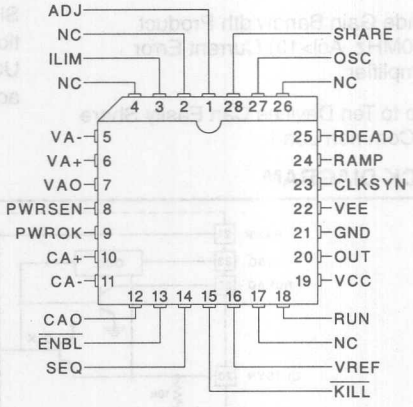
Input Voltage . . . . . .8V to 20V
Sink/Source Output Current 250mA
Timing Resistor R_T . . . . . .1k to 200k
Timing Capacitor C_T . . . . . .75pF to 2nF

CONNECTION DIAGRAMS

DIL-24, SOIC-24, TSSOP-24 (Top View)
J or N, DW, PW Packages



PLCC-28 (Top View)
Q Package



ELECTRICAL CHARACTERISTICS

Unless otherwise stated these specifications apply for T_A = –55°C to +125°C for UC1826; –40°C to +85°C for UC2826; and 0°C to +70°C for UC3826; VCC = 12V, VEE = GND, Output no load, C_T = 345pF, R_T = 4kΩ, RDEAD = 1000Ω, C_{RAMP} = 345pF, R_{RAMP} = 35.2kΩ, R_{CLKSYN} = 1k, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Current Error Amplifier					
Ib			0.5	3	µA
Vio	T_A = +25°C		0.75	3	mV
	Over Temperature			5	mV
Avo		60	90		dB
GBW (Note 2)	Acl = 10, R_{IN} = 1k, CC = 15pF, f = 200kHz (Note 1)	45	70		MHz
Vol	Io = 1mA, Voltage above VEE		0.5		V
Voh	Io = 0mA		3.8		V
	Io = –1mA		3.5		V
Voltage Error Amplifier					
Ib			0.5	3	µA
Vio				5	mV
Avo		60	90		dB

ELECTRICAL CHARACTERISTICS (cont.) Unless otherwise stated these specifications apply for T_A = –55°C to +125°C for UC1826; –40°C to +85°C for UC2826; and 0°C to +70°C for UC3826; VCC = 12V, VEE = GND, Output no load, C_T = 345pF, R_T = 4kΩ, RDEAD = 1000Ω, C_{RAMP} = 345pF, R_{RAMP} = 35.2kΩ, R_{CLKSYN} = 1k, T_A = T_J.

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
Voltage Error Amplifier (cont.)					
GBW (Note 2)	f = 200kHz		7		MHz
Vol	Io = 175mA, Volts above VEE			0.6	V
Voh	ILIM = 3V	2.85	3	3.15	V
Voh-ILIM	Tested ILIM = 0.5V, 1.0V, 2.0V	–100		100	mV
2X Amplifier and Share Amplifier					
V offset (b; y = mx + b)				20	mV
GAIN (m; y = mx + b)	Slope with A_{VOUT} = 1V and 2V	1.98		2.02	V
GBW (Note 2)			100		kHZ
R_{SHARE}	VCC = 0, V_{SHARE}/I_{SHARE}		200		kΩ
Total Offset	Negative supply is VEE, GND Open, VAO = GND	–75	0	75	mV
Vol	VAO = Voltage Amp Vol, Volts above VEE	0.2	0.45	0.6	V
Voh	Io = 0mA, ILIM = 3V, VAO = Voltage Amp Voh	5.7	6	6.3	V
	Io = –1mA, ILIM = 3V, VAO = Voltage Amp Voh	5.7	6	6.3	V
Adjust Amplifier					
Vio		40	60	80	mV
gm	Io = –2µA to 2µA, C_{ADJ} = 0.1µF		–0.1	–0.3	mS
Vol	I_{OUT} = 0	0.9	1	1.1	V
	I_{OUT} = 2µA	0.85	1	1.15	V
Voh	I_{OUT} = 0, V_{SHARE} = 6.5V	5.7	6	6.3	V
	I_{OUT} = –2µA, V_{SHARE} = 6.5V	5.7	6	6.3	V
Oscillator					
Frequency		450	500	550	kHz
Max Duty Cycle		72	76	80	%
OSC Ramp Amplitude		2	2.2	2.4	V
Ramp Saturation	Io = 10mA, OSC = 0V		0.44	0.8	V
Clock Driver/SYNC (CLKSYN)					
Vol			0.02	0.2	V
Voh			3.6		V
	R_{CLKSYN} = 200Ω		3.5		V
I_{SOURCE}			25		mA
R_{CLKSYN}	VCC = 0, V_{CLKSYN}/I_{CLKSYN}		10		k
V_{TH}			1.5		V
VREF Comparator					
Turn-on Threshold			4.65		V
Hysteresis			0.4		V
VCC Comparator					
Turn-on Threshold		7.9	8.4	8.9	V
Hysteresis			0.4		V
PWR Sense Comparator					
Voltage Threshold			1.25		V
Vol	Io = 1mA		0.3	0.4	V
Voh	Io = –100µA		4		V
KILL Comparator					
Voltage Threshold			3		V

ELECTRICAL CHARACTERISTICS (cont.) Unless otherwise stated these specifications apply for T_A = –55°C to +125°C for UC1826; –40°C to +85°C for UC2826; and 0°C to +70°C for UC3826; VCC = 12V, VEE = GND, Output no load, C_T = 345pF, R_T = 4kΩ, RDEAD = 1000Ω, C_{RAMP} = 345pF, R_{RAMP} = 35.2kΩ, R_{CLKSYN} = 1k, $T_A = T_J$.

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
Sequence Comparator					
Voltage Threshold			2.5		V
SEQ SAT	Io = 10mA		0.25		V
Enable Comparator					
Voltage Threshold			2.5		V
RUN SAT	Io = 10mA		0.2		V
Reference					
VREF	T_A = 25°C	4.95	5	5.05	V
	VCC = 15V	4.9		5.1	V
Line Regulation	10 < VCC < 20		3	15	mV
Load Regulation	0 < Io < 10mA		3	15	mV
Short Circuit I	VREF = 0V	30	60	90	mA
Output Stage					
Rise Time	C_L = 100pF		10	20	ns
Fall Time	C_L = 100pF		10	20	ns
Voh	VCC > 11V, Io = –10mA	8.0	8.4	8.8	V
	Io = –200mA	7.8			V
Vol	Io = 200mA			3.0	V
	Io = 10mA			0.5	V
Virtual Ground					
V_{GND} – VEE	VEE is externally supplied, GND is floating and used as Signal GND.	0.2	0.75		V
Icc					
Icc (run)			21	30	mA

Note 1: Guaranteed by design. Not 100% tested in production.
Note 2: Unless otherwise specified all voltages are with respect to GND. Currents are positive into, negative out of the specified terminal.

PIN DESCRIPTIONS

ADJ: The output of the transconductance (gm = –0.1mS) amplifier adjusts the control voltage to maintain equal current sharing. The chip sensing the highest output current will have its output clamped to 1V. A resistor divider between VREF and ADJ drives the control voltage (VA+) for the voltage amplifier. Each slave unit's ADJ voltage increases (to a maximum of 6V) its control voltage (VA+) until its load current is equal to the master. The 60mV input offset on the gm amplifier guarantees that the unit sensing the highest load current is chosen as the master. The 60mV offset is guaranteed by design to be greater than the inherent offset of the gm amplifier and the buffer amplifier. While the 60mV offset represents an error in current sharing, the gain of the current and 2X amplifiers reduces it to only 30mV. The total current sense gain is the current amplifier gain. This pin needs a 0.1µF capacitor to compensate the amplifier.

CA-, CA+: The inverting and non-inverting inputs to the current error amplifier. This amplifier needs a capacitor between CA- and CAO to set its dominant pole.

CAO: The output of the current error amplifier which is internally clamped to 4V. It is internally connected to the inverting input of the PWM comparator.

CLKSYN: The clock and synchronization pin for the oscillator. This is a bidirectional pin that can be used to synchronize several chips to the fastest oscillator. Its input synchronization threshold is 1.4V. The CLKSYN voltage is 3.6V when the oscillator capacitor C_T is being discharged, otherwise it is 0V.

PIN DESCRIPTIONS (cont.)

$\overline{\text{ENBL}}$: The active low input with a 2.5V threshold enables the output to switch. SEQ and RUN are driven low when $\overline{\text{ENBL}}$ is above its 2.5V threshold.

GND: The signal ground used for the voltage sense amplifier, current error amplifier, current error amplifier, voltage reference, 2X amplifier, and share amplifier. The output sink transistor is wired directly to this pin.

$\overline{\text{KILL}}$: The active low input with a 3.0V threshold stops the output from switching. Once this function is activated RUN must be cycled low by driving $\overline{\text{KILL}}$ above 3.0V and either resetting the power to the chip (VCC) or resetting the $\overline{\text{ENBL}}$ signal.

ILIM: A voltage on this pin programs the voltage error amplifier's Voh clamp. The voltage error amplifier output represents the average output current. The Voh clamp consequently limits the output current. If ILIM is tied to VREF, it defaults to 3.0V. A voltage less than 3.0V connected to ILIM clamps the voltage error amplifier at this voltage and consequently limits the maximum output current.

OSC: The oscillator ramp (not to be confused with PWM ramp) pin has a capacitor C_T to ground and two resistors in series R_T and R_{DEAD} to VREF. The total resistance of R_T and R_{DEAD} divided by VREF – V_{OSC} sets exponential charge current. The oscillator charges from 1.2V to 3.4V until the output transitions low. At this time an open collector transistor is turned on and discharges the C_T capacitor through RDEAD.

The charge time is approximately $T_{CHARGE} = 2(R_T + R_{DEAD}) \bullet C_T$ when the R_{DEAD} resistor is used.

The dead time is approximately $T_{DISCHARGE} = 2 \bullet R_{DEAD} \bullet C_T$.

$$(1)\quad \text{Frequency} \approx \frac{1}{T_{CHARGE} + T_{DISCHARGE}}$$

$$(2)\quad \text{Maximum Duty Cycle} \approx \frac{T_{CHARGE}}{T_{CHARGE} + T_{DISCHARGE}}$$

The C_T capacitance should be increased by approximately 40pF to account for parasitic capacitance.

OUT: The output of the PWM driver. It has an upper clamp of 8.5V. The peak current sink and source are 250mA. All UVLO, SEQ, $\overline{\text{ENBL}}$, and $\overline{\text{KILL}}$ logic either enable or disable the output driver.

PWRSEN: This pin is the input to the PWROK comparator.

PWROK: The output pin from the PWROK comparator. It has a 300µA current source output when driven high.

RAMP: An open collector that can sink 20mA to discharge the oscillator capacitor. An RC is tied between VCC and GND to accomplish feedforward. The PWM output drives this pin. When the output is high, the transistor is off enabling the charging of the RAMP capacitor. When the output transitions low, the transistor is turned on discharging the RAMP capacitor. The voltage at RAMP rises from 0.2V to near 4V at maximum duty cycle. Although this is an exponential ramp at high VCC voltage the ramp appears linear.

RDEAD: The pin that programs the maximum duty cycle by connecting a resistor between it and OSC. The maximum duty cycle is decreased by increasing this resistor value which increases the discharge time. The dead time, the time when the output is low, is $2 \bullet R_{DEAD} \bullet C_T$. The C_T capacitance should be increased by approximately 40pF to account for parasitic capacitance.

RUN: This is an open collector logic output that signifies when the chip is operational. RUN is pulled high to VREF through an external resistor when VCC is greater than 8.4V, VREF is greater than 4.65V, SEQ is greater than 2.5V, and $\overline{\text{KILL}}$ lower than 3.0V. RUN connected to the VA+ pin and to a capacitor to ground adds an RC rise time on the VA+ pin initiating a soft start.

SEQ: The sequence pin allows the sequencing of startup for multiple units. A resistor between VREF and SEQ and a capacitor between SEQ and GND create a unique RC rise time for each unit which sequences the output startup.

SHARE: The nearly DC voltage representing the average output current. This pin is wired directly to all SHARE pins and is the load share bus.

VA-, VA+: The inverting and non-inverting inputs to the voltage error amplifier.

VAO: The output of the voltage error amplifier. Its Voh is clamped with the ILIM pin.

VCC: The input voltage to the chip. The chip is operational between 8.4V and 20V.

VEE: The negative supply voltage to the chip which powers the lower voltage rail for all amplifiers. The chip is operational if VEE is connected to GND or if GND is floating. When voltage is applied externally to VEE, GND becomes a virtual ground because of an internal diode between VEE and GND. The GND current flows through the forward biased diode and out VEE. GND is always the signal ground from which the voltage reference and all amplifier inputs are referenced.

VREF: The reference voltage equal to 5.0V.

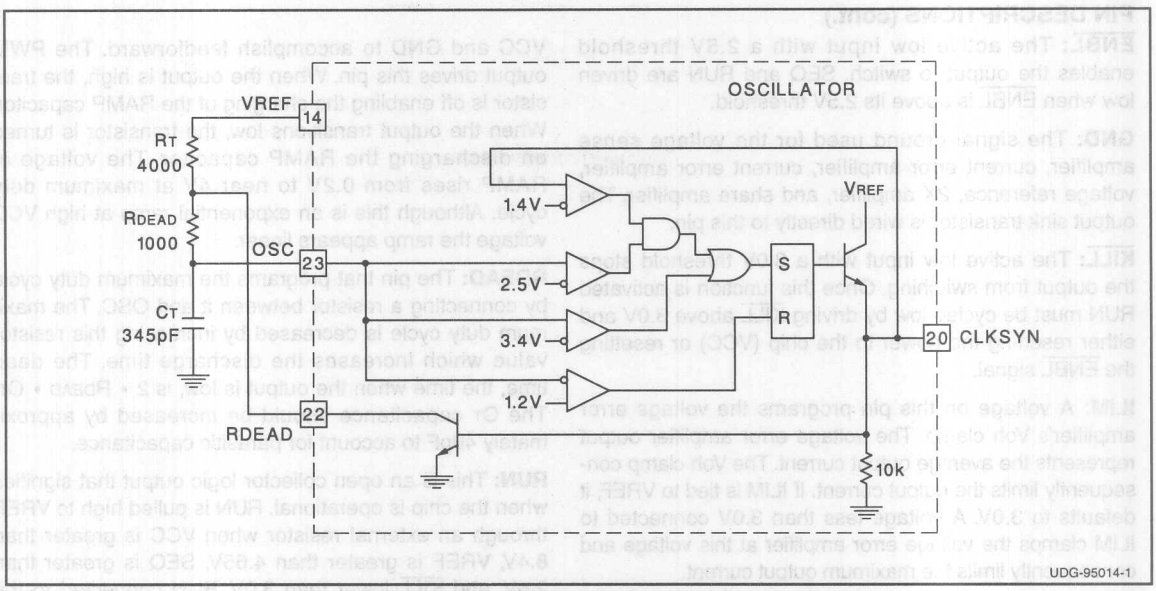


Figure 1. Oscillator Block with External Connections

CIRCUIT DESCRIPTION:

PWM Oscillator: The chip has two pins that set RC time constants. The resistor and capacitor tied to RAMP create the ramp used as the input to the PWM comparator. When the output pin OUT is high, RAMP charges until it passes the PWM comparator threshold. The output is then driven low and RAMP is discharged. The resistors and capacitor on the OSC pin are used to set the PWM operating frequency and its maximum duty cycle.

The oscillator block diagram with external wiring is shown in Figure 1. OSC has a capacitor (C_T) to ground and two resistors in series (R_T and R_{DEAD}) to VREF. The total resistance of R_T and R_{DEAD} divided by VREF – V_{OSC} sets the exponential charge current. The oscillator charges from 1.2V to a 3.4V threshold with an RC time delay of 2 • C_T • (R_{DEAD} + R_T). After exceeding this threshold, the RS flip-flop is set driving CLKSYN high and RDEAD low which discharges C_T. At this time and open collector transistor is turned on and discharges C_T capacitor through RDEAD with a RC time delay of 2 • C_T • R_{DEAD}. The oscillator and ramp waveforms are shown in Figure 2. Equations to attain frequency and maximum duty cycle are listed under the OSC pin description.

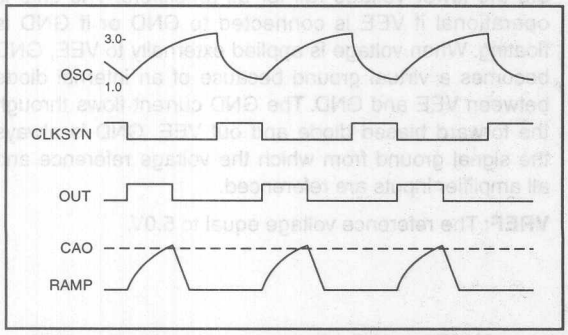


Figure 2. Oscillator and PWM Output Waveform

As shown in Figure 3, several oscillators are synchronized to the highest free running frequency by connecting 100pF capacitors in series with each CLKSYN pin and connecting the other side of the capacitors together forming the CLKSYN bus. The CLKSYN bus is then pulled down to ground with a resistance of approximately 10k. Referring to Figure 1, the synchronization threshold is 1.4V. The oscillator blanks any synchronization pulse that occurs when OSC is below 2.5V. This allows units, once they discharge below 2.5V, to continue through the current discharge and subsequent charge cycles whether or not other units on the CLKSYN bus are still synchronizing. This requires the frequency of all free running oscillators to be within 40% of each other to guarantee synchronization.

Grounds, Voltage Sensing and Current Sensing: The voltage is sensed directly at the load. Proper load sharing requires the same sensed voltage for each power supply connected in parallel. Referring to Figure 4, the

CIRCUIT BLOCK DESCRIPTION (cont.)

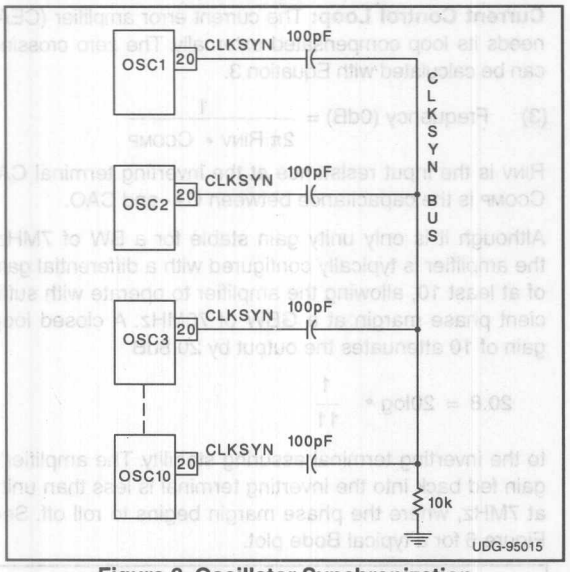


Figure 3. Oscillator Synchronization Connection Diagram

positive sense voltage (VSP) connects to the voltage error amplifier inverting terminal (VA-), the return lead for the on-chip reference is used as the negative sense (VSM). The current is sensed across the shunt resistor, Rs. The voltage across the shunt resistor is level shifted up so that the maximum voltage across Rs corresponds to the voltage error amplifier Voh.

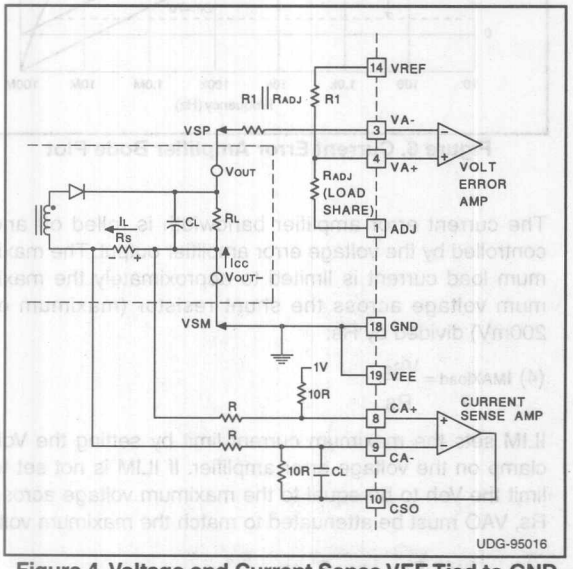


Figure 4. Voltage and Current Sense VEE Tied to GND

Figure 4 shows one recommended voltage and current sensing scheme when VEE is connected to GND. The signal ground is the negative sense point for the output voltage and the positive sense point for the output current. VEE is the negative supply for the current sense amplifier. When it is separated from GND, it extends the current sense amplifier's common mode input voltage range to include VEE which is approximately –0.7V below ground. The resistor R_{ADJ} is used for load sharing. The unit which is the master will force V_{ADJ} to 1.0V. Therefore, the regulated voltage being sensed is actually

$$V_{SP} - V_{SM} = (V_{REF} - V_{ADJ}) \bullet \left(\frac{R_{ADJ}}{R1 + R_{ADJ}}\right) + V_{ADJ}$$

$V_{SM} = 0V$, $V_{ADJ} = 1V$ (master), $V_{REF} = 5V$

$$V_{SP} = 4 \bullet \left(\frac{R_{ADJ}}{R1 + R_{ADJ}}\right) + 1V$$

The voltage at ADJ on the slave chips will increase forcing their load currents to increase to match the master.

The AC frequency response of the voltage error amplifier is shown in Figure 5.

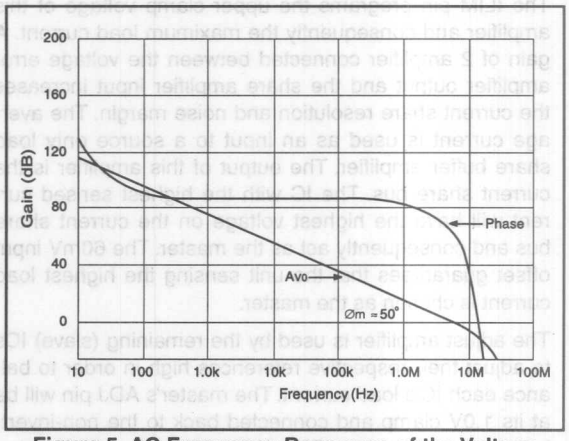


Figure 5. AC Frequency Response of the Voltage Error Amplifier

Startup and Shutdown: Isolated power up can be accomplished using the UCC1889. Application Note U-149 is available for additional information.

The UC1826 offers several features that enhance startup and shutdown. Soft start is accomplished by connecting RUN to VA+ and a capacitor to ground. The resulting RC rise time on the VA+ pin initiates a soft start. It can also be accomplished by connecting RUN to ILIM. When RUN is low it will command zero load current, guaranteeing a soft start. The undervoltage lockout (UVLO) is a logical AND of $\overline{ENBL}$ < 2.5V, SEQ > 2.5V, VCC > 8.4V and

CIRCUIT BLOCK DESCRIPTION (cont.)

VREF > 4.65V. The block diagram shows that the thresholds are set by comparators. By placing an RC divider on the SEQ pin, the enabling of multiple chips can be sequenced with different RC time constants. Similarly, different RC time constants on the $\overline{ENBL}$ pins can sequence shutdown. The UVLO keeps the output from switching; however the internal reference starts up with VCC less than 8.4V. The $\overline{KILL}$ input shuts down the switching of the chip. This can be used in conjunction with an overvoltage comparator for overvoltage protection. In order to restart the chip after $\overline{KILL}$ has been initiated, the chip must be powered down and then back up. A pulse on the $\overline{ENBL}$ pin also accomplishes this without actually removing voltage to the VCC pin.

Load Sharing: Load sharing is accomplished similarly to the UC1907 except it has the added constraint of using the sensed current for average current mode control. The sensed current for the UC1826 has an AC component that is amplified and then averaged. The voltage error amplifier represents this average current. The voltage error amplifier output is the current command signal and its voltage represents the average output load current. The ILIM pin programs the upper clamp voltage of this amplifier and consequently the maximum load current. A gain of 2 amplifier connected between the voltage error amplifier output and the share amplifier input increases the current share resolution and noise margin. The average current is used as an input to a source only load share buffer amplifier. The output of this amplifier is the current share bus. The IC with the highest sensed current will have the highest voltage on the current share bus and consequently act as the master. The 60mV input offset guarantees that the unit sensing the highest load current is chosen as the master.

The adjust amplifier is used by the remaining (slave) ICs to adjust their respective references high in order to balance each IC's load current. The master's ADJ pin will be at its 1.0V clamp and connected back to the non-inverting voltage error amplifier input through a high value resistor. This requires the user to initially calculate the control voltage with the ADJ pin at 1.0V.

VREF can be adjusted 150mV to 300mV which compensates for 5% unit to unit reference mismatch and external resistor mismatch. R_{ADJ} will typically be 10 to 30 times larger than R1. This also attenuates the overall variation of the ADJ clamp of 1V ±100mV by a factor of 10 to 30, contributing only a 3mV to 10mV additional delta to VREF. Refer to the UC3907 Application Note U-130 for further information on parallel power supply load sharing.

Current Control Loop: The current error amplifier (CEA) needs its loop compensated externally. The zero crossing can be calculated with Equation 3.

$$(3)\quad \text{Frequency (0dB)} = \frac{1}{2\pi\, R_{INV} \bullet C_{COMP}}$$

R_{INV} is the input resistance at the inverting terminal CA-
C_{COMP} is the capacitance between CA- and CAO.

Although it is only unity gain stable for a BW of 7MHz, the amplifier is typically configured with a differential gain of at least 10, allowing the amplifier to operate with sufficient phase margin at a GBW of 70MHz. A closed loop gain of 10 attenuates the output by 20.8dB

$$20.8 = 20\log \bullet \frac{1}{11}$$

to the inverting terminal assuring stability. The amplifier's gain fed back into the inverting terminal is less than unity at 7MHz, where the phase margin begins to roll off. See Figure 6 for a typical Bode plot.

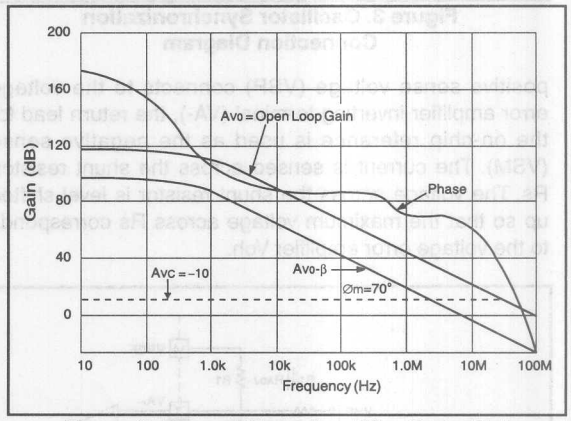


Figure 6. Current Error Amplifier Bode Plot

The current error amplifier bandwidth is rolled off and controlled by the voltage error amplifier output. The maximum load current is limited to approximately the maximum voltage across the shunt resistor (maximum of 200mV) divided by Rs:

$$(4)\quad I_{MAXload} = \frac{V_{Rs}}{Rs}$$

ILIM sets the maximum current limit by setting the Voh clamp on the voltage error amplifier. If ILIM is not set to limit the Voh to be equal to the maximum voltage across Rs, VAO must be attenuated to match the maximum volt-

age V_{RS} across the shunt resistor. By attenuating the maximum voltage at VAO to be equal to V_{RS}, the current control loop keeps the load from exceeding its current limit. If the ILIM pin is connected to VREF, the Voh is set at 3.0V. The maximum current limit clamp can be reduced by reducing the voltage on ILIM to less than 3.0V as described in the ILIM pin description.

Design Example: Figure 7 is an open loop test that lets the user test the circuit blocks discussed without having to build an entire control loop. The pulse width can be varied by either the V_{ADJ} or the V_{ISENSE} inputs. Figure 8 shows an isolated power supply using the UC1826 secondary side average current mode controller.

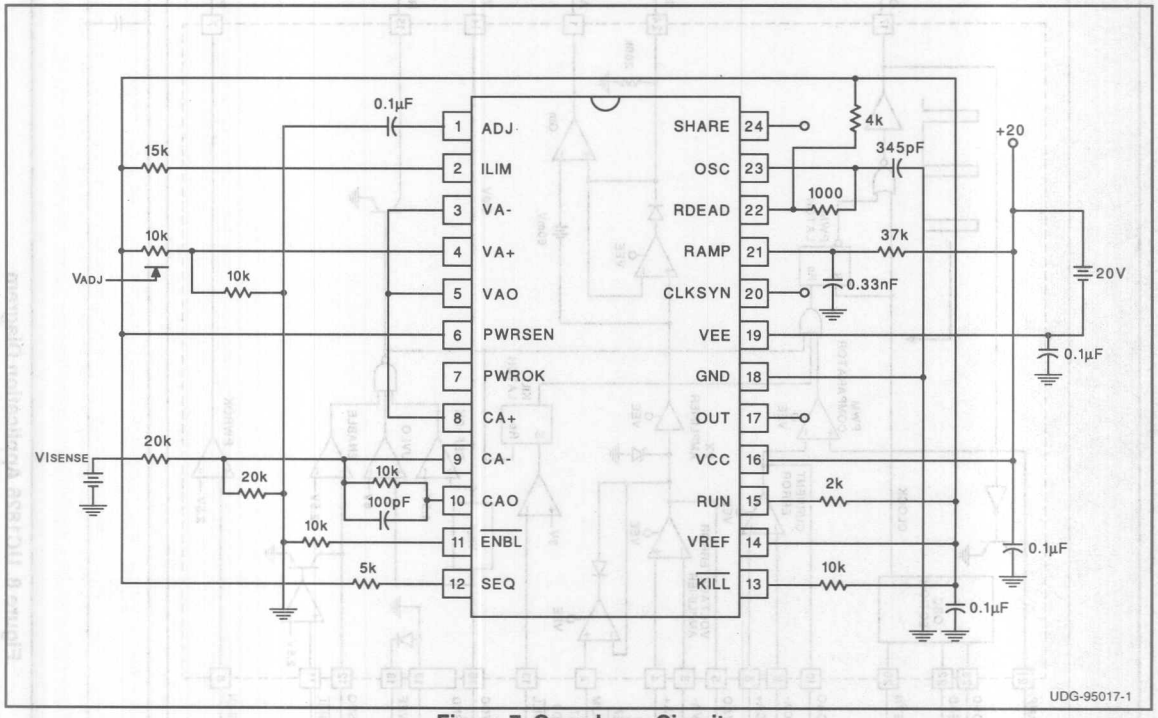


Figure 7. Open Loop Circuit

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
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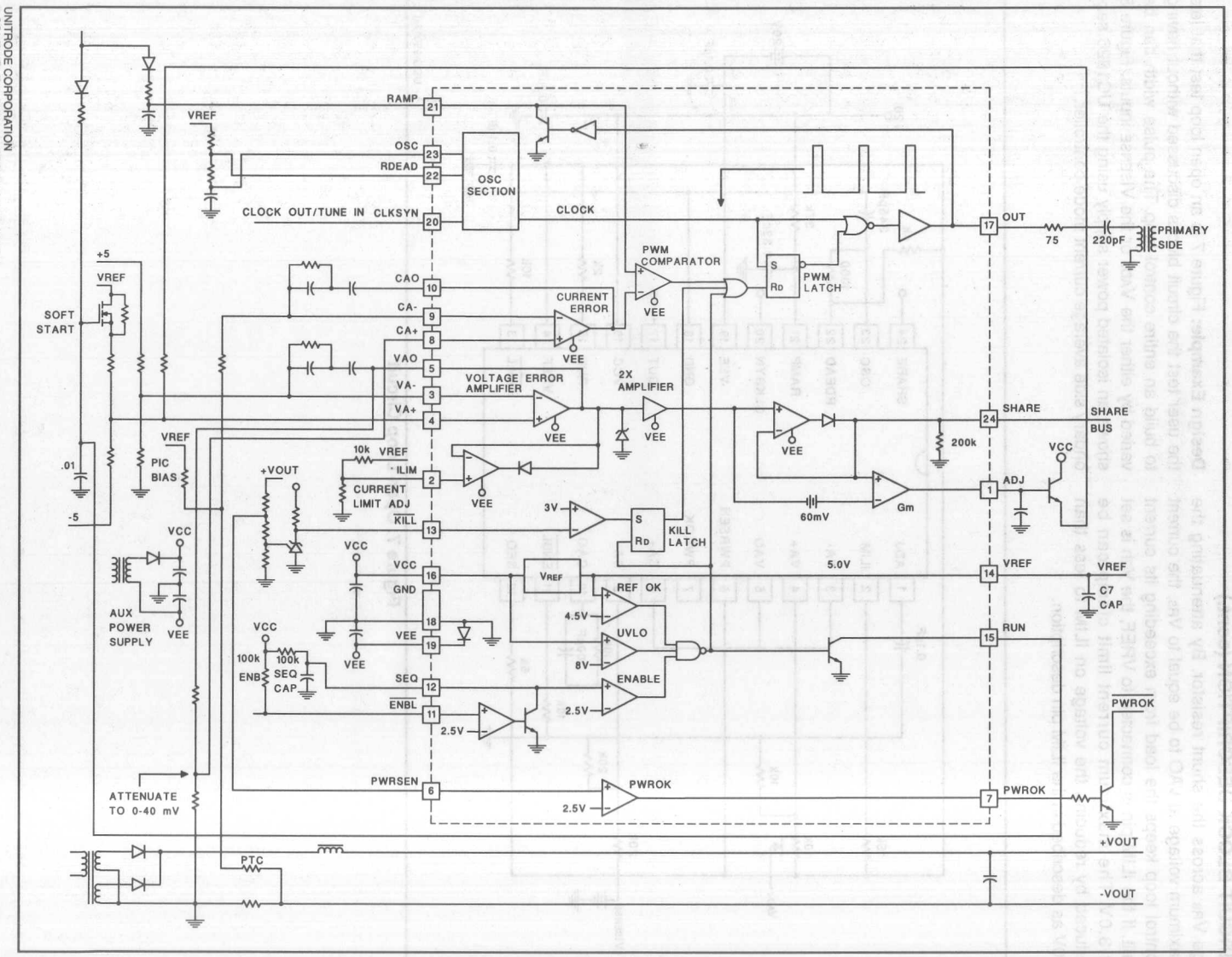


Figure 8. UC1826 Application Diagram

Buck Current/Voltage Fed Push-Pull PWM Controllers

PRELIMINARY

FEATURES

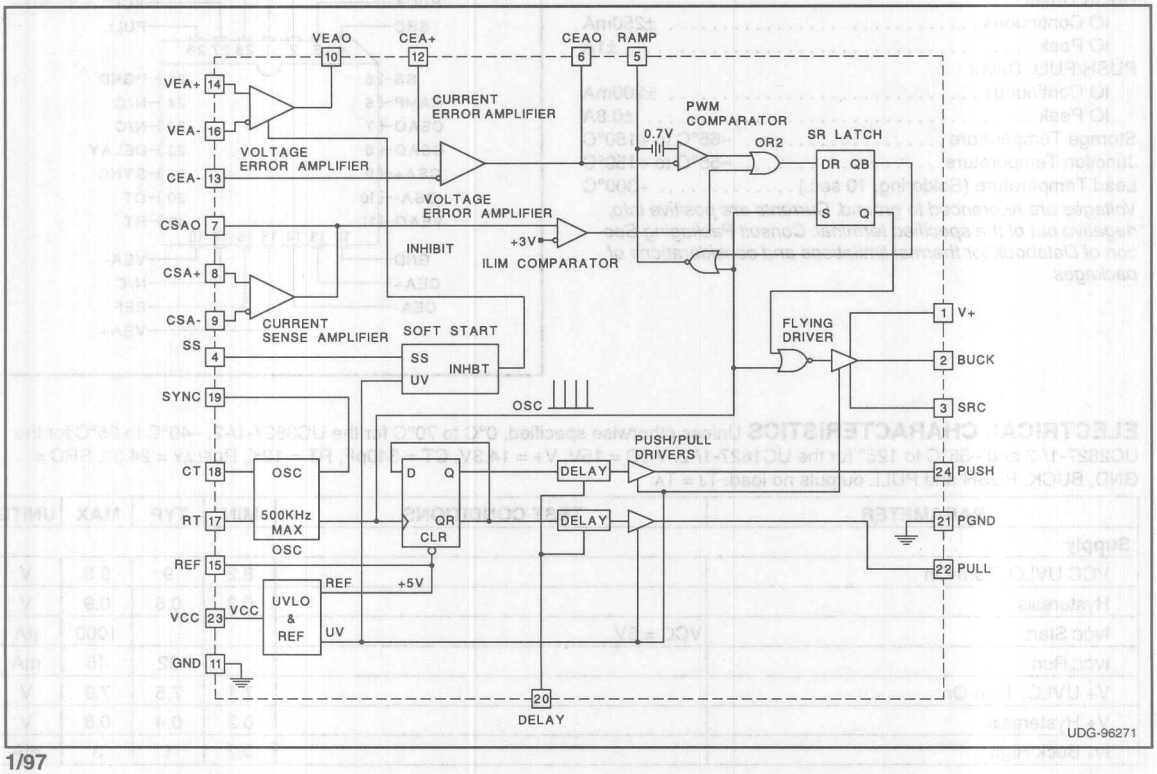
- Ideal for Multiple Output and/or High Voltage Output Voltage Converters
- Up to 500kHz Operation
- High Voltage, High Current Floating Driver for Buck Converter Stage
- UC3827-1 Current Fed Controller has Push-Pull Drivers with Overlapping Conduction Periods
- UC3827-2 Voltage Fed Controller has Push-Pull Drivers with Non-overlapping Conduction Periods
- Average Current Mode, Peak Current Mode or Voltage Mode with Input Voltage Feedforward Control for Buck Power Stage
- Wide Bandwidth, Low Offset, Differential Current Sense Amplifier
- Precise Short Circuit Current Control

DESCRIPTION

The UC3827 family of controller ICs provides an integrated control solution for cascaded buck and push-pull converters. These converters are known as current fed or voltage fed push-pull converters and are ideally suited for multiple output and/or high voltage output applications. In both current fed and voltage fed modes, the push-pull switches are driven at 50% nominal duty cycles and at one half the switching frequency of the buck stage. In the current fed mode, the two switches are driven with a guaranteed overlap period to prevent ringing and voltage stress on the devices. In the voltage fed mode, the two switches are driven with a guaranteed gap time between the switches to prevent shorting the transformer across the energy storage capacitor and to prohibit excessive currents flowing through the devices.

The converter's output voltage is regulated by pulse width modulation of the buck switch. The UC3827 contains complete protection and PWM control functions for the buck converter. Easy control of the floating switch is accomplished by the floating drive circuitry. The gate drive waveform is level shifted to support an input voltage up to 72Vdc.

BLOCK DIAGRAM



1/97

DESCRIPTION (cont.)

The UC3827 can be set up in traditional voltage mode control using input voltage feedforward technique or in current mode control. Using current mode control prevents potential core saturation of the push-pull transformer due to mismatches in timing and in component tolerances. With average current mode control, precise control of the inductor current feeding the push-pull stage is possible without the noise sensitivity associated with peak current mode control. The UC3827 average current mode loop can also be connected in parallel with the voltage regulation loop to assist only in fault conditions.

Other valuable features of the UC3827 include bidirectional synchronization capability, user programmable overlap time (UC3827-1), user programmable gap time (UC3827-2), a high bandwidth differential current sense amplifier, and soft start circuitry.

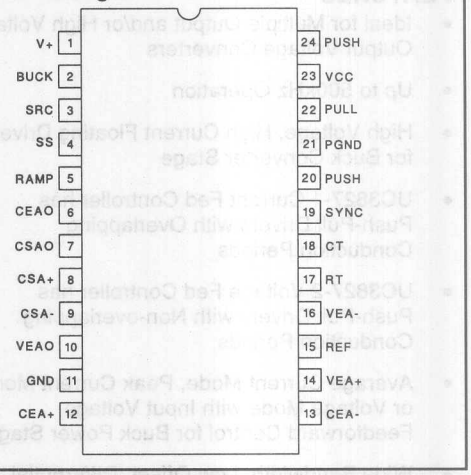
ABSOLUTE MAXIMUM RATINGS

Supply Voltage, VCC 20V
Input Voltage Range
  For all pins except V+, BUCK, SRC . . . . . –0.3V to 5V
  For V+ and BUCK 90V
  For SRC. 90V–VCC
BUCK Driver
  IO Continuous . . . . . ±250mA
  IO Peak . . . . . ±1A
PUSH/PULL Driver
  IO Continuous . . . . . ±200mA
  IO Peak . . . . . ±0.8A
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

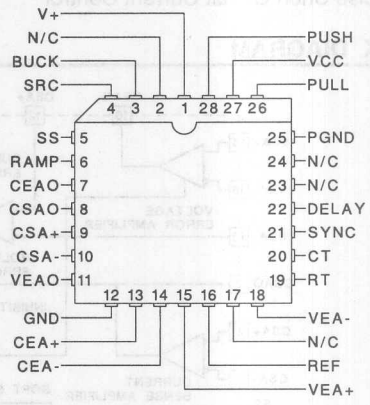
Voltages are referenced to ground. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAMS

DIL-24 (Top View)
N or J, DW Packages



PLCC-28 (Top View)
Q Package



ELECTRICAL CHARACTERISTICS

Unless otherwise specified, 0°C to 70°C for the UC3827-1/-2, –40°C to 85°C for the UC2827-1/-2 and –55°C to 125° for the UC1827-1/-2. VCC = 15V, V+ = 14.3V, CT = 340pF, RT = 10K, R_{DELAY} = 24.3k, SRC = GND, BUCK, PUSH and PULL outputs no load. $T_J = T_A$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply					
VCC UVLO, Turn-On		8.2	9	9.8	V
Hysteresis		0.3	0.6	0.9	V
Ivcc Start	VCC = 8V			1000	µA
Ivcc Run			32	45	mA
V+ UVLO, Turn-On		7.1	7.5	7.9	V
V+ Hysteresis		0.2	0.4	0.8	V
Iv+ Buck High		0.2	1	3	mA

ELECTRICAL CHARACTERISTICS (cont.) Unless otherwise specified, 0°C to 70°C for the UC3827-1/-2, –40°C to 85°C for the UC2827-1/-2 and –55°C to 125° for the UC1827-1/-2. VCC = 15V, V+ = 14.3V, CT = 340pF, RT = 10K, RDELAY = 24.3k, SRC = GND, BUCK, PUSH and PULL outputs no load. $T_J = T_A$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Voltage Error Amplifier					
IB			0.5	3	µA
VIO				10	mV
AVOL		80	95		dB
GBW	(Note 7)	2	4		MHz
VOL			0.3	0.5	V
VOH		2.85	3	3.15	V
Current Sense Amplifier					
IB			–1	–5	uA
VIO				5	mV
AVOL		80	110		dB
GBW	(Note 7)	20	29		MHz
VOL			0.6	1	V
VOH		3	3.3		V
Common Mode Range	(Note 7)	0		2	V
Current Error Amplifier					
IB			–1	–5	µA
VIO				10	mV
AVOL		80	110		dB
GBW	At 100kHz, Measure Gain	2	4.5		MHz
VOL			0.3	1	V
VOH		3.3	3.5		V
Common Mode Range	(Note 7)	0		5	V
Oscillator					
Frequency		150	200	250	kHz
CT Discharge Current	3.5V at CT when CT removed	7			mA
PWM Comparator					
Minimum Duty Cycle	200kHz			0	%
Maximum Duty Cycle	200kHz	85	90	95	%
Buck Output Stage					
Rise Time	1nF Load, (Note 3)		40	100	ns
Fall Time	1nF, Load		30	100	ns
VOH	I_{BUCK} = –15mA , V+ –BUCK (Note 4)		1.5	2.5	V
	I_{BUCK} = –150mA, V+ – BUCK (Note 4)		2	2.5	V
VOL	I_{BUCK} = 15mA (Note 5)		0.2	0.4	V
	I_{BUCK} = 150mA (Note 5)		0.7	1.2	V
Push/Pull Output Stages					
Rise Time	1nF Load		50	100	ns
Fall Time	1nF Load		35	100	ns
Overlap Time, -1 Only	1nF loads (Note 1)		185		ns
Non-Overlapping Time, -2 Only	(Note 2)		185		ns
VOH	$I_{PUSH/PULL}$ = –10mA, VCC – PUSH (Note 6)		2	3	V
	$I_{PUSH/PULL}$ = –100mA, VCC – PUSH (Note 6)		2.5	3	V
VOL	$I_{PUSH/PULL}$ = 10mA (Note 6)		0.2	0.4	V
	$I_{PUSH/PULL}$ = 100mA (Note 6)		0.6	1.2	V

ELECTRICAL CHARACTERISTICS (cont.) Unless otherwise specified, 0°C to 70°C for the UC3827X, –40°C to 85°C for the UC2827X and –55°C to 125° for the UC1827X. VCC = 15V, V+ = 14.3V, CT = 340pF, RT = 10K, RDELAY = 24.3k, SRC = GND, BUCK, PUSH and PULL outputs no load. $T_J = T_A$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Reference					
REF Voltage		4.8	5	5.2	V
Short Circuit Current	REF = 0V	–35	–50	–65	mA
Line Regulation	9.5V < VCC < 20V		5	20	mV
Load Regulation	0mA < IO < 10mA		8	20	mV
Soft Start					
VOL, Saturation	VCC = 7V		250	500	mV
Iss		–5	–12	–25	µA

Note 1: The overlap time is measured from the point at which the rising edge of PUSH/PULL crosses 5V until the falling edge of PULL/PUSH crosses 5V.

Note 2: The non-overlap time is measured from the point at which the falling edge of PUSH/PULL crosses 5V until the rising edge of PULL/PUSH crosses 5V.

Note 3: Measure the rise time from when BUCK crosses 1V until it crosses 9V.

Note 4: To force BUCK high, force CSAO=2.5V, CEAO = 2.5V, a 25k pulldown resistor form RAMP to ground, and CT = 0.5V.

Note 5: To force BUCK low, force CSAO = 2.5V, CEAO = 2.5V, a 10k pulldown resistor from RAMP to ground, and CT = 3.5V.

Note 6: To toggle PUSH or PULL into a desired state, pulse CT from 0.5V to 3.5V. PUSH and PULL toggle on the rising edge of CT.

Note 7: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

BUCK: Output of the buck PWM controller. The BUCK output is a floating driver, optimized for controlling the gate of an N-channel MOSFET. The peak sink and source currents are 1A. Any undervoltage faults will disable BUCK to an off condition (low).

CEA+: The non-inverting input of the current error amplifier.

CEA-: The inverting input of the current error amplifier.

CEAO: The output of the current error amplifier and the inverting input of the PWM comparator of the buck converter.

CSA+: The noninverting input of the current sense amplifier.

CSA-: The inverting input of the current sense amplifier.

CSAO: The output of the current sense amplifier and the noninverting input of the current limit comparator. When the signal level on this pin exceeds the 3V threshold of the current limit comparator, the buck gate drive pulse is terminated. This feature is useful to implement cycle-by-cycle current limiting for the buck converter.

CT: This pin is provided for the timing capacitor which is connected between CT and GND. The oscillator frequency is set by CT and a resistor RT, connected between pin RT and GND. The CT discharge current is approximately 40X the bias current through the resistor connected to RT. A practical maximum value for the discharge current is 20mA. The frequency of the oscillator is given by:

$$f_{OSC} = \frac{0.77}{R_T \bullet C_T}$$

DELAY: A resistor to GND programs the overlap time of the PUSH and PULL outputs of the UC3827-1 and the dead time of the PUSH and PULL outputs of the UC3827-2. The minimum value of the resistor, RDELAY, is 18kΩ. The delay or overlap time is given by:

$$T_{DELAY} = \frac{R_{DELAY}}{150\Omega} \bullet 10^{-9}\text{sec.}$$

GND: This pin is the ground reference for all sensitive setup components not related to driving the outputs. They include all timing, voltage sense, current sense, and bypass components.

PGND: Ground connection for the PUSH and PULL outputs. PGND must be connected to GND at a single point on the printed circuit board. This is imperative to prevent large, high frequency switching currents flowing through the ground metalization inside the IC.

PULL: Ground referenced output to drive an N-channel MOSFET. The PULL and the PUSH outputs are driving the two switches of the push-pull converter with complementary signals at close to a 50% duty cycle. Any undervoltage faults will disable PULL to an off condition (low).

PIN DESCRIPTIONS (cont.)

PUSH: Ground referenced output to drive an N-channel MOSFET. The PULL and the PUSH outputs are driving the two switches of the push-pull converter with complementary signals at close to a 50% duty cycle. Any undervoltage faults will disable PUSH to an off condition (low).

RAMP: The RAMP voltage, after a 700mV internal level shift, is fed to the noninverting input of the buck PWM comparator. A resistor to Vin and a capacitor to GND provide an input voltage feedforward signal for the buck controller in voltage mode control. In peak current mode control, the RAMP pin receives the current signal of the buck converter. In an average current mode setup, the RAMP pin has a linearly increasing ramp signal. This waveform may be generated either by connecting RAMP directly to CT, or by connecting both a resistor from VCC to RAMP and a capacitor from RAMP to GND.

REF: The output of the +5V on board reference. Bypass this pin with a capacitor to GND. The reference is off when the chip is in undervoltage lockout mode.

RT: A resistor to GND programs the charge current of the timing capacitor connected to CT. The charge current approximately equals

$$\frac{REF}{2 \bullet R_T}.$$

The charge current should be less than 500µA to keep CT's discharge peak current less than 20mA, which is CT's maximum practical discharge value. The discharge time, which sets the maximum duty cycle, is set internally and is influenced by the charge current.

SRC: The source connection for the floating buck switch. The voltage on the SRC pin can exceed VCC but must be lower than 90V-VCC. Also, during turn-off transients of the buck switch, the voltage at SRC can go to –2V.

SS: The soft start pin requires a capacitor to GND. During soft start the output of the voltage error amplifier is clamped to the soft start capacitor voltage which is slowly charged by an internal current source. In UVLO, SS is held low.

SYNC: SYNC is a bidirectional pin for the oscillator. This pin can be used to synchronize several chips to the fastest oscillator. Its input synchronization threshold is 1.4V. The SYNC voltage is 3.6V when the oscillator capacitor, CT, is discharged. Otherwise it is 0V. If the recommended synchronization circuit is not used, a 1k or lower value resistor from SYNC to GND may be needed to increase the fall time of the signal at SYNC.

VCC: A voltage source connected to this pin supplies the power for the UC3827. It is recommended to bypass this pin to both GND and PGND ground connections with good quality high frequency capacitors.

VEA+: The non-inverting input of the voltage error amplifier.

VEA-: The inverting input of the voltage error amplifier.

VEAO: The output of the voltage error amplifier.

V+: Supply voltage for the buck output. The floating driver of the UC3827 uses the bootstrap technique which requires a reservoir capacitor to store the required energy for the on time of the buck switch. A diode must be connected from VCC to V+ to charge the reservoir capacitor. This diode must be able to withstand Vin. The reservoir capacitor must be connected between V+ and SRC and its voltage is monitored directly by the undervoltage lockout circuitry of the buck driver.

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UNITRODE

UCC1829-1/-2
UCC2829-1/-2
UCC3829-1/-2

PRELIMINARY

High Speed PWM Controller

FEATURES

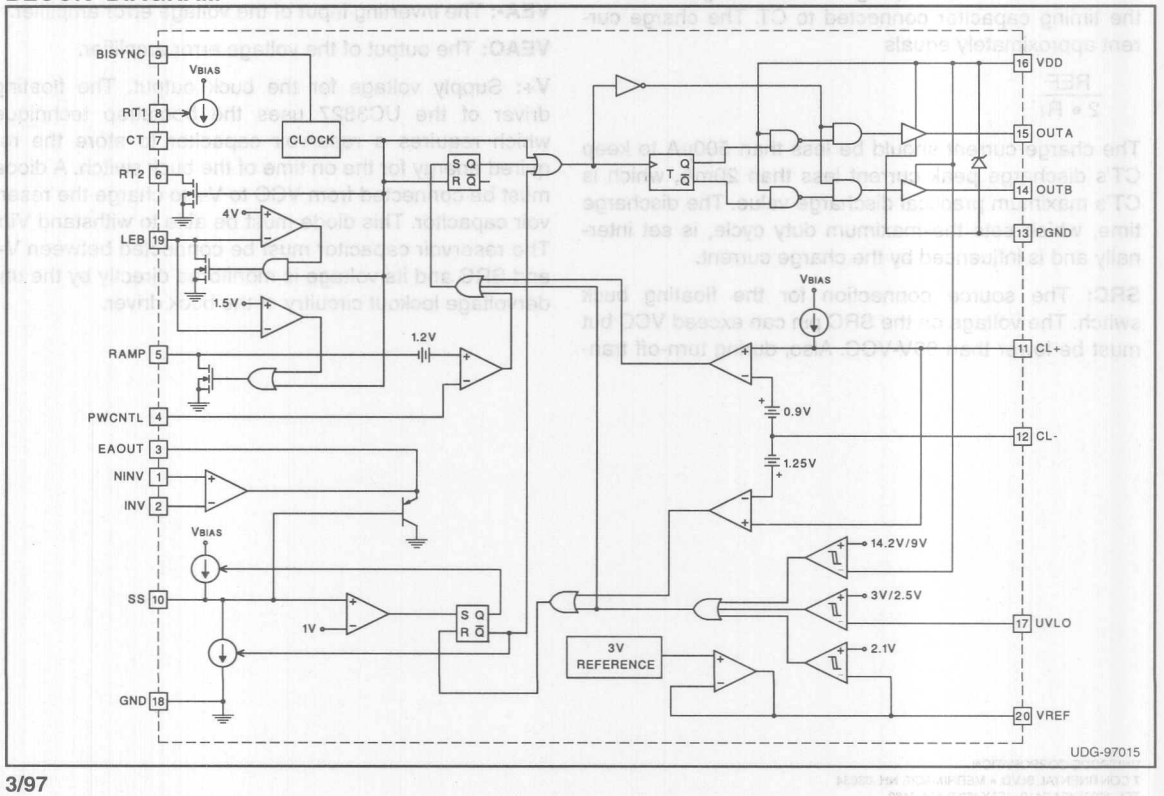
- Compatible with Voltage or Current Mode Topologies
- Practical Operation at Switching Frequencies to 4MHz
- 50ns Propagation Delay to Output
- High Current Complementary Outputs
- Programmable Dead Time and Frequency Oscillator
- Pulse by Pulse Current Limiting
- Latched Overcurrent Comparator with Full Cycle Restart
- Programmable Undervoltage Lockout (UVLO)
- Adjustable Blanking for leading Edge Noise Tolerance

DESCRIPTION

The UCC3829 is a BiCMOS High Speed PWM Controller IC. It is optimized for high frequency switched mode power supply applications. The IC can be used in both voltage mode and current mode control applications. Care was given to minimizing the propagation delays through the comparators and logic circuitry while maximizing the bandwidth and slew rate of the error amplifier. The oscillator frequency and deadtime can be programmed via two external resistors and a capacitor. The undervoltage lockout threshold can be programmed using an external resistor divider. The current limit and overcurrent threshold can be set externally. The chip is available in either single ended or push-pull output configuration.

Fault protection circuitry includes undervoltage detection for the internal bias supply, and overcurrent detection. The fault detection logic sets a latch that ensures full discharge of the soft start capacitor before allowing a restart. While the fault latch is set, the outputs are in a low state. In the event of continuous faults, the soft start capacitor is fully charged before discharging to insure that the fault frequency does not exceed the designed soft start period.

BLOCK DIAGRAM



3/97

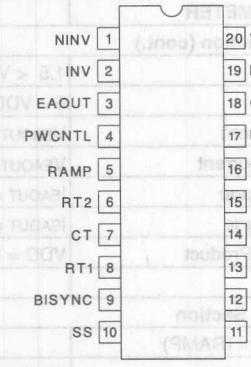
ABSOLUTE MAXIMUM RATINGS

Supply Voltage 15V
Supply Current 25mA
Output Current (OUTA, OUTB, PGND, VCC)
DC 0.5A
Pulsed (0.5µsec) 2.2A
PGND . . . . . ± 0.2V
Analog Inputs
INV, NINV, RAMP, SS. . . . . –0.3 to 7V
CL+, CL- . . . . . –1.5V to 6V
Error Amplifier Output Current 5mA
Error Amplifier Output Capacitance 20pF
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10sec.) . . . . . +300°C

Unless otherwise indicated, voltages are referenced to GND. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of package.

CONNECTION DIAGRAM

DIL-20, SOIC-20 (Top View)
N Package, DW Package



ORDERING INFORMATION

UCC ☐ 829 ☐ - ☐
OUTPUT
PACKAGE
TEMPERATURE RANGE

PART VERSION TABLE

PART NUMBER	OUTPUT	OUT A/B PHASE	OUTPUT FREQUENCY
UCCX829-1	Push-Pull	180°C Out of Phase	Half of -2
UCCX829-2	Single-Ended	In Phase	

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, 0°C to 70°C for the UCC3829-1/-2, –40°C to 85° for the UCC2829-1/-2 and –55°C to 125°C for the UCC1829-1/-2. RT1 = 33.2kΩ, CT = 470pF, RT2 = 392Ω, VDD = 12V. $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Reference Section					
Output Voltage	T_J = 25°C	2.97	3	3.03	V
Line Regulation	4.5V < VDD < 15V	–10		10	mV
Load Regulation	0 < I_{REF} < 5mA			10	mV
Total Output Variation	Line, Load, Temperature	2.94		3.06	V
Short Circuit Current	VREF = 0			25	mA
Oscillator Section					
Initial Accuracy	T_J = 25°C (Note 1)	360	400	440	kHz
Total Variation	Line, Temperature (Note 1)	350		450	kHz
Voltage Stability	12 < VDD < 15			1	%
Temperature Stability	$T_{MIN} < T_A < T_{MAX}$ (Note 1)		5	10	%
Initial Accuracy	RT1 = 25.7k, CT = 150pF, T_J = 25°C (Note 1)	0.9	1	1.1	MHz
Total Variation	RT1 = 25.7k, CT = 150pF, Line, Temperature (Note 1)	0.85		1.15	MHz
Ramp Peak		2			V
Ramp Valley				1	V
BISYNC Output Source Current	V_{BISYNC} = VDD – 0.5V		–200	–100	µA
BISYNC Output Sink Current	V_{BISYNC} = 0.5V	2	2.5		mA
BISYNC Input Threshold			1.5		V
Error Amplifier Section					
Input Offset Voltage				5	mV
Input Bias Current		–1		1	µA
Input Offset Current				250	nA
Open Loop Gain		70	80		dB

ELECTRICAL CHARACTERISTICS (cont.): Unless otherwise specified, 0°C to 70°C for the UCC3829-1/-2, –40°C to 85° for the UCC2829-1/-2 and –55°C to 125°C for the UCC1829-1/-2. RT1 = 33.2kΩ, CT = 470pF, RT2 = 392Ω, VDD = 12V. $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Error Amplifier Section (cont.)					
CMRR	1.5 < VCM < (VIN – 0.5)	75			dB
PSRR	5 < VDD < 15	75			dB
Output Sink Current	V_{EAOUT} = 1V, 5V < VDD < 15V	300	500		µA
Output Source Current	V_{EAOUT} = 3.5V, 5V < VDD < 15V		500	300	µA
Output High Voltage	I_{EAOUT} = –300µA	3	5		V
Output Low Voltage	I_{EAOUT} = 300µA		0.6	1	V
Gain Bandwidth Product	VDD = 12V, Temperature 25°C	8	10		MHz
Slew Rate		>>1.5	2		V/µs
PWM Comparator Section					
Input Bias Current (RAMP)		–1		1	µA
Minimum Duty Cycle	400kHz			0	%
Maximum Duty Cycle (UCC3829-1)	400 kHz, RT2 Resistor = 1Ω	42.5			%
Maximum Duty Cycle (UCC3829-2)	400kHz, RT2 Resistor = 1Ω	85			%
Delay to Output	T = 25°C T_{YP} = VDD = 12		50	100	ns
Current Limit Fault Section					
Soft Start Charge Current		–30		–10	µA
Full Soft Start Threshold	NINV Voltage		3		V
Restart Discharge Current		10		30	µA
Restart Threshold			1		V
Current Limit Threshold	Relative to CL-		0.875		V
Overcurrent Threshold	Relative to CL-		1.25		V
Current Limit Delay to Output	Over all Temperature, VDD >= 12V		50	100	ns
	Over all Temperature, Supply		100	400	ns
Output Section					
Output Low Saturation	I_{OUT} = 200mA, T_J = 25°C			0.5	V
Output High Saturation	I_{OUT} = –100mA, T_J = 25°C			0.5	V
UVLO Output Low Saturation	At 10mA		0.8	1.5	V
Rise Time	C_{LOAD} = 1nF, TJ = 25°C		20	40	ns
Fall Time	C_{LOAD} = 1nF, TJ = 25°C		10	20	ns
Output Source Current	V_{OUT} = 0, TJ = 25°C, T (Note 1)		–0.75		A
Output Sink Current	V_{OUT} = 12V, TJ = 25°C (Note 1)		1.5		A
Undervoltage Lockout					
UVLO Enable Threshold			3		V
UVLO Hysteresis			0.5		V
VDD UVLO Enable Threshold		13.5		15	V
VDD UVLO Hysteresis		3.5		7	V
Supply Section					
Startup Current	V_{UVLO} = 2, VDD = 13.5			1	mA
ICC	400kHz		8		mA
VDD Range	C_{LOAD} = 0nF	4.25		15	V

Note 1: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

BISYNC: Combination clock output/sync input pin. The clock signal can be viewed on this pin. If BISYNC is connected to BISYNC of other UCC3829-1/-2 chips, all the oscillators will run at the highest of all the chips frequencies. The BISYNC pin has a weak pull down and a strong pull up.

CL+: Current sense input for current limiting. The CL+ and CL- pins are used for current sensing. CL+ is the current signal while CL- is the kelvin return for the sensing function.

CL-: Current sense input kelvin common.

CT: Oscillator timing capacitor. A capacitor connected between CT and GND is charged by a current source controlled by RT1. The capacitor is discharged through a resistor connected between CT and RT2.

EAOUT: Error amplifier output. This output is normally connected directly to the RAMP pin. It can also be connected to RAMP through a resistor divider attenuation network to allow more swing of the error amplifier output. A maximum capacitive load of 20pF with respect to ground must be observed to insure stability of the error amplifier.

GND: Logic and analog ground. The GND pin should be used for all signal level returns, except the current sense inputs.

INV: Error amplifier inverting input.

LEB: Leading edge blanking programming pin. Connecting a resistor between VREF and LEB and a capacitor between LEB and GND will program a leading edge blanking time according to the RC of the resistor/capacitor combination. Connecting the LEB pin to VDD disables the Leading Edge Blanking function.

NINV: Error amplifier non-inverting input.

OUTA: Output A. The OUTA pin will pull down with approximately 1.5A and pull up with approximately 0.75A. The UCC3829-1 implements push-pull outputs with OUTA and OUTB active on alternating clock cycles. The UCC3829-2 implements OUTA and OUTB being in phase. The output frequency of the UCC3829-1 is half that of the UCC3829-2 .

OUTB: Output B. The OUTB pin will pull down with approximately 1.5A and pull up with approximately 0.75A. The UCC3829-1 implements push-pull outputs with OUTA and OUTB active on alternating clock cycles. The UCC3829-2 implements OUTA and OUTB being in phase. The output frequency of the UCC3829-1 is half that of the UCC3829-2 .

PGND: Power ground return. The PGND pin should be used as the return for the VDD bypass capacitor and the current sense kelvin CL-.

PWCNTL: Pulse width control input. This is connected to the PWM comparator inverting input.

RAMP: Ramp input . This is connected to the PWM comparator non-inverting input through a level shifting voltage of approximately 1.25V.

RT1: Oscillator charging current programming resistor. A 1V reference at this pin generates a current through a resistor connected between RT1 and GND. This current is mirrored and ratioed to charge the timing capacitor connected to pin CT.

RT2: Oscillator discharge time programming resistor. The oscillator (and output) dead time can be programmed via this pin. The discharge of the timing capacitor C_T is determined by an RC discharge using a resistor connected between RT2 and C_T.

SS: Soft start capacitor pin. A capacitor connected to SS determines the time the IC takes to soft start. The nominal SS pin pull up and pull down current is 20µA. The soft start time delay is approximately calculated as:

$$\frac{C_{SS} \bullet 3V}{20\mu A}$$

when charging from 0V. The restart time is approximately:

$$\frac{2 \bullet C_{SS} \bullet 3V}{20\mu A}$$

UVLO: Undervoltage lockout programming pin. Connecting a resistor divider between VDD, UVLO, and GND sets a VDD value at which the UCC3829-1/-2 chip will be enabled. When the voltage on the UVLO pin reaches 3V, the chip is enabled. When the voltage on UVLO falls below 2.5V, the chip is disabled.

VDD: Voltage supply to IC.

VREF: Voltage reference output and filtering. The voltage reference output appears on the VREF pin. It is buffered to drive approximately 5mA and short circuit protected at approximately 25mA. A bypass capacitor of at least 0.1µF must be connected from VREF to ground.

DESCRIPTION OF OPERATION

Oscillator

The oscillator uses an external capacitor C_T and two external resistors R_{T1} and R_{T2} to generate the clock frequency and dead time. A precise reference voltage is placed across resistor R_{T1} to generate a current reference. The current is then mirrored and used to charge the capacitor C_T from GND. When a "peak" threshold is reached, an on chip MOSFET connects the RT2 pin to GND, discharging CT to a "valley" threshold through an external resistor R_{T2}. The CT waveform has a linear ramp shape while charging and an exponential (RC) slope while discharging. The slope of the charging ramp is set by the C_T, R_{T1} combination and the slope of the discharging ramp is set by the values of C_T and R_{T2}.

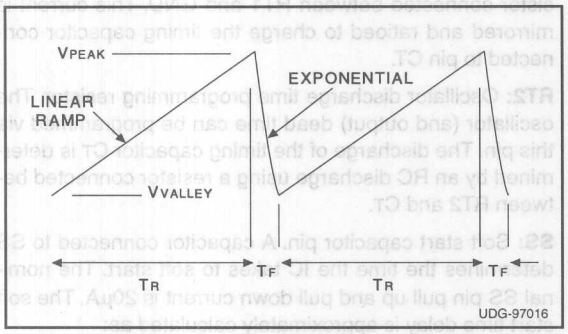


Figure 1.

The approximate equation for the rising edge (T_R) of the C_T waveform (maximum on-time period) is:

$$T_R = C_T R_{T1} \left(\frac{V_{PEAK} - V_{VALLEY}}{9.3} \right).$$

The approximate equation for the falling edge (T_F) of the C_T waveform (deadtime period) is:

$$T_F = R_{T2} C_T 1n \left(\frac{V_{Peak} - \frac{9.3 R_{T2}}{R_{T1}}}{V_{VALLEY} - \frac{9.3 R_{T2}}{R_{T1}}} \right).$$

Assuming that:

$$\frac{9.3 R_{T2}}{R_{T1}} < V_{PEAK} \text{ and } \frac{9.3 R_{T2}}{R} T1 << V_{VALLEY}$$

we get a simplified equation:

$$T_F = R_{T2} C_T 1n \left(\frac{V_{PEAK}}{V_{VALLEY}} \right).$$

Given a maximum on-time and frequency and assuming an initial value for either R_{T2} or C_T, you can use the T_F equation to calculate the other. Once you have a value for CT, you can calculate RT1 using the T_R equation .

Error Amplifier Section

The Error Amplifier has both inputs and the output brought out to pins NINV, INV, and EAOUT. The output of the error amplifier can be connected to the inverting input of the PWM comparator via the pin PWCNTL. This allows inserting attenuation which enables using the full output swing of the error amplifier. The output of the error amplifier is forced to follow the soft start waveform during soft start.

PWM and Output Section

The non-inverted input of the PWM comparator is connected to RAMP. The RAMP can be connected to either the C_T capacitor for voltage mode control, to the current sense resistor for current mode control, or to a feed forward capacitor for input voltage feed forward control. The C_T waveform can be coupled to RAMP to provide slope compensation in the current mode case. The MOSFET switch connected to RAMP provides for the discharge of the feedforward capacitor. There is a short time constant (3ns) filter across the inputs of the PWM comparator to reduce noise.

The output of the PWM comparator feeds an OR gate which, together with several other fault signals, sets the PWM latch. The latch is in turn reset on every dead time period of the clock waveform. The output of the PWM latch is OR'ed with the clock and the output of the Fault Latch (described below) to feed into the pulse steering Toggle Flip-Flop (TFF). The resulting signal is then steered to either the A or B output depending on the state of the TFF, enabling use in a push/pull application. The clock output becomes the deadtime between the outputs.

Leading Edge Blanking Section

The Leading Edge Blanking circuit provides a means to insert a blanking period at the beginning of the cycle, providing noise pulse elimination for current mode control applications. This feature is similar to that of the UC3825 and UC3823A/B ICs. When enabled, an external resistor is connected from LEB to VREF. An external capacitor is connected from LEB to either VREF or GND. During the deadtime, LEB is pulled to GND. At the beginning of the cycle, the pin is released and the capacitor charges through the resistor toward VREF. At the threshold VREF/2, a comparator senses the voltage and LEB is re-

DESCRIPTION OF OPERATION

moved. The leading edge blanking function can be disabled by connecting LEB to VDD (> VREF). Leading edge blanking is performed by the same MOSFET switch connected to RAMP that is used for voltage feed forward operation.

Current Sense Section

The current limit and overcurrent functions are accomplished using the pins CL+ and CL-. These two pins provide for differential current level sensing, with the trip points referenced to CL-, rather than GND. The current limit function provides a pulse by pulse current limiting, whereas the overcurrent function is considered a fault condition and initiates a fault logic soft start cycle.

Fault Logic Section

The fault logic detects and handles various fault conditions in the system. The output of the overcurrent comparator is logically ORed with the output combination of the undervoltage detection circuit ORed with the output of the VREF good circuit. The output of the precision reference voltage VREF is compared to a level (approximately 3 V_{BE} voltages) to determine if the reference is alive. The undervoltage circuit either uses a user programmed level with a 16% hysteresis or an on threshold equal to the VDD clamp voltage and an off threshold of 9V.

Once a fault occurs, a soft start cycle takes place. A fault sets the fault latch. The Q output of the fault latch sets the RS delay latch and turns on the 20µA soft start discharge current sink. The Q output of the fault latch is gated, however, by the output of the S_S complete comparator. This insures that a SS cycle cannot start before the previous one has finished. The soft start capacitor then is discharged to 1V which is sensed by the R_S delay comparator. The fault latch is then reset. This in turn resets the R_S delay latch and turns off the 20µA current sink and turns on a 20µA current source to charge the S_S capacitor.

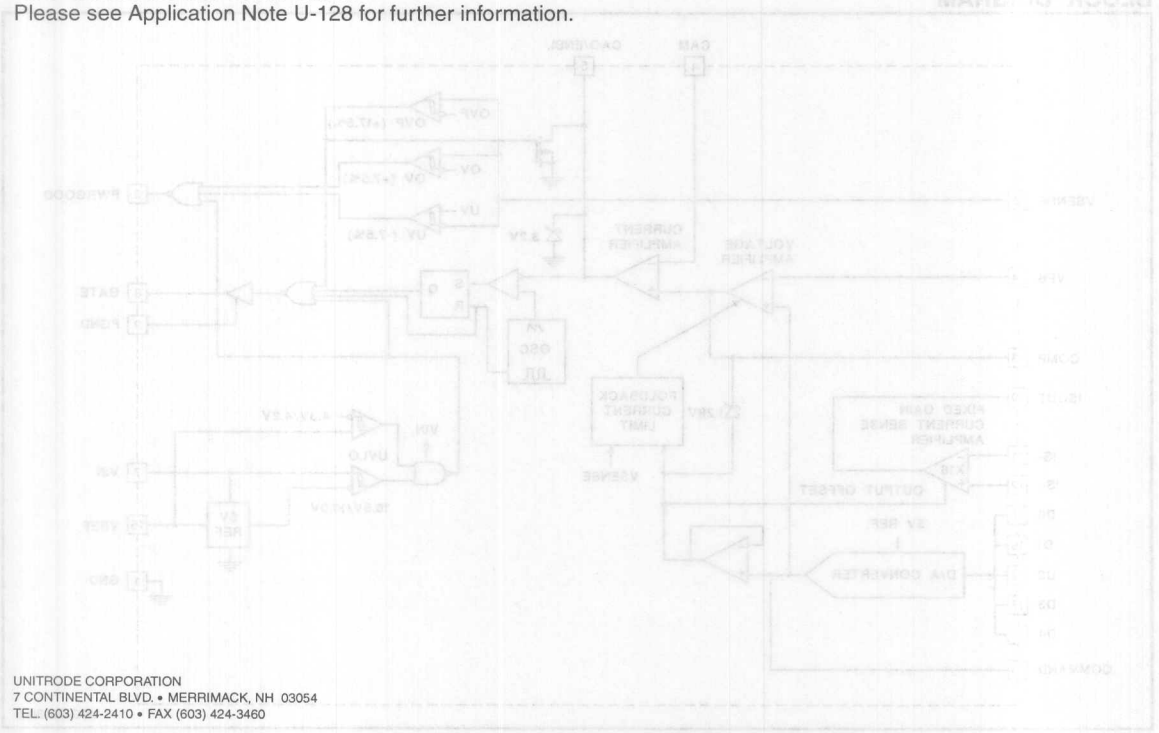
The under voltage detection is set to a default value of 14V turn on (VDD clamp active value) and 9V turn off when the UVLO pin is tied to GND. This default configuration can be overridden by connecting a resistor divider between VDD and GND to the UVLO pin. The hysteresis for the user set threshold is 16%.

Supply Section

The incoming voltage supply VDD is clamped by a shunt VDD Clamp circuit.

APPLICATION INFORMATION

Please see Application Note U-128 for further information.



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5-Bit Microprocessor Power Supply Controller

FEATURES

- 5-Bit Digital-to-Analog Converter (DAC)
- Supports 4-Bit and 5-Bit Microprocessor VID Codes
- Combined DAC/Voltage Monitor and PWM Functions
- 1% DAC/Reference
- Current Sharing
- 100kHz, 200kHz, 400kHz Oscillator Frequency Options
- Foldback Current Limiting
- Overvoltage and Undervoltage Fault Windows
- Undervoltage Lockout
- 2Ω Totem Pole Output
- Chip Disable Function

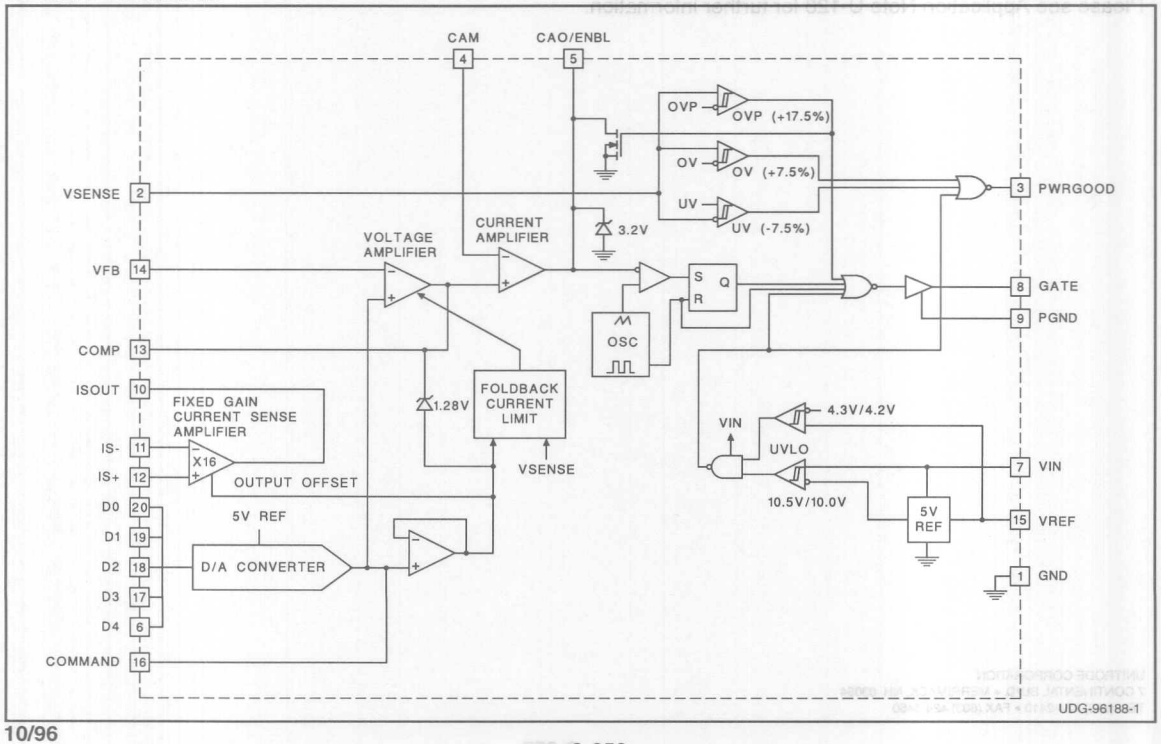
DESCRIPTION

The UCC3830-4/-5/-6 is a fully integrated single chip solution ideal for powering high performance microprocessors. The chip includes an average current mode PWM controller, has a fully integrated 5-Bit DAC, and includes an onboard precision reference and voltage monitor circuitry. The UCC3830-x converts 5VDC to an adjustable output, ranging from 3.5VDC down to 1.8VDC with 1% DC system accuracy. The UCC3830-x supports Intel's current 4-bit VID architecture and is also fully forward compatible with Intel's next generation Pentium® Pro microprocessors.

The chip includes a precision 5V reference which is capable of sourcing current to an external load. The output voltage of the DAC is derived from this reference, and is programmed directly by Intel's VID pins.

The accuracy of the DAC/reference combination is 1%. The overvoltage and undervoltage comparators monitor the system output voltage and indicate when it rises above or falls below its programmed value by more than 7.5%. A second overvoltage protection comparator pulls the current amplifier output voltage low to force zero duty cycle when the system output voltage exceeds its designed value by more than 17%. This comparator also terminates the cycle. Undervoltage lockout circuitry assures the correct logic states at the outputs during powerup and powerdown. The gate output can be disabled by bringing the CAO/ENBL pin to below 0.8V. **(continued)**

BLOCK DIAGRAM



DESCRIPTION (cont.)

The voltage and current amplifiers have a 4MHz gain bandwidth product to satisfy high performance system requirements. The internal current sense amplifier permits the use of a low value current sense resistor, minimizing power loss. The oscillator frequency is fixed internally at 100kHz, 200kHz, or 400kHz, depending upon the option selected. The foldback circuit reduces the converter short circuit current limit to 50% of its nominal value when the converter is short circuited. The gate driver is a 2Ω totem pole output stage capable of driving an external MOSFET.

This device is available in 20-pin dual in-line and surface mount packages. The UCC2830-x is specified for operation from –25°C to 85°C, and the UCC3830-x is specified for operation from 0°C to 70°C.

Pentium® Pro is a registered trademark of Intel Corporation.

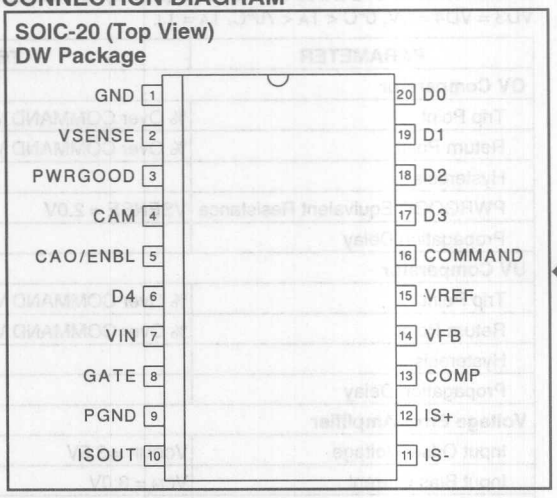
ORDERING INFORMATION

UCC □ 830 □ - □
- See Frequency Gain Table
- Package
- Temperature Range

Consult factory for temperature range or package options not shown.

CONNECTION DIAGRAM

SOIC-20 (Top View)
DW Package



Frequency Gain Table

	Frequency		
	100kHz	200kHz	400kHz
UCC3830-4	X		
UCC3830-5		X	
UCC3830-6			X

3 GENERAL POWER SUPPLY

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, VIN = 12V, VSENSE = 3.5V, VD0 = VD1 = VD2 = VD3 = VD4 = 0V, 0°C < T_A < 70°C, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Undervoltage Lockout					
VIN UVLO Turn-on Threshold			10.5	10.8	V
VIN UVLO Turn-off Threshold		9.5	10		V
UVLO Threshold Hysteresis			500		mV
Supply Current					
I_{IN}			3.5		mA
DAC/Reference					
COMMAND Voltage Accuracy	10.8V < VIN < 13.2V, I_{VREF} = 0mA	–1		1	%
D0-D4 Voltage High	DX Pin Floating		5		V
D0-D4 Input Bias Current	DX Pin Tied to GND		–70	–20	µA
VREF Output Voltage		4.975	5	5.025	V
VREF Load Regulation	I_{VREF} = 0mA to 5mA	–10	0		mV
VREF Sourcing Current	VREF = 0V		10		mA
OVP Comparator					
Trip Point	% Over COMMAND Voltage	10	17.5	25	%
Hysteresis			20	30	mV
VSENSE Input Bias Current	OV, OVP, UV Combined		–0.1		µA
Propagation Delay			1		µs

ELECTRICAL CHARACTERISTICS (cont.): Unless otherwise specified, VIN = 12V, VSENSE = 3.5V, VD0 = VD1 = VD2 = VD3 = VD4 = 0V, 0°C < T_A < 70°C, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
OV Comparator					
Trip Point	% Over COMMAND Voltage (Note 1)		7.6		%
Return Point	% Over COMMAND Voltage (Note 1)		7.4		%
Hysteresis			20	30	mV
PWRGOOD Equivalent Resistance	VSENSE = 2.0V			470	Ω
Propagation Delay			1		µs
UV Comparator					
Trip Point	% Over COMMAND Voltage (Note 1)		–7.6		%
Return Point	% Over COMMAND Voltage (Note 1)		–7.4		%
Hysteresis			20	30	mV
Propagation Delay			1		µs
Voltage Error Amplifier					
Input Offset Voltage	V_{COMP} = 3.5V		0.0		mV
Input Bias Current	V_{CM} = 3.0V		–0.02	0	µA
Open Loop Gain	1V < V_{COMP} < 4V		90		dB
Common Mode Rejection Ratio	1.8V < V_{COMP} < 3.5V		90		dB
Power Supply Rejection Ratio	10.8V < VIN < 15V		85		dB
Output Sourcing Current	V_{VFB} = 2V, $V_{COMMAND}$ = V_{COMP} = 2.5V		–0.5		mA
Output Sinking Current	V_{VFB} = 3V, $V_{COMMAND}$ = V_{COMP} = 2.5V		2.0		mA
Gain Bandwidth Product	F = 100kHz		3		MHz
Current Sense Amplifier					
Gain			16		V/V
Input Resistance			5		kΩ
Common Mode Rejection Ratio	0V < V_{CM} < 4.5V		60		dB
Power Supply Rejection Ratio	10.8V < VIN < 15V		80		dB
Output Sourcing Current	V_{IS-} = 2V, V_{ISOUT} = V_{IS+} = 2.5V		–0.5		mA
Output Sinking Current	V_{IS-} = 3V, V_{ISOUT} = V_{IS+} = 2.5V		6.0		mA
–3dB Frequency	At GAIN = 16		2		MHz
Current Amplifier					
Input Offset Voltage	V_{CM} = 3.0V			10	mV
Input Bias Current	V_{CM} = 3.0V		0.15		µA
Open Loop Gain	1V < $V_{CAO/ENBL}$ < 3V		90		dB
Output Voltage High	V_{COMP} = 3V, V_{CAM} = 2.5V		3.2		V
Common Mode Rejection Ratio	1.5V < V_{CM} < 4.9V		80		dB
Power Supply Rejection Ratio	10.8V < VIN < 15V		80		dB
Output Sourcing Current	V_{CAM} = 2V, $V_{CAO/ENBL}$ = V_{COMP} = 2.5V		–0.5		mA
Output Sinking Current	V_{CAM} = 3V, $V_{CAO/ENBL}$ = V_{COMP} = 2.5V		2.0		mA
Gain Bandwidth Product	F = 100kHz		3.5		MHz
Oscillator					
Frequency (-4)		85	100	115	kHz
Frequency (-5)			200		kHz
Frequency (-6)			400		kHz
Frequency Change With Voltage	10.8V < VIN < 15V		1		%

ELECTRICAL CHARACTERISTICS (cont.): Unless otherwise specified, VIN = 12V, VSENSE = 3.5V, VD0 = VD1 = VD2 = VD3 = VD4 = 0V, 0°C < T_A < 70°C, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Section					
Maximum Duty Cycle		90	95	99	%
Output Low Voltage	I_{GATE} = –100mA		0.2		V
Output High Voltage	I_{GATE} = 100mA		11.8		V
Rise Time	C_{GATE} = 3.3nF		20	80	ns
Fall Time	C_{GATE} = 3.3nF		15	80	ns
Output Impedance	I_{GATE} = 100mA		2		Ω
	I_{GATE} = –100mA		2		Ω
Foldback Current Limit					
Clamp Level	Measured at Voltage EA Output; V_{SENSE} = $V_{COMMAND}$ = 3V		4.28		V
	$V_{COMMAND}$ = 3V, V_{SENSE} = 0		3.64		V

Note 1: This percentage is measured with respect to the ideal COMMAND voltage programmed by the D0 - D4 pins.

PIN DESCRIPTIONS

CAM (Current Amplifier Inverting Input): The average load current feedback from ISOUT is applied through a resistor to this pin. The current loop compensation network is also connected to this pin (see CAO/ENBL below).

CAO/ENBL (Current Amplifier Output/Chip Enable): The current loop compensation network is connected between this pin and CAM. The voltage on this pin is the input to the PWM comparator and regulates the output voltage of the system. The GATE output is disabled (held low) unless the voltage on this pin exceeds 1V, allowing the PWM to force zero duty cycle when necessary. The PWM forces maximum duty cycle when the voltage on CAO/ENBL exceeds the oscillator peak voltage (3V). A 3.2V clamp circuit prevents the CAO/ENBL voltage from rising excessively past the oscillator peak voltage for excellent transient response. The user can force this pin below 0.8V externally with an open collector, disabling the GATE drive.

COMMAND (Digital-to-Analog Converter Output Voltage): This pin is the output of the 5-bit digital-to-analog converter (DAC) and the noninverting input of the voltage amplifier. The voltage on this pin sets the switching regulator output voltage. This voltage ranges from 1.8V to 3.5V as programmed by the 5-bit DAC. The GATE output is disabled when all 1s or illegal codes are presented at the 5 Bit DAC. The COMMAND source impedance is typically 1.2kΩ and must therefore drive only high impedance inputs if accuracy is to be maintained. Bypass COMMAND with a 0.01µF, low ESR, low ESL capacitor for best circuit noise immunity.

COMP (Voltage Amplifier Output): The system voltage compensation network is applied between COMP and VFB.

D0 - D4 (DAC Digital Input Control Codes): These are the DAC digital input control codes, with D0 representing the least significant bit (LSB) and D4, the most significant bit (MSB). A bit is set low by being connected to GND. A bit is set high by floating it, or connecting it to a 5V source. Each control pin is pulled up to approximately 5V by an internal 70µA current source.

GATE (PWM Output, MOSFET Driver): This output provides a 2Ω totem pole driver. Use a series resistor between this pin and the gate of the external MOSFET to prevent excessive overshoot.

GND (Signal Ground): All voltages are measured with respect to GND. Bypass capacitors on the VCC and VREF pins should be connected directly to the ground plane near the GND pin.

IS– (Current Sense Amplifier Inverting Input): This pin is the inverting input to the current sense amplifier and is connected to the low side of the average current sense resistor.

IS+ (Current Sense Amplifier Noninverting Input): This pin is the noninverting input to the current sense amplifier and is connected to the high side of the average current sense resistor.

ISOUT (Current Sense Amplifier Output): This pin is the output of the current sense amplifier. The voltage on this pin is (COMMAND + G_{CSA} • I • R_{SENSE}), where COMMAND is the voltage on the COMMAND pin, G_{CSA} is the fixed gain of the current sense amplifier, equal to 16, I is the current through the sense resistor, and R_{SENSE} is the value of the average current sensing resistor.

PIN DESCRIPTIONS (cont.)

PGND (Power Ground): This pin provides a dedicated ground for the output gate driver. The GND and PGND pins should be connected externally using a short printed circuit board trace close to the IC. Decouple VIN to PGND with a low ESR capacitor ≥ 0.10µF.

PWRGOOD (Undervoltage/Lower Overvoltage Output): This pin is an open drain output which is driven low to reset the microprocessor when VSENSE rises above or falls below its nominal value by 7.5%. The on resistance of the open drain switch will be no higher than 470Ω. The OV and UV comparators' hysteresis is fixed at 20mV independent of the COMMAND voltage.

VIN (Positive Supply Voltage): This pin supplies power to the chip. Connect VIN to a stable voltage source of at least 10.8V. The GATE and PWRGOOD outputs will be held low until VCC exceeds the upper undervoltage lockout threshold. This pin should be bypassed directly to the GND pin.

VFB (Voltage Amplifier Inverting Input): This input is connected to COMP through a feedback network and to the power supply output through a resistor or a divider network.

VREF (Voltage Reference Output): This pin provides an accurate 5V reference and is internally short circuit current limited. VREF powers the D/A converter and also provides a threshold voltage for the UVLO comparator. For best reference stability, bypass VREF directly to GND with a low ESR, low ESL capacitor of at least 0.01µF.

VSENSE (Output Voltage Sensing Input): This pin is connected to the system output voltage through a low pass filter. When the voltage on VSENSE rises above or falls below the COMMAND voltage by 7.5%, the PWRGOOD output is driven low to reset the microprocessor. When the voltage on VSENSE rises above the COMMAND voltage by 17.5%, the OVP comparator pulls the current amplifier output voltage below the oscillator valley voltage to force zero duty cycle at the GATE output. This pin is also used by the foldback current limiting circuitry.

APPLICATION INFORMATION

Short Circuit Current Limit

The short circuit current limit, I_{SC}, is set according to:

$$I_{SC} = \frac{1.28V}{R_{SENSE} \bullet G_{CSA}}$$

where R_{SENSE} is the average current sense resistor and G_{CSA} is the current sense amplifier gain. G_{CSA} equals 20.

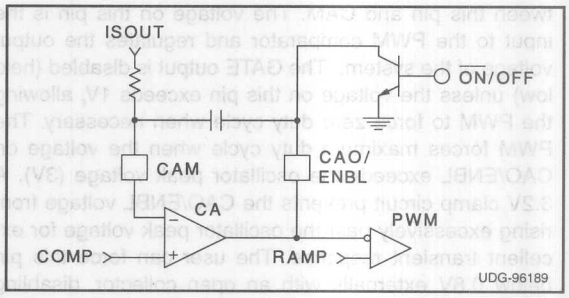
Example: Choose R_{SENSE} to set the short circuit limit at 16A using the UCC3830-5

$$R_{SENSE} = \frac{1.28V}{16A \bullet 16} = 0.005\Omega.$$

A lower resistance value may be needed if the AC ripple current in the inductor is more than 20% of the load current.

Enabling/Disabling the UCC3830-x Gate Drive

The CAO/ENBL pin can be used to disable the UCC3830 gate drive by forcing this pin below 0.8V, as shown. Bringing the voltage below the valley of the PWM oscillator ramp will insure a 0% duty cycle, effectively disabling the gate drive. A low noise open collector signal should be used as an Enable/Disable command.



Operating the 5-Bit Controller with Intel's 4-Bit Pentium Pro

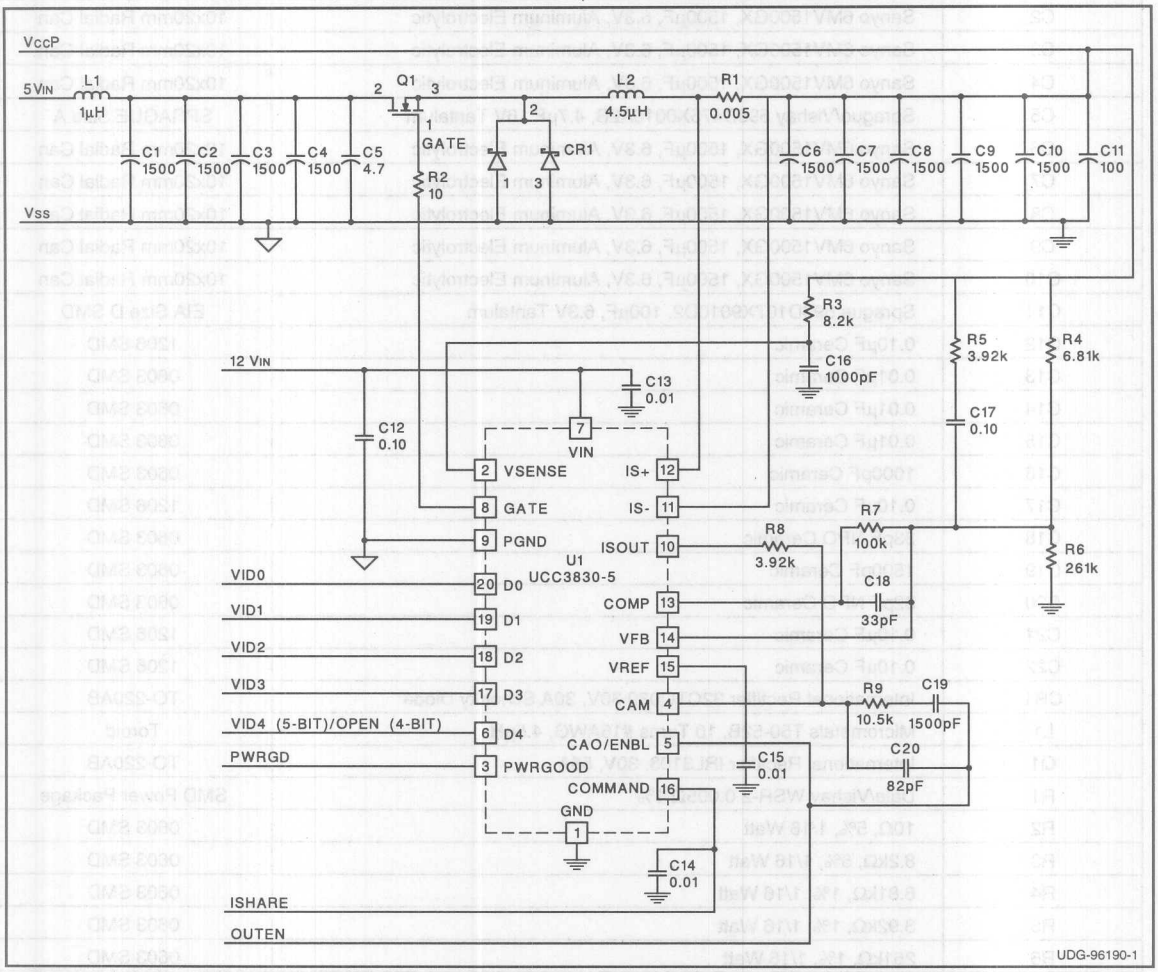
The UCC3830-x 5-Bit Controller is completely backward compatible. When the fifth bit, D4 is left open (4-Bit Processor in circuit), the UCC3830-x acts as a 4-Bit controller with the COMMAND voltage fully compatible with Intel's 4-Bit Pentium® Pro family.

Related Publications

U-156 and U-157 are Unitrode Application Notes describing the operation of the UC3886 and the UC3886/UC3910 together in a Pentium® Pro application.

TYPICAL APPLICATION

The UCC3830-x is ideal for converting the 5.0V system bus into the required Pentium® Pro bus voltage. The 3.3V system bus can also be converted using the UCC3830-x when the Pentium® Pro requires lower bus voltages.



UCC3830 Configured for 4-Bit or 5-Bit Operation

PARTS LIST

REF.	DESCRIPTION	PACKAGE
U1	Unitrode UCC3830DWP-5 DAC/PWM	SOIC-20 Wide
C1	Sanyo 6MV1500GX, 1500µF, 6.3V, Aluminum Electrolytic	10x20mm Radial Can
C2	Sanyo 6MV1500GX, 1500µF, 6.3V, Aluminum Electrolytic	10x20mm Radial Can
C3	Sanyo 6MV1500GX, 1500µF, 6.3V, Aluminum Electrolytic	10x20mm Radial Can
C4	Sanyo 6MV1500GX, 1500µF, 6.3V, Aluminum Electrolytic	10x20mm Radial Can
C5	Sprague/Vishay 595D475X0016A2B, 4.7µF 16V Tantalum	SPRAGUE Size A
C6	Sanyo 6MV1500GX, 1500µF, 6.3V, Aluminum Electrolytic	10x20mm Radial Can
C7	Sanyo 6MV1500GX, 1500µF, 6.3V, Aluminum Electrolytic	10x20mm Radial Can
C8	Sanyo 6MV1500GX, 1500µF, 6.3V, Aluminum Electrolytic	10x20mm Radial Can
C9	Sanyo 6MV1500GX, 1500µF, 6.3V, Aluminum Electrolytic	10x20mm Radial Can
C10	Sanyo 6MV1500GX, 1500µF, 6.3V, Aluminum Electrolytic	10x20mm Radial Can
C11	Sprague 593D107X9010D2, 100µF, 6.3V Tantalum	EIA Size D SMD
C12	0.10µF Ceramic	1206 SMD
C13	0.01µF Ceramic	0603 SMD
C14	0.01µF Ceramic	0603 SMD
C15	0.01µF Ceramic	0603 SMD
C16	1000pF Ceramic	0603 SMD
C17	0.10µF Ceramic	1206 SMD
C18	33pF NPO Ceramic	0603 SMD
C19	1500pF Ceramic	0603 SMD
C20	82pF NPO Ceramic	0603 SMD
C21	0.10µF Ceramic	1206 SMD
C22	0.10µF Ceramic	1206 SMD
CR1	International Rectifier 32CTQ030 30V, 30A Schottky Diode	TO-220AB
L1	Micrometals T50-52B, 10 Turns #16AWG, 4.5µH	Toroid
Q1	International Rectifier IRL3103, 30V, 56A	TO-220AB
R1	Dale/Vishay WSR-2 0.005Ω 1%	SMD Power Package
R2	10Ω, 5%, 1/16 Watt	0603 SMD
R3	8.2kΩ, 5%, 1/16 Watt	0603 SMD
R4	6.81kΩ, 1%, 1/16 Watt	0603 SMD
R5	3.92kΩ, 1%, 1/16 Watt	0603 SMD
R6	261kΩ, 1%, 1/16 Watt	0603 SMD
R7	100kΩ, 1%, 1/16 Watt	0603 SMD
R8	3.92kΩ, 1%, 1/16 Watt	0603 SMD
R9	10.5kΩ, 1%, 1/16 Watt	0603 SMD
Q1-HS	AAVID 576802 TO-220 Heat Sink	TO-220AB
CR1-HS	AAVID 577002 TO-220 Heat Sink	TO-220AB

Pentium® Pro is a registered trademark of Intel Corporation.

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UNITRODE

UC1838A
UC2838A
UC3838A

Magnetic Amplifier Controller

FEATURES

- Independent 1% Reference
- Two Uncommitted, Identical Operational Amplifiers
- 100mA Reset Current Source with -120V Capability
- 5V to 40V Analog Operation
- 5W DIL Package

DESCRIPTION

The UC1838A family of magnetic amplifier controllers contains the circuitry to generate and amplify a low-level analog error signal along with a high voltage-compliant current source. This source will provide the reset current necessary to enable a magnetic amplifier to regulate and control a power supply output in the range of 2A to 20A.

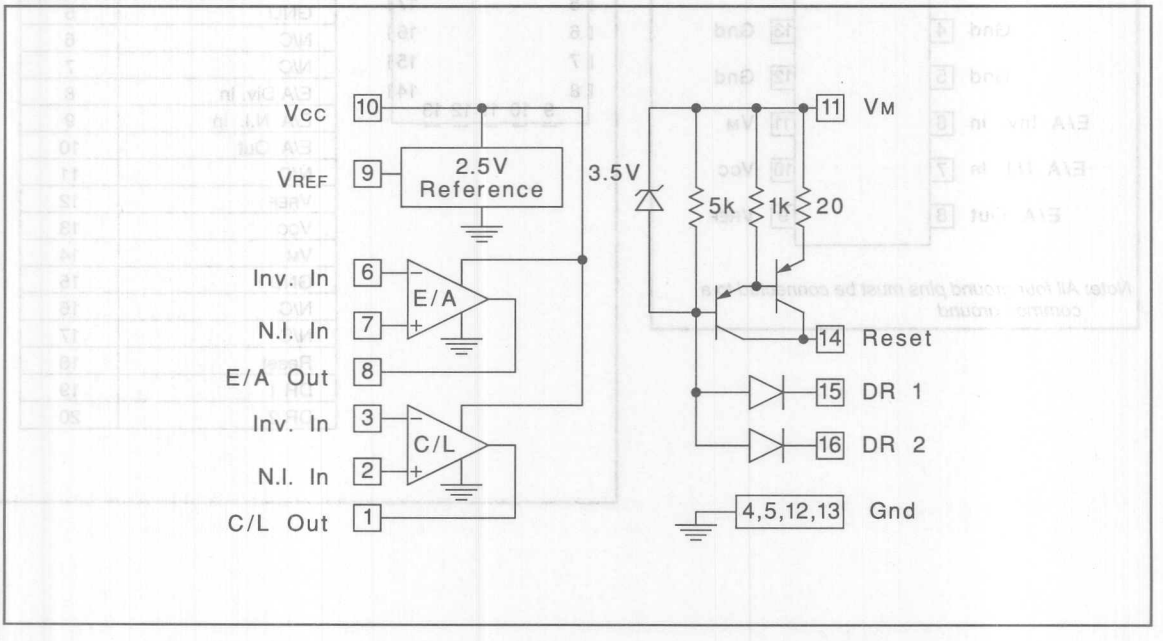
By controlling the reset current to a magnetic amplifier, this device will define the amount of volt-seconds the magnetic amplifier will block before switching to the conducting state. Magnetic amplifiers are ideal for post-regulators for multiple-output power supplies where each output can be independently controlled with efficiencies up to 99%. With a square or pulse-width-modulated input voltage, a magnetic amplifier will block a portion of this input waveform, allowing just enough to pass to provide a regulated output. With the UC1838A, only the magnetic amplifier coil, three diodes, and an output L-C filter are necessary to implement a complete closed-loop regulator.

The UC1838A contains a precision 2.5V reference, two uncommitted high-gain op amps and a high-gain PNP-equivalent current source which can deliver up to 100mA of magnetic amplifier reset current and with -120 volt capability.

These devices are available in a plastic "bat-wing" DIP for operation over a -20°C to +85°C temperature range and, with reduced power, in a hermetically sealed cerdip for -55°C to +125°C operation. Surface mount versions are also available.

This improved "A" version replaced the non "A" version formerly introduced.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

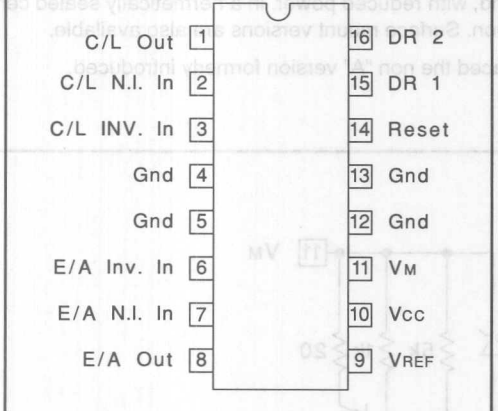
Supply Voltage, V_{CC} 40V
Magnetic Amp. Source Voltage, V_M 40V
Reset Output Voltage, V_R . . . . . -120V
Total Current Source Voltage, V_M - V_R . . . . . -140V
Amplifier Input Range . . . . . -0.3V to V_{CC}
Reset Input Current, I_{DR} . . . . . -10mA

	Q, N Package	J Package
Power Dissipation at T_A = 25°C	2W	1W
Power Dissipation at T (leads/case) = 25°C	5W	2W
Operating Temperature Range	-55°C to +125°C	
Storage Temperature Range	-65°C to +150°C	
Lead Temperature (Soldering, 10 sec)	300°C	

Note: All voltages are with respect to ground pins.
All currents are positive into the specified terminal.
Consult Packaging section of Databook for thermal limitations and considerations of package.

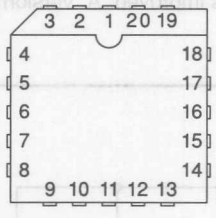
CONNECTION DIAGRAMS

DIL-16 (TOP VIEW)
J or N Package



Note: All four ground pins must be connected to a common ground

PLCC-20, LCC-20 (TOP VIEW)
Q, L Packages



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
C/L Out	2
C/L N.I. In	3
C/L Inv. In	4
GND	5
N/C	6
N/C	7
E/A Div. In	8
E/A N.I. In	9
E/A Out	10
N/C	11
V_{REF}	12
V_{CC}	13
V_M	14
GND	15
N/C	16
N/C	17
Reset	18
DR 1	19
DR 2	20

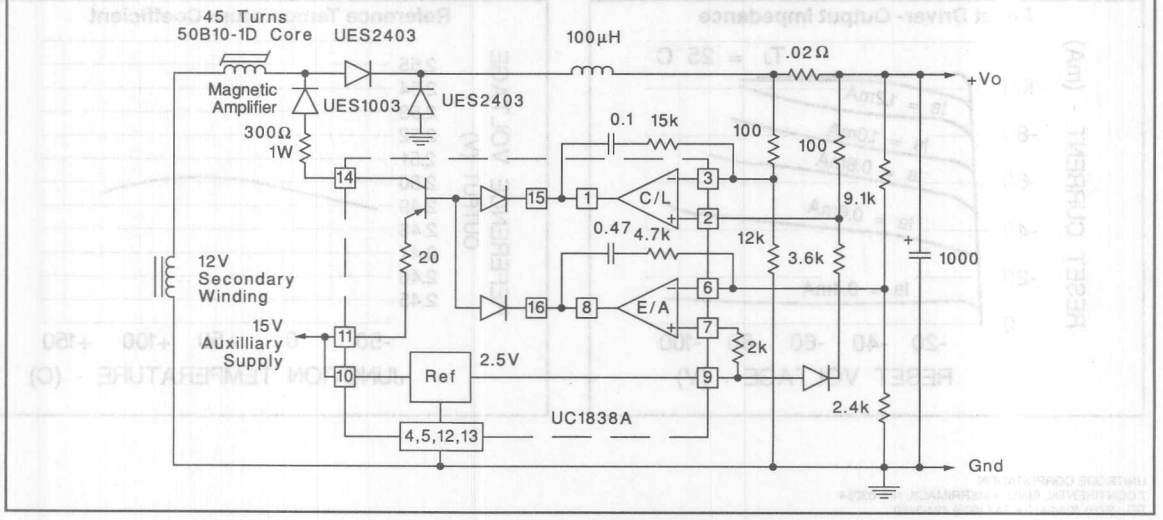
ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1838A, -20°C to +85°C for the UC2838A, and 0°C to +70°C for the UC3838A, V_{CC} = 20V, V_M = 5V, T_A = T_J.

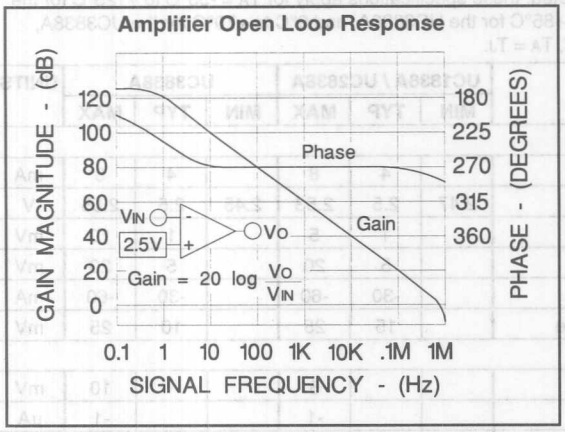
PARAMETER	TEST CONDITIONS	UC1838A / UC2838A			UC3838A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Reference Section								
Supply Current	V_{CC} = V_M = 40V		4	8		4	8	mA
Reference Output	T_A = 25°C	2.47	2.5	2.53	2.45	2.5	2.55	V
Line Regulation	V_{CC} = 5 to 30V		1	5		1	10	mV
Load Regulation	I_O = 0 to -2mA		5	20		5	20	mV
Short Circuit Current	V_{REF} = 0V		-30	-60		-30	-60	mA
Temperature Stability*	Over Operating Temp. Range		15	25		10	25	mV
Amplifier Section (Each Amplifier)								
Offset Voltage	V_{CM} = 2.5V			5			10	mV
Input Bias Current	V_{IN} = 0V			-1			-1	µA
Input Offset Current				100			100	nA
Minimum Output Swing		0.4		18	0.4		18	V
Output Sink Current	V_O = 5V	1	10	30	1	10	30	mA
Output Source Current	V_O = 0V	-1	-10	-20	-1	-10	-20	mA
A_{VOL}	V_O = 1 to 11V	100	120		100	120		dB
CMRR	V_{IN} = 1 to 11V	70	80		70	80		dB
PSRR	V_{CC} = 10 to 20V	70	100		70	100		dB
Gain Bandwidth*		0.6	0.8		0.6	0.8		MHz
Reset Drive Section								
Input Leakage	V_{DR} = 40V			10			10	µA
Output Leakage	V_R = -120V			-100			-100	µA
Input Current	I_R = -50mA		-1	-2		-1	-2	mA
Maximum Reset Current	I_{DR} = -3mA	-100	-120	-200	-100	-120	-200	mA
Transconductance	I_R = -10 to -50mA	.03	.042	.055	.03	.042	.055	A/V

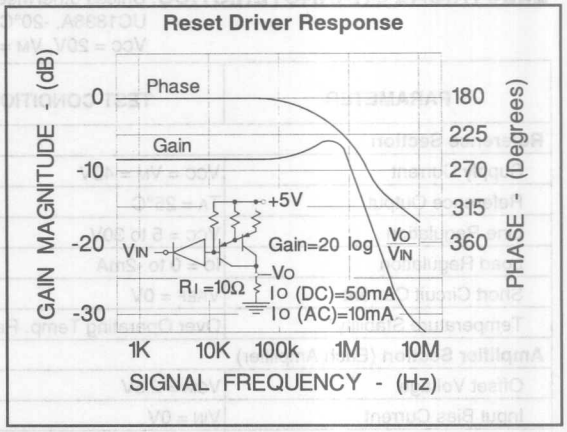
** These parameters are guaranteed by design but not 100% tested in production.*

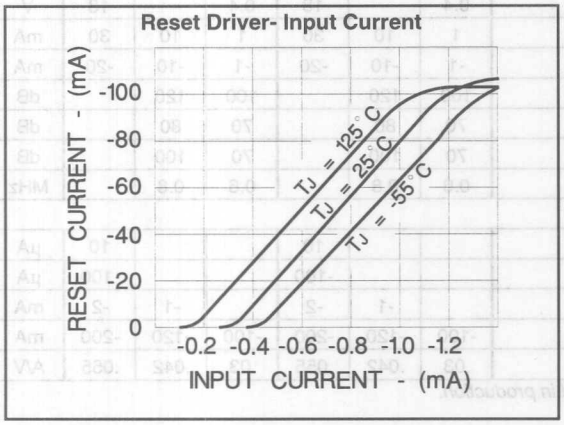
TYPICAL APPLICATION

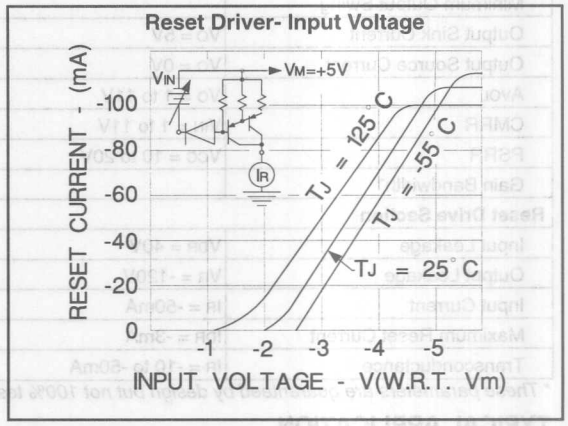
+12V, 4A Output With Switching Frequency = 50 kHz

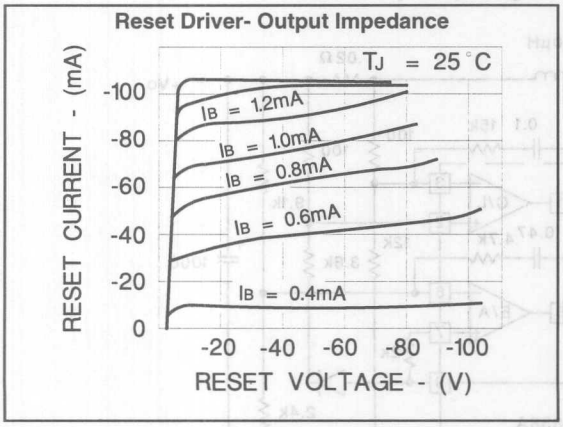


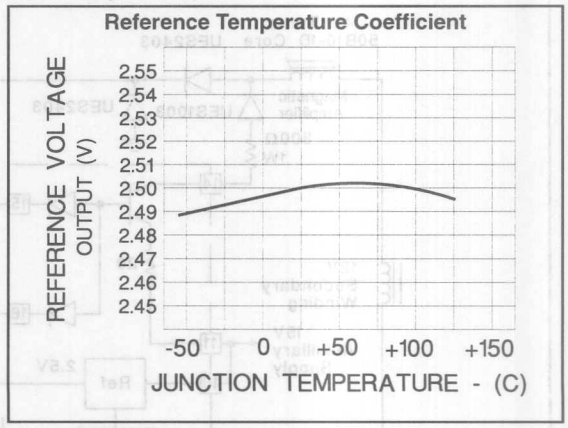












UNITRODE CORPORATION
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Secondary Side Average Current Mode Controller

FEATURES

- Practical Secondary Side Control of Isolated Power Supplies
- Provides a Self Regulating Bias Supply From a High Input Voltage Using an External N-Channel Depletion Mode FET
- Onboard Precision, Fixed Gain, Differential Current Sense Amplifier
- Wide Bandwidth Current Error Amplifier
- 5V Reference
- High Current, Programmable Gm Amplifier Optimized to Drive Opto-couplers

DESCRIPTION

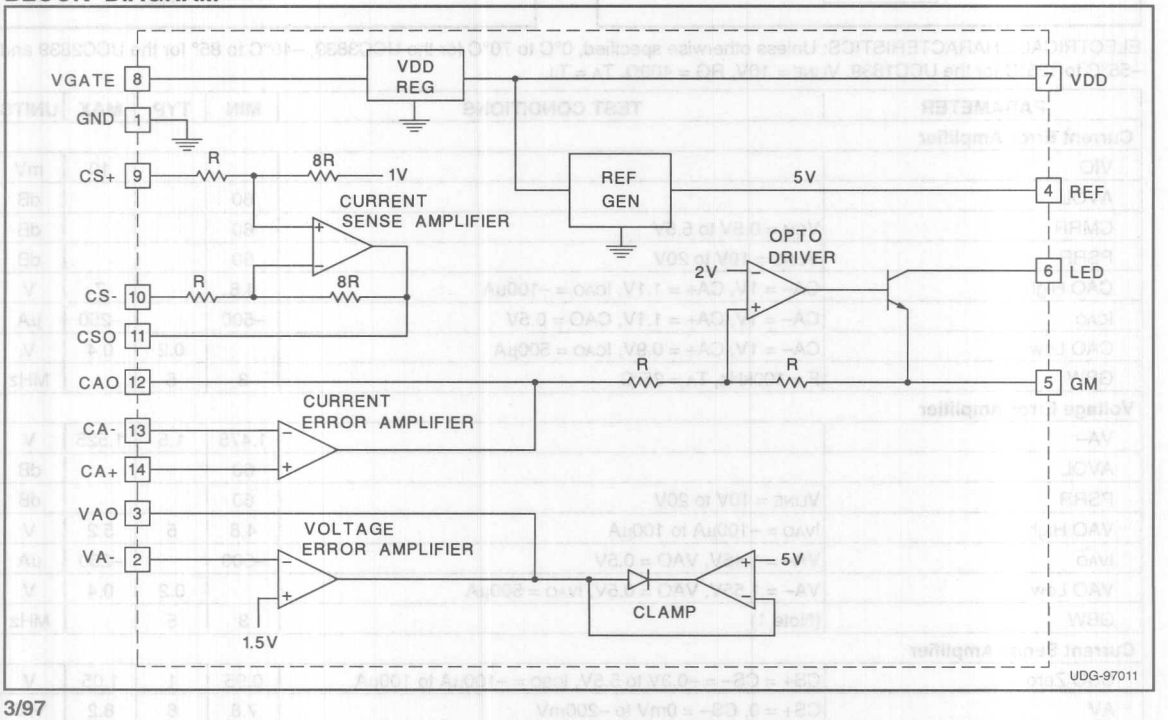
The UCC3839 provides the control functions for secondary side average current mode control in isolated power supplies. Start up, pulse width modulation and MOSFET drive must be accomplished independently on the primary side. Communication from secondary to primary side is anticipated through an opto-isolator.

Accordingly, the UCC3839 contains a fixed gain current sense amplifier, voltage and current error amplifiers, and a Gm type buffer/driver amplifier for the opto-isolator. Additional housekeeping functions include a precision 5V reference and a bias supply regulator.

Power for the UCC3839 can be generated by peak rectifying the voltage of the secondary winding of the isolation transformer. From this unregulated voltage, the UCC3839's bias supply regulator will generate its own 7.5V bias supply using an external, N-channel, depletion mode FET.

The UCC3839 can be configured for traditional average current mode control where the output of the voltage error amplifier commands the current error amplifier. It can also be configured for output voltage regulation with average current mode short circuit current limiting, employing two parallel control loops regulating the output voltage and output current independently.

BLOCK DIAGRAM



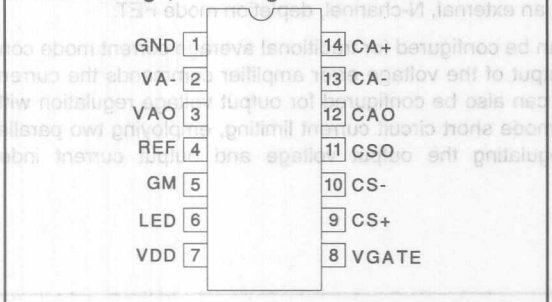
ABSOLUTE MAXIMUM RATINGS

Supply Voltage 15V
Supply Current
(LED not connected) 2mA
(LED connected) 14mA
Analog Inputs . . . . . –0.3V to 15V
Power Dissipation at T_A = 60°C
(LED not connected) 20mW
(LED connected) 55mW
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10sec.) . . . . . +300°C

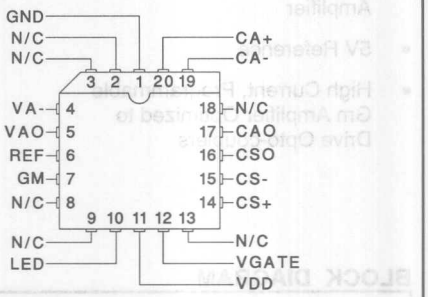
Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of package.

CONNECTION DIAGRAM

DIL-14, SOIC-14 (Top View)
J or N Package, D Package



PLCC-20 (Top View)
Q Packages



ELECTRICAL CHARACTERISTICS: Unless otherwise specified, 0°C to 70°C for the UCC3839, –40°C to 85° for the UCC2839 and –55°C to 125°C for the UCC1839. V_{LINE} = 10V, RG = 400Ω, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Current Error Amplifier					
VIO				10	mV
AVOL		60			dB
CMRR	V_{CM} = 0.5V to 5.5V	60			dB
PSRR	V_{LINE} = 10V to 20V	60			dB
CAO High	CA– = 1V, CA+ = 1.1V, I_{CAO} = –100uA	4.8		7	V
I_{CAO}	CA– = 1V, CA+ = 1.1V, CAO = 0.5V	–500		–250	µA
CAO Low	CA– = 1V, CA+ = 0.9V, I_{CAO} = 500µA		0.2	0.4	V
GBW	F = 100kHz, T_A = 25°C	3	5		MHz
Voltage Error Amplifier					
VA–		1.475	1.5	1.525	V
AVOL		60			dB
PSRR	V_{LINE} = 10V to 20V	60			dB
VAO High	I_{VAO} = –100µA to 100µA	4.8	5	5.2	V
I_{VAO}	VA– = 1.45V, VAO = 0.5V	–500		–250	µA
VAO Low	VA– = 1.55V, VAO = 0.5V, I_{VAO} = 500µA		0.2	0.4	V
GBW	(Note 1)	3	5		MHz
Current Sense Amplifier					
CSO Zero	CS+ = CS– = –0.3V to 5.5V, I_{CSO} = –100µA to 100µA	0.95	1	1.05	V
AV	CS+ = 0, CS– = 0mV to –200mV	7.8	8	8.2	V/V

ELECTRICAL CHARACTERISTICS (cont.): Unless otherwise specified, 0°C to 70°C for the UCC3839, –40°C to 85° for the UCC2839 and –55°C to 125°C for the UCC1839. V_{LINE} = 10V, RG = 400Ω. $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Current Sense Amplifier (cont.)					
Slew Rate	CS+ = 0, CS– = 0mV to –0.5V	2	4		V/µs
CSO	CS+ = –200mV, CS– = –700mV	4.8	5	5.2	V
LED Driver					
I_{LED}	LED = 5.5V, CA– = 1V, CA+ = 1.1V, RG = 400		0	10	µA
	LED = 5.5V, CA– = 1V, CA+ = 0.9V, RG = 400	9	10	11	mA
Gm	LED = 5.5V, CAO = 1V to 3V, RG = 400	2.25	2.5	2.75	mS
Slew Rate	CAO = 2V to 2.5V, LED = 400Ω to 5.5V, RG = 400	2	4		V/µs
Precision Reference					
REF	T_J = 25°C	4.95	5	5.05	V
	I_{REF} = 0mA to 1mA, V_{LINE} = 10V to 20V	4.925		5.075	V
VA+/REF		0.298	0.3	0.302	V/V
VDD Regulator					
VDD	IDD = 0mA to –15mA, V_{LINE} = 10V to 40V	7	7.5	8	V

Note 1: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

CA–: Current Error Amplifier Negative Input.

CAO: Current Error Amplifier Output. Output source current is limited, and output sink current is guaranteed to be greater than the VAO output source current. Current loop compensation components are generally connected to CAO and CA–.

CA+: Current Error Amplifier Positive Input.

CS–: Current Sense Amplifier Negative Input

CSO: Current Sense Amplifier Output. Internally set gain V_{OUT}/V_{IN} = 8 V_{IN} = 0V results in CSO = 1V.

CS+: Current Sense Amplifier Positive Input.

GM: Gm (transconductance) Programming Pin. Resistor R_{GM} = 400Ω to GND.

GND: Chip Ground.

LED: Output of LED Driver. Connect LED from VDD pin to LED.

REF: 5V Precision Reference Buffer Output. Minimum Decoupling Capacitance = 0.01µF

VA–: Voltage Error Amplifier Negative Input. Voltage Error Amplifier is internally referenced to 1.5V

VAO: Voltage Error Amplifier Output. In a two loop average current mode control configuration, VAO is connected to CA+ and is the current command signal. VAO is internally clamped not to exceed 5V for short circuit control. In a single loop voltage mode control configuration with a parallel average short circuit current control loop, VAO is connected directly to CAO. Output source current is limited, and output sink current is guaranteed to be greater than the CAO output source current.

VDD: 7.5V Regulator output. Supply for most of the chip. Minimum Decoupling Capacitance = 0.01µF

VGATE: External FET Gate Control Voltage.

APPLICATION INFORMATION

Figure 1 shows a typical secondary side average current mode controller configuration using the UCC3839. In this configuration, output voltage is sensed and regulated by the voltage error amplifier. Its output, VAO provides the reference for the current error amplifier at the CA+ pin. VAO can be connected to CA+ directly or through a resistive divider depending on the particular application requirements.

Average current mode control needs accurate output current information which is provided by a low value current sense resistor. The voltage proportional to the converter's output current is sensed and amplified by the precision current sense amplifier of the chip. The onboard current sense amplifier has a gain of 8 and is intended for differential sensing of the shunt voltage with a common mode voltage range from 0V up to 5V. The output of the current sense amplifier, CSO is 1V for zero input which guarantees that the circuit can control currents down to 0A.

APPLICATION INFORMATION (cont.)

The CSO signal is fed to the CA– input of the current error amplifier through a resistor. The current error amplifier takes the VAO and CSO signals and generates the error signal for the pulse width modulator.

Since the PWM function is located on the primary side of the power converter the CAO signal must be sent across the safety isolation boundary. The UCC3839 anticipates an opto-coupler to provide isolation between primary and secondary. Therefore, CAO drives a transconductance amplifier that controls LED current in an opto-isolator. During start up and when CAO exceeds 4V, the current in the LED drops to zero. Maximum LED current is obtained during normal operation as CAO reaches its lowest potential. Its value is determined by the programming resistor value from the GM pin to circuit GND.

An alternative secondary side controller configuration is introduced in Figure 2. In this circuit, the voltage and current control loops of the UCC3839 are connected parallel. It can be achieved by connecting the VAO and CAO pins together. The error amplifier with the lower output voltage controls the current in the opto-coupler providing the feedback signal for the PWM section on the primary side. Voltage regulation is still maintained by the voltage error amplifier until a user programmable output current is reached. At this time CAO will take control over the Gm amplifier and the output current of the converter will be regulated while the output voltage falls below its nominal value. This current level is set at the CA+ input by a resistive divider from the 5V reference of the chip.

Since the chip is powered from a peak rectifier which maintains the bias supply for the UCC3839 even under short circuit conditions, both of these techniques can be used to eliminate the short circuit runaway problem in isolated power supplies using peak current mode control on the primary side.

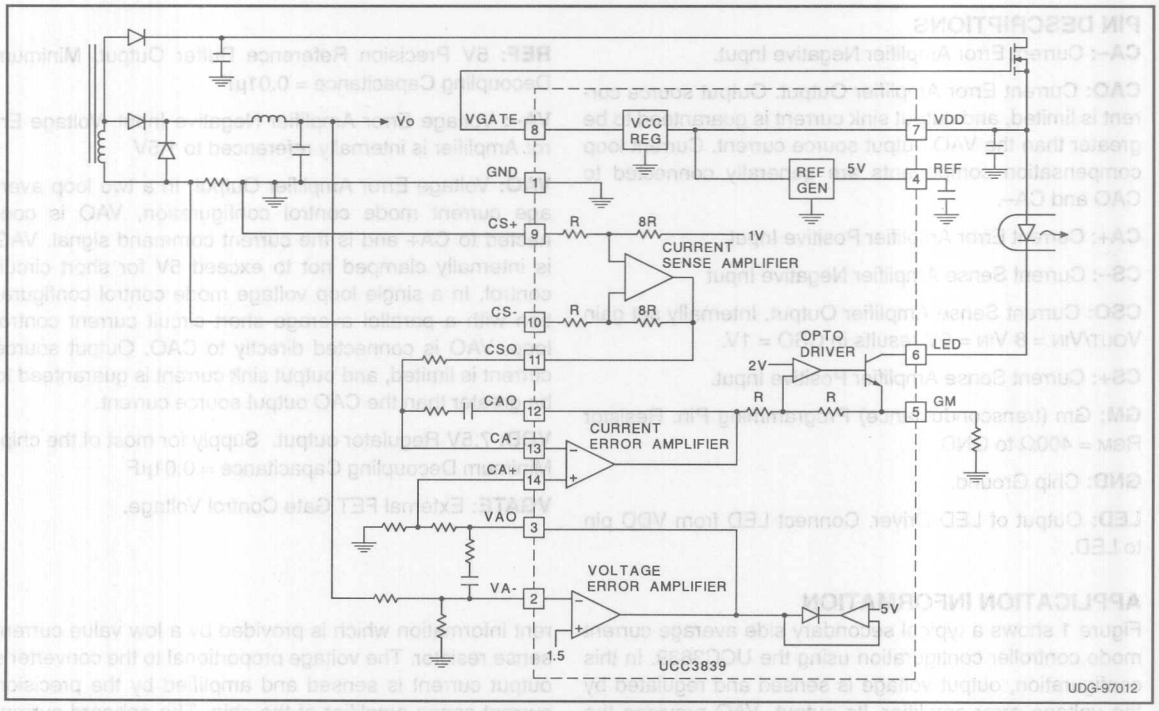


Figure 1. Secondary Side Average Current Mode Controller

APPLICATION INFORMATION (cont.)

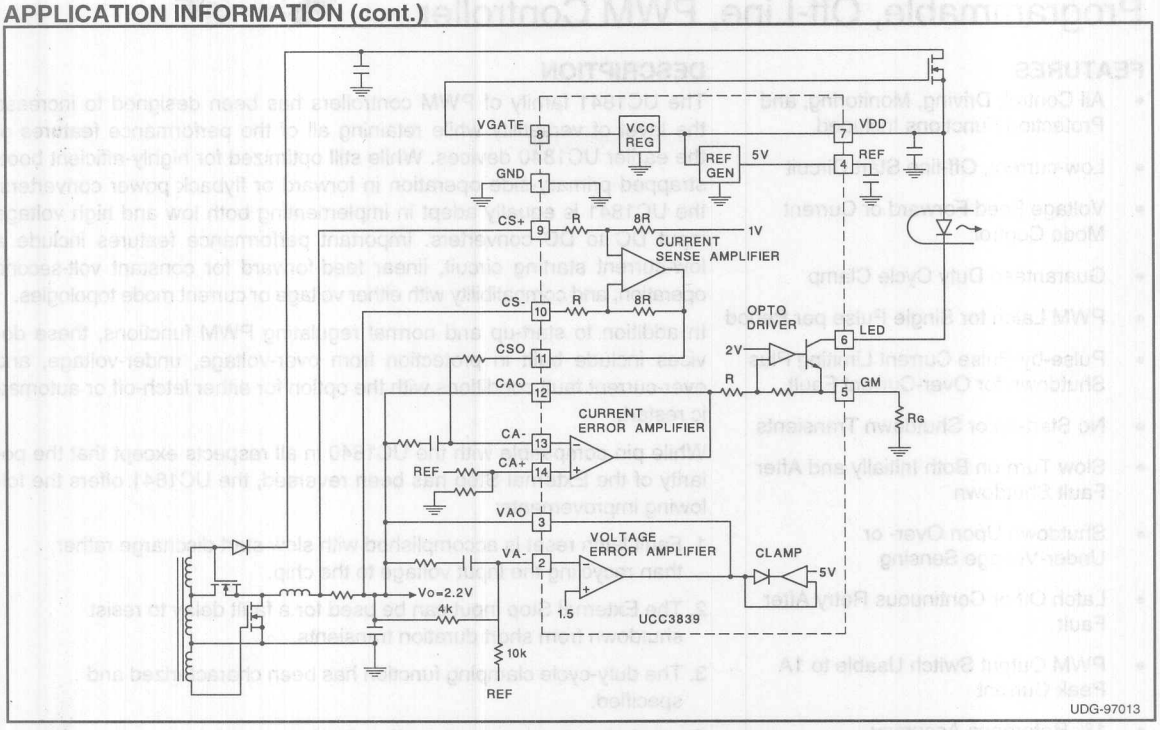


Figure 2. Voltage Mode with Average Current Short Circuit Limit

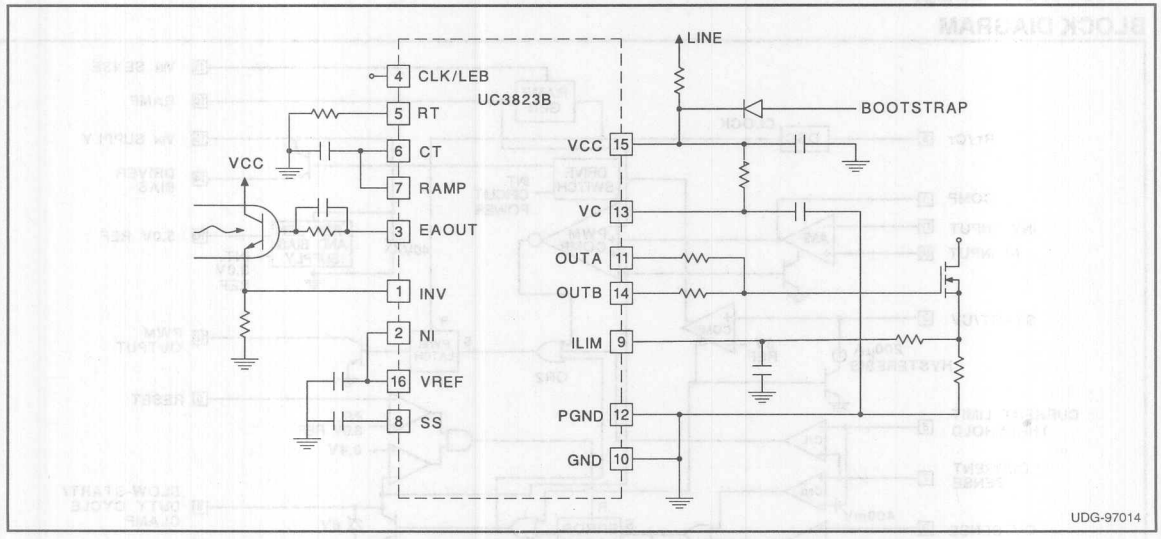


Figure 3. Typical Primary Side Circuit For Use With Secondary Side Average Current Mode Controller

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

UNITRODE

UC1841
UC2841
UC3841

Programmable, Off-Line, PWM Controller

FEATURES

- All Control, Driving, Monitoring, and Protection Functions Included
- Low-current, Off-line Start Circuit
- Voltage Feed Forward or Current Mode Control
- Guaranteed Duty Cycle Clamp
- PWM Latch for Single Pulse per Period
- Pulse-by-Pulse Current Limiting Plus Shutdown for Over-Current Fault
- No Start-up or Shutdown Transients
- Slow Turn-on Both Initially and After Fault Shutdown
- Shutdown Upon Over- or Under-Voltage Sensing
- Latch Off or Continuous Retry After Fault
- PWM Output Switch Usable to 1A Peak Current
- 1% Reference Accuracy
- 500kHz Operation
- 18 Pin DIL Package

DESCRIPTION

The UC1841 family of PWM controllers has been designed to increase the level of versatility while retaining all of the performance features of the earlier UC1840 devices. While still optimized for highly-efficient boot-strapped primary-side operation in forward or flyback power converters, the UC1841 is equally adept in implementing both low and high voltage input DC to DC converters. Important performance features include a low-current starting circuit, linear feed-forward for constant volt-second operation, and compatibility with either voltage or current mode topologies.

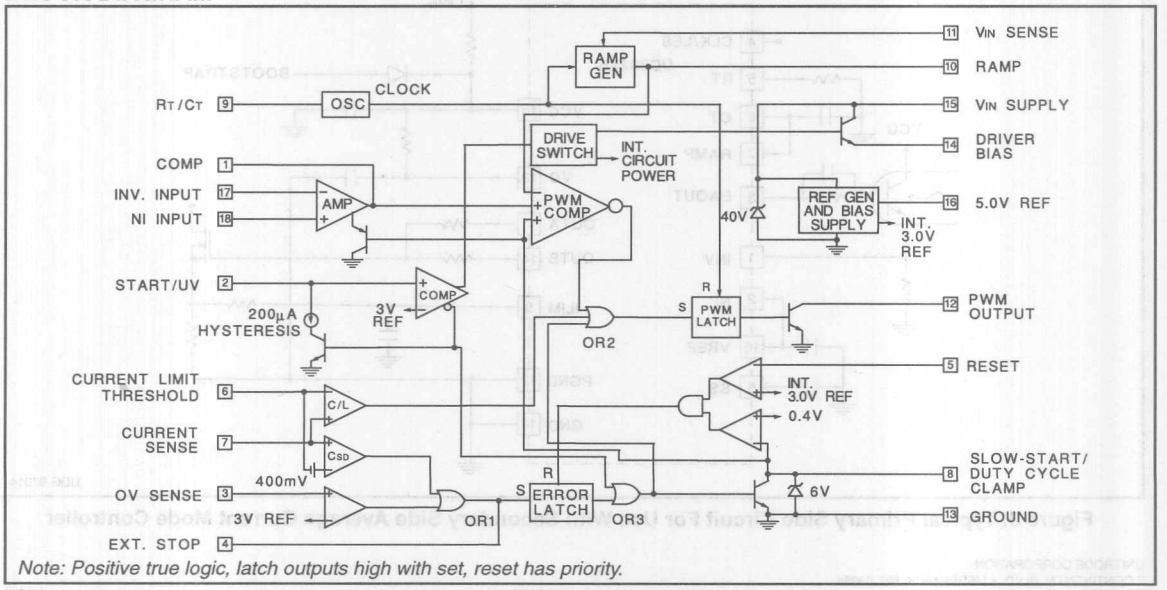
In addition to start-up and normal regulating PWM functions, these devices include built in protection from over-voltage, under-voltage, and over-current fault conditions with the option for either latch-off or automatic restart.

While pin compatible with the UC1840 in all respects except that the polarity of the External Stop has been reversed, the UC1841 offers the following improvements:

1. Fault latch reset is accomplished with slow start discharge rather than recycling the input voltage to the chip.
2. The External Stop input can be used for a fault delay to resist shutdown from short duration transients.
3. The duty-cycle clamping function has been characterized and specified.

The UC1841 is characterized for -55°C to +125°C operation while the UC2841 and UC3841 are designed for -25°C to +85°C and 0°to +70°C, respectively.

BLOCK DIAGRAM



Note: Positive true logic, latch outputs high with set, reset has priority.

6/93

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, +V_{IN} (Pin 15) (Note 2)
- Voltage Driven . . . . . +32V
- Current Driven, 100mA maximum . . . . . Self-limiting

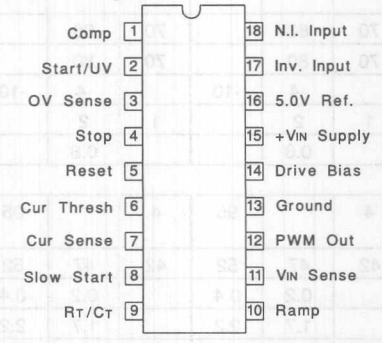
PWM Output Voltage (Pin 12) 40V
PWM Output Current, Steady-State (Pin 12) 400mA
PWM Output Peak Energy Discharge 20µJoules
Driver Bias Current (Pin 14) . . . . . -200mA
Reference Output Current (Pin 16) . . . . . -50mA
Slow-Start Sink Current (Pin 8) 20mA
V_{IN} Sense Current (Pin 11) 10mA
Current Limit Inputs (Pins 6 & 7) . . . . . -0.5 to +5.5V
Stop Input (Pin 4) . . . . . -0.3 to +5.5V
Comparator Inputs
(Pins 1, 7, 9-11, 16) . . . . . Internally clamped at 12V
Power Dissipation at T_A = 25°C (Note 3) 1000mW
Power Dissipation at T_C = 25°C (Note 3) 2000mW

Operating Junction Temperature . . . . . -55°C to +150°C
Storage Temperature Range . . . . . -65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . +300°C

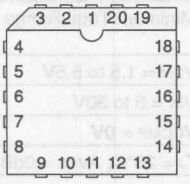
Note 1: All voltages are with respect to ground, Pin 13. Currents are positive-into, negative-out of the specified terminal.
Note 2: All pin numbers are referenced to DIL-18 package.
Note 3: Consult Packaging Section of Databook for thermal limitations and considerations of package.

CONNECTION DIAGRAMS

DIL-18, SOIC-18 (TOP VIEW)
J or N, DW Package



PLCC-20, LCC-20
(TOP VIEW)
Q or L Package



PACKAGE PIN FUNCTIONS	
FUNCTION	PIN
Comp	1
Start/UV	2
OV Sense	3
Stop	4
Reset	5
CUR Thresh	7
CUR Sense	8
Slow Start	9
RT/CT	10
Ramp	11
VIN Sense	12
PWM Out	13
Ground	14
Drive Bias	15
+VIN Supply	17
5.0V REF	18
Inv. Input	19
N.I. Input	20

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1841, -25°C to +85°C for the UC2841, and 0°C to +70°C for the UC3841; V_{IN} = 20V, R_T = 20kΩ, C_T = .001mfd, R_R = 10kΩ, C_R = .001mfd, Current Limit Threshold = 200mV, T_A = T_J.

PARAMETER	TEST CONDITIONS	UC1841 / UC2841			UC3841			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Power Inputs								
Start-Up Current	V_{IN} = 30V, Pin 2 = 2.5V		4.5	6		4.5	6	mA
Operating Current	V_{IN} = 30V, Pin 2 = 3.5V		10	14		10	14	mA
Supply OV Clamp	I_{IN} = 20mA	33	40	45	33	40	45	V
Reference Section								
Reference Voltage	T_J = 25°C	4.95	5.0	5.05	4.9	5.0	5.1	V
Line Regulation	V_{IN} = 8 to 30V		10	15		10	20	mV
Load Regulation	I_L = 0 to 10mA		10	20		10	30	mV
Temperature Stability	Over Operating Temperature Range	4.9		5.1	4.85		5.15	V
Short Circuit Current	V_{REF} = 0, T_J = 25°C		-80	-100		-80	-100	mA
Oscillator								
Nominal Frequency	T_J = 25°C	47	50	53	45	50	55	kHz
Voltage Stability	V_{IN} = 8 to 30V		0.5	1		0.5	1	%
Temperature Stability	Over Operating Temperature Range	45		55	43		57	kHz
Maximum Frequency	R_T = 2kΩ, C_T = 330pF	500			500			kHz

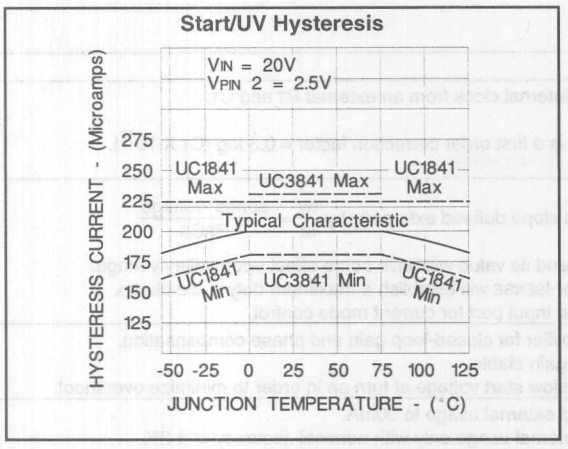
ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1841, -25°C to +85°C for the UC2841, and 0°C to +70°C for the UC3841; V_{IN} = 20V, R_T = 20kΩ, C_T = .001mfd, R_R = 10kΩ, C_R = .001mfd, Current Limit Threshold = 200mV, T_A = T_J.

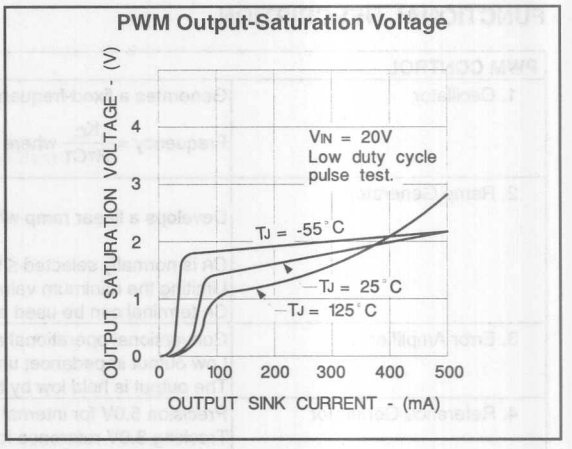
PARAMETER	TEST CONDITIONS	UC1841 / UC2841			UC3841			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Ramp Generator								
Ramp Current, Minimum	I_{SENSE} = -10µA		-11	-14		-11	-14	µA
Ramp Current, Maximum	I_{SENSE} = 1.0mA	-0.9	-.95		-0.9	-.95		mA
Ramp Valley		0.3	0.4	0.6	0.3	0.4	0.6	V
Ramp Peak	Clamping Level	3.9	4.2	4.5	3.9	4.2	4.5	V
Error Amplifier								
Input Offset Voltage	V_{CM} = 5.0V		0.5	5		2	10	mV
Input Bias Current			0.5	2		1	5	µA
Input Offset Current				0.5			0.5	µA
Open Loop Gain	ΔV_O= 1 to 3V	60	66		60	66		dB
Output Swing (Max. Output ≤ Ramp Peak - 100mV)	Minimum Total Range	0.3		3.5	0.3		3.5	V
CMRR	V_{CM} = 1.5 to 5.5V	70	80		70	80		dB
PSRR	V_{IN} = 8 to 30V	70	80		70	80		dB
Short Circuit Current	V_{COMP} = 0V		-4	-10		-4	-10	mA
Gain Bandwidth*	T_J = 25°C, A_{VOL} = 0dB	1	2		1	2		MHz
Slew Rate*	T_J = 25°C, A_{VCL} = 0dB		0.8			0.8		V/µs
PWM Section								
Continuous Duty Cycle Range* (other than zero)	Minimum Total Continuous Range, Ramp Peak < 4.2V	4		95	4		95	%
50% Duty Cycle Clamp	R_{SENSE} to V_{REF} = 10k	42	47	52	42	47	52	%
Output Saturation	I_{OUT} = 20mA		0.2	0.4		0.2	0.4	V
	I_{OUT} = 200mA		1.7	2.2		1.7	2.2	V
Output Leakage	V_{OUT} = 40V		0.1	10		0.1	10	µA
Comparator Delay*	Pin 8 to Pin 12, T_J = 25°C, R_L = 1kΩ		300	500		300	500	ns
Sequencing Functions								
Comparator Thresholds	Pins 2, 3, 5	2.8	3.0	3.2	2.8	3.0	3.2	V
Input Bias Current	Pins 3, 5 = 0V		-1.0	-4.0		-1.0	-4.0	µA
Input Leakage	Pins 3, 5 = 10V		0.1	2.0		0.1	2.0	µA
Start/UV Hysteresis Current	Pin 2 = 2.5V	170	200	220	170	200	230	µA
Ext. Stop Threshold	Pin 4	0.8	1.6	2.4	0.8	1.6	2.4	V
Error Latch Activate Current	Pin 4 = 0V, Pin 3 > 3V		-120	-200		-120	-200	µA
Driver Bias Saturation Voltage, V_{IN} - V_{OH}	I_B = -50mA		2	3		2	3	V
Driver Bias Leakage	V_B = 0V		-0.1	-10		-0.1	-10	µA
Slow-Start Saturation	I_S = 10mA		0.2	0.5		0.2	0.5	V
Slow-Start Leakage	V_S = 4.5V		0.1	2.0		0.1	2.0	µA
Current Control								
Current Limit Offset			0	5		0	10	mV
Current Shutdown Offset		370	400	430	360	400	440	mV
Input Bias Current	Pin 7 = 0V		-2	-5		-2	-5	µA
Common Mode Range*		-0.4		3.0	-0.4		3.0	V
Current Limit Delay*	T_J = 25°C, Pin 7 to 12, R_L = 1k		200	400		200	400	ns

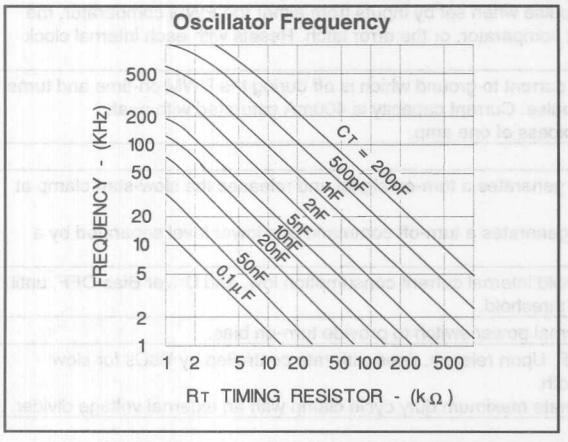
** These parameters are guaranteed by design but not 100% tested in production.*

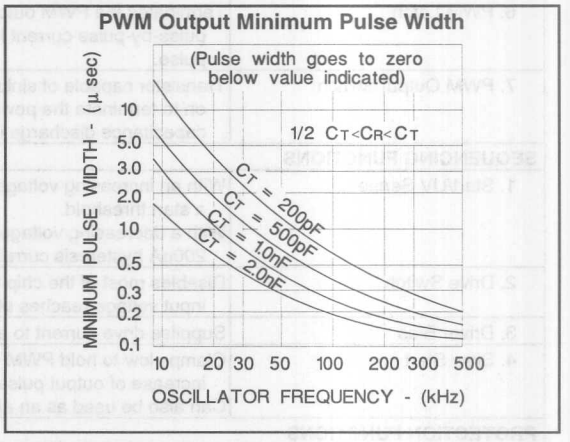
FUNCTIONAL DESCRIPTION

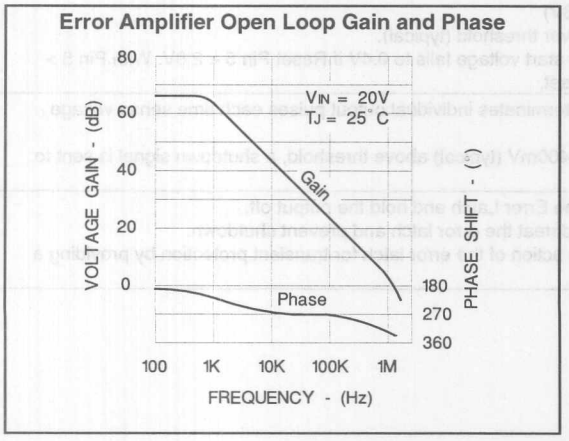
PWM CONTROL	
1. Oscillator	Generates a fixed-frequency internal clock from an external R_T and C_T. Frequency = $\frac{K_C}{R_T C_T}$ where K_C is a first order correction factor $\approx 0.3 \log (C_T \times 10^{12})$.
2. Ramp Generator	Develops a linear ramp with a slope defined externally by $\frac{dv}{dt} = \frac{\text{sense voltage}}{R_R C_R}$ C_R is normally selected $\leq C_T$ and its value will have some effect upon valley voltage. Limiting the minimum value for I_{SENSE} will establish a maximum duty cycle clamp. C_R terminal can be used as an input port for current mode control.
3. Error Amplifier	Conventional operational amplifier for closed-loop gain and phase compensation. Low output impedance; unity-gain stable. The output is held low by the slow start voltage at turn on in order to minimize overshoot.
4. Reference Generator	Precision 5.0V for internal and external usage to 50mA. Tracking 3.0V reference for internal usage only with nominal accuracy of ± 2%. 40V clamp zener for chip OV protection, 100mA maximum current.
5. PWM Comparator	Generates output pulse which starts at termination of clock pulse and ends when the ramp input crosses the lowest of two positive inputs.
6. PWM Latch	Terminates the PWM output pulse when set by inputs from either the PWM comparator, the pulse-by-pulse current limit comparator, or the error latch. Resets with each internal clock pulse.
7. PWM Output Switch	Transistor capable of sinking current to ground which is off during the PWM on-time and turns on to terminate the power pulse. Current capacity is 400mA saturated with peak capacitance discharge in excess of one amp.
SEQUENCING FUNCTIONS	
1. Start/UV Sense	With an increasing voltage, it generates a turn-on signal and releases the slow-start clamp at a start threshold. With a decreasing voltage, it generates a turn-off command at a lower level separated by a 200µA hysteresis current.
2. Drive Switch	Disables most of the chip to hold internal current consumption low, and Driver Bias OFF, until input voltage reaches start threshold.
3. Driver Bias	Supplies drive current to external power switch to provide turn-on bias.
4. Slow Start	Clamps low to hold PWM OFF. Upon release, rises with rate controlled by $R_S C_S$ for slow increase of output pulse width. Can also be used as an alternate maximum duty cycle clamp with an external voltage divider.
PROTECTION FUNCTIONS	
1. Error Latch	When set by momentary input, this latch insures immediate PWM shutdown and hold off until reset. Inputs to Error Latch are: a. OV > 3.2V (typically 3V) b. Stop > 2.4V (typically 1.6V) c. Current Sense 400mV over threshold (typical). Error Latch resets when slow start voltage falls to 0.4V if Reset Pin 5 < 2.8V. With Pin 5 > 3.2V, Error Latch will remain set.
2. Current Limiting	Differential input comparator terminates individual output pulses each time sense voltage rises above threshold. When sense voltage rises to 400mV (typical) above threshold, a shutdown signal is sent to Error Latch.
3. External Stop	A voltage over 1.2V will set the Error Latch and hold the output off. A voltage less than 0.8V will defeat the error latch and prevent shutdown. A capacitor here will slow the action of the error latch for transient protection by providing a typical delay of 13ms/µF.

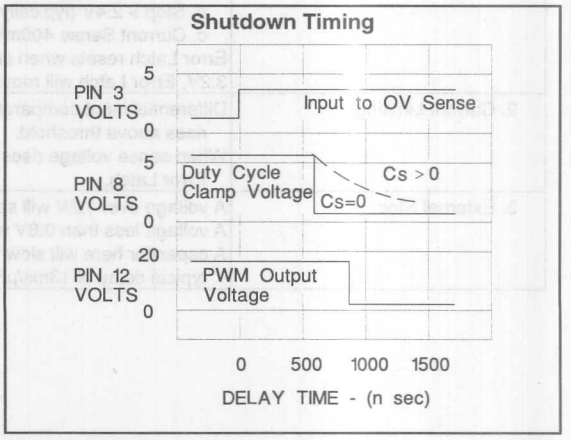

Start/UV Hysteresis
VIN = 20V
VPIN 2 = 2.5V
UC1841 Max
UC3841 Max
UC1841 Max
Typical Characteristic
UC1841 Min
UC3841 Min
UC1841 Min
HYSTERESIS CURRENT - (Microamps)
275
250
225
200
175
150
125
-50 -25 0 25 50 75 100 125
JUNCTION TEMPERATURE - (°C)


PWM Output-Saturation Voltage
OUTPUT SATURATION VOLTAGE - (V)
VIN = 20V
Low duty cycle
pulse test.
TJ = -55°C
TJ = 25°C
TJ = 125°C
4
3
2
1
0
0 100 200 300 400 500
OUTPUT SINK CURRENT - (mA)

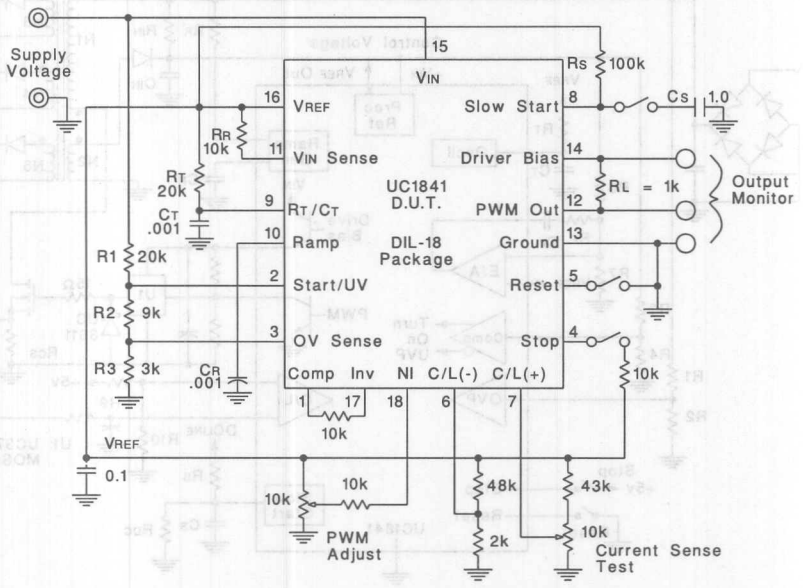

Oscillator Frequency
FREQUENCY - (KHz)
500
200
100
50
20
10
5
2
1
CT = 200pF
500pF
1nF
2nF
5nF
10nF
20nF
50nF
0.1µF
1 2 5 10 20 50 100 200 500
RT TIMING RESISTOR - (kΩ)


PWM Output Minimum Pulse Width
(Pulse width goes to zero
below value indicated)
MINIMUM PULSE WIDTH - (µ sec)
10
5.0
3.0
2.0
1.0
0.5
0.3
0.2
0.1
1/2 CT<CR<CT
CT = 200pF
CT = 500pF
CT = 1.0nF
CT = 2.0nF
10 20 30 50 100 200 300 500
OSCILLATOR FREQUENCY - (kHz)


Error Amplifier Open Loop Gain and Phase
VOLTAGE GAIN - (dB)
80
60
40
20
0
VIN = 20V
TJ = 25°C
Gain
Phase
PHASE SHIFT - (°)
180
270
360
100 1K 10K 100K 1M
FREQUENCY - (Hz)


Shutdown Timing
PIN 3
VOLTS
5
0
Input to OV Sense
PIN 8
VOLTS
5
0
Duty Cycle
Clamp Voltage
Cs=0
Cs > 0
PIN 12
VOLTS
20
0
PWM Output
Voltage
0 500 1000 1500
DELAY TIME - (n sec)

OPEN-LOOP TEST CIRCUIT



Nominal Frequency = $\frac{1}{R_T C_T}$ = 50 kHz

UV Fault Voltage = $3\left(\frac{R1 + R2 + R3}{R2 + R3}\right)$ = 8V

Current Limit = 200mV

Current Fault Voltage = 600mV

Start Voltage = $3\left(\frac{R1 + R2 + R3}{R2 + R3}\right)$ +0.2R1 = 12V

OV Fault Voltage = $3\left(\frac{R1 + R2 + R3}{R3}\right)$ = 32V

Duty Cycle Clamp = 50%

FLYBACK APPLICATION (A)

In this application (see Figure A, next page), complete control is maintained on the primary side. Control power is provided by RIN and CIN during start-up, and by a primary-referenced low voltage winding, N2, for efficient operation after start. The error amplifier loop is closed to regulate the DC voltage from N2 with other outputs following through their magnetic coupling – a task made even easier with the UC1841's feed–forward line regulation.

An extension to this application for more precise regulation would be the use of the UC1901 Isolated Feedback Generator for direct closed-loop control to an output.

Not shown, are protective snubbers or additional interface circuitry which may be required by the choice of the high-voltage switch, Qs, or the application; however, one example of power transistor interfacing is provided on the following page.

REGULATOR APPLICATION (B)

With the addition of a level shifting transistor, Q1, the UC1841 is an ideal control circuit for DC to DC converters such as the buck regulator shown in Figure B opposite. In addition to providing constant current drive pulses to the PIC661 power switch, this circuit has full fault protection and high speed dynamic line regulation due to its feed-forward capability. An additional feature is the ability to

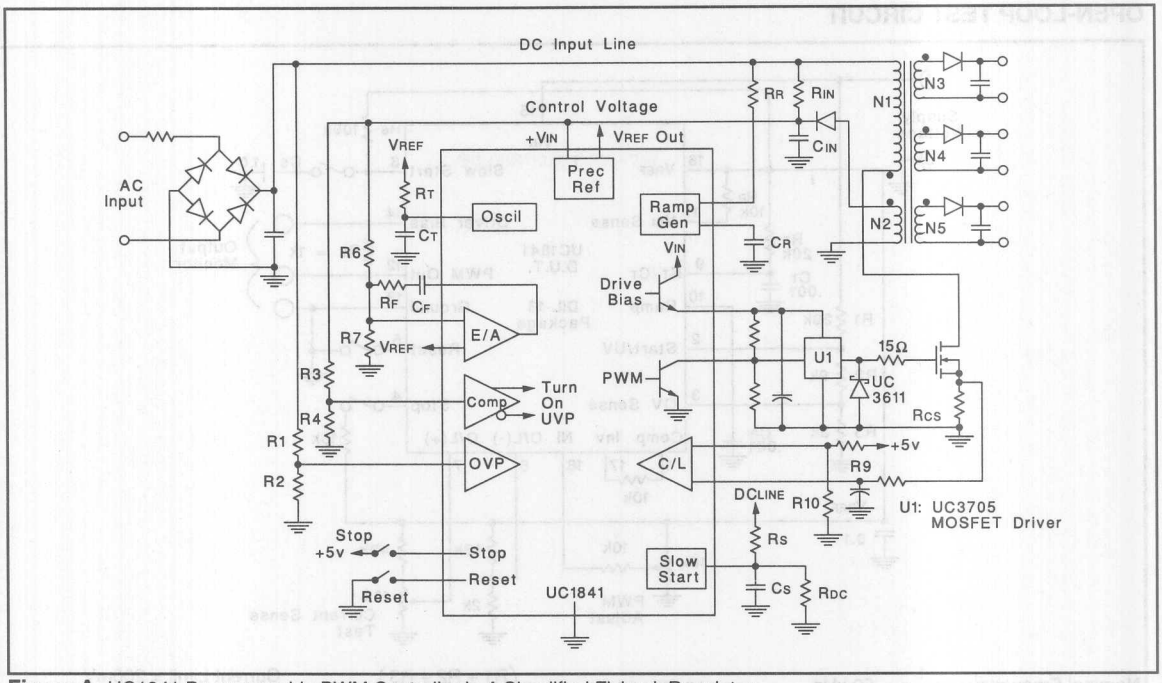


Figure A. UC1841 Programmable PWM Controller In A Simplified Flyback Regulator

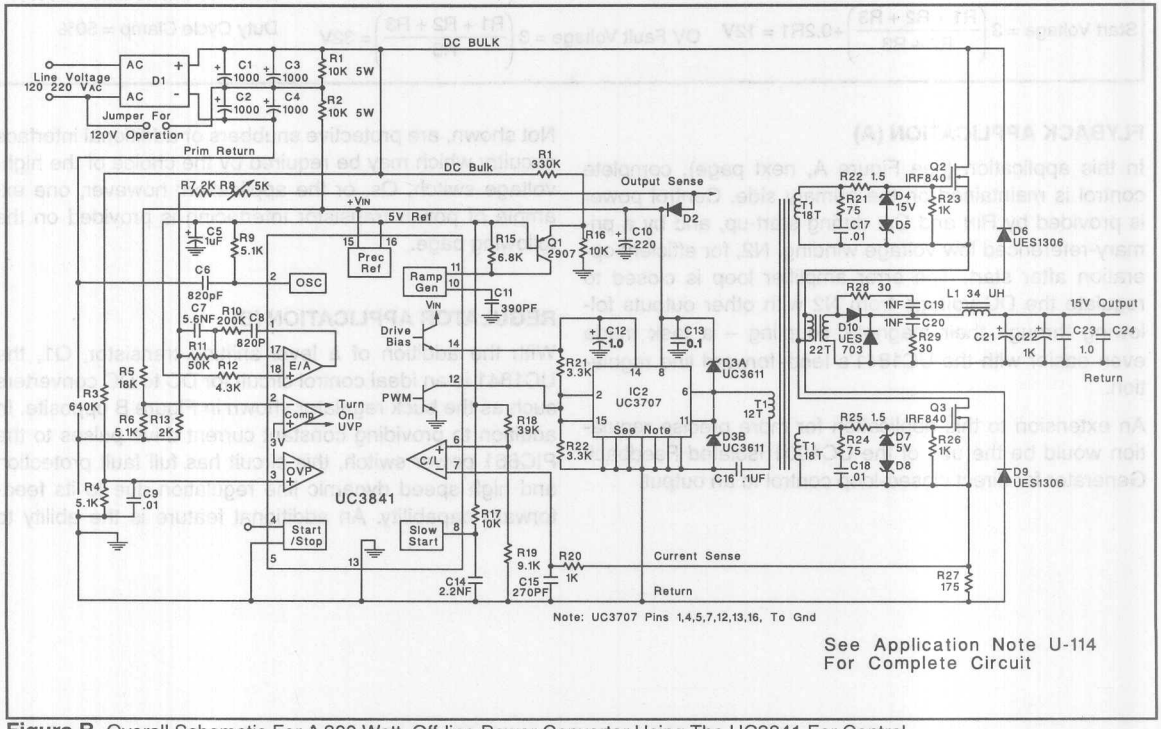
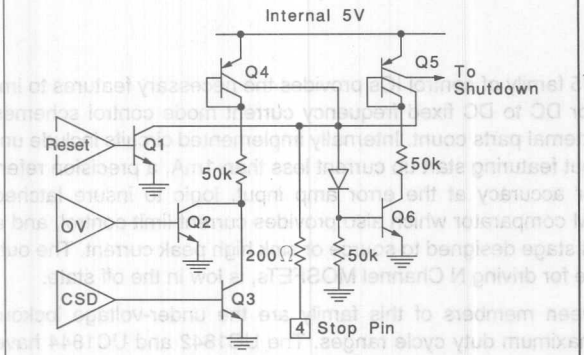


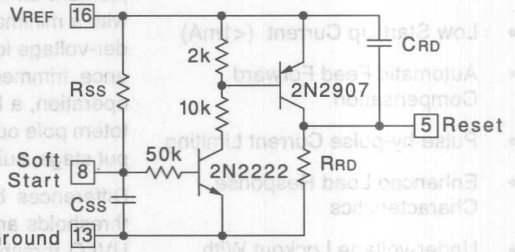
Figure B. Overall Schematic For A 300 Watt, Off-line Power Converter Using The UC3841 For Control

ERROR LATCH INTERNAL CIRCUITRY



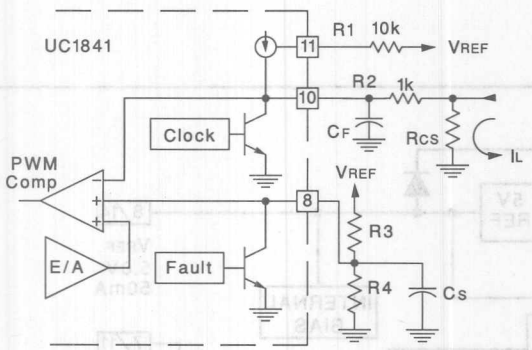
The Error Latch consists of Q5 and Q6 which, when both on, turns off the PWM Output and pulls the Slow-Start pin low. This latch is set by either the Over-Voltage or Current Shutdown comparators, or by a high signal on Pin 4. Reset is accomplished by either the Reset comparator or a low signal on Pin 4. An activation time delay can be provided with an external capacitor on Pin 4 in conjunction with the ≈ 100µA collector current from Q4.

PROGRAMMABLE SOFT START AND RESTART DELAY CIRCUIT



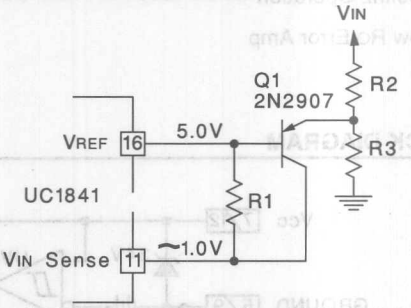
Restart Delay = (.51)(RRD)(CRD)

CURRENT MODE CONTROL



Since Pin 10 is a direct input to the PWM comparator, this point can also serve as a current sense port for current mode control. In this application, current sensing is ground referenced through RCS. Resistor R1 sets a 400mV offset across R2 (assuming R2 > RCS) so that both the Error Amplifier and Fault Shutdown can force the current completely to zero. R2 is also used along with CF as a small filter to attenuate leading-edge spikes on the load current waveform. In this mode, current limiting can be accomplished by divider R3/R4 which forms a clamp overriding the output of the Error Amplifier.

VOLTAGE FEED-FORWARD COMBINED WITH MAXIMUM DUTY-CYCLE CLAMP



In this circuit, R1 is used in conjunction with CR (not shown) to establish a minimum ramp charging current such that the ramp voltage reaches 4.2V at the required maximum output pulse width.

The purpose of Q1 is to provide an increasing ramp current above a threshold established by R2 and R3 such that the duty cycle is further reduced with increasing VIN.

The minimum ramp current is:

$$I_{R(MIN)} = \frac{V_{REF} - V_{IN\ SENSE}}{R1} \approx \frac{4V}{R1}$$

The threshold where VIN begins to add extra ramp current is:

$$V_{IN} \approx 5.6V\left(\frac{R2 + R3}{R3}\right)$$

Above the threshold, the ramp current will be:

$$I_R\ (VARIAB) \approx \frac{4}{R1} + \frac{V_{IN} - 5.6}{R2} - \frac{5.6}{R3}$$

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UNITRODE

UC1842/3/4/5
UC2842/3/4/5
UC3842/3/4/5

Current Mode PWM Controller

FEATURES

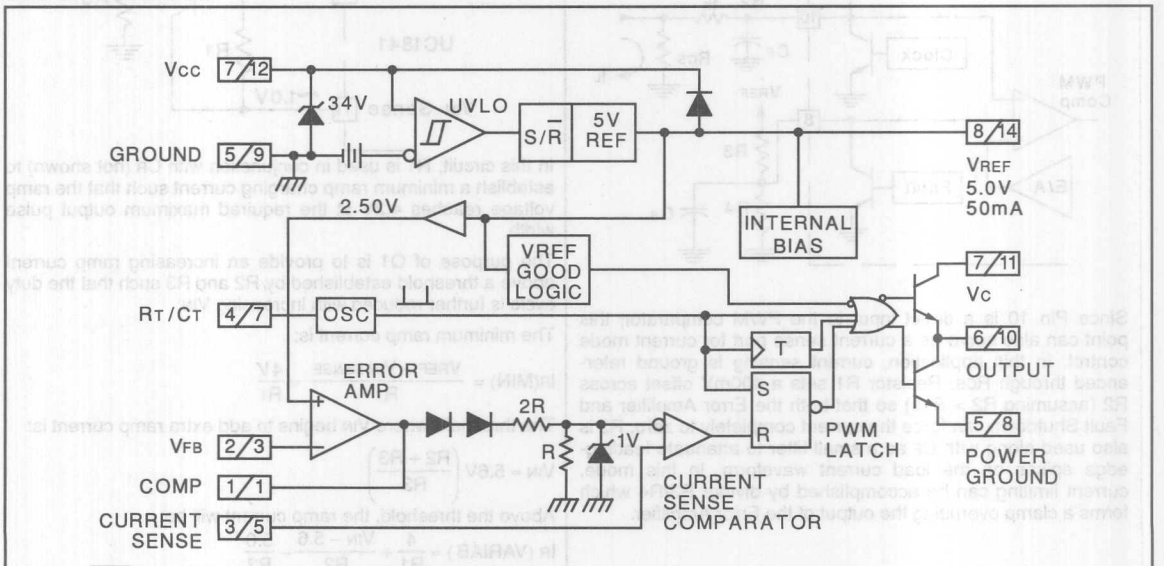
- Optimized For Off-line And DC To DC Converters
- Low Start Up Current (<1mA)
- Automatic Feed Forward Compensation
- Pulse-by-pulse Current Limiting
- Enhanced Load Response Characteristics
- Under-voltage Lockout With Hysteresis
- Double Pulse Suppression
- High Current Totem Pole Output
- Internally Trimmed Bandgap Reference
- 500khz Operation
- Low Ro Error Amp

DESCRIPTION

The UC1842/3/4/5 family of control ICs provides the necessary features to implement off-line or DC to DC fixed frequency current mode control schemes with a minimal external parts count. Internally implemented circuits include under-voltage lockout featuring start up current less than 1mA, a precision reference trimmed for accuracy at the error amp input, logic to insure latched operation, a PWM comparator which also provides current limit control, and a totem pole output stage designed to source or sink high peak current. The output stage, suitable for driving N Channel MOSFETs, is low in the off state.

Differences between members of this family are the under-voltage lockout thresholds and maximum duty cycle ranges. The UC1842 and UC1844 have UVLO thresholds of 16V (on) and 10V (off), ideally suited to off-line applications. The corresponding thresholds for the UC1843 and UC1845 are 8.4V and 7.6V. The UC1842 and UC1843 can operate to duty cycles approaching 100%. A range of zero to 50% is obtained by the UC1844 and UC1845 by the addition of an internal toggle flip flop which blanks the output off every other clock cycle.

BLOCK DIAGRAM



Note 1: A/B A = DIL-8 Pin Number. B = SO-14 Pin Number.
Note 2: Toggle flip flop used only in 1844 and 1845.

4/97

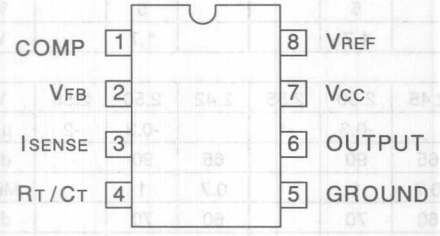
ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (Low Impedance Source) 30V
Supply Voltage (Icc <30mA) ..... Self Limiting
Output Current ..... ±1A
Output Energy (Capacitive Load) 5µJ
Analog Inputs (Pins 2, 3) ..... -0.3V to +6.3V
Error Amp Output Sink Current 10mA
Power Dissipation at $T_A \leq 25°C$ (DIL-8) 1W
Power Dissipation at $T_A \leq 25°C$ (SOIC-14) 725mW
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

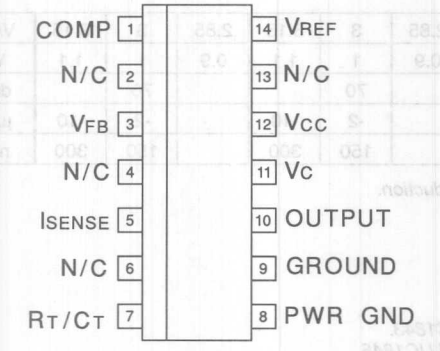
Note 1: All voltages are with respect to Pin 5.
All currents are positive into the specified terminal.
Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAMS

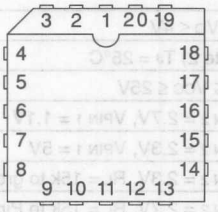
DIL-8, SOIC-8 (TOP VIEW)
N or J Package, D8 Package



SOIC-14 (TOP VIEW)
D Package



PLCC-20 (TOP VIEW)
Q Package



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
COMP	2
N/C	3
N/C	4
VFB	5
N/C	6
ISENSE	7
N/C	8
N/C	9
RT/CT	10
N/C	11
PWR GND	12
GROUND	13
N/C	14
OUTPUT	15
N/C	16
VC	17
VCC	18
N/C	19
VREF	20

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for -55°C ≤ T_A ≤ 125°C for the UC184X; -40°C ≤ T_A ≤ 85°C for the UC284X; 0°C ≤ T_A ≤ 70°C for the 384X; V_{CC} = 15V (Note 5); R_T = 10k; C_T =3.3nF, T_A=T_J.

PARAMETER	TEST CONDITIONS	UC1842/3/4/5 UC2842/3/4/5			UC3842/3/4/5			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Reference Section								
Output Voltage	T_J = 25°C, I_O = 1mA	4.95	5.00	5.05	4.90	5.00	5.10	V
Line Regulation	12 ≤ V_{IN} ≤ 25V		6	20		6	20	mV
Load Regulation	1 ≤ I_O ≤ 20mA		6	25		6	25	mV
Temp. Stability	(Note 2) (Note 7)		0.2	0.4		0.2	0.4	mV/°C
Total Output Variation	Line, Load, Temp. (Note 2)	4.9		5.1	4.82		5.18	V
Output Noise Voltage	10Hz ≤ f ≤ 10kHz, T_J = 25°C (Note2)		50			50		µV
Long Term Stability	T_A = 125°C, 1000Hrs. (Note 2)		5	25		5	25	mV
Output Short Circuit		-30	-100	-180	-30	-100	-180	mA
Oscillator Section								
Initial Accuracy	T_J = 25°C (Note 6)	47	52	57	47	52	57	kHz
Voltage Stability	12 ≤ V_{CC} ≤ 25V		0.2	1		0.2	1	%
Temp. Stability	T_{MIN} ≤ T_A ≤ T_{MAX} (Note 2)		5			5		%
Amplitude	$V_{PIN\ 4}$ peak to peak (Note 2)		1.7			1.7		V
Error Amp Section								
Input Voltage	$V_{PIN\ 1}$ = 2.5V	2.45	2.50	2.55	2.42	2.50	2.58	V
Input Bias Current			-0.3	-1		-0.3	-2	µA
A_{VOL}	2 ≤ V_O ≤ 4V	65	90		65	90		dB
Unity Gain Bandwidth	(Note 2) T_J = 25°C	0.7	1		0.7	1		MHz
PSRR	12 ≤ V_{CC} ≤ 25V	60	70		60	70		dB
Output Sink Current	$V_{PIN\ 2}$ = 2.7V, $V_{PIN\ 1}$ = 1.1V	2	6		2	6		mA
Output Source Current	$V_{PIN\ 2}$ = 2.3V, $V_{PIN\ 1}$ = 5V	-0.5	-0.8		-0.5	-0.8		mA
V_{OUT} High	$V_{PIN\ 2}$ = 2.3V, R_L = 15k to ground	5	6		5	6		V
V_{OUT} Low	$V_{PIN\ 2}$ = 2.7V, R_L = 15k to Pin 8		0.7	1.1		0.7	1.1	V
Current Sense Section								
Gain	(Notes 3 and 4)	2.85	3	3.15	2.85	3	3.15	V/V
Maximum Input Signal	$V_{PIN\ 1}$ = 5V (Note 3)	0.9	1	1.1	0.9	1	1.1	V
PSRR	12 ≤ V_{CC} ≤ 25V (Note 3) (Note 2)		70			70		dB
Input Bias Current			-2	-10		-2	-10	µA
Delay to Output	$V_{PIN\ 3}$ = 0 to 2V (Note 2)		150	300		150	300	ns

Note 2: These parameters, although guaranteed, are not 100% tested in production.
Note 3: Parameter measured at trip point of latch with $V_{PIN\ 2}$ = 0.
Note 4: Gain defined as

$$A = \frac{\Delta\ VPIN\,1}{\Delta\ VPIN\,3},\ 0 \le VPIN\,3 \le 0.8V$$

Note 5: Adjust V_{CC} above the start threshold before setting at 15V.
Note 6: Output frequency equals oscillator frequency for the UC1842 and UC1843.
Output frequency is one half oscillator frequency for the UC1844 and UC1845.
Note 7: Temperature stability, sometimes referred to as average temperature coefficient, is described by the equation:

$$Temp\ Stability = \frac{V_{REF}\,(max) - VREF\,(min)}{TJ\,(max) - TJ\,(min)}$$

V_{REF} (max) and V_{REF} (min) are the maximum and minimum reference voltages measured over the appropriate temperature range. Note that the extremes in voltage do not necessarily occur at the extremes in temperature.

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for $-55°C \le T_A \le 125°C$ for the UC184X; $-40°C \le T_A \le 85°C$ for the UC284X; $0°C \le T_A \le 70°C$ for the 384X; V_{CC} = 15V (Note 5); R_T = 10k; C_T =3.3nF, T_A=T_J.

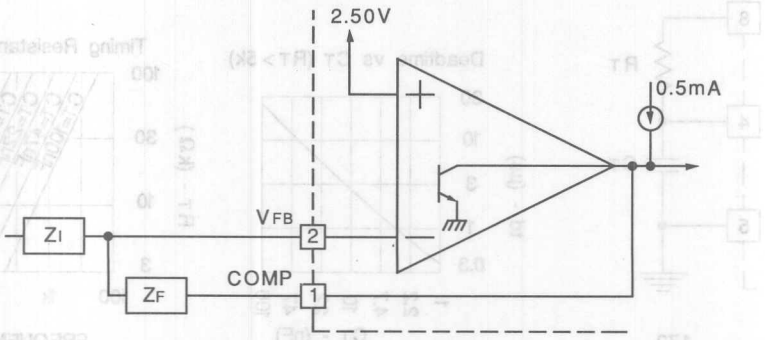
PARAMETER	TEST CONDITION	UC1842/3/4/5 UC2842/3/4/5			UC3842/3/4/5			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Output Section								
Output Low Level	I_{SINK} = 20mA		0.1	0.4		0.1	0.4	V
	I_{SINK} = 200mA		1.5	2.2		1.5	2.2	V
Output High Level	I_{SOURCE} = 20mA	13	13.5		13	13.5		V
	I_{SOURCE} = 200mA	12	13.5		12	13.5		V
Rise Time	T_J = 25°C, C_L = 1nF (Note 2)		50	150		50	150	ns
Fall Time	T_J = 25°C, C_L = 1nF (Note 2)		50	150		50	150	ns
Under-voltage Lockout Section								
Start Threshold	X842/4	15	16	17	14.5	16	17.5	V
	X843/5	7.8	8.4	9.0	7.8	8.4	9.0	V
Min. Operating Voltage After Turn On	X842/4	9	10	11	8.5	10	11.5	V
	X843/5	7.0	7.6	8.2	7.0	7.6	8.2	V
PWM Section								
Maximum Duty Cycle	X842/3	95	97	100	95	97	100	%
	X844/5	46	48	50	47	48	50	%
Minimum Duty Cycle				0			0	%
Total Standby Current								
Start-Up Current			0.5	1		0.5	1	mA
Operating Supply Current	$V_{PIN\ 2}$ = $V_{PIN\ 3}$ = 0V		11	17		11	17	mA
V_{CC} Zener Voltage	I_{CC} = 25mA	30	34		30	34		V

Note 2: These parameters, although guaranteed, are not 100% tested in production.
Note 3: Parameter measured at trip point of latch with $V_{PIN\ 2}$ = 0.
Note 4: Gain defined as:

$$A = \frac{\Delta\ VPIN\ 1}{\Delta\ VPIN\ 3};\ 0 \le VPIN\ 3 \le 0.8V.$$

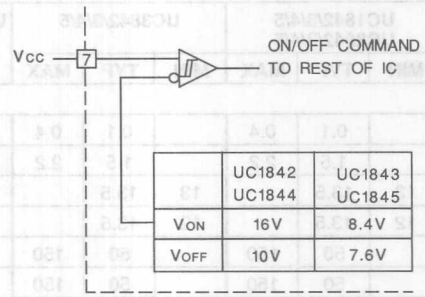
Note 5: Adjust V_{CC} above the start threshold before setting at 15V.
Note 6: Output frequency equals oscillator frequency for the UC1842 and UC1843.
Output frequency is one half oscillator frequency for the UC1844 and UC1845.

ERROR AMP CONFIGURATION

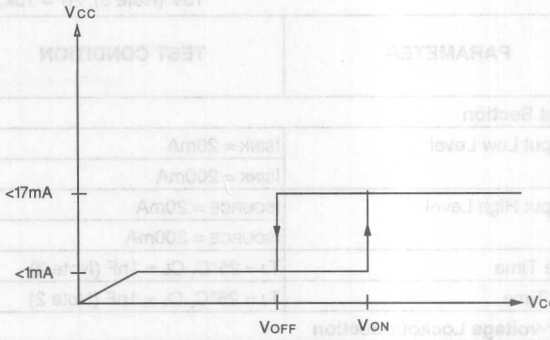


Error Amp can Source or Sink up to 0.5mA

UNDER-VOLTAGE LOCKOUT

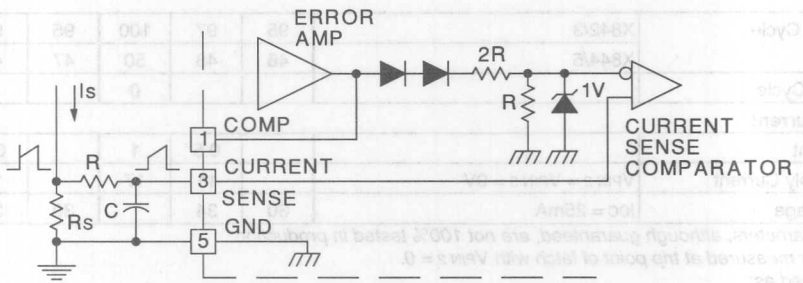


	UC1842 UC1844	UC1843 UC1845
VON	16V	8.4V
VOFF	10V	7.6V



During under-voltage lock-out, the output driver is biased to sink minor amounts of current. Pin 6 should be shunted to ground with a bleeder resistor to prevent activating the power switch with extraneous leakage currents.

CURRENT SENSE CIRCUIT

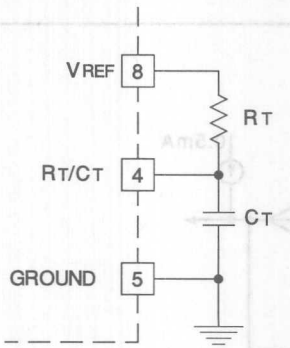


Peak Current (Is) is Determined By The Formula

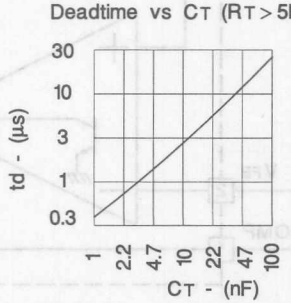
$$I_{SMAX} \approx \frac{1.0V}{Rs}$$

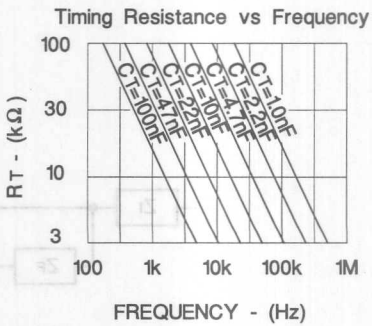
A small RC filter may be required to suppress switch transients.

OSCILLATOR SECTION

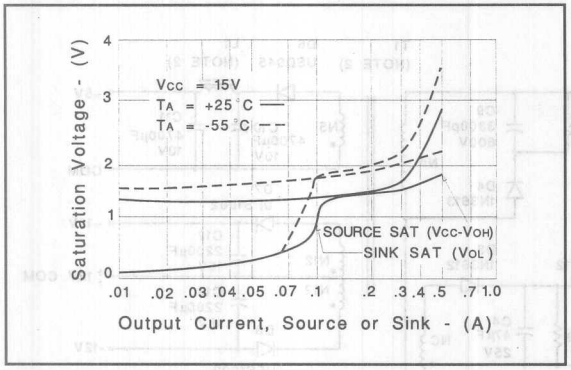


For $R_T > 5k$ $f \sim \frac{1.72}{R_T C_T}$

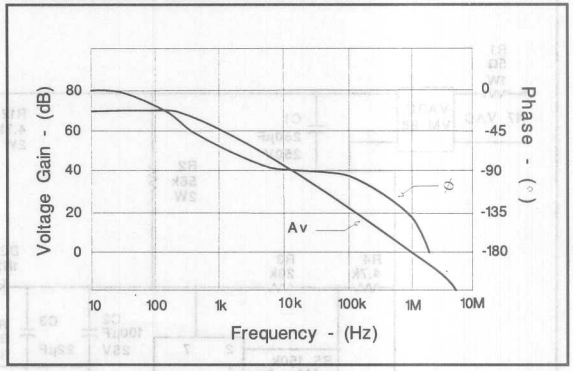




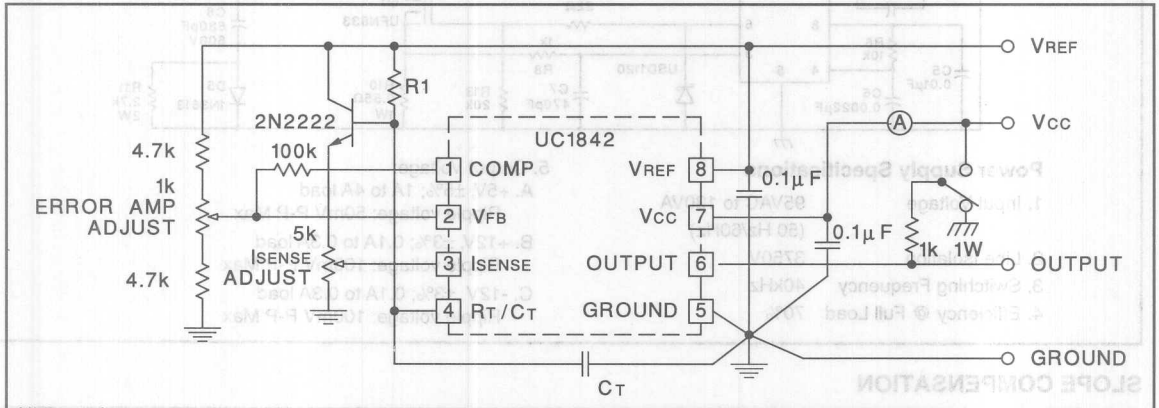
OUTPUT SATURATION CHARACTERISTICS



ERROR AMPLIFIER OPEN-LOOP FREQUENCY RESPONSE

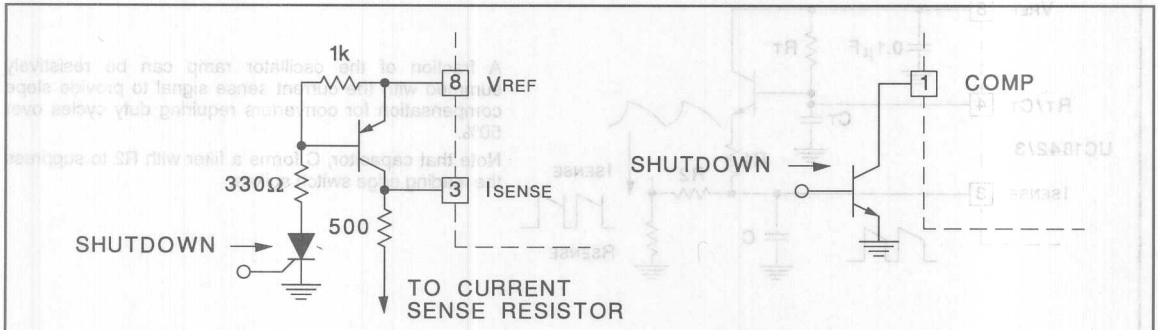


OPEN-LOOP LABORATORY FIXTURE



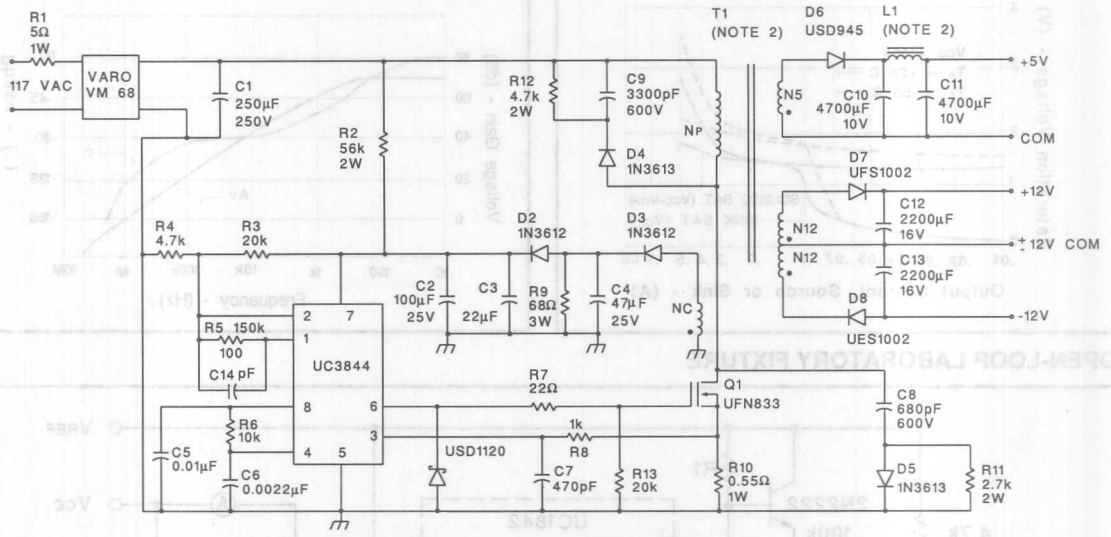
High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to pin 5 in a single point ground. The transistor and 5k potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to pin 3.

SHUT DOWN TECHNIQUES



Shutdown of the UC1842 can be accomplished by two methods; either raise pin 3 above 1V or pull pin 1 below a voltage two diode drops above ground. Either method causes the output of the PWM comparator to be high (refer to block diagram). The PWM latch is reset dominant so that the output will remain low until the next clock cycle after the shutdown condition at pin 1 and/or 3 is removed. In one example, an externally latched shutdown may be accomplished by adding an SCR which will be reset by cycling Vcc below the lower UVLO threshold. At this point the reference turns off, allowing the SCR to reset.

OFFLINE FLYBACK REGULATOR

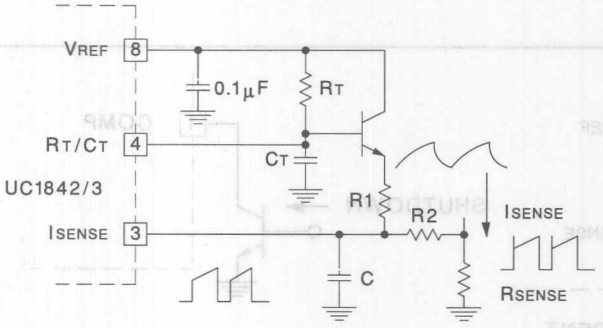


Power Supply Specifications

1. Input Voltage	95VAC to 130VA (50 Hz/60Hz)
2. Line Isolation	3750V
3. Switching Frequency	40kHz
4. Efficiency @ Full Load	70%

5. Output Voltage:
   - A. +5V, ±5%; 1A to 4A load
     Ripple voltage: 50mV P-P Max
   - B. +12V, ±3%; 0.1A to 0.3A load
     Ripple voltage: 100mV P-P Max
   - C. -12V ,±3%; 0.1A to 0.3A load
     Ripple voltage: 100mV P-P Max

SLOPE COMPENSATION



A fraction of the oscillator ramp can be resistively summed with the current sense signal to provide slope compensation for converters requiring duty cycles over 50%.

Note that capacitor, C forms a filter with R2 to suppress the leading edge switch spikes.

UNITRODE CORPORATION
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UNITRODE

UC1842A/3A/4A/5A
UC2842A/3A/4A/5A
UC3842A/3A/4A/5A

Current Mode PWM Controller

FEATURES

- Optimized for Off-line and DC to DC Converters
- Low Start Up Current (<0.5mA)
- Trimmed Oscillator Discharge Current
- Automatic Feed Forward Compensation
- Pulse-by-Pulse Current Limiting
- Enhanced Load Response Characteristics
- Under-Voltage Lockout With Hysteresis
- Double Pulse Suppression
- High Current Totem Pole Output
- Internally Trimmed Bandgap Reference
- 500kHz Operation
- Low RO Error Amp

DESCRIPTION

The UC1842A/3A/4A/5A family of control ICs is a pin for pin compatible improved version of the UC3842/3/4/5 family. Providing the necessary features to control current mode switched mode power supplies, this family has the following improved features. Start up current is guaranteed to be less than 0.5mA. Oscillator discharge is trimmed to 8.3mA. During under voltage lockout, the output stage can sink at least 10mA at less than 1.2V for VCC over 5V.

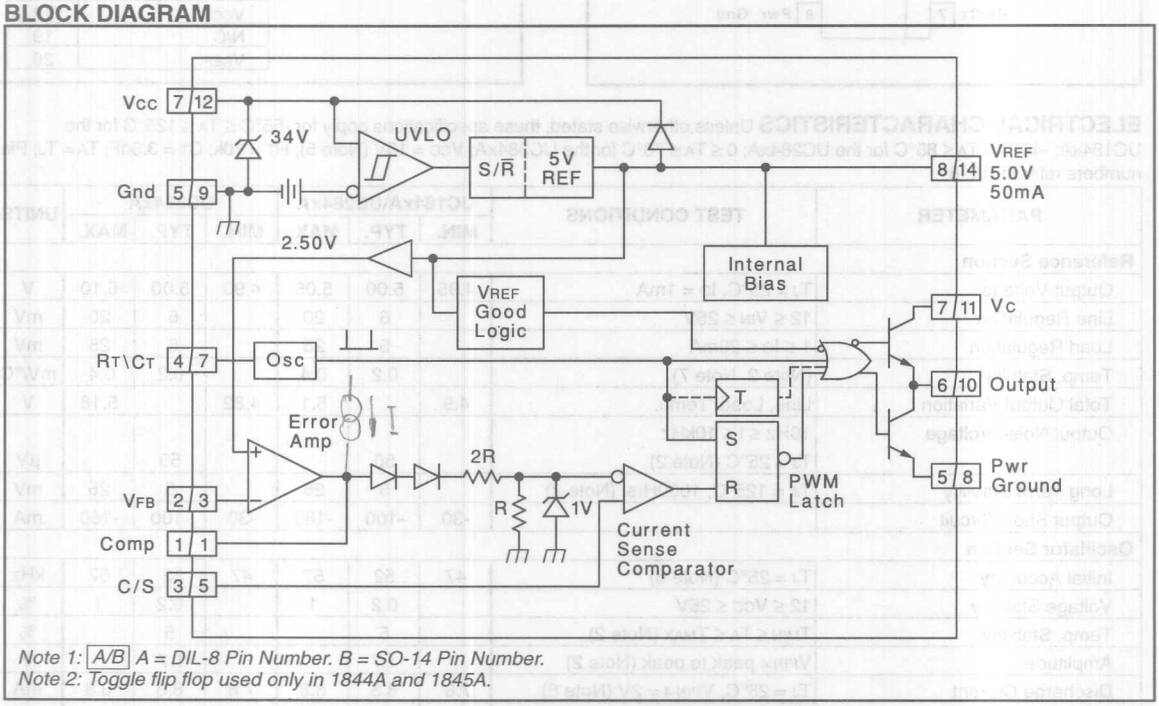
The difference between members of this family are shown in the table below.

Part #	UVLO On	UVLO Off	Maximum Duty Cycle
UC1842A	16.0V	10.0V	<100%
UC1843A	8.5V	7.9V	<100%
UC1844A	16.0V	10.0V	<50%
UC1845A	8.5V	7.9V	<50%

3

GENERAL POWER SUPPLY

BLOCK DIAGRAM



Note 1: A/B A = DIL-8 Pin Number. B = SO-14 Pin Number.
Note 2: Toggle flip flop used only in 1844A and 1845A.

9/94

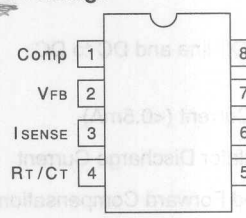
ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (Low Impedance Source) 30V
Supply Voltage (Icc mA) . . . . . Self Limiting
Output Current . . . . . ±1A
Output Energy (Capacitive Load) 5µJ
Analog Inputs (Pins 2, 3) . . . . . -0.3V to +6.3V
Error Amp Output Sink Current 10mA
Power Dissipation at $T_A \leq 25°C$ (DIL-8) 1W
Storage Temperature Range . . . . . -65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) . . . . . 300°C

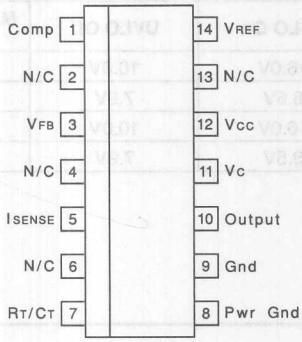
Note 1. All voltages are with respect to Ground, Pin 5. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages. Pin numbers refer to DIL package only.

CONNECTION DIAGRAMS

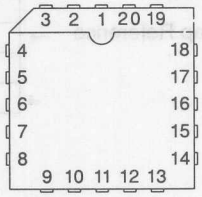
DIL-8, SOIC-8 (TOP VIEW)
J or N, D8 Package



SOIC-14 (TOP VIEW)
D Package



PLCC-20, LCC-20
(TOP VIEW)
Q, L Packages



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
Comp	2
N/C	3-4
VFB	5
N/C	6
ISENSE	7
N/C	8-9
RT/CT	10
N/C	11
Pwr Gnd	12
Gnd	13
N/C	14
Output	15
N/C	16
VC	17
VCC	18
N/C	19
VREF	20

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply for $-55°C \leq T_A \leq 125°C$ for the UC184xA; $-40°C \leq T_A \leq 85°C$ for the UC284xA; $0 \leq T_A \leq 70°C$ for the UC384xA; V_{CC} = 15V (Note 5); R_T = 10k; C_T = 3.3nF; $T_A = T_J$; Pin numbers refer to DIL-8.

PARAMETER	TEST CONDITIONS	UC184xA\UC284xA			UC384xA			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Reference Section								
Output Voltage	T_J = 25°C, Io = 1mA	4.95	5.00	5.05	4.90	5.00	5.10	V
Line Regulation	$12 \leq V_{IN} \leq 25V$		6	20		6	20	mV
Load Regulation	$1 \leq Io \leq 20mA$		6	25		6	25	mV
Temp. Stability	(Note 2, Note 7)		0.2	0.4		0.2	0.4	mV/°C
Total Output Variation	Line, Load, Temp.	4.9		5.1	4.82		5.18	V
Output Noise Voltage	10Hz ≤ f ≤ 10kHz T_J = 25°C (Note 2)		50			50		µV
Long Term Stability	T_A = 125°C, 1000Hrs. (Note 2)		5	25		5	25	mV
Output Short Circuit		-30	-100	-180	-30	-100	-180	mA
Oscillator Section								
Initial Accuracy	T_J = 25°C (Note 6)	47	52	57	47	52	57	kHz
Voltage Stability	$12 \leq V_{CC} \leq 25V$		0.2	1		0.2	1	%
Temp. Stability	$T_{MIN} \leq T_A \leq T_{MAX}$ (Note 2)		5			5		%
Amplitude	$V_{PIN\ 4}$ peak to peak (Note 2)		1.7			1.7		V
Discharge Current	T_J = 25°C, $V_{PIN\ 4}$ = 2V (Note 8)	7.8	8.3	8.8	7.8	8.3	8.8	mA
	$V_{PIN\ 4}$ = 2V (Note 8)	7.5		8.8	7.6		8.8	mA

ELECTRICAL CHARACTERISTICS (cont.) Unless otherwise stated, these specifications apply for -55°C ≤ TA ≤ 125°C for the UC184xA; -40°C ≤ TA ≤ 85°C for the UC284xA; 0 ≤ TA ≤ 70°C for the UC384xA; VCC = 15V (Note 5); RT = 10k; CT = 3.3nF; TA = TJ; Pin numbers refer to DIL-8.

PARAMETER	TEST CONDITIONS	UC184xA\UC284xA			UC384xA			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Error Amp Section								
Input Voltage	VPIN 1 = 2.5V	2.45	2.50	2.55	2.42	2.50	2.58	V
Input Bias Current			-0.3	-1		-0.3	-2	µA
AVOL	2 ≤ VO ≤ 4V	65	90		65	90		dB
Unity Gain Bandwidth	TJ = 25°C (Note 2)	0.7	1		0.7	1		MHz
PSRR	12 ≤ VCC ≤ 25V	60	70		60	70		dB
Output Sink Current	VPIN 2 = 2.7V, VPIN 1 = 1.1V	2	6		2	6		mA
Output Source Current	VPIN 2 = 2.3V, VPIN 1 = 5V	-0.5	-0.8		-0.5	-0.8		mA
VOUT High	VPIN 2 = 2.3V, RL = 15k to ground	5	6		5	6		V
VOUT Low	VPIN 2 = 2.7V, RL = 15k to Pin 8		0.7	1.1		0.7	1.1	V
Current Sense Section								
Gain	(Note 3, Note 4)	2.85	3	3.15	2.85	3	3.15	V/V
Maximum Input Signal	VPIN 1 = 5V (Note 3)	0.9	1	1.1	0.9	1	1.1	V
PSRR	12 ≤ VCC ≤ 25V (Note 3)		70			70		dB
Input Bias Current			-2	-10		-2	-10	µA
Delay to Output	VPIN 3 = 0 to 2V (Note 2)		150	300		150	300	ns
Output Section								
Output Low Level	ISINK = 20mA		0.1	0.4		0.1	0.4	V
	ISINK = 200mA		15	2.2		15	2.2	V
Output High Level	ISOURCE = 20mA	13	13.5		13	13.5		V
	ISOURCE = 200mA	12	13.5		12	13.5		V
Rise Time	TJ = 25°C, CL = 1nF (Note 2)		50	150		50	150	ns
Fall Time	TJ = 25°C, CL = 1nF (Note 2)		50	150		50	150	ns
UVLO Saturation	VCC = 5V, ISINK = 10mA		0.7	1.2		0.7	1.2	V
Under-Voltage Lockout Section								
Start Threshold	x842A/4A	15	16	17	14.5	16	17.5	V
	x843A/5A	7.8	8.4	9.0	7.8	8.4	9.0	V
Min. Operation Voltage After	x842A/4A	9	10	11	8.5	10	11.5	V
TurnOn	x843A/5A	7.0	7.6	8.2	7.0	7.6	8.2	V
PWM Section								
Maximum Duty Cycle	x842A/3A	94	96	100	94	96	100	%
	x844A/5A	47	48	50	47	48	50	%
Minimum Duty Cycle				0			0	%
Total Standby Current								
Start-Up Current			0.3	0.5		0.3	0.5	mA
Operating Supply Current	VPIN 2 = VPIN 3 = 0V		11	17		11	17	mA
VCC Zener Voltage	ICC = 25mA	30	34		30	34		V

Note 2: These parameters, although guaranteed, are not 100% tested in production.

Note 3: Parameter measured at trip point of latch with VPIN2 = 0.

Note 4: Gain defined as: $A = \frac{\Delta V_{PIN\ 1}}{\Delta V_{PIN\ 3}}$ *; 0 ≤ VPIN 3 ≤ 0.8V.*

Note 5: Adjust VCC above the start threshold before setting at 15V.

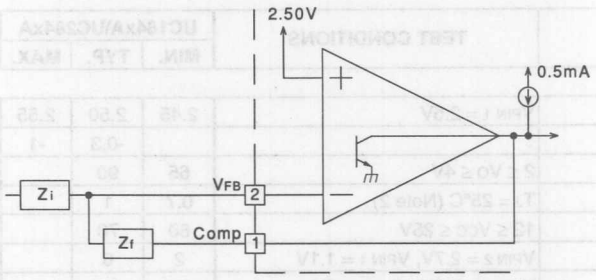
Note 6: Output frequency equals oscillator frequency for the UC1842A and UC1843A. Output frequency is one half oscillator frequency for the UC1844A and UC1845A.

Note 7: "Temperature stability, sometimes referred to as average temperature coefficient, is described by the equation:

$$\text{Temp Stability} = \frac{V_{REF}\,(max) - V_{REF}\,(min)}{T_J\,(max) - T_J\,(min)}.$$

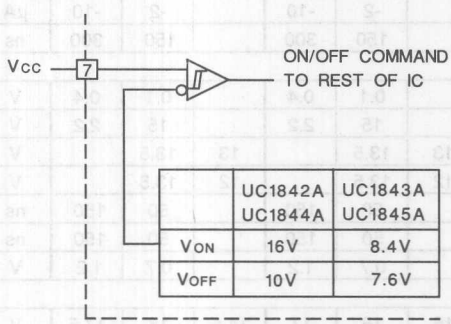
VREF (max) and VREF (min) are the maximum & minimum reference voltage measured over the appropriate temperature range. Note that the extremes in voltage do not necessarily occur at the extremes in temperature."

Note 8: This parameter is measured with RT = 10kΩ to VREF. This contributes approximately 300µA of current to the measurement. The total current flowing into the RT/CT pin will be approximately 300µA higher than the measured value.

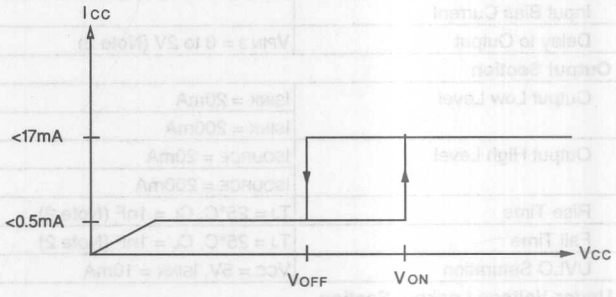


Error Amp can Source and Sink up to 0.5mA, and Sink up to 2mA.

Under-Voltage Lockout

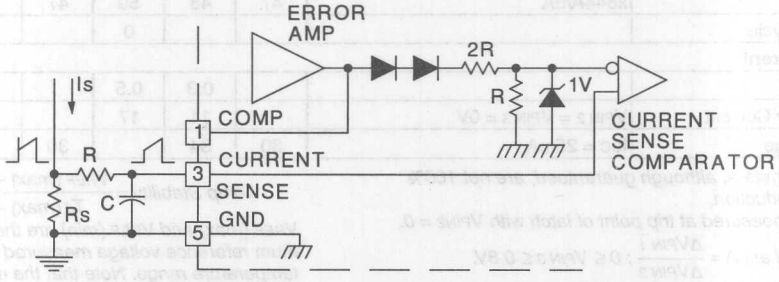


	UC1842A UC1844A	UC1843A UC1845A
VON	16V	8.4V
VOFF	10V	7.6V



During UVLO, the Output is low.

Current Sense Circuit



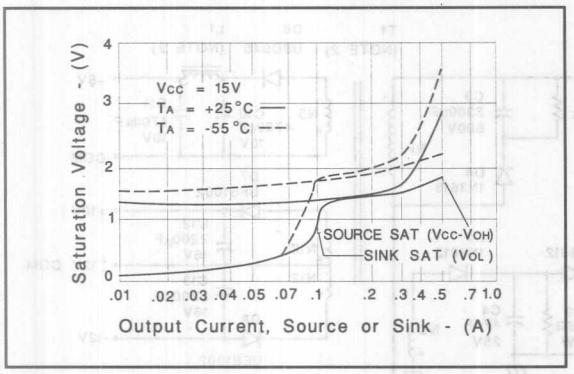
Peak Current (Is) is Determined By The Formula

$$I_{SMAX} \approx \frac{1.0V}{Rs}$$

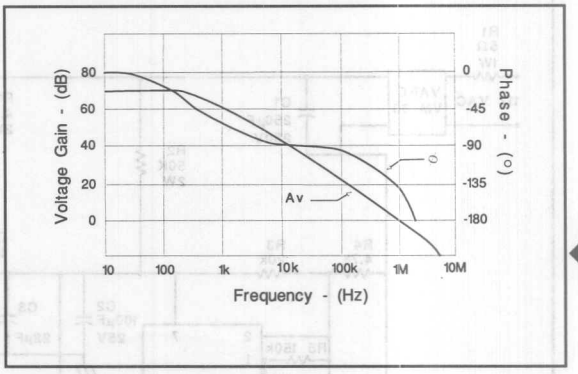
A small RC filter may be required to suppress switch transients.

APPLICATIONS DATA (cont.)

Output Saturation Characteristics

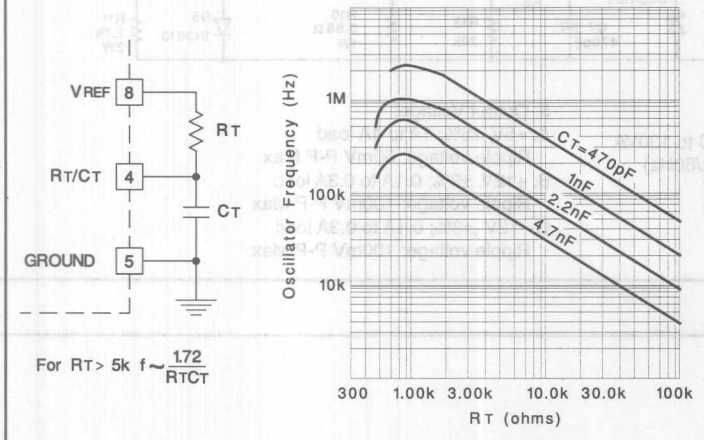


Error Amplifier Open-Loop Frequency Response

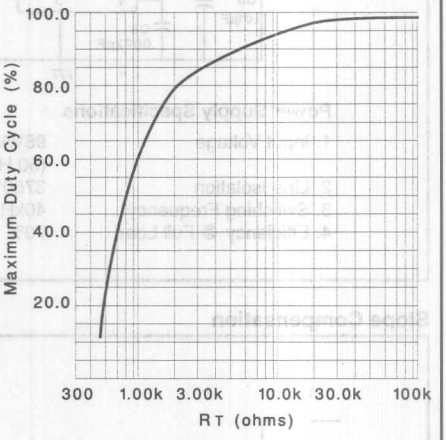


Oscillator Section

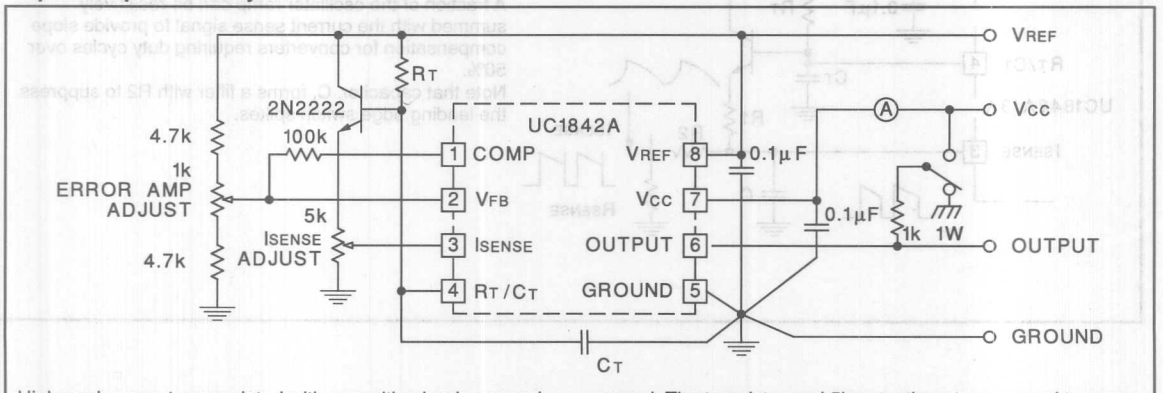
Oscillator Frequency vs Timing Resistance



Maximum Duty Cycle vs Timing Resistor



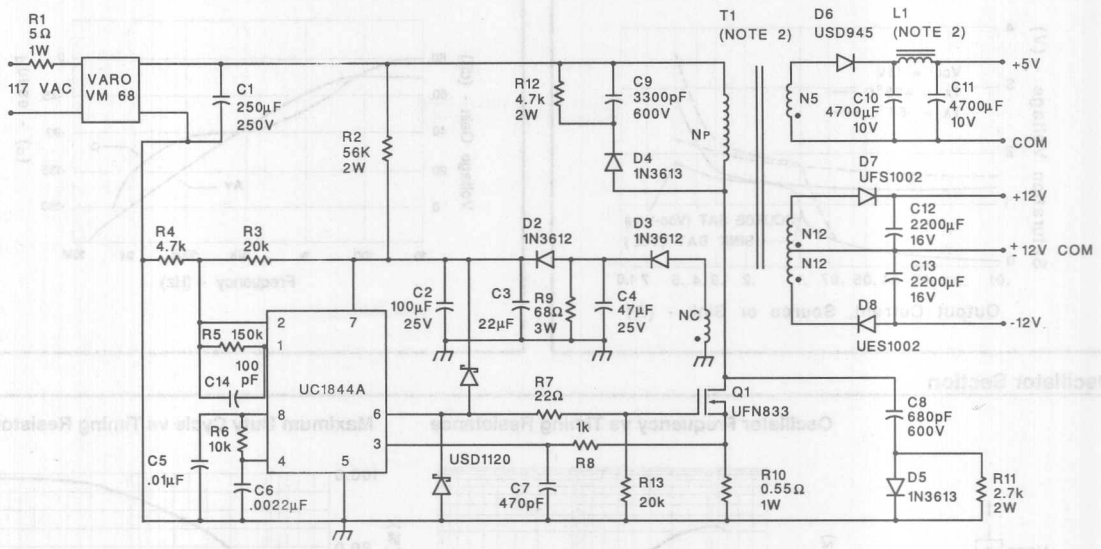
Open-Loop Laboratory Test Fixture



High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to pin 5 in a single point ground. The transistor and 5k potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to pin 3.

APPLICATIONS DATA (cont.)

Off-line Flyback Regulator

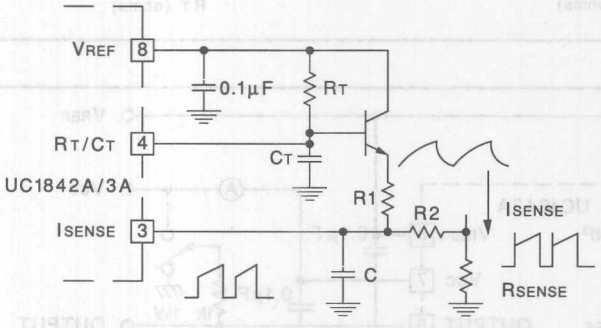


Power Supply Specifications

1. Input Voltage	95VAC to 130VA (50 Hz/60Hz)
2. Line Isolation	3750V
3. Switching Frequency	40kHz
4. Efficiency @ Full Load	70%

5. Output Voltage:
   A. +5V, ±5%; 1A to 4A load
      Ripple voltage: 50mV P-P Max
   B. +12V, ±3%; 0.1A to 0.3A load
      Ripple voltage: 100mV P-P Max
   C. -12V ,±3%; 0.1A to 0.3A load
      Ripple voltage: 100mV P-P Max

Slope Compensation



A fraction of the oscillator ramp can be resistively summed with the current sense signal to provide slope compensation for converters requiring duty cycles over 50%.
Note that capacitor, C, forms a filter with R2 to suppress the leading edge switch spikes.

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
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UNITRODE

Current Mode PWM Controller

UC1846/7
UC2846/7
UC3846/7

FEATURES

- Automatic Feed Forward Compensation
- Programmable Pulse-by-Pulse Current Limiting
- Automatic Symmetry Correction in Push-pull Configuration
- Enhanced Load Response Characteristics
- Parallel Operation Capability for Modular Power Systems
- Differential Current Sense Amplifier with Wide Common Mode Range
- Double Pulse Suppression
- 500mA (Peak) Totem-pole Outputs
- ±1% Bandgap Reference
- Under-voltage Lockout
- Soft Start Capability
- Shutdown Terminal
- 500kHZ Operation

DESCRIPTION

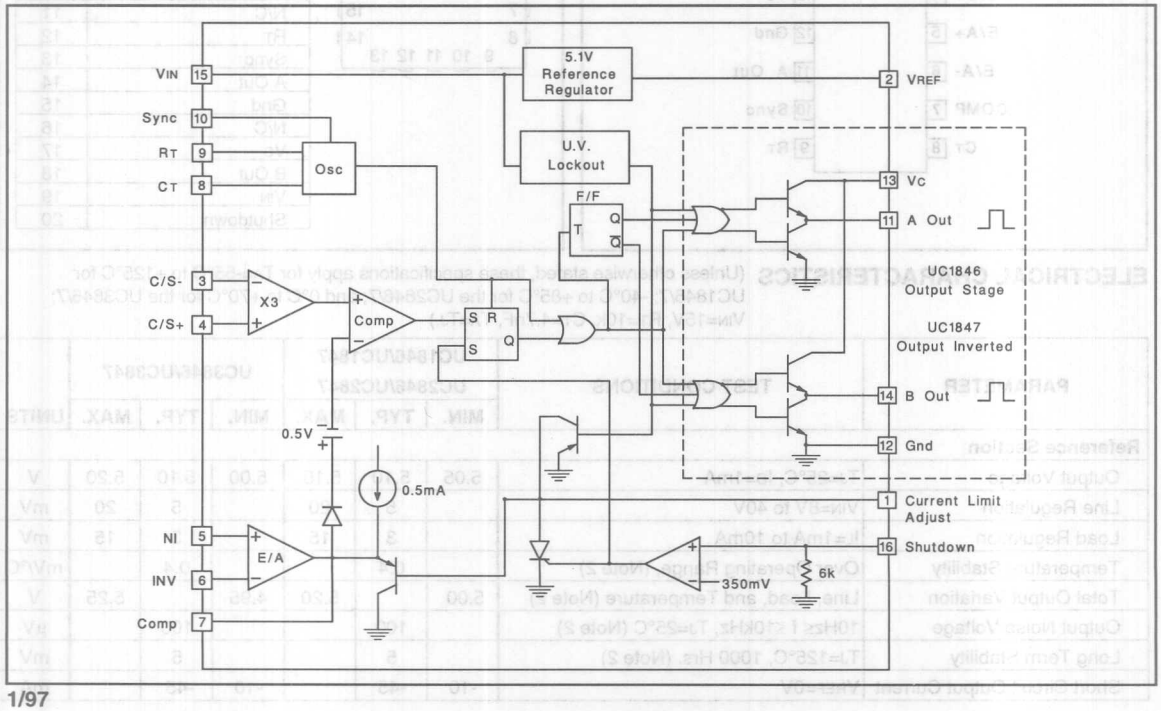
The UC1846/7 family of control ICs provides all of the necessary features to implement fixed frequency, current mode control schemes while maintaining a minimum external parts count. The superior performance of this technique can be measured in improved line regulation, enhanced load response characteristics, and a simpler, easier-to-design control loop. Topological advantages include inherent pulse-by-pulse current limiting capability, automatic symmetry correction for push-pull converters, and the ability to parallel "power modules" while maintaining equal current sharing.

Protection circuitry includes built-in under-voltage lockout and programmable current limit in addition to soft start capability. A shutdown function is also available which can initiate either a complete shutdown with automatic restart or latch the supply off.

Other features include fully latched operation, double pulse suppression, deadline adjust capability, and a ±1% trimmed bandgap reference.

The UC1846 features low outputs in the OFF state, while the UC1847 features high outputs in the OFF state.

BLOCK DIAGRAM



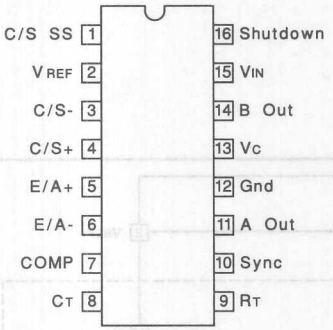
1/97

Supply Voltage (Pin 15) ..... +40V
Collector Supply Voltage (Pin 13) ..... +40V
Output Current, Source or Sink (Pins 11, 14) 500mA
Analog Inputs (Pins 3, 4, 5, 6, 16) ..... -0.3V to +V_{IN}
Reference Output Current (Pin 2) ..... -30mA
Sync Output Current (Pin 10) ..... -5mA
Error Amplifier Output Current (Pin 7) ..... -5mA
Soft Start Sink Current (Pin 1) 50mA
Oscillator Charging Current (Pin 9) 5mA
Power Dissipation at T_A=25°C 1000mW
Power Dissipation at T_C=25°C 2000mW
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10 seconds) ..... +300°C

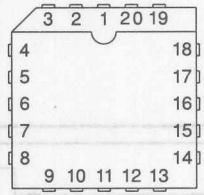
Note 1. All voltages are with respect to Ground, Pin 13. Currents are positive into, negative out of the speficied terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages. Pin numbers refer to DIL and SOIC packages only.

CONNECTION DIAGRAMS

DIL-16, SOIC-16
(TOP VIEW)
J or N Package, DW Package



PLCC-20, LCC-20
(TOP VIEW)
Q, L Packages



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
C/L SS	2
V_{REF}	3
C/S-	4
C/S+	5
N/C	6
E/A+	7
E/A-	8
Comp	9
C_T	10
N/C	11
R_T	12
Sync	13
A Out	14
Gnd	15
N/C	16
Vc	17
B Out	18
V_{IN}	19
Shutdown	20

ELECTRICAL CHARACTERISTICS

(Unless otherwise stated, these specifications apply for T_A=-55°C to +125°C for UC1846/7; -40°C to +85°C for the UC2846/7; and 0°C to +70°C for the UC3846/7; V_{IN}=15V, R_T=10k, C_T=4.7nF, T_A=T_J.)

PARAMETER	TEST CONDITIONS	UC1846/UC1847 UC2846/UC2847			UC3846/UC3847			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Reference Section								
Output Voltage	T_J=25°C, I_O=1mA	5.05	5.10	5.15	5.00	5.10	5.20	V
Line Regulation	V_{IN}=8V to 40V		5	20		5	20	mV
Load Regulation	I_L=1mA to 10mA		3	15		3	15	mV
Temperature Stability	Over Operating Range, (Note 2)		0.4			0.4		mV/°C
Total Output Variation	Line, Load, and Temperature (Note 2)	5.00		5.20	4.95		5.25	V
Output Noise Voltage	10Hz≤ f ≤10kHz, T_J=25°C (Note 2)		100			100		µV
Long Term Stability	T_J=125°C, 1000 Hrs. (Note 2)		5			5		mV
Short Circuit Output Current	V_{REF}=0V	-10	-45		-10	-45		mA

ELECTRICAL CHARACTERISTICS (cont.)

(Unless otherwise stated, these specifications apply for T_A=-55°C to +125°C for UC1846/7; -40°C to +85°C for the UC2846/7; and 0°C to +70°C for the UC3846/7; V_{IN}=15V, R_T=10k, C_T=4.7nF, T_A=T_J.)

PARAMETER	TEST CONDITIONS	UC1846/UC1847 UC2846/UC2847			UC3846/UC3847			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Oscillator Section								
Initial Accuracy	T_J=25°C	39	43	47	39	43	47	kHz
Voltage Stability	V_{IN}=8V to 40V		-1	2		-1	2	%
Temperature Stability	Over Operating Range (Note 2)		-1			-1		%
Sync Output High Level		3.9	4.35		3.9	4.35		V
Sync Output Low Level			2.3	2.5		2.3	2.5	V
Sync Input High Level	Pin 8=0V	3.9			3.9			V
Sync Input Low Level	Pin 8=0V			2.5			2.5	V
Sync Input Current	Sync Voltage=3.9V, Pin 8=0V		1.3	1.5		1.3	1.5	mA
Error Amp Section								
Input Offset Voltage			0.5	5		0.5	10	mV
Input Bias Current			-0.6	-1		-0.6	-2	µA
Input Offset Current			40	250		40	250	nA
Common Mode Range	V_{IN}=8V to 40V	0		V_{IN}-2V	0		V_{IN}-2V	V
Open Loop Voltage Gain	ΔV_O=1.2 to 3V, V_{CM}=2V	80	105		80	105		dB
Unity Gain Bandwidth	T_J=25°C (Note 2)	0.7	1.0		0.7	1.0		MHz
CMRR	V_{CM}=0V to 38V, V_{IN}=40V	75	100		75	100		dB
PSRR	V_{IN}=8V to 40V	80	105		80	105		dB
Output Sink Current	V_{ID}=-15mV to -5V, $V_{PIN\ 7}$=1.2V	2	6		2	6		mA
Output Source Current	V_{ID}=15mV to 5V, $V_{PIN\ 7}$=2.5V	-0.4	-0.5		-0.4	-0.5		mA
High Level Output Voltage	R_L=(Pin 7) 15kΩ	4.3	4.6		4.3	4.6		V
Low Level Output Voltage			0.7	1		0.7	1	V
Current Sense Amplifier Section								
Amplifier Gain	$V_{PIN\ 3}$=0V, Pin 1 Open (Notes 3 & 4)	2.5	2.75	3.0	2.5	2.75	3.0	V
Maximum Differential Input Signal ($V_{PIN\ 4}$-$V_{PIN\ 3}$)	Pin 1 Open (Note 3) R_L (Pin 7)=15kW	1.1	1.2		1.1	1.2		V
Input Offset Voltage	$V_{PIN\ 1}$=0.5V, Pin 7 Open (Note 3)		5	25		5	25	mV
CMRR	V_{CM}=1V to 12V	60	83		60	83		dB
PSRR	V_{IN}=8V to 40V	60	84		60	84		dB
Input Bias Current	$V_{PIN\ 1}$=0.5V, Pin 7 Open (Note 3)		-2.5	-10		-2.5	-10	µA
Input Offset Current	$V_{PIN\ 1}$=0.5V, Pin 7 Open (Note 3)		0.08	1		0.08	1	µA
Input Common Mode Range		0		V_{IN}-3	0		V_{IN}-3	V
Delay to Outputs	T_J=25°C, (Note 2)		200	500		200	500	ns
Current Limit Adjust Section								
Current Limit Offset	$V_{PIN\ 3}$=0V, $V_{PIN\ 4}$=0V, Pin 7 Open (Note 3)	0.45	0.5	0.55	0.45	0.5	0.55	V
Input Bias Current	$V_{PIN\ 5}$=V_{REF}, $V_{PIN\ 6}$=0V		-10	-30		-10	-30	µA
Shutdown Terminal Section								
Threshold Voltage		250	350	400	250	350	400	mV
Input Voltage Range		0		V_{IN}	0		V_{IN}	V
Minimum Latching Current ($I_{PIN\ 1}$)	(Note 6)	3.0	1.5		3.0	1.5		mA

ELECTRICAL CHARACTERISTICS (cont.)

(Unless otherwise stated, these specifications apply for T_A=-55°C to +125°C for UC1846/7; -40°C to +85°C for the UC2846/7; and 0°C to +70°C for the UC3846/7; V_{IN}=15V, R_T=10k, C_T=4.7nF, T_A=T_J.)

PARAMETER	TEST CONDITIONS	UC1846/UC1847 UC2846/UC2847			UC3846/UC3847			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Shutdown Terminal Section (cont.)								
Maximum Non-Latching Current ($I_{PIN\ 1}$)	(Note 7)		1.5	0.8		1.5	0.8	mA
Delay to Outputs	T_J=25°C (Note 2)		300	600		300	600	ns
Output Section								
Collector-Emitter Voltage		40			40			V
Collector Leakage Current	V_C=40V (Note 5)			200			200	µA
Output Low Level	I_{SINK}=20mA		0.1	0.4		0.1	0.4	V
	I_{SINK}=100mA		0.4	2.1		0.4	2.1	V
Output High Level	I_{SOURCE}=20mA	13	13.5		13	13.5		V
	I_{SOURCE}=100mA	12	13.5		12	13.5		V
Rise Time	C_L=1nF, T_J=25°C (Note 2)		50	300		50	300	ns
Fall Time	C_L=1nF, T_J=25°C (Note 2)		50	300		50	300	ns
Under-Voltage Lockout Section								
Start-Up Threshold			7.7	8.0		7.7	8.0	V
Threshold Hysteresis			0.75			0.75		V
Total Standby Current								
Supply Current			17	21		17	21	mA

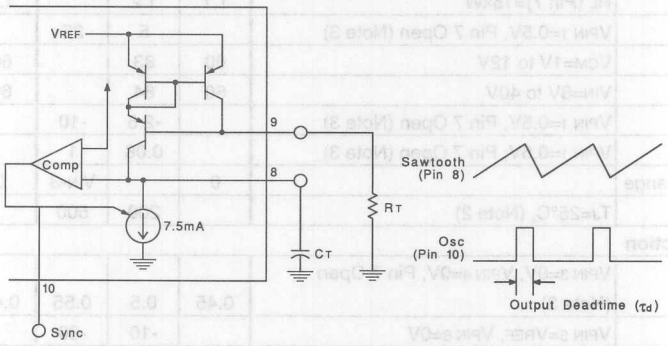
Note 2. These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.
Note 3. Parameter measured at trip point of latch with $V_{PIN\ 5}$ = V_{REF}, $V_{PIN\ 6}$ = 0V.

Note 4. Amplifier gain defined as: $G = \frac{\Delta V_{PIN\ 7}}{\Delta V_{PIN\ 4}}$; ΔV_{PIN4} = 0 to 1.0V.

Note 5. Applies to UC1846/UC2846/UC3846 only due to polarity of outputs.
Note 6. Current into Pin 1 guaranteed to latch circuit in shutdown state.
Note 7. Current into Pin 1 guaranteed not to latch circuit in shutdown state.

APPLICATIONS DATA

Oscillator Circuit



Output deadtime is determined by the external capacitor, C_T, according to the formula: $\tau_d(\mu s) = 145 C_T(\mu f)\left(\frac{I_D}{I_D - \frac{3.6}{R_T(k\Omega)}}\right)$.

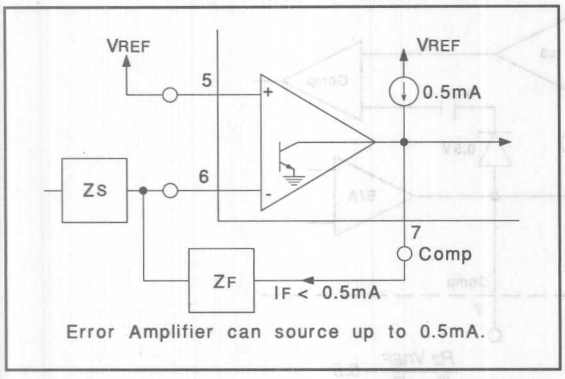
I_D = Oscillator discharge current at 25°C is typically 7.5.

For large values of R_T: $\tau_d(\mu s) \approx 145 C_T(\mu f)$.

Oscillator frequency is approximated by the formula: $f_T(kHz) \approx \frac{2.2}{R_T(k\Omega) \bullet C_T(\mu f)}$.

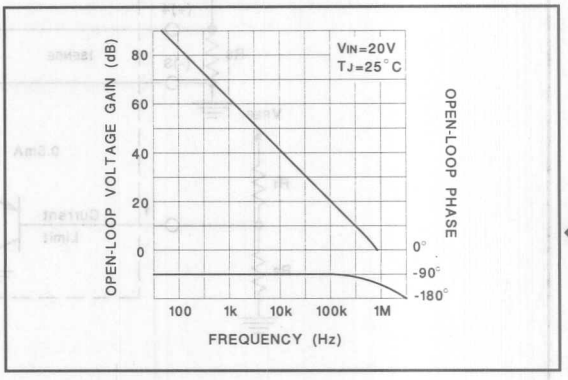
APPLICATIONS DATA (cont.)

Error Amp Output Configuration

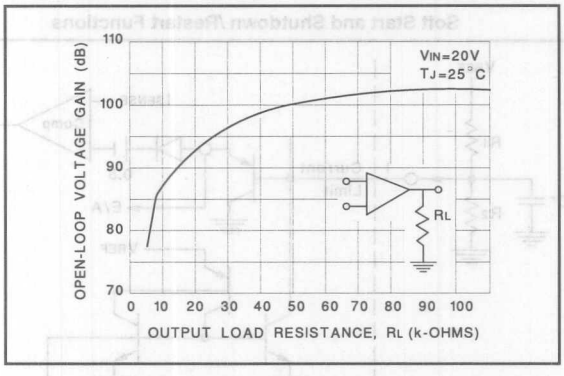


Error Amplifier can source up to 0.5mA.

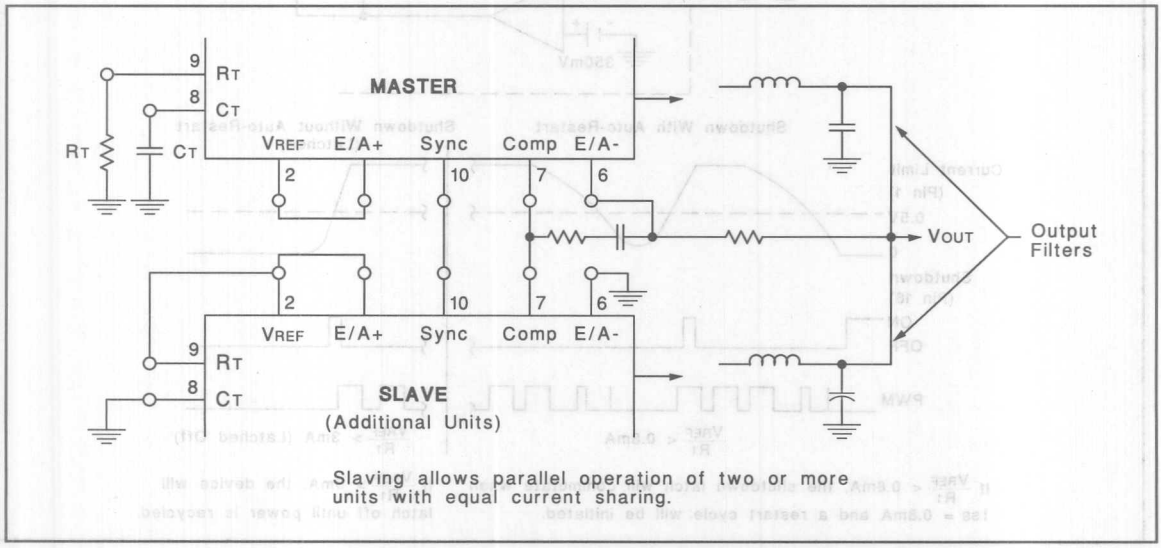
Error Amp Gain and Phase vs Frequency



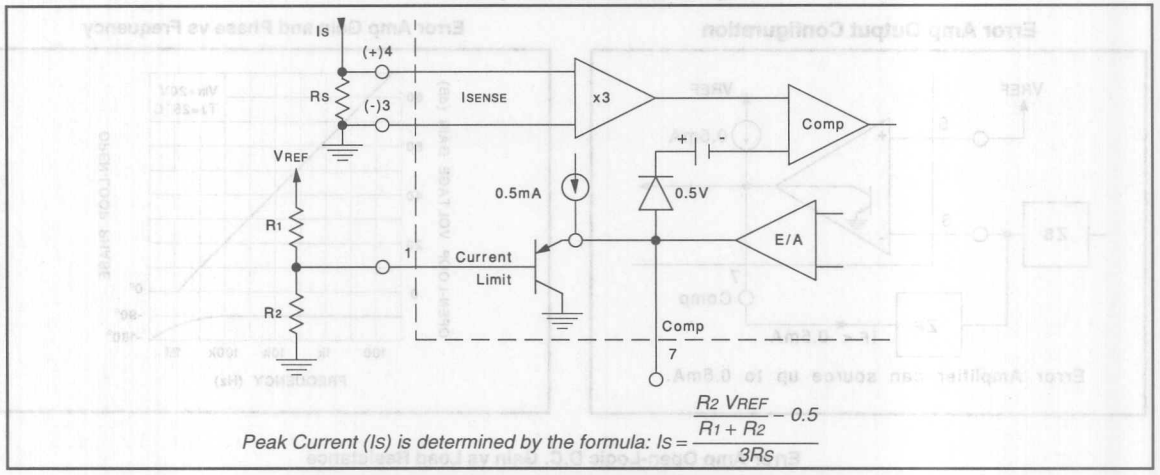
Error Amp Open-Logic D.C. Gain vs Load Resistance



Parallel Operation

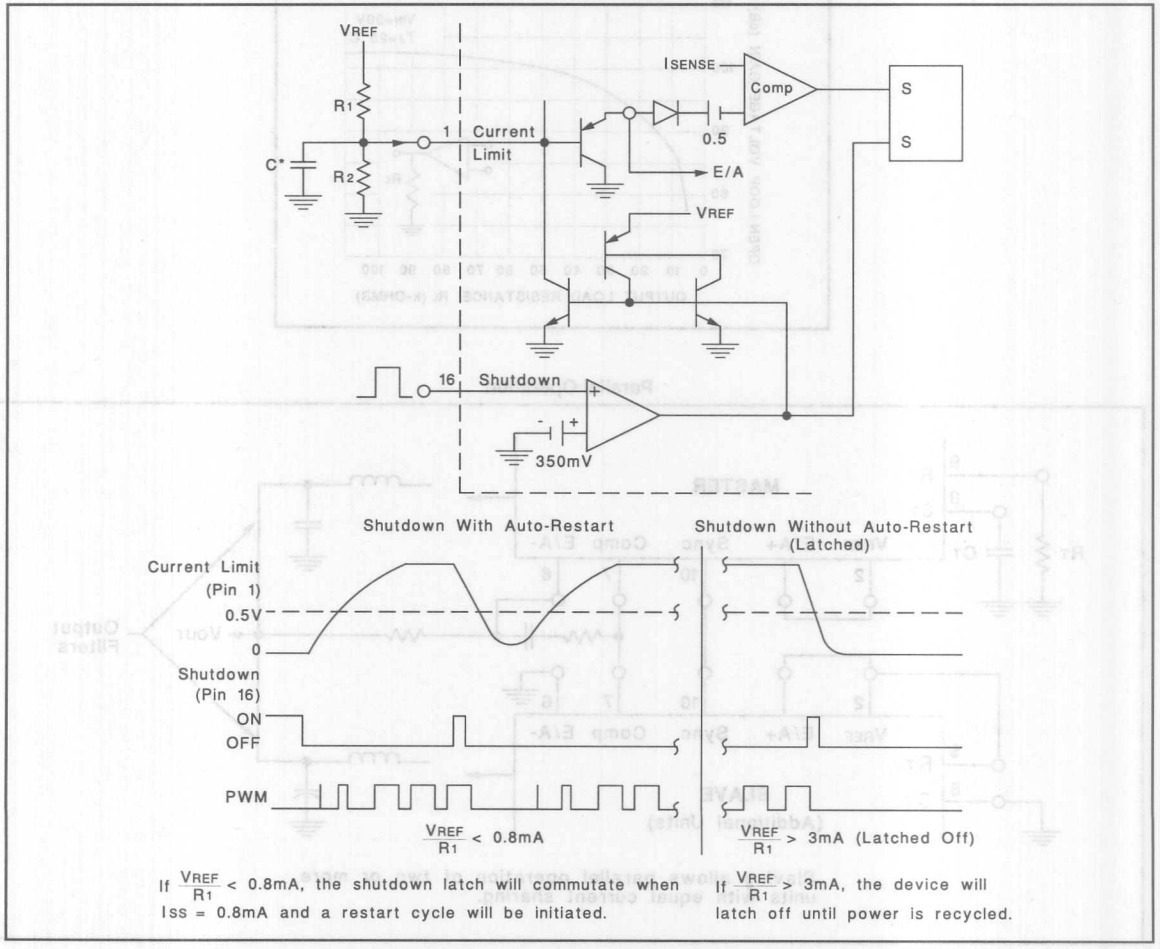


Slaving allows parallel operation of two or more units with equal current sharing.



Peak Current (Is) is determined by the formula: $Is = \dfrac{\frac{R2\ VREF}{R1 + R2} - 0.5}{3Rs}$

Soft Start and Shutdown /Restart Functions

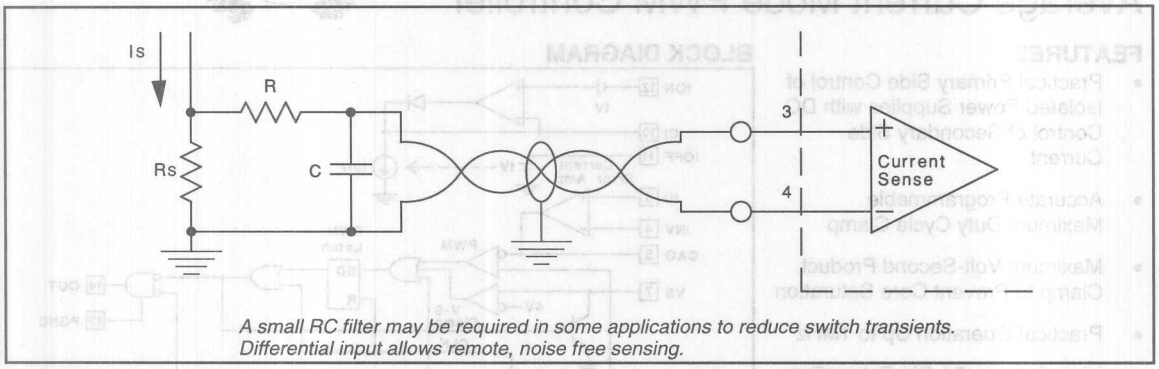


If $\frac{VREF}{R1}$ < 0.8mA, the shutdown latch will commutate when Iss = 0.8mA and a restart cycle will be initiated.

If $\frac{VREF}{R1}$ > 3mA, the device will latch off until power is recycled.

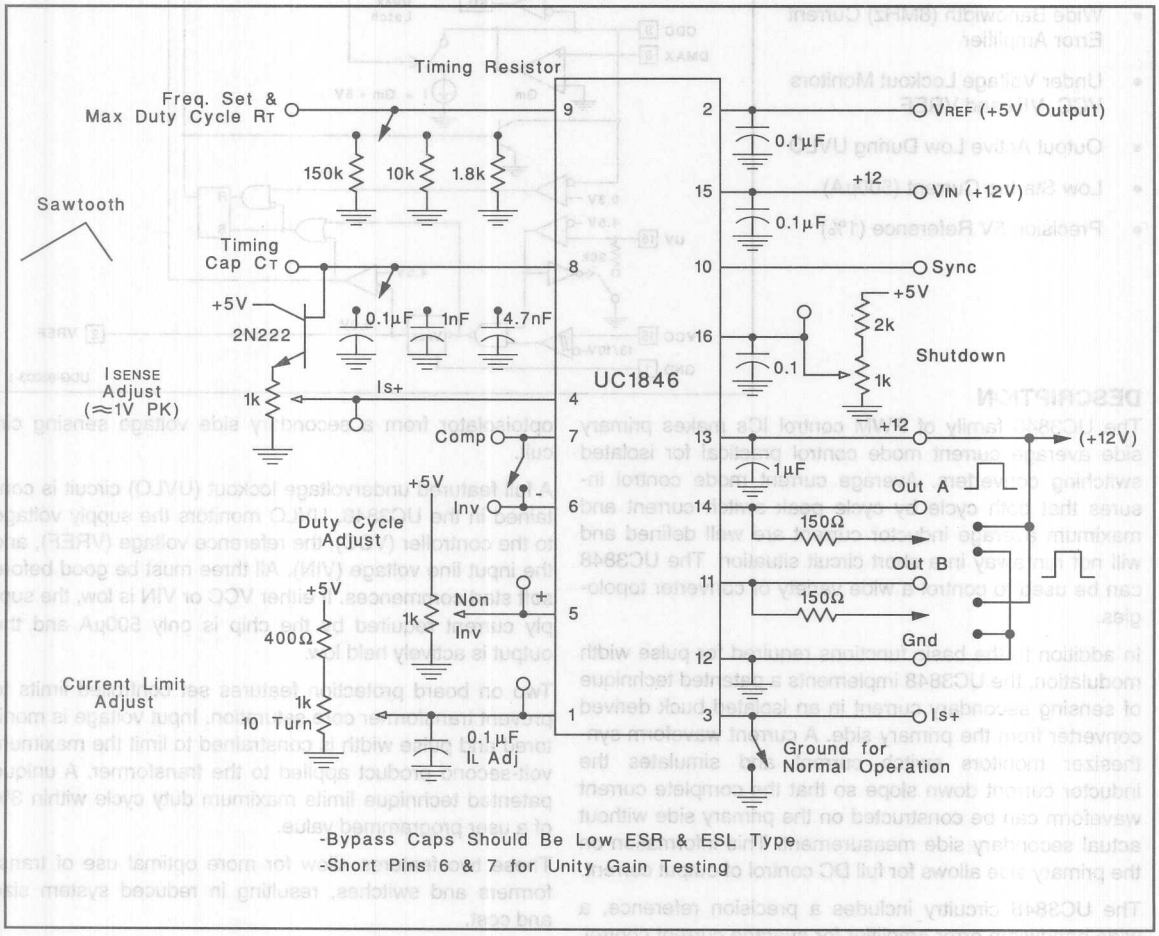
APPLICATIONS DATA (cont.)

Current Sense Amp Connection



A small RC filter may be required in some applications to reduce switch transients. Differential input allows remote, noise free sensing.

UC1846 Open Loop Test Circuit



-Bypass Caps Should Be Low ESR & ESL Type
-Short Pins 6 & 7 for Unity Gain Testing

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

UNITRODE

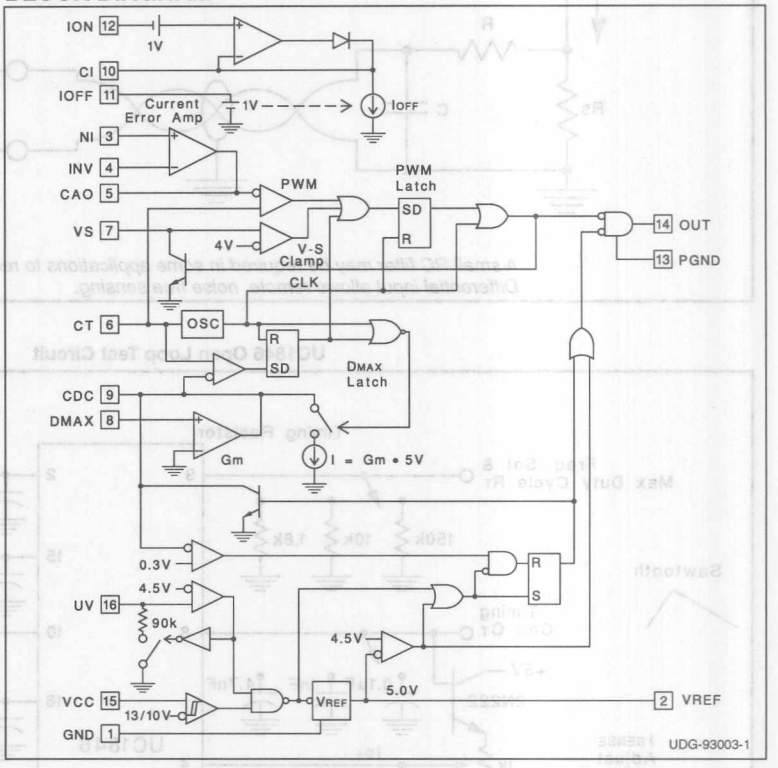
UC1848
UC2848
UC3848

Average Current Mode PWM Controller

FEATURES

- Practical Primary Side Control of Isolated Power Supplies with DC Control of Secondary Side Current
- Accurate Programmable Maximum Duty Cycle Clamp
- Maximum Volt-Second Product Clamp to Prevent Core Saturation
- Practical Operation Up to 1MHz
- High Current (2A Pk) Totem Pole Output Driver
- Wide Bandwidth (8MHz) Current Error Amplifier
- Under Voltage Lockout Monitors VCC, VIN and VREF
- Output Active Low During UVLO
- Low Startup Current (500µA)
- Precision 5V Reference (1%)

BLOCK DIAGRAM



DESCRIPTION

The UC3848 family of PWM control ICs makes primary side average current mode control practical for isolated switching converters. Average current mode control insures that both cycle by cycle peak switch current and maximum average inductor current are well defined and will not run away in a short circuit situation. The UC3848 can be used to control a wide variety of converter topologies.

In addition to the basic functions required for pulse width modulation, the UC3848 implements a patented technique of sensing secondary current in an isolated buck derived converter from the primary side. A current waveform synthesizer monitors switch current and simulates the inductor current down slope so that the complete current waveform can be constructed on the primary side without actual secondary side measurement. This information on the primary side allows for full DC control of output current.

The UC3848 circuitry includes a precision reference, a wide bandwidth error amplifier for average current control, an oscillator to generate the system clock, latching PWM comparator and logic circuits, and a high current output driver. The current error amplifier easily interfaces with an optoisolator from a secondary side voltage sensing circuit.

A full featured undervoltage lockout (UVLO) circuit is contained in the UC3848. UVLO monitors the supply voltage to the controller (VCC), the reference voltage (VREF), and the input line voltage (VIN). All three must be good before soft start commences. If either VCC or VIN is low, the supply current required by the chip is only 500µA and the output is actively held low.

Two on board protection features set controlled limits to prevent transformer core saturation. Input voltage is monitored and pulse width is constrained to limit the maximum volt-second product applied to the transformer. A unique patented technique limits maximum duty cycle within 3% of a user programmed value.

These two features allow for more optimal use of transformers and switches, resulting in reduced system size and cost.

Patents embodied in the UC3848 belong to Lambda Electronics Incorporated and are licensed for use in applications employing these devices.

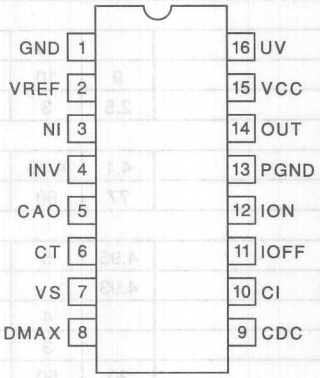
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Pin 15) 22V
Output Current, Source or Sink (Pin 14)
DC 0.5A
Pulse (0.5µs) 2.2A
Power Ground to Ground (Pin 1 to Pin 13) . . . . . ±0.2V
Analog Input Voltages
(Pins 3, 4, 7, 8, 12, 16) . . . . . -0.3 to 7V
Analog Input Currents, Source or Sink
(Pins 3, 4, 7, 8, 11, 12, 16) 1mA
Analog Output Currents, Source or Sink (Pins 5 & 10) . . . 5mA
Power Dissipation at T_A = 60°C 1W
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering 10 seconds) . . . . . +300°C

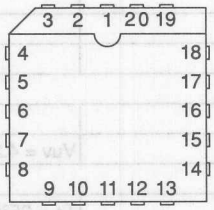
Notes: All voltages are with respect to ground (DIL and SOIC pin 1). Currents are positive into the specified terminal. Pin numbers refer to the 16 pin DIL and SOIC packages. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAMS

DIL-16, SOIC-16
(Top View)
J, N, or DW Pack-



PLCC-20 & LCC-20
(Top View)
Q & L Packages



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
GND	2
VREF	3
NI	4
INV	5
N/C	6
CAO	7
CT	8
VS	9
DMAX	10
N/C	11
CDC	12
CI	13
IOFF	14
ION	15
N/C	16
PGND	17
OUT	18
VCC	19
UV	20

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, all specifications are over the junction temperature range of −55°C to +125°C for the UC1848, −40°C to +85°C for the UC2848, and 0°C to +70°C for the UC3848. Test conditions are: VCC = 12V, CT = 400pF, CI = 100pF, IOFF = 100µA, CDC = 100nF, Cvs = 100pF, and Ivs = 400µA, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Real Time Current Waveform Synthesizer					
Ion Amplifier					
Offset Voltage		0.95	1	1.05	V
Slew Rate (Note 1)		20	25		V/µs
Iib			-2	-20	µA
IOFF Current Mirror					
Input Voltage		0.95	1	1.05	V
Current Gain		0.9	1	1.1	A/A
Current Error Amplifier					
AVOL		60	100		dB
Vio	12V ≤ VCC ≤ 20V, 0V ≤ VCM ≤ 5V			10	mV
Iib			-0.5	-3	µA
Voh	Io = −200µA	3	3.3		V
Vol	Io = 200µA		0.3	0.6	V
Source Current	Vo = 1V	1.4	1.6	2.0	mA
GBW Product	f = 200kHz	5	8		MHz
Slew Rate (Note 1)		8	10		V/µs

Note 1: Guaranteed by design.

ELECTRICAL CHARACTERISTICS (cont.): Unless otherwise stated, all specifications are over the junction temperature range of 0°C to +125°C for the UC1848, –40°C to +85°C for the UC2848, and 0°C to +70°C for the UC3848. Test conditions are: VCC = 12V, CT = 400pF, CI = 100pF, IOFF = 100µA, CDC = 100nF, Cvs = 100pF, and Ivs = 400µA, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator					
Frequency	T_A = 25°C	240	250	260	kHz
		235		265	kHz
Ramp Amplitude		1.5	1.65	1.8	V
Duty Cycle Clamp					
Max Duty Cycle	$V(D_{MAX}) = 0.75 \bullet V_{REF}$	73.5	76.5	79.5	%
Volt Second Clamp					
Max On Time		900		1100	ns
VCC Comparator					
Turn-on Threshold			13	14	V
Turn-off Threshold		9	10		V
Hysteresis		2.5	3	3.5	V
UV Comparator					
Turn-on Threshold		4.1	4.35	4.6	V
$R_{HYSTERESIS}$	Vuv = 4.2V	77	90	103	kΩ
Reference					
VREF	T_A = 25°C	4.95	5	5.05	V
	0 < Io < 10mA, 12 < VCC < 20	4.93		5.07	V
Line Regulation	12 < V_{CC} < 20V		4	15	mV
Load Regulation	0 < Io < 10mA		3	15	mV
Short Circuit Current	V_{REF} = 0V	30	50	70	mA
Output Stage					
Rise & Fall Time (Note 1)	CI = 1nF		20	45	ns
Output Low Saturation	Io = 20mA		0.25	0.4	V
	Io = 200mA		1.2	2.2	V
Output High Saturation	Io = -200mA		2.0	3.0	V
UVLO Output Low Saturation	Io = 20mA		0.8	1.2	V
Icc					
I_{START}	VCC = 12V		0.2	0.4	mA
Icc (pre-start)	VCC = 15V, V(UV) = 0		0.5	1	mA
Icc (run)			22	26	mA

Note 1: Guaranteed by design.

UNDERVOLTAGE LOCKOUT

The Under Voltage Lockout block diagram is shown in Figure 1. The VCC comparator monitors chip supply voltage. Hysteretic thresholds are set at 13V and 10V to facilitate off-line applications. If the VCC comparator is low, ICC is low (<500µA) and the output is low.

The UV comparator monitors input line voltage (V_{IN}). A pair of resistors divides the input line to UV. Hysteretic input line thresholds are programmed by Rv1 and Rv2. The thresholds are

$V_{IN}(on) = 4.35V \bullet (1 + Rv1/Rv2')$ and

$V_{IN}(off) = 4.35V \bullet (1 + Rv1/Rv2)$ where

$Rv2' = Rv2||90k$.

The resulting hysteresis is

$V_{IN}(hys) = 4.35V \bullet Rv1 / 90k$.

When the UV comparator is low, Icc is low (500µA) and the output is low.

UNDERVOLTAGE LOCKOUT (cont.)

When both the UV and VCC comparators are high, the internal bias circuitry for the rest of the chip is activated. The CDC pin (see discussion on Maximum Duty Cycle Control and Soft Start) and the Output are held low until VREF exceeds the 4.5V threshold of the VREF comparator. When VREF is good, control of the output driver is transferred to the PWM circuitry and CDC is allowed to charge.

If any of the three UVLO comparators go low, the UVLO latch is set, the output is held low, and CDC is discharged. This state will be maintained until all three comparators are high and the CDC pin is fully discharged.

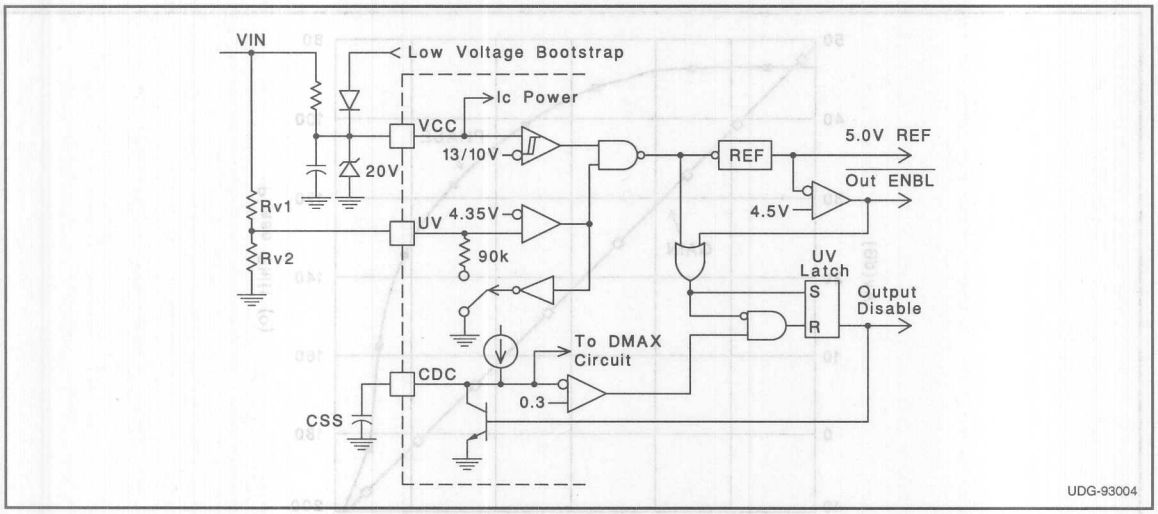


Figure 1: Under Voltage Lockout

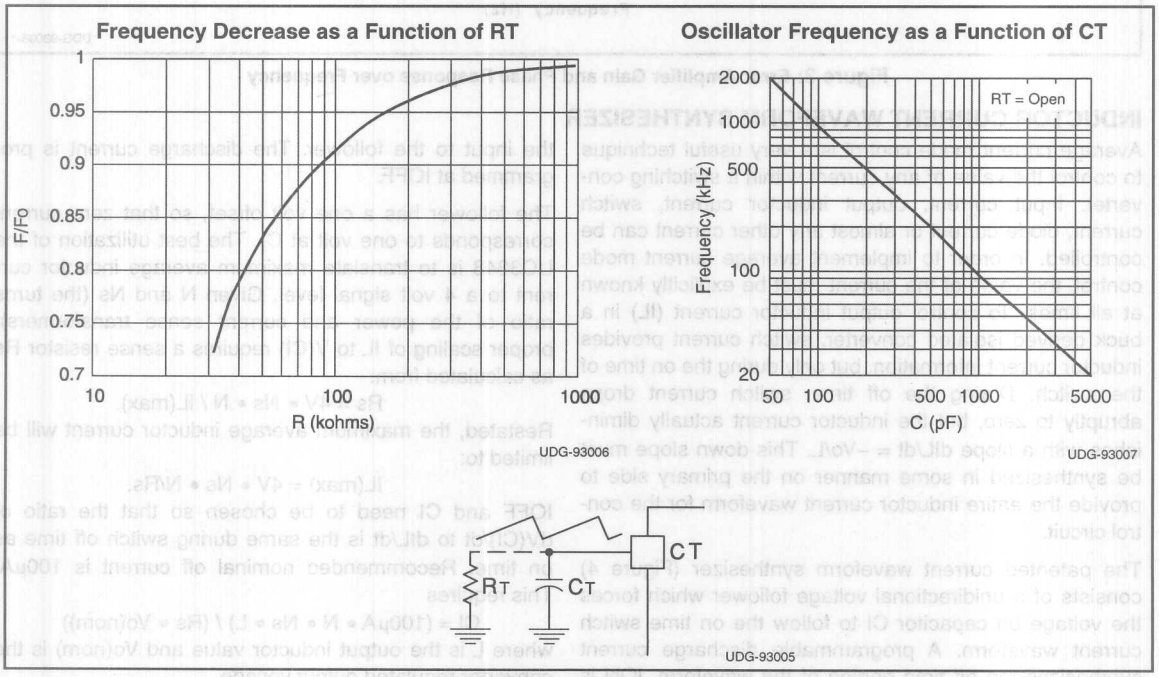


Figure 2: Oscillator Frequency

OSCILLATOR

A capacitor from the CT pin to GND programs oscillator frequency, as shown in Figure 2. Frequency is determined by:

$$F = 1 / (10k \bullet CT).$$

The sawtooth wave shape is generated by a charging current of 200µA and a discharge current of 1800µA. The discharge time of the sawtooth is guaranteed dead time for the output driver. If the maximum duty cycle control is defeated by connecting DMAX to VREF, the maximum duty cycle is limited by the oscillator to 90%. If an adjustment is required, an additional trim resistor RT from CT to Ground can be used to adjust the oscillator frequency. RT should not be less than 40kohms. This will allow up to a 22% decrease in frequency.

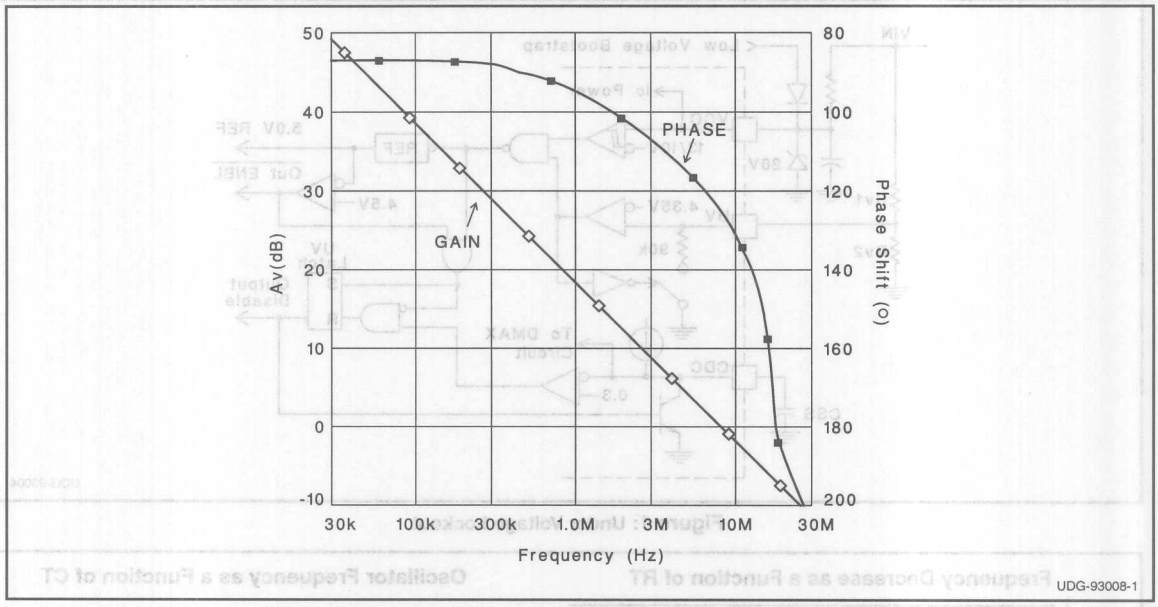


Figure 3: Error Amplifier Gain and Phase Response over Frequency

INDUCTOR CURRENT WAVEFORM SYNTHESIZER

Average current mode control is a very useful technique to control the value of any current within a switching converter. Input current, output inductor current, switch current, diode current or almost any other current can be controlled. In order to implement average current mode control, the value of the current must be explicitly known at all times. To control output inductor current (IL) in a buck derived isolated converter, switch current provides inductor current information, but only during the on time of the switch. During the off time, switch current drops abruptly to zero, but the inductor current actually diminishes with a slope dIL/dt = –Vo/L. This down slope must be synthesized in some manner on the primary side to provide the entire inductor current waveform for the control circuit.

The patented current waveform synthesizer (Figure 4) consists of a unidirectional voltage follower which forces the voltage on capacitor CI to follow the on time switch current waveform. A programmable discharge current synthesizes the off time portion of the waveform. ION is the input to the follower. The discharge current is programmed at IOFF.

The follower has a one volt offset, so that zero current corresponds to one volt at CI. The best utilization of the UC3848 is to translate maximum average inductor current to a 4 volt signal level. Given N and Ns (the turns ratio of the power and current sense transformers), proper scaling of IL to V(CI) requires a sense resistor Rs as calculated from:

$$Rs = 4V \bullet Ns \bullet N / IL(max).$$

Restated, the maximum average inductor current will be limited to:

$$IL(max) = 4V \bullet Ns \bullet N/Rs.$$

IOFF and CI need to be chosen so that the ratio of dV(CI)/dt to dIL/dt is the same during switch off time as on time. Recommended nominal off current is 100µA. This requires

$$CI = (100\mu A \bullet N \bullet Ns \bullet L) / (Rs \bullet Vo(nom))$$

where L is the output inductor value and Vo(nom) is the converter regulated output voltage.

INDUCTOR CURRENT WAVEFORM SYNTHESIZER (cont.)

There are several methods to program IOFF. If accurate average current control is required during short circuit operation, IOFF must track output voltage. The method shown in Figure 4 derives a voltage proportional to VIN • D (Duty Cycle). (In a buck converter, output voltage is proportional to VIN • D.) A resistively loaded diode connection to the bootstrap winding yields a square wave whose amplitude is proportional to VIN and is duty cycle modulated by the control circuit. Averaging this waveform with a filter generates a primary side replica of secondary regulated Vo. A single pole filter is shown, but in practice a two or three pole filter provides better transient response. Filtered voltage is converted by ROFF to a current to the IOFF pin to control CI down slope.

If the system is not sensitive to short circuit requirements, Figure 5 shows the simplest method of downslope generation: a single resistor (ROFF = 40k) from IOFF to VREF. The discharge current is then 100µA. The disadvantage to this approach is that the synthesizer continues to generate a down slope when the switch is off even during short circuit conditions. Actual inductor down slope is closer to zero during a short circuit. The penalty is that the average current is understated by an amount approximately equal to the nominal inductor ripple current. Output short circuit is therefore higher than the designed maximum output current.

A third method of generating IOFF is to add a second winding to the output inductor core (Figure 6). When the power switch is off and inductor current flows in the free wheeling diode, the voltage across the inductor is equal to the output voltage plus the diode drop. This voltage is then transformed by the second winding to the primary side of the converter. The advantages to this approach are its inherent accuracy and bandwidth. Winding the second coil on the output inductor core while maintaining the required isolation makes this a more costly solution. In the example, ROFF = Vo / 100µA. The 4 • ROFF resistor is added to compensate the one volt input level of the IOFF pin. Without this compensation, a minor current foldback behavior will be observed.

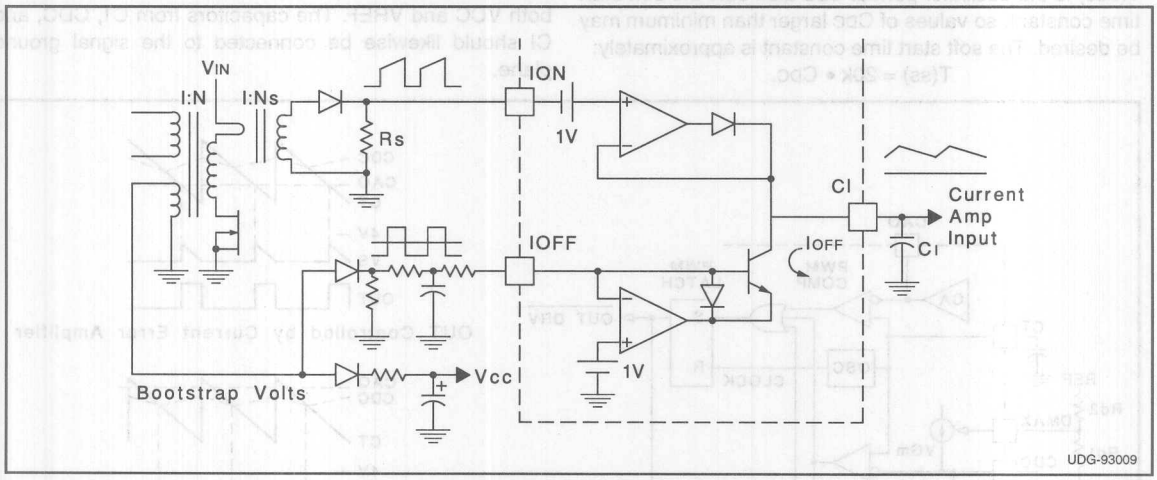


Figure 4: Inductor Current Waveform Synthesizer

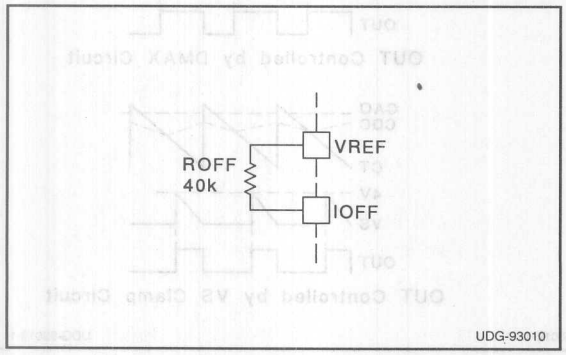


Figure 5: Fixed IOFF

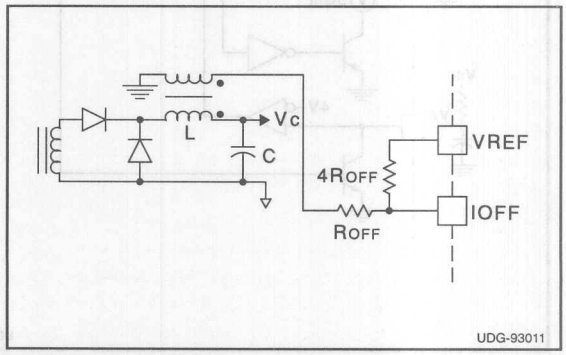


Figure 6: Second Inductor Winding Generation of IOFF

MAXIMUM VOLT-SECOND CIRCUIT

A maximum volt-second product can be programmed by a resistor (Rvs) from VS to VIN and a capacitor (Cvs) from VS to ground (Figure 7). VS is discharged while the switch is off. When the output turns on, VS is allowed to charge. Since the threshold of the VS comparator is much less than VIN, the charging profile at Vs will be essentially linear. If VS crosses the 4.0V threshold before the PWM turns the output off, the VS comparator will turn the output off for the remainder of the cycle. The maximum volt-second product is

$$V_{IN} \bullet T_{ON}(max) = 4.0V \bullet Rvs \bullet Cvs.$$

MAXIMUM DUTY CYCLE AND SOFT START

A patented technique is used to accurately program maximum duty cycle. Programming is accomplished by a divider from VREF to DMAX (Figure 7). The value programmed is:

$$D(max) = Rd1 / (Rd1 + Rd2).$$

For proper operation, the integrating capacitor, C_{DC}, should be larger than $C_{DC}(min) > T(osc) / 80k$, where T(osc) is the oscillator period. C_{DC} also sets the soft start time constant, so values of C_{DC} larger than minimum may be desired. The soft start time constant is approximately:

$$T(ss) = 20k \bullet C_{DC}.$$

GROUND PLANES

The output driver on the UC3848 is capable of 2A peak currents. Careful layout is essential for correct operation of the chip. A ground plane must be employed (Figure 8). A unique section of the ground plane must be designated for high di/dt currents associated with the output stage. This point is the power ground to which to PGND pin is connected. Power ground can be separated from the rest of the ground plane and connected at a single point, although this is not strictly necessary if the high di/dt paths are well understood and accounted for. VCC should be bypassed directly to power ground with a good high frequency capacitor. The sources of the power MOSFET should connect to power ground as should the return connection for input power to the system and the bulk input capacitor. The output should be clamped with a high current Schottky diode to both VCC and PGND. Nothing else should be connected to power ground.

VREF should be bypassed directly to the signal portion of the ground plane with a good high frequency capacitor. Low esr/esl ceramic 1µF capacitors are recommended for both VCC and VREF. The capacitors from CT, CDC, and CI should likewise be connected to the signal ground plane.

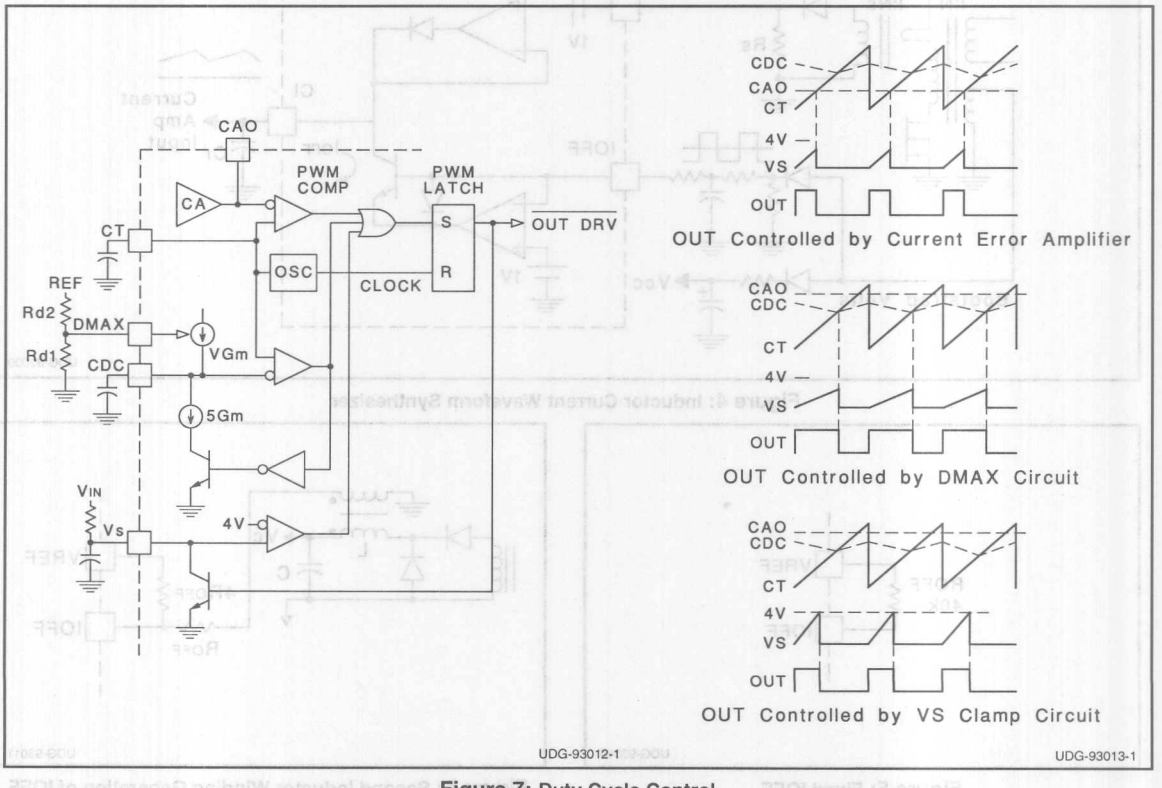


Figure 7: Duty Cycle Control

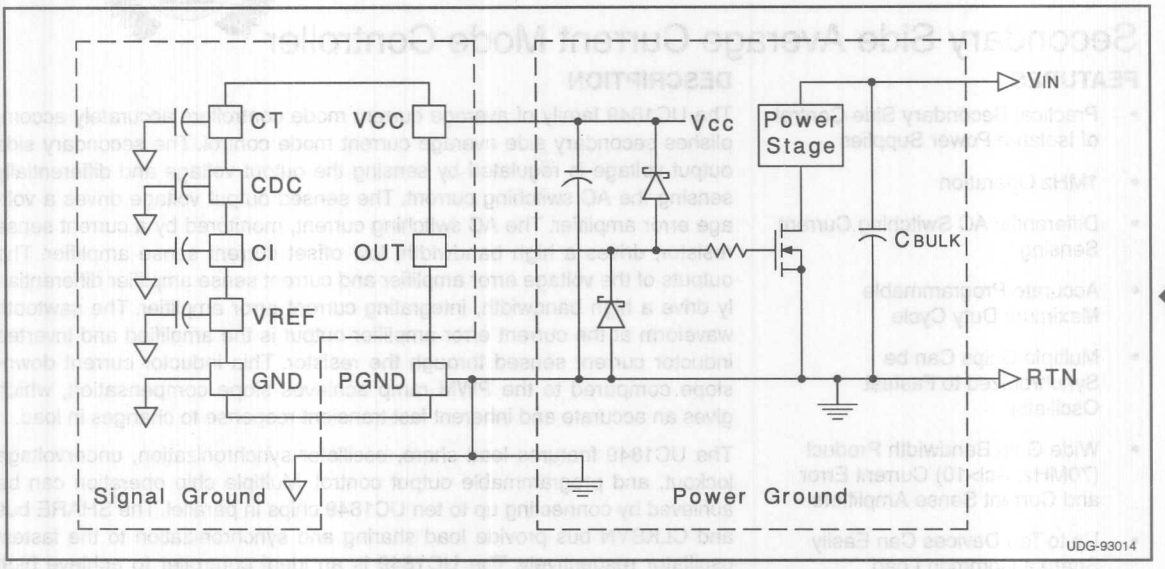


Figure 8: Ground Plane Considerations

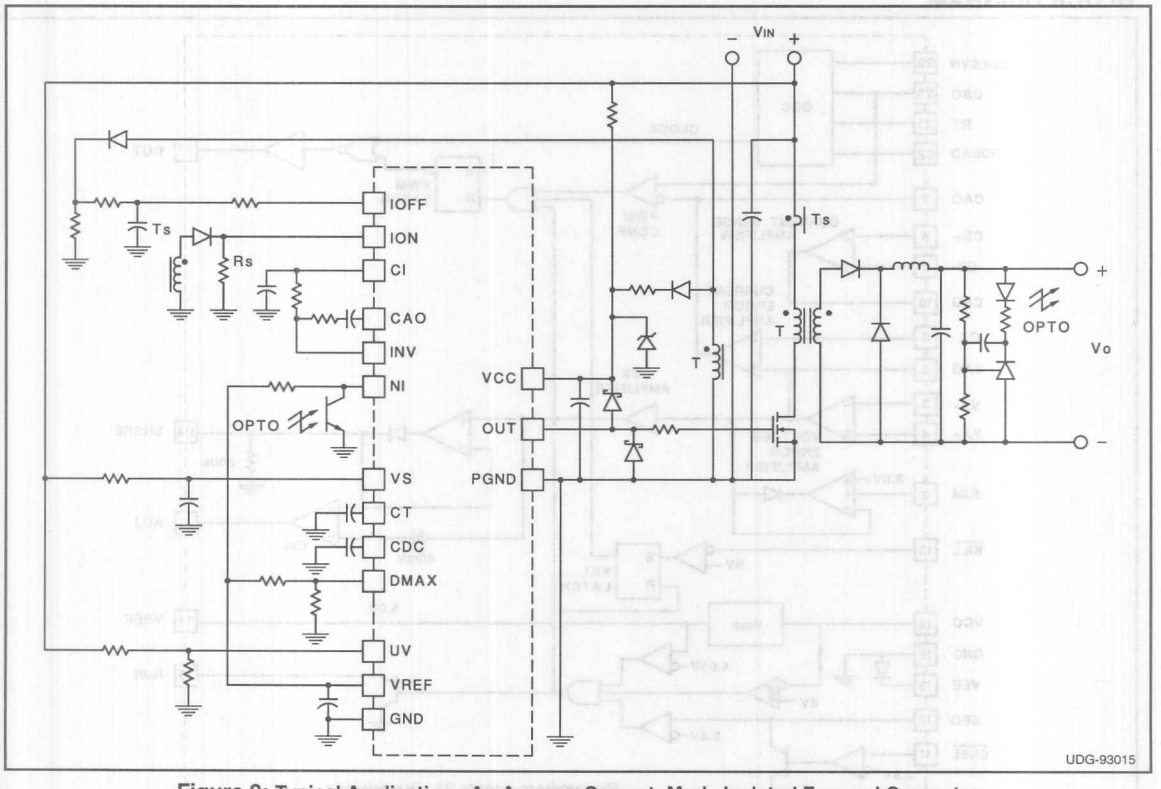


Figure 9: Typical Application - An Average Current -Mode Isolated Forward Converter

UNITRODE CORPORATION
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Secondary Side Average Current Mode Controller

FEATURES

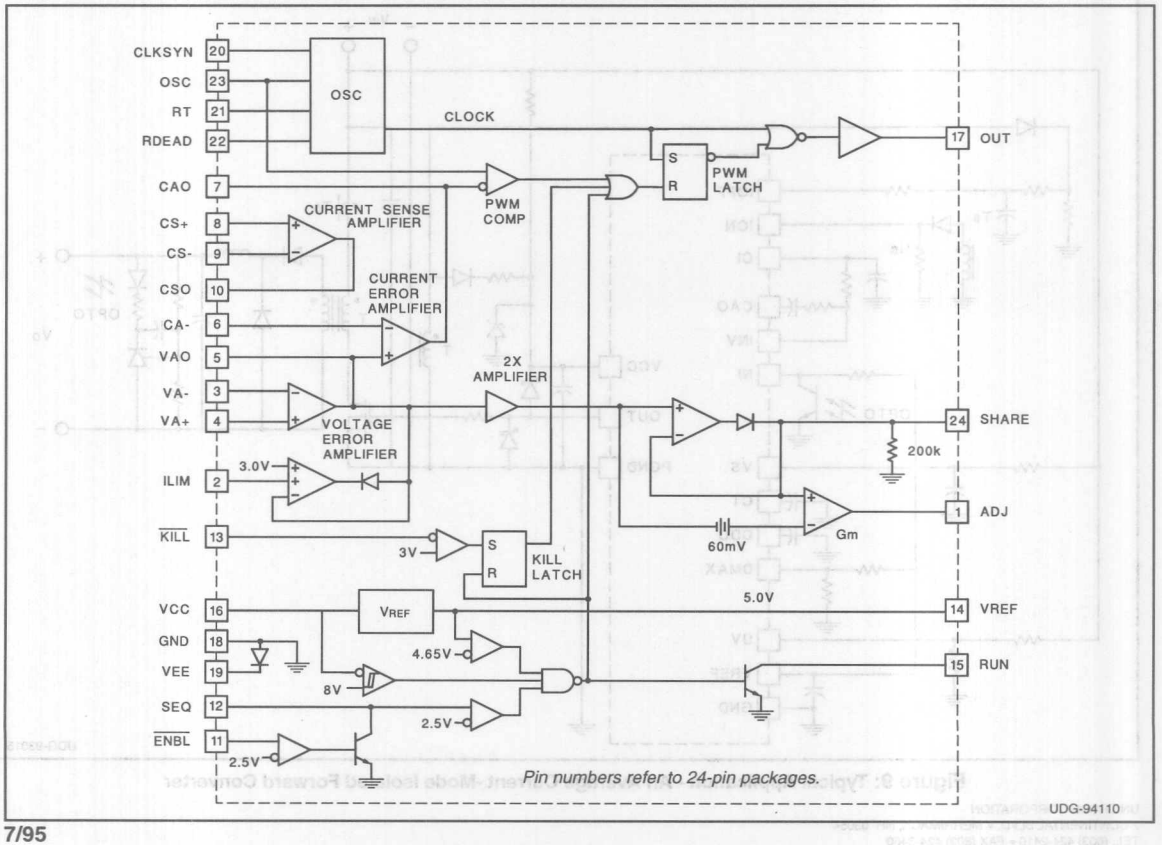
- Practical Secondary Side Control of Isolated Power Supplies
- 1MHz Operation
- Differential AC Switching Current Sensing
- Accurate Programmable Maximum Duty Cycle
- Multiple Chips Can be Synchronized to Fastest Oscillator
- Wide Gain Bandwidth Product (70MHz, Acl>10) Current Error and Current Sense Amplifiers
- Up to Ten Devices Can Easily Share a Common Load

DESCRIPTION

The UC1849 family of average current mode controllers accurately accomplishes secondary side average current mode control. The secondary side output voltage is regulated by sensing the output voltage and differentially sensing the AC switching current. The sensed output voltage drives a voltage error amplifier. The AC switching current, monitored by a current sense resistor, drives a high bandwidth, low offset current sense amplifier. The outputs of the voltage error amplifier and current sense amplifier differentially drive a high bandwidth, integrating current error amplifier. The sawtooth waveform at the current error amplifier output is the amplified and inverted inductor current sensed through the resistor. This inductor current downslope compared to the PWM ramp achieves slope compensation, which gives an accurate and inherent fast transient response to changes in load.

The UC1849 features load share, oscillator synchronization, undervoltage lockout, and programmable output control. Multiple chip operation can be achieved by connecting up to ten UC1849 chips in parallel. The SHARE bus and CLKSYN bus provide load sharing and synchronization to the fastest oscillator respectively. The UC1849 is an ideal controller to achieve high power, secondary side average current mode control.

BLOCK DIAGRAM



7/95

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (VCC) 20V
Output Current Source or Sink 0.3A
Analog Input Voltages .....–0.3V to 7V
ILIM, KILL, SEQ, ENBL, RUN .....–0.3V to 7 V
CLKSYN Current Source 12mA
RUN Current Sink 15mA
SEQ Current Sink 20mA
RDEAD Current Sink 20mA
Share Bus Voltage (voltage with respect to GND) . . .0V to 6.2V
ADJ Voltage (voltage with respect to GND) .....0.9V to 6.3V
VEE (voltage with respect to GND) .....–1.5V
Storage Temperature .....–65°C to +150°C
Junction Temperature .....–65°C to +150°C
Lead Temperature (Soldering, 10 sec.) .....+300°C

All voltages with respect to VEE except where noted; all currents are positive into, negative out of the specified terminal.
Consult Packaging Section of Databook for thermal limitations and considerations of packages.

RECOMMENDED OPERATING CONDITIONS

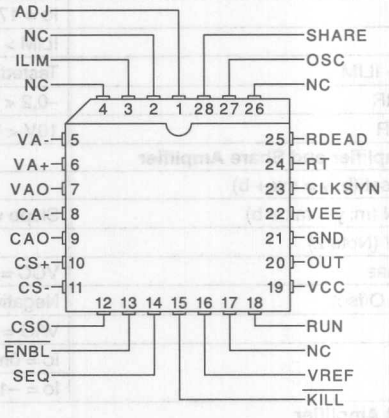
Input Voltage 8V to20V
Sink/Source Output Current 250mA
Timing Resistor (RT) .....1k to 200k
Timing Capacitor (CT) .....75pF to 2nF

CONNECTION DIAGRAMS

DIL-24, SOIC-24, TSSOP-24 (Top View)
J or N, DW, PW Packages



PLCC-28 (Top View)
Q Package



ELECTRICAL CHARACTERISTICS Unless otherwise stated these specifications apply for T_A = –55°C to +125°C for UC1849; –40°C to +85°C for UC2849; and 0°C to +70°C for UC3849; VCC = 12V, VEE = GND, Output no load, CT = 345pF, RT = 4530Ω, RDEAD = 511Ω, R_{CLKSYN} = 1k, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Current Sense Amplifier					
Ib			0.5	3	µA
Vio	TA = +25°C			3	mV
	Over Temperature			5	mV
Avo		60	90		dB
GBW (Note 2)	Acl = 1, RIN = 1k, CC = 15pF, f = 200kHz (Note 1)	4.5	7		MHz
Vol	Io = 1mA, Voltage above VEE		0.5		V
Voh	Io = 0mA		3.8		V
	Io = –1mA		3.5		V
CMRR	–0.2 < Vcm < 8V		80		dB
PSRR	10V < VCC < 20V		80		dB
Current Error Amplifier					
Ib			0.5	3	µA
Vio			3	20	mV

ELECTRICAL CHARACTERISTICS Unless otherwise stated these specifications apply for T_A = –55°C to +125°C for UC1849; –40°C to +85°C for UC2849; and 0°C to +70°C for UC3849; VCC = 12V, VEE = GND, Output no load, CT = 345pF, RT = 4530Ω, RDEAD = 511Ω, R_{CLKSYN} = 1k, T_A = T_J.

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
Current Error Amplifier (cont.)					
Avo		60	90		dB
GBW (Note 2)	Acl = 1, R_{IN} = 1k, CC=15pF, f=200kHz (Note 1)	4.5	7		MHz
Vol	Io = 1mA, Voltage above VEE		0.5		V
Voh	Io = 0mA		3.8		V
	Io = –1mA		3.5		V
CMRR	–0.2 < Vcm < 8V		80		dB
PSRR	10V < VCC < 20V		80		dB
Voltage Error Amplifier					
Ib			0.5	3	µA
Vio			2	5	mV
Avo		60	90		dB
GBW (Note 2)	f = 200kHz	4.5	7		MHz
Vol	Io = 175µA, Volts above VEE		0.3	0.6	V
Voh	ILIM > 3V	2.85	3	3.15	V
Voh - ILIM	Tested ILIM = 0.5V, 1.0V, 2.0V	–100		100	mV
CMRR	–0.2 < Vcm < 8V		80		dB
PSRR	10V < VCC < 20V		80		dB
2X Amplifier and Share Amplifier					
V offset (b; y = mx + b)				20	mV
GAIN (m; y = mx + b)	Slope with AV_{OUT} = 1V and 2V	1.98		2.02	V
GBW (Note 2)			100		kHZ
R_{SHARE}	VCC = 0, V_{SHARE}/I_{SHARE}		200		k
Total Offset	Negative supply is VEE, GND Open, VAO = GND	–75	0	75	mV
Vol	VAO = Voltage Amplifier Vol, Volts above VEE	0.2	0.45	0.6	V
Voh	Io = 0mA, ILIM = 3V, VAO = Voltage Amp Voh	5.7	6	6.3	V
	Io = –1mA, ILIM = 3V, VAO = Voltage Amp Voh	5.7	6	6.3	V
Adjust Amplifier					
Vio		40	60	80	mV
gm	I_{OUT}= –10µA to 10µA, V_{OUT} = 3.5V, C_{ADJ} = 1µF		–1		mS
Vol	I_{OUT} = 0	0.9	1	1.1	V
	I_{OUT} = 50µA	0.85	1	1.15	V
Voh	I_{OUT} = 0, V_{SHARE} = 6.5V	5.7	6	6.3	V
	I_{OUT} = –50µA, V_{SHARE} = 6.5V	5.7	6	6.3	V
Oscillator					
Frequency		450	500	550	kHz
Max Duty Cycle		80	85	90	%
OSC Ramp Amplitude		2	2.5	2.8	V
Clock Driver/SYNC (CLKSYN)					
Vol			0.02	0.2	V
Voh			3.6		V
	R_{CLKSYN} = 200Ω		3.2		V
I_{SOURCE}			25		mA
R_{CLKSYN}	VCC = 0, V_{CLKSYN}/I_{CLKSYN}		10		k
V_{TH}			1.5		V

ELECTRICAL CHARACTERISTICS (cont) Unless otherwise stated these specifications apply for T_A = –55°C to +125°C for UC1849; –40°C to +85°C for UC2849; and 0°C to +70°C for UC3849; VCC = 12V, VEE = GND, Output no load, CT = 345pF, RT = 4530Ω, RDEAD = 511Ω, R_{CLKSYN} = 1k, T_A = T_J.

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
VREF Comparator					
Turn-on threshold			4.65		V
Hysteresis			0.4		V
VCC Comparator					
Turn-on Threshold		7.9	8.3	8.7	V
Hysteresis			0.4		V
KILL Comparator					
Voltage Threshold			3		V
Sequence Comparator					
Voltage Threshold			2.5		V
SEQ SAT	Io = 10mA		0.25		V
Enable Comparator					
Voltage Threshold			2.5		V
RUN SAT	Io = 10mA		0.25		V
Reference					
VREF	T_A = 25°C	4.95	5	5.05	V
VREF	VCC = 15V	4.9		5.1	V
Line Regulation	10 < VCC < 20		3	15	mV
Load Regulation	0 < Io < 10mA		3	15	mV
Short Circuit I	VREF = 0V	30	60	90	mA
Output Stage					
Rise Time	C_L = 100pF		10	20	ns
Fall Time	C_L = 100pF		10	20	ns
Voh	VCC > 11V, Io = –10mA	8.0	8.4	8.8	V
	Io = –200mA	7.8			V
Vol	Io = 200mA			3.0	V
	Io = 10mA			0.5	V
Virtual Ground					
V_{GND}-VEE	VEE is externally supplied, GND is floating and used as Signal GND.	0.2	0.75		V
Icc					
Icc (run)			21	30	mA

Note 1: If a closed loop gain greater than 1 is used, the possible GBW will increase by a factor of ACL + 10; where ACL is the closed loop gain.

Note 2: Guaranteed by design. Not 100% tested in production.

Note 3: Unless otherwise specified all voltages are with respect to GND. Currents are positive into, negative out of the specified terminal.

PIN DESCRIPTIONS

ADJ: The output of the transconductance (gm = –1mS) amplifier adjusts the control voltage to maintain equal current sharing. The chip sensing the highest output current will have its output clamped to 1V. A resistor divider between VREF and ADJ drives the control voltage (VA+) for the voltage amplifier. Each slave unit's ADJ voltage increases (to a maximum of 6V) its control voltage (VA+) until its load current is equal to the master. The 60mV input offset on the gm amplifier guarantees that the unit sensing the highest load current is chosen as the master. The 60mV offset guarantees by design to be greater than the inherent offset of the gm amplifier and the buffer amplifier. While the 60mV offset represents an error in current sharing, the gain of the current and 2X amplifiers reduces it to only 30mV. This pin needs a 1µF capacitor to compensate the amplifier.

CA-: The inverting input to the current error amplifier. This amplifier needs a capacitor between CA- and CAO to set its dominant pole.

PIN DESCRIPTIONS (cont.)

CAO: The output of the current error amplifier which is internally clamped to 4V. It is internally connected to the inverting input of the PWM comparator.

CS-, CS+: The inverting and non-inverting inputs to the current sense amplifier. This amplifier is not internally compensated so the user must compensate externally to attain the highest GBW for the application.

CLKSYN: The clock and synchronization pin for the oscillator. This is a bidirectional pin that can be used to synchronize several chips to the fastest oscillator. Its input synchronization threshold is 1.4V. The CLKSYN voltage is 3.6V when the oscillator capacitor (CT) is being discharged, otherwise it is 0V. If the recommended synchronization circuit is not used, a 1k or lower value resistor from CLKSYN to GND may be needed to increase fall time on CLKSYN pin.

CSO: The output of the current sense amplifier which is internally clamped to 4V.

$\overline{\text{ENBL}}$: The active low input with a 2.5V threshold enables the output to switch. SEQ and RUN are driven low when $\overline{\text{ENBL}}$ is above its 2.5V threshold.

GND: The signal ground used for the voltage sense amplifier, current sense amplifier, current error amplifier, voltage reference, 2X amplifier, and share amplifier. The output sink transistor is wired directly to this pin.

KILL: The active low input with a 3.0V threshold stops the output from switching. Once this function is activated RUN must be cycled low by driving $\overline{\text{KILL}}$ above 3.0V and either resetting the power to the chip (VCC) or resetting the ENBL signal.

ILIM: A voltage on this pin programs the voltage error amplifier's Voh clamp. The voltage error amplifier output represents the average output current. The Voh clamp consequently limits the output current. If ILIM is tied to VREF, it defaults to 3.0V. A voltage less than 3.0V connected to ILIM clamps the voltage error amplifier at this voltage and consequently limits the maximum output current.

OSC: The oscillator ramp pin which has a capacitor (CT) to ground and a resistor (RDEAD) to the RDEAD pin programs its maximum duty cycle by programming a minimum dead time. The ramp oscillates between 1.2V to 3.4V when an RDEAD resistor is used. The maximum duty cycle can be increased by connecting RDEAD to OSC which changes the oscillator ramp to vary between 0.2V and 3.5V. In order to guarantee zero duty cycle in this configuration VEE should not be connected to GND.

The charge time is approximately $T_{CHARGE} = R_T \cdot C_T$ when the RDEAD resistor is used.

The dead time is approximately $T_{DISCHARGE} = 2 \cdot RDEAD \cdot C_T$.

(1) $$\text{Frequency} \approx \frac{1}{T_{CHARGE} + T_{DISCHARGE}}$$

(2) $$\text{Maximum Duty Cycle} \approx \frac{T_{CHARGE}}{T_{CHARGE} + T_{DISCHARGE}}$$

The C_T capacitance should be increased by approximately 40pF to account for parasitic capacitance.

OUT: The output of the PWM driver. It has an upper clamp of 8.5V. The peak current sink and source are 250mA. All UVLO, SEQ, ENBL, and $\overline{\text{KILL}}$ logic either enable or disable the output driver.

RDEAD: The pin that programs the maximum duty cycle by connecting a resistor between it and OSC. The maximum duty cycle is decreased by increasing this resistor value which increases the discharge time. The dead time, the time when the output is low, is $2 \cdot RDEAD \cdot C_T$. The C_T capacitance should be increased by approximately 40pF to account for parasitic capacitance.

RT: This pin programs the charge time of the oscillator ramp. The charge current is

$$\frac{VREF}{2 \cdot R_T}$$

The charge time is approximately $T_{CHARGE} \approx R_T \cdot C_T$ when the RDEAD resistor is used.

The dead time is approximately $T_{DISCHARGE} \approx 2 \cdot RDEAD \cdot C_T$.

RUN: This is an open collector logic output that signifies when the chip is operational. RUN is pulled high to VREF through an external resistor when VCC is greater than 8.4V, VREF is greater than 4.65V, SEQ is greater than 2.5V, and $\overline{\text{KILL}}$ lower than 3.0V. RUN connected to the VA+ pin and to a capacitor to ground adds an RC rise time on the VA+ pin initiating a soft start.

SEQ: The sequence pin allows the sequencing of startup for multiple units. A resistor between VREF and SEQ and a capacitor between SEQ and GND creates a unique RC rise time for each unit which sequences the output startup.

SHARE: The nearly DC voltage representing the average output current. This pin is wired directly to all SHARE pins and is the load share bus.

VA+, VA-: The inverting and non-inverting inputs to the voltage error amplifier.

VAO: The output of the voltage error amplifier. Its Voh is clamped with the ILIM pin.

PIN DESCRIPTIONS (cont.)

VCC: The input voltage of the chip. The chip is operational between 8.4V and 20V.

VEE: The negative supply to the chip which powers the lower voltage rail for all amplifiers. The chip is operational if VEE is connected to GND or if GND is floating. When voltage is applied externally to VEE, GND becomes a virtual ground because of an internal diode between VEE and GND. The GND current flows through the forward biased diode and out VEE. GND is always the signal ground from which the voltage reference and all amplifier inputs are referenced.

VREF: The reference voltage equal to 5.0V.

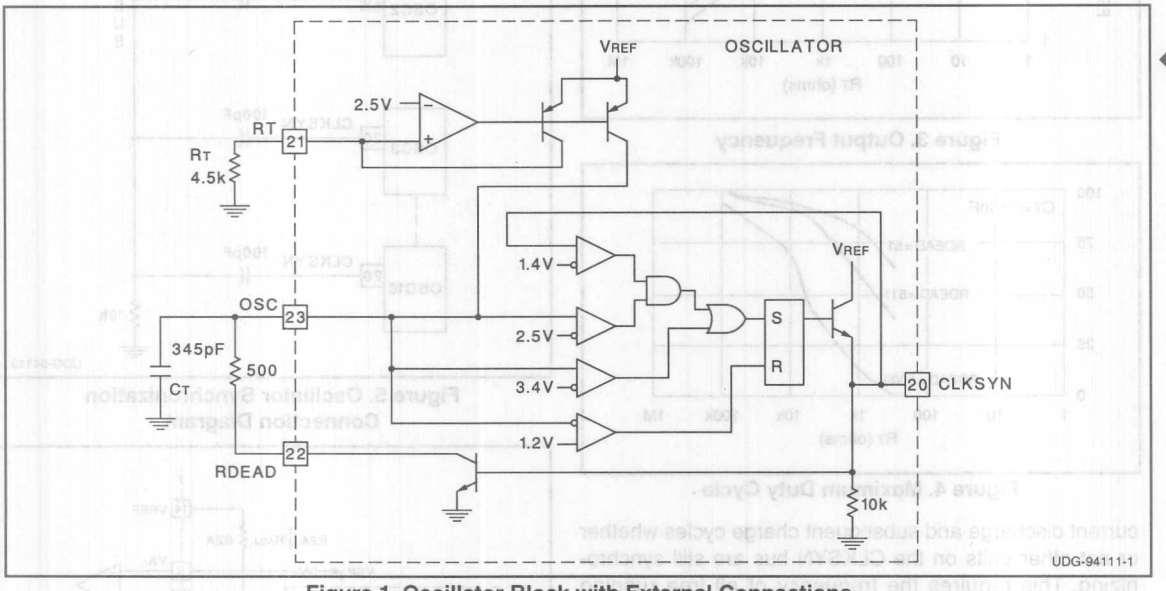


Figure 1. Oscillator Block with External Connections

CIRCUIT BLOCK DESCRIPTION:

PWM Oscillator: The oscillator block diagram with external connections is shown in Figure 1. A resistor (R_T) connected to pin RT sets the linear charge current;

$$I_{RT} \approx \frac{2.5V}{R_T}$$

The timing capacitor (C_T) is linearly charged with the charge current forcing the OSC pin to charge to a 3.4V threshold. After exceeding this threshold, the RS flip-flop is set driving CLKSYN high and RDEAD low which discharges C_T. This discharge time with the RC time delay of 2 • C_T • RDEAD is the minimum output low time. OSC continues to discharge until it reaches a 1.2V threshold and resets the RS flip-flop which repeats the charging sequence as shown in Figure 2. Equations to approximate frequency and maximum duty cycle are listed under the OSC pin description. Figure 3 and 4 graphs show measured variation of frequency and maximum duty cycle with varying RT, CT, and RDEAD component values.

As shown in Figure 5, several oscillators are synchronized to the highest free running frequency by connecting 100pF capacitors in series with each CLKSYN pin and connecting the other side of the capacitors together forming the CLKSYN bus. The CLKSYN bus is then pulled down to ground with a resistance of approximately 10k. Referring to Figure1, the synchronization threshold is 1.4V. The oscillator blanks any synchronization pulse that occurs when OSC is below 2.5V. This allows units, once they discharge below 2.5V, to continue through the

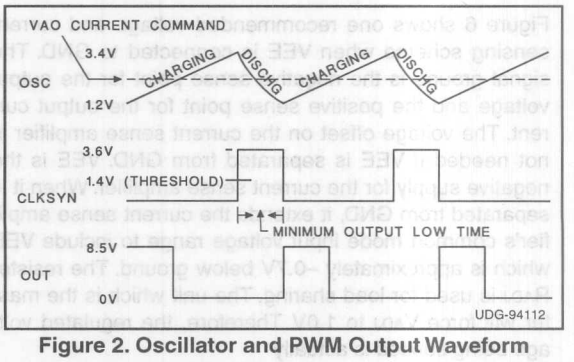


Figure 2. Oscillator and PWM Output Waveform

CIRCUIT BLOCK DESCRIPTION (cont.)

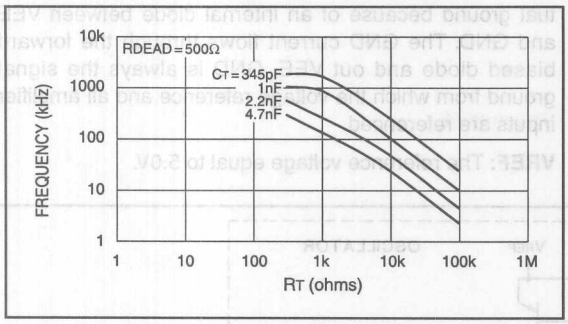


Figure 3. Output Frequency

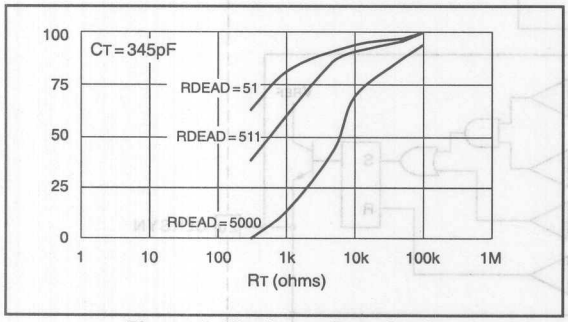


Figure 4. Maximum Duty Cycle

current discharge and subsequent charge cycles whether or not other units on the CLKSYN bus are still synchronizing. This requires the frequency of all free running oscillators to be within 40% of each other to guarantee synchronization.

Grounds, Voltage Sensing and Current Sensing: The voltage is sensed directly at the load. Proper load sharing requires the same sensed voltage for each power supply connected in parallel. Referring to Figure 6, the positive sense voltage (VSP) connects to the voltage error amplifier inverting terminal (VA-), the return lead for the on-chip reference is used as the negative sense (VSM). The current is sensed across the shunt resistor, Rs.

Figure 6 shows one recommended voltage and current sensing scheme when VEE is connected to GND. The signal ground is the negative sense point for the output voltage and the positive sense point for the output current. The voltage offset on the current sense amplifier is not needed if VEE is separated from GND. VEE is the negative supply for the current sense amplifier. When it is separated from GND, it extends the current sense amplifier's common mode input voltage range to include VEE which is approximately –0.7V below ground. The resistor R_{ADJ} is used for load sharing. The unit which is the master will force V_{ADJ} to 1.0V. Therefore, the regulated voltage being sensed is actually

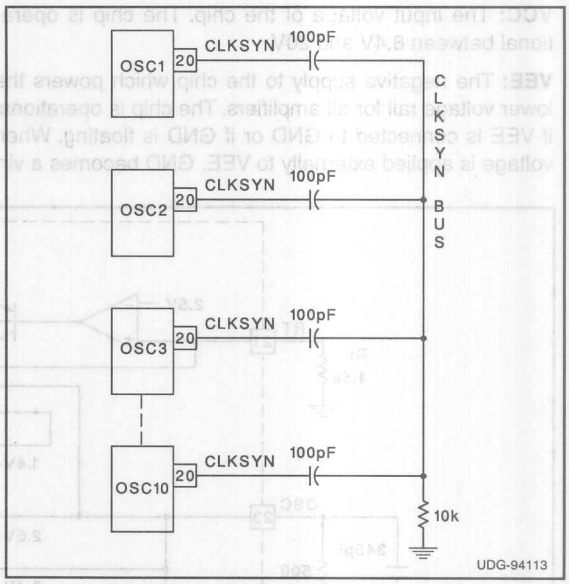


Figure 5. Oscillator Synchronization Connection Diagram

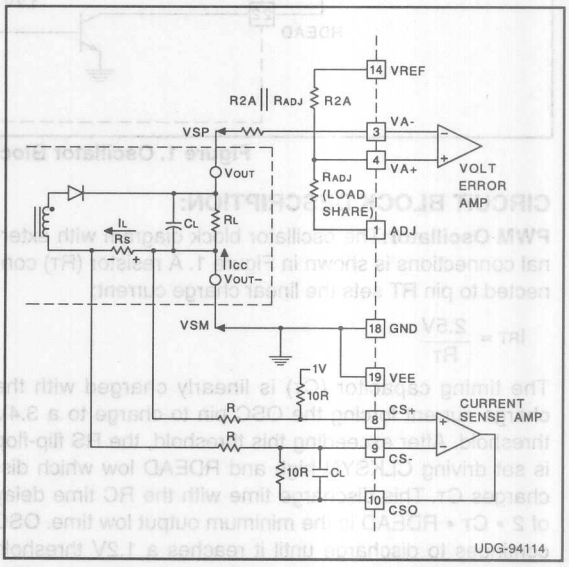


Figure 6. Voltage and Current Sense VEE Tied to GND

$$V_{SP} - V_{SM} = (V_{REF} - V_{ADJ}) \bullet \left(\frac{R_{ADJ}}{R1 + R_{ADJ}}\right) + V_{ADJ}$$

V_{SM} = 0V, V_{ADJ} = 1V (master), V_{REF} = 5V

$$V_{SP} = 4 \bullet \left(\frac{R_{ADJ}}{R1 + R_{ADJ}}\right) + 1V$$

CIRCUIT BLOCK DESCRIPTION (cont.)

The ADJ pin voltage on the slave chips will increase forcing their load currents to increase to match the master.

The AC frequency response of the voltage error amplifier is shown in Figure 7.

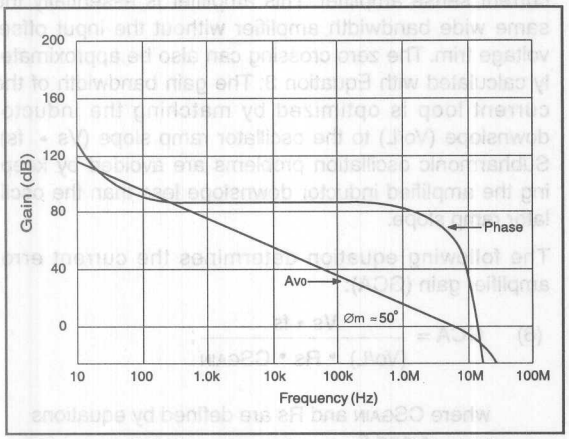


Figure 7. AC Frequency Response of the Voltage Error Amplifier

Startup and Shutdown: Isolated power up can be accomplished using the UCC1889. Application Note U-149 is available for additional information.

The UC1849 offers several features that enhance startup and shutdown. Soft start is accomplished by connecting RUN to VA+ and a capacitor to ground. The resulting RC rise time on the VA+ pin initiates a soft start. It can also be accomplished by connecting RUN to ILIM. When RUN is low it will command zero load current, guaranteeing a soft start. The undervoltage lockout (UVLO) is a logical AND of $\overline{ENBL}$ < 2.5V, SEQ > 2.5V, VCC > 8.4V and VREF > 4.65V. The block diagram shows that the thresholds are set by comparators. By placing an RC divider on the SEQ pin, the enabling of multiple chips can be sequenced with different RC time constants. Similarly, different RC time constants on the $\overline{ENBL}$ pins can sequence shutdown. The UVLO keeps the output from switching; however the internal reference starts up with VCC less than 8.4V. The $\overline{KILL}$ input shuts down the switching of the chip. This can be used in conjunction with an overvoltage comparator for overvoltage protection. In order to restart the chip after $\overline{KILL}$ has been initiated, the chip must be powered down and then back up. A pulse on the $\overline{ENBL}$ pin also accomplishes this without actually removing voltage to the VCC pin.

Load Sharing: Load sharing is accomplished similar to the UC1907. The sensed current for the UC1849 has an AC component that is amplified and then averaged. The voltage error amplifier output is the current command signal representing the average output load current. The ILIM pin programs the upper clamp voltage of this amplifier and consequently the maximum load current. A gain of 2 amplifier connected between the voltage error amplifier output and the share amplifier input increases the current share resolution and noise margin. The average current is used as an input to a source only load share buffer amplifier. The output of this amplifier is the current share bus. The IC with the highest sensed current will have the highest voltage on the current share bus and consequently act as the master. The 60mV input offset guarantees that the unit sensing the highest load current is chosen as the master.

The adjust amplifier is used by the remaining (slave) ICs to adjust their respective references high in order to balance each IC's load current. The master's ADJ pin will be at its 1.0V clamp and connected back to the non-inverting voltage error amplifier input through a high value resistor. This requires the user to initially calculate the control voltage with the ADJ pin at 1.0V.

VREF can be adjusted 150mV to 300mV which compensates for 5% unit to unit reference mismatch and external resistor mismatch. R_{ADJ} will typicaily be 10 to 30 times larger than R1. This also attenuates the overall variation of the ADJ clamp of 1V ±100mV by a factor of 10 to 30, contributing only a 3mV to 10mV additional delta to VREF. Refer to the UC3907 Application Note U-130 for further information on parallel power supply load sharing.

Current Control Loop: The current sense amplifier (CSA) is designed specifically for the task of sensing and amplifying the inductor ripple current at frequencies up to 1MHz. The CSA's input offset voltage (VIO) is trimmed to less than 1mV to minimize error of the average current signal. This amplifier is not internally compensated allowing the user to optimally choose the zero crossing bandwidth.

$$(3)\quad \text{Frequency (0dB)} = \frac{1}{2\pi\, R_{INV} \bullet C_{COMP}}$$

R_{INV} is the input resistance at the inverting terminal CS-
C_{COMP} is the capacitance between CS- and CSO.

Although it is only unity gain stable for a GBW of 7MHz, the amplifier is typically configured with a differential gain of at least 10, allowing the amplifier to operate at 70MHz with sufficient phase margin. A closed loop gain of 10 attenuates the output by 20.8dB.

$$20.8 = 20\log \bullet \frac{1}{11}$$

to the inverting terminal assuring stability. The amplifier's gain fed back into the inverting terminal is less than unity

CIRCUIT BLOCK DESCRIPTION (cont.)

at 7MHz, where the phase margin begins to roll off. See Figure 8 for typical Bode plot.

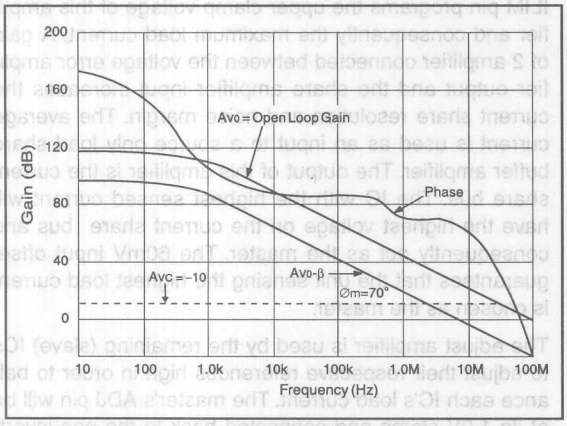


Figure 8. Current Sense Amplifier and Current Error Amplifier Bode Plot

The gain of the differential current sense amplifier (CS_{GAIN}) is calculated by knowing the maximum load current. The maximum voltage across the shunt resistor (R_S) divided by R_S is the maximum load current. By amplifying the voltage across RS, V_{RS}, to be equal to the voltage error amplifier Voh, the current control loop keeps the load from exceeding its current limit. Voh is set at 3.0V if ILIM is connected to VREF. The maximum current limit clamp can be reduced by reducing the voltage at ILIM to less than 3.0V as described in the ILIM pin description.

$$(4)\quad R_S = \frac{V_{RS}}{\text{Max } I_{LOAD}}$$

$$(5)\quad CS_{GAIN} = \frac{V_{ILIM}}{V_{RS}}$$

The current error amplifier (CEA) also needs its loop compensated by the user with the same criteria as the current sense amplifier. This amplifier is essentially the same wide bandwidth amplifier without the input offset voltage trim. The zero crossing can also be approximately calculated with Equation 3. The gain bandwidth of the current loop is optimized by matching the inductor downslope (Vo/L) to the oscillator ramp slope (Vs • fs). Subharmonic oscillation problems are avoided by keeping the amplified inductor downslope less than the oscillator ramp slope.

The following equation determines the current error amplifier gain (GCA):

$$(6)\quad GCA = \frac{Vs \bullet fs}{(Vo/L) \bullet R_S \bullet CS_{GAIN}};$$

where CS_{GAIN} and R_S are defined by equations 4 and 5,
Vs is the oscillator peak to peak voltage,
fs is the oscillator frequency,
Vo is the output voltage,
and L is the inductance.

Additional Information about average current mode control can be found in Unitrode Application Note U-140.

Design Example: Figure 9 is an open loop test that lets the user test the circuit blocks discussed without having to build an entire control loop. The pulse width can be varied by either the V_{ADJ} or the V_{ISENSE} inputs. Figure 10 shows an isolated power supply using the UC1849 secondary side average current mode controller.

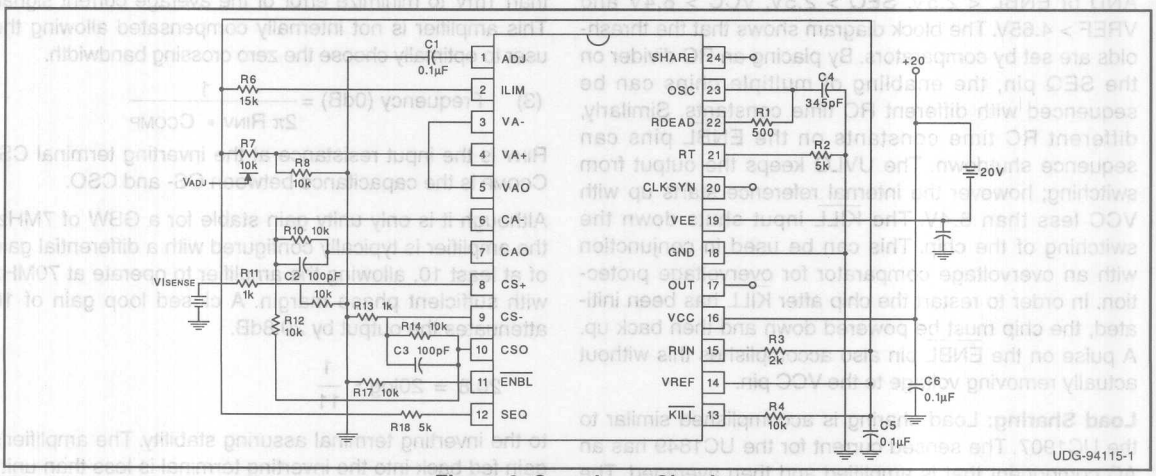


Figure 9. Open Loop Circuit

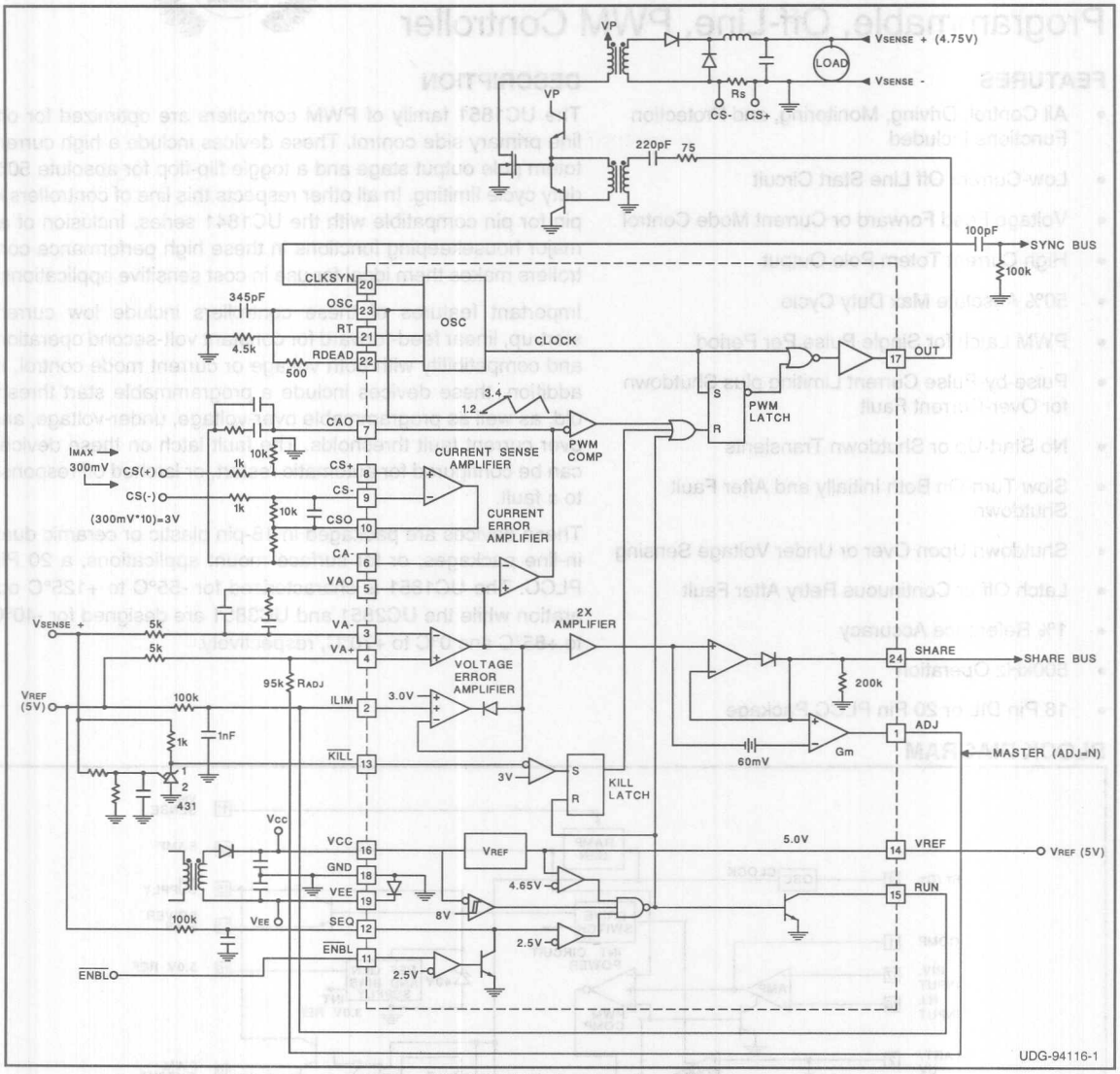


Figure 10. UC1849 Application Diagram

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. 603-424-2410 • FAX 603-424-3460

UNITRODE

UC1851
UC2851
UC3851

Programmable, Off-Line, PWM Controller

FEATURES

- All Control, Driving, Monitoring, and Protection Functions Included
- Low-Current Off Line Start Circuit
- Voltage Feed Forward or Current Mode Control
- High Current Totem Pole Output
- 50% Absolute Max Duty Cycle
- PWM Latch for Single Pulse Per Period
- Pulse-by-Pulse Current Limiting plus Shutdown for Over-Current Fault
- No Start-Up or Shutdown Transients
- Slow Turn-On Both Initially and After Fault Shutdown
- Shutdown Upon Over or Under Voltage Sensing
- Latch Off or Continuous Retry After Fault
- 1% Reference Accuracy
- 500kHz Operation
- 18 Pin DIL or 20 Pin PLCC Package

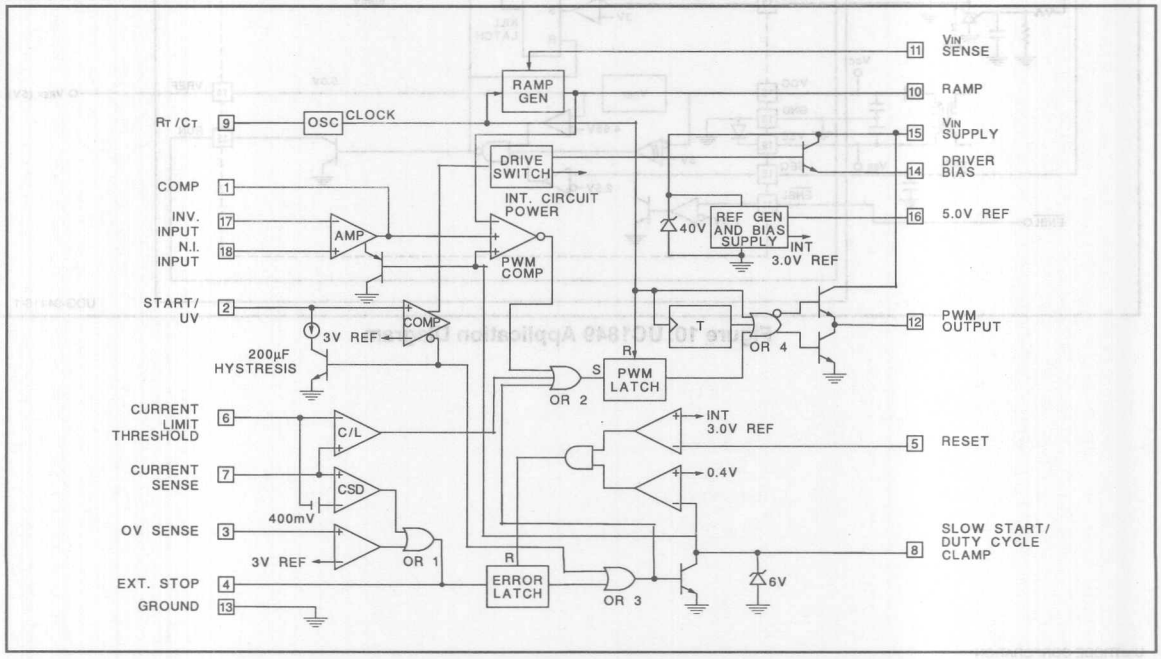
DESCRIPTION

The UC1851 family of PWM controllers are optimized for off-line primary side control. These devices include a high current totem pole output stage and a toggle flip-flop for absolute 50% duty cycle limiting. In all other respects this line of controllers is pin for pin compatible with the UC1841 series. Inclusion of all major housekeeping functions in these high performance controllers makes them ideal for use in cost sensitive applications.

Important features of these controllers include low current start-up, linear feed-forward for constant volt-second operation, and compatibility with both voltage or current mode control. In addition, these devices include a programmable start threshold, as well as programmable over-voltage, under-voltage, and over current fault thresholds. The fault latch on these devices can be configured for automatic restart, or latched off response to a fault.

These devices are packaged in 18-pin plastic or ceramic dual-in-line packages, or for surface mount applications, a 20 Pin PLCC. The UC1851 is characterized for -55°C to +125°C operation while the UC2851 and UC3851 are designed for -40°C to +85°C and 0°C to +70°C, respectively.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage, +VIN (Pin 15)
- Voltage Driven . . . . . +32V
- Current Driven, 100mA maximum . . . . . Self-limiting

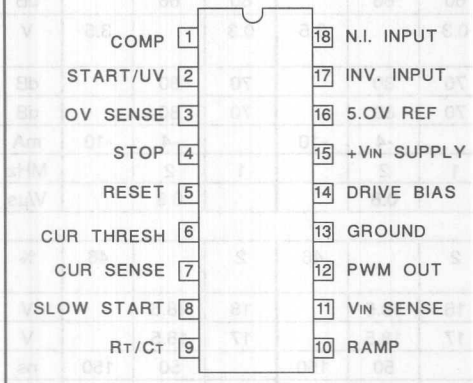
PWM Output Voltage (Pin 12) 40V
PWM Output Current, Steady-State (Pin 12) 400mA
PWM Output Peak Energy Discharge 20µJoules
Driver Bias Current (Pin 14) . . . . . -200mA
Reference Output Current (Pin 16) . . . . . -50mA
Slow-Start Sink Current (Pin 8) 20mA
VIN Sense Current (Pin 11) 10mA
Current Limit Inputs (Pins 6 & 7) . . . . . -0.5 to +5.5V
Stop Input (Pin 4) . . . . . -0.3 to +5.5V

Comparator Inputs
(Pins 1–7, 9–11, 16) . . . . . Internally clamped at 12V
Power Dissipation at T_A = 25°C (Note 3) 1000mW
Power Dissipation at T_C = 25°C (Note 3) 2000mW
Operating Junction Temperature . . . . . -55°C to +150°C
Storage Temperature Range . . . . . -65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . +300°C

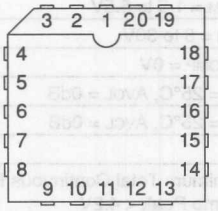
Note 1: All voltages are with respect to ground, Pin 13. Currents are positive-into, negative-out of the specified terminal
Note 2: All pin numbers are referenced to DIL-18 package.
Note 3: Consult Packaging Section of Databook for thermal limitations and considerations of package.

CONNECTION DIAGRAMS

DIL-18, SOIC-18 (TOP VIEW)
J or N, DW Package



PLCC-20, LCC-20
(TOP VIEW)
Q, L PACKAGE



PACKAGE PIN FUNCTIONS	
FUNCTION	PIN
COMP	1
START/UV	2
OV SENSE	3
STOP	4
RESET	5
CUR THRESH	7
CUR SENSE	8
SLOW START	9
RT/CT	10
RAMP	11
VIN SENSE	12
PWM OUT	13
GROUND	14
DRIVE BIAS	15
+VIN SUPPLY	17
5.0V REF	18
INV. INPUT	19
N.I. INPUT	20

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1851, -40°C to +85°C for the UC2851, and 0°C to 70°C for the UC3851; V_{IN} = 20V, R_T = 20kΩ, C_T = .001 mfd, R_R = 10kΩ, C_R = .001mfd. Current Limit Threshold = 200mV, T_A = T_J.

PARAMETER	TEST CONDITIONS	UC1851 / UC2851			UC3851			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Power Inputs								
Start-Up Current	VIN = 30V, Pin 2 = 2.5V		4.5	6		4.5	6	mA
Operating Current	VIN = 30V, Pin 2 = 3.5V		15	21		15	21	mA
Supply OV Clamp	VIN = 20mA	33	39	45	33	39	45	V
Reference Section								
Reference Voltage	TJ = 25°C	4.95	5.0	5.05	4.9	5.0	5.1	V
Line Regulation	VIN = 8 to 30V		10	15		10	20	mV
Load Regulation	IL = 0 to 10mA		10	20		10	30	mV
Total Ref Variation	Over Operating Temperature Range	4.9		5.1	4.85		5.15	V
Short Circuit Current	VREF = 0, TJ = 25°C		-80	-100		-80	-100	mA
Oscillator								
Nominal Frequency	TJ = 25°C	47	50	53	45	50	55	kHz
Voltage Stability	VIN = 8 to 30V		0.5	1		0.5	1	%
Total Ref Variation	Over Operating Temperature Range	45		55	43		57	kHz
Maximum Frequency	RT = 2kΩ, CT = 330pF	500			500			kHz

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1851, -40°C to +85°C for the UC2851, and 0°C to 70°C for the UC3851; V_{IN} = 20V, R_T = 20kΩ, C_T = .001 mfd, R_R = 10kΩ, C_R = .001mfd. Current Limit Threshold = 200mV, T_A = T_J.

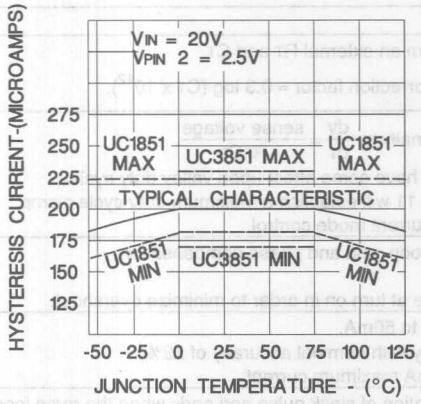
PARAMETER	TEST CONDITIONS	UC1851 / UC2851			UC3851			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Ramp Generator								
Ramp Current, Minimum	I_{SENSE} = –10µA		-11	-14		-11	-14	µA
Ramp Current, Maximum	I_{SENSE} = 1.0mA	-0.9	-.95		-0.9	-.95		mA
Ramp Valley		0.3	0.4	0.6	0.3	0.4	0.6	V
Ramp Peak	Clamping Level	3.9	4.2	4.5	3.9	4.2	4.5	V
Error Amplifier								
Input Offset Voltage	V_{CM} = 5.0V		0.5	5		2	10	mV
Input Bias Current			0.5	2		1	5	µA
Input Offset Current				0.5			0.5	µA
Open Loop Gain	ΔV_O = 1 to 3V	60	66		60	66		dB
Output Swing (Max Output ≤ Ramp Peak - 100mV)	Minimum Total Range	0.3		3.5	0.3		3.5	V
CMRR	V_{CM} = 1.5 to 5.5V	70	80		70	80		dB
PSRR	V_{IN} = 8 to 30V	70	80		70	80		dB
Short Circuit Current	V_{COMP} = 0V		-4	-10		-4	-10	mA
Gain Bandwidth (Note 1)	T_J = 25°C, A_{VOL} = 0dB	1	2		1	2		MHz
Slew Rate (Note 1)	T_J = 25°C, A_{VCL} = 0dB		0.8			0.8		V/µs
PWM Section								
Continuous Duty Cycle Range (other than zero) (Note 1)	Minimum Total Continuous Range Ramp Peak < 4.2V	2		46	2		46	%
Output High Level	I_{SOURCE} = 20mA	18	18.5		18	18.5		V
	I_{SOURCE} = 200mA	17	18.5		17	18.5		V
Rise Time (Note 1)	T_J = 25°C, C_L = 1nF		50	150		50	150	ns
Fall Time (Note 1)	T_J = 25°C, C_L = 1nF		50	150		50	150	ns
Output Saturation	I_{OUT} = 20mA		0.2	0.4		0.2	0.4	V
	I_{OUT} = 200mA		1.7	2.2		1.7	2.2	V
Comparator Delay (Note 1)	Pin 8 to Pin 12, T_J = 25°C, R_L = 1kΩ		300	500		300	500	ns
Sequencing Functions								
Comparator Thresholds	Pins 2, 3, 5	2.8	3.0	3.2	2.8	3.0	3.2	V
Input Bias Current	Pins 3, 5 = 0V		-1.0	-4.0		-1.0	-4.0	µA
Input Leakage	Pins 3, 5 = 10V		0.1	2.0		0.1	2.0	µA
Start/UV Hysteresis Current	Pin 2 = 2.5V	170	200	220	170	200	230	µA
Ext. Stop Threshold	Pin 4	0.8	1.6	2.4	0.8	1.6	2.4	V
Error Latch Activate Current	Pin 4 = 0V, Pin 3 > 3V		-120	-200		-120	-200	µA
Driver Bias Saturation Voltage, V_{IN}-V_{OH}	I_B = -50mA		2	3		2	3	V
Driver Bias Leakage	V_B = 0V		-0.1	-10		-0.1	-10	µA
Slow-Start Saturation	I_S = 10mA		0.2	0.5		0.2	0.5	V
Slow-Start Leakage	V_S = 4.5V		0.1	2.0		0.1	2.0	µA
Current Control								
Current Limit Offset			0	5		0	10	mV
Current Shutdown Offset		370	400	430	360	400	440	mV
Input Bias Current	Pin 7 = 0V		-2	-5		-2	-5	µA
Common Mode Range (Note 1)		-0.4		3.0	-0.4		3.0	V
Current Limit Delay (Note 1)	T_J = 25°C, Pin 7 to 12, R_L = 1k		200	400		200	400	ns

Note 1:Guaranteed by design. Not 100% tested in production.

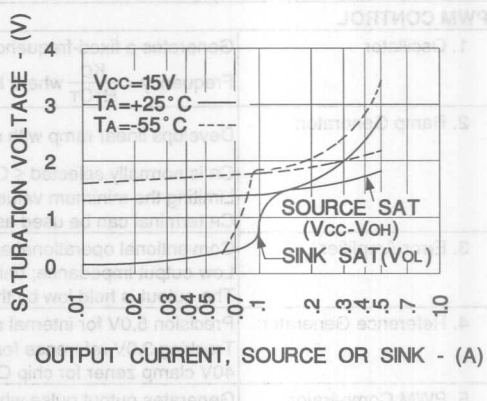
FUNCTIONAL DESCRIPTION

PWM CONTROL	
1. Oscillator	Generates a fixed-frequency internal clock from an external R_T and C_T. Frequency = $\frac{K_C}{R_T C_T}$ where K_C is a first-order correction factor ≈ 0.3 log (C_T x 10^{12}).
2. Ramp Generator:	Develops linear ramp with slope defined externally by $\frac{dV}{dT} = \frac{\text{sense voltage}}{R_R C_R}$. C_R is normally selected ≤ C_T and its value will have some effect upon valley duty cycle. Limiting the minimum value for I_{SENSE} into pin 11 will establish a maximum duty cycle clamp. C_R terminal can be used as an input port for current mode control.
3. Error Amplifier	Conventional operational amplifier for closed-loop gain and phase compensation. Low output impedance; unity-gain stable. The output is held low by the slow start voltage at turn on in order to minimize overshoot.
4. Reference Generator:	Precision 5.0V for internal and external usage to 50mA. Tracking 3.0V reference for internal usage only with nominal accuracy of ±2%. 40V clamp zener for chip OV protection, 100mA maximum current.
5. PWM Comparator:	Generates output pulse which starts at termination of clock pulse and ends when the ramp input crosses the lowest of two positive inputs.
6. PWM Latch:	Terminates the PWM output pulse when set by inputs from either the PWM comparator, the pulse-by-pulse comparator, or the error latch. Resets with each internal clock pulse.
7. PWM Output Switch:	Totem pole output stage capable of sourcing and sinking 1 amp peak current. The active "on" state is high.
SEQUENCING FUNCTIONS	
1. Start/UV Sense:	With an increasing voltage, this comparator generates a turn-on signal and releases the slow start clamp at a start threshold. With a decreasing voltage, it generates a turn-off command at a lower level separated by a 200µA hysteresis current.
2. Drive Switch:	Disables most of the chip to hold internal current consumption low, and Driver Bias OFF, until input voltage reaches start threshold.
3. Driver Bias:	Supplies drive to external circuitry upon start-up.
4. Slow Start:	Clamps low to hold PWM OFF. Upon release, rises with rate controlled by $R_S C_S$ for slow increase of output pulse width. Can also be used as an alternate maximum duty cycle clamp with an external voltage divider.
PROTECTION FUNCTIONS	
1. Error Latch:	When set by momentary input, this latch insures immediate PWM shutdown and hold off until reset. Inputs to Error Latch are: a. OV > 3.2V (Typically 3V) b. Stop > 2.4V (Typically 1.6V) c. Current Sense 400mV over threshold. (Typical). Error Latch resets when slow start voltage falls to 0.4V if Reset Pin < 2.8V. With Pin 5 > 3.2V, Error Latch will remain set.
2. Current Limiting:	Differential input comparator terminates individual output pulses each time sense voltage rises above threshold. When sense voltage rises to 400mV (typical) above threshold, a shutdown signal is sent to Error Latch.
3. External Stop:	A voltage over 2.4 will set the Error Latch and hold the output off. A voltage less than 0.8V will defeat the error latch and prevent shutdown. A capacitor here will slow the action of the error latch for transient protection by providing a Typical Delay of 13ms/µF.

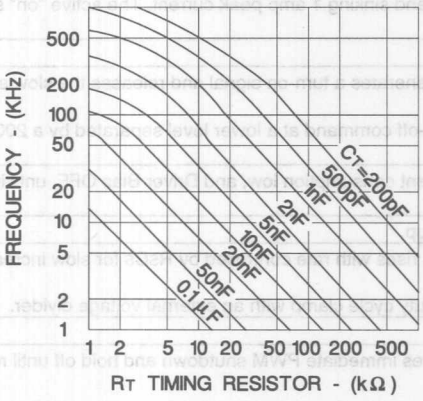
Start/UV Hysteresis Current



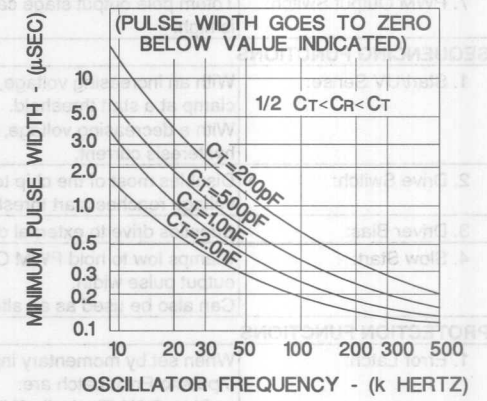
Output Saturation Characteristics



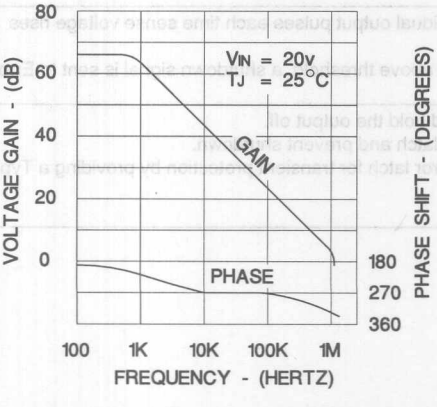
Oscillator Frequency



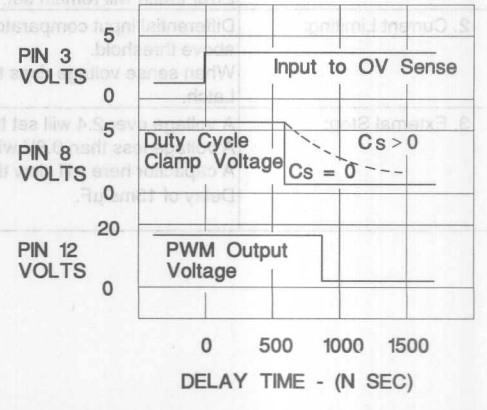
PWM Output Minimum Pulse Width



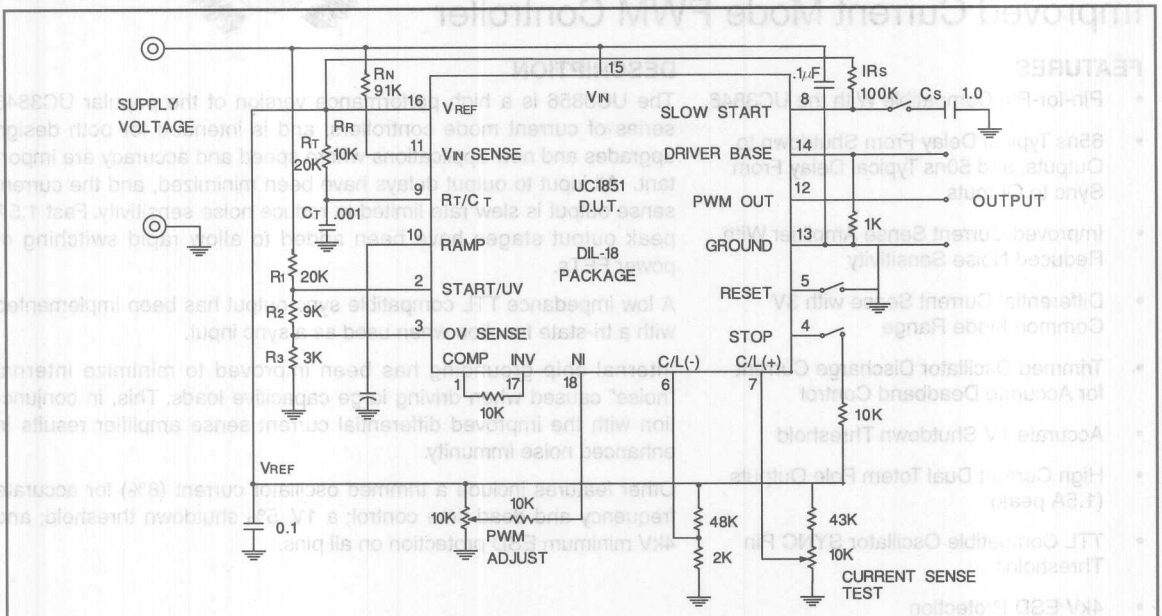
Error Amplifier Open-Loop Gain and Phase



Shutdown Timing



OPEN-LOOP CIRCUIT



$$\text{Nominal Frequency} = \frac{1}{R_T C_T} = 50\text{kHz}$$

$$\text{Start Voltage} = 3\left(\frac{R1 + R2 + R3}{R2 + R3}\right) + 0.2R1 = 12\text{V}$$

$$\text{UV Fault Voltage} = 3\left(\frac{R1 + R2 + R3}{R2 + R3}\right) = 8\text{V}$$

$$\text{OV Fault Voltage} = 3\left(\frac{R1 + R2 + R3}{R3}\right) = 32\text{V}$$

Current Limit = 200mV

Current Fault Voltage = 600mV

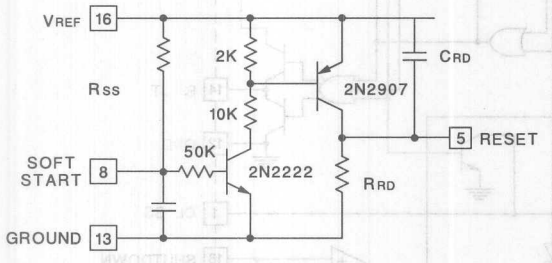
Duty Cycle Clamp = 50%

@ V_{IN} = 15V, Duty Cycle = 48%

@ V_{IN} = 30V, Duty Cycle = 24%

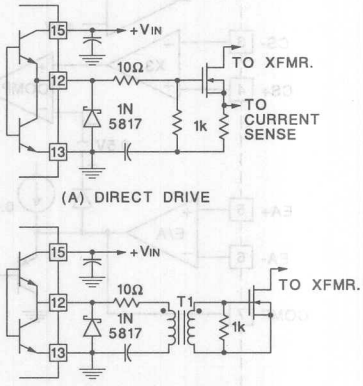
High Peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to pin 13 in a single ground point.

Programmable Soft Start and Restart Delay Circuit



For further application information see UC1840/UC1841 Data Sheets

UC1851 Power MOSFET Drive Interface



UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

UNITRODE

UC1856
UC2856
UC3856

Improved Current Mode PWM Controller

FEATURES

- Pin-for-Pin Compatible With the UC3846
- 65ns Typical Delay From Shutdown to Outputs, and 50ns Typical Delay From Sync to Outputs
- Improved Current Sense Amplifier With Reduced Noise Sensitivity
- Differential Current Sense with 3V Common Mode Range
- Trimmed Oscillator Discharge Current for Accurate Deadband Control
- Accurate 1V Shutdown Threshold
- High Current Dual Totem Pole Outputs (1.5A peak)
- TTL Compatible Oscillator SYNC Pin Thresholds
- 4kV ESD Protection

DESCRIPTION

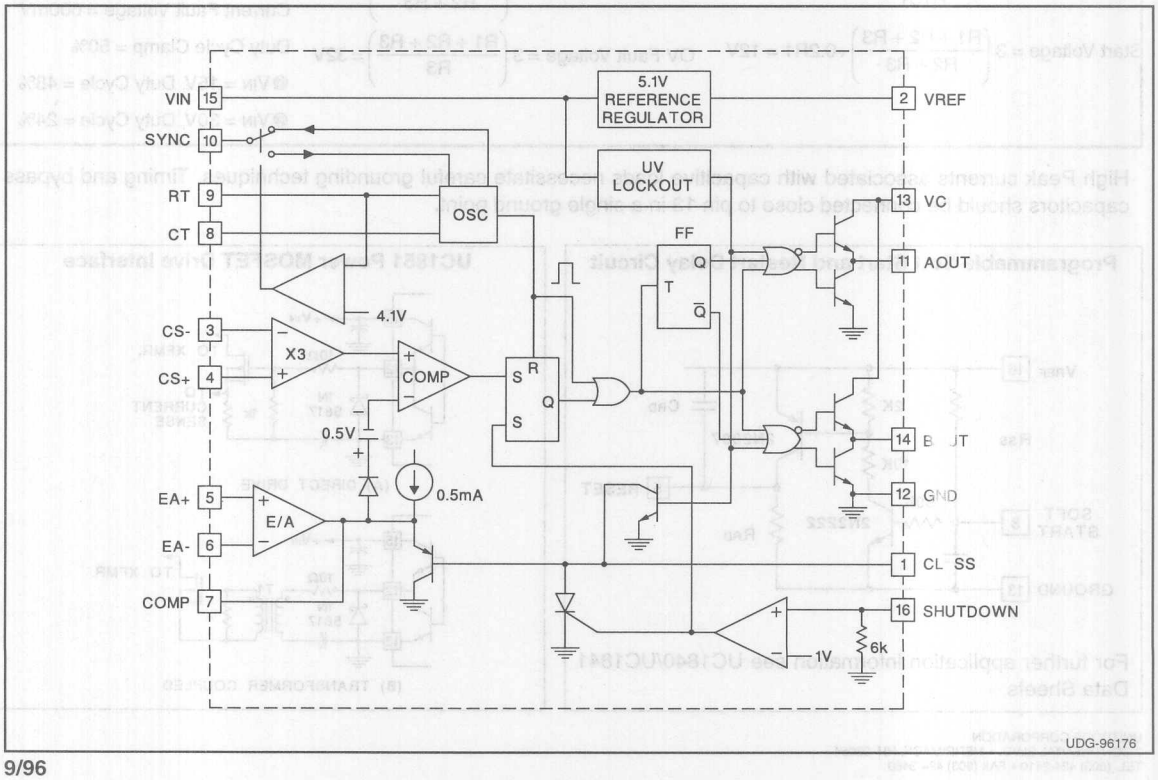
The UC3856 is a high performance version of the popular UC3846 series of current mode controllers, and is intended for both design upgrades and new applications where speed and accuracy are important. All input to output delays have been minimized, and the current sense output is slew rate limited to reduce noise sensitivity. Fast 1.5A peak output stages have been added to allow rapid switching of power FETs.

A low impedance TTL compatible sync output has been implemented with a tri-state function when used as a sync input.

Internal chip grounding has been improved to minimize internal "noise" caused when driving large capacitive loads. This, in conjunction with the improved differential current sense amplifier results in enhanced noise immunity.

Other features include a trimmed oscillator current (8%) for accurate frequency and dead time control; a 1V, 5% shutdown threshold; and 4kV minimum ESD protection on all pins.

BLOCK DIAGRAM



9/96

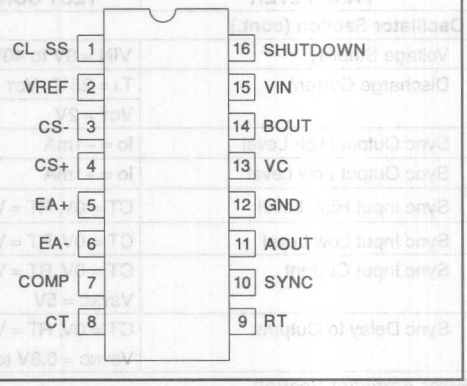
ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... +40V
Collector Supply Voltage ..... +40V
Output Current, Source or Sink
DC 0.5A
Pulse (0.5µs) 2.0A
Error Amp Inputs ..... –0.3V to +VIN
Shutdown Input ..... –0.3V to +10V
Current Sense Inputs ..... –0.3V to +3V
SYNC Output Current ..... ±10mA
Error Amplifier Output Current ..... –5mA
Soft Start Sink Current 50mA
Oscillator Charging Current 5mA
Power Dissipation at TA = 25°C (Note 2) 1000mW
Power Dissipation at Tc = 25°C (Note 2) 2000mW
Junction Temperature ..... –55°C to +150°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

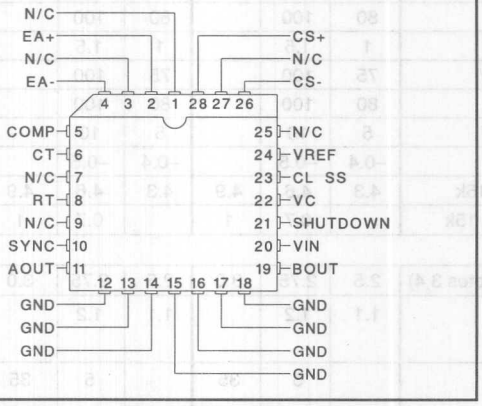
All voltages are with respect to Ground. Currents are positive into, negative out of the specified terminal. Consult packaging section of databook for thermal limitations and considerations of package.

CONNECTION DIAGRAMS

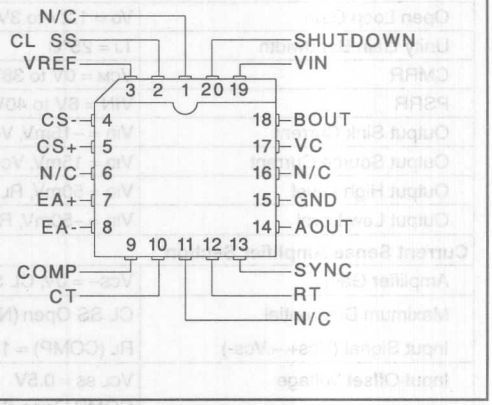
DIL–16, SOIC-16 (Top View)
J or N, DW PACKAGE



PLCC-28 (Top View)
QP PACKAGE



PLCC-20 (Top View)
Q PACKAGE



ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply for TA = –55°C to +125°C for UC1856; – 40°C to +85°C for the UC2856; and 0°C to +70°C for the UC3856, VIN = 15V, RT = 10k, CT = 1nF, TA = TJ.

PARAMETER	TEST CONDITIONS	UC1856/UC2856			UC3856			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Reference Section								
Output Voltage	TJ = 25°C, Io = 1mA	5.05	5.10	5.15	5.00	5.10	5.20	V
Line Regulation	VIN = 8V to 40V			20			20	mV
Load Regulation	Io = –1mA to –10mA			15			15	mV
Total Output Variation	Line, Load, and Temperature	5.00		5.20	4.95		5.25	V
Output Noise Voltage	10Hz < f < 10kHz, TJ = 25°C		50			50		µV
Long Term Stability	TJ = 125°C, 1000 Hrs (Note 2)		5	25		5	25	mV
Short Circuit Current	VREF = 0V	–25	–45	–65	–25	–45	–65	mA
Oscillator Section								
Initial Accuracy	TJ = 25°C	180	200	220	180	200	220	kHz
	Over Operating Range	170		230	170		230	kHz

ELECTRICAL CHARACTERISTICS (cont.) Unless otherwise stated, these specifications apply for T_A = –55°C to +125°C for UC1856; – 40°C to +85°C for the UC2856; and 0°C to +70°C for the UC3856, VIN = 15V, RT = 10k, CT = 1nF, T_A = T_J.

PARAMETER	TEST CONDITIONS	UC1856/UC2856			UC3856			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Oscillator Section (cont.)								
Voltage Stability	VIN = 8V to 40V			2			2	%
Discharge Current	T_J = 25°C, V_{CT} = 2V	7.5	8.0	8.8	7.5	8.0	8.8	mA
	V_{CT} = 2V	6.7	8.0	8.8	6.7	8.0	8.8	mA
Sync Output High Level	Io = –1mA	2.4	3.6		2.4	3.6		V
Sync Output Low Level	Io = +1mA		0.2	0.4		0.2	0.4	V
Sync Input High Level	CT = 0V, RT = VREF	2.0	1.5		2.0	1.5		V
Sync Input Low Level	CT = 0V, RT = VREF		1.5	0.8		1.5	0.8	V
Sync Input Current	CT = 0V, RT = VREF V_{SYNC} = 5V		1	10		1	10	µA
Sync Delay to Outputs	CT = 0V, RT = VREF V_{SYNC} = 0.8V to 2V		50	100		50	100	ns
Error Amplifier Section								
Input Offset Voltage	V_{CM} = 2V			5			10	mV
Input Bias Current				–1			–1	µA
Input Offset Current				500			500	nA
Common Mode Range	VIN = 8V to 40V	0		VIN – 2	0		VIN – 2	V
Open Loop Gain	Vo = 1.2V to 3V	80	100		80	100		dB
Unity Gain Bandwidth	T_J = 25°C	1	1.5		1	1.5		MHz
CMRR	V_{CM} = 0V to 38V, VIN = 40V	75	100		75	100		dB
PSRR	VIN = 8V to 40V	80	100		80	100		dB
Output Sink Current	V_{ID} = –15mV, V_{COMP} = 1.2V	5	10		5	10		mA
Output Source Current	V_{ID} = 15mV, V_{COMP} = 2.5V	–0.4	–0.5		–0.4	–0.5		mA
Output High Level	V_{ID} = 50mV, R_L (COMP) = 15k	4.3	4.6	4.9	4.3	4.6	4.9	V
Output Low Level	V_{ID} = –50mV, R_L (COMP) = 15k		0.7	1		0.7	1	V
Current Sense Amplifier Section								
Amplifier Gain	V_{CS-} = 0V, CL SS Open (Notes 3,4)	2.5	2.75	3.0	2.5	2.75	3.0	V/V
Maximum Differential Input Signal (V_{CS+} – Vcs-)	CL SS Open (Note 3) R_L (COMP) = 15k	1.1	1.2		1.1	1.2		V
Input Offset Voltage	$V_{CL\ SS}$ = 0.5V COMP Open (Note 3)		5	35		5	35	mV
CMRR	V_{CM} = 0V to 3V	60			60			dB
PSRR	VIN = 8V to 40V	60			60			dB
Input Bias Current	$V_{CL\ SS}$ = 0.5V, COMP Open (Note 3)			–1	–3	–1	–3	µA
Input Offset Current	$V_{CL\ SS}$ = 0.5V, COMP Open (Note 3)			1			1	mA
Input Common Mode Range		0		3	0		3	V
Delay to Outputs	V_{EA+} = VREF, EA– = 0V CS+ – CS– = 0V to 1.5V		120	250		120	250	ns
Current Limit Adjust Section								
Current Limit Offset	V_{CS-} = 0V V_{CS+} = 0V, COMP = Open (Note 3)	0.43	0.5	0.57	0.43	0.5	0.57	V
Input Bias Current	V_{EA+} = VREF, V_{EA-} = 0V		–10	–30		–10	–30	µA
Shutdown Terminal Section								
Threshold Voltage		0.95	1.00	1.05	0.95	1.00	1.05	V
Input Voltage Range		0		5	0		5	V

ELECTRICAL CHARACTERISTICS (cont.) Unless otherwise stated, these specifications apply for T_A = –55°C to +125°C for UC1856; – 40°C to +85°C for the UC2856; and 0°C to +70°C for the UC3856, VIN = 15V, RT = 10k, CT = 1nF, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	UC1856/UC2856			UC3856			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Shutdown Terminal Section (cont.)								
Minimum Latching Current ($I_{CL\ SS}$)	(Note 5)	3	1.5		3	1.5		mA
Maximum Non-Latching Current ($I_{CL\ SS}$)	(Note 6)		1.5	0.8		1.5	0.8	mA
Delay to Outputs	$V_{SHUTDOWN}$ = 0 to 1.3V		65	110		65	110	ns
Output Section								
Collector-Emitter Voltage		40			40			V
Off-State Bias Current	VC = 40V			250			250	µA
Output Low Level	I_{OUT} = 20mA		0.1	0.5		0.1	0.5	V
	I_{OUT} = 200mA		0.5	2.6		0.5	2.6	V
Output High Level	I_{OUT} = –20mA	12.5	13.2		12.5	13.2		V
	I_{OUT} = –200mA	12	13.1		12	13.1		V
Rise Time	C1 = 1nF		40	80		40	80	ns
Fall Time	C1 = 1nF		40	80		40	80	ns
UVLO Low Saturation	VIN = 0V, I_{OUT} = 20mA		0.8	1.5		0.8	1.5	V
PWM Section								
Maximum Duty Cycle		45	47	50	45	47	50	%
Minimum Duty Cycle				0			0	%
Undervoltage Lockout Section								
Startup Threshold			7.7	8.0		7.7	8.0	V
Threshold Hysterisis			0.7			0.7		V
Total Standby Current								
Supply Current			18	23		18	23	mA

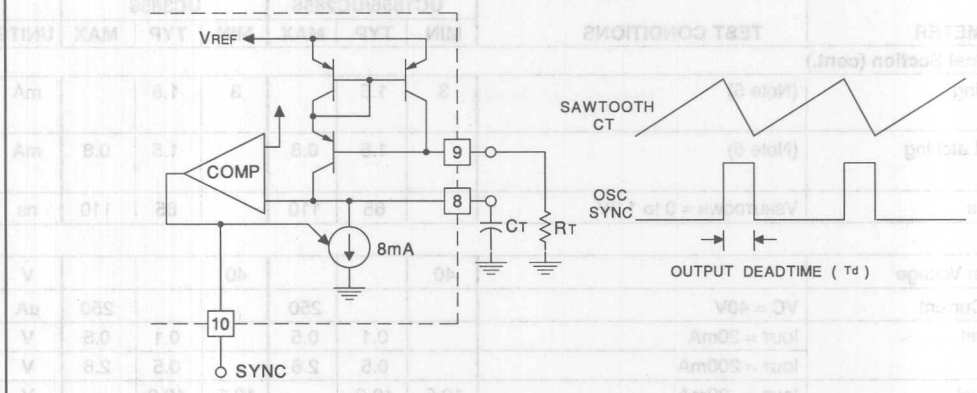
Note 1: All voltages are with respect to GND. Currents are positive into, negative out of the specified terminal.
Note 2: This parameter, although guaranteed over the recommended operating conditions is not 100% tested in production.
Note 3: Parameter measured at trip point of latch with V_{EA+} = VREF, V_{EA-} = 0V.
Note 4: Amplifier gain defined as:

$$G = \frac{\Delta V_{COMP}}{\Delta V_{CS+}}; \qquad \Delta V_{CS-} = 0V \text{ to } 1.0V$$

Note 5: Current into CL SS guaranteed to latch circuit into shutdown state.
Note 6: Current into CL SS guaranteed not to latch circuit into shutdown state.

APPLICATIONS INFORMATION

Oscillator Circuit



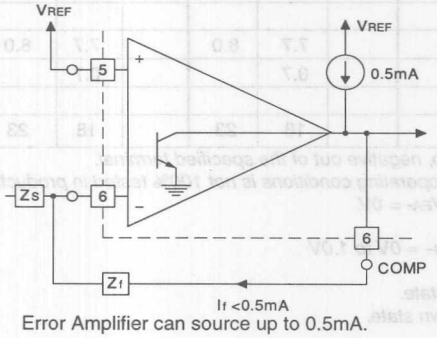
Output deadtime is determined by size of the external capacitor, C_T, according to the formula: $T_d = \frac{2C_T}{8mA - \frac{3.6}{R_T}}$

For large values of R_T: $T_d = 250C_T$

Oscillator frequency is approximated by the formula: $f_T = \frac{2}{R_T C_T}$

UDG-96177

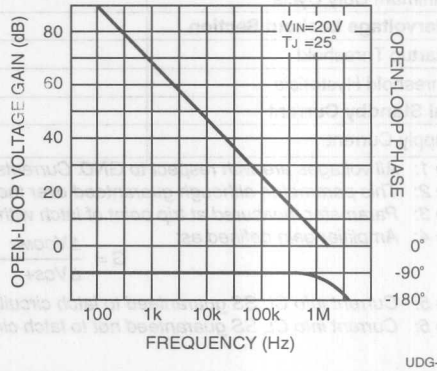
Error Amplifier Output Configuration



Error Amplifier can source up to 0.5mA.

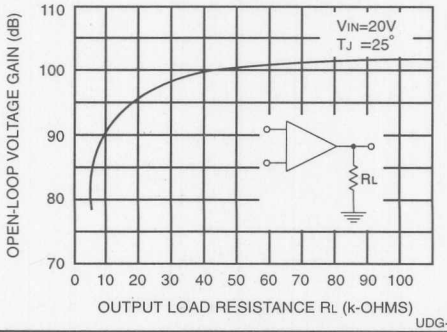
UDG-96178

Error Amplifier Gain and Phase vs Frequency



UDG-96179

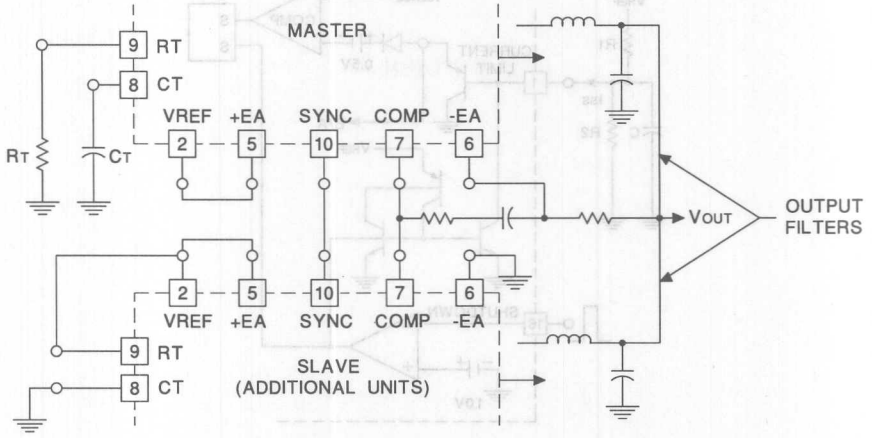
Error Amplifier Open-Loop D.C. Gain vs Load Resistance



UDG-96180

APPLICATIONS INFORMATION (cont.)

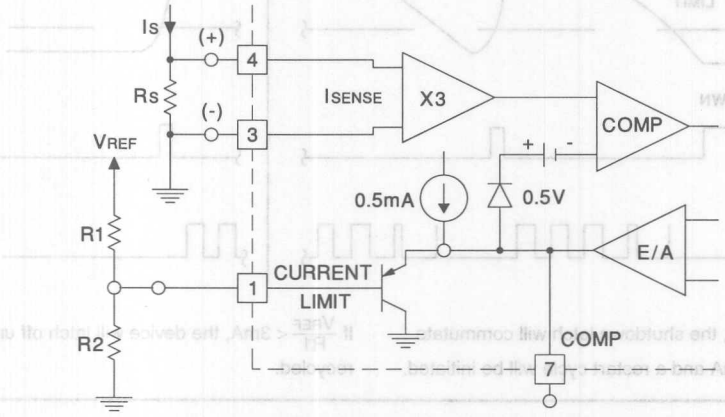
Parallel Operation



Slaving allows parallel operation of two or more units with equal current sharing.

UDG-96181

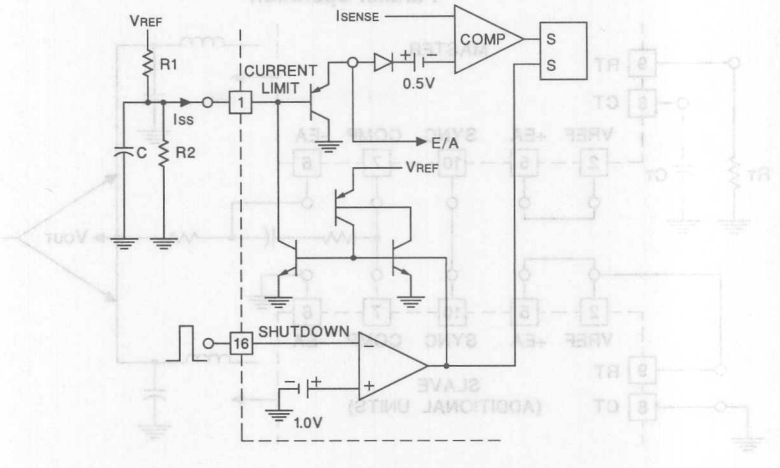
Pulse by Pulse Current Limiting



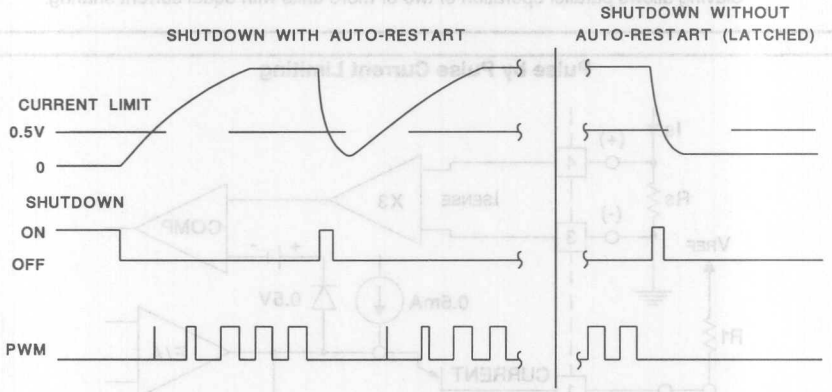
Peak current (Is) is determined by the formula: $Is = \frac{\left(\frac{R2\ V_{REF}}{R1 + R2}\right) - 0.5}{3Rs}$

UDG-96182

APPLICATIONS DATA (cont.)



UDG-96183

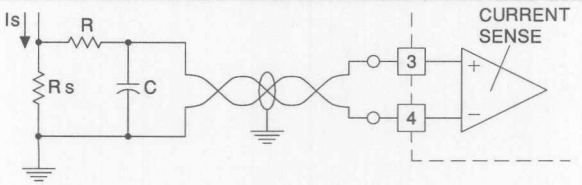


UDG-96184

If $\frac{V_{REF}}{R1} < 0.8mA$, the shutdown latch will commutate when Iss = 0.8mA and a restart cycle will be initiated.

If $\frac{V_{REF}}{R1} < 3mA$, the device will latch off until power is recycled.

Current Sense Amplifier Connections

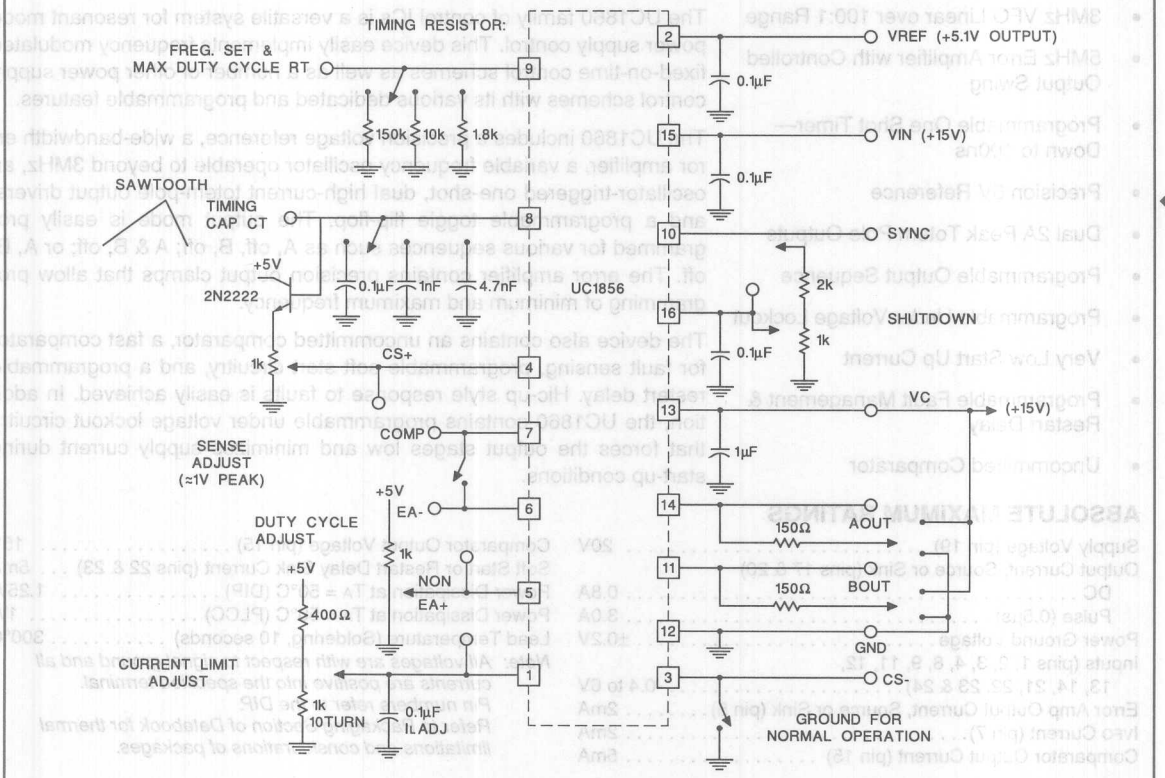


A small RC filter may be required in some applications to reduce switch transients. Differential input allows remote, noise sensing.

UDG-96185

APPLICATIONS INFORMATION (cont.)

UC1856 Open Loop Test Circuit



- BYPASS CAPS SHOULD BE LOW ESR & ESL TYPE
- SHORT E/A- & COMP FOR UNITY GAIN TESTING

THE USE OF A GROUND PLANE IS HIGHLY RECOMMENDED

UDG-96186

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. 603-424-2410 • FAX 603-424-3460

UNITRODE

UC1860
UC2860
UC3860

Resonant Mode Power Supply Controller

FEATURES

- 3MHz VFO Linear over 100:1 Range
- 5MHz Error Amplifier with Controlled Output Swing
- Programmable One Shot Timer—Down to 100ns
- Precision 5V Reference
- Dual 2A Peak Totem Pole Outputs
- Programmable Output Sequence
- Programmable Under Voltage Lockout
- Very Low Start Up Current
- Programmable Fault Management & Restart Delay
- Uncommitted Comparator

DESCRIPTION

The UC1860 family of control ICs is a versatile system for resonant mode power supply control. This device easily implements frequency modulated fixed-on-time control schemes as well as a number of other power supply control schemes with its various dedicated and programmable features.

The UC1860 includes a precision voltage reference, a wide-bandwidth error amplifier, a variable frequency oscillator operable to beyond 3MHz, an oscillator-triggered one-shot, dual high-current totem-pole output drivers, and a programmable toggle flip-flop. The output mode is easily programmed for various sequences such as A, off, B, off; A & B, off; or A, B, off. The error amplifier contains precision output clamps that allow programming of minimum and maximum frequency.

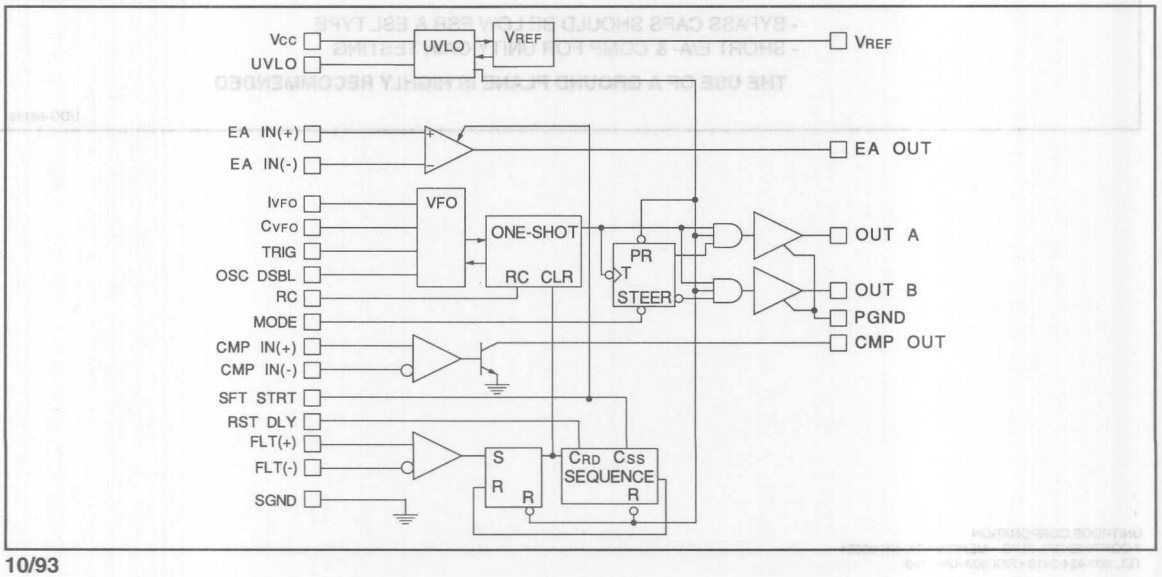
The device also contains an uncommitted comparator, a fast comparator for fault sensing, programmable soft start circuitry, and a programmable restart delay. Hic-up style response to faults is easily achieved. In addition, the UC1860 contains programmable under voltage lockout circuitry that forces the output stages low and minimizes supply current during start-up conditions.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (pin 19) 20V
Output Current, Source or Sink (pins 17 & 20)
DC 0.8A
Pulse (0.5µs) 3.0A
Power Ground Voltage . . . . . ±0.2V
Inputs (pins 1, 2, 3, 4, 8, 9, 11, 12, 13, 14, 21, 22, 23 & 24) . . . . . -0.4 to 6V
Error Amp Output Current, Source or Sink (pin 5) 2mA
I_{VFO} Current (pin 7) 2mA
Comparator Output Current (pin 15) 5mA
Comparator Output Voltage (pin 15) 15V
Soft Start or Restart Delay Sink Current (pins 22 & 23) . . . 5mA
Power Dissipation at T_A = 50°C (DIP) 1.25W
Power Dissipation at T_A = 50°C (PLCC) 1W
Lead Temperature (Soldering, 10 seconds) . . . . . 300°C

Note: All voltages are with respect to signal ground and all currents are positive into the specified terminal. Pin numbers refer to the DIP. Refer to Packaging Section of Databook for thermal limitations and considerations of packages.

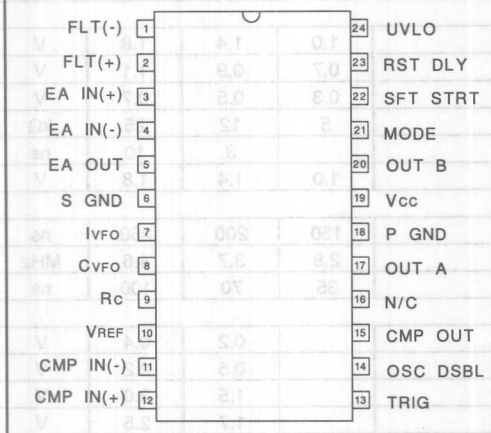
BLOCK DIAGRAM



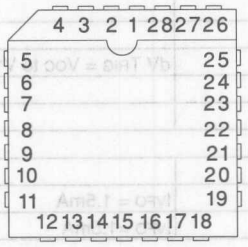
10/93

CONNECTION DIAGRAM

DIL - 24 (TOP VIEW)
J or N Package



PLCC-28, LCC-28
(TOP VIEW)
Q or L Package



PIN PACKAGE FUNCTION	
FUNCTION	PIN
S GND	1
IVFO	2
CVFO	3
RC	4
VREF	5
CMP IN (-)	6
CMP IN (+)	7
TRIG	8
OSC DSBL	9
CMP OUT	10
N/C	11, 12
OUT A	13
PGND	14
N/C	15
VCC	16
OUT B	17
N/C	18, 19
MODE	20
SFT STRT	21
RST DLY	22
UVLO	23
FLT (-)	24
FLT (+)	25
EA IN (+)	26
EA IN (-)	27
EA OUT	28

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, all specifications apply for -55°C ≤ TA ≤ 125°C for the UC1860, -25°C ≤ TA ≤ 85°C for the UC2860, 0 ≤ TA ≤ 70°C for the UC3860, VCC = 12V, CVFO = 330pF, IVFO = 0.5mA, C = 330pF, and R = 2.7k, TA = TJ.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Reference Section					
Output Voltage	TA = 25°C, Io = 0	4.95	5.00	5.05	V
	Io = 0, Over Temp	4.93		5.07	V
Line Regulation	10 ≤ VCC ≤ 20V		2	15	mV
Load Regulation	0≤ Io ≤ 10mA		2	25	mV
Output Noise Voltage*	10Hz ≤ f ≤ 10kHz		50		μVRMS
Short Circuit Current	VREF = 0V	-150		-15	mA
Error Amplifier Section					
Input Offset Voltage	2.8 ≤ VCM ≤ 4.5V		1	8	mV
Input Bias Current			50	500	nA
Open Loop Gain	dVO = 1.5V	60	80		dB
PSRR	10 ≤ VCC ≤ 20V	70	100		dB
Output Low (VO-VIVFO)	-0.1 ≤ Io ≤ 0.1mA	-8	0	8	mV
Output High (VO-VIVFO)	-0.5 ≤ Io ≤ 0.5mA	1.9	2	2.1	V
Unity Gain Bandwidth*	RIN = 2k	4	5		MHz
Oscillator Section					
Nominal Frequency*		1.0	1.5	2.0	MHz
dF/dIOSC*	100 ≤ IVFO ≤ 500μA	2	3	4	GHz/A

Guaranteed by design but not 100% tested.

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, all specifications apply for -55°C ≤ T_A ≤ 125°C for the UC1860, -25° ≤ T_A ≤ 85°C for the UC2860, 0 ≤ T_A ≤ 70°C for the UC3860, V_{CC} = 12V, C_{VFO} = 330pF, I_{VFO} = 0.5mA, C = 330pF, and R = 2.7k, T_A = T_J.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator Section (cont'd)					
Trig in Threshold		1.0	1.4	1.8	V
Trig in Open Circuit Voltage		0.7	0.9	1.1	V
Trig in Delta (V_{TH}-V_{OC})		0.3	0.5	0.7	V
Trig in Input Resistance	dV $_{TRIG}$ = V_{OC} to V_{TH}	5	12	25	kΩ
Minimum Trig in Pulse Width*			3	10	ns
Osc. Disable Threshold		1.0	1.4	1.8	V
One Shot Timer					
On Time*		150	200	250	ns
Clamp Frequency*	I_{VFO} = 1.5mA	2.8	3.7	4.6	MHz
Dead Time*	I_{VFO} =1.5mA	35	70	100	ns
Output Stage					
Output Low Saturation	20mA		0.2	0.4	V
	200mA		0.5	2.2	V
Output High Saturation	-20mA		1.5	2.0	V
	-200mA		1.7	2.5	V
Rise/Fall Time*	C_{LOAD} = 1nF		15	30	ns
UVLO Low Saturation	20mA		0.8	1.5	V
Output Mode Low Input				0.4	V
Output Mode High Input		2.0			V
Under Voltage Lockout Section					
V_{CC} Comparator Threshold	On	16	17.3	18.5	V
	Off	9.5	10.5	12	V
UVLO Comparator Threshold	On	3.6	4.2	4.8	V
	Hysteresis	0.2	0.4	0.6	V
UVLO Input Resistance	UVLO = 4/V_{CC} = 8	10	23	50	kΩ
V_{REF} Comparator Threshold	V_{CC} = UVLO = V_{REF}		4.5	4.9	V
Supply Current					
I_{CC}	V_{CC} = 12V, V_{OSC} DSBL = 3V		30	40	mA
I_{START}	UVLO pin open V_{CC} = V_{CC} (on) -0.3V		0.3	0.5	mA
Fault Comparator					
Input Offset Voltage	–0.3 ≤ V_{CM} ≤ 3V		2	10	mV
Input Bias Current	V_{CM} = 0V		100	200	µA
Input Offset Current	V_{CM} = 0V		10	30	µA
Propagation Delay To Output*	±50mV input		100	150	ns
Uncommitted Comparator					
Input Offset Voltage	-0.3 ≤ V_{CM} ≤ 3V		2	10	mV
Input Bias Current	V_{CM} = 0V		100	200	µA
Input Offset Current	V_{CM} = 0V		10	30	µA
Output Low Voltage	Io = 2mA		0.3	0.5	V
Propagation Delay To Sat*	±50mV input, 2.5k load to 5V		50	100	ns
Soft Start/Restart Control Section					
Saturation Voltage (2 pins)	I_{SINK} = 100µA		0.2	0.5	V
Charge Current (2 pins)		2	5	10	µA
Restart Delay Threshold		2.8	3.0	3.2	V

Guaranteed by design but not 100% tested.

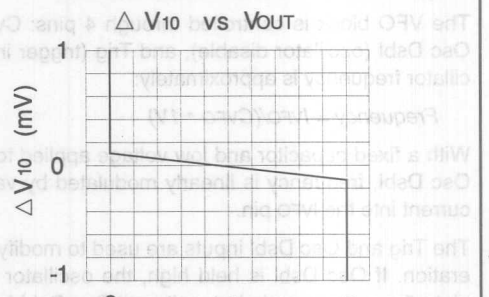
ERROR AMPLIFIER

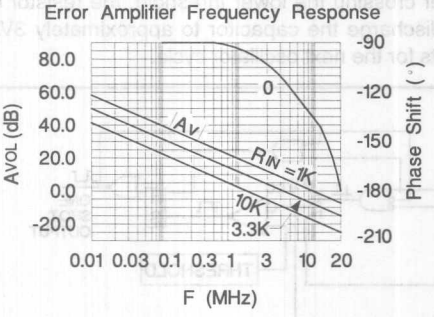
The error amplifier is a high gain, low offset, high bandwidth design with precise limits on its output swing. The bandwidth of the amplifier is externally determined by the resistance seen at the inverting input. Unity gain bandwidth is approximately:

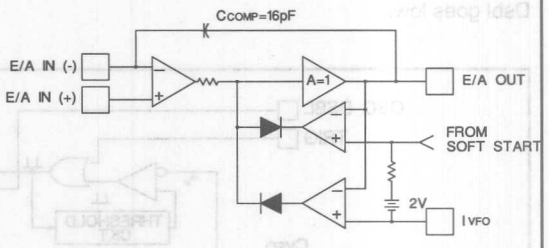
*Frequency (0dB) = 1/(2π * RIN (-) * CCOMP)*

The input common mode range of the amplifier is from 2.8 to 4.5V. As long as one pin is within this range, the other can go as low as zero.

The output swing with respect to the IVFO pin is limited from zero to 2V. Note that pulling Sft Strt (soft start) low will lower the reference of the upper clamp. The lower clamp, however, will dominate should the upper clamp reference drop below the lower reference.





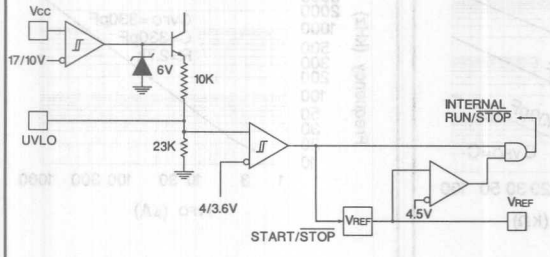


UNDER VOLTAGE LOCKOUT SECTION

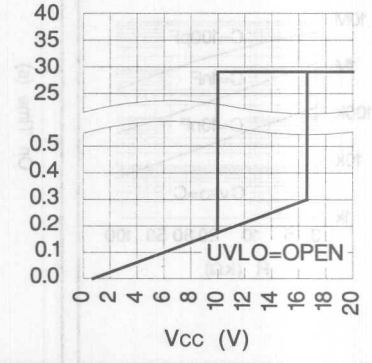
The under voltage lockout consists of three comparators that monitor VCC, UVLO and VREF. The VREF comparator makes sure that the reference voltage is sufficiently high before operation begins. When the UVLO comparator is low, the outputs are driven low, the fault latch is reset, the soft start pin is discharged, and the toggle flip-flop is loaded for output A.

The VCC comparator is used for off-line applications by leaving the UVLO pin open. In this application the supply current is typically less than 0.3mA during start-up.

The UVLO comparator is used for DC to DC applications or to gate the chip on and off. To utilize its hysteretic threshold by an external resistive divider, the internal impedance of the pin must be accounted for. To run from a 5V external supply, UVLO, VCC, and VREF are tied together.



Icc vs Vcc



VARIABLE FREQUENCY OSCILLATOR

The VFO block is controlled through 4 pins: CVFO, IVFO, Osc Dsbl (oscillator disable), and Trig (trigger input). Oscillator frequency is approximately:

*Frequency = IVFO/(CVFO * 1V)*

With a fixed capacitor and low voltage applied to Trig and Osc Dsbl, frequency is linearly modulated by varying the current into the IVFO pin.

The Trig and Osc Dsbl inputs are used to modify VFO operation. If Osc Dsbl is held high, the oscillator will complete the current cycle but wait until Osc Dsbl is returned low to initiate a new cycle. If a pulse is applied to Trig during a cycle, the oscillator will immediately initiate a new cycle. Osc Dsbl has priority over Trig, but if a trigger pulse is received while Osc Dsbl is high, the VFO will remember the trigger pulse and start a new cycle as soon as Osc Dsbl goes low.

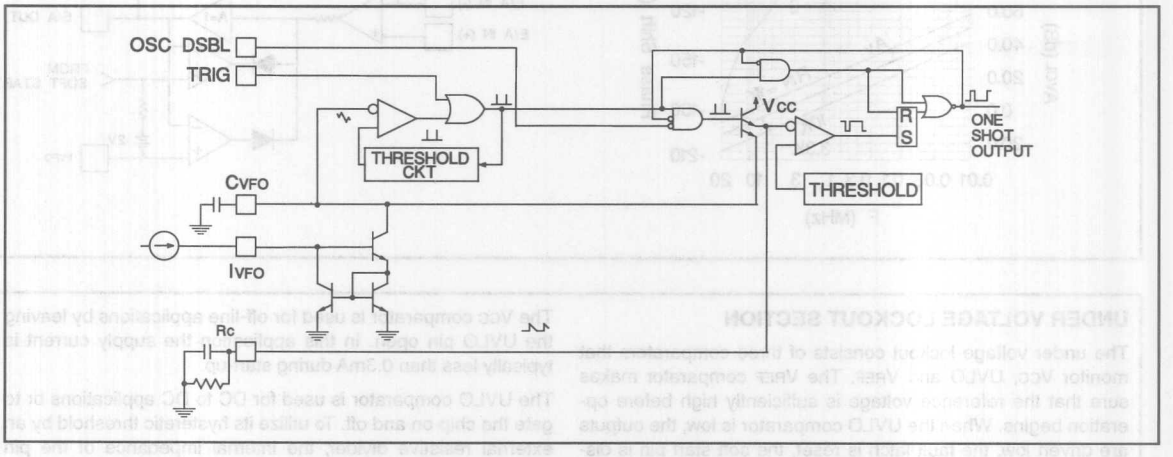
Normally low trigger pulses are used to synchronize the oscillator to a faster clock. Normally high trigger pulses can also be used to synchronize to a slower clock.

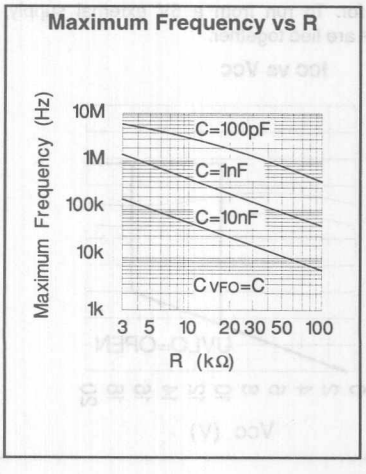
ONE SHOT TIMER

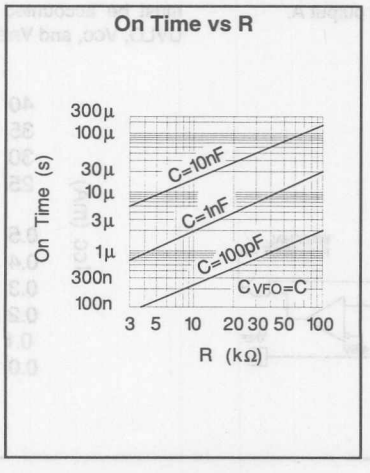
The one shot timer performs three functions and is programmed by the RC pin. The first function is to control output driver pulse width. Secondly, it clocks the toggle flip-flop. Thirdly, it establishes the maximum allowable frequency for the VFO. One shot operation is initiated at the beginning of each oscillator cycle. The RC pin, programmed by an external resistor and capacitor to ground, is charged to approximately 4.3V and then allowed to discharge. The lower threshold is approximately 80% of the peak. On time is approximately:

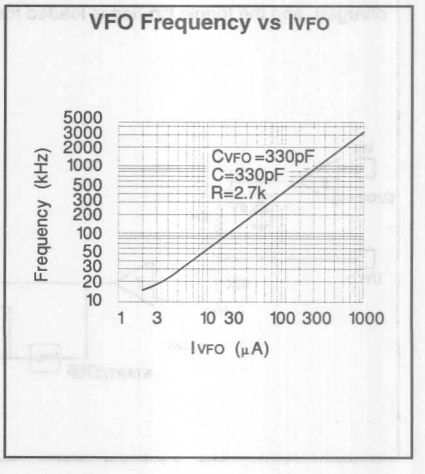
*t(on) = 0.2 * R * C.*

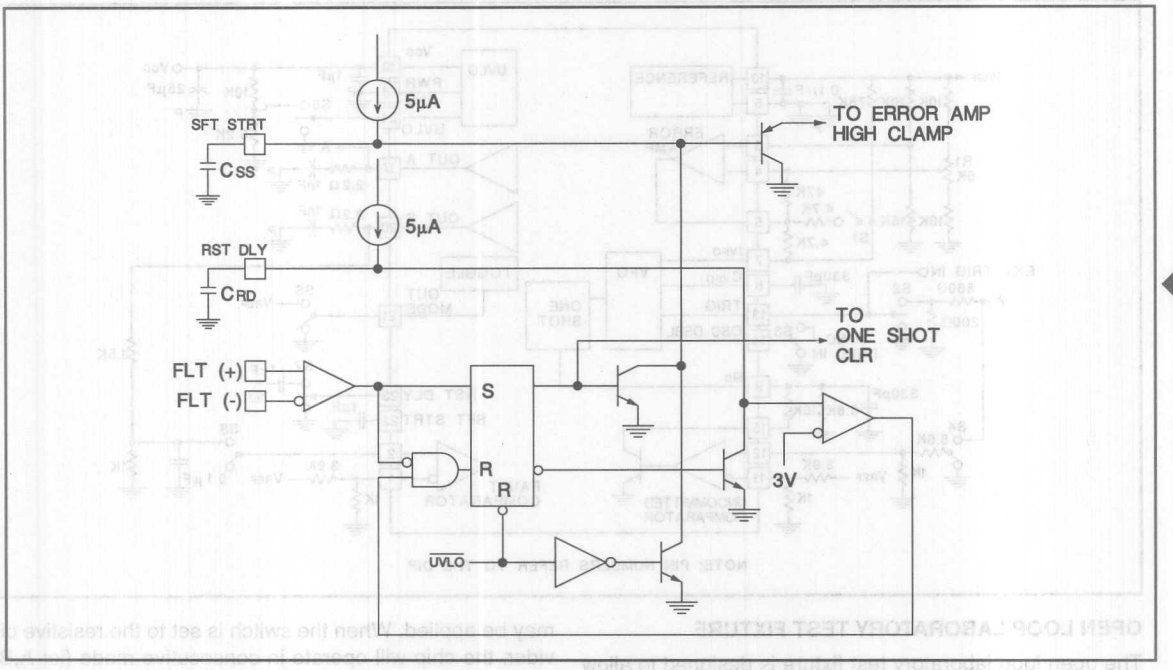
After crossing the lower threshold, the resistor continues to discharge the capacitor to approximately 3V, where it waits for the next oscillator cycle.











FAULT MANAGEMENT SECTION

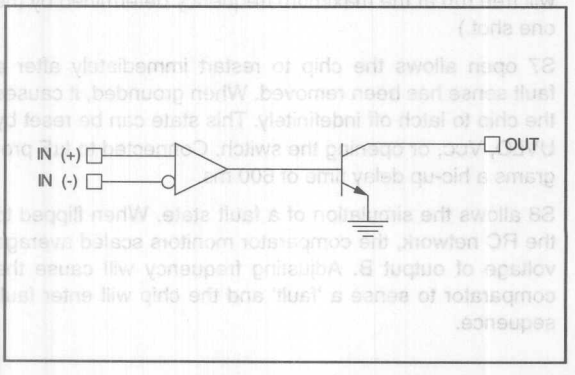
During UVLO, the fault management section is initialized. The latch is reset, and both Sft Strt (soft start) and Rst Dly (restart delay) are pulled low. When Sft Strt is low, it lowers the upper clamp of the error amplifier. As Sft Strt increases in voltage, the upper clamp increases from a value equal to the lower clamp until it is 2V more positive. A capacitor to ground from the Sft Strt pin will control the start rate.

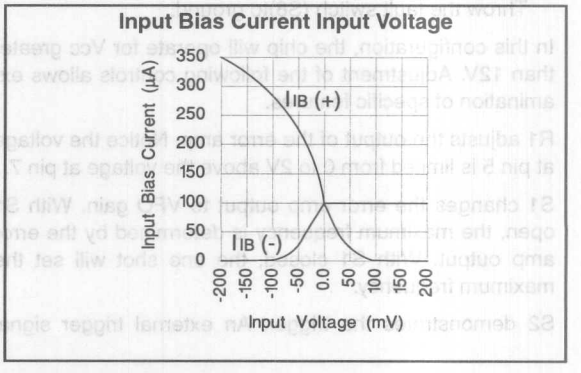
UNCOMMITTED COMPARATOR

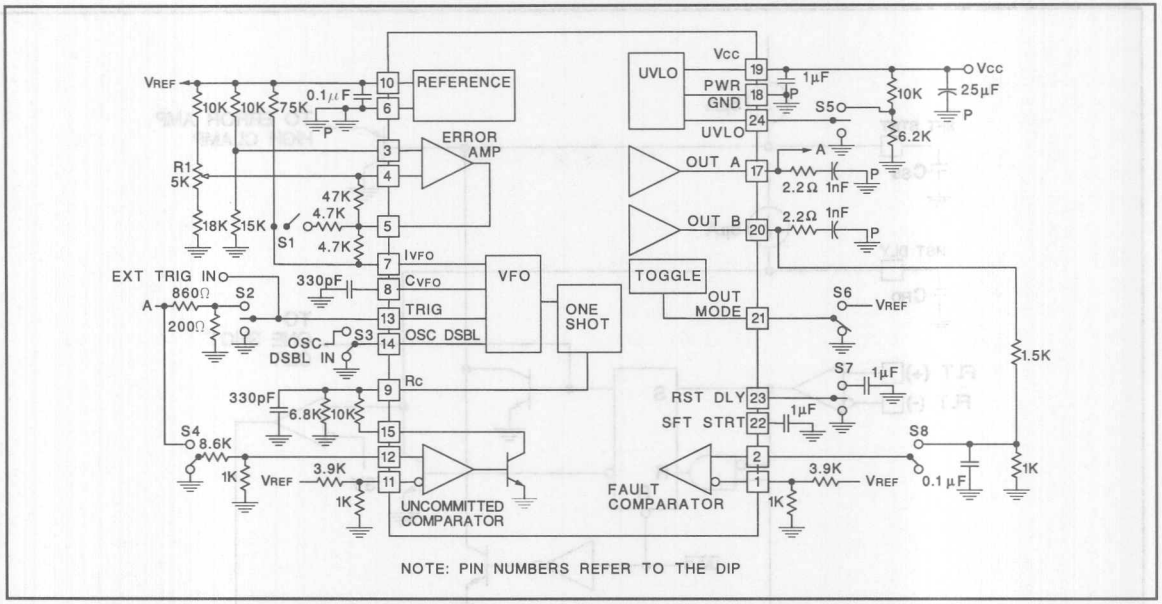
The uncommitted comparator, biased from the reference voltage, operates independently from the rest of the chip. The open collector output is capable of sinking 2mA. The inputs are valid in the common mode range of -0.3 to 3.0V. As long as one of the inputs is within this range, the other can be as high as 5V.

The high speed fault comparator will work over the input common mode range of -0.3 to 3.0V. When a fault is sensed, the one shot is immediately terminated, Sft Strt is pulled low, and Rst Dly is allowed to go high. Three modes of fault disposition can easily be implemented. If Rst Dly is externally held low, then a detected fault will shut the chip down permanently. If the Rst Dly pin is left open, a fault will simply cause an interruption of operation. If a capacitor is connected from Rst Dly to ground, then hic-up operation is implemented. The hic-up time is:

*t (off) = 600 kohm * C(Rst Dly).*







NOTE: PIN NUMBERS REFER TO THE DIP

OPEN LOOP LABORATORY TEST FIXTURE

The open loop laboratory test fixture is designed to allow familiarization with the operating characteristics of the UC3860. Note the pin numbers apply to the DIP.

To get started, preset all the options as follows:

Adjust the error amplifier variable resistor pot (R1) so the wiper is at a high potential.

Open the I_{VFO} resistor switch (S1).

Throw the Trig switch (S2) to ground.

Throw the Osc Dsbl switch (S3) to ground.

Throw the uncommitted comparator switch (S4) to ground.

Throw the UVLO switch (S5) to the resistive divider.

Throw the Out Mode switch (S6) to ground.

Open the restart delay switch (S7).

Throw the fault switch (S8)to ground.

In this configuration, the chip will operate for Vcc greater than 12V. Adjustment of the following controls allows examination of specific features.

R1 adjusts the output of the error amp. Notice the voltage at pin 5 is limited from 0 to 2V above the voltage at pin 7.

S1 changes the error amp output to VFO gain. With S1 open, the maximum frequency is determined by the error amp output. With S1 closed, the one shot will set the maximum frequency.

S2 demonstrates the trigger. An external trigger signal may be applied. When the switch is set to the resistive divider, the chip will operate in consecutive mode (ie: A,B, off,...)

S3 allows input of an external logic signal to disable the oscillator.

S4 demonstrates the uncommitted comparator. When set to output A, the comparator will accelerate the discharge of pin 9, shortening the output pulse.

S5 shorted to ground will disable the chip and the outputs will be low. If the switch is open, the Vcc start and stop thresholds are 17 and 10V. Switched to the resistive divider, the thresholds are approximately 12 and 10V.

S6 sets the mode of the toggle flip-flop. When grounded, the outputs operate alternately. Switched to 5V, the outputs switch in unison. (Note: If S6 and S2 are set for unison operation and triggered consecutive outputs, the chip will free run at the maximum frequency determined by the one shot.)

S7 open allows the chip to restart immediately after a fault sense has been removed. When grounded, it causes the chip to latch off indefinitely. This state can be reset by UVLO, Vcc, or opening the switch. Connected to 1μF programs a hic-up delay time of 600 ms.

S8 allows the simulation of a fault state. When flipped to the RC network, the comparator monitors scaled average voltage of output B. Adjusting frequency will cause the comparator to sense a 'fault' and the chip will enter fault sequence.

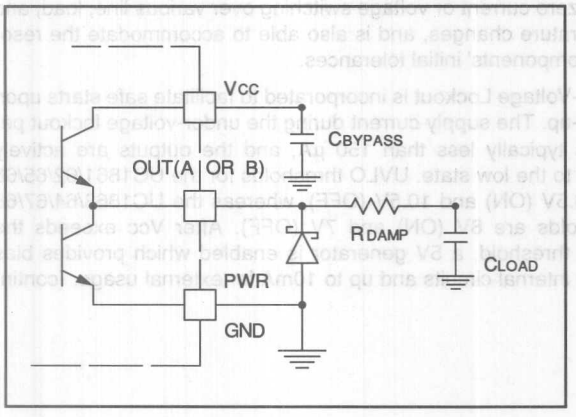
OUTPUT STAGE

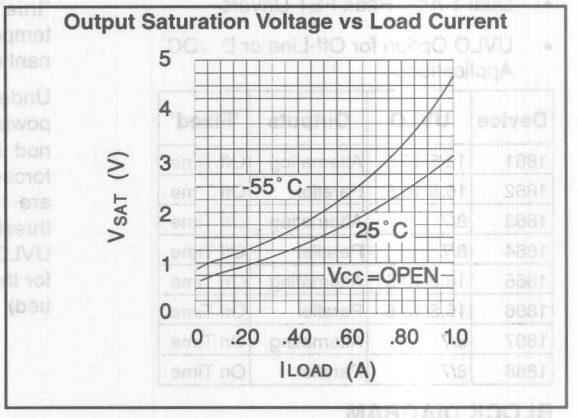
The two totem pole output stages can be programmed by Mode to operate alternately or in unison. When Mode is low the outputs alternate. During UVLO, the outputs are low.

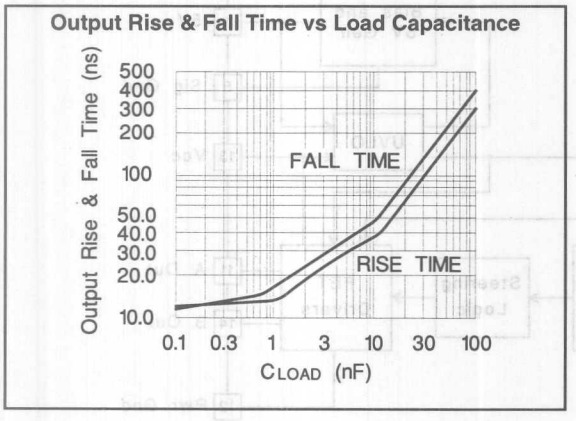
Extreme care needs to be exercised in the application of these outputs. Each output can source and sink transient currents of 2A or more and is designed for high values of dI/dt. This dictates the use of a ground plane, shielded interconnect cables, Schottky diode clamps from the output pins to Pwr Gnd (power ground), and some series resistance to provide damping. Pwr Gnd should not exceed ±0.2V from signal ground.

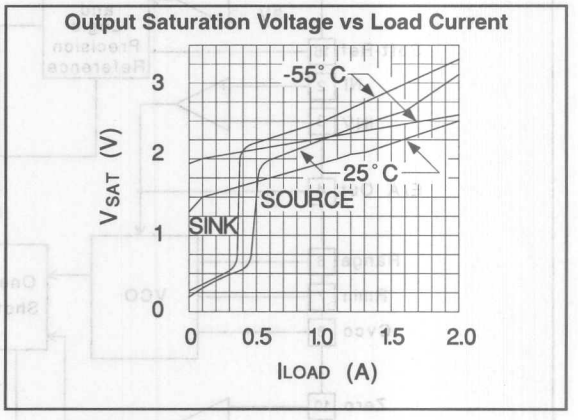
BYPASS NOTE

The reference should be bypassed with a 0.1µF ceramic capacitor from the V_{REF} pin directly to the ground plane near the Signal Ground pin. The timing capacitors on C_{VFO} and RC should be treated likewise. V_{CC}, however, should be bypassed with a ceramic capacitor from the V_{CC} pin to the section of ground plane that is connected to Power Ground. Any required bulk reservoir capacitor should parallel this one. The two ground plane sections can then be joined at a single point to optimize noise rejection and minimize DC drops.









UNITRODE CORPORATION
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TEL. (603) 424-2410 • FAX (603) 424-3460

UNITRODE

Resonant-Mode Power Supply Controllers

UC1861-1868
UC2861-2868
UC3861-3868

FEATURES

- Controls Zero Current Switched (ZCS) or Zero Voltage Switched (ZVS) Quasi-Resonant Converters
- Zero-Crossing Terminated One Shot Timer
- Precision 1%, Soft-Started 5V Reference
- Programmable Restart Delay Following Fault
- Voltage-Controlled Oscillator (VCO) with Programmable Minimum and Maximum Frequencies from 10kHz to 1MHz
- Low Start-Up Current (150µA typ.)
- Dual 1 Amp Peak FET Drivers
- UVLO Option for Off-Line or DC/DC Applications

Device	UVLO	Outputs	'Fixed'
1861	16.5/10.5	Alternating	Off Time
1862	16.5/10.5	Parallel	Off Time
1863	8/7	Alternating	Off Time
1864	8/7	Parallel	Off Time
1865	16.5/10.5	Alternating	On Time
1866	16.5/10.5	Parallel	On Time
1867	8/7	Alternating	On Time
1868	8/7	Parallel	On Time

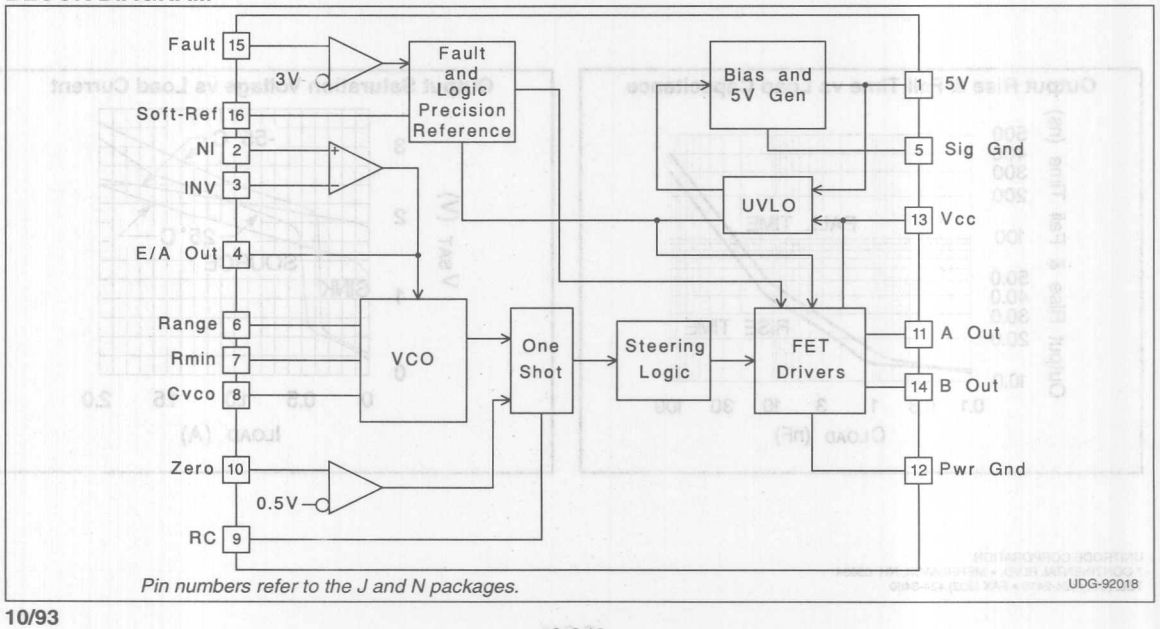
DESCRIPTION

The UC1861-1868 family of ICs is optimized for the control of Zero Current Switched and Zero Voltage Switched quasi-resonant converters. Differences between members of this device family result from the various combinations of UVLO thresholds and output options. Additionally, the one-shot pulse steering logic is configured to program either on-time for ZCS systems (UC1865-1868), or off-time for ZVS applications (UC1861-1864).

The primary control blocks implemented include an error amplifier to compensate the overall system loop and to drive a voltage controlled oscillator (VCO), featuring programmable minimum and maximum frequencies. Triggered by the VCO, the one-shot generates pulses of a programmed maximum width, which can be modulated by the Zero Detection comparator. This circuit facilitates "true" zero current or voltage switching over various line, load, and temperature changes, and is also able to accommodate the resonant components' initial tolerances.

Under-Voltage Lockout is incorporated to facilitate safe starts upon power-up. The supply current during the under-voltage lockout period is typically less than 150 µA, and the outputs are actively forced to the low state. UVLO thresholds for the UC1861/62/65/66 are 16.5V (ON) and 10.5V (OFF), whereas the UC1863/64/67/68 thresholds are 8V (ON) and 7V (OFF). After Vcc exceeds the UVLO threshold, a 5V generator is enabled which provides bias for the internal circuits and up to 10mA for external usage. (continued)

BLOCK DIAGRAM



Pin numbers refer to the J and N packages.

UDG-92018

DESCRIPTION (cont.)

A Fault comparator serves to detect fault conditions and set a latch while forcing the output drivers low. The Soft-Ref pin serves three functions: providing soft start, restart delay, and the internal system reference.

Each device features dual 1 Amp peak totem pole output drivers for direct interface to power MOSFETS. The outputs are programmed to alternate in the UC1861/63/65/67 devices. The UC1862/64/66/68 outputs operate in unison alllowing a 2 Amp peak current.

ABSOLUTE MAXIMUM RATINGS

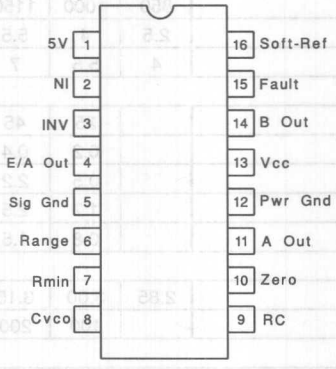
Vcc 22V
Output Current, Source or Sink (Pins 11 & 14) DC 0.5A
Pulse (0.5µs) 1.5A
Power Ground Voltage ..... ±0.2V
Inputs (Pins 2, 3, 10, & 15) ..... -0.4 to 7V
Error Amp Output Current ..... ±2mA
Power Dissipation 1W
Junction Temperature (Operating) ..... 150°C
Lead Temperature (Soldering, 10 seconds) ..... 300°C

Note 1: All voltages are with respect to signal ground and all currents are positive into the specified terminal. Pin numbers refer to the J and N packages.

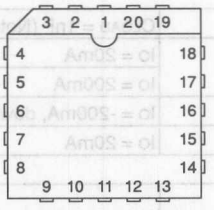
Note 2: Consult Unitrode Integrated Circuits databook for information regarding thermal specifications and limitations of packages.

CONNNECTION DIAGRAMS

DIL-16, SOIC-16 (Top View)
J or N, DW Packages



PLCC-20 & LCC-20
(Top View)
Q & L Package



PACKAGE PIN FUNCTION	
FUNCTION	PIN
Soft Ref	1
5V	2
NI	3
INV	4
E/A Out	5
Sig Gnd	6
Range	7
RMIN	8
CVCO	9
RC	10
Zero	11
NC	12
NC	13
A Out	14
Pwr Gnd	15
Pwr Gnd	16
Vcc	17
B Out	18
NC	19
Fault	20

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, all specifications apply for -55°C≤TA≤125°C for the UC186x, -25°C≤TA≤85°C for the UC286x, and 0°C≤TA≤70°C for the UC386x, Vcc=12V, CVCO=1nF, Range=7.15k, RMIN=86.6k, C=200pF, R=4.02k, and CSR=0.1µF. TA=TJ.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
5V Generator					
Output Voltage	12V ≤ Vcc ≤ 20V, -10mA ≤ Io ≤ 0mA	4.8	5.0	5.2	V
Short Circuit Current	Vo = 0V	-150		-15	mA
Soft-Reference					
Restart Delay Current	V = 2V	10	20	35	µA
Soft Start Current	V = 2V	-650	-500	-350	µA
Reference Voltage	TJ = 25°C, Io = 0A	4.95	5.00	5.05	V
	12V ≤ Vcc ≤ 20V, -200µA ≤ Io ≤ 200µA	4.85		5.15	V
Line Regulation	12V ≤ Vcc ≤ 20V		2	20	mV
Load Regulation	-200µA ≤ Io ≤ 200µA		10	30	mV
Error Amplifier (Note 3)					
Input Offset Voltage	VCM = 5V, Vo = 2V, Io = 0A	-10		10	mV
Input Bias Current	VCM = 0V	-2.0	-0.3		µA
Voltage Gain	Vcm = 5V, 0.5V ≤ Vo ≤ 3.7V, Io = 0A	70	100		dB
Power Supply Rejection Ratio	Vcm = 5V, Vo = 2V, 12V ≤ Vcc ≤ 20V	70	100		dB

ELECTRICAL CHARACTERISTICS Unless otherwise stated, all specifications apply for -55°C≤TA≤125°C for the UC186x, -25°C≤TA≤85°C for the UC286x, and 0°C≤TA≤70°C for the UC386x, VCC=12V, CVCO=1nF, Range=7.15k, RMIN=86.6k, C=200pF, R=4.02k, and Csr=0.1µF. TA=TJ.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Error Amplifier (Note 3) (cont.)					
Common Mode Rejection Ratio	0V ≤ Vcm ≤ 6V, Vo = 2V	65	100		dB
VOUT Low	VID = -100mV, Io = 200µA		0.17	0.25	V
VOUT High	VID = 100mV, Io = -200µA	3.9	4.2		V
Unity Gain Bandwidth	(Note 4)	0.5	0.8		MHz
Voltage Controlled Oscillator					
Maximum Frequency	VID (Error Amp) = 100mV, TJ = 25°C	450	500	550	kHz
	VID (Error Amp) = 100mV	425		575	kHz
Minimum Frequency	VID (Error Amp) = -100mV, TJ = 25°C	45	50	55	kHz
	VID (Error Amp) = -100mV	42		58	kHz
One Shot					
Zero Comparator Vth		0.45	0.50	0.55	V
Propagation Delay	(Note 4)		120	200	ns
Maximum Pulse Width	VZERO = 1V	850	1000	1150	ns
Maximum to Minimum Pulse	VZERO = 0V UCx861 - UCx864	2.5	4	5.5	
Width Ratio	VZERO = 0V UCx865 - UCx868	4	5.5	7	
Output Stage					
Rise and Fall Time	CLOAD = 1nF (Note 4)		25	45	ns
Output Low Saturation	Io = 20mA		0.2	0.4	V
	Io = 200mA		0.5	2.2	V
Output High Saturation	Io = -200mA, down from Vcc		1.7	2.5	V
UVLO Low Saturation	Io = 20mA		0.8	1.5	V
Fault Comparator					
Fault Comparator Vth		2.85	3.00	3.15	V
Delay to Output	(Note 4) (Note 5)		100	200	ns
UVLO					
Vcc Turn-on Threshold	UCx861, UCx862, UCx865, UCx866	15	16.5	18	V
	UCx863, UCx864, UCx867, UCx868	7	8.0	9	V
Vcc Turn-off Threshold	UCx861, UCx862, UCx865, UCx866	9.5	10.5	11.5	V
	UCx863, UCx864, UCx867, UCx868	6	7.0	8	V
Icc Start	Vcc = Vcc(on) - 0.3V		150	300	µA
Icc Run	VID = 100mV		25	32	mA

Note 1: Currents are defined as positive into the pin.
Note 2: Pulse measurement techniques are used to insure that TJ = TA.
Note 3: VID = V(NI) - V(INV).
Note 4: This parameter is not 100% tested in production but guaranteed by design.
Note 5: Vi = 0 to 4V tr(Vi) ≤ 10ns tpd = t(Vo = 6V) - t(Vi = 3V)

UVLO & 5V GENERATOR (See Figure 1): When power is applied to the chip and Vcc is less than the upper UVLO threshold, Icc will be less than 300µA, the 5V generator will be off, and the outputs will be actively held low.

When Vcc exceeds the upper UVLO threshold, the 5V generator turns on. Until the 5V pin exceeds 4.9V, the outputs will still remain low.

The 5V pin should be bypassed to signal ground with a 0.1µF capacitor. The capacitor should have low equivalent series resistance and inductance.

FAULT AND SOFT-REFERENCE (See Figure 1): The Soft-Ref pin serves three functions: system reference, restart delay, and soft-start. Designed to source or sink 200µA, this pin should be used as the input reference for the error amplifier circuit. This pin requires a bypass capacitor of at least 0.1µF. This yields a minimum soft-start time of 1ms.

Under-Voltage Lockout sets both the fault and restart delay latches. This holds the outputs low and discharges the Soft-Ref pin. After UVLO, the fault latch is reset by the

sets the delay latch and Soft-Ref charges via the 0.5mA current source.

The fault pin is input to a high speed comparator with a threshold of 3V. In the event of a detected fault, the fault latch is set and the outputs are driven low. If Soft-Ref is above 4V, the delay latch is set. Restart delay is timed as Soft-Ref is discharged by 20µA. When Soft-Ref is fully discharged, the fault latch is reset if the fault input signal is low. The Fault pin can be used as a system shutdown pin.

If a fault is detected during soft-start, the fault latch is set and the outputs are driven low. The delay latch will remain reset until Soft-Ref charges to 4V. This sets the delay latch, and restart delay is timed. Note that restart delay since Soft-Ref must be discharged from 5V instead of 4V.

The restart delay to soft-start time ratio is 24:1 for a fault occurring during normal operation and 19:1 for faults occurring during soft-start. Shorter ratios can be programmed down to a limit of approximately 3:1 by the addition of a 20kΩ or larger resistor from Soft-Ref to ground.

A 100kΩ resistor from Soft-Ref to 5V will have the effect of permanent shut down after a fault since the internal 20µA current source can't pull Soft-Ref low. This feature can be used to require recycling Vcc after a fault. Care must be taken to insure Soft-Ref is indeed low at start up, or the fault latch will never be reset.

UVLO, 5V, Fault, and Soft-Ref

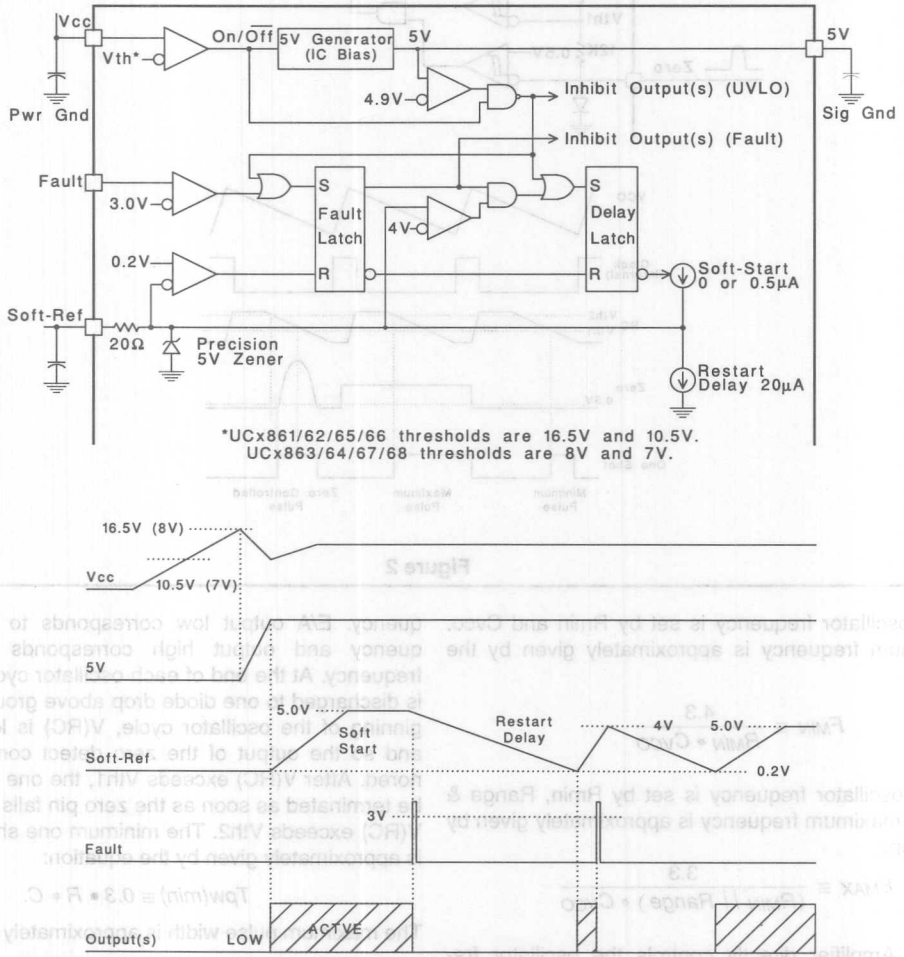


Figure 1

Error Amp, Voltage Controlled Oscillator, and One Shot

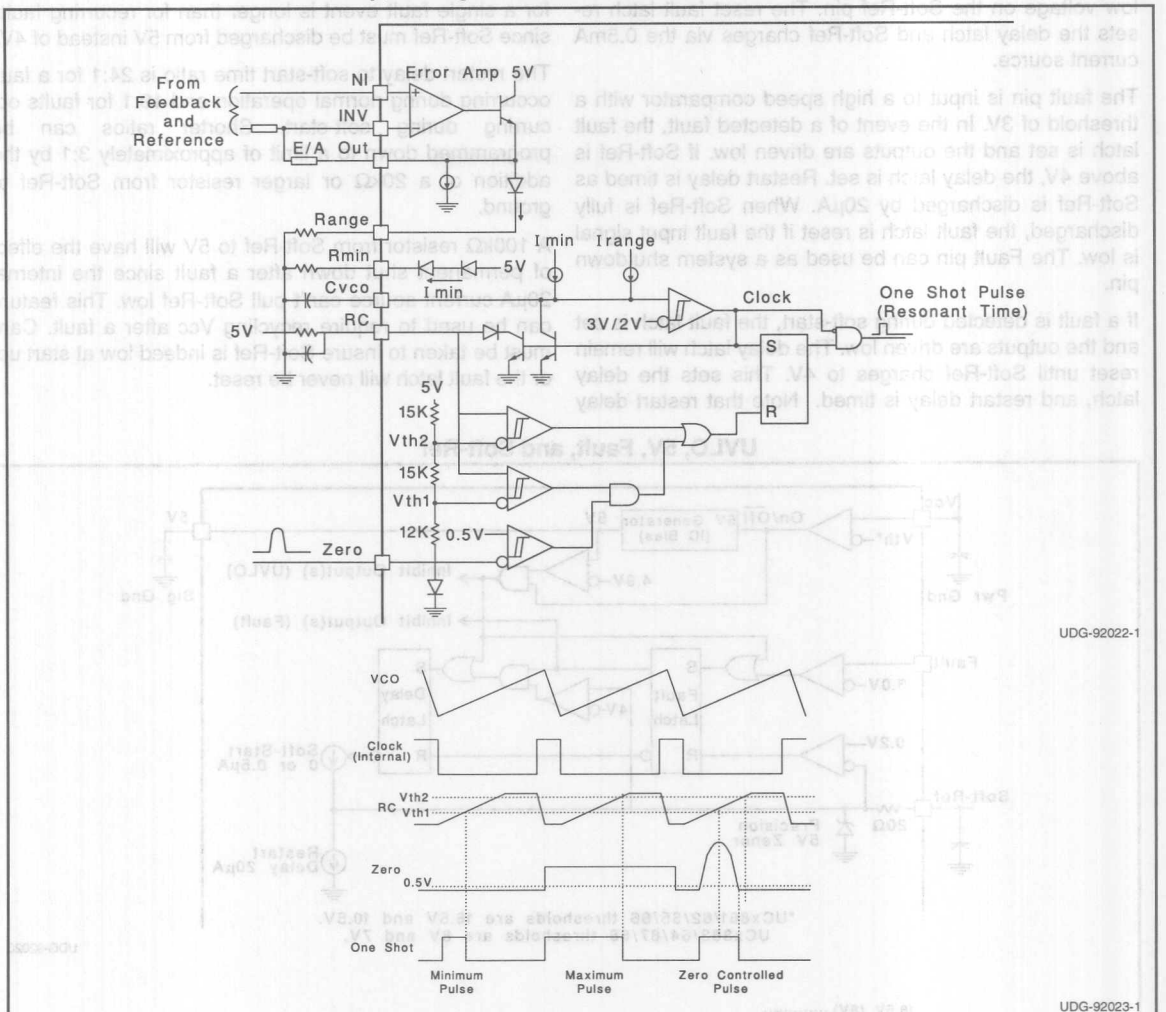


Figure 2

Minimum oscillator frequency is set by Rmin and Cvco. The minimum frequency is approximately given by the equation:

$$F_{MIN} \cong \frac{4.3}{R_{MIN} \bullet C_{VCO}}$$

Maximum oscillator frequency is set by Rmin, Range & Cvco. The maximum frequency is approximately given by the equation:

$$F_{MAX} \cong \frac{3.3}{(R_{MIN} \,//\, Range) \bullet C_{VCO}}$$

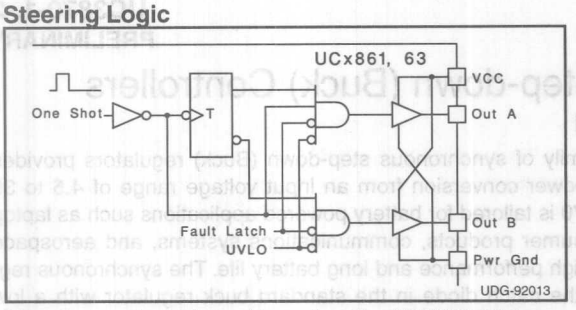
The Error Amplifier directly controls the oscillator frequency. E/A output low corresponds to minimum frequency and output high corresponds to maximum frequency. At the end of each oscillator cycle, the RC pin is discharged to one diode drop above ground. At the beginning of the oscillator cycle, V(RC) is less than Vth1 and so the output of the zero detect comparator is ignored. After V(RC) exceeds Vth1, the one shot pulse will be terminated as soon as the zero pin falls below 0.5V or V(RC) exceeds Vth2. The minimum one shot pulse width is approximately given by the equation:

$$Tpw(min) \cong 0.3 \bullet R \bullet C.$$

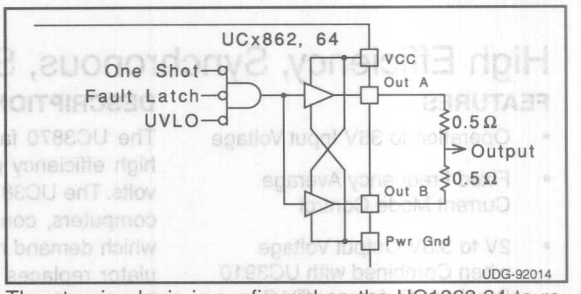
The maximum pulse width is approximately given by:

$$Tpw(max) \cong 1.2 \bullet R \bullet C.$$

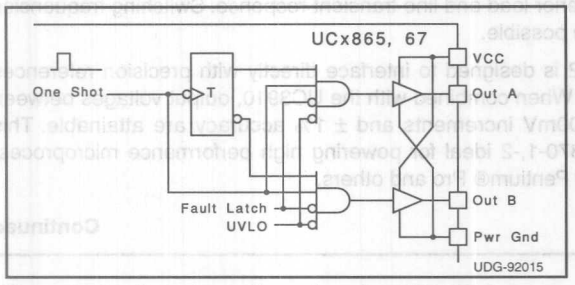
Steering Logic



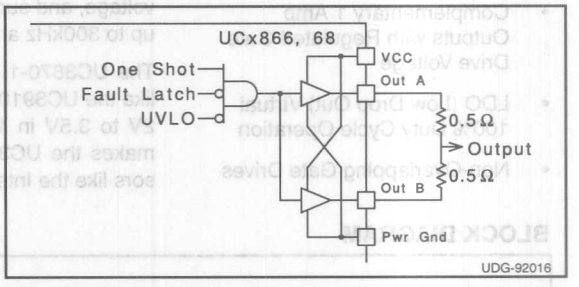
The steering logic is configured on the UC1861,63 to result in dual non-overlapping square waves at outputs A & B. This is suited to drive dual switch ZVS systems.



The steering logic is configured on the UC1862,64 to result in inverted pulse trains occurring identically at both output pins. This is suited to drive single switch ZVS systems. Both outputs are available to drive the same MOSFET gate. It is advisable to join the pins with 0.5 ohm resistors.



The steering logic is configured on the UC1865,67 to result in alternating pulse trains at outputs A & B. This is suited to drive dual switch ZCS systems.



The steering logic is configured on the UC1866,68 to result in non-inverted pulse trains occurring identically at both output pins. This is suited to drive single switch ZCS systems. Both outputs are available to drive the same MOSFET gate. It is advisable to join the pins with 0.5 ohm resistors.

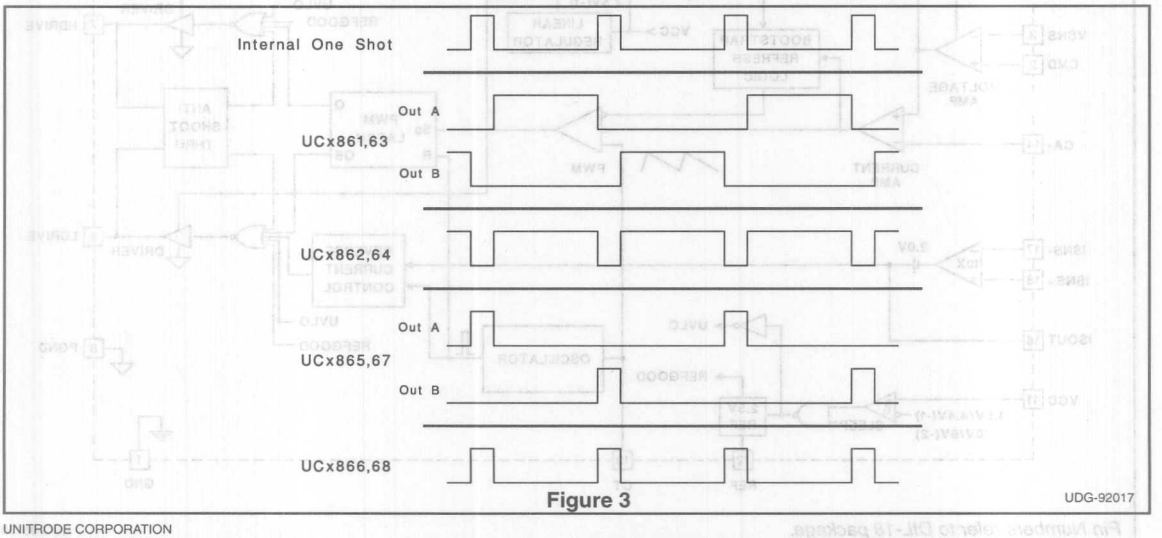


Figure 3

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

High Efficiency, Synchronous, Step-down (Buck) Controllers

FEATURES

- Operation to 36V Input Voltage
- Fixed Frequency Average Current Mode Control
- 2V to 3.5V Output Voltage when Combined with UC3910 Precision Reference/DAC
- Drives External N-Channel MOSFETs for Highest Efficiency
- Sleep Mode Current <50µA
- Complementary 1 Amp Outputs with Regulated Gate Drive Voltage
- LDO (Low Drop Out) Virtual 100% Duty Cycle Operation
- Non-Overlapping Gate Drives

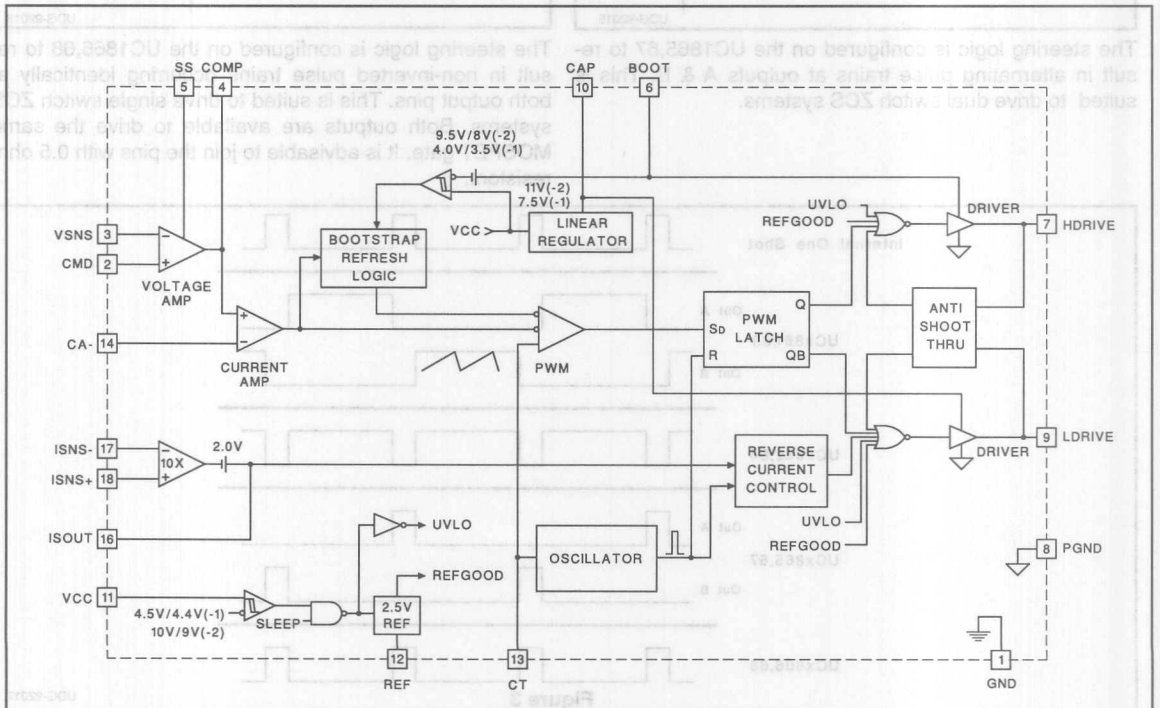
DESCRIPTION

The UC3870 family of synchronous step-down (Buck) regulators provides high efficiency power conversion from an input voltage range of 4.5 to 36 volts. The UC3870 is tailored for battery powered applications such as laptop computers, consumer products, communications systems, and aerospace which demand high performance and long battery life. The synchronous regulator replaces the catch diode in the standard buck regulator with a low $R_{DS(on)}$ N-channel MOSFET switch allowing for significant efficiency improvements. The high side N-channel MOSFET switch is driven out of phase from the low side N-channel MOSFET switch by an on-chip bootstrap circuit which requires only a single external capacitor to develop the regulated gate drive. Fixed frequency, average current mode control provides the regulator with inherent slope compensation, tight regulation of the output voltage, and superior load and line transient response. Switching frequencies up to 300kHz are possible.

The UC3870-1,-2 is designed to interface directly with precision references like the UC3910. When combined with the UC3910, output voltages between 2V to 3.5V in 100mV increments and ± 1% accuracy are attainable. This makes the UC3870-1,-2 ideal for powering high performance microprocessors like the Intel Pentium® Pro and others.

Continued

BLOCK DIAGRAM



Pin Numbers refer to DIL-18 package.

UDG-96158

DESCRIPTION (cont.)

A low power sleep mode can be invoked through the SS pin. Quiescent supply current in sleep mode is typically less than 50µA. Two UVLO options are available. The UC3870-1 is designed for logic level MOSFETs and has UVLO turn-on and turn-off thresholds of 4.5V and 4.4V respectively. The UC3870-2 is designed for standard power MOSFETs and has UVLO turn-on and turn-off thresholds of 10V and 9V respectively. A precision 2.5V reference can supply 20mA to external circuitry. An error amplifier with soft start, high bandwidth current amplifier, and a synchronizable oscillator are additional features.

Available packages include 18-pin plastic and ceramic DIP (N, J), 18-pin SOIC (DW), and 20-pin plastic and ceramic leadless chip carriers (Q, L).

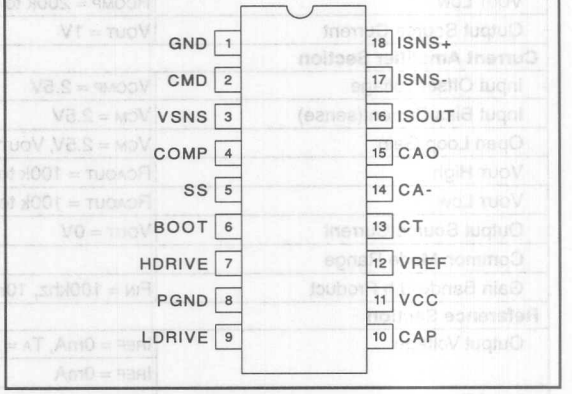
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (VCC) 36V
Boost Voltage (BOOT) 50V
OUTPUT Drivers (HDRIVE, LDRIVE) Currents
(continuous) . . . . . .±0.25A
(peak) . . . . . .±1A
VREF Current . . . . . .Internally Limited
Inputs (VSNS, SS, COMP, CT) . . . . . .–0.3 to 10V
Inputs (ISNS+, ISNS-) . . . . . .–0.3 to20V
Outputs (CAO) . . . . . .–0.3 to10V
Soft Start Sinking Current 1.5mA
Storage Temperature . . . . . .–65°C to +150°C
Junction Temperature . . . . . .–65°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . .+300°C

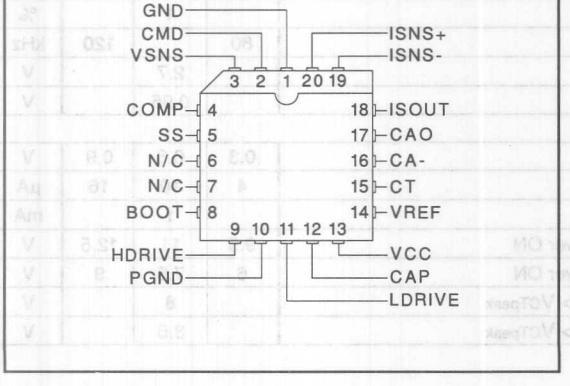
All currents are positive into, negative out of the specified terminal.
All voltages are referenced to GND.
Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAMS

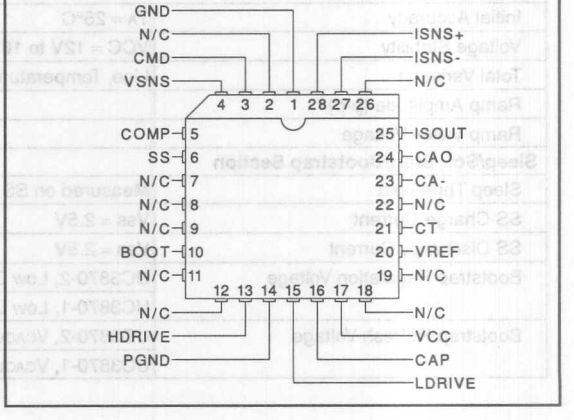
DIL-18, (Top View)
J or N, DW Packages



PLCC-20 (Top View)
Q Package



LCC-28 (Top View)
L Package



ELECTRICAL CHARACTERISTICS (cont) Unless otherwise stated these specifications apply for T_A = –55°C to +125°C for UC1870X; –25°C to +85°C for UC2870X; 0°C to +70°C for UC3870X; VCC = 12V, CT = 680pF, C_{CAP} = 1µF; C_{BOOT} = 0.1µF, V_{COMP} = 2.5V, V_{CAOUT} = 2.5V, T_A = T_J.

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
Overall Section					
Supply Current, Sleep	SOFTSTART = 0V		50		µA
Supply Current, Operating			8.5		mA
VCC Turn-on Threshold	UC3870-2		10	10.5	V
	UC3870-1		4.5	4.8	V
VCC Turn-off Threshold	UC3870-2	8.5	9		V
	UC3870-1	4.1	4.4		V
Voltage Amplifier Section					
Input Voltage Offset	T_A = 25°C		0		mV
VSNS Bias Current		–500	25	500	nA
Transconductance	I_{COMP} = –7.5µA to +7.5µA		675		µMho
V_{OUT} High	R_{COMP} = 200k to GND		3.2		V
V_{OUT} Low	R_{COMP} = 200k to VREF		0.15		V
Output Source Current	V_{OUT} = 1V		35		µA
Current Amplifier Section					
Input Offset Voltage	V_{COMP} = 2.5V	–10	0	10	mV
Input Bias Current(sense)	V_{CM} = 2.5V	–500		500	nA
Open Loop Gain	V_{CM} = 2.5V, V_{OUT} = 1V to 3.5V	80	110		dB
V_{OUT} High	R_{CAOUT} = 100k to GND		3.7		V
V_{OUT} Low	R_{CAOUT} = 100k to VREF		0.7		V
Output Source Current	V_{OUT} = 0V	80	100	120	µA
Common Mode Range		–0.3		3	V
Gain Bandwidth Product	F_{IN} = 100khz, 10mV p-p	2	3.5		MHz
Reference Section					
Output Voltage	I_{REF} = 0mA, T_A = 25°C	2.45	2.5	2.55	V
	I_{REF} = 0mA	2.425	2.5	2.575	V
Load Regulation	I_{REF} = 0mA to 5mA		2	15	mV
Line Regulation	VCC = 12V to 24V		2	15	mV
Short Circuit Current	VREF = 0V	10	20	25	mA
Oscillator Section					
Initial Accuracy	T_A = 25°C		100		kHz
Voltage Stability	VCC = 12V to 18V		1		%
Total Variation	Line, Temperature	80		120	kHz
Ramp Amplitude (p-p)			2.7		V
Ramp Valley Voltage			0.95		V
Sleep/Soft Start/Bootstrap Section					
Sleep Threshold	Measured on SS	0.3	0.6	0.9	V
SS Charge Current	Vss = 2.5V	4	10	16	µA
SS Discharge Current	Vss = 2.5V		1		mA
Bootstrap Regulation Voltage	UC3870-2, Low Driver ON	9.5	11	12.5	V
	UC3870-1, Low Driver ON	6	7.5	9	V
Bootstrap Refresh Voltage	UC3870-2, V_{CAOUT} > V_{CTpeak}		8		V
	UC3870-1, V_{CAOUT} > V_{CTpeak}		3.5		V

ELECTRICAL CHARACTERISTICS (cont) Unless otherwise stated these specifications apply for T_A = –55°C to +125°C for UC1870X; –25°C to +85°C for UC2870X; 0°C to +70°C for UC3870X; VCC = 12V, CT = 680pF, C_{CAP} = 1µF; C_{BOOT} = 0.1µF, V_{COMP} = 2.5V, V_{CAOUT} = 2.5V, T_A = T_J.

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
High Side Driver Output Section					
Output High Voltage	I_{OUT} = –50mA, BOOT = 23V	21	22.2		V
Output Low Voltage	I_{OUT} = 50mA		1	2.2	V
	I_{OUT} = 10mA		300	500	mV
Output Low (UVLO)	I_{OUT} = 50mA, VCC = 0V		0.9	1.5	V
Output Rise Time	C_{OUT} = 1nf		100		ns
Output Fall Time	C_{OUT} = 1nf		100		ns
Low Side Driver Output Section					
Output High Voltage	I_{OUT} = –50mA, V_{CAP} = 11V	8.8	9.5		V
Output Low Voltage	I_{OUT} = 50mA		1	2.2	V
	I_{OUT} = 10mA		300	500	mV
Output Low (UVLO)	I_{OUT} = 50mA, VCC = 0V		0.9	1.5	V
Output RISE/FALL Time	C_{LOAD} = 1nF		100		ns
Output FALL Time	C_{OUT} = 1nF		100		ns
X10 Amplifier Section					
Gain	V_{ISNS+} - V_{ISNS-} = 20mV to 80mV		10		V/V
Output Offset voltage	V_{ISNS+} = V_{ISNS-}	1.9	2	2.1	V
PSRR	VCC = 12V to 24V		tbd		
Common Mode Rejection	V_{ISNS+} = V_{ISNS-} = 0V to 2V		tbd		dB
Slew Rate Rising			tbd		V/µs
Slew Rate Falling			tbd		V/µs
Input Resistance	T_J = 25°C	75	100	150	kΩ

PIN DESCRIPTIONS

BOOT: This pin provides the high side rail for the HDRIVE output. An external capacitor (C_{BST}) is connected between this pin and the drain of the external low side MOSFET. When the low side MOSFET is conducting C_{BST} is charged to 11V (UC3870-2), 7.5V (UC3870-1), via an external diode tied to CAP. When the low side MOSFET turns off and the high side MOSFET turns on, the C_{BST} bootstraps itself up with the source of high side MOSFET, ultimately providing a 10V V_{GS} for the upper MOSFET. Since this 10V is referenced to the source of the high side N-channel MOSFET, the actual voltage on BOOT and HDRIVE is approximately 10V above VCC while the high side MOSFET is conducting. The voltage on BOOT is continuously monitored during low input voltage conditions when the duty cycle equals approximately 100% to insure that a sufficient gate drive level is being supplied by the UC3870. If the voltage on BOOT falls below 8V (UC3870-2) or 3.5V (UC3870-1), the IC forces the low side driver to cycle itself on for the few cycles required to replenish C_{BST}. In this way, virtual 100% duty cycle operation is provided.

CA-: This is the inverting input to the current amplifier. Connect a series resistor and capacitor between this pin and CAO to set the current loop compensation. An input resistor between this pin and ISOUT provides the inductor current sense signal to the amplifier and also sets the high frequency gain of the amplifier. The common mode operating range for this input is between GND and 4V. The normal range during operation is between 2V and 3V.

CAO: This is the output of the wide bandwidth current amplifier and one of the inputs to the PWM duty cycle comparator. The output signal generated by this amplifier commands the PWM to force the correct duty cycle to maintain output voltage in regulation. The output can swing from 0.1V to 4V.

CAP: A capacitor is normally connected between this pin and GND providing bypass for the internal 11V (UC3870-2) and 7.5V (UC3870-1) regulator. Charge is transferred from this capacitor to C_{BST} via an external diode when the low side MOSFET is conducting. If VCC ≤ 10V logic level MOSFETs are generally specified. CAP should then be shorted to VCC in conjuncton with a low VF Schottky to BOOT to maximize the gate drive amplitude. This technique provides adequate gate drive signal amplitudes with VCC as low as 4.5V. For high input volt-

age applications, a simple external shunt zener regulator circuit can be connected to CAP, thereby offloading power dissipation requirements from the IC to an external transistor.

COMP: This is the output of the voltage amplifier. It provides the current command signal to the current amplifier. The voltage is clamped to approximately 3.2V.

CMD: This is the non-inverting input of the voltage error amplifier. The voltage applied to CMD sets the output voltage of the power converter. The 2V to 3.5V input common mode range allows for direct interfacing to the UC3910 DAC/precision reference.

CT: A capacitor from CT to GND sets the PWM oscillator frequency according to the following equation:

$$F = \frac{1}{14250 \bullet CT}.$$

Use a high quality ceramic capacitor with low ESL and ESR for best results. A minimum CT value of 220pF insures good accuracy and less susceptibility to circuit layout parasitics. The oscillator and PWM are designed to provide practical operation to 300kHZ.

GND: All voltages are measured with respect to this pin. All bypass capacitors and timing components except those listed under the PGND pin description should be connected to this pin. Component leads should be as short and direct as possible.

HDRIVE, LDRIVE: The outputs of the PWM are totem pole MOSFET gate drivers on the HDRIVE and LDRIVE pins. The outputs can sink approximately 1A and source 500mA. This characteristic optimizes the switching transitions by providing a controlled dV/dT at turn-on and a lower impedance at turn-off. These are complementary outputs with a typical deadtime of 200ns. Internal circuitry prevents the possibility of simultaneous conduction of the output MOSFETs (shoot through). HDRIVE is the high side bootstrapped output. Its upper power supply rail is the BOOT pin which means that its output will fly approximately 10V above VCC when the upper side of the totem pole output is conducting. The power supply rail for LDRIVE is CAP. As a result the V_{GS} of both gates are regulated to approximately 10V if VCC is >11V. A series resistor between these pins and the MOSFET gates of at least 10 ohms can be used to control ringing. Additionally, a low VF Schottky diode should be connected between these pins and GND to prevent substrate conduction and possible erratic operation.

ISNS-: This is the inverting input to the X10 instrumentation amplifier. The common mode input range for this pin extends from GND to VCC. A low value resistor in series with the output inductor is connected between this pin and ISNS+ to develop the current sense signal.

ISNS+: This is the non-inverting input to the X10 instrumentation amplifier. The common mode input range for this pin extends from GND to VCC.

ISOUT: This is the output of the X10 instrumentation amplifier. The output voltage on this pin is level shifted 2V above GND, such that if a 100mV differential input is applied across ISNS+ and ISNS-, the output will be 3V.

PGND: This is the high current ground for the IC. The MOSFET driver transistors are referenced to this ground. For best performance an external star ground connection should be made between this pin, the source of the low side MOSFET, the capacitor on CAP, the anodes of any external Schottky clamp diodes and the output filter capacitor. As with all high frequency layouts, a ground plane and short leads are highly recommended.

SS: A capacitor from this pin to GND in conjunction with an internal 10μA current source provides a soft start function for the IC. The voltage level on SS clamps the output of the voltage amplifier through an internal buffer, thus providing a controlled startup. The SS time is approximately:

$$\frac{Css \bullet \left(\frac{V_O}{V_{IN}}\right) \bullet 3V}{10\mu A}.$$

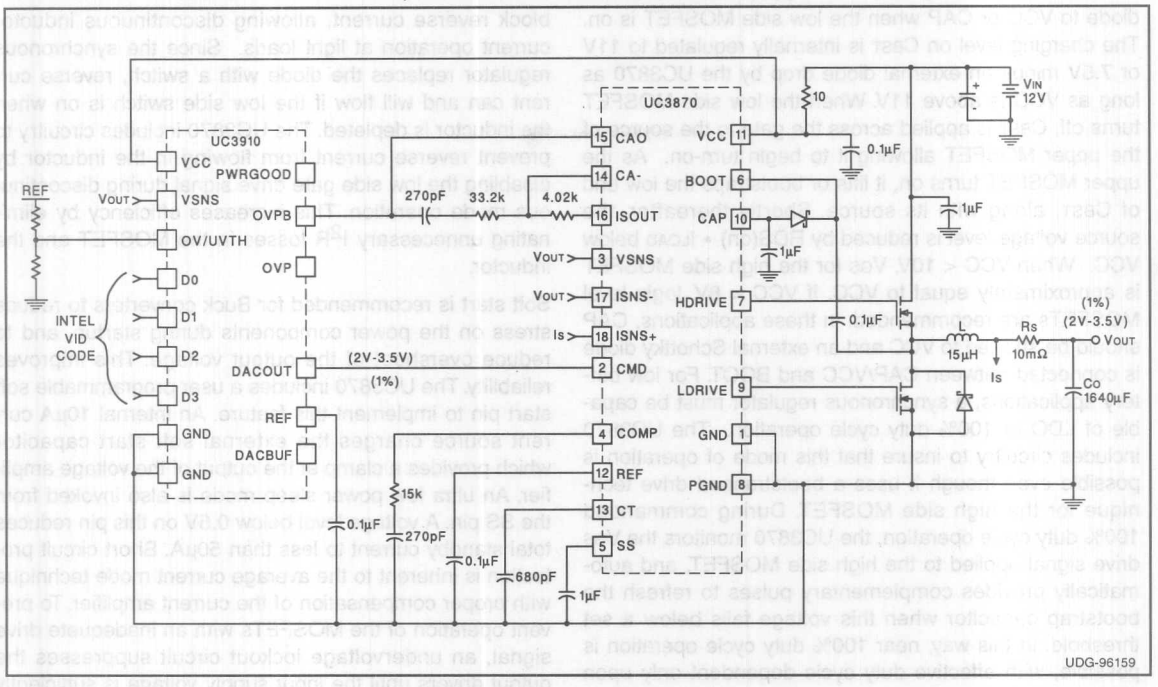
Once the device has completed its soft start cycle, a low power sleep mode can be invoked by pulling SS below 0.5V typically. In sleep mode, all of the device functions are disabled except for those which are required to bring the device out of sleep mode when SS is released. Typical sleep mode supply current is less than 50μA.

VCC: Positive supply rail for the IC. Bypass this pin to GND with a 1μF low ESL/ESR ceramic capacitor. The maximum voltage for VCC is 36V. The turn on voltage level on VCC is 4.5V with 100mV of hysteresis for the UC3870-1 and 10V with 1V of hysteresis for the UC3870-2.

VREF: VREF is the output of the precision reference. The output is capable of supplying 20mA to peripheral circuitry and is internally short circuit current limited. VREF is disabled and low whenever VCC is below the UVLO threshold, and when SS is pulled below 0.5V. A VREF "GOOD" comparator senses VREF and disables the PWM stage until VREF has attained approximately 90% of its nominal value. Bypass VREF to GND with a 0.1μF ceramic capacitor for best performance.

VSNS: This pin is the inverting input of the voltage amplifier and serves as the output voltage feedback point for the synchronous regulator. It senses the output voltage through a voltage divider which produces a nominal 2V.

TYPICAL APPLICATION: UC3870-1,-2 Pentium® Pro Power Converter



OPERATION: Refer to Application Schematic

The UC3870 employs a fixed frequency average current mode control Buck topology to convert a higher battery voltage down to a tightly regulated output voltage. Special design techniques allow this bipolar IC to deliver exceptional performance while consuming approximately 6mA of supply current over an input voltage range of 4.5 to 35 volts. Fixed frequency operation allows synchronization to an existing system clock, and easier filtering. Average current mode control provides inherent slope compensation and accurate short circuit current limiting.

The output inductor current is sensed by an external low value shunt resistor (RSENSE). This signal at full load current should be no larger than 100mV in order to minimize sensing losses. The differential voltage across RSENSE is amplified by the internal X10 instrumentation amplifier. The common mode input range for this amplifier extends from GND to VCC in order to maintain accurate current sensing under normal conditions as well as abnormal conditions such as output short circuit and low drop out (LDO) modes. The output of the X10 instrumentation amplifier is applied to the inverting input of the current amplifier through an external resistor. The converter's output voltage feedback is applied to the VSNS pin through an external voltage divider. The difference between the voltage at VSNS and the voltage at the non-inverting input is amplified by the voltage amplifier and applied to the non-inverting input of the current amplifier. This instantaneous reference level forms the current command input for the average current control loop. The average current amplifier develops the duty cycle command signal by integrating the current feedback signal with respect to the instantaneous current command input. This output is compared to the fixed high amplitude oscillator ramp waveform at the inputs of the PWM comparator to develop duty cycle information for the PWM drive. The large amplitude oscillator ramp provides both high noise margin and built-in slope compensation in average current mode control methodology. The fixed frequency oscillator is programmed with a single external capacitor connected between CT and GND, and is capable of switching frequencies up to 300kHz. The UC3870 can be synchronized to an external clock by capacitively coupling the signal to the junction of the capacitor at CT and a low value resistor tied to GND. Refer to Application Note U-111.

The PWM drive signal is applied to the complementary output driver stages. Since the high side switch is an N-channel MOSFET, a means for driving its gate above VCC is required. This is accomplished via the internal 11V (UC3870-2)/7.5V (UC3870-1) regulator and an external capacitor (CBST). CBST is charged through an external

OPERATION (cont): Refer to Application Schematic

diode to VCC or CAP when the low side MOSFET is on. The charging level on C_{BST} is internally regulated to 11V or 7.5V minus an external diode drop by the UC3870 as long as VCC is above 11V. When the low side MOSFET turns off, C_{BST} is applied across the gate to the source of the upper MOSFET allowing it to begin turn-on. As the upper MOSFET turns on, it lifts or bootstraps the low end of C_{BST}, along with its source. Shortly thereafter, the source voltage level is reduced by RDS(on) • I_{LOAD} below VCC. When VCC < 10V, V_{GS} for the high side MOSFET is approximately equal to VCC. If VCC < 8V, logic level MOSFETs are recommended. In these applications, CAP should be shorted to VCC and an external Schottky diode is connected between CAP/VCC and BOOT. For low battery applications, a synchronous regulator must be capable of LDO or 100% duty cycle operation. The UC3870 includes circuitry to insure that this mode of operation is possible even though it uses a bootstrapped drive technique for the high side MOSFET. During commanded 100% duty cycle operation, the UC3870 monitors the V_{GS} drive signal applied to the high side MOSFET, and automatically provides complementary pulses to refresh the bootstrap capacitor when this voltage falls below a set threshold. In this way, near 100% duty cycle operation is possible, with effective duty cycle dependent only upon the value of C_{BST}.

High efficiency is obtained primarily by the low side MOSFET which replaces the Schottky diode in the standard Buck configuration. Its low R_{DS}(on) produces a much lower voltage drop than a low VF Schottky diode. As output voltages get lower, these improvements become more evident.

Another efficiency consideration is the the possibility of reverse current in the output inductor. For a non-synchronous regulator this isn't a problem since the diode will block reverse current, allowing discontinuous inductor current operation at light loads. Since the synchronous regulator replaces the diode with a switch, reverse current can and will flow if the low side switch is on when the inductor is depleted. The UC3870 includes circuitry to prevent reverse current from flowing in the inductor by disabling the low side gate drive signal during discontinuous mode operation. This increases efficiency by eliminating unnecessary I^2R losses in the MOSFET and the inductor.

Soft start is recommended for Buck converters to reduce stress on the power components during startup, and to reduce overshoot of the output voltage. This improves reliability. The UC3870 includes a user programmable soft start pin to implement this feature. An internal 10µA current source charges the external soft start capacitor which provides a clamp at the output of the voltage amplifier. An ultra low power sleep mode is also invoked from the SS pin. A voltage level below 0.5V on this pin reduces total standby current to less than 50µA. Short circuit protection is inherent to the average current mode technique with proper compensation of the current amplifier. To prevent operation of the MOSFETs with an inadequete drive signal, an undervoltage lockout circuit suppresses the output drivers until the input supply voltage is sufficiently high enough for proper operation. The UC3870-1 is intended for applications with logic level MOSFETs and its VCC turn-on and turn-off thresholds are 4.5V/4.4V respectively. The UC3870-2 is intended for applications with standard MOSFETs and has UVLO turn-on and turn-off thresholds of 10V and 9V respectively. The precision 2.5V reference can provide 10mA to power external circuitry. The reference output is disabled during UVLO and sleep modes.

ORDERING INFORMATION

UC [ ] 870 [ ] — [ ]

- UVLO Threshold
- Package
- Temperature Range

UVLO Turn On/Off Threshold	Package	Temperature Range
1: 4.5V/4.4V	J: Ceramic DIL-18	1: –55°C to +125°C
2: 10V/9V	N: Plastic DIL-18	2: –40°C to +85°C
	DW: SOIC-18	3: 0°C to +70°C

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

High Efficiency, Synchronous, Step-down (Buck) Controllers

FEATURES:

- Operation to 36V Input Voltage
- Fixed Frequency Average Current Mode Control
- Standby Mode for Improved Efficiency at Light Load
- Drives External N-Channel MOSFETs for Highest Efficiency
- Sleep Mode Current < 50µA
- Complementary 1 Amp Outputs with Regulated Gate Drive Voltage
- LDO (Low Drop Out) Virtual 100% Duty Cycle Operation
- Non-Overlapping Gate Drives

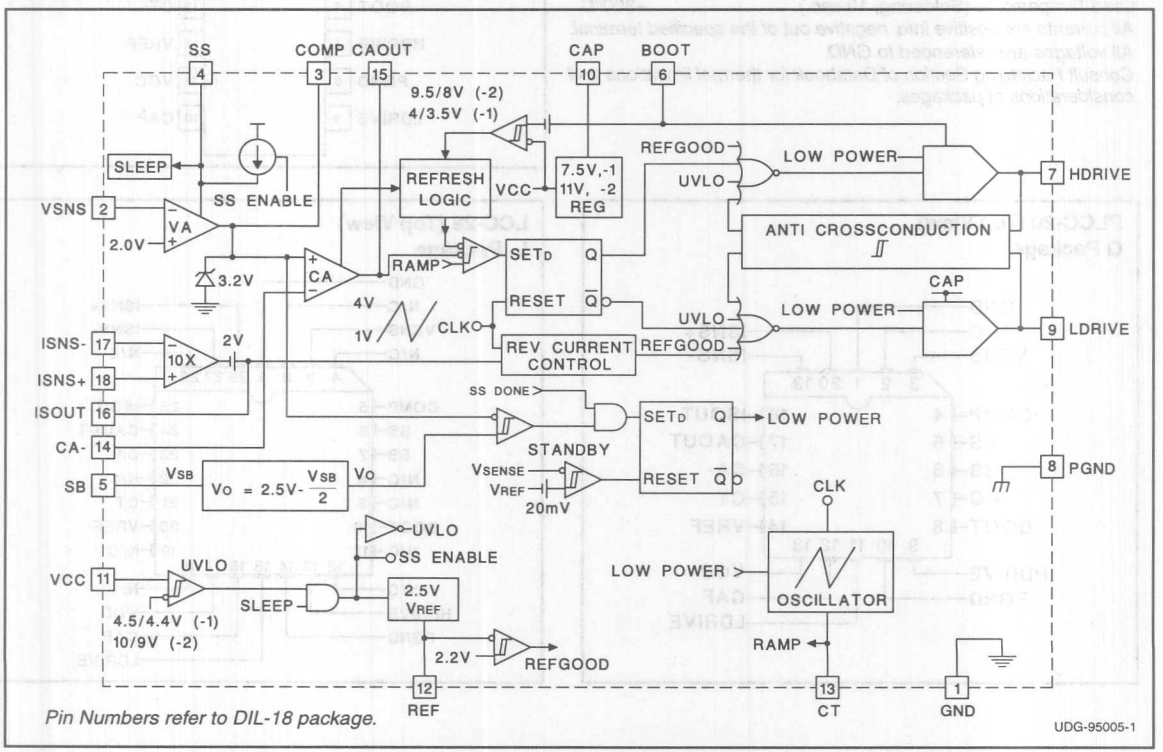
DESCRIPTION:

The UC3874 family of synchronous step-down (Buck) regulators provides high efficiency power conversion from an input voltage range of 4.5 to 36 volts. The UC3874 is tailored for battery powered applications such as laptop computers, consumer products, communications systems, and aerospace which demand high performance and long battery life. The synchronous regulator replaces the catch diode in the standard buck regulator with a low $R_{DS(on)}$ N-channel MOSFET switch allowing for significant efficiency improvements. The high side N-channel MOSFET switch is driven out of phase from the low side N-channel MOSFET switch by an on-chip bootstrap circuit which requires only a single external capacitor to develop the regulated gate drive. Fixed frequency, average current mode control provides the regulator with inherent slope compensation, tight regulation of the output voltage, and superior load and line transient response. Switching frequencies up to 300kHz are possible.

Light load efficiency is improved by a fully programmable standby mode, in which the quiescent current consumption of the controller is significantly reduced. The reduction is achieved by disabling the MOSFET driver outputs and the internal oscillator when the controller has sensed that the the output load current has dropped a user programmable amount from full load. During standby operation, the output capacitor supplies all of the load current

Continued

BLOCK DIAGRAM



DESCRIPTION (cont.)

requirements. Normal operation returns when the output voltage has drooped by 1%. Reverse current in the inductor is prevented by on-chip circuitry providing additional efficiency improvements. Virtual 100% duty cycle operation is easily attained by the controller even though a bootstrapped high side drive technique is employed.

A low power sleep mode can be invoked through the SS pin. Quiescent supply current in sleep mode is typically less than 50µA. Two UVLO options are available. The UC3874-1 is designed for logic level MOSFETs and has UVLO turn-on and turn-off thresholds of 4.5V and 4.4V respectively. The UC3874-2 is designed for standard power MOSFETs and has UVLO turn-on and turn-off thresholds of 10V and 9V respectively. A precision 2.5V reference can supply 20mA to external circuitry. An error amplifier with soft start, high bandwidth current amplifier, and a synchronizable oscillator are additional features.

Available packages include 18-pin plastic and ceramic DIP (N, J), 18-pin SOIC (DW), and 20-pin plastic and ceramic leadless chip carriers (Q, L).

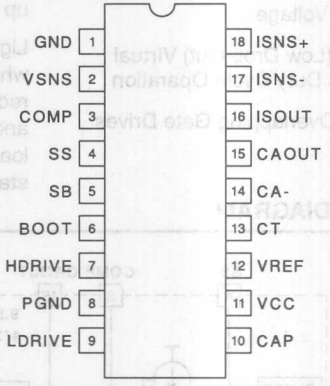
ABSOLUTE MAXIMUM RATINGS:

Supply Voltage (VCC) 36V
Boost Voltage (BOOT) 50V
OUTPUT Drivers (HDRIVE, LDRIVE) Currents
(continuous) . . . . . .±0.25A
(peak) . . . . . .±1A
VREF Current . . . . . .Internally Limited
Inputs (VSNS, SS, COMP, CT) . . . . . .–0.3 to 10V
Inputs (ISNS+, ISNS-) . . . . . .–0.3 to20V
Outputs (CAOUT) . . . . . .–0.3 to10V
Soft Start Sinking Current 1.5mA
Storage Temperature . . . . . .–65°C to +150°C
Junction Temperature . . . . . .–65°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . .+300°C

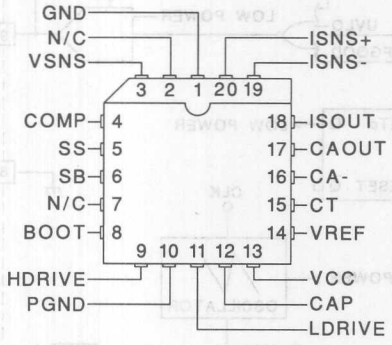
All currents are positive into, negative out of the specified terminal.
All voltages are referenced to GND.
Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAMS

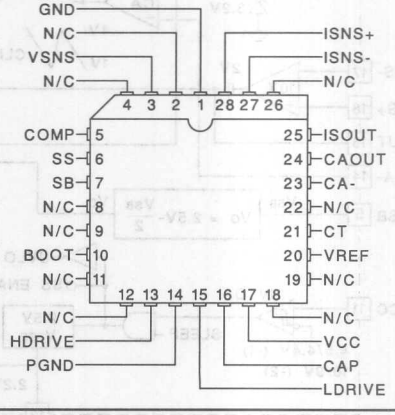
DIL-18, (Top View)
J or N, DW Packages



PLCC-20 (Top View)
Q Package



LCC-28 (Top View)
L Package



ELECTRICAL CHARACTERISTICS (cont) Unless otherwise stated these specifications apply for T_A = –55°C to +125°C for UC1874; –40°C to +85°C for UC2874; 0°C to +70°C for UC3874; VCC = 12V, CT = 680pF, C_{CAP} = 1µF; C_{BOOT} = 0.1µF, V_{COMP} = 2.5V, V_{CAOUT} = 2.5V, T_A = T_J.

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
Overall Section					
Supply Current, Sleep	SOFTSTART = 0V		50		µA
Supply Current, Operating			8.5		mA
Supply Current, Standby			2.5		mA
VCC Turn-on Threshold	UC3874-2		10	10.5	V
	UC3874-1		4.5	4.8	V
VCC Turn-off Threshold	UC3874-2	8.5	9		V
	UC3874-1	4.1	4.4		V
Voltage Amplifier Section					
Input Voltage	T_A = 25°C	1.97	2	2.03	V
VSNS Bias Current		–500	25	500	nA
Transconductance	I_{COMP} = +20µA to –20µA		675		µMho
V_{OUT} High	R_{COMP} = 200k to GND		3.2		V
V_{OUT} Low	R_{COMP} = 200k to VREF		0.15		V
Output Source Current	V_{OUT} = 1V		35		µA
Current Amplifier Section					
Input Offset Voltage	V_{COMP} = 2.5V	–10	0	10	mV
Input Bias Current(sense)	Vcm = 2.5V	–500		500	nA
Open Loop Gain	Vcm = 2.5V, V_{OUT} = 1V to 3.5V	80	110		dB
V_{OUT} High	R_{CAOUT} = 100k to GND		3.7		V
V_{OUT} Low	R_{CAOUT} = 100k to VREF		0.7		V
Output Source Current	V_{OUT} = 0V	80	100	120	µA
Common Mode Range		–0.3		3	V
Gain Bandwidth Product	F_{IN} = 100khz, 10mV p-p	2	3.5		MHz
Reference Section					
Output Voltage	I_{REF} = 0mA, T_A = 25°C	2.45	2.5	2.55	V
	I_{REF} = 0mA	2.425	2.5	2.575	V
Load Regulation	I_{REF} = 0 to 5mA	0	2	15	mV
Line Regulation	VCC = 12V to 24V	0	2	15	mV
Short Circuit Current	VREF = 0V	10	20	25	mA
Oscillator Section					
Initial Accuracy	T_A = 25°C	85	100	115	kHz
Voltage Stability	VCC = 12V to 18V		1		%
Total Variation	Line, Temperature	80		120	kHz
Ramp Amplitude (p-p)			2.7		V
Ramp Valley Voltage			0.95		V
Sleep/Soft Start/Bootstrap Section					
Sleep Threshold	Measured on SS	0.3	0.6	0.9	V
SS Charge Current	Vss = 2.5V	4	10	16	µA
SS Discharge Current	Vss = 2.5Vk		1		mA
Bootstrap Regulation Voltage	UC3874-2, Low Driver ON	9.5	11	12.5	V
	UC3874-1, Low Driver ON	6	7.5	9	V
Bootstrap Refresh Voltage	UC3874-2, V_{CAOUT} > V_{CTpeak}		8		V
	UC3874-1, V_{CAOUT} > V_{CTpeak}		3.5		V

ELECTRICAL CHARACTERISTICS (cont) Unless otherwise stated these specifications apply for T_A = –55°C to +125°C for UC1874; –40°C to +85°C for UC2874; 0°C to +70°C for UC3874; VCC = 12V, CT = 680pF, C_{CAP} = 1µF; C_{BOOT} = 0.1µF, V_{COMP} = 2.5V, V_{CAOUT} = 2.5V, T_A = T_J.

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
High Side Driver Output Section					
Output High Voltage	I_{OUT} = –50mA, BOOT = 23V	21	22.2		V
Output Low Voltage	I_{OUT} = 50mA		1	2.2	V
	I_{OUT} = 10mA		300	500	mV
Output Low (UVLO)	I_{OUT} = 50mA, VCC = 0V		0.9	1.5	V
Output Rise Time	C_{OUT} = 1nf		100		ns
Output Fall Time	C_{OUT} = 1nf		100		ns
Low Side Driver Output Section					
Output High Voltage	I_{OUT} = –50mA, V_{CAP} = 11V	9.5	10.2		V
Output Low Voltage	I_{OUT} = 50mA		1	2.2	V
	I_{OUT} = 10mA		300	500	mV
Output Low (UVLO)	I_{OUT} = 50mA, VCC = 0V		0.9	1.5	V
Output RISE/FALL Time	C_{LOAD} = 1nF		100		ns
Output FALL Time	C_{OUT} = 1nF		100		ns
X10 Amplifier Section					
Gain	V_{ISNS+} - V_{ISNS-} = 20mV to 80mV		10		V/V
Output Offset voltage	V_{ISNS+} = V_{ISNS-}	1.9	2	2.1	V
PSRR	VCC = 12V to 24V		tbd		
Slew Rate Rising			tbd		V/µs
Slew Rate Falling			tbd		V/µs
Input Resistance		75	100	150	kΩ

PIN DESCRIPTIONS

BOOT: This pin provides the high side rail for the HDRIVE output. An external capacitor (C_{BST}) is connected between this pin and the drain of the external low side MOSFET. When the low side MOSFET is conducting C_{BST} is charged to 11V via an external diode tied to CAP. When the low side MOSFET turns off and the high side MOSFET turns on, the C_{BST} bootstraps itself up with the source of high side MOSFET, ultimately providing a 10V V_{GS} for the upper MOSFET. Since this 10V is referenced to the source of the high side N-channel MOSFET, the actual voltage on BOOT and HDRIVE is approximately 10V above VCC while the high side MOSFET is conducting. The voltage on BOOT is continuously monitored during low input voltage conditions when the duty cycle equals approximately 100% to insure that a sufficient gate drive level is being supplied by the UC3874. If the voltage on BOOT falls below 8V (UC3874-2) or 3.5V (UC3874-1), the IC forces the low side driver to cycle itself on for the few cycles required to replenish C_{BST}. In this way, virtual 100% duty cycle operation is provided.

CA-: This is the inverting input to the current amplifier. Connect a series resistor and capacitor between this pin and CAOUT to set the current loop compensation. An input resistor between this pin and ISOUT provides the inductor current sense signal to the amplifier and also sets the high frequency gain of the amplifier. The common mode operating range for this input is between GND and 4V. The normal range during operation is between 2V and 3V.

CAOUT: This is the output of the wide bandwidth current amplifier and one of the inputs to the PWM duty cycle comparator. The output signal generated by this amplifier commands the PWM to force the correct duty cycle to maintain output voltage in regulation. The output can swing from 0.1V to 4V.

CAP: A capacitor is normally connected between this pin and GND providing bypass for the internal 11V regulator. Charge is transferred from this capacitor to CBST via an external diode when the low side MOSFET is conducting. If VCC ≤ 10V logic level MOSFETs are generally specified. CAP should then be shorted to VCC in conjunction with a low VF Schottky to BOOT to maximize the gate drive amplitude. This technique provides adequate gate drive signal amplitudes with VCC as low as 4.5V. For high input voltage applications, a simple external shunt zener regulator circuit can be connected to CAP, thereby offloading power dissipation requirements from the IC to an external transistor.

COMP: This is the output of the voltage amplifier. It provides the current command signal to the current amplifier. The voltage is clamped to approximately 3.2V.

CT: A capacitor from CT to GND sets the PWM oscillator frequency according to the following equation:

$$F = \frac{1}{14250 \bullet CT}.$$

Use a high quality ceramic capacitor with low ESL and ESR for best results. A minimum CT value of 220pF insures good accuracy and less susceptibility to circuit layout parasitics. The oscillator and PWM are designed to provide practical operation to 300kHZ.

GND: All voltages are measured with respect to this pin. All bypass capacitors and timing components except those listed under the PGND pin description should be connected to this pin. Component leads should be as short and direct as possible.

HDRIVE, LDRIVE: The outputs of the PWM are totem pole MOSFET gate drivers on the HDRIVE and LDRIVE pins. The outputs can sink approximately 1A and source 500mA. This characteristic optimizes the switching transitions by providing a controlled dV/dT at turn-on and a lower impedance at turn-off. These are complementary outputs with a typical deadtime of 200ns. Internal circuitry prevents the possibility of simultaneous conduction of the output MOSFETs (shoot through). HDRIVE is the high side bootstrapped output. Its upper power supply rail is the BOOT pin which means that its output will fly approximately 10V above VCC when the upper side of the totem pole output is conducting. The power supply rail for LDRIVE is CAP. As a result the VGS of both gates are regulated to approximately 10V if VCC is >11V. A series resistor between these pins and the MOSFET gates of at least 10 ohms can be used to control ringing. Additionally, a low VF Schottky diode should be connected between these pins and GND to prevent substrate conduction and possible erratic operation.

ISNS-: This is the inverting input to the X10 instrumentation amplifier. The common mode input range for this pin extends from GND to VCC. A low value resistor in series with the output inductor is connected between this pin and ISNS+ to develop the current sense signal.

ISNS+: This is the non-inverting input to the X10 instrumentation amplifier. The common mode input range for this pin extends from GND to VCC.

ISOUT: This is the output of the X10 instrumentation amplifier. The output voltage on this pin is level shifted 2V above GND, such that if a 100mV differential input is applied across ISNS+ and ISNS-, the output will be 3V.

PGND: This is the high current ground for the IC. The MOSFET driver transistors are referenced to this ground. For best performance an external star ground connection should be made between this pin, the source of the low side MOSFET, the capacitor on CAP, the anodes of any external Schottky clamp diodes and the output filter capacitor. As with all high frequency layouts, a ground plane and short leads are highly recommended.

SB: The voltage on SB sets the output current level at which standby mode is initiated. A voltage level from 0V to 1V programs the threshold from 50% to 0% of full load current. Full load current corresponds to a 100mV differential signal across the ISNS inputs. Since this is a high impedance input, a voltage divider derived from VREF may be used to program this level. Another possible use is to actively control this level with external circuitry to adaptively control converter efficiency. Tying SB to VREF disables standby mode operation.

SS: A capacitor from this pin to GND in conjunction with an internal 10µA current source provides a soft start function for the IC. The voltage level on SS clamps the output of the voltage amplifier through an internal buffer, thus providing a controlled startup. The SS time is approximately:

$$\frac{Css \bullet \left(\frac{VO}{VIN}\right) \bullet 3V}{10\mu A}.$$

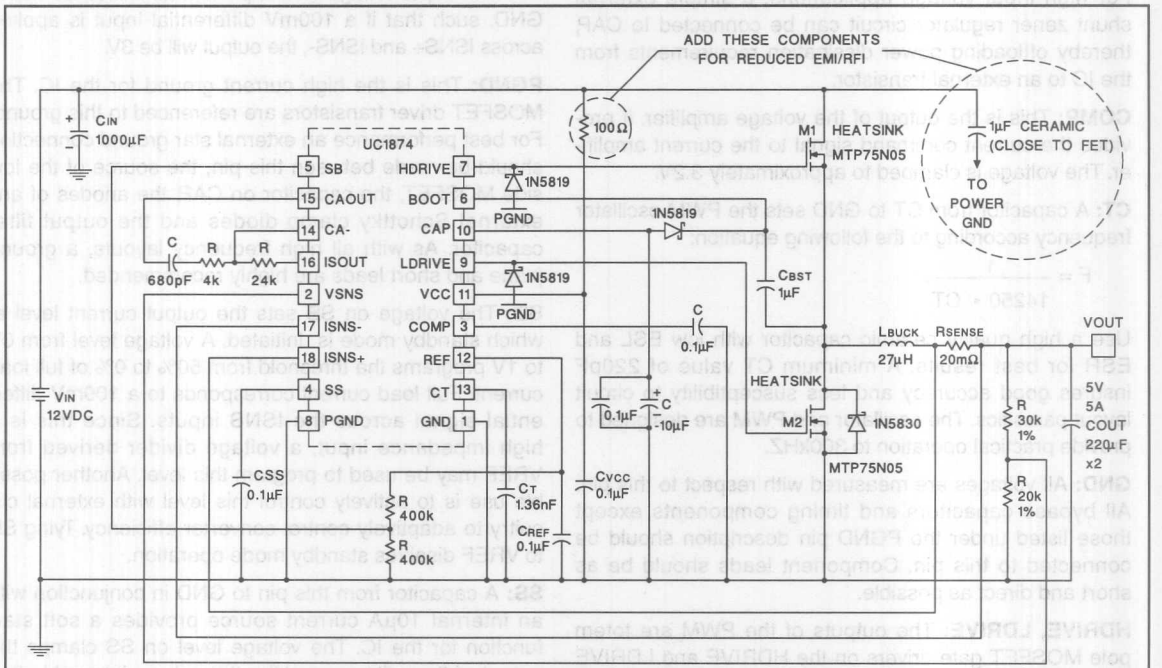
Once the device has completed its soft start cycle, a low power sleep mode can be invoked by pulling SS below 0.5V typically. In sleep mode, all of the device functions are disabled except for those which are required to bring the device out of sleep mode when SS is released. Typical sleep mode supply current is less than 50µA.

VCC: Positive supply rail for the IC. Bypass this pin to GND with a 1µF low ESL/ESR ceramic capacitor. The maximum voltage for VCC is 36V. The turn on voltage level on VCC is 4.5V with 100mV of hysteresis for the UC3874-1 and 10V with 1V of hysteresis for the UC3874-2.

VREF: VREF is the output of the precision reference. The output is capable of supplying 20mA to peripheral circuitry and is internally short circuit current limited. VREF is disabled and low whenever VCC is below the UVLO threshold, and when SS is pulled below 0.5V. A VREF "GOOD" comparator senses VREF and disables the PWM stage until VREF has attained approximately 90% of its nominal value. Bypass VREF to GND with a 0.1µF ceramic capacitor for best performance.

VSNS: This pin is the inverting input of the voltage amplifier and serves as the output voltage feedback point for the synchronous regulator. It senses the output voltage through a voltage divider which produces a nominal 2.0V.

APPLICATION DIAGRAM:



Note: 1. CIN, COUT, M2 Source, PGND, and CCAP form a star ground connection.
2. Pin Numbers refer to DIL-18 package.
3. Connect PGND and GND together close to the I.C.

OPERATION: Refer to 5V, 25W Application Schematic

The UC3874 employs a fixed frequency average current mode control Buck topology to convert a higher battery voltage down to a tightly regulated output voltage. Special design techniques allow this bipolar IC to deliver exceptional performance while consuming approximately 6mA of supply current over an input voltage range of 4.5 to 35 volts. Fixed frequency operation allows synchronization to an existing system clock, and easier filtering. Average current mode control provides inherent slope compensation and accurate short circuit current limiting. An additional benefit is its ability to maintain a constant regulator gain regardless of whether the inductor current is continuous or discontinuous.

The output inductor current is sensed by an external low value shunt resistor (RSENSE). This signal at full load current should be no larger than 100mV in order to minimize sensing losses. The differential voltage across RSENSE is amplified by the internal X10 instrumentation amplifier. The common mode input range for this amplifier extends from GND to VCC in order to maintain accurate current sensing under normal conditions as well as abnormal conditions such as output short circuit and low drop out

OPERATION (cont): Refer to 5V, 25W Application Schematic

(LDO) modes. The output of the X10 instrumentation amplifier is applied to the inverting input of the current amplifier through an external resistor. The converter's output voltage feedback is applied to the VSNS pin through an external voltage divider. The difference between the voltage at VSNS and the internal reference level at the non-inverting input is amplified by the voltage amplifier and applied to the non-inverting input of the current amplifier. This instantaneous reference level forms the current command input for the average current control loop. The average current amplifier develops the duty cycle command signal by integrating the current feedback signal with respect to the instantaneous current command input. This output is compared to the fixed high amplitude oscillator ramp waveform at the inputs of the PWM comparator to develop duty cycle information for the PWM drive. The large amplitude oscillator ramp provides both high noise margin and built-in slope compensation in average current mode control methodology. The fixed frequency oscillator is programmed with a single external capacitor connected between CT and GND, and is capable of switching frequencies up to 300kHz. The UC3874 can be synchronized to an external clock by capacitively coupling the signal to the junction of the capacitor at CT and a low value resistor tied to GND. Refer to Application Note U-111.

The PWM drive signal is applied to the complementary output driver stages. Since the high side switch is an N-channel MOSFET, a means for driving its gate above VCC is required. This is accomplished via the internal 11V regulator and an external capacitor (C_{BST}). C_{BST} is charged through an external diode to VCC or CAP when the low side MOSFET is on. The charging level on C_{BST} is internally regulated to 11V minus an external diode drop by the UC3874 as long as VCC is above 11V. When the low side MOSFET turns off, C_{BST} is applied across the gate to the source of the upper MOSFET allowing it to begin turn-on. As the upper MOSFET turns on, it lifts or bootstraps the low end of C_{BST}, along with its source. Shortly thereafter, the source voltage level is reduced by $R_{DS(on)} \cdot I_{LOAD}$ below VCC. When VCC < 10V, V_{GS} for the high side MOSFET is approximately equal to VCC. If VCC < 8V, logic level MOSFETs are recommended. In these applications, CAP should be shorted to VCC and an external Schottky diode is connected between CAP/VCC and BOOT. For low battery applications, a synchronous regulator must be capable of LDO or 100% duty cycle operation. The UC3874 includes circuitry to insure that this mode of operation is possible even though it uses a bootstrapped drive technique for the high side MOSFET. During commanded 100% duty cycle operation, the UC3874 monitors the V_{GS} drive signal applied to the high side MOSFET, and automatically provides complementary pulses to refresh the bootstrap capacitor when this voltage falls below a set threshold. In this way, near 100% duty cycle operation is possible, with effective duty cycle dependent only upon the value of C_{BST}.

High efficiency is obtained primarily by the low side MOSFET which replaces the Schottky diode in the standard Buck configuration. Its low $R_{DS(on)}$ produces a much lower voltage drop than a low VF Schottky diode. As output voltages get lower, these improvements become more evident. Additional efficiency improvements at light regulator load currents are obtained by automatic switchover to standby mode. In standby mode, the UC3874 disables its MOSFET drivers and oscillator saving both quiescent supply current consumption and more importantly MOSFET gate drive charge current. Standby mode is initiated when the output inductor current has dropped to a user programmable fraction of the designed full load current. Programmability is easily attained by setting the SB pin to a voltage level between 0V and 1V, which corresponds to 50% to 0% of the peak load current. In this manner, the user can accurately determine when standby mode is initiated, giving the flexibility to directly shape the efficiency vs. load curve. In standby mode, all output current requirements are handled by the output capacitor. Since the output capacitor isn't being refreshed by the PWM converter, the output voltage will decay at a rate determined by the load current and the output capacitor value:

$$\frac{dV}{dT} = \frac{I_{LOAD}}{C_{OUT}}.$$

Normal operation returns when the output voltage has decayed by approximately 1% from its nominal value. Standby operation can be easily disabled by connecting the SB pin directly to VREF. Another efficiency consideration is the the possibility of reverse current in the output inductor. For a non-synchronous regulator this isn't a problem since the diode will block reverse current, allowing discontinuous inductor current operation at light loads. Since the synchronous regulator replaces the diode with a switch, reverse current can and will flow if the low side switch is on when the inductor is depleted. The UC3874 includes circuitry to prevent reverse current from flowing in the inductor by disabling the low side gate drive signal during discontinuous mode operation. This increases efficiency by eliminating unnecessary I^2R losses in the MOSFET and the inductor.

Soft start is recommended for Buck converters to reduce stress on the power components during startup, and to

OPERATION (cont.): Refer to 5V, 25W Application Schematic

reduce overshoot of the output voltage. This improves reliability. The UC3874 includes a user programmable soft start pin to implement this feature. An internal 10µA current source charges the external soft start capacitor which provides a clamp at the output of the voltage amplifier. An ultra low power sleep mode is also invoked from the SS pin. A voltage level below 0.5V on this pin reduces total standby current to less than 50µA. Short circuit protection is inherent to the average current mode technique with proper compensation of the current amplifier. To prevent operation of the MOSFETs with an inadequete drive signal, an undervoltage lockout circuit suppresses the output drivers until the input supply voltage is sufficiently high enough for proper operation. The UC3874-1 is intended for applications with logic level MOSFETs and its VCC turn-on and turn-off thresholds are 4.5V/4.4V respectively. The UC3874-2 is intended for applications with standard MOSFETs and has UVLO turn-on and turn-off thresholds of 10V and 9V respectively. The precision 2.5V reference can provide 20mA to power external circuitry. The reference output is disabled during UVLO and sleep modes.

ORDERING INFORMATION

UC [ ] 874 [ ] — [ ]

- UVLO Threshold
- Package
- Temperature Range

UVLO Turn On/Off Threshold	Package	Temperature Range
1: 4.5V/4.4V	J: Ceramic DIL-18	1: –55°C to +125°C
2: 10V/9V	N: Plastic DIL-18	2: –40°C to +85°C
	DW: SOIC-18	3: 0°C to +70°C

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

UNITRODE

UC1875/6/7/8
UC2875/6/7/8
UC3875/6/7/8

Phase Shift Resonant Controller

FEATURES

- Zero to 100% Duty Cycle Control
- Programmable Output Turn-On Delay
- Compatible with Voltage or Current Mode Topologies
- Practical Operation at Switching Frequencies to 1MHz
- Four 2A Totem Pole Outputs
- 10MHz Error Amplifier
- Undervoltage Lockout
- Low Startup Current —150µA
- Outputs Active Low During UVLO
- Soft-Start Control
- Latched Over-Current Comparator With Full Cycle Restart
- Trimmed Reference

DESCRIPTION

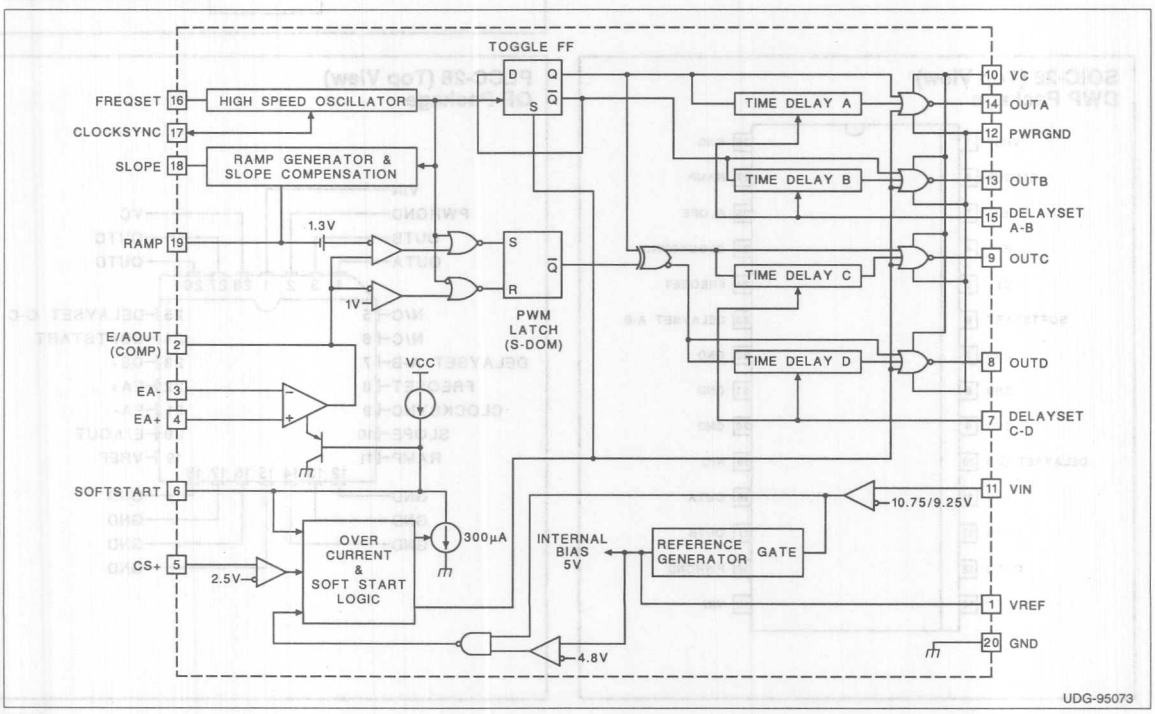
The UC1875 family of integrated circuits implements control of a bridge power stage by phase-shifting the switching of one half-bridge with respect to the other, allowing constant frequency pulse-width modulation in combination with resonant, zero-voltage switching for high efficiency performance at high frequencies. This family of circuits may be configured to provide control in either voltage or current mode operation, with a separate over-current shutdown for fast fault protection.

A programmable time delay is provided to insert a dead-time at the turn-on of each output stage. This delay, providing time to allow the resonant switching action, is independently controllable for each output pair (A-B, C-D).

With the oscillator capable of operation at frequencies in excess of 2MHz, overall switching frequencies to 1MHz are practical. In addition to the standard free running mode, with the CLOCKSYNC pin, the user may configure these devices to accept an external clock synchronization signal, or may lock together up to 5 units with the operational frequency determined by the fastest device.

Protective features include an undervoltage lockout which maintains all outputs in an active-low state until the supply reaches a 10.75V threshold. 1.5V hysteresis is built in for reliable, boot-strapped chip supply. Over-current protection is provided, and will latch the outputs in the OFF state within 70nsec of a fault. The current-fault circuitry implements full-cycle restart operation.

BLOCK DIAGRAM



4/97

DESCRIPTION (cont.)

Additional features include an error amplifier with bandwidth in excess of 7MHz, a 5V reference, provisions for soft-starting, and flexible ramp generation and slope compensation circuitry.

These devices are available in 20-pin DIP, 28-pin "bat-wing" SOIC and 28 lead power PLCC plastic packages for operation over both 0°C to 70°C and –25°C to +85°C temperature ranges; and in hermetically sealed cerdip, and surface mount packages for –55°C to +125°C operation.

Device	UVLO Turn-On	UVLO Turn-Off	Delay Set
UC1875	10.75	9.25V	Yes
UC1876	15.25V	9.25V	Yes
UC1877	10.75V	9.25V	No
UC1878	15.25V	9.25V	No

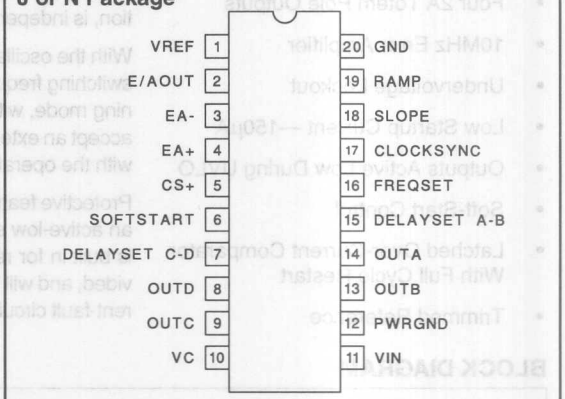
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (VC, VIN) 20V
Output Current, Source or Sink
DC 0.5A
Pulse (0.5µs) 3A
Analog I/0s
(Pins 1, 2, 3, 4, 5, 6, 7, 15, 16, 17, 18, 19) .....–0.3 to 5.3V
Storage Temperature Range .....–65°C to +150°C
Junction Temperature .....–55°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

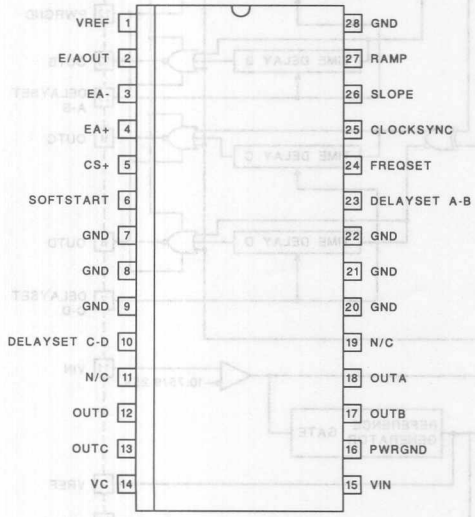
Note: Pin references are to 20 pin packages. All voltages are with respect to ground. Currents are positive into, negative out of, device terminals. Consult Unitrode Integrated Circuits databook for information regarding thermal specifications and limitations of packages.

CONNECTION DIAGRAMS

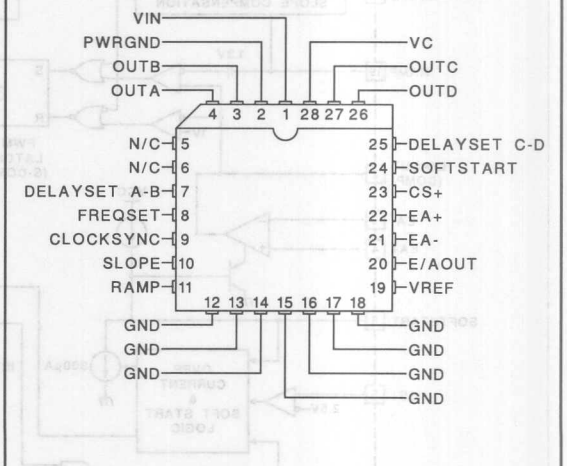
DIL-20 (Top View)
J or N Package



SOIC-28 (Top View)
DWP Package



PLCC-28 (Top View)
QP Package



ELECTRICAL CHARACTERISTICS Unless otherwise stated, –55°C < T_A < 125°C for the UC1875/6/7/8, –25°C < T_A < 85°C for the UC2875/6/7/8 and 0°C < T_A < 70°C for the UC3875/6/7/8, VC = VIN = 12V, $R_{FREQSET}$ = 12kΩ, $C_{FREQSET}$ = 330pF, R_{SLOPE} = 12kΩ, C_{RAMP} = 200pF, $C_{DELAYSET\ A\text{-}B}$ = $C_{DELAYSET\ C\text{-}D}$ = 0.01µF, $I_{DELAYSET\ A\text{-}B}$ = $I_{DELAYSET\ C\text{-}D}$ = –500µA, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Undervoltage Lockout					
Start Threshold	UC1875/UC1877		10.75	11.75	V
	UC1876/UC1878		15.25		V
UVLO Hysteresis	UC1875/UC1877	0.5	1.25	2.0	V
	UC1876/UC1878		6.0		V
Supply Current					
I_{IN} Startup	VIN = 8V, VC = 20V, R_{SLOPE} open, I_{DELAY} = 0		150	600	µA
Ic Startup	VIN = 8V, VC = 20V, R_{SLOPE} open, I_{DELAY} = 0		10	100	µA
I_{IN}			30	40	mA
Ic			15	30	mA
Voltage Reference					
Output Voltage	T_J = +25°C	4.92	5	5.08	V
Line Regulation	11 < VIN < 20V		1	10	mV
Load Regulation	I_{VREF} = –10mA		5	20	mV
Total Variation	Line, Load, Temperature	4.9		5.1	V
Noise Voltage	10Hz to 10kHz		50		µVrms
Long Term Stability	T_J = 125°C, 1000 hours		2.5		mV
Short Circuit Current	VREF = 0V, T_J = 25°C		60		mA
Error Amplifier					
Offset Voltage			5	15	mV
Input Bias Current			0.6	3	µA
AVOL	1V < $V_{E/AOUT}$ < 4V		60	90	dB
CMRR	1.5V < V_{CM} < 5.5V	75	95		dB
PSRR	11V < VIN < 20V	85	100		dB
Output Sink Current	$V_{E/AOUT}$ = 1V	1	2.5		mA
Output Source Current	$V_{E/AOUT}$ = 4V		–1.3	–0.5	mA
Output Voltage High	$I_{E/AOUT}$ = –0.5mA	4	4.7	5	V
Output Voltage Low	$I_{E/AOUT}$ = 1mA	0	0.5	1	V
Unity Gain BW		7	11		MHz
Slew Rate		6	11		V/µsec
PWM Comparator					
Ramp Offset Voltage	T_J = 25°C (Note 3)		1.3		V
Zero Phase Shift Voltage	(Note 4)	0.55	0.9		V
PWM Phase Shift	$V_{E/AOUT}$ > (Ramp Peak + Ramp Offset)	98	99.5	102	%
(Note1)	$V_{E/AOUT}$ < Zero Phase Shift Voltage	0	0.5	2	%
Output Skew (Note 1)	$V_{E/AOUT}$ < 1V		5	±20	nsec
Ramp to Output Delay	UC3875/6/7/8 (Note 6)		65	100	nsec
	UC1875/6/7/8, UC2875/6/7/8 (Note 6)		65	125	nsec
Oscillator					
Initial Accuracy	T_J = 25°C	0.85	1	1.15	MHz
Voltage Stability	11V < VIN < 20V		0.2	2	%
Total Variation	Line, Temperature	0.80		1.20	MHz
Sync Pin Threshold	T_J = 25°C		3.8		V
Clock Out Peak	T_J = 25°C		4.3		V
Clock Out Low	T_J = 25°C		3.3		V
Clock Out Pulse Width	$R_{CLOCKSYNC}$ = 3.9kΩ		30	100	nsec
Maximum Frequency	$R_{FREQSET}$ = 5kΩ	2			MHz

ELECTRICAL CHARACTERISTICS (cont.) Unless otherwise stated, –55°C < T_A < 125°C for the UC1875/6/7/8, –25°C < T_A < 85°C for the UC2875/6/7/8 and 0°C < T_A < 70°C for the UC3875/6/7/8, VC = VIN = 12V, $R_{FREQSET}$ = 12kΩ, $C_{FREQSET}$ = 330pF,

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Ramp Generator/Slope Compensation					
Ramp Current, Minimum	I_{SLOPE} = 10µA, $V_{FREQSET}$ = VREF		–11	–14	µA
Ramp Current, Maximum	I_{SLOPE} = 1mA, $V_{FREQSET}$ = VREF	–0.8	–0.95		mA
Ramp Valley			0		V
Ramp Peak - Clamping Level	$R_{FREQSET}$ = 100kΩ		3.8	4.1	V
Current Limit					
Input Bias	V_{CS+} = 3V		2	5	µA
Threshold Voltage		2.4	2.5	2.6	V
Delay to Output	UC3875/6/7/8		85	125	nsec
	UC1875/6/7/8, UC2875/6/7/8		85	150	nsec
Soft-Start/Reset Delay					
Charge Current	$V_{SOFTSTART}$ = 0.5V	–20	–9	–3	µA
Discharge Current	$V_{SOFTSTART}$ = 1V	120	230		µA
Restart Threshold		4.3	4.7		V
Discharge Level			300		mV
Output Drivers					
Output Low Level	I_{OUT} = 50mA		0.2	0.4	V
	I_{OUT} = 500mA		1.2	2.6	V
Output High Level	I_{OUT} = –50mA		1.5	2.5	V
	I_{OUT} = –500mA		1.7	2.6	V
Delay Set (UC1875 and UC1876 only)					
Delay Set Voltage	I_{DELAY} = –500µA	2.3	2.4	2.6	V
Delay Time	I_{DELAY} = –250µA (Note 5) (UC3875/6/7/8, UC2875/6/7/8)	150	250	400	nsec
	I_{DELAY} = –250µA (Note 5) (UC1875/6/7/8)	150	250	600	nsec

Note 1: Phase shift percentage (0% = 0°, 100% = 180°) is defined as $\theta = \frac{200}{T}\Phi\%$, *where θ is the phase shift, and Φ and T are defined in Figure1. At 0% phase shift, Φ is the output skew.*

Note 2: Delay time is defined as delay = T ($\frac{1}{2}$ *–(duty cycle)), where T is defined in Figure 1.*

Note 3: Ramp offset voltage has a temperature coeffecient of about –4mV/°C.

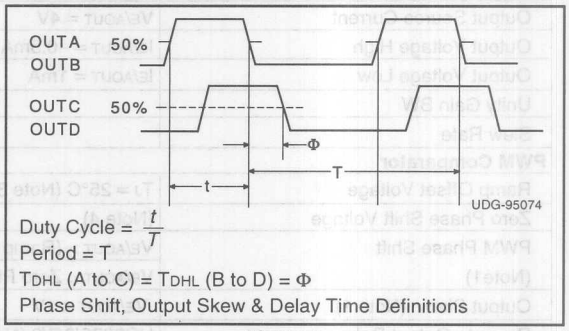
Note 4: Zero phase shift voltage has a temperature coeffecient of about –2mV/°C.

Note 5: Delay time can be programmed via resistors from the delay set pins to ground.

Delay time ≅ $62.5x10^{-12}$ *sec. Where*

$I_{DELAY} = \frac{\text{Delay set voltage}}{R_{DELAY}}$ *The recommended range for* I_{DELAY} *is 25µA ≤* I_{DELAY} *≤ 1mA*

Note 6: Ramp delay to output time is defined in Figure 2.



Duty Cycle = $\frac{t}{T}$
Period = T
T_{DHL} (A to C) = T_{DHL} (B to D) = Φ
Phase Shift, Output Skew & Delay Time Definitions

Figure 1

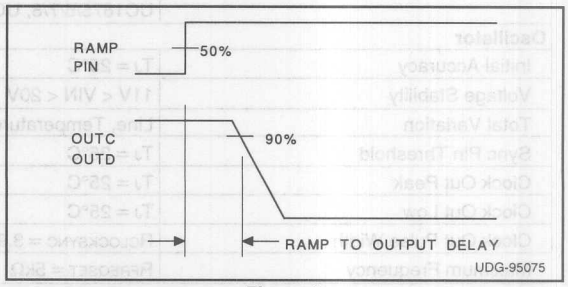


Figure 2

PIN FUNCTIONAL DESCRIPTIONS

CLOCKSYNC (bi-directional clock and synchronization pin): Used as an output, this pin provides a clock signal. As an input, this pin provides a synchronization point. In its simplest usage, multiple devices, each with their own local oscillator frequency, may be connected together by the CLOCKSYNC pin and will synchronize on the fastest oscillator. This pin may also be used to synchronize the device to an external clock, provided the external signal is of higher frequency than the local oscillator. A resistor load may be needed on this pin to minimize the clock pulse width.

E/AOUT (error amplifier output): This is is the gain stage for overall feedback control. Error amplifier output voltage levels below 1 volt will force 0° phase shift. Since the error amplifier has a relatively low current drive capability, the output may be overridden by driving with a sufficiently low impedance source.

CS+ (current sense): The non-inverting input to the current-fault comparator whose reference is set internally to a fixed 2.5V (separate from VREF). When the voltage at this pin exceeds 2.5V the current-fault latch is set, the outputs are forced OFF and a SOFT-START cycle is initiated. If a constant voltage above 2.5V is applied to this pin the outputs are disabled from switching and held in a low state until the CS+ pin is brought below 2.5V. The outputs may begin switching at 0 degrees phase shift before the SOFT-START pin begins to rise -- this condition will not prematurely deliver power to the load.

FREQSET (oscillator frequency set pin): A resistor and a capacitor from FREQSET to GND will set the oscillator frequency.

DELAYSET A-B, DELAYSET C-D (output delay control): The user programmed current flowing from these pins to GND set the turn-on delay for the corresponding output pair. This delay is introduced between turn-off of one switch and turn-on of another in the same leg of the bridge to provide a dead time in which the resonant switching of the external power switches takes place. Separate delays are provided for the two half-bridges to accommodate differences in the resonant capacitor charging currents.

EA- (error amplifier inverting input): This is normally connected to the voltage divider resistors which sense the power supply output voltage level.

EA+ (error amplifier non-inverting input): This is normally connected to a reference voltage used for comparison with the sensed power supply output voltage level at the EA+ pin.

GND (signal ground): All voltages are measured with respect to GND. The timing capacitor, on the FREQSET pin, any bypass capacitor on the VREF pin, bypass capacitors on VIN and the ramp capacitor, on the RAMP pin, should be connected directly to the ground plane near the signal ground pin.

OUTA-OUTD (outputs A-D): The outputs are 2A totem-pole drivers optimized for both MOSFET gates and level-shifting transformers. The outputs operate as pairs with a nominal 50% duty-cycle. The A-B pair is intended to drive one half-bridge in the external power stage and is syncronized with the clock waveform. The C-D pair will drive the other half-bridge with switching phase shifted with respect to the A-B outputs.

PWRGND (power ground): VC should be bypassed with a ceramic capacitor from the VC pin to the section of the ground plane that is connected to PWRGND. Any required bulk reservoir capacitor should parallel this one. Power ground and signal ground may be joined at a single point to optimize noise rejection and minimize DC drops.

RAMP (voltage ramp): This pin is the input to the PWM comparator. Connect a capacitor from here to GND. A voltage ramp is developed at this pin with a slope:

$$\frac{dV}{dT} = \frac{\text{Sense Voltage}}{R_{SLOPE} \bullet C_{RAMP}}$$

Current mode control may be achieved with a minimum amount of external circuitry, in which case this pin provides slope compensation.

Because of the 1.3V offset between the ramp input and the PWM comparator, the error amplifier output voltage can not exceed the effective ramp peak voltage and duty cycle clamping is easily achievable with appropriate values of R_{SLOPE} and C_{RAMP}.

SLOPE (set ramp slope/slope compensation): A resistor from this pin to VCC will set the current used to generate the ramp. Connecting this resistor to the DC input line voltage will provide voltage feed-forward.

SOFTSTART (soft start): SOFTSTART will remain at GND as long as VIN is below the UVLO threshold. SOFT-START will be pulled up to about 4.8V by an internal 9µA current source when VIN becomes valid (assuming a non-fault condition). In the event of a current-fault (CS+ voltage exceeding 2.5V), SOFTSTART will be pulled to GND and them ramp to 4.8V. If a fault occurs during the SOFT-START cycle, the outputs will be immediately disabled and SOFTSTART must charge fully prior to resetting the fault latch.

For paralleled controllers, the SOFTSTART pins may be paralled to a single capacitor, but the charge currents will be additive.

VC (output switch supply voltage): This pin supplies power to the output drivers and their associated bias circuitry. Connect VC to a stable source above 3V for normal operation, above 12V for best performance. This supply should be bypassed directly to the PWRGND pin with low ESR, low ESL capacitors.

PIN FUNCTIONAL DESCRIPTION (cont.)

VIN (primary chip supply voltage): This pin supplies power to the logic and analog circuitry on the integrated circuit that is not directly associated with driving the output stages. Connect VIN to a stable source above 12V for normal operation. To ensure proper chip functionality, these devices will be inactive until VIN exceeds the upper undervoltage lockout threshold. This pin should by bypassed directly to the GND pin with low ESR, low ESL capacitors.

NOTE: When VIN exceeds the UVLO threshold the supply current (I_{IN}) will jump from about 100µA to a current in excess of 20mA. If the UC1875 is not connected to a well bypassed supply, it may immediately enter UVLO again.

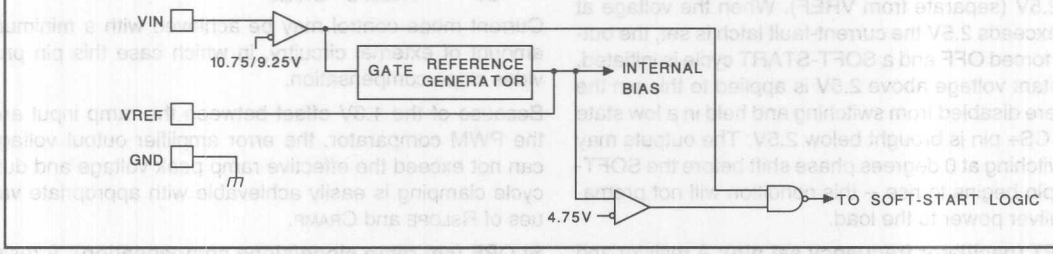
VREF: This pin is an accurate 5V voltage reference. This output is capable of delivering about 60mA to peripheral circuitry and is internally short circuit current limited. VREF is disabled while VIN is low enough to force the chip into UVLO. The circuit is also in UVLO until VREF reaches approximately 4.75V. For best results bypass VREF with a 0.1µF, low ESR, low ESL, capacitor to the GND pin.

APPLICATIONS INFORMATION

UNDERVOLTAGE LOCKOUT SECTION

When power is applied to the circuit and VIN is below the upper UVLO threshold, I_{IN} will be below 600µA, the reference generator will be off, the fault latch is reset, the soft-start pin is discharged, and the outputs are actively held low.

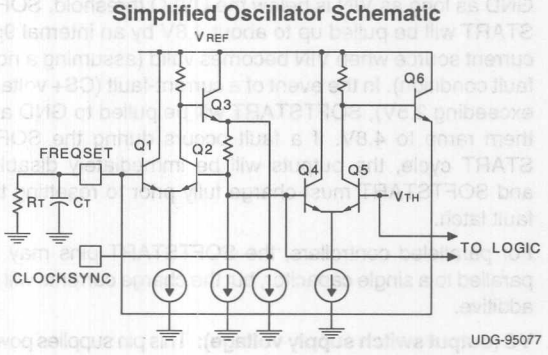
When VIN exceeds the upper UVLO threshold, the reference generator turns on. All else remains in the shutdown mode until the output of the reference, VREF, exceeds 4.75V.

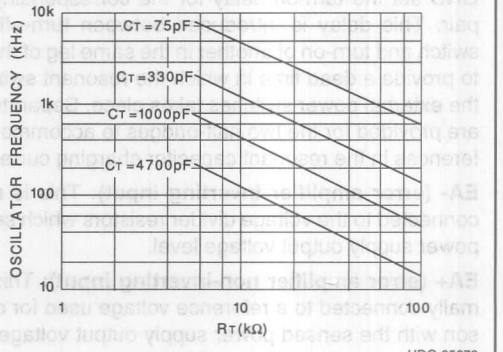


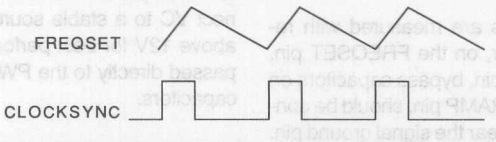
OSCILLATOR

The high frequency oscillator may be either free-running or externally synchronized. For free-running operation, the frequency is set via an external resistor and capacitor to ground from the FREQSET pin.

Simplified Oscillator Schematic





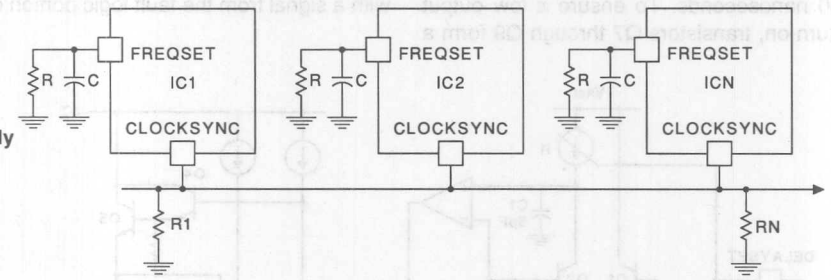


APPLICATIONS INFORMATION (cont.)

SYNCHRONIZING THE OSCILLATOR

The CLOCKSYNC pin of the oscillator may be used to synchronize multiple UC1875 devices simply by connecting the CLOCKSYNC of each UC1875 to the others:

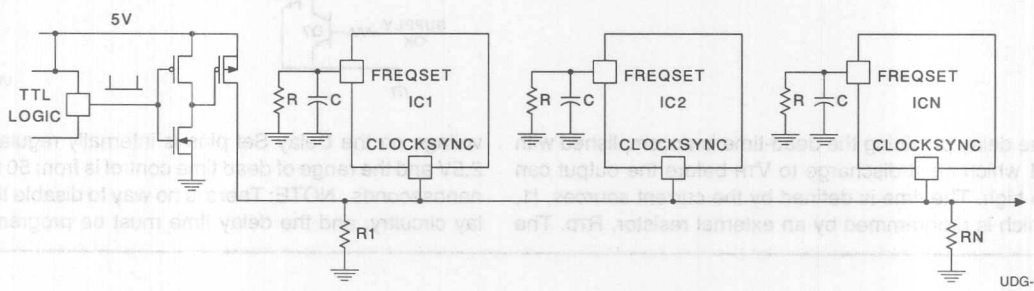
1875/6/7/8s only



UDG-95080

All ICs will sync to chip with the fastest local oscillator.
R1 & RN *may* be needed to keep sync pulse narrow due to capacitance on line.
R1 & RN *may* also be needed to properly terminate RSYNC line.

Syncing to external TTL/CMOS



UDG-95081

ICs will sync to fastest chip or TTL clock if it is higher frequency.
R & RN *may* be needed for same reasons as above

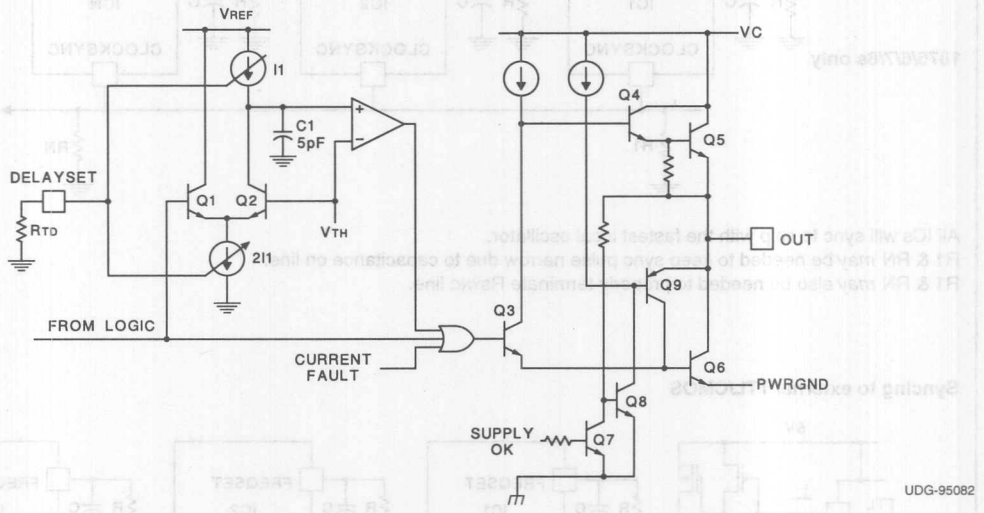
Although each UC1875/6/7/8 has a local oscillator frequency, the group of devices will synchronize to the fastest oscillator driving the CLOCKSYNC pin. This arrangement allows the synchronizing connection between ICs to be broken without any local loss of functionality.

Synchronizing the device to an external clock signal may be accomplished with a minimum of external circuitry, as shown in the previous figure.

Capacitive loading on the CLOCKSYNC pin will increase the clock pulse width, and may adversely effect system performance. Therefore, a resistor to ground from the CLOCKSYNC pin is optional, but may be required to offset capacitive loading on this pin. These resistors are shown in the oscillator schematics as R1, RN.

DELAY BLOCKS AND OUTPUT STAGES

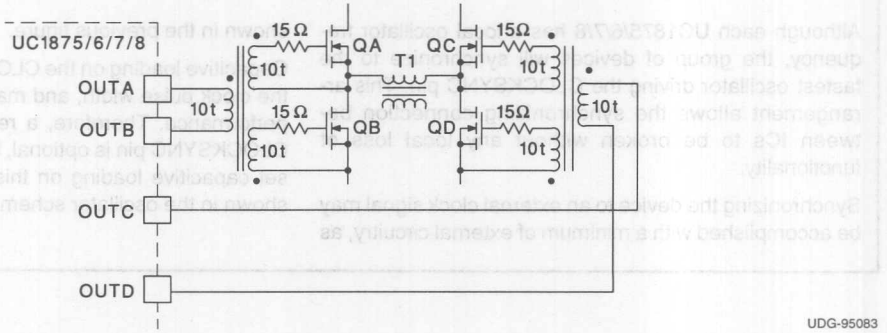
In each of the output stages, transistors Q3 through Q6 form a high-speed totem-pole driver which will source or sink more than one amp peak with a total delay of approximately 30 nanoseconds. To ensure a low output level prior to turn-on, transistors Q7 through Q9 form a self-biased driver to hold Q6 on prior to the supply reaching its turn-on threshold. This circuit is operable when the chip supply is zero. Q6 is also turned on and held low with a signal from the fault logic portion of the chip.



The delay providing the dead-time is accomplished with C1 which must discharge to VTH before the output can go high. The time is defined by the current sources, I1, which is programmed by an external resistor, RTD. The voltage on the Delay Set pins is internally regulated to 2.5V and the range of dead time control is from 50 to 200 nanoseconds. NOTE: There is no way to disable the delay circuitry, and the delay time must be programmed.

OUTPUT SWITCH ORIENTATION

The four outputs of the UC1875/6/7/8 interface to the full bridge converter switches as shown below:



3 Winding Bifilar, AWG 30 Kynar Insulation

APPLICATIONS INFORMATION (cont.)

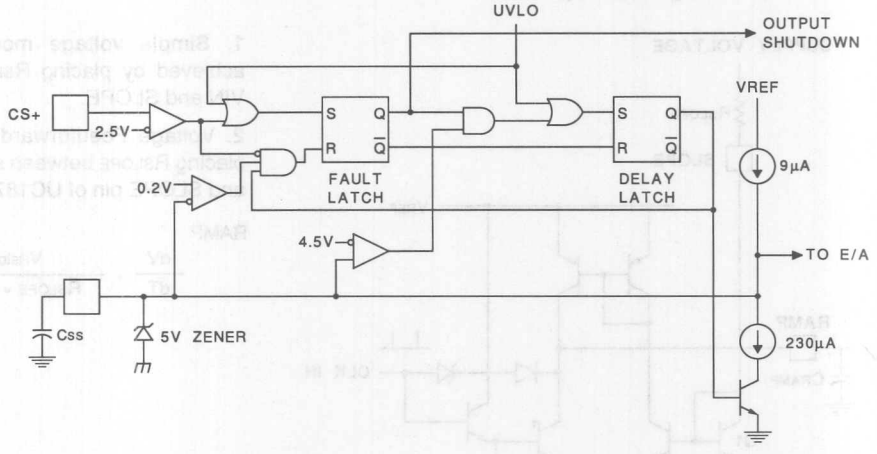
FAULT/SOFT-START

The fault control circuitry provides two forms of power shutdown:

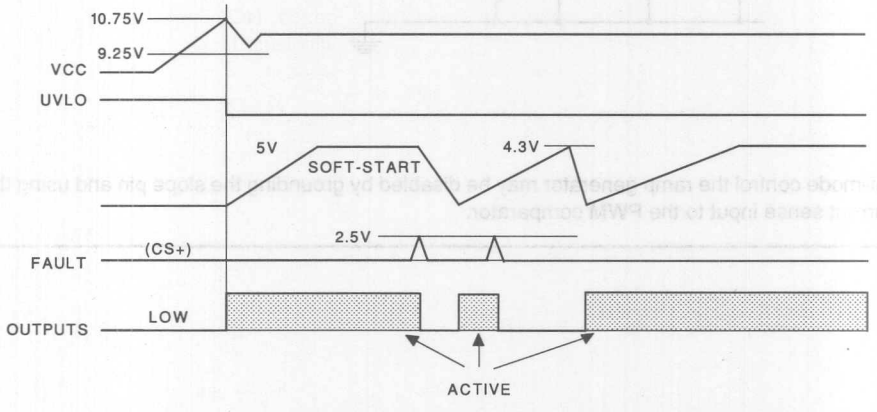
- Complete turn-off of all four output power stages.
- Clamping the phase shift command to zero.

Complete turn-off is ordered for an over-current fault or a low supply voltage. When the SOFTSTART pin reaches its low threshold, switching is allowed to proceed while the phase-shift is advanced from zero to its nominal value with the time constant of the SOFT-START capacitor.

The fault logic insures that a continuous fault will institute a low frequency "hiccup" retry cycle by forcing the SOFT-START capacitor to charge through its full cycle between each restart attempt.



UDG-95084



UDG-95085

APPLICATIONS INFORMATION (cont.)

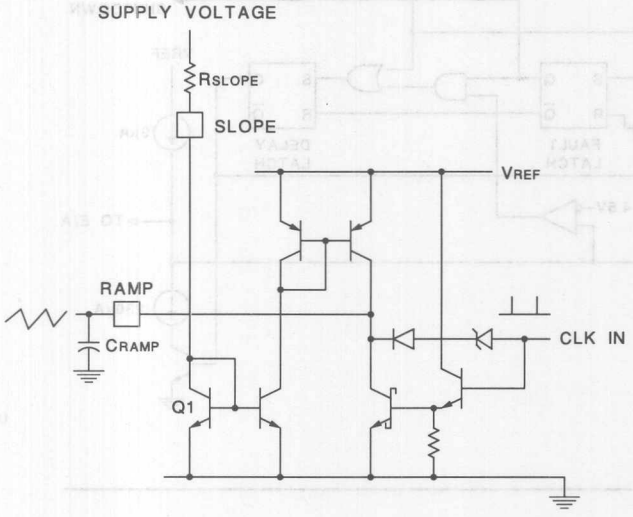
SLOPE/RAMP PINS

The ramp generator may be configured for the following control methods:

- Voltage Mode
- Voltage Feedforward
- Current Mode
- Current Mode with Slope Compensation

The figure below shows a voltage-mode configuration. With RSLOPE tied to a stable voltage source, the waveform on CRAMP will be a constant-slope ramp, providing conventional voltage-mode control. If RSLOPE is connected to the power supply input voltage, a variable-slope ramp will provide voltage feedforward.

Voltage Mode Operation



1. Simple voltage mode operation achieved by placing RSLOPE between VIN and SLOPE.

2. Voltage Feedforward achieved by placing RSLOPE between supply voltage and SLOPE pin of UC1875.

RAMP

$$\frac{dV}{dT} \approx \frac{V_{Rslope}}{R_{SLOPE} \bullet C_{RAMP}}$$

For current-mode control the ramp generator may be disabled by grounding the slope pin and using the ramp pin as a direct current sense input to the PWM comparator.

UNITRODE CORPORATION
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Phase Shift Resonant Controller

FEATURES

- Programmable Output Turn On Delay; Zero Delay Available
- Compatible with Voltage Mode or Current Mode Topologies
- Practical Operation at Switching Frequencies to 300kHz
- Four 100mA Totem Pole Outputs
- 10MHz Error Amplifier
- Pin Programmable Undervoltage Lockout
- Low Startup Current - 150µA
- Soft Start Control
- Outputs Active Low During UVLO

DESCRIPTION

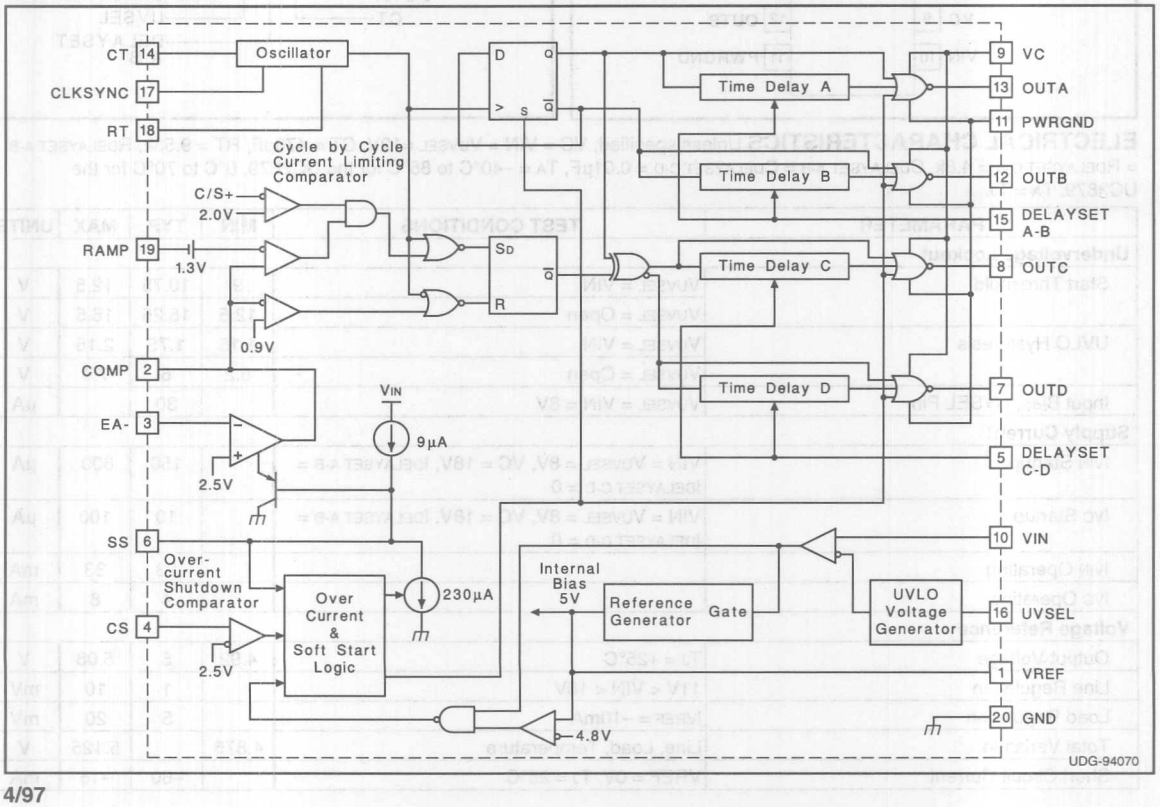
The UC3879 controls a bridge power stage by phase shifting the switching of one half-bridge with respect to the other. This allows constant frequency pulse width modulation in combination with resonant, zero-voltage switching for high efficiency performance. The UC3879 can be configured to provide control in either voltage mode or current mode operation, with overcurrent shutdown for fast fault protection.

Independently programmable time delays provide dead-time at the turn-on of each output stage, allowing time for each resonant switching interval.

With the oscillator capable of operating in excess of 600kHz, overall output switching frequencies to 300kHz are practical. In addition to the standard free running mode, with the CLKSYNC pin, the user may configure the UC3879 to accept an external clock synchronization signal. Alternatively, up to three units can be locked together with the operational frequency determined by the fastest device.

Protective features include an undervoltage lockout and overcurrent protection. Additional features include a 10MHz error amplifier, a 5V precision reference, and soft start. The UC3879 is available in 20 pin N, J, DW, and Q and 28 pin L packages.

BLOCK DIAGRAM



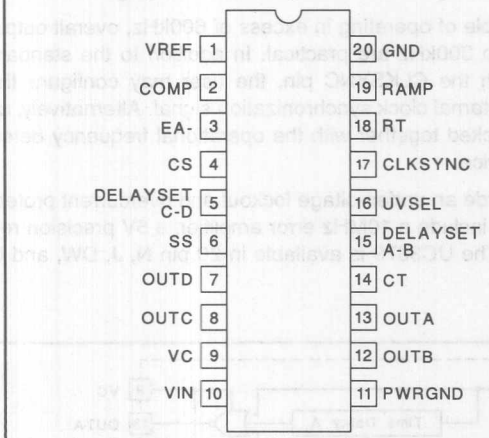
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (VC, VIN) 20V
Output Current, Source or Sink, DC 20mA
Analog I/Os
(Pins 1, 2, 3, 4, 5, 6, 14, 15, 17, 18, 19) . . . . . –0.3 to 5.3V
(Pin 16) . . . . . –.03V to VIN
Storage Temperature Range . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

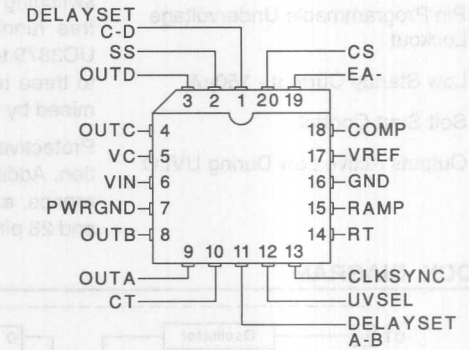
Notes: Pin references are to 20 pin DIL and SOIC packages. All voltages are with respect to ground unless otherwise stated. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAMS

DIL-20, SOIC-20 (Top View)
J or N Package, DW Package



PLCC-20 (Top View)
Q Package



ELECTRICAL CHARACTERISTICS

Unless specified; VC = VIN = V_{UVSEL} =12V, CT = 470pF, RT = 9.53k, $R_{DELAYSET\ A-B}$ = $R_{DELAYSET\ C-D}$ = 4.8k, $C_{DELAYSET\ A-B}$ = $C_{DELAYSET\ C-D}$ = 0.01µF, T_A = –40°C to 85°C for the UC2879, 0°C to 70°C for the UC3879. T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Undervoltage Lockout					
Start Threshold	V_{UVSEL} = VIN	9	10.75	12.5	V
	V_{UVSEL} = Open	12.5	15.25	16.5	V
UVLO Hysteresis	V_{UVSEL} = VIN	1.15	1.75	2.15	V
	V_{UVSEL} = Open	5.2	6	7.4	V
Input Bias, UVSEL Pin	V_{UVSEL} = VIN = 8V		30		µA
Supply Current					
I_{VIN} Startup	VIN = V_{UVSEL} = 8V, VC = 18V, $I_{DELAYSET\ A-B}$ = $I_{DELAYSET\ C-D}$ = 0		150	600	µA
I_{VC} Startup	VIN = V_{UVSEL} = 8V, VC = 18V, $I_{DELAYSET\ A-B}$ = $I_{DELAYSET\ C-D}$ = 0		10	100	µA
I_{VIN} Operating			23	33	mA
I_{VC} Operating			4	8	mA
Voltage Reference					
Output Voltage	T_J = +25°C	4.92	5	5.08	V
Line Regulation	11V < VIN < 18V		1	10	mV
Load Regulation	I_{VREF} = –10mA		5	20	mV
Total Variation	Line, Load, Temperature	4.875		5.125	V
Short Circuit Current	VREF = 0V, T_J = 25°C		–60	–15	mA

ELECTRICAL CHARACTERISTICS (cont.) Unless specified; VC = VIN = V_{UVSEL} =12V, CT = 470pF, RT = 9.53k, $I_{DELAYSET\ A-B}$ = $I_{DELAYSET\ C-D}$ = –500µA $C_{DELAYSET\ A-B}$ = $C_{DELAYSET\ C-D}$ = 0.01µF, T_A = –40°C to 85°C for the UC2879, 0°C to 70°C for the UC3879. T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Error Amplifier					
Error Amplifier Input Voltage		2.4	2.5	2.6	V
Input Bias Current			0.6	3	µA
AVOL	1V < V_{COMP} < 4V	60	90		dB
PSRR	11V < VIN < 18V	85	100		dB
Output Sink Current	V_{COMP} = 1V	1	2.5		mA
Output Source Current	V_{COMP} = 4V		-1.3	-0.5	mA
Output Voltage High	I_{COMP} = –0.5mA	4	4.7	5	V
Output Voltage Low	I_{COMP} = 1mA	0	0.5	1	V
Slew Rate	T_A = +25°C	6	11		V/µs
PWM Comparator					
RAMP Offset Voltage	T_J = 25°C, Note 3	1.1	1.25	1.4	V
PWM Phase Shift,	V_{COMP} > $V_{RAMPpeak}$ + $V_{RAMPoffset}$	98	99.7	102	%
$T_{DELAYSET\ A-B,\ C-D}$ = 0, Note 1	V_{COMP} < Zero Phase Shift Voltage	0	0.3	2	%
Output Skew,	V_{COMP} > $V_{RAMPpeak}$ + $V_{RAMPoffset}$		10		ns
$T_{DELAYSET\ A-B,\ C-D}$ = 0, Note 1	V_{COMP} < Zero Phase Shift Voltage		10		ns
Ramp to Output Delay, $T_{DELAYSET\ A-B,\ C-D}$ = 0			115	250	ns
Oscillator					
Initial Accuracy	T_A = 25°C	180	200	220	kHz
Voltage Stability	11V < VIN < 18V		1	2	%
Total Variation	Line, Temperature	160	200	240	kHz
CLKSYNC Threshold		2.3	2.5	2.7	V
Clock Out High		2.8	4		V
Clock Out Low		0.5	1	1.5	V
Clock Out Pulse Width			400	600	ns
Ramp Valley Voltage			0.2	0.4	V
Ramp Peak Voltage		2.8	2.9	3.2	V
Current Limit					
Input Bias	V_{CS} = 3.0V		2	10	µA
Threshold Voltage		2.35	2.5	2.65	V
Delay to OUTA, B, C, D			160	300	ns
Cycle-by-Cycle Current Limit					
Input Bias	V_{CS} = 2.2V		2	10	µA
Threshold Voltage		1.85	2	2.15	V
Delay to Output Zero Phase			110	300	ns
Soft Start/Reset Delay					
Charge Current	V_{SS} = 0.5V	–20	–9	–3	µA
Discharge Current	V_{SS} = 1V	120	230		µA
Restart Threshold		4.3	4.7		V
Discharge Level			300		mV
Output Drivers					
Output Low Level	I_{OUT} = 10mA		0.3	0.4	V
Output High Level	I_{OUT} = –10mA, Referenced to VC		2.2	3	V

ELECTRICAL CHARACTERISTICS (cont.) Unless specified; VC = VIN = V_{UVSEL} =12V, CT = 470pF, RT = 9.53k, $I_{DELAYSET\ A\text{-}B}$ = $I_{DELAYSET\ C\text{-}D}$ = –500µA $C_{DELAYSET\ A\text{-}B}$ = $C_{DELAYSET\ C\text{-}D}$ = 0.01µF, T_A = –40°C to 85°C for the UC2879, 0°C to 70°C for the UC3879. T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Delay Set (Note 5)					
Delay Time	$R_{DELAYSET\ A\text{-}B}$ = $R_{DELAYSET\ C\text{-}D}$ = 4.8k	300	450	600	ns
Delay Time	$R_{DELAYSET\ A\text{-}B}$ = $R_{DELAYSET\ C\text{-}D}$ = 1.9k	130	200	250	ns
Zero Delay	$V_{DELAYSET\ A\text{-}B}$ = $V_{DELAYSET\ C\text{-}D}$ = 5V		5		ns

Note 1. Phase shift percentage (0% = 0°, 100% = 180°) is defined as

$$\theta = \frac{200}{T}\Phi\ \%$$

where θ is the phase shift, and Φ and T are defined in Figure 1. At 0% phase shift, Φ is the output skew.

Note 2. Delay time is defined as

$$\text{delay} = T \bullet \left(\frac{1}{2} - \text{duty cycle}\right)$$

where T is defined in Figure 1.

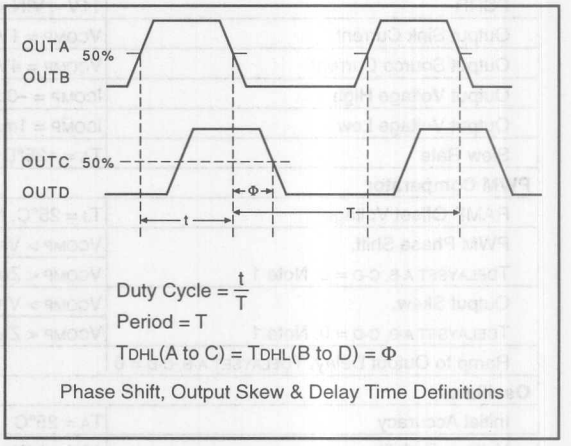
Note 3. Ramp offset voltage has a temperature coeffecient of about –4mV/°C.

Note 4. The zero phase shift voltage is the voltage measured at COMP which forces zero phase shift. This condition corresponds to zero effective output power. Zero phase shift voltage has a temperature coeffecient of about –2mV/°C.

Note 5. Delay time can be programmed via resistors from the delay set pins to ground.

$$\text{Delay time} = [1.04 \bullet 10^{-10} \bullet R_{DELAY}]\ sec.$$

The recommended range for R_{DELAY} is 1.9k to 10k.



Duty Cycle = $\frac{t}{T}$

Period = T

T_{DHL}(A to C) = T_{DHL}(B to D) = Φ

Phase Shift, Output Skew & Delay Time Definitions

Figure 1

PIN DESCRIPTIONS

CLKSYNC (Bi-directional Clock and Synchronization): Used as an output, CLKSYNC provides a clock signal. As an input, this pin provides a synchronization point. Multiple UC3879s, each with their own local oscillator frequency, may be connected together by the CLKSYNC pin, and they will synchronize to the fastest oscillator. This pin may also be used to synchronize the UC3879 to an external clock, provided the frequency of the external signal is higher than the frequency of the local oscillator. CLKSYNC is internally connected to an emitter follower pull-up and a current source pull-down (300µA typical). Therefore an external resistor to GND can be used to improve the CLKSYNC pin's ability to drive capacitive loads.

COMP (Error Amplifier Output): This pin is the output of the gain stage for overall feedback control. Error amplifier output voltage levels below 0.9 volt forces zero phase shift. Since the error amplifier has a relatively low current drive capability, the output may be overridden by driving it with a sufficiently low impedance source.

CT (Oscillator Frequency Set): After choosing RT to set the required upper end of the linear duty cycle range, the timing capacitor (CT) value is calculated to set the oscillator frequency as follows:

$$CT = \frac{D_{lin}}{1.08 \bullet RT \bullet f}$$

Connect the timing capacitor directly between CT and GND. Use a high quality ceramic capacitor with low ESL and ESR for best results. A minimum CT value of 200pF insures good accuracy and less susceptibility to circuit layout parasitics. The oscillator and PWM are designed to provide practical operation to 600kHz.

CS (Current Sense): This pin is the non-inverting input to the two current fault comparators whose references are set internally to fixed values of 2.0V and 2.5V. When the voltage at this pin exceeds 2.0V, and the error amplifier output voltage exceeds the voltage on the ramp input, the phase shift limiting overcurrent comparator will limit the phase shifting on a cycle-by-cycle basis. When the voltage at this pin exceeds 2.5V, the current fault latch is set, the outputs are forced OFF, and a soft start cycle is initiated. If a constant voltage above 2.5V is applied to this pin the outputs are disabled and held low. When CS

PIN DESCRIPTIONS (cont.)

is brought below 2.5V, the outputs will begin switching at 0 degrees phase shift before the SS pin begins to rise. This condition will not prematurely deliver power to the load.

DELAYSET A-B, C-D (Output Delay Control): The user programmed currents from these pins to GND set the turn on delay for the corresponding output pair. This delay is introduced between the turn off of one switch and the turn on of another in the same leg of the bridge to allow resonant switching to take place. Separate delays are provided for the two half-bridges to accommodate differences in the resonant capacitor charging currents.

EA- (Error Amplifier Inverting Input): This is normally connected to the voltage divider resistors which sense the power supply output voltage level. The loop compensation components are connected between this pin and COMP.

GND (Signal Ground): All voltages are measured with respect to GND. The timing capacitor on CT, and bypass capacitors on VREF and VIN should be connected directly to the ground plane near GND.

OUT A-OUT D (Outputs A-D): The outputs are 100mA totem pole output drivers optimized to drive FET driver ICs. The outputs operate as pairs with a nominal 50% duty cycle. The A-B pair is intended to drive one half-bridge in the external power stage and is synchronized to the clock waveform. The C-D pair drives the other half-bridge with switching phase shifted with respect to the A-B outputs.

PWRGND (Power Ground): VC should be bypassed with a ceramic capacitor from VC to the section of the ground plane that is connected to PWRGND. Any required bulk reservoir capacitor should be connected in parallel. PWRGND and GND should be connected at a single point near the chip to optimize noise rejection and minimize DC voltage drops.

RAMP (Voltage Ramp): This pin is the input to the PWM comparator. Connect it to CT for voltage mode control. For current mode control, connect RAMP to CS and also to the output of the current sense transformer circuit. Slope compensation can be achieved by injecting a portion of the ramp voltage from CT to RAMP.

RT (Clock/Sync Duty Cycle Set Pin): The UC3879 oscillator produces a sawtooth waveform. The rising edge is generated by connecting a resistor from RT to GND and a capacitor from CT to GND (see CT pin description). During the rising edge, the modulator has linear control of the duty cycle. The duty cycle jumps to 100% when the voltage on COMP exceeds the oscillator peak voltage. Selection of RT should be done first, based on the required upper end of the linear duty cycle range (D_{lin}) as follows:

$$RT = \frac{2.5}{10mA \bullet (1 - D_{lin})}$$

Recommended values for RT range from 2.5k to 100k.

SS: Connect a capacitor between this pin and GND to set the soft start time. The voltage at SS will remain near zero volts as long as VIN is below the UVLO threshold. Soft start will be pulled up to about 4.8V by an internal 9µA current source when VIN and VREF become valid (assuming a non-fault condition). In the event of a current fault (CS voltage exceeding 2.5V), soft start will be pulled to GND and then ramp to 4.8V. If a fault occurs during the soft start cycle, the outputs will be immediately disabled and soft start must fully charge prior to resetting the fault latch. For paralleled controllers, the soft start pins may be paralleled to a single capacitor, but the charge currents will be additive.

UVSEL: Connecting this pin to VIN sets a turn on voltage of 10.75V with 1.5V of UVLO hysteresis. Leaving the pin open-circuited programs a turn on voltage of 15.25V with 6.0V of hysteresis.

VC (Output Switch Supply Voltage): This pin supplies power to the output drivers and their associated bias circuitry. The difference between the output high drive and VC is typically 2.1V. This supply should be bypassed directly to PWRGND with a low ESR/ESL capacitor.

VIN (Primary Chip Supply Voltage): This pin supplies power to the logic and analog circuitry on the integrated circuit that is not directly associated with driving the output stages. Connect VIN to a stable source above 12V for normal operation. To ensure proper functionality, the UC3879 is inactive until VIN exceeds the upper undervoltage lockout threshold. This pin should be bypassed directly to GND with a low ESR/ESL capacitor. NOTE: When VIN exceeds the UVLO threshold the supply current (I_{IN}) jumps from about 100µA to greater than 20mA. If the UC3879 is not connected to a well bypassed supply, it may immediately enter the UVLO state again. Therefore, sufficient bypass capacity must be added to ensure reliable startup.

VREF: This pin provides an accurate 5V voltage reference. It is internally short circuit current limited. VREF is disabled while VIN is below the UVLO threshold. The circuit is also disabled until VREF reaches approximately 4.75V. For best results bypass VREF with a 0.1µF, low ESR/ESL capacitor.

UNITRODE CORPORATION
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Pentium® Pro Controller

FEATURES

- Combined DAC/Voltage Monitor and PWM Functions
- 4-Bit Digital-to-Analog Converter (DAC)
- 1.0% DAC/Reference
- Low Offset X20 Current Sense Amplifier
- 100kHz, 200kHz, 400kHz Oscillator Frequency Options
- Foldback Current Limiting
- Overvoltage and Undervoltage Fault Windows
- Undervoltage Lockout
- 2Ω Totem Pole Output
- Chip Disable Function

DESCRIPTION

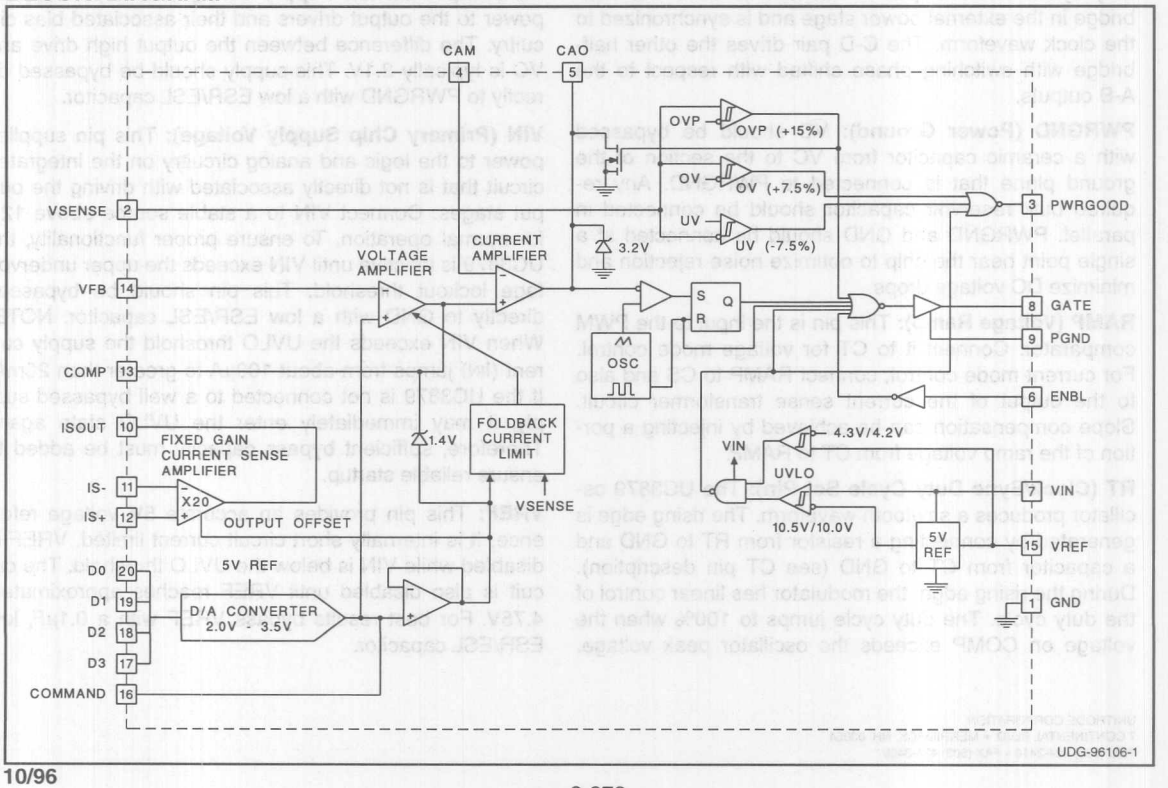
The UCC3880-4/-5/-6 combines high precision reference and voltage monitoring circuitry with average current mode PWM controller circuitry to power Intel Pentium Pro and other high-end microprocessors with a minimum of external components. The UCC3880-x converts 5VDC to an adjustable output, ranging from 2.0VDC to 3.5VDC in 100mV steps with 1% DC system accuracy.

The chip includes a precision 5V reference which is capable of sourcing current to an external load. The output voltage of the DAC is derived from this reference, and is programmed directly by Intel's VID pins (Table 1).

The accuracy of the DAC/reference combination is 1.0%. The overvoltage and undervoltage comparators monitor the system output voltage and indicate when it rises above or falls below its programmed value by more than 7.5%. A second overvoltage protection comparator pulls the current amplifier output voltage low to force zero duty cycle when the system output voltage exceeds its designed value by more than 15%. This comparator also terminates the cycle. Undervoltage lockout circuitry assures the correct logic states at the outputs during powerup and powerdown. Grounding the ENABLE pin forces the GATE output low.

(continued)

BLOCK DIAGRAM



DESCRIPTION (cont.)

The voltage and current amplifiers have a 4MHz gain bandwidth product to satisfy high performance system requirements. The internal current sense amplifier permits the use of a low value current sense resistor, minimizing power loss. The oscillator frequency is fixed internally at 100kHz, 200kHz, or 400kHz, depending upon the option selected. The foldback circuit reduces the converter short circuit current limit to 50% of its nominal value when the converter is short circuited. The gate driver is a 2Ω totem pole output stage capable of driving an external MOSFET.

This device is available in 20-pin dual in-line and surface mount packages. The UCC2880-x is specified for operation from –25°C to 85°C, and the UCC3880-x is specified for operation from 0°C to 70°C.

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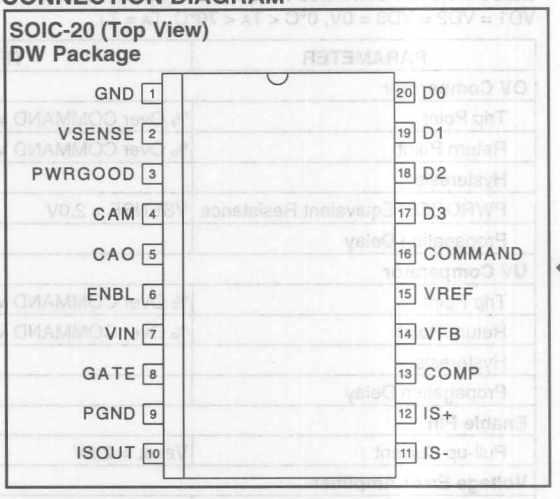
ORDERING INFORMATION

UCC ☐ 880 ☐ - ☐
- ☐ — See Frequency Gain Table
- ☐ — Package
- ☐ — Temperature Range

Consult factory for temperature range or package options not shown.

CONNECTION DIAGRAM

SOIC-20 (Top View)
DW Package



Frequency Gain Table

	Frequency		
	100kHz	200kHz	400kHz
UCC3880-4	X		
UCC3880-5		X	
UCC3880-6			X

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, VIN = 12V, VSENSE = 3.5V, V_{ENBL} = 5V, VD0 = VD1 = VD2 = VD3 = 0V, 0°C < T_A < 70°C, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Undervoltage Lockout					
VIN UVLO Turn-on Threshold			10.5	10.8	V
VIN UVLO Turn-off Threshold		9.5	10		V
UVLO Threshold Hysteresis			500		mV
Supply Current					
I_{IN}			3.5		mA
DAC/Reference					
COMMAND Voltage Accuracy	10.8V < VIN < 13.2V, I_{VREF} = 0mA	–1		1	%
D0-D3 Voltage High	DX Pin Floating		5		V
D0-D3 Input Bias Current	DX Pin Tied to GND		–70	–20	µA
VREF Output Voltage		4.975	5	5.025	V
VREF Load Regulation	I_{VREF} = 0mA to 5mA	–10	0		mV
VREF Sourcing Current	VREF = 0V		10		mA
OVP Comparator					
Trip Point	% Over COMMAND Voltage	10	15	20	%
Hysteresis			20	30	mV
VSENSE Input Bias Current	OV, OVP, UV Combined		–0.1		µA
Propagation Delay			1		µs

ELECTRICAL CHARACTERISTICS (cont.): Unless otherwise specified, VIN = 12V, VSENSE = 3.5V, V_{ENBL} = 5V, VD0 = VD1 = VD2 = VD3 = 0V, 0°C < T_A < 70°C, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
OV Comparator					
Trip Point	% Over COMMAND Voltage (Note 1)		7.6	10	%
Return Point	% Over COMMAND Voltage (Note 1)	5	7.4		%
Hysteresis			20	30	mV
PWRGOOD Equivalent Resistance	VSENSE = 2.0V			470	Ω
Propagation Delay			1		µs
UV Comparator					
Trip Point	% Over COMMAND Voltage (Note 1)	–10	–7.6		%
Return Point	% Over COMMAND Voltage (Note 1)		–7.4	–5	%
Hysteresis			20	30	mV
Propagation Delay			1		µs
Enable Pin					
Pull-up Current	V_{ENBL} = 2.5V		–50	–20	µA
Voltage Error Amplifier					
Input Offset Voltage	V_{COMP} = 3.5V		0.0		mV
Input Bias Current	V_{CM} = 3.0V		–0.02	0	µA
Open Loop Gain	1V < V_{COMP} < 4V		90		dB
Common Mode Rejection Ratio	2V < V_{COMP} < 3.5V		90		dB
Power Supply Rejection Ratio	10.8V < VIN < 15V		85		dB
Output Sourcing Current	V_{VFB} = 2V, $V_{COMMAND}$ = V_{COMP} = 2.5V		–0.5		mA
Output Sinking Current	V_{VFB} = 3V, $V_{COMMAND}$ = V_{COMP} = 2.5V		2.0		mA
Gain Bandwidth Product	F = 100kHz		3		MHz
Current Sense Amplifier					
Gain			20		V/V
Input Resistance			5		kΩ
Common Mode Rejection Ratio	0V < V_{CM} < 4.5V		60		dB
Power Supply Rejection Ratio	10.8V < VIN < 15V		80		dB
Output Sourcing Current	V_{IS-} = 2V, V_{ISOUT} = V_{IS+} = 2.5V		–0.5		mA
Output Sinking Current	V_{IS-} = 3V, V_{ISOUT} = V_{IS+} = 2.5V		6.0		mA
–3dB Frequency	At GAIN = 20		1.75		MHz
Current Amplifier					
Input Offset Voltage	V_{CM} = 3.0V			10	mV
Input Bias Current	V_{CM} = 3.0V		0.15		µA
Open Loop Gain	1V < V_{CAO} < 3V		90		dB
Output Voltage High	V_{COMP} = 3V, V_{CAM} = 2.5V		3.2		V
Common Mode Rejection Ratio	1.5V < V_{CM} < 4.9V		80		dB
Power Supply Rejection Ratio	10.8V < VIN < 15V		80		dB
Output Sourcing Current	V_{CAM} = 2V, V_{CAO} = V_{COMP} = 2.5V		–0.5		mA
Output Sinking Current	V_{CAM} = 3V, V_{CAO} = V_{COMP} = 2.5V		2.0		mA
Gain Bandwidth Product	F = 100kHz		3.5		MHz

ELECTRICAL CHARACTERISTICS (cont.): Unless otherwise specified, VIN = 12V, VSENSE = 3.5V, V_{ENBL} = 5V, VD0 = VD1 = VD2 = VD3 = 0V, 0°C < T_A < 70°C, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator					
Frequency (-4)		85	100	115	kHz
Frequency (-5)			200		kHz
Frequency (-6)			400		kHz
Frequency Change With Voltage	10.8V < VIN < 15V		1		%
Output Section					
Maximum Duty Cycle		90	95	99	%
Output Low Voltage	I_{GATE} = –100mA		0.20		V
Output High Voltage	I_{GATE} = 100mA		11.8		V
Rise Time	C_{GATE} = 3.3nF		20	80	ns
Fall Time	C_{GATE} = 3.3nF		15	80	ns
Output Impedance	I_{GATE} = 100mA		2		Ω
	I_{GATE} = –100mA		2		Ω
Foldback Current Limit					
Clamp Level	Measured at Voltage EA Output; V_{SENSE} = $V_{COMMAND}$ = 3V		4.4		V
	$V_{COMMAND}$ = 3V, V_{SENSE} = 0		3.7		V

Note 1: This percentage is measured with respect to the ideal COMMAND voltage programmed by the D0 - D3 pins.

PIN DESCRIPTIONS (cont.)

CAM (Current Amplifier Inverting Input): The average load current feedback from ISOUT is applied through a resistor to this pin. The current loop compensation network is also connected to this pin (see CAO below).

CAO (Current Amplifier Output): The current loop compensation network is connected between this pin and CAM. The voltage on this pin is the input to the PWM comparator and regulates the output voltage of the system. The GATE output is disabled (held low) unless the voltage on this pin exceeds 1V, allowing the PWM to force zero duty cycle when necessary. The PWM forces maximum duty cycle when the voltage on CAO exceeds the oscillator peak voltage (3V). A 3.2V clamp circuit prevents the CAO voltage from rising excessively past the oscillator peak voltage for excellent transient response.

COMMAND (Digital-to-Analog Converter Output Voltage): This pin is the output of the 4-bit digital-to-analog converter (DAC) and the noninverting input of the voltage amplifier. The voltage on this pin sets the switching regulator output voltage. Setting all input control codes low produces 3.5V at COMMAND; setting all codes high produces 2.0V at COMMAND. The DAC LSB step size (i.e. resolution) is 100mV (See Table 1). The COMMAND source impedance is typically 1.2kΩ and must therefore drive only high impedance inputs if accuracy is to be maintained. Bypass COMMAND with a 0.01µF, low ESR, low ESL capacitor for best circuit noise immunity.

Decimal Code	D3	D2	D1	D0	COMMAND Voltage
15	1	1	1	1	2.0
14	1	1	1	0	2.1
13	1	1	0	1	2.2
12	1	1	0	0	2.3
11	1	0	1	1	2.4
10	1	0	1	0	2.5
9	1	0	0	1	2.6
8	1	0	0	0	2.7
7	0	1	1	1	2.8
6	0	1	1	0	2.9
5	0	1	0	1	3.0
4	0	1	0	0	3.1
3	0	0	1	1	3.2
2	0	0	1	0	3.3
1	0	0	0	1	3.4
0	0	0	0	0	3.5

Table 1. Programming the COMMAND Voltage

COMP (Voltage Amplifier Output): The system voltage compensation network is applied between COMP and VFB.

D0 - D3 (DAC Digital Input Control Codes): These are the DAC digital input control codes, with D0 representing the least significant bit (LSB) and D3, the most significant bit (MSB). A bit is set low by being connected to GND. A

PIN DESCRIPTIONS (cont.)

bit is set high by floating it, or connecting it to a 5V source. Each control pin is pulled up to approximately 5V by an internal 70µA current source.

ENBL (Chip Enable Pin): This input is used to disable the GATE and PWRGOOD outputs. Grounding this pin causes the GATE output to be held low; floating the pin or pulling it up to 5V ensures normal operation. ENBL is pulled up to 5V internally.

GATE (PWM Output, MOSFET Driver): This output provides a 2Ω totem pole driver. Use a series resistor of at least 5Ω between this pin and the gate of the external MOSFET to prevent excessive overshoot.

GND (Signal Ground): All voltages are measured with respect to GND. Bypass capacitors on the VCC and VREF pins should be connected directly to the ground plane near the GND pin.

IS– (Current Sense Amplifier Inverting Input): This pin is the inverting input to the current sense amplifier and is connected to the low side of the average current sense resistor.

IS+ (Current Sense Amplifier Noninverting Input): This pin is the noninverting input to the current sense amplifier and is connected to the high side of the average current sense resistor.

ISOUT (Current Sense Amplifier Output): This pin is the output of the current sense amplifier. The voltage on this pin is (COMMAND + G_{CSA} • I • R_{SENSE}), where COMMAND is the voltage on the COMMAND pin, G_{CSA} is the fixed gain of the current sense amplifier, equal to 20, I is the current through the sense resistor, and R_{SENSE} is the value of the average current sensing resistor.

PGND (Power Ground): This pin provides a dedicated ground for the output gate driver. The GND and PGND pins should be connected externally using a short printed circuit board trace close to the IC. Decouple VIN to PGND with a low ESR capacitor ≥ 0.10µF.

PWRGOOD (Undervoltage/Lower Overvoltage Output): This pin is an open drain output which is driven low to reset the microprocessor when VSENSE rises above or falls below its nominal value by 7.5%. The on resistance of the open drain switch will be no higher than 470Ω. The OV and UV comparators' hysteresis is fixed at 20mV independent of the COMMAND voltage.

VIN (Positive Supply Voltage): This pin supplies power to the chip. Connect VIN to a stable voltage source of at least 10.8V. The GATE and PWRGOOD outputs will be held low until VCC exceeds the upper undervoltage lockout threshold. This pin should be bypassed directly to the GND pin.

VFB (Voltage Amplifier Inverting Input): This input is connected to COMP through a feedback network and to the power supply output through a resistor or a divider network.

VREF (Voltage Reference Output): This pin provides an accurate 5V reference and is internally short circuit current limited. VREF powers the D/A converter and also provides a threshold voltage for the UVLO comparator. For best reference stability, bypass VREF directly to GND with a low ESR, low ESL capacitor of at least 0.01µF.

VSENSE (Output Voltage Sensing Input): This pin is connected to the system output voltage through a low pass filter. When the voltage on VSENSE rises above or falls below the COMMAND voltage by 7.5%, the PWRGOOD output is driven low to reset the microprocessor. When the voltage on VSENSE rises above the COMMAND voltage by 15%, the OVP comparator pulls the current amplifier output voltage below the oscillator valley voltage to force zero duty cycle at the GATE output. This pin is also used by the foldback current limiting circuitry.

APPLICATION INFORMATION

Current Limit

The short circuit current limit, I_{SC}, is set according to:

$$I_{SC} = \frac{1.4V}{R_{SENSE} \bullet G_{CSA}}$$

where R_{SENSE} is the average current sense resistor and G_{CSA} is the current sense amplifier gain, where G_{CSA} equals 20. Example: Choose R_{SENSE} to set the short circuit current limit at 16A using the UCC3880-5

$$R_{SENSE} = \frac{1.4V}{16A \bullet 20} = 4.4m\Omega$$

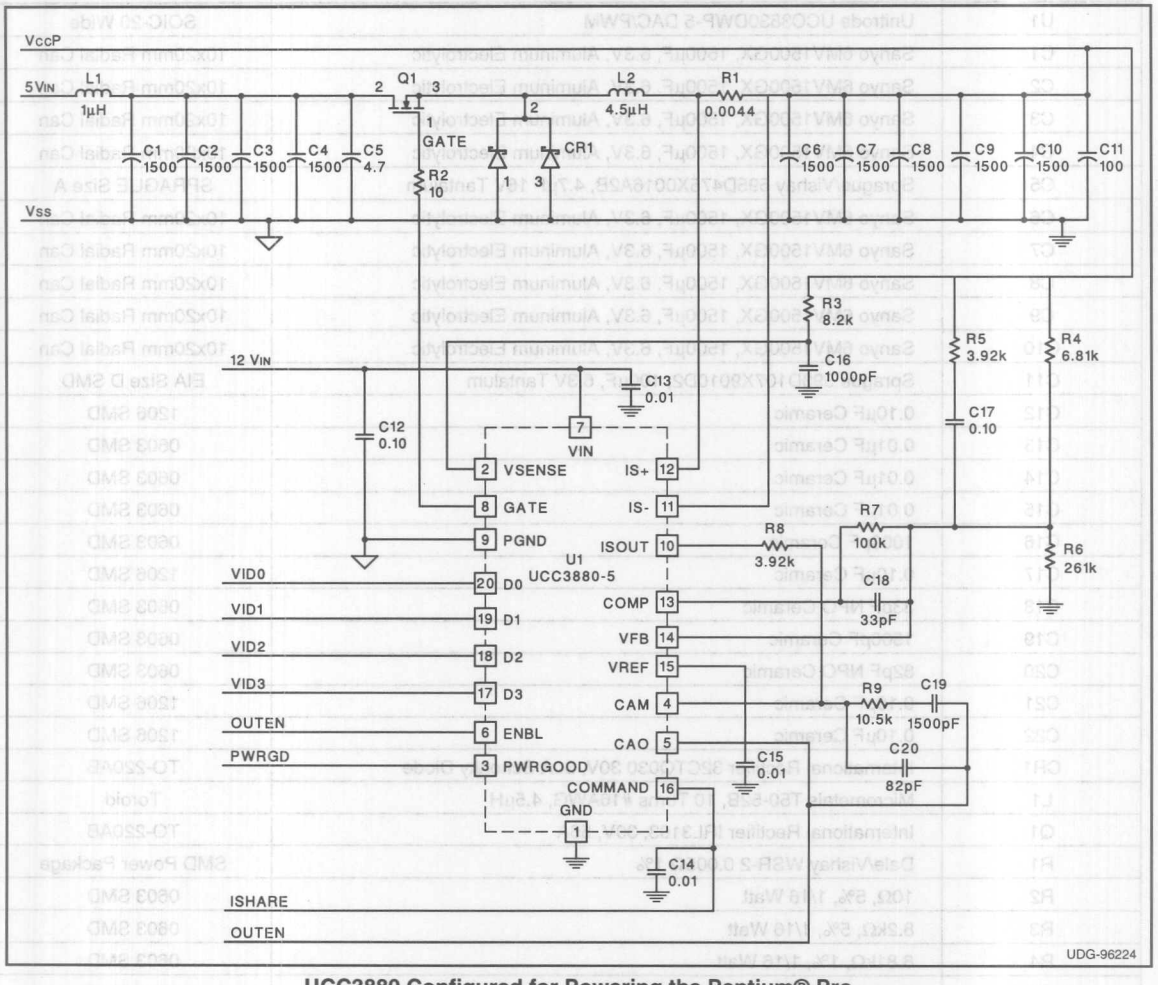
A lower resistance value may be needed if the AC ripple current in the inductor is more than 20% of the full load current.

Related Publications

U-156 and U-157 are Unitrode Application Notes describing the operation of the UC3886 and the UC3886/UC3910 together in a Pentium® Pro application.

TYPICAL APPLICATION

The UCC3880-x is ideal for converting the 5.0V system bus into the required Pentium® Pro bus voltage.



UCC3880 Configured for Powering the Pentium® Pro

PARTS LIST

REF.	DESCRIPTION	PACKAGE
U1	Unitrode UCC3830DWP-5 DAC/PWM	SOIC-20 Wide
C1	Sanyo 6MV1500GX, 1500µF, 6.3V, Aluminum Electrolytic	10x20mm Radial Can
C2	Sanyo 6MV1500GX, 1500µF, 6.3V, Aluminum Electrolytic	10x20mm Radial Can
C3	Sanyo 6MV1500GX, 1500µF, 6.3V, Aluminum Electrolytic	10x20mm Radial Can
C4	Sanyo 6MV1500GX, 1500µF, 6.3V, Aluminum Electrolytic	10x20mm Radial Can
C5	Sprague/Vishay 595D475X0016A2B, 4.7µF 16V Tantalum	SPRAGUE Size A
C6	Sanyo 6MV1500GX, 1500µF, 6.3V, Aluminum Electrolytic	10x20mm Radial Can
C7	Sanyo 6MV1500GX, 1500µF, 6.3V, Aluminum Electrolytic	10x20mm Radial Can
C8	Sanyo 6MV1500GX, 1500µF, 6.3V, Aluminum Electrolytic	10x20mm Radial Can
C9	Sanyo 6MV1500GX, 1500µF, 6.3V, Aluminum Electrolytic	10x20mm Radial Can
C10	Sanyo 6MV1500GX, 1500µF, 6.3V, Aluminum Electrolytic	10x20mm Radial Can
C11	Sprague 593D107X9010D2, 100µF, 6.3V Tantalum	EIA Size D SMD
C12	0.10µF Ceramic	1206 SMD
C13	0.01µF Ceramic	0603 SMD
C14	0.01µF Ceramic	0603 SMD
C15	0.01µF Ceramic	0603 SMD
C16	1000pF Ceramic	0603 SMD
C17	0.10µF Ceramic	1206 SMD
C18	33pF NPO Ceramic	0603 SMD
C19	1500pF Ceramic	0603 SMD
C20	82pF NPO Ceramic	0603 SMD
C21	0.10µF Ceramic	1206 SMD
C22	0.10µF Ceramic	1206 SMD
CR1	International Rectifier 32CTQ030 30V, 30A Schottky Diode	TO-220AB
L1	Micrometals T50-52B, 10 Turns #16AWG, 4.5µH	Toroid
Q1	International Rectifier IRL3103, 30V, 56A	TO-220AB
R1	Dale/Vishay WSR-2 0.005Ω 1%	SMD Power Package
R2	10Ω, 5%, 1/16 Watt	0603 SMD
R3	8.2kΩ, 5%, 1/16 Watt	0603 SMD
R4	6.81kΩ, 1%, 1/16 Watt	0603 SMD
R5	3.92kΩ, 1%, 1/16 Watt	0603 SMD
R6	261kΩ, 1%, 1/16 Watt	0603 SMD
R7	100kΩ, 1%, 1/16 Watt	0603 SMD
R8	3.92kΩ, 1%, 1/16 Watt	0603 SMD
R9	10.5kΩ, 1%, 1/16 Watt	0603 SMD
Q1-HS	AAVID 576802 TO-220 Heat Sink	TO-220AB
CR1-HS	AAVID 577002 TO-220 Heat Sink	TO-220AB

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High Performance Average Current Mode PWM

ADVANCED INFORMATION

FEATURES

- Combined Accurate Voltage Reference and PWM Functions
- 1% DAC/Reference
- Low Offset Voltage Amplifier
- High Bandwidth Current and Voltage Amplifiers
- Low Offset x10, x20 Current Sense Amplifier
- 100kHz, 200kHz, 400kHz Oscillator Frequency Options
- Foldback Current Limiting
- Undervoltage Lockout
- 1.5A Peak Totem Pole Output
- Chip Disable Function

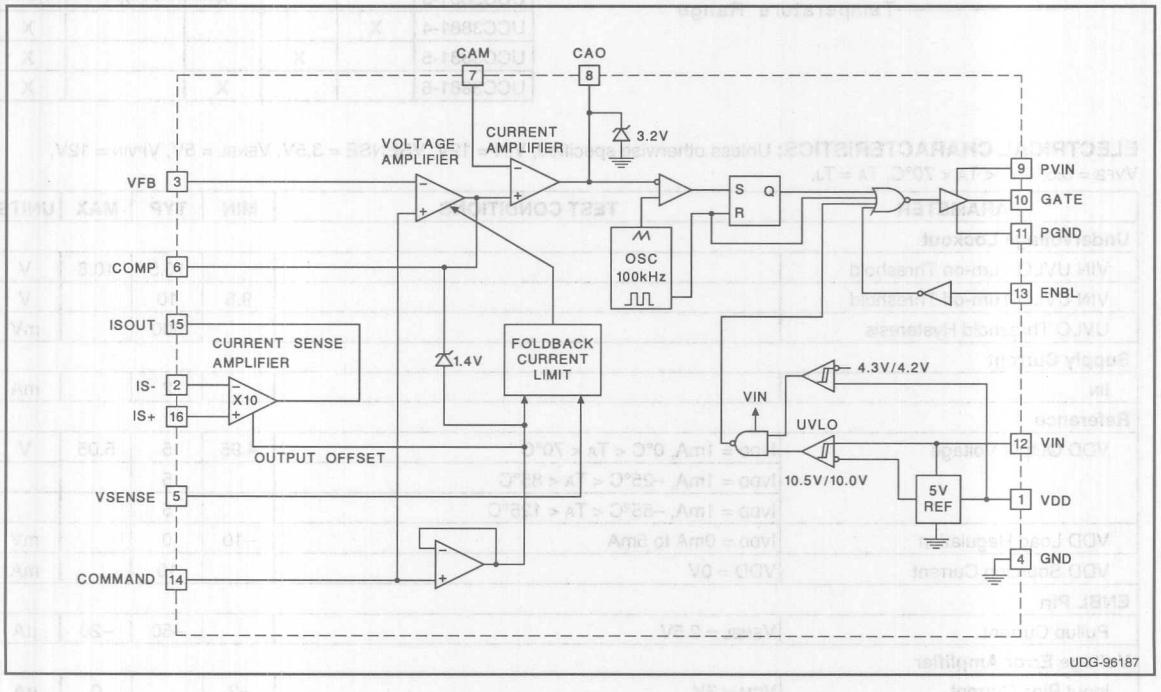
DESCRIPTION

The UCC3881-1,-2,-3,-4,-5,-6 combines high precision reference circuitry with average current mode PWM controller circuitry to power Intel Pentium® Pro and other high end microprocessors with a minimum of external components. The chip includes a precision 5V reference which is accurate to ±1% and is capable of sourcing current to external circuitry. Undervoltage lockout circuitry assures correct logic states at the output during power up and power down. Grounding the ENBL pin forces the GATE output low.

The voltage and current amplifiers have a 5.5MHz gain-bandwidth product to satisfy high performance system requirements. An internal current sense amplifier permits the use of a low value current sense resistor, minimizing power loss. Oscillator frequency is fixed internally at 100kHz, 200kHz, or 400kHz depending upon the option selected. Foldback circuitry reduces the converter current limit to 50% of its nominal value when the converter is short circuited. The gate driver is a totem pole output stage capable of driving an external MOSFET with 1.5A peak current.

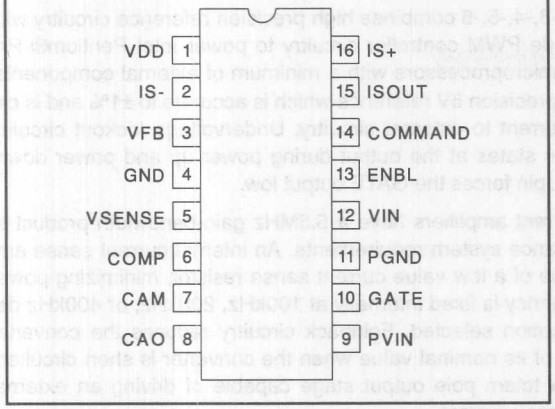
This device is available in 16-pin dual in-line and surface-mount packages. The UCC1881-x is specified for operation from –55°C to +125°C, the UCC2881-x is specified for operation from –25°C to +85°C, and the UCC3881-x is specified for operation from 0°C to 70°C.

BLOCK DIAGRAM



CONNECTION DIAGRAM

DIL-16, SOIC-16 (Top View)
N or J Package, DW Package



ORDERING INFORMATION



Frequency Gain Table

	Frequency			CS Amplifier Gain	
	100kHz	200kHz	400kHz	10	20
UCC3881-1	X			X	
UCC3881-2		X		X	
UCC3881-3			X	X	
UCC3881-4	X				X
UCC3881-5		X			X
UCC3881-6			X		X

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, VIN = 12V, VSENSE = 3.5V, V_{ENBL} = 5V, V_{PVIN} = 12V, V_{VFB} = 3.5, 0°C < T_A < 70°C, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Undervoltage Lockout					
VIN UVLO Turn-on Threshold			10.5	10.8	V
VIN UVLO Turn-off Threshold		9.5	10		V
UVLO Threshold Hysteresis			500		mV
Supply Current					
I_{IN}			2		mA
Reference					
VDD Output Voltage	I_{VDD} = 1mA, 0°C < T_A < 70°C	4.95	5	5.05	V
	I_{VDD} = 1mA, –25°C < T_A < 85°C		5		
	I_{VDD} = 1mA, –55°C < T_A < 125°C		5		
VDD Load Regulation	I_{VDD} = 0mA to 5mA	–10	0		mV
VDD Sourcing Current	VDD = 0V		10		mA
ENBL Pin					
Pullup Current	V_{ENBL} = 2.5V		–50	–20	µA
Voltage Error Amplifier					
Input Bias Current	V_{CM} = 3V	–2		0	µA
Input Offset Current	V_{CM} = 3V			0.01	µA
Open Loop Gain	1V < V_{COMP} < 4V		90		dB

ELECTRICAL CHARACTERISTICS (cont.): Unless otherwise specified, VIN = 12V, VSENSE = 3.5V, V_{ENBL} = 5V, V_{PVIN} = 12V, V_{VFB} = 3.5, 0°C < T_A < 70°C, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Voltage Error Amplifier (cont.)					
Common Mode Rejection Ratio	1V < VCM < 3.5V		80		dB
Power Supply Rejection Ratio	10.8V< VIN < 15V		85		dB
Output Sourcing Current	V_{VFB} = 2V, $V_{COMMAND}$ = V_{COMP} = 2.5V		–0.9		mA
Output Sinking Current	V_{VFB} = 3V, $V_{COMMAND}$ = V_{COMP} = 2.5V		7.2		mA
Gain Bandwidth Product	F = 100kHz	3			MHz
Current Sense Amplifier					
Gain (UCCx881-1,-2,-3)			10		V/V
Gain (UCCx881-4,-5,-6)			20		V/V
Input Resistance			5		kΩ
Common Mode Rejection Ratio	0V < V_{CM} < 4.5V		60		dB
Power Supply Rejection Ratio	10.8V < VIN < 15V		80		dB
Output Sourcing Current	V_{IS-} = 2V, V_{ISOUT} = V_{IS+} = 2.5V		–0.9		mA
Output Sinking Current	V_{IS-} = 3V, V_{ISOUT} = V_{IS+} = 2.5V		7.2		mA
–3dB Frequency (UCCx881-1,-2,-3)	At Gain = 10	3.5			MHz
–3dB Frequency (UCCx881-4,-5,-6)	At Gain = 20	1.75			MHz
Current Amplifier					
Input Offset Voltage	V_{CM} = 3V			10	mV
Input Bias Current	V_{CM} = 3V		0.1		µA
Open Loop Gain	1V < V_{CAO} < 3V		90		dB
Output Voltage High			3.2		V
Common Mode Rejection Ratio	1V < V_{CM} < 4.9V		80		dB
Power Supply Rejection Ratio	10.8V < VIN < 15V		80		dB
Output Sourcing Current	V_{CAM} = 2V, V_{CAO} = V_{COMP} = 2.5V		–0.9		mA
Output Sinking Current	V_{CAM} = 3V, V_{CAO} = V_{COMP} = 2.5V		7.2		mA
Gain Bandwidth Product	F = 100kHz	3.5			MHz
Oscillator					
Frequency (UCCx881-1,-4)	T_A = 25°C	85	100	115	kHz
Frequency (UCCx881-2,-5)	T_A = 25°C		200		kHz
Frequency (UCCx881-3,-6)	T_A = 25°C		400		kHz
Frequency Change with Voltage	10.8V < VIN < 15V		1		%
Output Section					
Maximum Duty Cycle		90	95	99	%
Output Low Voltage	I_{GATE} = –100mA		0.2		V
Output High Voltage	I_{GATE} = 100mA		11.8		V
Rise Time	C_{GATE} = 3.3nF		20	80	ns
Fall Time	C_{GATE} = 3.3nF		15	80	ns
Foldback Current Limit					
Clamp Level	Measured at Volt EA Output; VFB = $V_{COMMAND}$ = 3V		4.4		V
	$V_{COMMAND}$ = 3V, V_{VFB} = 0, VFB = $V_{COMMAND}$ = 3V		3.7		V
Output Impedance	I_{GATE} = 100mA		2		Ω
	I_{GATE} = –100mA		2		Ω

PIN DESCRIPTIONS

CAM (current amplifier inverting input): The average load current feedback from ISOUT is applied through a resistor to this pin. The current loop compensation network is also connected to this pin (see CAO below).

CAO (current amplifier output): The current loop compensation network is connected between this pin and CAM. The voltage on this pin is the input to the PWM comparator and regulates the output voltage of the system. The GATE output is disabled (held low) unless the voltage on this pin exceeds 1V, allowing the PWM to force zero duty cycle when necessary. The PWM forces 100% duty cycle when the voltage on CAO exceeds the oscillator peak voltage (3V). To provide superior transient response, a 3.2V clamp circuit prevents the CAO voltage from rising excessively past the oscillator peak voltage.

COMMAND (digital-to-analog converter output voltage): This pin is the noninverting input of the voltage amplifier. The voltage on this pin sets the switching regulator output voltage. A high accuracy voltage may be generated by connecting this pin to the tap point of a resistor divider connected between VDD and GND. Bypass COMMAND with a 0.01µF, low ESR, low ESL capacitor for best circuit noise immunity.

COMP (voltage amplifier output): The system voltage compensation network is applied between COMP and VFB.

GATE (PWM output, MOSFET driver): This output provides a 1.5A totem pole driver. Use a series resistor of at least 5Ω between this pin and the gate of the external MOSFET to prevent excessive overshoot. GATE has a typical output impedance of 2Ω.

GND (signal ground): All voltages are measured with respect to GND. Bypass capacitors on VIN and VDD should be connected directly to the ground plane near GND.

ENBL (chip enable pin): This input is used to disable the GATE output. Grounding this pin causes the GATE output to be held low; floating the pin or pulling it up to 5V ensures normal operation. ENBL is pulled up to 5V internally.

IS- (current sense amplifier inverting input): This pin is the inverting input to the current sense amplifier and is connected to the low side of the average current sense resistor.

IS+ (current sense amplifier noninverting input): This pin is the noninverting input to the current sense amplifier and is connected to the high side of the average current sense resistor.

ISOUT (current sense amplifier output): This pin is the output of the current sense amplifier. The voltage on this pin is (COMMAND + GCSA • I_{AVG} • R_{SENSE}), where COMMAND is the voltage on COMMAND, I_{AVG} is the average load current of the system, and R_{SENSE} is the value of the average current sensing resistor. GCSA is the fixed gain of the current sense amplifier (10 for UCCx881-1,-2,-3, and 20 for UCCx881-4,-5,-6).

PGND (power ground): This pin provides a dedicated ground for the output gate driver. GND and PGND should be connected externally using a short PC board trace. Decouple PVIN to PGND with a low ESR capacitor ≥0.1µF.

PVIN (positive power supply voltage): This pin provides a dedicated power supply connection for the output gate driver. This pin should be bypassed directly to PGND. VIN and PVIN may be tied together directly, or VIN may be filtered from PVIN.

VFB (voltage amplifier inverting input): This input is connected to COMP through a feedback network and to the power supply output through a resistor or a divider network.

VDD (voltage reference output): This pin provides an accurate 5V reference and is internally short circuit current limited. VDD also provides a threshold voltage for the UVLO comparator. For best reference stability, bypass VDD directly to GND with a low ESR, low ESL capacitor of at least 0.01µF.

VIN (positive signal supply voltage): This pin supplies power to the chip. Connect VIN to a stable voltage source that is at least 10.8V above GND and capable of sourcing at least 15mA. The GATE output will be held low until VDD exceeds the upper undervoltage lockout threshold. This pin should be bypassed directly to GND.

VSENSE (output voltage sensing input): This pin is connected directly to the system output voltage and is used by the foldback current limiting circuitry.

UNITRODE CORPORATION
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Average Current Mode Synchronous Controller With 5-Bit DAC

FEATURES

- Combined DAC/Voltage Monitor and PWM with Synchronous Rectification Functions
- 5-Bit Digital-to-Analog (DAC) Converter
- 1% DAC/Reference Combined Accuracy
- Compatible with 5V and 12V Systems and 12V-only Systems
- Low Offset Current Sense Amplifier
- Programmable Oscillator Frequency Practical to 700kHz
- Foldback Current Limiting
- Overvoltage and Undervoltage Fault Windows
- 2Ω Totem Pole Outputs with Programmable Dead Times to Eliminate Cross-Conduction
- Chip Disable Function

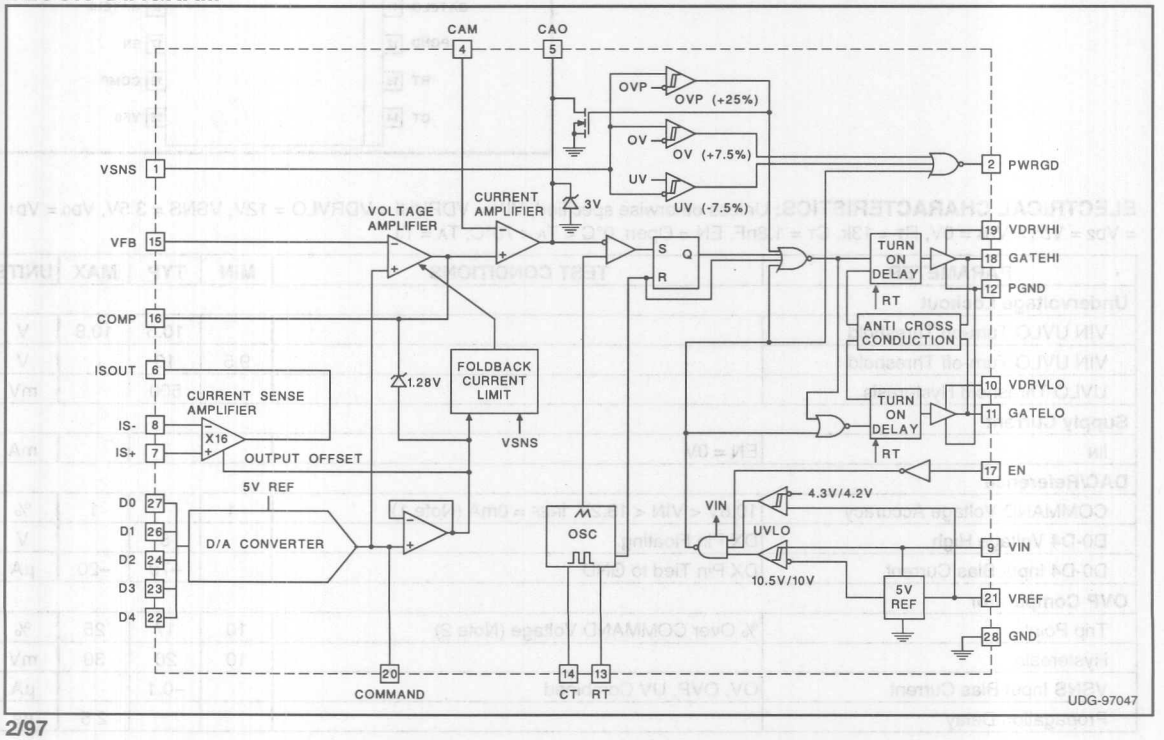
DESCRIPTION

The UCC3882 combines high precision reference and voltage monitoring circuitry with average current mode PWM synchronous rectification controller circuitry to power high-end microprocessors with a minimum of external components. The UCC3882 converts 5V or 12V to an adjustable output ranging from 1.8VDC to 2.05VDC in 50mV steps and 2.1VDC to 3.5VDC in 100mV steps with 1% DC system accuracy.

The chip includes a 5V precision reference which is capable of sourcing current to external circuitry. The output voltage of the DAC is derived from this reference, and is programmed directly by Intel's VID pins. The DAC output voltage covers 1.3V to 2.05V in 50mV steps and 2.1V to 3.5V in 100mV steps. The accuracy of the DAC/reference combination is better than 1%. Undervoltage lockout circuitry assures the correct logic states at the outputs during power up and power down. The overvoltage and undervoltage comparators monitor the system output voltage and indicate when it rises above or falls below its designed value by more than 7.5%. A second overvoltage comparator digitally forces GATEHI off and GATELO on when the system output voltage exceeds its designed value by more than 25%. Grounding the EN pin, programming a DAC output voltage below 1.8V, or programming all of the VID in-

(continued)

BLOCK DIAGRAM



DESCRIPTION (cont.)

puts high also disables the GATEHI and GATELO outputs, shutting down the power supply.

The voltage and current amplifiers have 5.5MHz gain-bandwidth product to satisfy high performance system requirements. The internal current sense amplifier permits the use of a low value current sense resistor, minimizing power loss. The oscillator frequency is externally programmed with R_T and C_T. The foldback circuit reduces the converter short circuit current limit to 50% of its nominal value when the converter is short-circuited, minimizing component stress and dissipation during abnormal conditions. The gate drivers are low impedance totem pole output stages capable of driving large external MOSFETs. Cross conduction is eliminated internally by programming the dead time between turn-off and turn on of the external high side and synchronous MOSFETs.

This device is available in a 28-pin wide body surface mount package. The UCC2882 is specified for operation from –25°C to +85°C and the UCC3882 is specified for operation from 0°C to 70°C.

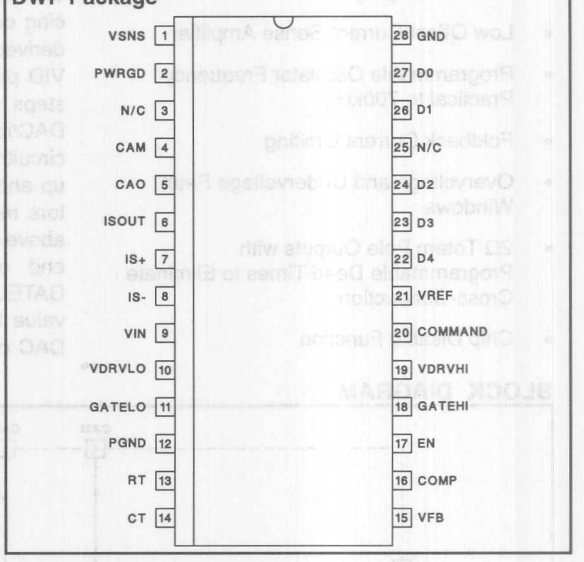
ABSOLUTE MAXIMUM RATINGS

VDRVHI, VDRVLO, GATEHI, GATELO . . . . . –0.3V to 20V
All other pins referenced to GND . . . . . –0.3V to 15V
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature. . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

Currents are positive into, negative out of the specified terminal.
Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

SOIC-28 (Top View)
DWP Package



ELECTRICAL CHARACTERISTICS: Unless otherwise specified, VIN = VDRVHI = VDRVLO = 12V, VSNS = 3.5V, V_{D0} = V_{D1} = V_{D2} = V_{D3} = V_{D4} = 0V, R_T = 13k, C_T = 1.8nF, EN = Open, 0°C < T_A < 70°C, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Undervoltage Lockout					
VIN UVLO Turn-on Threshold			10.5	10.8	V
VIN UVLO Turn-off Threshold		9.5	10		V
UVLO Threshold Hysteresis			500		mV
Supply Current					
I_{IN}	EN = 0V		7		mA
DAC/Reference					
COMMAND Voltage Accuracy	10.8V < VIN < 13.2V, I_{REF} = 0mA (Note 1)	–1		1	%
D0-D4 Voltage High	DX Pin Floating		5		V
D0-D4 Input Bias Current	DX Pin Tied to GND		–70	–20	µA
OVP Comparator					
Trip Point	% Over COMMAND Voltage (Note 2)	10	17	25	%
Hysteresis		10	20	30	mV
VSNS Input Bias Current	OV, OVP, UV Combined		–0.1		µA
Propagation Delay				2.5	µs

ELECTRICAL CHARACTERISTICS (cont.): Unless otherwise specified, VIN = VDRVHI = VDRVLO = 12V, VSNS = 3.5V, V_{D0} = V_{D1} = V_{D2} = V_{D3} = V_{D4} = 0V, R_T = 13k, C_T = 1.8nF, EN = Open, 0°C < T_A < 70°C, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
OV Comparator					
Trip Point	% Over COMMAND Voltage (Note 2)		7.6		%
Hysteresis		10	20	30	mV
PWRGD On Resistance				470	Ω
Propagation Delay				2.5	µs
UV Comparator					
Trip Point	% Over COMMAND Voltage (Note 2)		–7.6		%
Hysteresis		10	20	30	mV
Propagation Delay				2.5	µs
Enable Pin					
Pull Up Current	V_{EN} = 2.5V		–50	–20	µA
Voltage Error Amplifier					
Input Offset Voltage	V_{CM} = 3V		0		mV
Input Bias Current	V_{CM} = 3V	–2		0	µA
Input Offset Current	V_{CM} = 3V			0.01	µA
Open Loop Gain	2.05V < V_{COMP} < 3.05V		90		dB
Common Mode Rejection Ratio	2V < V_{CM} < 3.5V		90		dB
Power Supply Rejection Ratio	10.8V < VIN < 15V		85		dB
Output Sourcing Current	V_{VFB} = 2V, $V_{COMMAND}$ = V_{COMP} = 2.5V	–0.4			mA
Output Sinking Current	V_{VFB} = 3V, $V_{COMMAND}$ = V_{COMP} = 2.5V	0.4			mA
Gain Bandwidth Product	F = 100kHz		5.5		MHz
Current Sense Amplifier					
Gain			16		V/V
Input Resistance			5		kΩ
Common Mode Rejection Ratio	0V < V_{CM} < 4.5V		60		dB
Power Supply Rejection Ratio	10.8V < VIN < 15V		80		dB
Output Sourcing Current	V_{IS-} = 2V, V_{ISOUT} = V_{IS+} = 2.5V	–0.4			mA
Output Sinking Current	V_{IS-} = 3V, V_{ISOUT} = V_{IS+} = 2.5V	0.4			mA
Gain Rolloff	F = 3.5MHz	–3	–2		dB
Current Amplifier					
Input Offset Voltage	V_{CM} = 3V			10	mV
Input Bias Current	V_{CM} = 3V		0.1		µA
Open Loop Gain	1V < V_{CAO} < 2.5V		90		dB
Output Voltage High			3.2		V
Common Mode Rejection Ratio	1.5V < V_{CM} < 4.9V		80		dB
Power Supply Rejection Ratio	10.8V < VIN < 15V		80		dB
Output Sourcing Current	V_{CAM} = 2V, V_{CAO} = V_{COMP} = 2.5V		–0.9		mA
Output Sinking Current	V_{CAM} = 3V, V_{CAO} = V_{COMP} = 2.5V		7.2		mA
Gain Bandwidth Product	F = 100kHz		5.5		MHz
Oscillator					
Initial Accuracy	T_A = 25°C	270	300	330	kHz
	0°C < T_A < 70°C	250	300	350	kHz
Valley to Peak Voltage			1.83		V
Frequency Change With Voltage	10.8V < VIN < 15V		1		%
Output Section (GATEHI and GATELO)					
Maximum Duty Cycle		90	95	99	%

ELECTRICAL CHARACTERISTICS (cont.): Unless otherwise specified, VIN = VDRVHI = VDRVLO = VSNS, V_{D0} = V_{D1} = V_{D2} = V_{D3} = V_{D4} = 0V, R_T = 13k, C_T = 1.8nF, EN = Open, 0°C < T_A < 70°C, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Section (GATELO and GATEHI) (cont.)					
Output Low Voltage	I_{GATE} = –100mA		0.2		V
Output High Voltage	I_{GATE} = 100mA		11.8		V
Rise Time	C_{GATE} = 3.3nF		20	80	ns
Fall Time	C_{GATE} = 3.3nF		15	80	ns
Turn On Delay					
GATEHI Turn Off to GATELO Turn On			60		ns
GATELO Turn Off to GATEHI Turn On			100		ns
Foldback Current Limit					
Clamp Level	$V_{COMMAND}$ = V_{SNS} V_{FB} = $V_{COMMAND}$ – 100mV (Note 3)		1.28		V
	V_{SNS} = 0 V_{FB} = $V_{COMMAND}$ – 100mV (Note 3)		0.64		V

Note 1: This test measures the combined errors of the COMMAND voltage and the voltage amplifier offset voltage. Applies to all DAC codes from 1.8V to 3.5V.

Note 2: This percentage is measured with respect to the ideal COMMAND voltage programmed by the D0 - D4 pins. Applies to all DAC codes from 1.8V to 3.5V.

Note 3: This voltage is measured with respect to the COMMAND voltage. Applies to all DAC codes from 1.8V to 3.5V.

PIN DESCRIPTIONS

CAM: This pin is the inverting input to the current amplifier. The average load current feedback from the ISOUT pin is applied through a resistor to this pin. The current loop compensation network is also connected to this pin (see CAO below).

CAO: This pin is the current amplifier output. The current loop compensation network is connected between this pin and the CAM pin. The voltage on this pin is the input to the PWM comparator and regulates the output voltage of the system. The voltage at this output ranges from below 0.5V (forcing 0% duty cycle) to above 2.5V forcing maximum duty cycle. A 3V clamp circuit prevents the CAO voltage from rising excessively past the oscillator peak voltage, for excellent transient response.

COMP: This pin is the voltage error amplifier output voltage. The system voltage compensation network is applied between COMP and VFB. A 1.28V clamp above COMMAND is used to force the power supply into current limit mode when the output is short circuited. See the Applications Section for programming current limit.

COMMAND: This pin is the output of the 5-bit digital-to-analog (DAC) converter and is the non-inverting input of the voltage error amplifier. The voltage on this pin sets the switching regulator output voltage. The COMMAND voltage is set by the DAC input pins D0-D4. The COMMAND source impedance is typically 1.2kΩ and must therefore drive only high impedance inputs if accuracy is to be maintained. Bypass COMMAND with a 0.01µF, low ESR, low ESL capacitor for best circuit noise immunity.

CT: This pin is used with RT to program the internal PWM oscillator frequency. Use a high quality capacitor for best oscillator accuracy. See the Applications Section for programming the oscillator.

D0-D4: These are the digital input control codes for the DAC. The DAC is comprised of two ranges set by D4 and with D0 representing the least significant bit (LSB) and D3, the most significant bit (MSB). A bit is set low by being connected to GND; a bit is set high by floating it, or connecting it to a 5V source. Each control pin is pulled up to approximately 5V by an internal pull up.

EN: This input is used to disable the GATEHI and GATELO outputs, resulting in disabling the power supply. Pulling EN to GND causes the GATEHI and GATELO outputs to be held low, while floating the pin or pulling it up to 5V ensures normal operation. EN is pulled up to 5V internally.

GATEHI: This output provides a low impedance totem pole driver to drive the high-side external MOSFET. A series resistor between this pin and the gate of the external MOSFET is recommended to prevent gate drive ringing and overshoot. Good layout techniques should be used to prevent GATEHI from ringing more than 0.3V below PGND. The VDRVHI pin provides the power for the GATEHI pin. GATEHI is disabled during UVLO and overvoltage conditions. GATEHI is also disabled when the

PIN DESCRIPTIONS (cont.)

COMMAND voltage is programmed between 1.3 and 1.75V or when the D0-D4 pins are all logic high levels, indicating no processor is present.

GATELO: This output provides a low impedance totem pole driver to drive the low-side synchronous external MOSFET. A series resistor between this pin and the gate of the external MOSFET is recommended to prevent gate drive ringing and overshoot. Good layout techniques should be used to prevent GATELO from ringing more than 0.3V below PGND. The VDRVLO pin provides the power for GATELO. GATELO is disabled during UVLO conditions. GATELO is also disabled when the COMMAND voltage is programmed between 1.3 and 1.75V or when the D0-D4 pins are all logic high levels, indicating no processor is present.

GND: Ground reference for the device. All voltages, with the exception of the GATE voltages, are measured with respect to GND. Bypass capacitors on VIN, VREF, VSNS and COMMAND should be connected directly to the ground plane near GND.

IS-: This pin is the inverting input to the current sense amplifier and is connected to the low side of the average current sense resistor.

IS+: This pin is the non-inverting input to the current sense amplifier and is connected to the high side of the average current sense resistor.

ISOUT: This pin is the output of the current sense amplifier. The voltage on this pin is equal to the voltage across the sense resistor multiplied by 16 and biased up by the COMMAND voltage. This voltage is used for Average Current mode control and for current limiting.

PGND: This pin provides a dedicated ground for the output gate drivers. The GND and PGND pins should be connected externally using a short PC board trace or plane. Decouple VDRVHI and VDRVLO to PGND with low ESR capacitor of at least 0.1µF.

PWRGD: This pin is an open drain output which is driven low to reset the microprocessor when VSNS rises above or falls below its nominal value by 7.5%. The on resistance of the open-drain switch will be no higher than 470Ω. This output should be pulled up to a logic level voltage and should be programmed to sink 1mA or less.

RT: This pin is used with CT to program the internal PWM oscillator frequency. It is also used to program the delay times between the external MOSFET turn on and turn off periods, which eliminates cross conduction in those MOSFETs. See the Applications Section for programming the oscillator and for controlling cross conduction.

VDRVHI: This pin supplies power to the high side output driver, GATEHI. Connect VDRVHI to an 18V source for power supplies converting 12VDC to lower voltages, and to a 12V source for systems for power supplies converting 5VDC. This pin should be bypassed directly to PGND using a low ESR capacitor.

VDRVLO: This pin supplies power to the low side output driver, GATELO. VDRVLO is typically connected to a 12V source, but may be connected to a 5V source for driving logic level MOSFETs. This pin should be bypassed directly to PGND using a low ESR capacitor.

VIN: This pin supplies power to the chip. Connect VIN to a stable voltage source that is at least 10.8V above GND. The GATEHI, GATELO and PWRGD outputs will be held low until VCC exceeds the upper undervoltage lockout threshold. This pin should be bypassed directly to GND.

VFB: This pin is the inverting input to the error amplifier. This input is connected to COMP through a feedback network and to the power supply output through a resistor or a divider network.

VREF: This pin provides an accurate 5V reference and is internally short circuit current limited. VREF powers the D/A Converter and also provides a threshold voltage for the UVLO comparator. For best reference stability, bypass VREF directly to GND with a low ESR, low ESL capacitor of at least 0.01µF.

VSNS: This pin is connected to the system output voltage through a low pass R-C filter. When the voltage on VSNS rises above or falls below the COMMAND voltage by 7.5%, the PWRGD output is driven low to reset the microprocessor. When the voltage on VSNS rises above the COMMAND voltage by 25%, the OVP comparator disables the GATEHI output and enables the GATELO output, forcing 0% duty cycle on the power supply. This pin is also used by the foldback current limiting circuitry to indicate when the output voltage has been short circuited. VSNS should be decoupled very closely to the IC with a capacitor to GND. The OV and UV comparators' hysteresis is typically 20mV, requiring good layout and filtering techniques to insure that noise and ground-bounce do not inadvertently trip the OV and UV comparators. It is recommended that an R-C filter set to approximately Fs/10 be used to filter noise from the system output, where Fs is the oscillator frequency.

APPLICATION INFORMATION

This IC is intended to be used in a high performance power supply to power the Klamath or a similar processor. Figure 1 shows a typical application circuit of Klamath power supply which converts +5V to lower Klamath specific voltages.

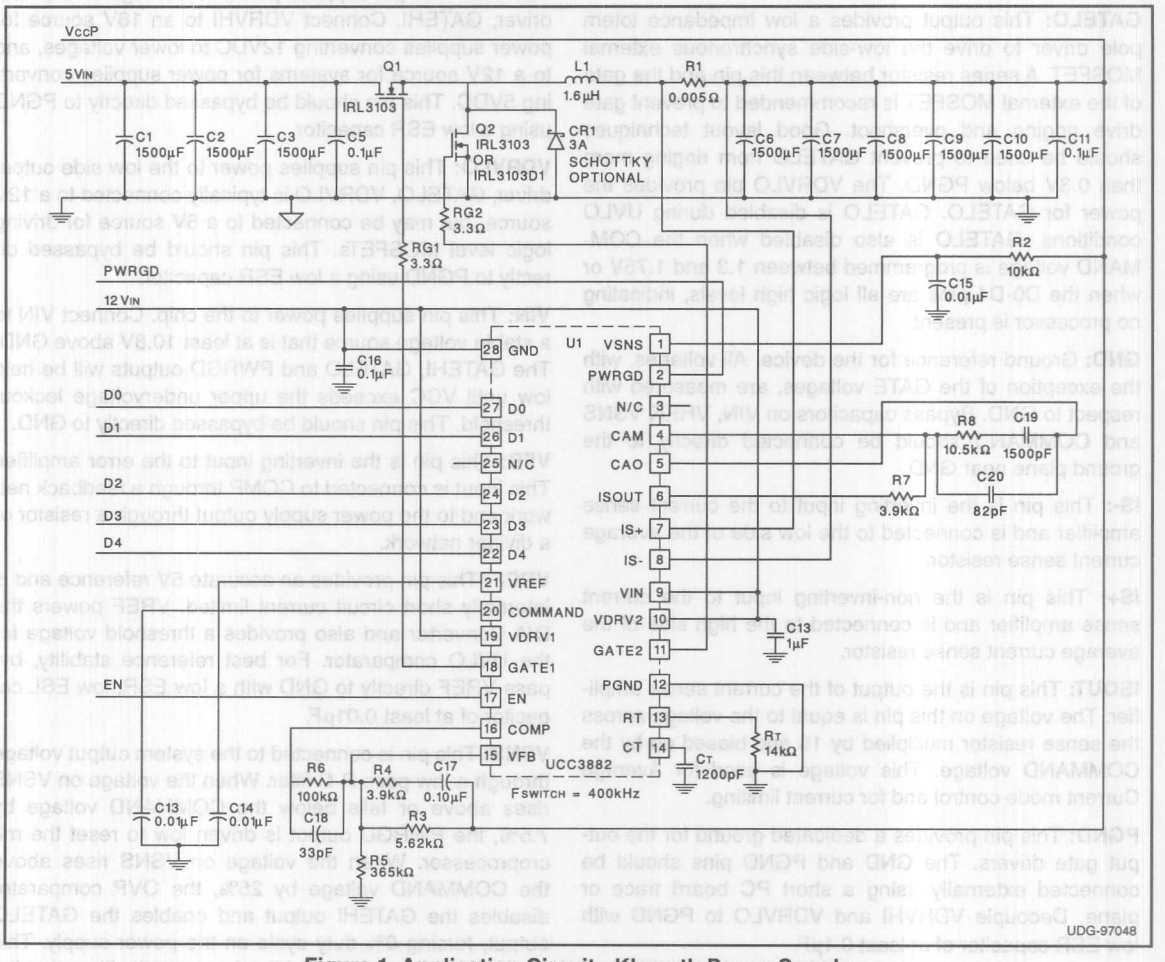


Figure 1. Application Circuit - Klamath Power Supply

Synchronous Switching Delay Time

Figure 2 shows that the fundamental difference between a Buck and a Synchronous Buck regulator is the use of a MOSFET rather than a Schottky diode as the low side or free-wheeling switch.

In order to maintain safe and efficient operation of a Synchronous Buck regulator, both MOSFETs, Q1 and Q2, should never be turned on at the same time. Having both MOSFETs on at the same time results in cross conduction, which can result in excessively high power dissipation in one or both MOSFETs. The UCC3882 has a built in delay between the turn OFF of one MOSFET and the turn ON of the other MOSFET. This delay is a controlled delay between the GATEHI and GATELO drive outputs and is programmable by the selection of the resistor R_T. Controlling the delay between the gate drive outputs is only part of the solution. The power supply designer must also understand intrinsic delays involving MOSFET turn on, turn off, rise and fall times in order to insure that there is no cross conduction.

It is recommended that a value between 12.1kΩ and 15kΩ be used for R_T, which minimizes the delay and can result in the highest efficiency operation. A higher value of R_T will result in a larger delay between the MOSFET

APPLICATION INFORMATION (cont.)

Gate transitions. RT should be between 12.1kΩ minimum and 50kΩ maximum.

Programming the Oscillator

The first step in programming the oscillator is choosing the value of RT as described above. The second step is

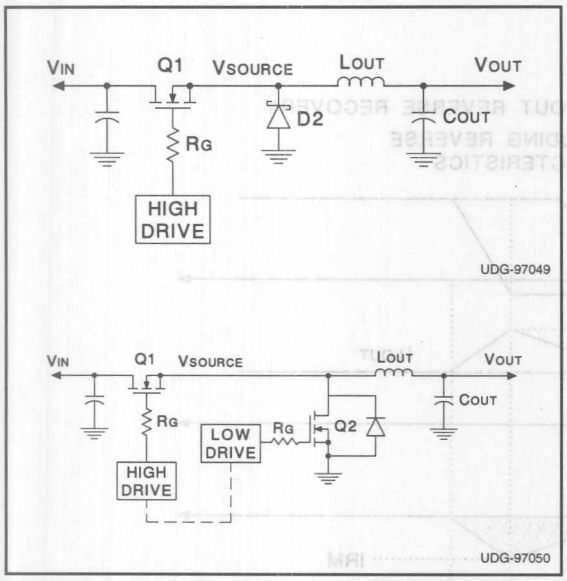


Figure 2. Buck vs. Synchronous Buck Regulator

to program the frequency according to the curves shown in Figure 3, by choosing the appropriate capacitor value.

For convenience, values are shown in Table 1 for nominal frequencies from 100kHz to 700kHz using standards resistors and capacitor values.

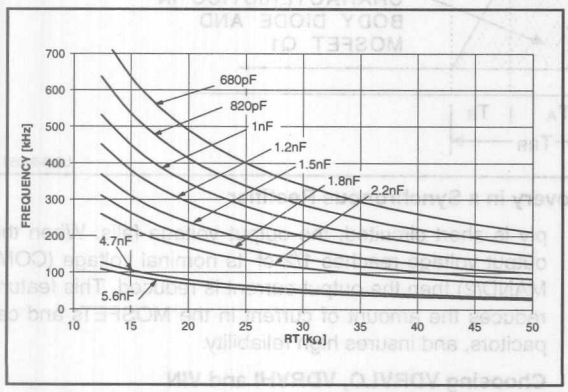


Figure 3. Programming UCC3882 Oscillator Frequency

FREQUENCY (kHz)	RT (kΩ)	CT (pF)
100	13.3	5600
200	13.3	2700
300	13.0	1800
400	14.3	1200
500	13.3	1000
600	13.3	820
700	13.7	680

Table 1. Programming Standard Frequencies

An excessively long delay time between gate drive signals, or a delay time that is too small, will result in a inefficient power supply design. The third step in programming the oscillator is to observe the actual circuit waveforms to insure that the delay is optimal. The designer should vary RT and CT accordingly to adjust the delay time and to program the proper oscillator frequency.

Using an External Schottky Diode in Parallel With the Low Side MOSFET

The purpose of using a synchronous buck regulator is to substitute a low voltage drop MOSFET in place of a Schottky diode as the low side switch. An external Schottky diode may still be required however, in order to reduce the losses due to the reverse recovery of the low-side MOSFET body diode. Figure 4 illustrates the effects on power losses due to the non-ideal nature of a typical MOSFET body diode. IRM is the peak recovery current of the body diode of Q2 and ILOUT is the current of the output inductor. Using a parallel Schottky diode, as shown in the application circuit of Figure 1, can greatly reduce these losses and increase circuit efficiency. The size of the diode should be increased as a function of load current, input voltage, and operating frequency. The diode should be as close to the lower MOSFET, Q2, as possible, to reduce stray inductance.

Choosing RSENSE to Set the Current Limit

RSENSE is chosen to limit the maximum (short circuit) current of the power supply. The short circuit current equation for the UCC3882 is:

$$I_{SC} = \frac{1.28V}{R_{SENSE} \bullet 16}$$

and therefore, the value of the sense resistor, for a chosen short circuit current is:

$$R_{SENSE} = \frac{1.28V}{I_{SC} \bullet 16}$$

The short circuit current limit does vary slightly as a function of the switching regulator's output inductor value and

APPLICATION INFORMATION (cont.)

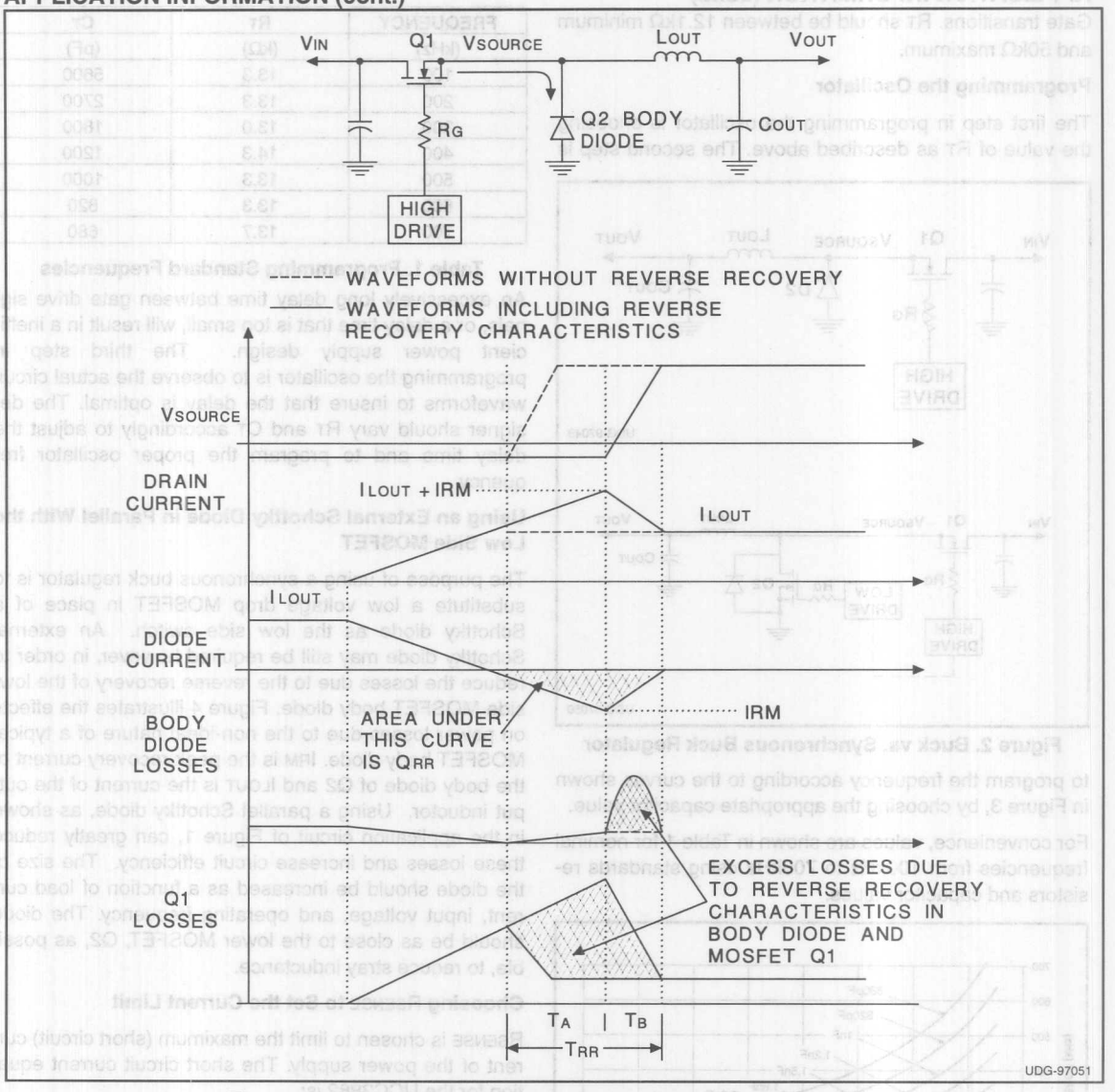


Figure 4. Effects of Reverse Recovery in a Synchronous Rectifier

operating frequency because a high value of ripple current will reduce the average short circuit current limit. Figure 5 shows the variation in Isc given common values for the UCC3882. The UCC3882 is nominally configured so that a 0.005mΩ resistor will set the current limit to approximately 15A.

The UCC3882 incorporates short circuit current foldback, as shown in Figure 6. When the output of the power supply is short circuited, the output voltage falls. When the output voltage reaches 1/2 of its nominal voltage (COMMAND/2) then the output current is reduced. This feature reduces the amount of current in the MOSFETs and capacitors, and insures high reliability.

Choosing VDRVLO, VDRVHI and VIN

The UCC3882 requires a nominal 12V input supplied at VIN. VDRVLO and VDRVHI can be set to any voltage

APPLICATION INFORMATION (cont.)

less than 20V, and may be set individually. A power supply deriving its power from +5V should use +12V at the VDRVHI pin, but may use either +5V or +12V depending on the drive requirements of the synchronous low-side MOSFET. A power supply deriving its power from +12V should use +18V at VDRVHI in order to provide adequate voltage (6V) gate drive to the high-side MOSFET. VIN must be less than +15V.

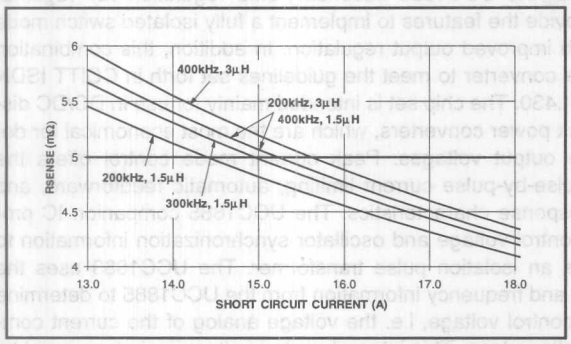


Figure 5. Short Circuit Current Limit vs. RSENSE for Various Frequency and Inductor Values

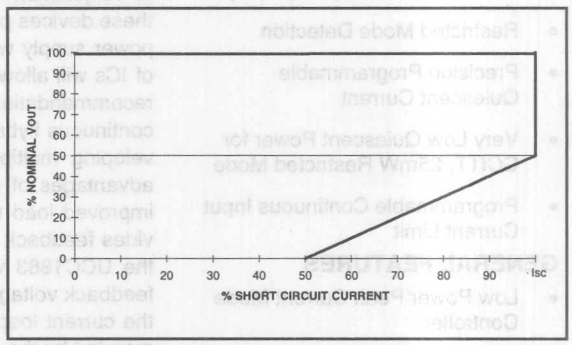


Figure 6. Short Circuit Foldback Reduces Stress on Circuit Components by Reducing Short Circuit Current

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Micropower Peak Current Mode Controller

ISDN I.430 RELATED FEATURES

- Zero-Power Startup Capability
- Restricted Mode Detection
- Precision Programmable Quiescent Current
- Very Low Quiescent Power for CCITT, 25mW Restricted Mode
- Programmable Continuous Input Current Limit

GENERAL FEATURES

- Low Power Peak Current Mode Controller
- Oscillator Synchronizes to Secondary Side Clock
- Leading Edge Blanking of Current Sense Waveform
- 50% Maximum Duty Cycle
- Undervoltage Lockout with Hysteresis
- 5V V_{DD} Logic Supply Regulator
- Programmable Low Line Sensing

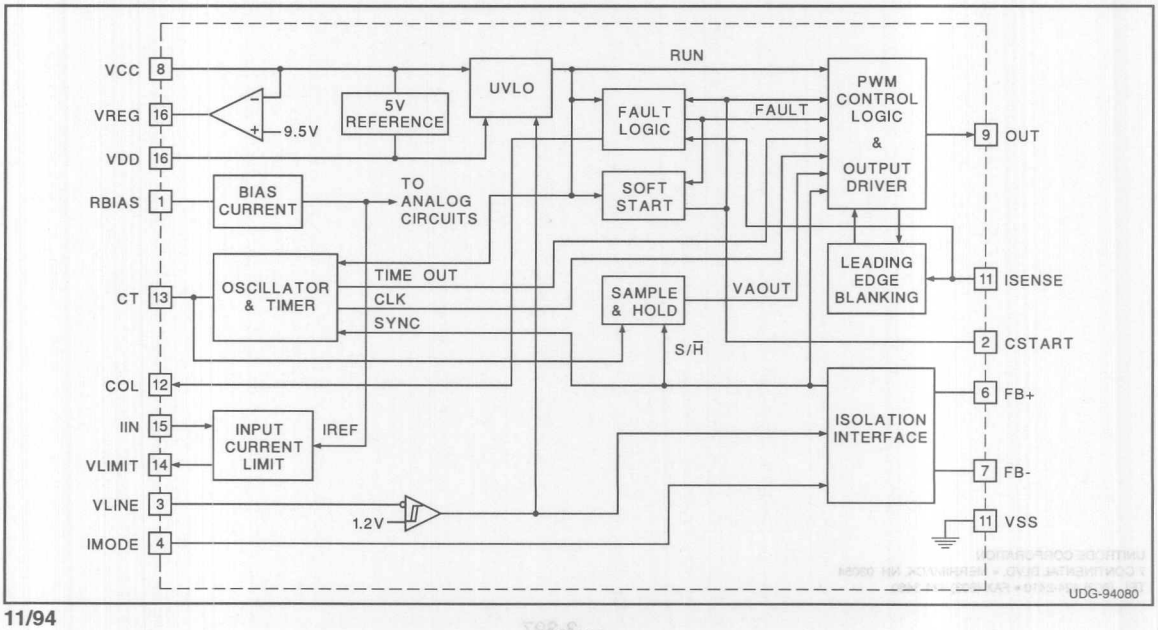
DESCRIPTION

The UCC1883 is a peak current mode PWM controller designed to operate in conjunction with the UCC1885 secondary-side regulation IC. Together these devices provide the features to implement a fully isolated switch mode power supply with improved output regulation. In addition, this combination of ICs will allow a converter to meet the guidelines set forth in CCITT ISDN recommendation I.430. The chip set is intended mainly for use in DC/DC discontinuous flyback power converters, which are the most economical for developing multiple output voltages. Peak current mode control offers the advantages of pulse-by-pulse current limiting, automatic feedforward, and improved load response characteristics. The UCC1885 companion IC provides feedback control voltage and oscillator synchronization information to the UCC1883 via an isolation pulse transformer. The UCC1883 uses the feedback voltage and frequency information from the UCC1885 to determine the current loop control voltage, i.e. the voltage analog of the current commanded by the voltage loop. This internal control voltage is, in turn, used by the UCC1883 in a conventional peak current mode PWM circuit. Internal leading edge blanking of the current sense waveform eliminates the need for an external filtering network on the ISENSE input. When in restricted mode or lightly loaded, the UCC1883 operates with a minimum pulse width determined by the leading edge blanking circuit. This eliminates the spurious EMI generated if arbitrarily short output pulses are produced by the PWM.

In addition to pulse-by-pulse current limiting, an overcurrent threshold is maintained. A fault condition may also be triggered by repeated peak current limit conditions, through the use of the programmable output overload detector. If either of these faults is detected, OUT is immediately disabled, and a programmable restart period occurs before a soft start sequence is initiated.

BLOCK DIAGRAM

continued



ABSOLUTE MAXIMUM RATINGS

Supply Voltage (VCC) 16.5
Maximum VCC Slew Rate 10V/ms
Maximum Voltage:
RBIAS, CSTART, VLINE
IMODE, FB+, FB-, OUT, VREG ..... VCC + 0.3V to 18V
VDD 7V
COL, ISENSE, CT ..... VDD + 0.3V to 7V
VLIMIT, IIN 0.3V
Minimum Voltage:
VLIMIT ..... –VCC
All Other Pins ..... –0.3V
Maximum DC Current, Any Pin, Source or Sink 100mA
Maximum Peak Current, Any Pin, Source or Sink 500mA
Storage Temperature ..... –65°C to+150°C
Junction Temperature ..... –55°C to+150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

Note 1: All voltages expressed with respect to VSS, currents are positive into the specified terminal.

Note 2: All maximum signal pin voltage limits apply for cases of zero source impedance. Higher or lower voltages may be impressed through a finite source impedance which causes the input current to be limited to the values specified with total package power dissipation at or below specified limits.

Note 3: Consult Packaging Section of Databook for thermal limitations and considerations of package.

DESCRIPTION (cont.)

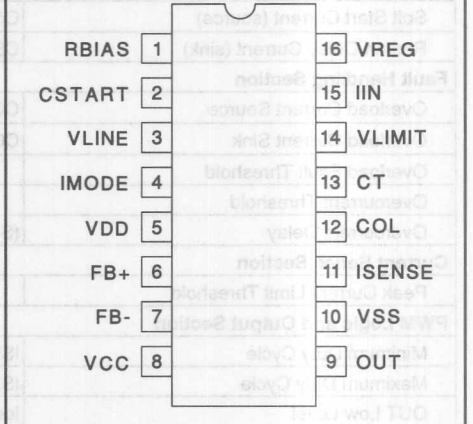
ISDN-specific features allow the UCC1883/UCC1885 combination to be compatible with CITT Recommendation I.430. The linear pre-regulator is intended to control a depletion-mode NMOS pass transistor, such as BSS129. Startup power drawn from the line can be reduced to zero if a bootstrap winding provides power to the UCC1883 VCC pin. An internal current comparator is provided to sense restricted mode directly from the input to the converter. Maximum input current may be accurately programmed and continuously limited with the use of an external PMOS pass transistor. Precision programming of the quiescent current used by the UCC1883 allows the system to meet the 25mW restricted mode power limit, or the current can be set to achieve higher operating frequencies at the cost of increased power consumption.

The UCC1883 is fabricated in Unitrode's 3µM BiCMOS process. Even though the device contains internal clamping diodes on all pins, the part should still be considered static sensitive. Normal ESD handling procedures for CMOS devices should be observed when using the UCC1883.

Pin No.	Pin Name	Pin Type	Function
1	RBIAS	Analog Program	Quiescent Bias Current Set
2	CSTART	Analog Program	Soft Start and Restart Delay Timing Set
3	VLINE	Analog Input	Input Line Voltage Sense
4	IMODE	Analog Input	Input Line Polarity Sense
5	VDD	Analog Output	5V Logic Regulator
6	FB+	Digital I/O	Differential Feedback Communication Signal (+)
7	FB-	Digital I/O	Differential Feedback Communication Signal (-)
8	VCC	Power Supply	Positive Power Supply Input
9	OUT	Digital Output	Power Switch Control Voltage
10	VSS	Power Supply	UCC1883 Ground Reference
11	ISENSE	Analog Input	Primary Current Sense
12	COL	Analog Program	Output Overload Timing Set
13	CT	Analog Program	Oscillator Frequency Set
14	VLIMIT	Analog Output	Input Current Limit Control Voltage
15	IIN	Analog Program	Input Current Limit Set
16	VREG	Analog Output	9.5V Pre-regulator Control Voltage

CONNECTION DIAGRAM

DIL-16
(Top View)
J or N Package



ELECTRICAL CHARACTERISTICS Unless otherwise noted, all specifications apply for T_A = 0°C to 70°C for the UCC3883, T_A = –40°C to +85°C for the UCC2883, –55°C to +125°C for the UCC1883, VCC = 12V , VDD = 5V , RBIAS = 200kΩ, CT = 100pF, T_A=T_J.

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
UVLO Section					
VCC Start Threshold		8.0	9.0	10.5	V
VCC Threshold Hysteresis		1.5	2	2.5	V
Linear Pre-Regulator Section					
Regulated VCC Voltage	(See Note 4)	8.5	9.5	10.5	V
Regulated Vcc to UVLO Delta		0	500	800	mV
VCC Override Threshold				11	V
User Bias Section					
RBIAS Voltage	T_J = +25°C	1.17	1.2	1.23	V
RBIAS Voltage Line Regulation	10.0V < VCC < 13.5V		8	16	mV
Total RBIAS Voltage Variation	Initial + Line + Temperature	1.15		1.25	V
Input Current Limit Section					
IIN Offset Voltage	VLIMIT = –3V	–20		20	mV
Output Reference Current	T_J = 25°C, IIN = 0V	1.6	1.9	2.1	µA
I_{REF} Line Regulation	10.0V < VCC < 13.5V		10	50	nA
Total I_{REF} Variation	Initial + Line + Temperature	1.5		2.2	µA
VLIMIT Low Level	IIN = 0.2V, |OUT| < 10nA	-10.5	–9		V
VLIMIT High Level	IIN = 0.2V, |OUT| < 10nA		0.6	1.0	V
VLIMIT Output Current	IIN = –0.2V, VLIMIT = –3V	3	6	14	mA
Oscillator Section					
Initial Accuracy	T_J = 25°C	30	35	40	kHz
Voltage Stability	10.0V < VCC < 13.5V		1	3	%
Total Oscillator Variation	Initial + Line + Temperature	29.5		41.5	kHz
CT Ramp Amplitude		2.35	2.5	2.65	V
Soft Start Section					
Soft Start Current (source)	CSTART = 2.5V	17	30	43	µA
Restart Delay Current (sink)	CSTART = 2.5V	0.5	1	2	mA
Fault Handling Section					
Overload Current Source	COL = 0.5V	1.4	2.3	3.0	µA
Overload Current Sink	COL = 0.5V	1.4	2.2	3.0	µA
Overload Fault Threshold		1.4	1.5	1.6	V
Overcurrent Threshold		1.4	1.5	1.6	V
Overcurrent Delay	(See Figure 1) (Note 6)		100	200	ns
Current Sense Section					
Peak Current Limit Threshold		1.1	1.2	1.3	V
PWM Logic and Output Section					
Minimum Duty Cycle	ISENSE = 0V			0	%
Maximum Duty Cycle	ISENSE = 1.3V	49	50	50	%
OUT Low Level	I_{OUT} = 10mA		0.05	0.15	V
	I_{OUT} = 100mA		0.5	1.5	V
OUT High Level	I_{OUT} = –10mA	11.85	11.95		V
	I_{OUT} = –100mA	10.5	11.5		V
OUT Rise Time	T_J = 25°C,C_{LOAD} = 1nF (See Figure 2)		25	75	ns
OUT Fall Time	T_J = 25°C,C_{LOAD} = 1nF (See Figure 2)		25	75	ns

ELECTRICAL CHARACTERISTICS Unless otherwise noted, all specifications apply for T_A = 0°C to 70°C for the UCC3883, T_A = –40°C to +85°C for the UCC2883, –55°C to +125°C for the UCC1883, VCC = 12V , VDD = 5V , RBIAS = 200kΩ, CT = 100pF, T_A=T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Isolation Interface Section					
FB Input High Voltage	FB = V(FB+)-V(FB-), 0 ≤ FB ≤ VDD		1.3	2.1	V
FB Input Low Voltage	FB = V(FB+)-V(FB-), 0 ≤ FB ≤ VDD	–2.1	–1.3		V
FB Input Pulse Width	(See Figure 3) (Note 6)	80	300		ns
FB Output Width	(See Figure 3) (Note 6)		75		ns
LOLINE Status Threshold		1.0	1.2	1.3	V
RSMODE Status Threshold		0.5	2	4	µA
VDD Regulator					
VDD Output	No External Load	4.6	5	5.4	V
VDD Line Regulation	1.0V < VCC < 13.5V		10	30	mV
VDD Load Regulation	–3mA < I_{OUT} < 0mA		100	300	mV
VDD Short Circuit Current Limit	VDD = 0V	7	50	80	mA
Power Supply					
DC Supply Current			200	275	µA
CDD			150		pF

Note 4: BSS129 (or equivalent) External Pass Element, 1µF Ceramic Bypass; See Figure 6.
Note 5: Operating in conjunction with UCCx885 using equal valued RBIAS.
Note 6: Guaranteed by design. Not 100% tested in production.

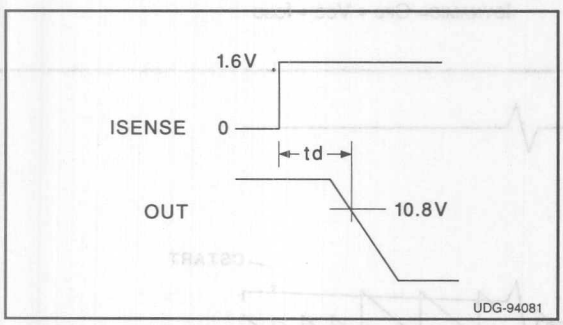


Figure 1. Overcurrent Fault Timing

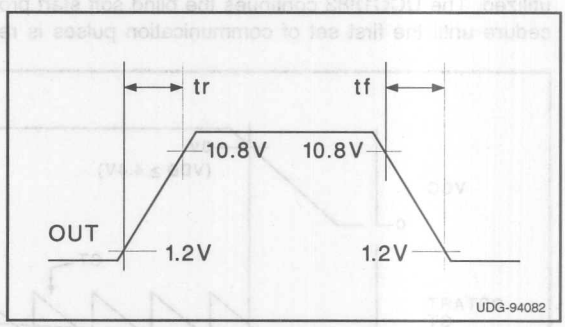


Figure 2. Output Rise & Fall Time

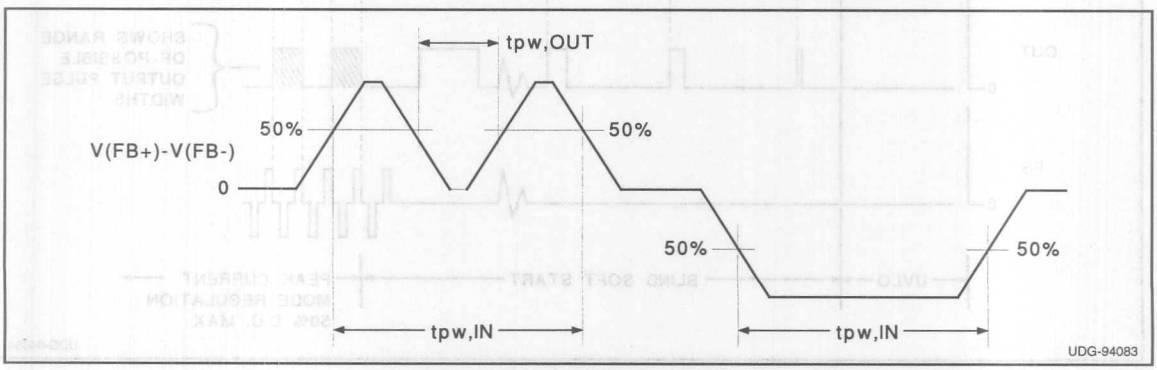


Figure 3. Isolation Interface Timing

APPLICATION INFORMATION

UNDERVOLTAGE LOCKOUT AND SOFT START

When power is first applied to the UCC1883, CSTART is held at VSS until VCC exceeds 9.0V and VDD exceeds 4.4V. During this period of UVLO, the following state exists:

1) CSTART is held low,
2) OUT is held low,
3) VREG is forced to VCC until VCC > 4V, and
4) VLIMIT becomes a high impedance output.

Once adequate operating voltages have been established, the input current limit function is enabled. CSTART and OUT are still held low until the voltage on the VLINE pin exceeds 1.2V, indicating ample voltage is stored on the converter's bulk filter capacitor. At that time, CSTART is released and allowed to charge from an internal 25µA current source. The UCC1883 then begins to transfer energy to the secondary side of the converter by pulse width modulating the ramp voltage on CT against the charging voltage on CSTART. During this soft start period, all fault functions, pulse-by-pulse current limiting, and input current limiting are enabled. Note that the dV/dt of CSTART must be strictly less than the dV/dt established on the UCC1885 SOFTREF pin, if secondary-side soft start is utilized. The UCC1883 continues the blind soft start procedure until the first set of communication pulses is received from the secondary side via the isolation interface. At that time, all control of the power switch is effectively transferred to the secondary-side regulation IC. Should communication pulses never be received, or should they be discontinued during operation, blind PWM operation continues with the output pulse width limited by the internal 50% duty cycle clamp or pulse-by-pulse current limit with all fault processing enabled.

USER BIAS PROGRAMMING

The RBIAS pin may be used to set the amount of quiescent current consumed by certain analog circuits within the UCC1883. A resistor from this pin to VSS establishes a reference current according to the equation

$$IBIAS = \frac{1.2V}{RBIAS}$$

Recommended range for RBIAS is 39.2kΩ to 392kΩ. Internal circuits on the UCC1883 consume a total quiescent current of 9 • IBIAS, plus some fixed currents amounting to about 85µA at room temperature. Additional dynamic current consumption may be calculated with C_{PD} (see specifications), given a certain oscillator frequency f_{OSC}, from the equation

$$I_{DYNAMIC} = C_{PD} \bullet V_{CC} \bullet f_{OSC}$$

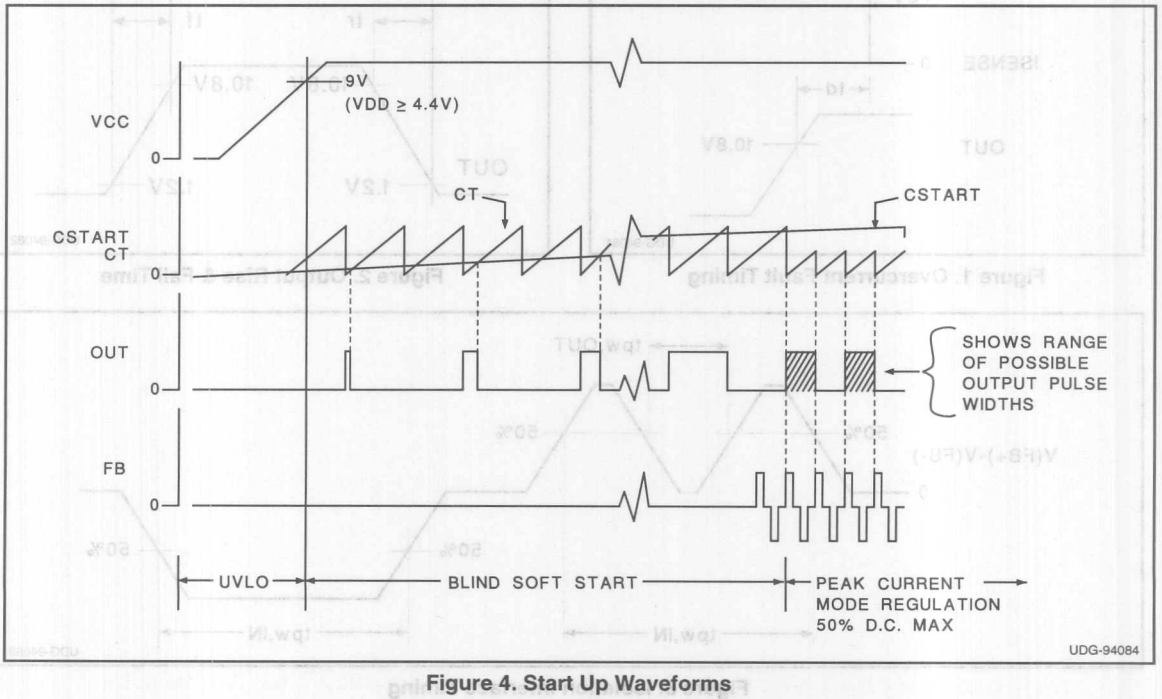


Figure 4. Start Up Waveforms

APPLICATION INFORMATION (cont.)

9.5V LINEAR PRE-REGULATOR

The UCC1883 contains a control amplifier, which when used with a depletion-mode NMOS pass transistor such as the BSS129, can provide a 9.5V linear pre-regulator to supply VCC directly from the input line. The depletion-mode device guarantees the regulator is self-starting. Bypass values less than 3.3µF are recommended when the pre-regulator is utilized. The pre-regulator may subsequently be fully disabled by a tertiary bootstrap winding providing a minimum of 10.6V to the VCC pin. Note that the UCC1883 has 2V of UVLO hysteresis to allow use of more conventional startup circuitry, if the power consumption of such implementations can be tolerated. In these cases, any value of bypass capacitance is acceptable, although a minimum value of 0.01µF is recommended for all configurations.

INPUT CURRENT LIMIT PROGRAMMING

The UCC1883 also incorporates the necessary control amplifier and current reference to implement a continuous input current limit mask conforming to CCITT recommendation I.430. When using this feature, the ratio of RSENSE to RBIAS determines the magnitude of the current passed by an external PMOS transistor. The PMOS device must be able to withstand the maximum input voltage seen by the converter, and its RON will cause some reduction in efficiency during normal operation, due to conduction losses. Referencing the application diagram of Figure 7, the control amplifier programs a peak input current according to the equation

$$ILIMIT = \left(\frac{RP}{RS} + 1\right) \bullet \frac{0.4}{RBIAS}$$

by driving the gate of the external PMOS device until equal voltage is impressed across RP and RS. In addition to the input capacitance of the PMOS pass device, some compensation capacitance from VLIMIT to VSS may be required. However, too much capacitance on VLIMIT will increase the inrush current response time beyond that allowed by recommendation I.430. A total capacitance of between 330pF and 2.2nF is recommended. A shunt bleeder resistor should be added across the PMOS pass transistor to facilitate converter startup. Due to the large values of resistance which will typically be encountered, a 10pF speedup capacitor across RP is suggested to help maintain good phase margin in the control loop. A clamping diode across RS improves transient response by preventing excessive error voltage from being stored on the RP speedup capacitor during VLIMIT slewing. Finally, a 12V zener clamp from VLIMIT to VSS is recommended to protect the gate of the PMOS device from over voltage and to limit the voltage slew which must occur before entering the current limit state. During normal converter operation, when less than the programmed current limit is being drawn from the line, the control loop opens and VLIMIT moves to its maximum negative value, effectively turning the PMOS limit transistor into a series switch.

If a more accurate reference than that supplied by the UCC1883 is desired, a precision resistor may be wired from an appropriate reference voltage to IIN. Since IIN is

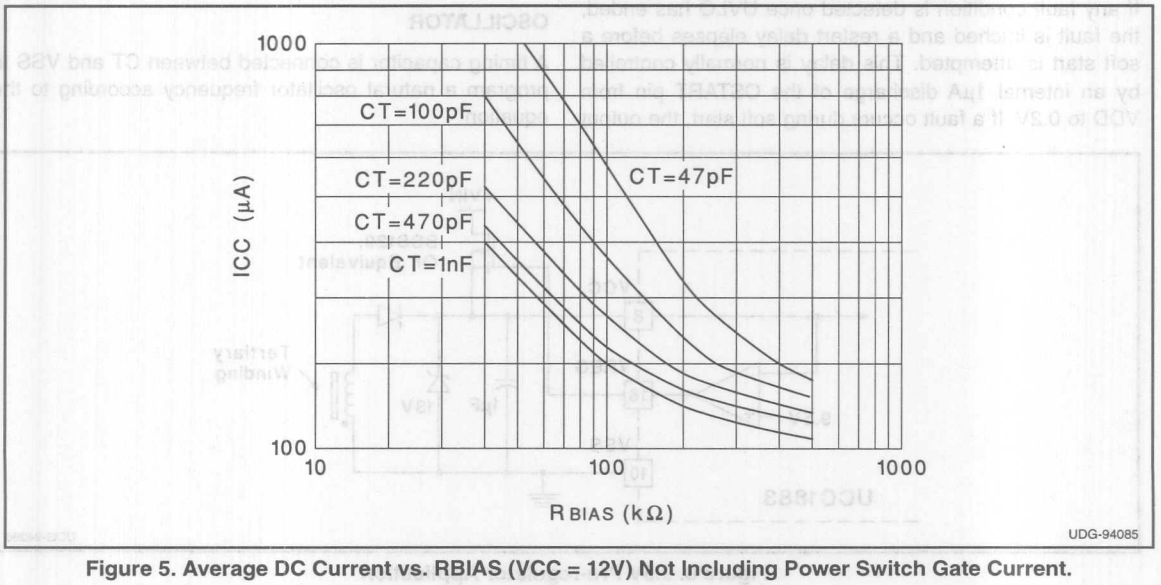


Figure 5. Average DC Current vs. RBIAS (VCC = 12V) Not Including Power Switch Gate Current.

APPLICATION INFORMATION (cont.)

held at VSS (ground) by the current limit control amplifier, the additional current created in this case is equal to the reference voltage divided by the external resistor. A reference of at least 2V is recommended to eliminate errors caused by the input offset voltage of the control amplifier. Because the reference current provided by the UCC1883 sums into the IIN pin a minimum external reference current value of 4V/RBIAS is recommended to minimize errors caused by the initial tolerance of the internal current reference.

FAULT HANDLING

Three fault conditions which immediately disable the output are detected by the UCC1883 housekeeping circuitry. These are:

1) UVLO,
2) 1.5V or higher on the ISENSE pin, and
3) 1.5V or higher on the COL integrator pin.

Unlike the pulse-by-pulse current limit comparator, no leading blanking is applied to the overcurrent fault comparator, which has a nominal 1.5V threshold. A capacitor to VSS may be used on the COL pin to program the output overload fault integrator. The polarity of the 2.2µA current sourced by the internal circuitry driving the COL pin potentially changes on each falling edge of OUT. If the output pulse was terminated as the result of a peak current event, then current is sourced to COL, otherwise current is sunk from COL to VSS. If the voltage on COL ever reaches 1.5V, a fault condition is set.

If any fault condition is detected once UVLO has ended, the fault is latched and a restart delay elapses before a soft start is attempted. This delay is normally controlled by an internal 1µA discharge of the CSTART pin from VDD to 0.2V. If a fault occurs during soft start, the output is immediately disabled, but CSTART is fully charged (4.8V) before a restart delay begins. A fixed restart delay to soft start timing ratio of 25:1 may be obtained with only a capacitor from CSTART to VSS. This ratio may be decreased by adding an external resistor between CSTART and VSS. The value of this resistor should be greater than the value of the current programming resistor on the RBIAS pin.

ISOLATION INTERFACE

In addition to receiving synchronization and duty cycle control information from the secondary side of the converter, the UCC1883 isolation interface also transmits digital status information to the secondary side. This digital information reflects the state of two internal analog comparators which monitor the VLINE and IMODE pins. A voltage of less than 1.2V on VLINE is indicated by a true LOLINE bit, and an input current of less than 2µA into the IMODE pin is interpreted as a true RSMODE (restricted power mode) condition. These digital bits are transmitted across the isolation barrier and appear as outputs on the UCC1885 secondary-side regulation IC. Recall that no UCC1885 output will occur until a voltage greater than 1.2V is initially established on VLINE.

VDD LOGIC SUPPLY

The internal CMOS logic on the UCC1883 runs from a regulated 5V which is available externally at the VDD pin. This pin should be bypassed to VSS with a high quality ceramic capacitor having a value of at least 0.01µF. Values in excess of 10µF are not recommended.

OSCILLATOR

A timing capacitor is connected between CT and VSS to program a natural oscillator frequency according to the equation

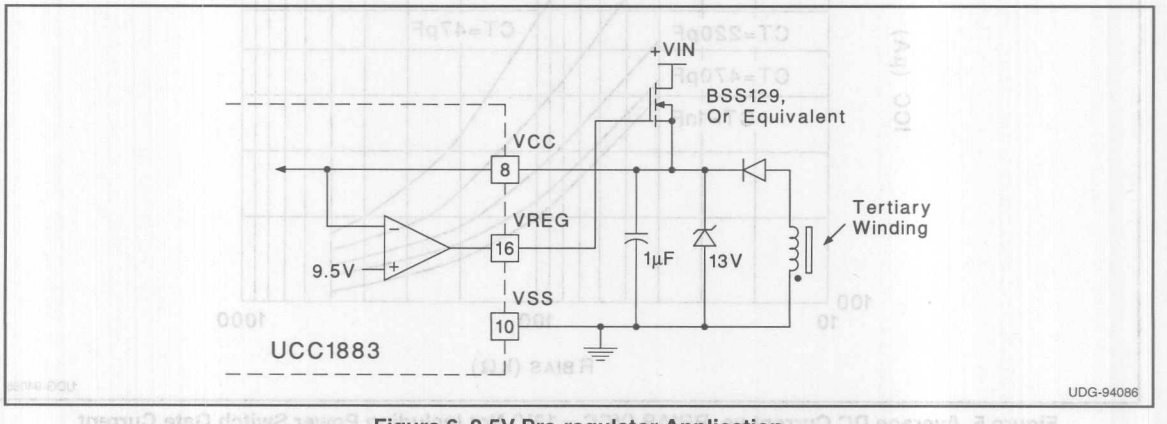


Figure 6. 9.5V Pre-regulator Application

APPLICATION INFORMATION (cont.)

$$fosc = \frac{0.72}{CT \bullet RBIAS}$$

A ramp voltage running from VSS to 2.5V is created on the CT pin. This oscillator is automatically synchronized to the secondary-side clock frequency when data communication occurs across the isolation interface. Proper synchronization will only occur if the frequency of the secondary-side clock exceeds the natural frequency of the UCC1883 oscillator. A new oscillator cycle (ramp returns to VSS) will be initiated on the rising edge of each positive isolation interface input pulse, with a corresponding decrease in ramp amplitude. The UCC1883 is designed so that the dV/dt established on its CT pin will be nominally the same as that of the UCC1885 CT pin, if equivalent components are used on the RBIAS and CT pins of both devices. However, the natural frequency of the UCC1883 oscillator will automatically be lower, to allow synchronization. Proper CT ramp slope is important to the UCC1883, because it uses this information, along with the pulses received over the isolation interface, to reconstruct the analog output of the UCC1885 voltage error amplifier. This reconstructed voltage is in turn used to control the peak current mode PWM. The ratio of the slope of the UCC1883 timing ramp to the UCC1885 timing ramp sets the gain applied by the UCC1883 to the UCC1885 error amplifier output.

Other variations of the UCC1883 implementing voltage mode control, duty cycles greater than 50%, or faster natural oscillator frequencies may be available. Contact the factory for further information.

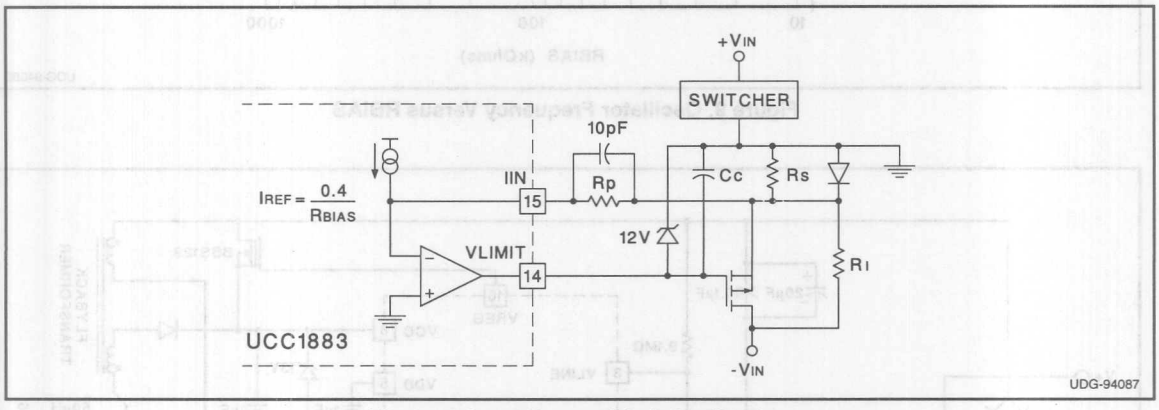


Figure 7. Input Current Limit Application

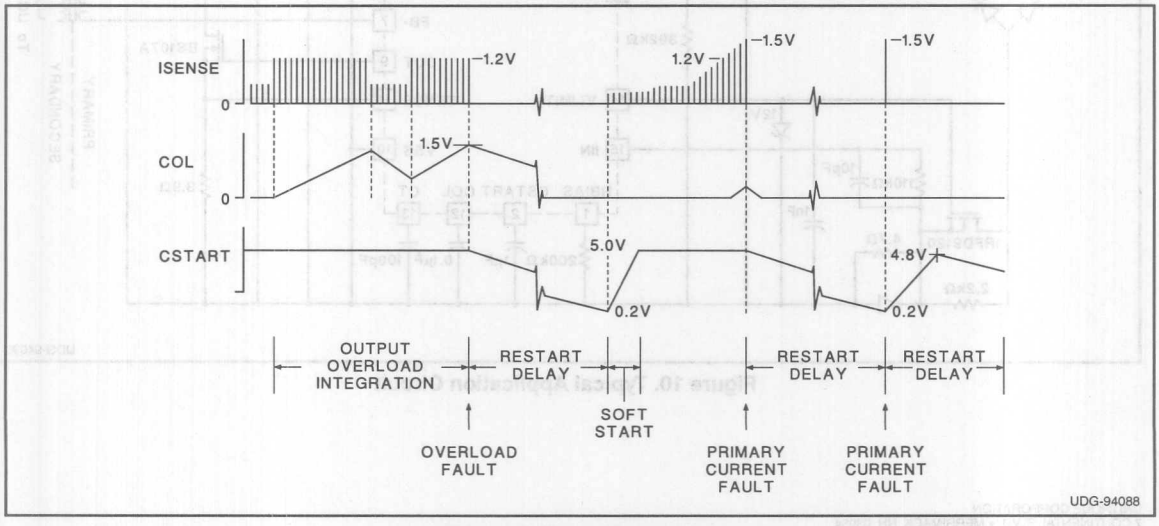


Figure 8. Fault Waveforms

APPLICATION INFORMATION (cont.)

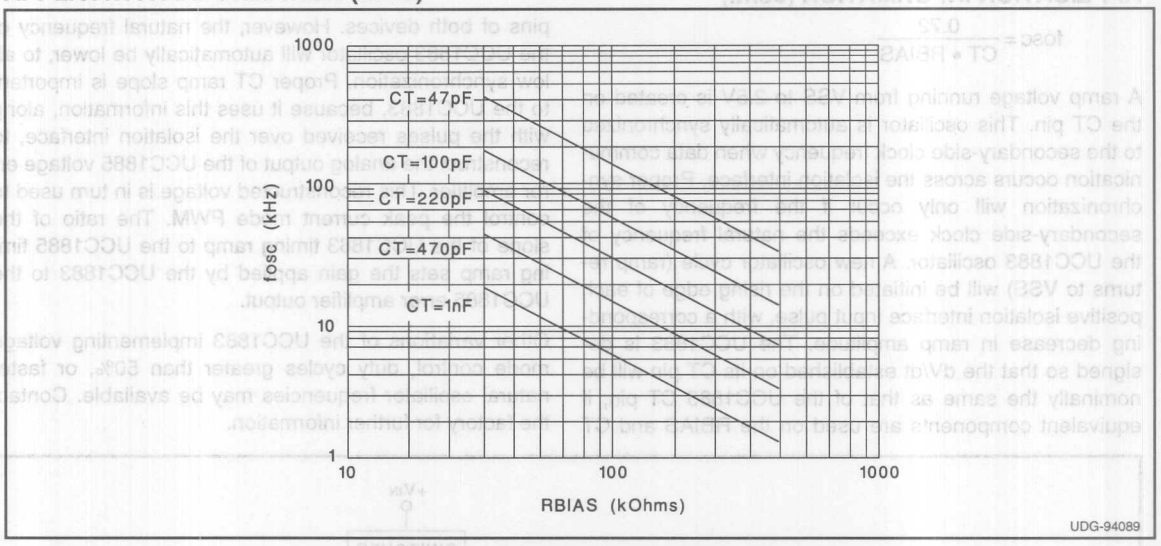


Figure 9. Oscillator Frequency Versus RBIAS

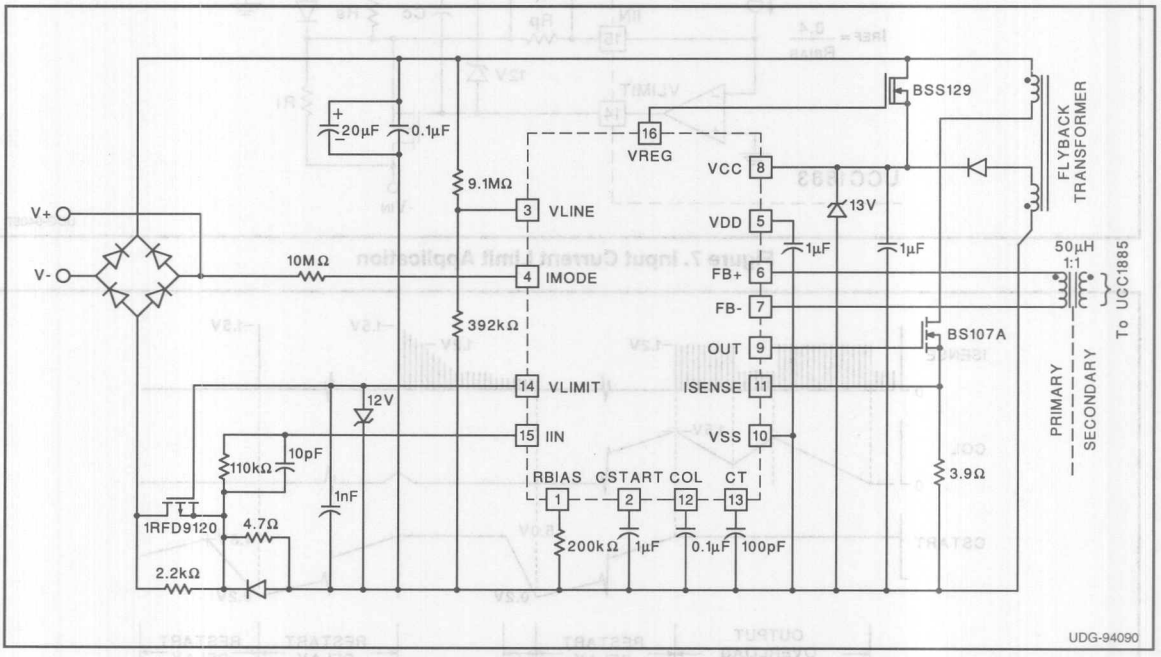


Figure 10. Typical Application Circuit

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Frequency Foldback Current Mode PWM Controller

PRELIMINARY

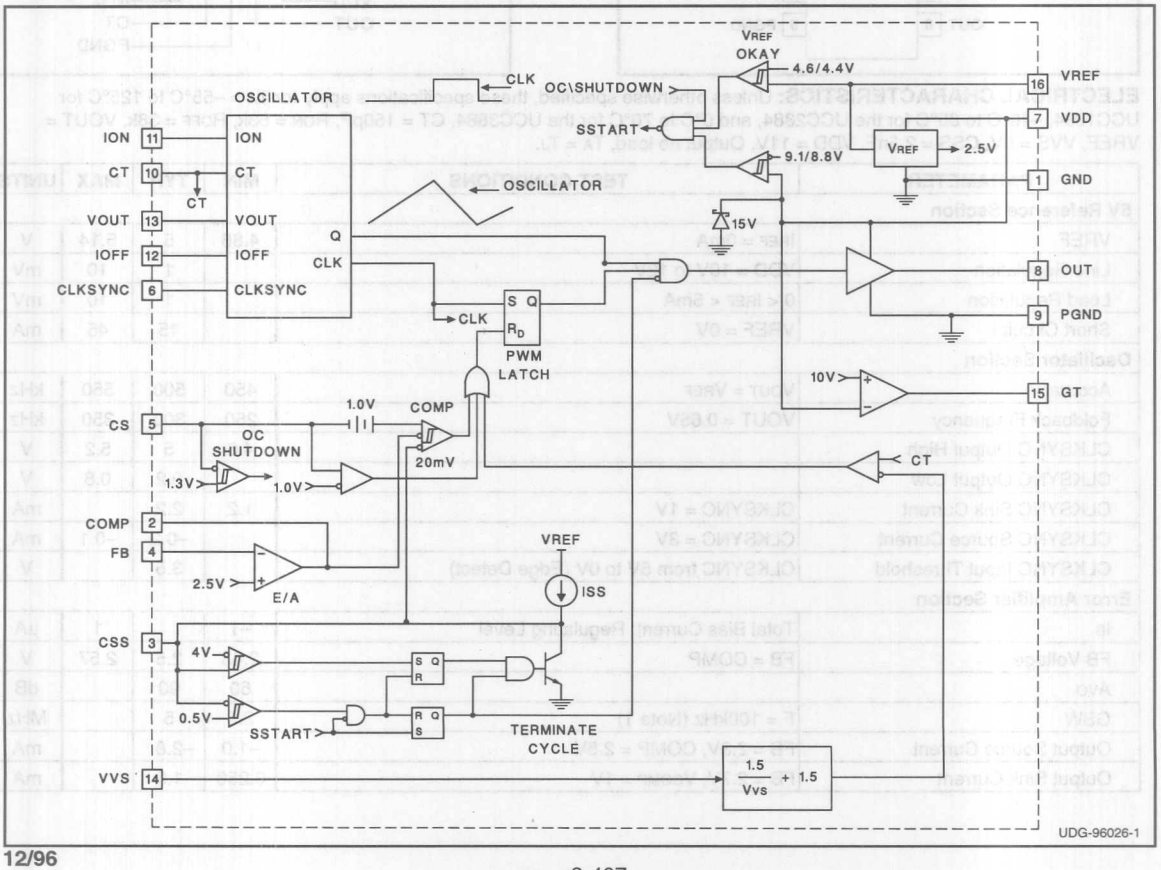
FEATURES

- Frequency Foldback Reduces Operating Frequency Under Fault Conditions
- Accurate Programmable Volt-Second Clamp
- Programmable Maximum Duty Cycle Clamp
- Oscillator Synchronization
- Overcurrent Protection
- Shutdown with Full Soft Start
- Wide Gain Bandwidth Amplifier (GBW > 2.5MHz)
- Current Mode Operation
- Precision 5V Reference

DESCRIPTION

The UCC3884 is a high performance current mode PWM controller intended for single ended switch mode power supplies. The chip implements a frequency foldback scheme that decreases the oscillator frequency as the output voltage falls below a programmed value. This technique decreases the average output current sourced into a low impedance load which can occur during an output short circuit or overload condition. Excessive short circuit current is more prevalent in high frequency converters where the propagation delay and switch turn-off time forces a minimum attainable duty cycle. An accurate volt-second clamp limits the duty cycle during line or load transient conditions which could otherwise saturate the transformer. The volt-second clamp may also be used with an external overvoltage protection circuit to handle fault conditions such as current sense disconnect or current transformer saturation. The frequency foldback, volt-second clamp, cycle-by-cycle current limit, and overcurrent shutdown provide a rich set of protection features for use in peak current mode pulse width modulators.

BLOCK DIAGRAM



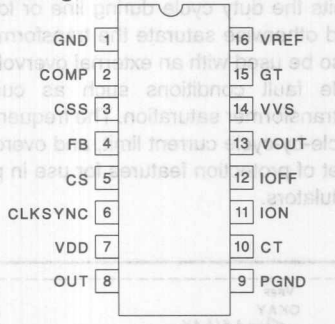
ABSOLUTE MAXIMUM RATINGS

Supply Voltage 15V
Output Sink Current 1A
Output Source Current 0.5A
All Other Pins 6V
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

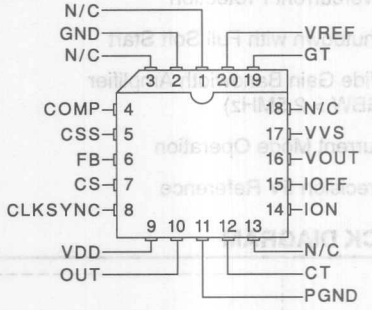
Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAMS

DIL-16, SOIC-16 (Top View)
J, N or D Packages



PLCC-20 (Top View)
Q Package



ELECTRICAL CHARACTERISTICS: Unless otherwise specified, these specifications apply for T_A = –55°C to 125°C for UCC1884, –40°C to 85°C for the UCC2884, and 0°C to 70°C for the UCC3884, CT = 150pF, R_{ON} = 53k, R_{OFF} = 38k, VOUT = VREF, VVS = 0V, CSS = 2.5nF, VDD = 11V, Output no load, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
5V Reference Section					
VREF	I_{REF} = 0mA	4.86	5	5.14	V
Line Regulation	VDD = 10V to 12V		1	10	mV
Load Regulation	0 < I_{REF} < 5mA		1	10	mV
Short Circuit I	VREF = 0V		15	45	mA
Oscillator Section					
Accuracy	V_{OUT} = V_{REF}	450	500	550	kHz
Foldback Frequency	VOUT = 0.65V	250	300	350	kHz
CLKSYNC Output High		4.8	5	5.2	V
CLKSYNC Output Low			0.2	0.8	V
CLKSYNC Sink Current	CLKSYNC = 1V	1.2	2.2		mA
CLKSYNC Source Current	CLKSYNC = 3V		–0.2	–0.1	mA
CLKSYNC Input Threshold	CLKSYNC from 5V to 0V (Edge Detect)		3.5		V
Error Amplifier Section					
I_B	Total Bias Current; Regulating Level	–1		1	µA
FB Voltage	FB = COMP	2.43	2.5	2.57	V
Avo		60	90		dB
GBW	F = 100kHz (Note 1)	2.5	5		MHz
Output Source Current	FB = 2.3V, COMP = 2.5V	–1.0	–2.8		mA
Output Sink Current	FB = 2.7V, V_{COMP} = 1V	0.250	1.5		mA

ELECTRICAL CHARACTERISTICS (cont.): Unless otherwise specified, these specifications apply for T_A = –55°C to 125°C for UCC1884, –40°C to 85°C for the UCC2884, and 0°C to 70°C for the UCC3884, CT = 150pF, R_{ON} = 53k, R_{OFF} = 38k, VOUT = VREF, VVS = 0V, CSS = 2.5nF, VDD = 11V, Output no load, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Error Amplifier Section (cont.)					
V_{OL}	Io = 100µA		0.3	0.8	V
V_{OH}	Io = –100µA	2.7	3.1	3.5	V
PWM Section					
Minimum Duty Cycle	FB = 3V, CS = 0V			0	%
Maximum Duty Cycle	FB = 0V, CS = 0V	77	80	83	%
Current Sense Section					
Input Bias Current (CS)				2	µA
CS Shutdown Threshold		1.235	1.3	1.365	V
CS Shutdown Hysteresis			20		mV
CS Over Current Threshold		0.95	1	1.05	V
Current/Fault Section					
Soft Start Charge Current		–10	–20	–30	µA
Soft Start Discharge Current		10	20	30	µA
V_{OL}			0	50	mV
Soft Start Complete Threshold		3.6	4	4.4	V
Soft Start Restart Threshold		0.4	0.5	0.6	V
Volt Second Clamp					
Duty Cycle	VVS = 1.4V, T_A = –55°C to 125°C	57.6	64	70.4	%
	VVS = 1.4V, T_A = –40°C to 85°C	60.8	64	67.2	%
	VVS = 1.4V, T_A = 0°C to 70°C	62.08	64	65.92	%
	VVS = 3.7V, T_A = –55°C to 125°C	21.6	24	26.4	%
	VVS = 3.7V, T_A = –40°C to 85°C	22.8	24	25.2	%
	VVS = 3.7V, T_A = 0°C to 70°C	23.28	24	24.72	%
I_B	VVS = 3.7V	–1		+1	µA
Output Stage					
Output Low Saturation	I_{OUT} = 100mA		0.5	0.9	V
Output High Saturation	I_{OUT} = –50mA		0.5	0.9	V
	I_{OUT} = –200mA			1.9	V
UVLO Output Low Saturation	I_{OUT} = 20mA, VDD = 0V		0.7	1.2	V
Rise Time	CL = 1nF		50	70	ns
Fall Time	CL = 1nF		30	50	ns
Undervoltage Lockout					
Turn-On Threshold Voltage		8.4	8.9	9.4	V
Hysteresis		200	600		mV
Startup Regulator					
Regulated VDD Voltage		9.5	10	10.5	V
VDD Override Threshold				10.7	V
Overall					
I_{DD} (run)	f = 500kHz	2	5	10	mA
I_{DD} Startup Current	VDD = 5.4V			200	µA
VDD Clamp	IDD = 10mA	12	13.5	15	V

Note 1: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

CLKSYNC: An edge triggered active low TTL signal to this pin synchronizes the oscillator to an external clock. When VOUT decreases below 3.0V, the frequency foldback circuit is activated and the controller becomes unsynchronized. When VOUT exceeds 3.0V, the controller resynchronizes to the external clock.

COMP: The output of the voltage error amplifier used for compensation. The output is clamped to 3.0V minimum.

CS: Current sense input. This pin accepts a voltage proportional to converter inductor current. The voltage at CS is compared to the output of the compensated error amplifier to control the on-time of the switch. Voltage mode control can be realized by driving this pin with a fixed sawtooth ramp. Voltage feedforward is achieved by making the peak of this ramp proportional to the input voltage.

CSS: A capacitor, C_{SS}, to ground programs the soft start time for the power up sequence. This function is also used when an overcurrent fault occurs. As CSS is charged, the PWM comparator uses the lowest of either the voltage at CSS or the error amplifier output voltage to determine the duty cycle. The duty cycle, therefore, slowly increases during the soft start cycle. The faults that cause CSS to discharge and shutdown the controller are the logical OR of VREF below 4.4V or VDD below 8.8V. If a fault is still present when CSS is discharged below 0.5V, the supply remains off until the fault is cleared. The soft start time is determined by:

$$T_{SS} = 3.5 \bullet \frac{C_{SS}}{I_{SS}}$$

where I_{SS} is 20µA. A current limit terminates the present cycle. It does not generate a soft start cycle.

CT: A capacitor, C_T to ground, is charged and discharged creating the oscillator waveform. This waveform varies between 1.5V and 3.5V. The operating frequency is determined by

$$f = \frac{4.4}{C_T \bullet \left(\frac{R_{ON}}{1.5} + \frac{R_{OFF}}{3.5} \right)}$$

The ratio of the time duration of the positive sloped portion of the CT voltage waveform to the period gives the maximum duty cycle.

FB: The inverting input of the voltage amplifier used to sense the output voltage. The non-inverting input of the error amplifier is internally connected to 2.5V.

GND: The ground pin internally used for all the amplifiers and as the return for all resistor and capacitor connections to the UCC3884.

GT: Used to drive an external depletion-mode MOSFET for the housekeeping power supply. The MOSFET is turned off when the bootstrap winding voltage exceeds 10V. There is 300mV of hysteresis around the 10V turn-off voltage to prevent oscillation. See Typical Application.

IOFF: A resistor, R_{OFF}, to ground, programs the discharge current of the timing capacitor C_T. This is a variable discharge current which determines the negative slope of the oscillator voltage waveform at CT. The discharge time is dependent on the voltage at the VOUT pin. The discharge current is given by $I_{OFF} = VOUT/R_{OFF}$. The VOUT pin is internally clamped to 3.5V maximum.

ION: A resistor, R_{ON}, to ground programs the charge current of the timing capacitor, C_T, which generates the positive slope of the oscillator waveform. The charge time is constant and corresponds to the maximum output on-time at OUT. The charge current equation is $I_{ON} = 1.5V/R_{ON}$. When required the linear positive slope of the C_T voltage could be buffered and used to provide slope compensation into the CS pin.

OUT: The output of the controller. The peak source current is 0.5A and the peak sink current is 1.0A. The faults listed under the CSS description turn off this output.

PGND: The power ground pin is used as the return for the output transistor drive stage.

VDD: The input voltage of the chip. A low ESR and ESL ceramic capacitor from this pin to GND should be used to bypass internal switching transients.

VOUT: This pin accomplishes frequency foldback by controlling the discharge current for the oscillator C_T capacitor. A dc voltage proportional to the output voltage is connected to this pin. To startup with zero output voltage the user should tie a resistor between VREF and VOUT. The value depends on the lowest desired operating frequency. When VOUT decreases below 3.5V the frequency decreases by reducing the discharge current I_{OFF}. When VOUT increases, the frequency increases by increasing the discharge current. The maximum operating frequency occurs when VOUT = 3.5V. The C_T charge time is constant to guarantee a maximum output duty cycle. This pin must be above 3.0V to allow synchronization to occur.

PIN DESCRIPTIONS (cont.)

VREF: This pin is the output of the 5V regulated reference. Bypass this pin with a low ESR and ESL ceramic capacitor (e.g., 0.47µF).

VVS: Provides a programmable duty cycle clamp which is dependent upon the input voltage. A resistor divider network reduces the input voltage supplied to VVS. The IC determines the reciprocal of the voltage at VVS and scales the result. The voltage is then compared to the oscillator waveform to clamp the duty cycle. The purpose of this clamp is to reduce the likelihood of saturating the isolation transformer during unusual line or load conditions.

APPLICATION INFORMATION

Theory of Operation: The UCC3884 current mode PWM controller contains a programmable oscillator which includes the ability to synchronize multiple PWMs. The positive and negative sloped portions of the oscillator waveform (measured at CT), have time intervals that are set by external resistors at ION and IOFF. The operating frequency is inversely proportional to the timing capacitor. The negative sloped portion of the oscillator waveform is extended in time as the measured output voltage decreases providing protection during output faults. The power supply output voltage and the voltage from VREF are fed back to VOUT. When the output voltage decreases, the voltage at VOUT also decreases. As VOUT decreases below 3.5V, the operating frequency decreases. This reduction in frequency allows the duty cycle to decrease below what the CS to OUT delay would otherwise permit. This is referred to as frequency foldback. An output short circuit or overload causes the converter to enter the frequency foldback mode. Synchronization to other controllers can only occur during normal operation, that is, when VOUT is greater than 3.0V.

GT is provided to turn off an external depletion-mode MOSFET after startup when the bootstrap winding exceeds 10V. This depletion-mode MOSFET is used in the housekeeping section of the converter to simplify startup biasing circuitry. The amplifier that drives this MOSFET has 300mV of hysteresis to avoid oscillation during power up.

An accurate programmable volt-second technique clamps the duty cycle. The duty cycle limit is inversely proportional to input voltage and a resistor divider network is used to program the proportionality constant. At a given input voltage and constant load, under closed loop control, the operating duty cycle is a fixed value. The volt-second clamp duty cycle may then be set somewhat higher than this operating duty cycle. For other input voltages, the volt-second clamp will still exceed the steady state operating duty cycle. This allows normal closed loop operation of the converter. It is during a load transient (a fault such as a momentary short circuit) as the error amplifier increases the duty cycle, that when the volt-second clamp accurately limits the maximum volt-seconds. This ensures that the transformer does not saturate during a fault which can fail the power supply. After the fault is removed the converter resumes closed loop control.

CSS is provided which allows the UCC3884 to be disabled with an external transistor. The increasing pulse width at OUT during soft start should be programmed to be less than the pulse width of the duty cycle limit that the frequency foldback circuitry creates. The frequency foldback circuit will be in effect during soft start since the output voltage fed back to VOUT is less than 3.5V. Designing the circuit in this fashion allows a proper startup sequence.

The current sense feedback pin has an overcurrent protection feature which forces a soft start cycle only if the IC is not currently in a soft start cycle. A 1V bias at the PWM comparator's non-inverting input and a reset dominant PWM latch permit zero duty cycle operation.

The error amplifier has a wide gain-bandwidth product and its non-inverting input is internally set to 2.5VDC.

APPLICATION INFORMATION (cont.)

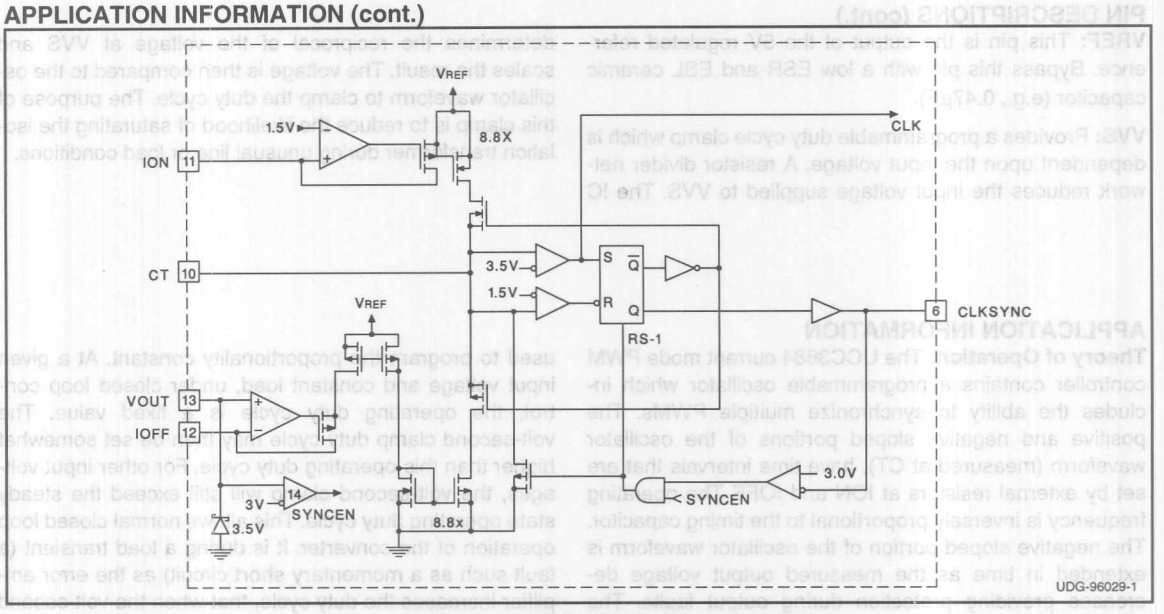


Figure 1. UCC3884 Oscillator

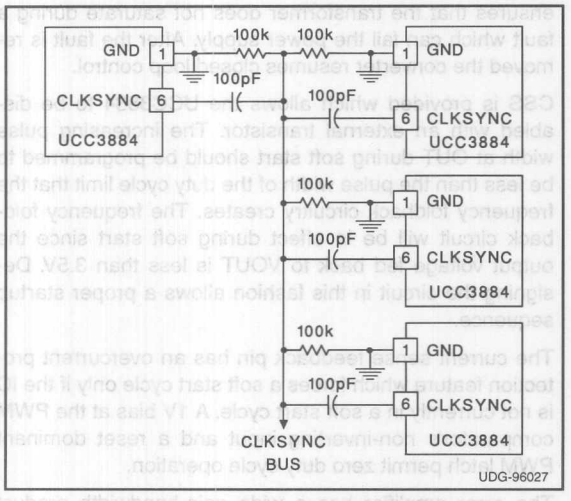


Figure 2. Oscillator Synchonization Connection Diagram

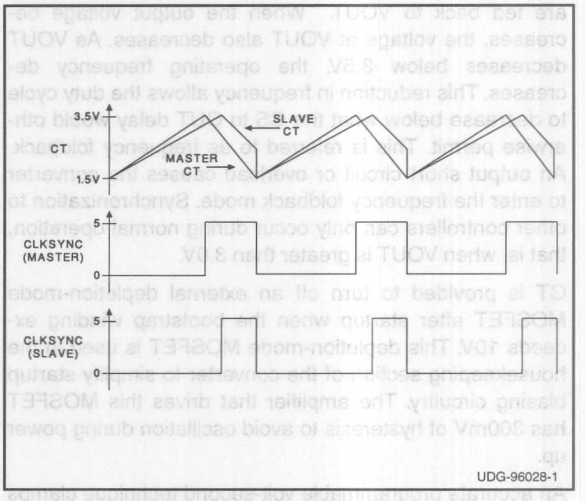


Figure 3. Oscillator Waveforms

OSCILLATOR INFORMATION

The oscillator has charge and discharge currents programmed with resistors to ground from ION and IOFF respectively, as seen on the Oscillator Block Diagram (Figure 1). This generates a linear sawtooth waveform on CT. Frequency foldback is accomplished by the level shifted output voltage controlling the VOUT voltage which decreases the discharge current and the frequency.

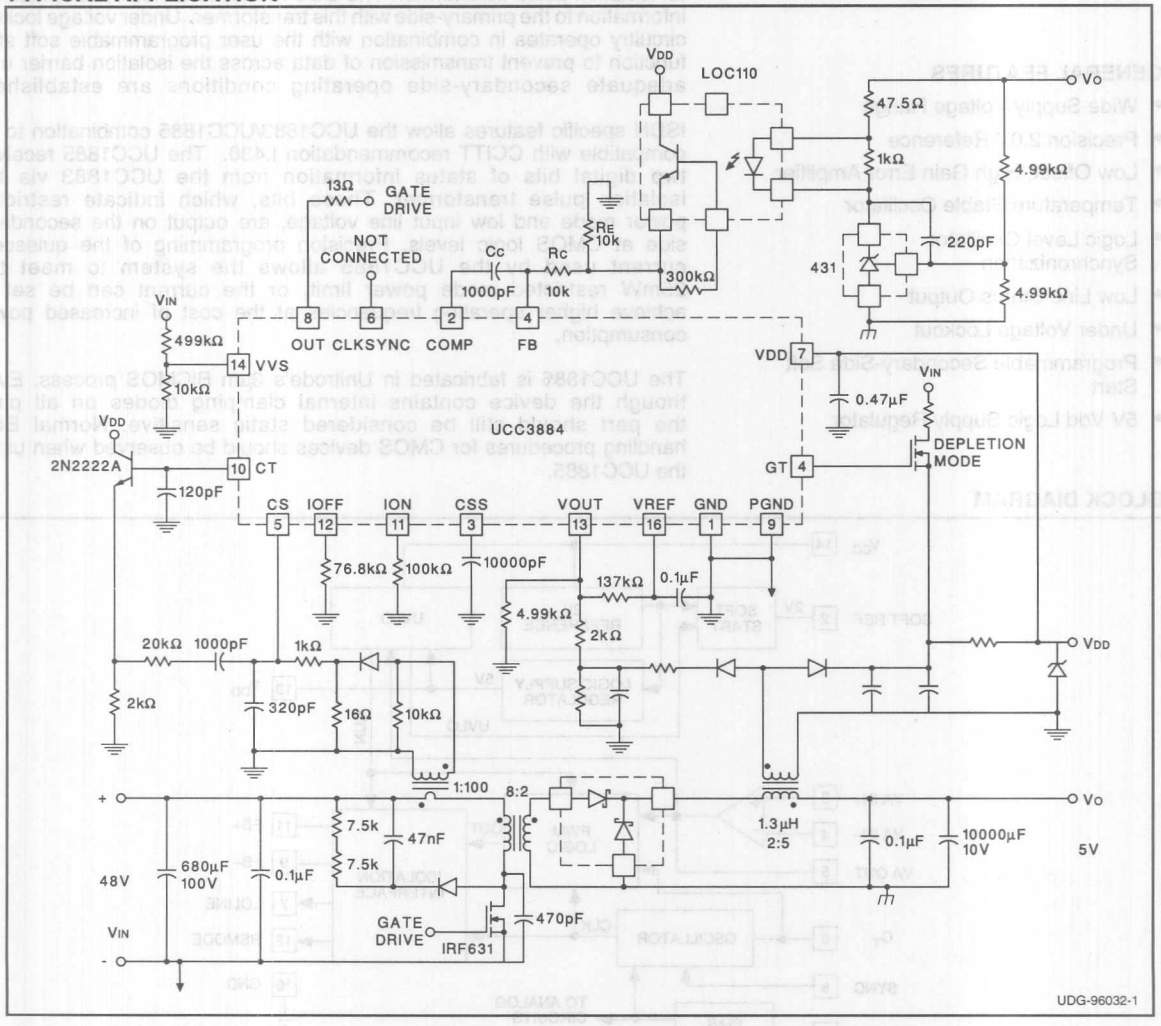
Synchronization is accomplished by coupling the fastest oscillator CLKSYNC signal as shown on the Oscillator Synchronization Diagram (Figure 2). The fastest (master) CLKSYNC pin will couple a negative pulse into the slower (slave) CLKSYNC pins forcing the slaves' CT pins to quickly discharge as shown on the Oscillator Waveform diagram (Figure 3).

OSCILLATOR INFORMATION (cont.)

The following explains two synchronization techniques:

1. If the user does not care which unit is the master, then the oscillator frequencies are designed as accurate as necessary and one unit will become the master and synchronize the remaining units. The user will never know exactly which unit will be the master upon power up.
2. If the user does care which unit is the master, a unit should be identified as the master, and the frequency and maximum duty cycle clamp should be programmed accordingly. The R_{OFF} resistor which programs the slave units oscillator discharge ramp should be between 50% and 100% of the R_{OFF} resistor which programs the master. This guarantees that if a slave unit tries to synchronize the master, the master frequency will still be faster than the slave frequency and the master will synchronize all the remaining units.

TYPICAL APPLICATION



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ELECTRICAL CHARACTERISTICS Unless otherwise noted, all specifications apply for T_A -55°C to +125°C for the UCC1885; -40°C to +85°C for the UCC2885; 0°C to +70°C for the UCC3885 $V_{CC} = V_{DD} = 5V$, SYNC = OV, R_{BIAS} = 200Kohms, Ct = 100pF, and $T_J = T_A$(min) to T_A(max)

UCC1885
UCC2885
UCC3885

PARAMETER	TEST CONDITIONS	Min	Typ	Max	Units
UVLO Section					
V_{CC} Start Threshold	$V_{DD} = V_{CC}$	2.4	2.7	3.0	V
V_{CC} Threshold Hysteresis	$V_{DD} = V_{CC}$	260	400	600	mV
V_{DD} Start Threshold	$V_{DD} < V_{CC}$	2.0	2.4	2.9	V
VA OUT Run Threshold	VA OUT = VA IN(–)	1.0	1.15	1.3	V
Reference Section					
Reference Voltage	Tj = 25°C, Rload > 50Mohm	1.98	2	2.02	V
Line Regulation	3V < V_{CC} < 16.5V	–	2	10	mV
Load Regulation	–500nA < Iout < 500nA	–	12	35	mV
Total Reference Variation	Initial + Line + Temperature Rload > 50Mohm	1.96	–	2.04	V
Soft Start Current	SOFTREF = 0V	4	10	16	uA
External Override Threshold		–	–	2.45	V
Input Bias Current	SOFTREF = 5V	–	–	50	nA
User Bias Section					
R_{BIAS} Voltage	Tj = 25°C	1.17	1.2	1.23	V
R_{BIAS} Pin Line Regulation	3V < Vcc < 16.5V	–	8	30	mV
Total R_{BIAS} Pin Variation	Initial + Line + Temperature	1.15	–	1.25	V
Error Amplifier Section					
Input Common Mode Range	VA OUT = 1V	1	–	4.5	V
Input Offset Voltage	VA IN(+) = 2V, VA OUT = 1V	– 8	–	8	mV
Input Bias Current	VA IN(+) = 2V, VA OUT = 1V	-100	–	100	nA
VA OUT Low Level	Vdm = –10mV, Iout = 700uA	–	0.05	0.15	V
VA OUT High Level	R_{BIAS} = 200K, Vdm = 10mV, Iout = – 50uA	2.0	2.6	–	V
	R_{BIAS} = 39.2K, Vdm = 10mV, Iout = – 250uA	2.0	2.7	–	V
VA OUT Short Circuit Current	VA OUT = 0V, R_{BIAS} = 39.2 Kohms	– 0.4	– 1	– 5	mA
Open Loop Voltage Gain	Vcm = 2V, 0.1 < VA OUT = < 2.0V R_{BIAS} = 39.2 Kohms	80	110	–	dB
DC PSRR	Vcm = 2V, 0.1 < VA OUT = 1V R_{BIAS} = 39.2K, 3V < Vcc < 16.5V	70	110	–	dB
DC CMRR	VA OUT = 1V, R_{BIAS} = 39.2K 1V < Vcm < 4V	70	100	–	dB
Unity Gain Bandwidth	R_{BIAS} = 200 Kohms, Cout = 25pF (Note 1)	375	500	–	KHz
	R_{BIAS} = 39.2 Kohms, Cout = 25pF (Note 1)	1.6	2.2	–	MHz
Open Loop Output Impedance	R_{BIAS} = 200K (Note 1)	–	2.2	3.3	Kohms
	R_{BIAS} = 39.2K (Note 1)		450	675	ohms
VA OUT Slew Rate	R_{BIAS} = 200K, Cout = 25pF (Note 1)	140	250	–	mV/us
	R_{BIAS} = 39.2K, Cout = 25pF (Note 1)	0.7	1.25	–	V/us
Oscillator Section					
Initial Accuracy	T_J = 25°C	42	48	56	KHz
Voltage Stability	3V < V_{CC} = V_{DD} < 7V	–	1	3	%
Total Oscillator Variation	Inital + Line + Temperature	41.5	–	58	KHz
C_T Ramp Amplitude		1.65	1.8	1.9	V
SYNC Input Low Voltage		–	–	1.5	V
SYNC Input High Voltage		3.5	–	–	V

ABSOLUTE MAXIMUM RATINGS

Analog Supply Voltage (V_{CC}) 18V
Maximum V_{CC} Slew Rate 3V/mS
Digital Supply Voltage (V_{DD}) 7V
Maximum Voltage, All Signal Pins ..... V_{DD} + 0.3V to 7V
Minimum Voltage, All Pins ..... – 0.3V
Maximum DC Current, Any Pin, Source or Sink 100mA
Maximum Peak Current, Any Pin, Source or Sink 500mA
Total Package Dissipation (N package) 1W
Total Package Dissipation (D package) 800mW
Storage Temperature ..... – 65°C to +150°C
Lead Temperature (Soldering, 10 seconds) ..... +300°C

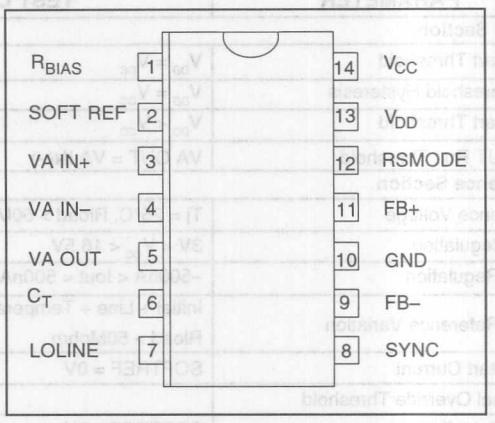
Note 1: All voltages expressed with respect to pin 10, currents are positive into the specified terminal.

Note 2: All maximum signal pin voltage limits apply for cases of zero source impedance. Higher or lower voltages may be impressed through a finite source impedance which causes the input current to be limited to the values specified, with total package power dissipation at or below specified limits.

Note 3: Consult Packaging Section of Databook for thermal limitations and considerations of package.

CONNECTION DIAGRAM

DIL-14, J or N Package, SOIC-14, D-Package



Pin Number	Pin Name	Pin Type	Function
1	R_{BIAS}	Analog Program	Quiescent Bias Current Set
2	SOFTREF	Analog Program & Output	Soft Start Timing Set and 2.0V Reference Output
3	VA IN +	Analog Input	Voltage Error Amplifier Non-Inverting Input
4	VA IN –	Analog Input	Voltage Error Amplifier Inverting Input
5	VA OUT	Analog Output	Voltage Error Amplifier Output
6	C_T	Analog Program	Oscillator Frequency Set
7	LOLINE	Digital Output	Low Primary-Side Line Voltage Status Bit (High = True)
8	SYNC	Digital Input	Oscillator SYNC (Positive-Edge Triggered)
9	FB –	Digital I/O	Differential Feedback Communication Signal (–)
10	GND	Supply Return	System Ground
11	FB +	Digital I/O	Differential Feedback Communication Signal (+)
12	RSMODE	Digital Output	CCITT Restricted Power Mode Status Bit (High = True)
13	V_{DD}	Logic Supply	5.0V Internal Regulator Output or Logic Supply Input
14	V_{CC}	Power Supply	Analog Power Supply Input

UNITRODE

UCC1885
UCC2885
UCC3885

Micropower Secondary Regulation IC

ISDN I.430 RELATED FEATURES

- Secondary-Side Voltage Sense for Improved Regulation
- Restricted Mode Status Output
- Precision Programmable Quiescent Current
- Very Low Quiescent Power for CCITT 25mW Restricted Mode

GENERAL FEATURES

- Wide Supply Voltage Range
- Precision 2.0V Reference
- Low Offset, High Gain Error Amplifier
- Temperature Stable Oscillator
- Logic Level Oscillator Synchronization
- Low Line Status Output
- Under Voltage Lockout
- Programmable Secondary-Side Soft Start
- 5V Vdd Logic Supply Regulator

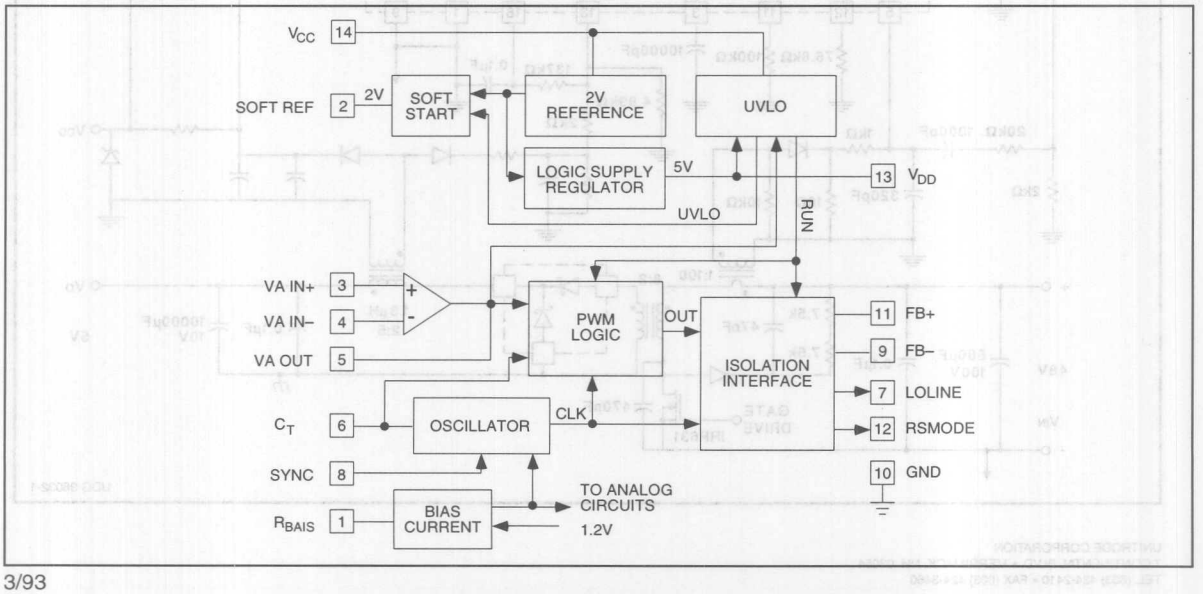
DESCRIPTION

The UCC1885 supplies the necessary functions to implement a fully isolated, ISDN compatible SMPS meeting the guidelines of CCITT recommendation I.430, when used in conjunction with the UCC1883 primary-side PWM controller. The UCC1885 secondary-side regulation IC provides improved regulation by allowing direct sensing of the output voltage on the secondary side of the DC/DC converter. The UCC1885 contains a precision system reference and a complete error amplifier. The output of the amplifier serves as the PWM control voltage and is provided to the primary-side via an isolation pulse transformer. The UCC1885 also sends synchronization information to the primary-side with this transformer. Under voltage lockout circuitry operates in combination with the user programmable soft start function to prevent transmission of data across the isolation barrier until adequate secondary-side operating conditions are established.

ISDN specific features allow the UCC1883/UCC1885 combination to be compatible with CCITT recommendation I.430. The UCC1885 receives two digital bits of status information from the UCC1883 via the isolation pulse transformer. These bits, which indicate restricted power mode and low input line voltage, are output on the secondary-side at CMOS logic levels. Precision programming of the quiescent current used by the UCC1885 allows the system to meet the 25mW restricted mode power limit, or the current can be set to achieve higher operating frequencies at the cost of increased power consumption.

The UCC1885 is fabricated in Unitrode's 3µm BiCMOS process. Even though the device contains internal clamping diodes on all pins, the part should still be considered static sensitive. Normal ESD handling procedures for CMOS devices should be observed when using the UCC1885.

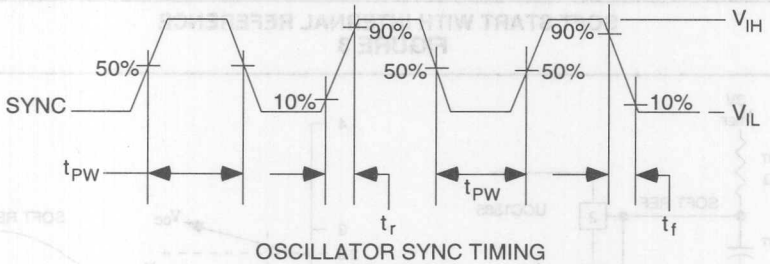
BLOCK DIAGRAM



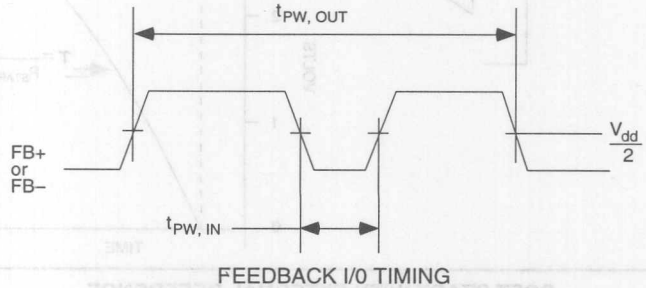
ELECTRICAL CHARACTERISTICS : Unless otherwise noted, all specifications apply for T_A -55°C to +125°C for the UCC1885; -40°C to +85°C for the UCC2885; 0°C to +70°C for the UCC3885 $V_{CC} = V_{DD} = 5V$, SYNC = OV, R_{BIAS} = 200Kohms, Ct = 100pF, and $T_J = T_A(min)$ to $T_A(max)$

PARAMETER	TEST CONDITIONS	Min	Typ	Max	Units
Oscillator Section (Continued)					
Maximum SYNC Rise, Fall Time	(See Figure 1 and Note 1)	500	–	–	nS
Minimum SYNC Pulse Width	(See Figure 1 and Note 1)	10	15	nS	
Isolation Interface Section					
FB Output High Voltage	Rload = 500 ohms	4.0	4.5	–	V
FB Output Low Voltage	Rload = 50 ohms to 5V	–	0.5	0.85	V
FB Output Pulse Width	R_{BIAS} = 200 Kohms (See Figure 2)	200	300	450	ns
	R_{BIAS} = 39.2 Kohms (See Figure 2)	–	100	–	ns
FB Output PW Matching		–	15	–	ns
Minimum FB Input Pulse Width	(See Figure 2 and Note 1)	–	10	–	ns
Digital Status Output High	LOLINE, RSMODE, Iout = – 200uA	4.85	4.95	–	V
Digital Status Output Low	LOLINE, RSMODE, Iout = 800µA	–	0.3	0.45	V
V_{DD} Regulator					
V_{DD} Output Voltage	$V_{DD} < V_{CC}$, No External Load	4.75	5	5.25	V
V_{DD} Line Regulator	$7V < V_{CC} < 16.5V$	–	10	50	mV
V_{DD} Load Regulation	– 3mA < Iout < 0mA	–	100	250	mV
V_{DD} Regulator Dropout	No External Load	–	0.9	1.7	V
V_{DD} Short Circuit Current	V_{DD} = 0V	8	30	70	mA
Power Supplies					
DC Supply Current		–	100	150	uA
Cpd	(Note 2)	–	150	–	pF

Notes: 1. This parameter not 100% tested in production, but guaranteed by design.
2. Total power dissipation will be determined by associated isolation pulse transformer characteristics. A pulse transformer with a low loss core and at least 50µH of magnetizing inductance is strongly recommended.



OSCILLATOR SYNC TIMING
FIGURE 1



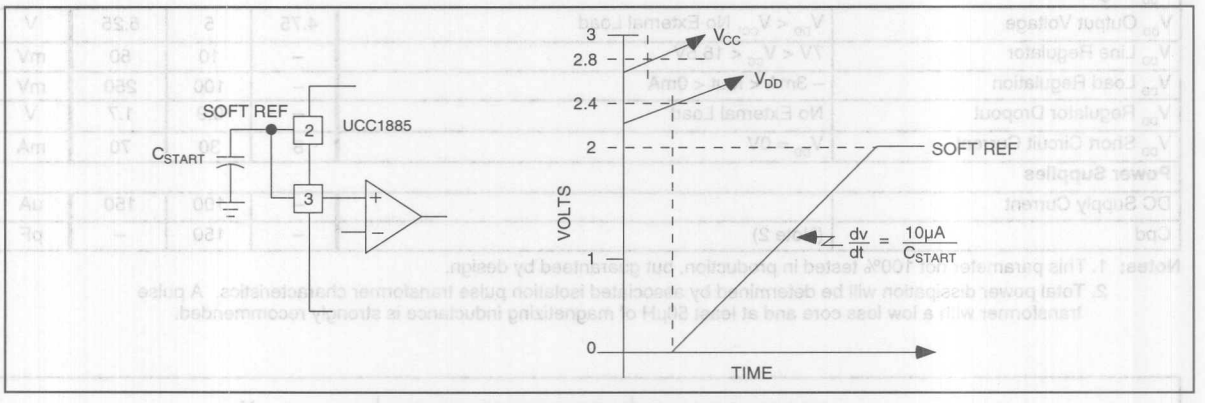
FEEDBACK I/0 TIMING
FIGURE 2

APPLICATIONS INFORMATION

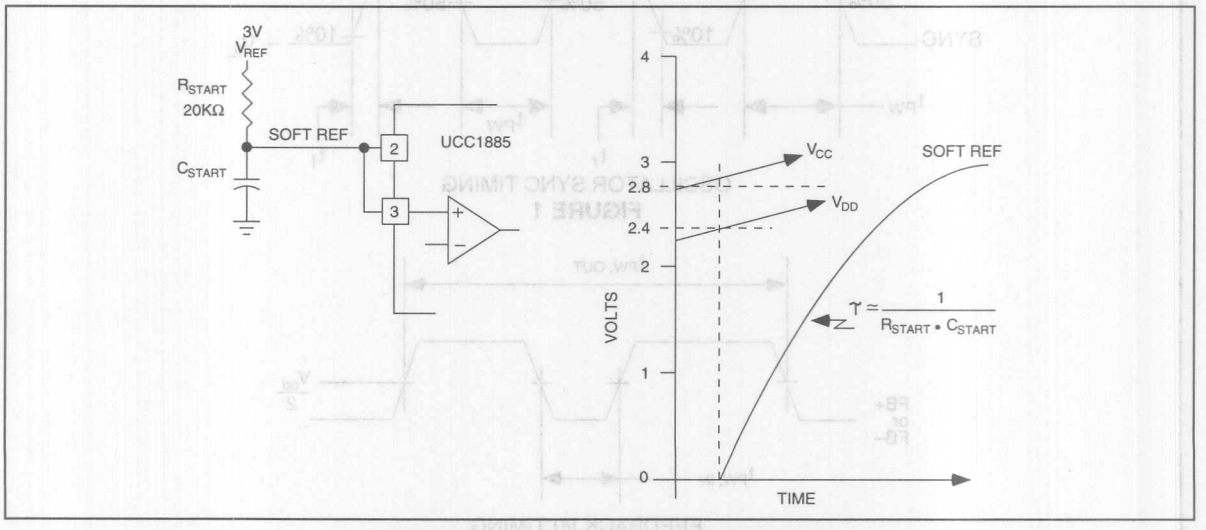
UNDER VOLTAGE LOCKOUT

When power is first applied to the UCC1885, SOFTREF is held at ground until V_{CC} exceeds 2.8V and V_{DD} exceeds 2.4V. Once adequate operating voltages have been established, SOFTREF is released and allowed to charge from an internal 10uA current source. A capacitor from this pin to ground may be used to continue an output soft start after the UCC1885 takes control of the SMPS with feedback communication to the UCC1883. In this case, the dV/dt established on SOFTREF must exceed the dV/dt established on the regulated output by the blind soft start being provided by the UCC1883. Normally the SOFTREF pin will charge to 2.0V, the value of the internal precision reference. Once the internal reference voltage is reached, the current source is disabled and the SOFTREF pin maintains an output impedance of 30KΩ, which, acting with any soft start capacitance, will then form a single-pole reference noise filter.

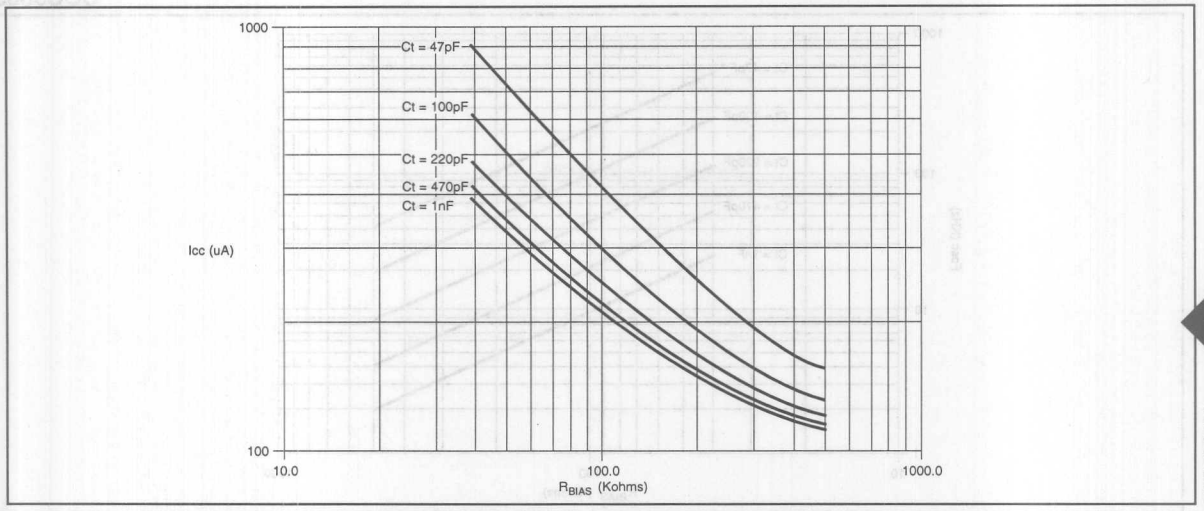
If the use of an external reference (V_{REF} > 2.5V) is desired, the soft start function can still be maintained on SOFTREF. In this case, the user must also supply a soft start resistor between the external reference and SOFTREF. The value of this resistor should be chosen such that the current sourced into the SOFTREF pin when the voltage reaches 2.0V is at least 20uA, which will allow the UCC1885 to sense the presence of an external reference. Once the external reference is sensed, the internal reference is disconnected from SOFTREF, making it high impedance and eliminating any DC error across the soft start resistor. The minimum value of the soft start resistor



SOFT START WITH INTERNAL REFERENCE
FIGURE 3



SOFT START WITH EXTERNAL REFERENCE
FIGURE 4



AVERAGE DC CURRENT VERSUS R_{BIAS} (Not including Pulse Transformer Loses)

FIGURE 5

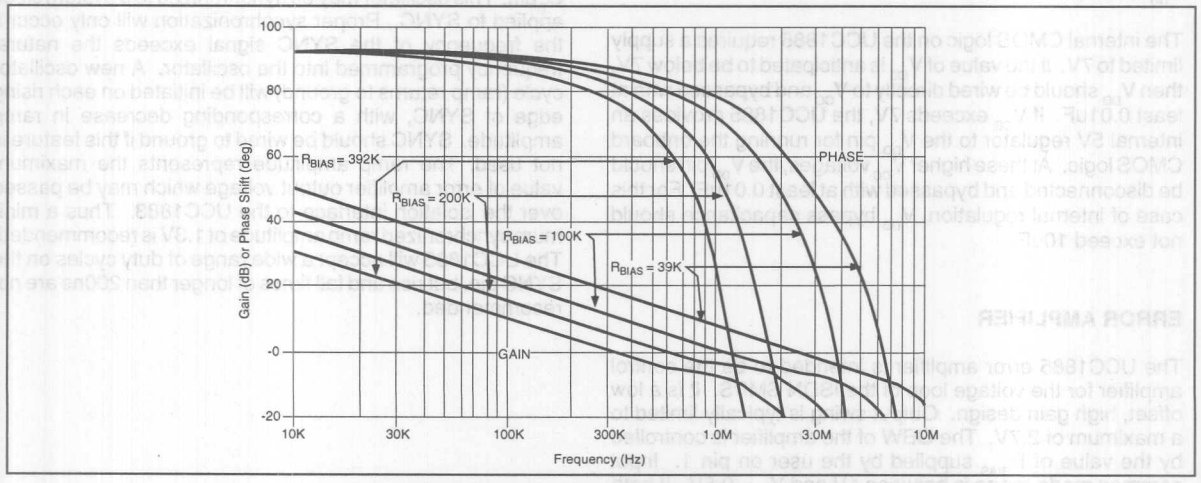
should be limited to allow SOFTREF to pull low during UVLO. The output impedance of SOFTREF during this phase of operation is about 300 ohms to ground.

The final portion of the UCC1885 UVLO sequence occurs when the output of the error amplifier increases above 1.15V. Normally this will not occur until the system reference has charged to some intermediate value. Assuming that adequate operating voltage has also been established, then the isolation interface on the UCC1885 begins transmitting output pulse width control information to the UCC1883 via an isolation pulse transformer. The 1.15V required on the output of the error amplifier guarantees that the UCC1885 will initially begin transmitting information to the primary-side PWM controller which keeps energy flowing to the secondary allowing the control loop to come into regulation. Once the isolation interface is enabled, the UVLO circuitry ignores all voltages appearing on the output of the error amplifier.

USER BIAS PROGRAMMING

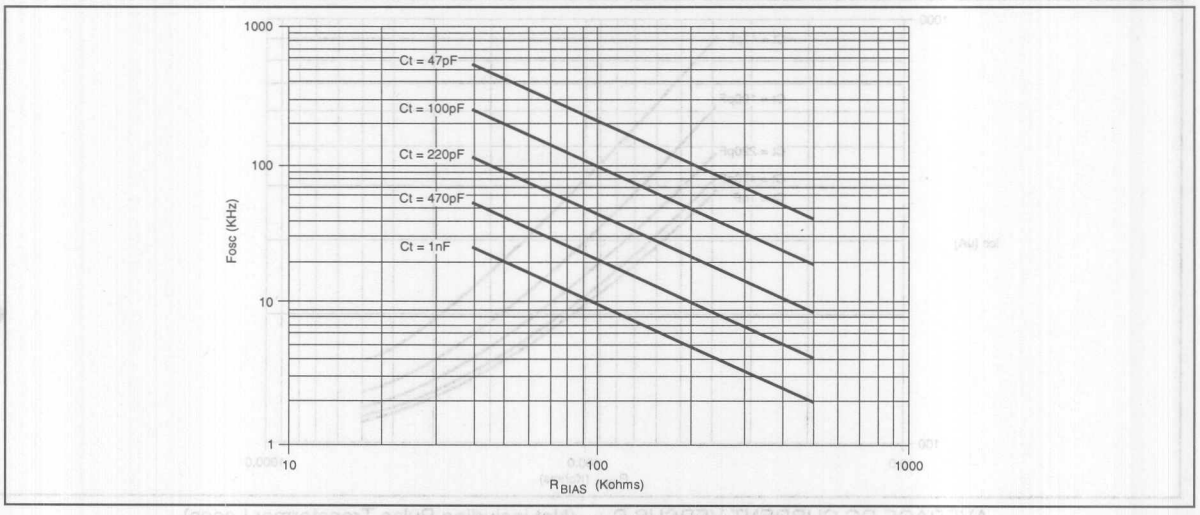
The R_{BIAS} pin may be used to set the amount of quiescent current consumed by certain analog circuits within the UCC1885. A resistor from this pin to ground establishes a user bias current according to the equation

$$I_{BIAS} = \frac{1.2V}{R_{BIAS}}$$



ERROR AMPLIFIER GBW VERSUS R_{BIAS}

FIGURE 6



OSCILLATOR FREQUENCY VERSUS R_{BIAS}
FIGURE 7

Recommended range for R_{BIAS} is 39.2 KΩ to 392 KΩ. Internal circuits on the UCC1885 consume a total quiescent current of $9 \bullet I_{BIAS}$, plus some fixed currents amounting to about 50uA at room temperature. Additional dynamic current consumption may be calculated with C_{PD} (see specifications), given a certain oscillator frequency f_{OSC}, from the equation

$$I_{DYNAMIC} = C_{PD} \bullet V_{DD} \bullet f_{OSC}$$

Also note from the specifications that the voltage on R_{BIAS} is well controlled and thus may be effectively used as another reference voltage in the system.

V_{DD} LOGIC SUPPLY

The internal CMOS logic on the UCC1885 requires a supply limited to 7V. If the value of V_{CC} is anticipated to be below 7V, then V_{DD} should be wired directly to V_{CC} and bypassed with at least 0.01uF. If V_{CC} exceeds 7V, the UCC1885 provides an internal 5V regulator to the V_{DD} pin for running the onboard CMOS logic. At these higher V_{CC} voltages, the V_{DD} pin should be disconnected and bypassed with at least 0.01uF. For this case of internal regulation, V_{DD} bypass capacitance should not exceed 10uF.

ERROR AMPLIFIER

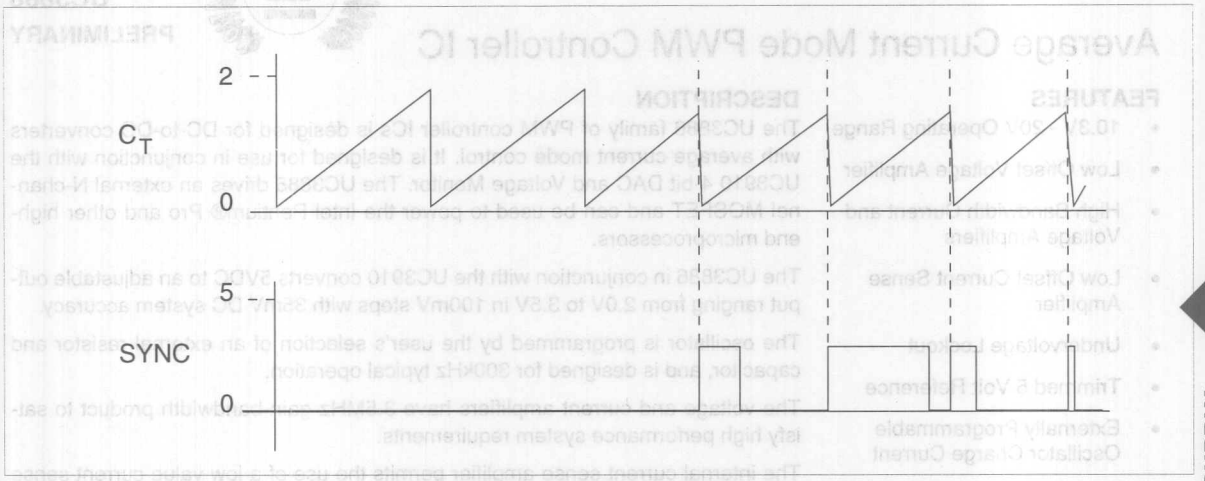
The UCC1885 error amplifier is intended to be the control amplifier for the voltage loop of the ISDN SMPS. It is a low offset, high gain design. Output swing is typically limited to a maximum of 2.7V. The GBW of the amplifier is controlled by the value of R_{BIAS} supplied by the user on pin 1. Input common mode range is between 1V and V_{CC} - 0.5V. If both inputs are beneath the common mode range during soft start, special circuitry on the UCC1885 guarantees VA out will be very near ground to insure proper startup.

OSCILLATOR

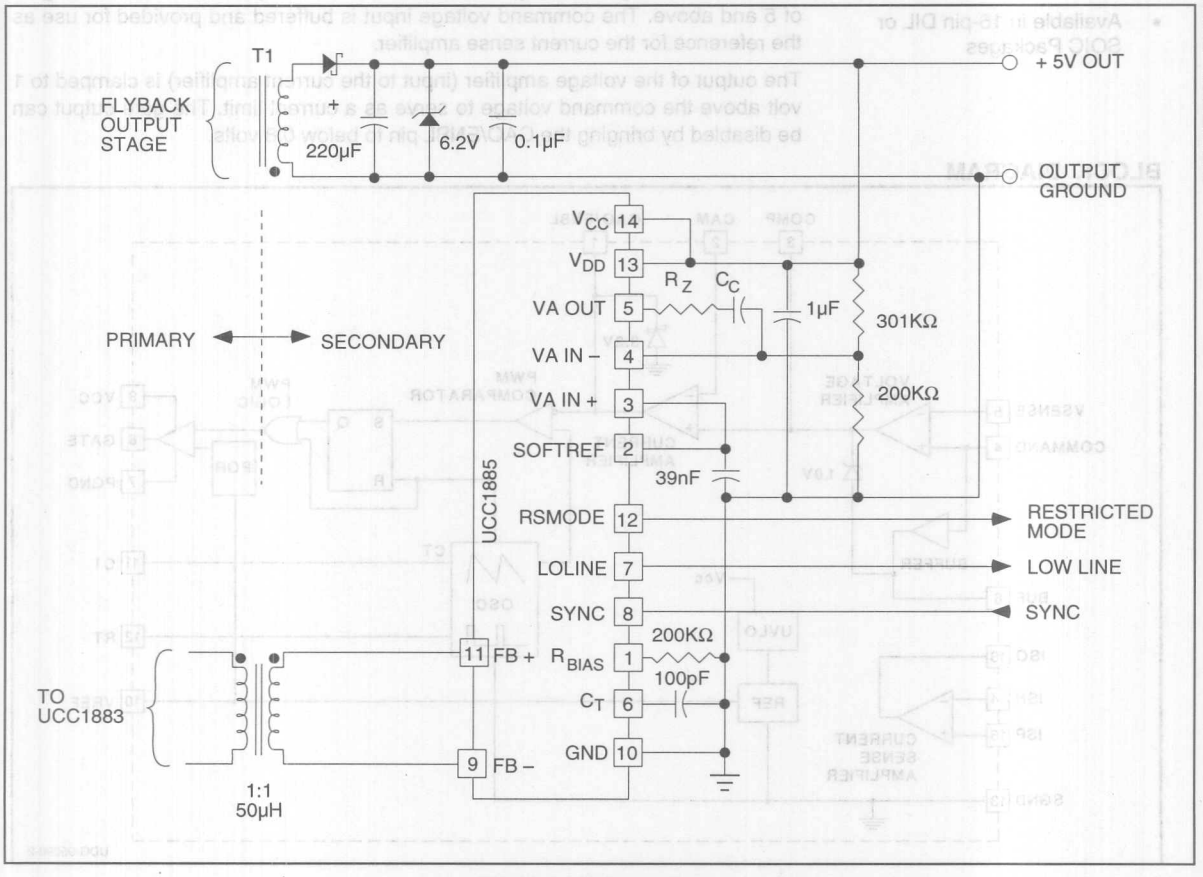
A timing capacitor is connected between C_T and ground to program a natural oscillator frequency according to the equation

$$f_{OSC} = \frac{1}{C_T \bullet R_{BIAS}}$$

A ramp voltage running from ground to 1.8V is created on the C_T pin. This oscillator may be synchronized to a system clock applied to SYNC. Proper synchronization will only occur if the frequency of the SYNC signal exceeds the natural frequency programmed into the oscillator. A new oscillator cycle (ramp returns to ground) will be initiated on each rising edge of SYNC, with a corresponding decrease in ramp amplitude. SYNC should be wired to ground if this feature is not used. The ramp amplitude represents the maximum value of error amplifier output voltage which may be passed over the isolation interface to the UCC1883. Thus a minimum synchronized ramp amplitude of 1.3V is recommended. The UCC1885 will accept a wide range of duty cycles on the SYNC pin, but rise and fall times of longer than 200ns are not recommended.



OSCILLATOR WAVEFORMS
FIGURE 8



TYPICAL APPLICATION
FIGURE 9

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. 603-424-2410 • FAX 603-424-3460

UNITRODE

UC1886
UC2886
UC3886
PRELIMINARY

Average Current Mode PWM Controller IC

FEATURES

- 10.3V - 20V Operating Range
- Low Offset Voltage Amplifier
- High Bandwidth Current and Voltage Amplifiers
- Low Offset Current Sense Amplifier
- Undervoltage Lockout
- Trimmed 5 Volt Reference
- Externally Programmable Oscillator Charge Current
- 1.5A Peak Totem Pole Output
- Available in 16-pin DIL or SOIC Packages

DESCRIPTION

The UC3886 family of PWM controller ICs is designed for DC-to-DC converters with average current mode control. It is designed for use in conjunction with the UC3910 4-bit DAC and Voltage Monitor. The UC3886 drives an external N-channel MOSFET and can be used to power the Intel Pentium® Pro and other high-end microprocessors.

The UC3886 in conjunction with the UC3910 converts 5VDC to an adjustable output ranging from 2.0V to 3.5V in 100mV steps with 35mV DC system accuracy.

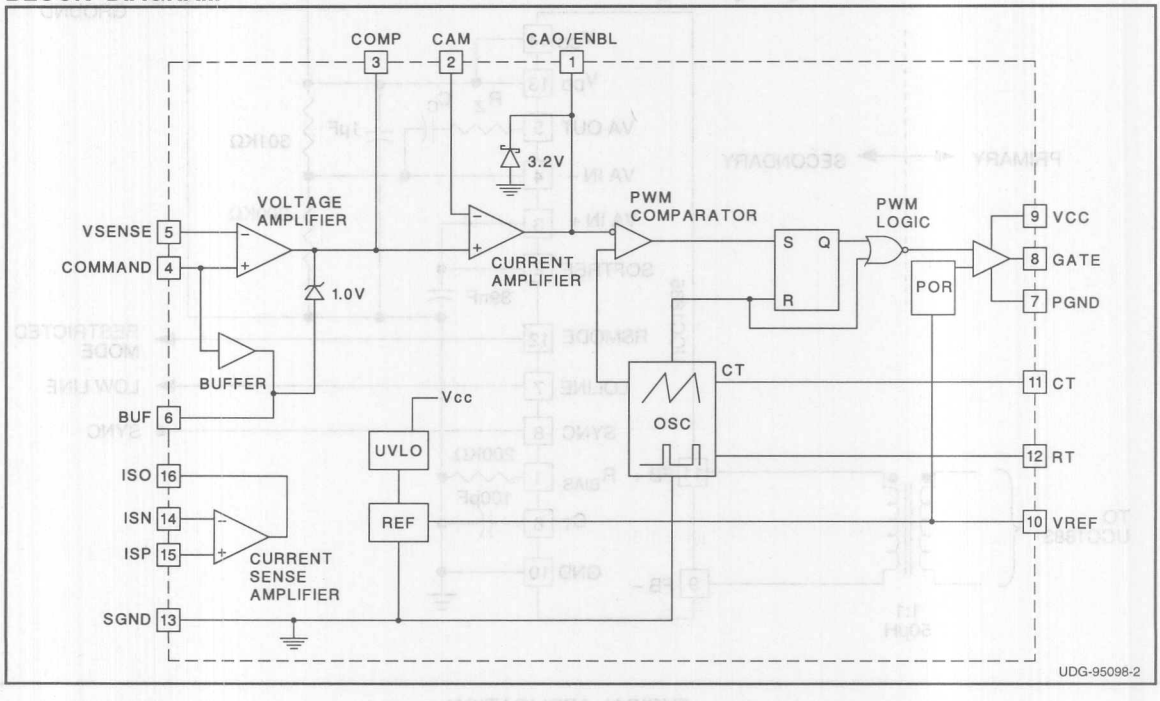
The oscillator is programmed by the user's selection of an external resistor and capacitor, and is designed for 300kHz typical operation.

The voltage and current amplifiers have 3.5MHz gain-bandwidth product to satisfy high performance system requirements.

The internal current sense amplifier permits the use of a low value current sense resistor, minimizing power loss. It has inputs and outputs accessible to allow user-selection of gain-setting resistors, and is internally compensated for a gain of 5 and above. The command voltage input is buffered and provided for use as the reference for the current sense amplifier.

The output of the voltage amplifier (input to the current amplifier) is clamped to 1 volt above the command voltage to serve as a current limit. The gate output can be disabled by bringing the CAO/ENBL pin to below 0.8 volts.

BLOCK DIAGRAM

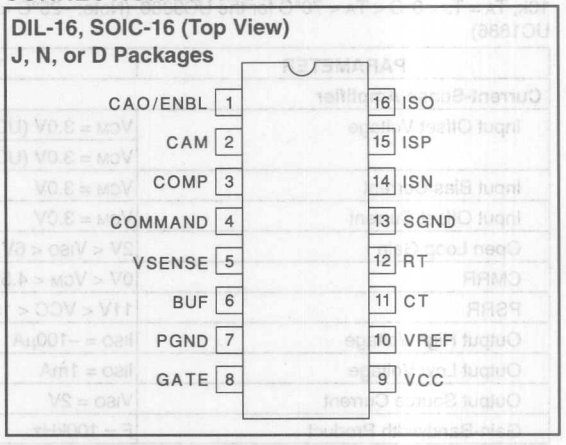


ABSOLUTE MAXIMUM RATINGS

Supply Voltage 20V
Output Current
CAM, COMMAND, VSENSE, ISN, ISP. . . . . ±1A
Analog Input . . . . . –0.3V to 7V
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperatue (Soldering, 10 sec.). . . . . +300°C
Currents are positive into, negative out of the specified terminal.
Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

DIL-16, SOIC-16 (Top View)
J, N, or D Packages



ELECTRICAL CHARACTERISTICS

Unless otherwise specified, VCC = 12V, VCOMMAND = 3.0V, CT = 1nF, RT = 10k, TA = TJ = 0°C < TA < 70°C for the UC3886. (Note: –25°C < TA < 85°C for the UC2886, and –55°C < TA < 125°C for the UC1886)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Overall					
Supply Current	VCC = 11V, Gate Open		10	15	mA
	VCC = 9.3V			5	mA
Undervoltage Lockout					
Start Threshold		9.7	10.3	10.8	V
UVLO Hysteresis			0.25	0.4	V
Voltage Error Amplifier					
Input Offset Voltage	VCM = 3.0V (UC3886)			4	mV
	VCM = 3.0V (UC2886, UC1886)			15	mV
Input Bias Current	VCM = 3.0V			–2	µA
Input Offset Current	VCM = 3.0V (UC3886)			0.01	µA
	VCM = 3.0V (UC2886, UC1886)			0.1	µA
Open Loop Gain	2.5V < VCOMP < 3.5V	60	85		dB
Common-Mode Rejection Ratio	2V < VCOMP < 4V	60	85		dB
Power Supply Rejection Ratio	11V < VCC < 15V	60	85		dB
Output High Voltage (Clamp)	ICOMP = –100µA (UC3886)	3.95	4	4.05	V
	ICOMP = –100µA (UC2886, UC1886)	3.9		4.1	V
Output Low Voltage (Clamp)	ICOMP = 100µA	1.9		2.7	V
Output Sink Current	VCOMP = 3.7V	0.9			mA
Output Source Current	VCOMP = 2.8V	–0.15	–0.25		mA
Gain-Bandwidth Product	F = 100kHz	2	3.5		MHz
5.0V Reference					
Output Voltage	IVREF = 1.0mA	4.9	5	5.1	V
Total Variation	Line, Load, Temperature	4.825		5.175	V
Line Regulation	11V < VCC < 15V			10	mV
Load Regulation	0 < IVREF < 2mA			15	mV
Short Circuit Current		–10		–40	mA
Input Buffer					
Gain	IBUF = ±500µA (UC3886)	0.98	1	1.02	V/V
	IBUF = ±500µA (UC2886, UC1886)	0.95		1.05	V/V

ELECTRICAL CHARACTERISTICS (cont.) Unless otherwise specified, VCC = 12V, $V_{COMMAND}$ = 3.0V, CT = 1nF, RT = 10k, $T_A = T_J = 0°C < T_A < 70°C$ for the UC3886. (Note: $-25°C < T_A < 85°C$ for the UC2886, and $-55°C < T_A < 125°C$ for the UC1886)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Current-Sense Amplifier					
Input Offset Voltage	V_{CM} = 3.0V (UC3886)			2	mV
	V_{CM} = 3.0V (UC2886, UC1886)			6	mV
Input Bias Current	V_{CM} = 3.0V			-1	µA
Input Offset Current	V_{CM} = 3.0V			0.2	µA
Open Loop Gain	2V < V_{ISO} < 6V	60	85		dB
CMRR	0V < V_{CM} < 4.5V	60	85		dB
PSRR	11V < VCC < 15V	60	85		dB
Output High Voltage	I_{ISO} = –100µA	5			V
Output Low Voltage	I_{ISO} = 1mA			1	V
Output Source Current	V_{ISO} = 2V	–0.2			mA
Gain-Bandwidth Product	F = 100kHz	2	3.5		MHz
Current Amplifier					
Input Offset Voltage	V_{CM} = 3.0V (UC3886)			13	mV
	V_{CM} = 3.0V (UC2886, UC1886)			18	mV
Input Bias Current	V_{CM} = 3.0V			1	µA
Open Loop Gain	1V < V_{CAO} < 3V	60	85		dB
CMRR	1.5V < V_{CM} < 4.5V	60	85		dB
PSRR	11V < VCC < 15V	60	85		dB
Output High Voltage	I_{CAO} = –100µA	3		3.3	V
Output Low Voltage	I_{CAO} = 100µA			1	V
Output Source Current	V_{CAO} =1V	–0.1	–0.25		mA
Gain-Bandwidth Product	F = 100kHz	2	3.5		MHz
Oscillator					
Frequency	RT = 10k, CT = 1nF (UC3886)	90	100	110	kHz
	RT = 10k, CT = 1nF (UC2886, UC1886)	85		115	kHz
Frequency Change With Voltage	11V > VCC > 15V			1	%
CT Peak Voltage		2.6	2.8		V
CT Valley Voltage			1	1.2	V
CT Peak-to-Peak Voltage		1.6	1.8	2.0	V
Output Section					
Output Low Voltage	I_{GATE} = 200mA		1.6	2.2	V
Output High Voltage	I_{GATE} = –200mA	9	10.3		V
Output Low Voltage	5V < VCC < 9V, I_{GATE} = 10mA			0.5	V
	V_{CAO} < 0.8V, I_{GATE} = 10mA			0.5	V
Rise/Fall Time	C_L = 1nF			150	ns
Maximum Duty Cycle	(UC3886)	90			%
	(UC2886, UC1886)	85			%

PIN DESCRIPTIONS

BUF (Buffer output): The voltage on COMMAND pin is buffered and presented to the user here. This voltage is used to provide the operating bias point for the current sense amplifier by connecting a resistor between BUF and ISP. Decouple BUF with 0.01µF or greater to SGND.

CAM (Current Amplifier Minus input): The average load current feedback from ISO is typically applied through a resistor here.

CAO/ENBL (Current Amplifier Output/Chip Enable): The current loop compensation network is connected between CAO/ENBL and CAM, the inverting input of the current amplifier. The voltage at CAO/ENBL is the input to the PWM comparator and regulates the output voltage of the system. The GATE output is disabled (held low) unless the voltage at this pin exceeds 1.0 volts, allowing the PWM to force zero duty cycle when necessary. The user can force this pin below 0.8 volts externally with an open collector, disabling the GATE drive.

COMMAND (Voltage amplifier non-inverting input): This input to the voltage amplifier is connected to a command voltage, such as the output of a DAC. This voltage sets the switching regulator output voltage.

COMP(Compensation, Voltage Amplifier output): The system voltage compensation network is applied between COMP and VSENSE. The voltage at COMP is clamped to prevent it from going more than 1V above the COMMAND voltage. This is used to provide an accurate average current limit. The voltage on COMP is also clamped to 0.7V below the voltage on COMMAND. This is done to avoid applying a full charge to capacitors in the compensation network during transients, allowing quick recovery time and little overshoot.

CT (Oscillator timing capacitor): A capacitor from CT to SGND along with the resistor on RT, sets the PWM frequency and maximum duty cycle according to these formulas:

$$D_{MAX} = 1 - \frac{2.0V}{(R_T \bullet 4.0mA)}$$

where D_{MAX} is the maximum operating duty cycle, and RT is in ohms.

$$F_{OSC} = \frac{2.0V \bullet ((4.0mA \bullet R_T) - 2.0V)}{C_T \bullet 1.8V \bullet R_T^2 \bullet 4.0mA}$$

where F_{OSC} is the UC3886 oscillator switching frequency in Hz, R_T is in ohms, and C_T is in farads.

GATE (PWM output): The output is a 1A totem pole driver. Use a series resistor of at least 5 ohms to prevent interaction between the gate impedance and the output driver that might cause excessive overshoot.

ISN (Current Sense Amplifier inverting input): A resistor to the low side of the average current sense resistor and a resistor to ISO are applied to this pin to make a differential sensing amplifier.

ISO (Current Sense Amplifier output): A feedback resistor to ISN is connected here to make a differential sensing amplifier. The voltage at this pin is equal to (V_{BUF} + A • I_{AVG} • R_{SENSE}) where A is the user determined gain of the differential amplifier, I_{AVG} is the average load current of the system, and R_{SENSE} is the average current sensing resistor. For stability, A must be greater than 5. Set A such that A • Isc • R_{SENSE} = 1.0V where ISC is the user-determined short circuit current limit.

ISP (Current Sense Amplifier non-inverting input): A resistor to the high side of the average current sense resistor and a resistor to BUF are connected to this pin to make a differential sensing amplifier.

PGND (power ground): The PWM output current returns to ground through this pin. This is separated from SGND to avoid on-chip ground noise generated by the output current.

RT (Oscillator charging current): This pin is held at 2V. Resistor RT from this pin to SGND sets the oscillator charging current. Use 5k < RT < 100k.

SGND (Signal Ground): For better noise immunity, signal ground is provided at this pin.

VCC (Positive supply voltage): This pin supplies power to the chip and to the gate drive output. Decouple to PGND and separately to SGND for best noise immunity. The reference (VREF), GATE output, oscillator, and amplifiers are disabled until VCC exceeds 10.3 volts.

VREF (Voltage reference output): An accurate 5V reference as provided at this pin. The output can deliver 2mA to external circuitry, and is internally short circuit current limited. VREF is disabled if VCC is below UVLO. Bypass 5V REF to SGND with an 0.01µF or larger capacitor for best stability

VSENSE (Voltage sense input): This input is connected to COMP through a feedback network and to the power supply output through a resistor or a divider network.

APPLICATION INFORMATION

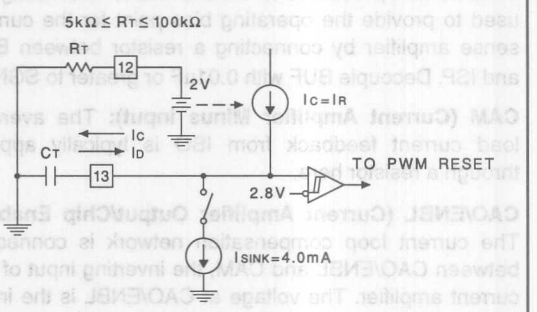
OSCILLATOR

The UC3886 oscillator is a saw tooth. The rising edge is governed by a current controlled by RT flowing into the capacitor CT. The falling edge of the sawtooth sets the dead time for the output. Selection of RT should be done first, based on desired maximum duty cycle. CT can then be chosen based on the desired frequency, FS, and the value of RT. The design equations are:

$$D_{MAX} = 1 - \frac{2.0V}{(R_T \bullet 4.0mA)}$$

$$F_{OSC} = \frac{2.0V \bullet ((4.0mA \bullet R_T) - 2.0V)}{C_T \bullet 1.8V \bullet R_T^2 \bullet 4.0mA}$$

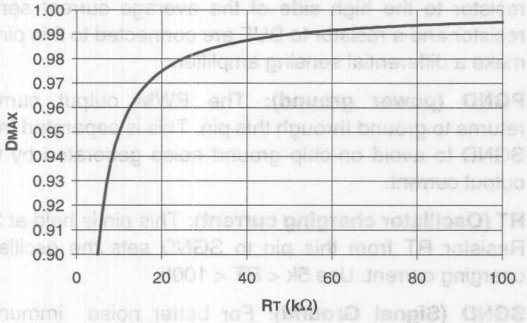
Oscillator



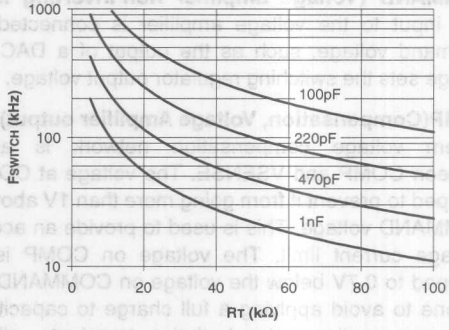
UDG-96022

OSCILLATOR (cont.)

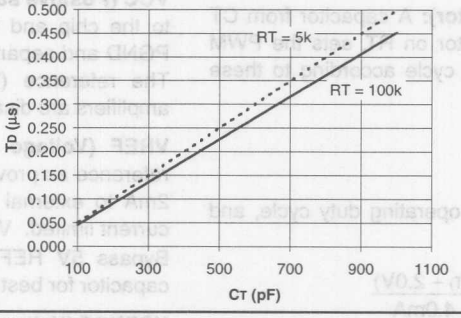
Programming Maximum Duty Cycle with RT



Programming Switching Frequency with CT



Deadtime vs. CT and RT



APPLICATION INFORMATION (cont.)

Configuring the Current Sense Amplifier

The UC3886 Current Sense Amplifier is used to amplify a differential current sense signal across a low value current sense resistor, RSENSE. This amplifier must be set up as a differential amplifier as shown.

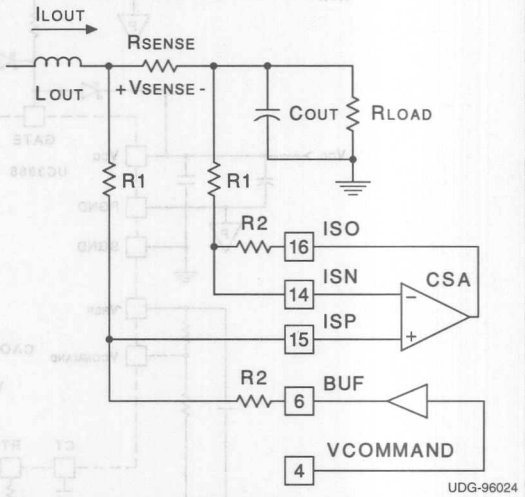
The Current Sense Amplifier gain, GCSA, is given by the ratio of R2/R1. The output of the Current Sense Amplifier at the ISO pin is given by

$$V_{ISO} = V_{BUF} + V_{SENSE} \bullet \frac{R2}{R1}$$

The Current Sense Amplifier gain, GCSA, must be programmed to be greater than or equal to 5.0 (14dB), as this amplifier is not stable with gain below 5.0. The Current Sense Amplifier gain is limited on the high side by its Gain-Bandwidth product of 2.5MHz. Therefore GCSA must be programmed between

$G_{CSA_MIN} = 5.0$ and $G_{CSA_MAX} = 2.5MHz/F_{SWITCH}$

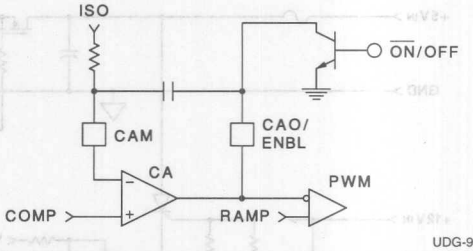
Configuring the Current Sense Amplifier of the UC3886



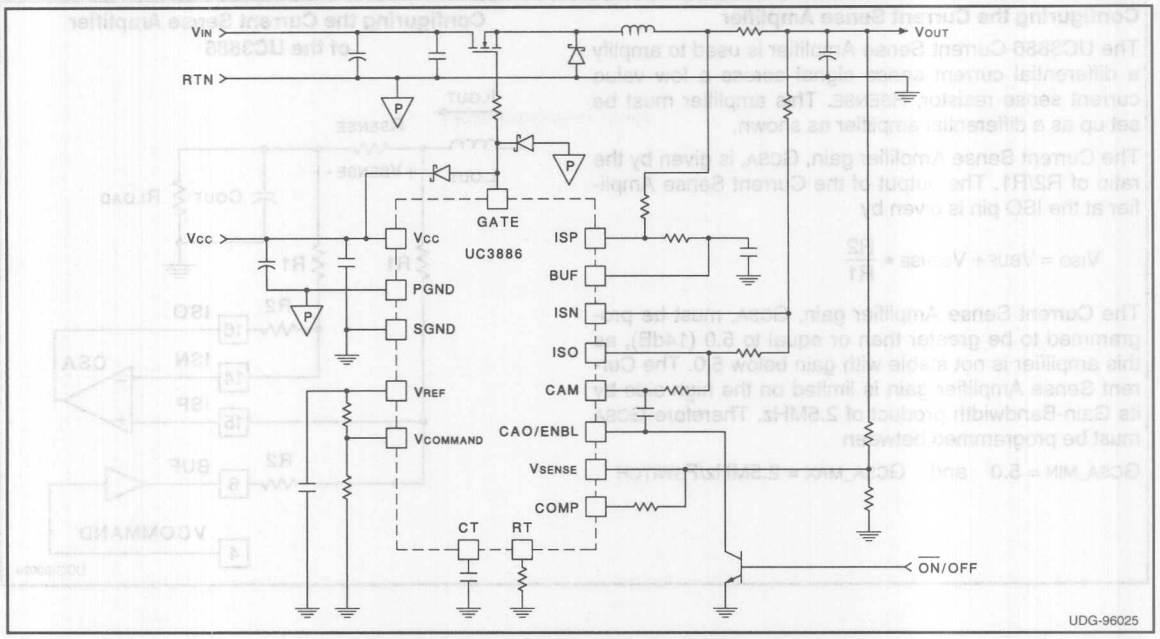
Enabling/Disabling the UC3886 Gate Drive

The CAO/ENBL pin can be used to Disable the UC3886 gate drive by forcing this pin below 0.8V, as shown. Bringing the voltage below the valley of the PWM oscillator ramp will insure a 0% duty cycle, effectively disabling the gate drive. A low noise open collector signal should be used as an Enable/Disable command.

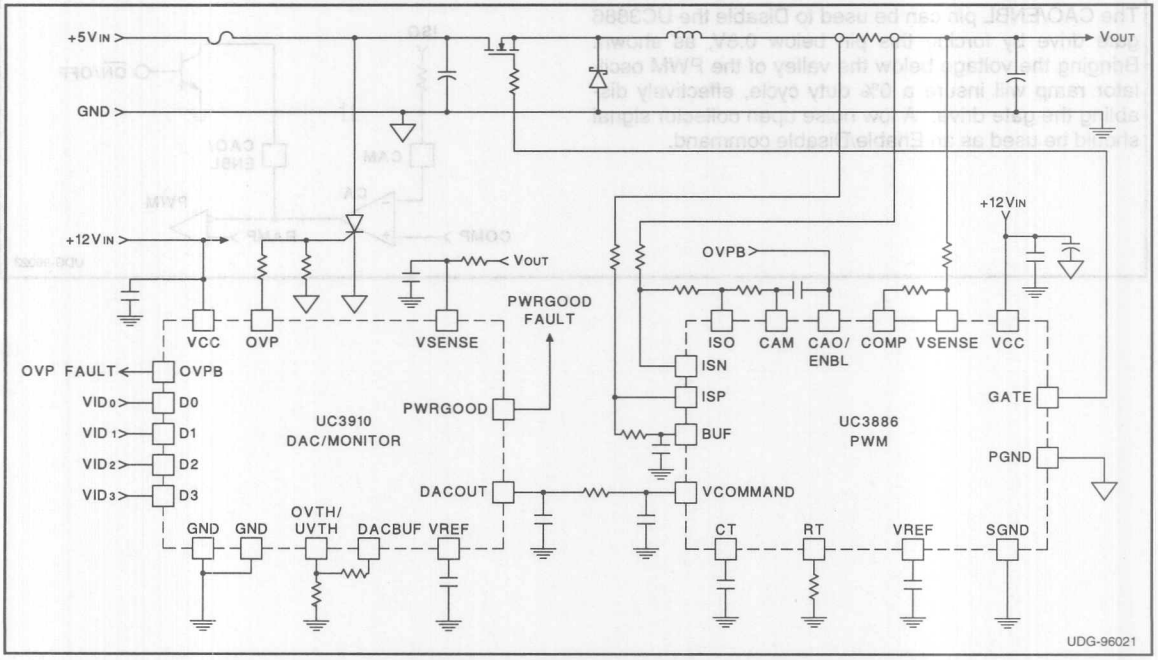
Enabling/Disabling the UC3886



TYPICAL APPLICATIONS



The UC3886 Configured in a Buck Regulator



UC3886 Configured with the UC3910 for a Pentium® Pro DC/DC Converter

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

Off-line Power Supply Controller

FEATURES

- Transformerless Off-line Power Supply
- Wide 100VDC to 400VDC Allowable Input Range
- Fixed 5VDC or Adjustable Low Voltage Output
- Output Sinks 200mA, Sources 150mA Into a MOSFET Gate
- Uses Low Cost SMD Inductors
- Short Circuit Protected
- Optional Isolation Capability

DESCRIPTION

The UCC3888 controller is optimized for use as an off-line, low power, low voltage, regulated bias supply. The unique circuit topology utilized in this device can be visualized as two cascaded flyback converters, each operating in the discontinuous mode, both driven from a single external power switch. The significant benefit of this approach is the ability to achieve voltage conversion ratios as high as 400V to 2.7V with no transformer and low internal losses.

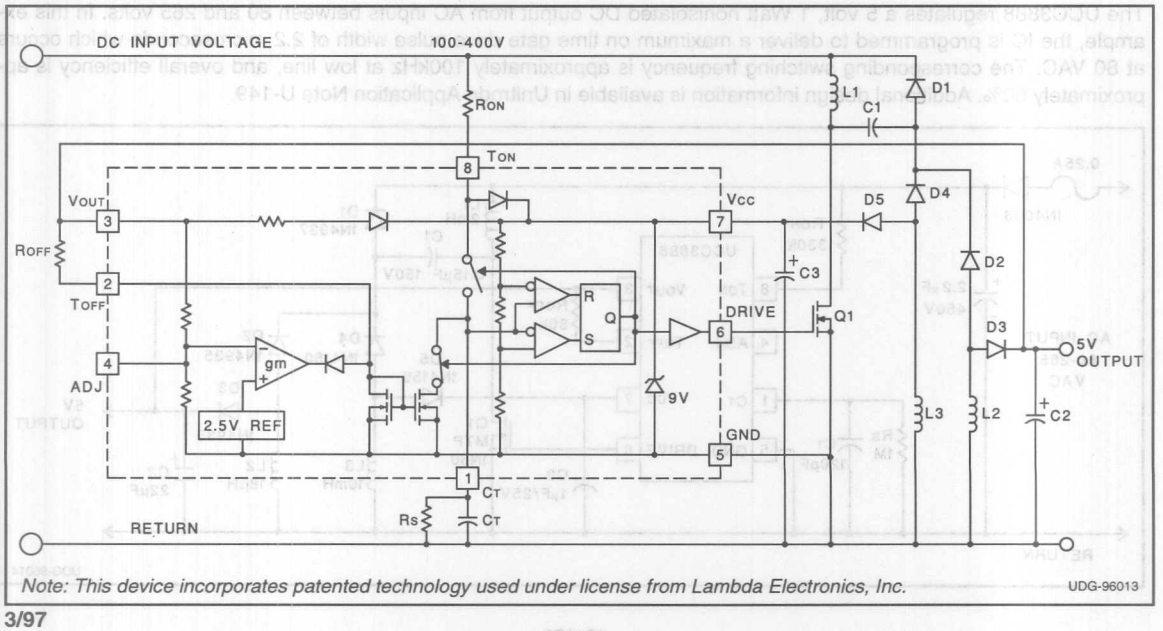
The control algorithm utilized by the UCC3888 sets the switch on time inversely proportional to the input line voltage and sets the switch off time inversely proportional to the output voltage. This action is automatically controlled by an internal feedback loop and reference. The cascaded configuration allows a voltage conversion from 400V to 2.7V to be achieved with a switch duty cycle of 7.6%. This topology also offers inherent short circuit protection since as the output voltage falls to zero, the switch off time approaches infinity.

The output voltage is set internally to 5V. It can be programmed for other output voltages with two external resistors. An isolated version can be achieved with this topology as described further in Unitrode Application Note U-149.

OPERATION

With reference to the application diagram below, when input voltage is first applied, the current through RON into TON is directed to VCC where it charges the external capacitor, C3, connected to VCC. As voltage builds on VCC, an internal undervoltage lockout holds the circuit off and the output at DRIVE low until VCC reaches 8.4V. At this time, DRIVE goes high turning on the power switch, Q1, and redirecting the current into TON to the timing capacitor, CT. CT charges to a fixed threshold with a current $I_{CHG}=0.8 \bullet (V_{IN} - 4.5V)/R_{ON}$. Since DRIVE will only be high for as long as CT charges, the power switch on time will be inversely proportional to line voltage. This provides a constant (line voltage) • (switch on time) product.

TYPICAL APPLICATION



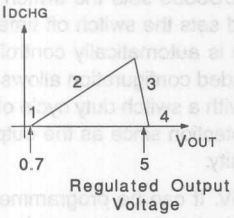
Note: This device incorporates patented technology used under license from Lambda Electronics, Inc.

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OPERATION (cont.)

At the end of the on time, Q1 is turned off and the current through RON is again diverted to VCC. Thus the current through RON, which charges CT during the on time, contributes to supplying power to the chip during the off time.

The power switch off time is controlled by the discharge of CT which, in turn, is programmed by the regulated output voltage. The relationship between CT discharge current, IDCHG, and output voltage is illustrated as follows:



Region 1. When VOUT = 0, the off time is infinite. This feature provides inherent short circuit protection. However, to ensure output voltage startup when the output is not a short, a high value resistor, RS, is placed in parallel with CT to establish a minimum switching frequency.

Region 2. As VOUT rises above approximately 0.7V to its regulated value, IDCHG is defined by ROFF, and is equal to:

$$I_{DCHG} = (V_{OUT} - 0.7V) / R_{OFF}$$

As VOUT increases, IDCHG increases reducing off time. The operating frequency increases and VOUT rises quickly to its regulated value.

Region 3. In this region, a transconductance amplifier reduces IDCHG in order to maintain a regulated VOUT.

Region 4. If VOUT should rise above its regulation range, IDCHG falls to zero and the circuit returns to the minimum frequency established by RS and CT.

The range of switching frequencies is established by RON, ROFF, RS, and CT as follows:

$$\text{Frequency} = 1/(T_{ON} + T_{OFF})$$

$$T_{ON} = R_{ON} \bullet C_T \bullet 4.6\,V/(V_{IN} - 4.5V)$$

$$T_{OFF}\,(\text{max}) = 1.4 \bullet R_S \bullet C_T$$

Regions 1 and 4

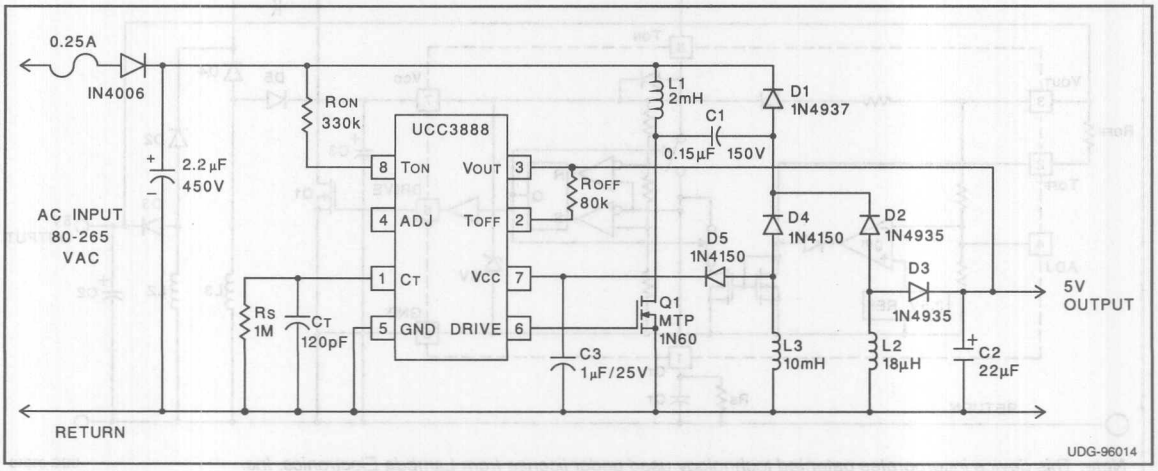
$$T_{OFF} = R_{OFF} \bullet C_T \bullet 3.7V\,/(V_{OUT} - 0.7V)$$

Region 2, excluding the effects of RS which have a minimal impact on TOFF.

The above equations assume that VCC equals 9V. The voltage at TON increases from approximately 2.5V to 6.5V while CT is charging. To take this into account, VIN is adjusted by 4.5V in the calculation of TON. The voltage at TOFF is approximately 0.7V.

DESIGN EXAMPLE

The UCC3888 regulates a 5 volt, 1 Watt nonisolated DC output from AC inputs between 80 and 265 volts. In this example, the IC is programmed to deliver a maximum on time gate drive pulse width of 2.2 microseconds which occurs at 80 VAC. The corresponding switching frequency is approximately 100kHz at low line, and overall efficiency is approximately 50%. Additional design information is available in Unitrode Application Note U-149.



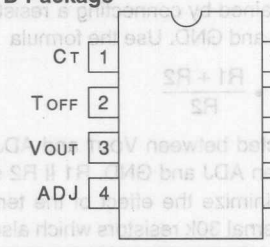
ABSOLUTE MAXIMUM RATINGS

Icc 8mA
Current into TON Pin 1.5mA
Voltage on VOUT Pin 20V
Current into TOFF Pin 250µA
Storage Temperature . . . . . -65°C to +150°C

Note: Unless otherwise indicated, voltages are referenced to ground and currents are positive into, negative out of, the specified terminals.

CONNECTION DIAGRAM

DIL-8, SOIC-8 (Top View)
N or J, D Package



ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications hold for TA = 0°C to 70°C for the UCC3888, -40°C to +85°C for the UCC2888, and -55°C to +125°C for the UCC1888. No load at DRIVE pin (CLOAD=0).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
General					
VCC Zener Voltage	ICC < 1.5mA	8.6	9.0	9.3	V
Startup Current	VOUT = 0		150	250	µA
Operating Current I(VCC)	VCC = VCC(zener) – 100mV, F = 150kHz		1.2	2.5	mA
Under-Voltage-Lockout					
Start Threshold	VOUT = 0	8.0	8.4	8.8	V
Minimum Operating Voltage after Start	VOUT = 0	6.0	6.3	6.6	V
Hysteresis	VOUT = 0	1.8			V
Oscillator					
Amplitude	VCC = 9V	3.5	3.7	3.9	V
CT to DRIVE high Propagation Delay	Overdrive = 0.2V		100	200	ns
CT to DRIVE low Propagation Delay	Overdrive = 0.2V		50	100	ns
Driver					
VOL	I = 20mA, VCC = 9V		0.15	0.4	V
	I = 100mA, VCC = 9V		0.7	1.8	V
VOH	I = –20mA, VCC = 9V	8.5	8.8		V
	I = –100mA, VCC = 9V	6.1	7.8		V
Rise Time	CLOAD = 1nF		35	70	ns
Fall Time	CLOAD = 1nF		30	60	ns
Line Voltage Detection					
Charge Coefficient: ICHG / I(TON)	VCT = 3V, DRIVE = High, I(TON) = 1mA	0.73	0.79	0.85	
Minimum Line Voltage for Fault	RON = 330k	60	80	100	V
Minimum Current I(TON) for Fault	RON = 330k		220		µA
On Time During Fault	CT = 150pF, VLINE = Min – 1V		2		µs
Oscillator Restart Delay after Fault			0.5		ms
VOUT Error Amp					
VOUT Regulated 5V (ADJ Open)	VCC = 9V, IDCHG = I(TOFF)/2	4.5	5.0	5.5	V
Discharge Ratio: IDCHG / I(TOFF)	I(TOFF) = 50µA	0.95	1.01	1.07	
Voltage at TOFF	I(TOFF) = 50µA	0.6	0.95	1.3	V
Regulation gm (Note 1)	Max IDCHG = 50µA		2.4		mA/V
	Max IDCHG = 125µA	1.9	4.1	7.0	mA/V

Note 1: gm is defined as $\frac{\Delta I_{DCHG}}{\Delta V_{OUT}}$ *for the values of VOUT when VOUT is in regulation. The two points used to calculate gm are for IDCHG at 65% and 35% of its maximum value.*

PIN DESCRIPTIONS

ADJ: The ADJ pin is used to provide a 5V regulated supply without additional external components. Other output voltages can be obtained by connecting a resistor divider between VOUT, ADJ and GND. Use the formula

$$V_{OUT} = 2.5V \bullet \frac{R1 + R2}{R2}$$

where R1 is connected between VOUT and ADJ, and R2 is connected between ADJ and GND. R1 II R2 should be less than 1kΩ to minimize the effect of the temperature coefficient of the internal 30k resistors which also connect to VOUT, ADJ, and GND. See Block Diagram.

CT (timing capacitor): The signal voltage at CT has a peak-to-peak swing of 3.7V for 9V VCC. As the voltage at CT crosses the oscillator upper threshold, DRIVE goes low. As the voltage on CT crosses the oscillator lower threshold, DRIVE goes high.

DRIVE: This output is a CMOS stage capable of sinking 200mA peak and sourcing 150mA peak. The output voltage swing is 0 to VCC.

GND (chip ground): All voltages are measured with respect to GND.

TOFF (regulated output control): TOFF sets the discharge current of the timing capacitor through an external resistor connected between VOUT and TOFF.

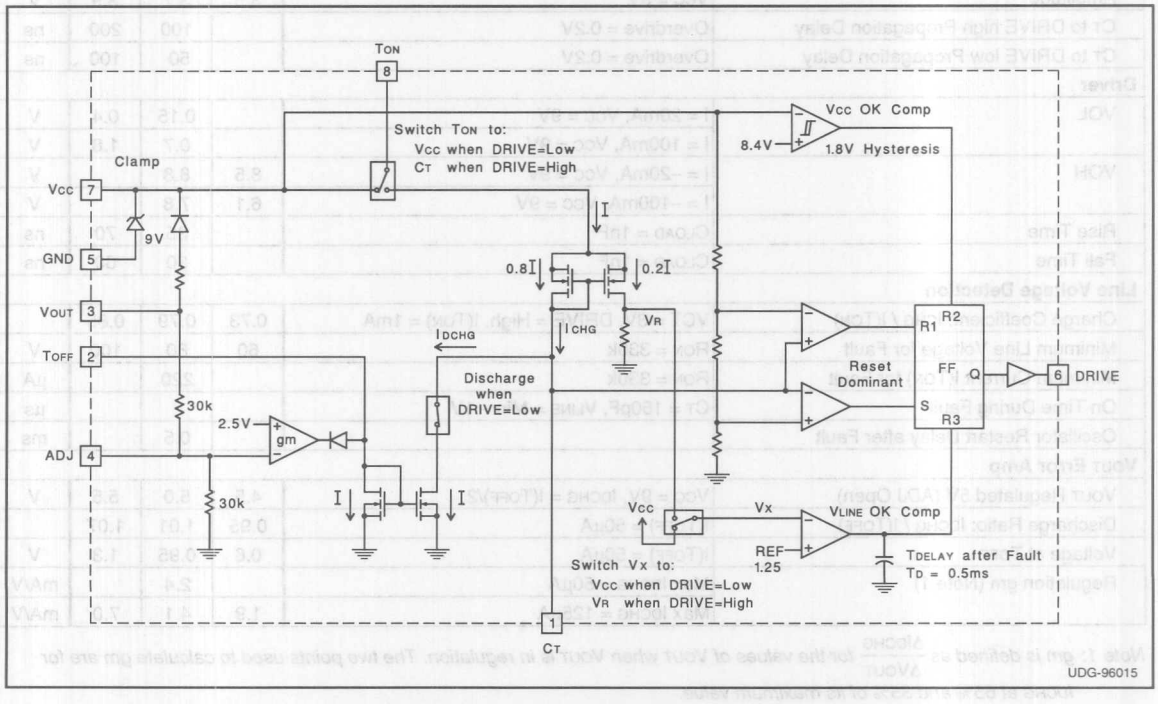
TON (line voltage control): TON serves three functions. When CT is discharging (off time), the current through TON is routed to VCC. When CT is charging (on time), the current through TON is split 80% to set the CT charge time and 20% to sense minimum line voltage which occurs for a TON current of 220µA. For a minimum line voltage of 80V, RON is 330kΩ.

The CT voltage slightly affects the value of the charge current during the on time. During this time, the voltage at the TON pin increases from 2.5V to 6.5V.

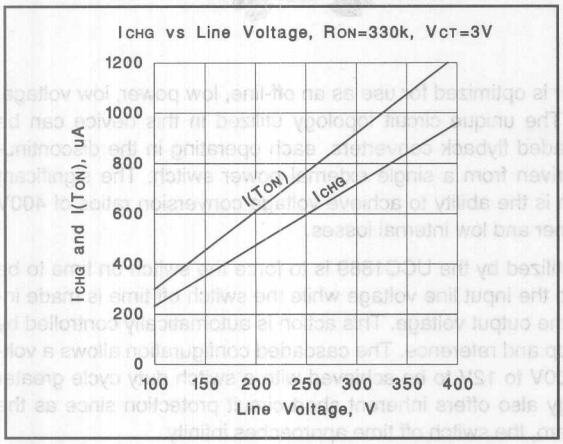
VCC (chip supply voltage): The supply voltage of the device at pin VCC is internally clamped at 9V. The device needs an external supply, from a source such as the rectified AC line or derived from the switching circuit. Precautions must be taken to ensure that total ICC does not exceed 8mA.

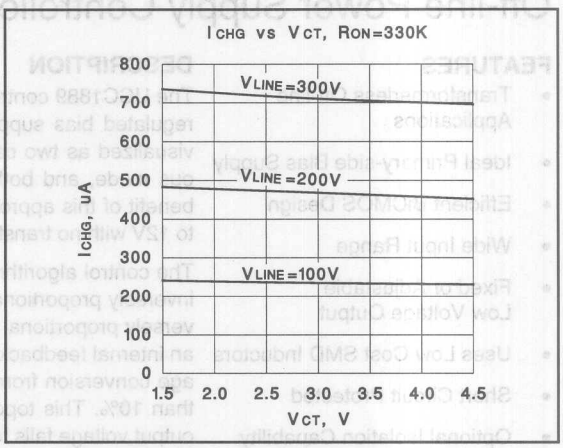
VOUT (regulated output): The VOUT pin is directly connected to the power supply output voltage. When VOUT is greater than VCC, VOUT bootstraps VCC.

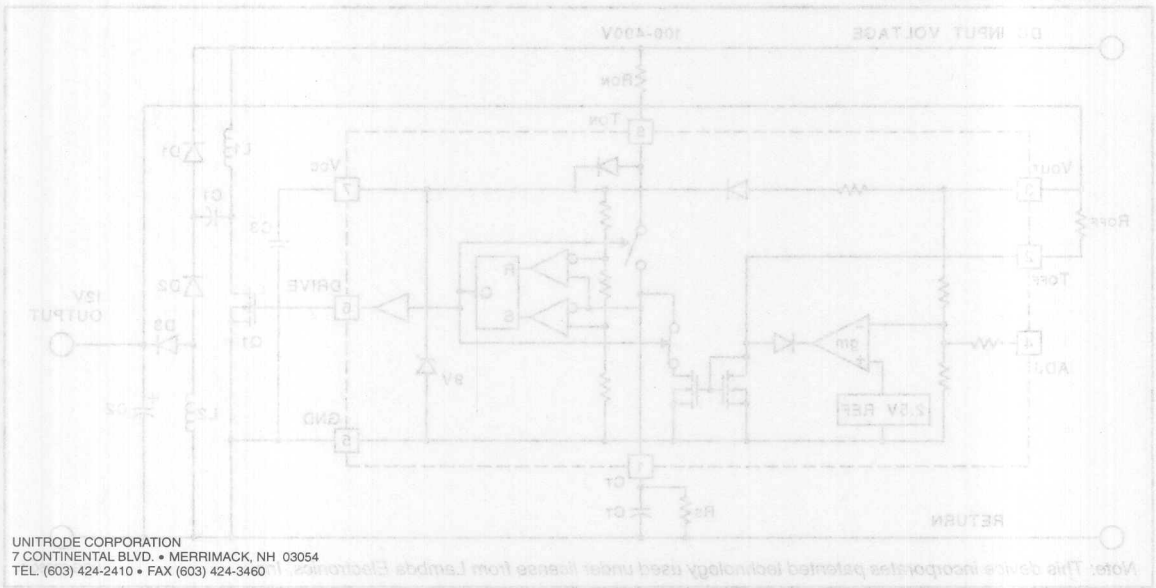
BLOCK DIAGRAM



TYPICAL CHARACTERISTICS CURVES







UNITRODE CORPORATION
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UNITRODE

UCC1889
UCC2889
UCC3889

Off-line Power Supply Controller

FEATURES

- Transformerless Off-line Applications
- Ideal Primary-side Bias Supply
- Efficient BiCMOS Design
- Wide Input Range
- Fixed or Adjustable Low Voltage Output
- Uses Low Cost SMD Inductors
- Short Circuit Protected
- Optional Isolation Capability

DESCRIPTION

The UCC1889 controller is optimized for use as an off-line, low power, low voltage, regulated bias supply. The unique circuit topology utilized in this device can be visualized as two cascaded flyback converters, each operating in the discontinuous mode, and both driven from a single external power switch. The significant benefit of this approach is the ability to achieve voltage conversion ratios of 400V to 12V with no transformer and low internal losses.

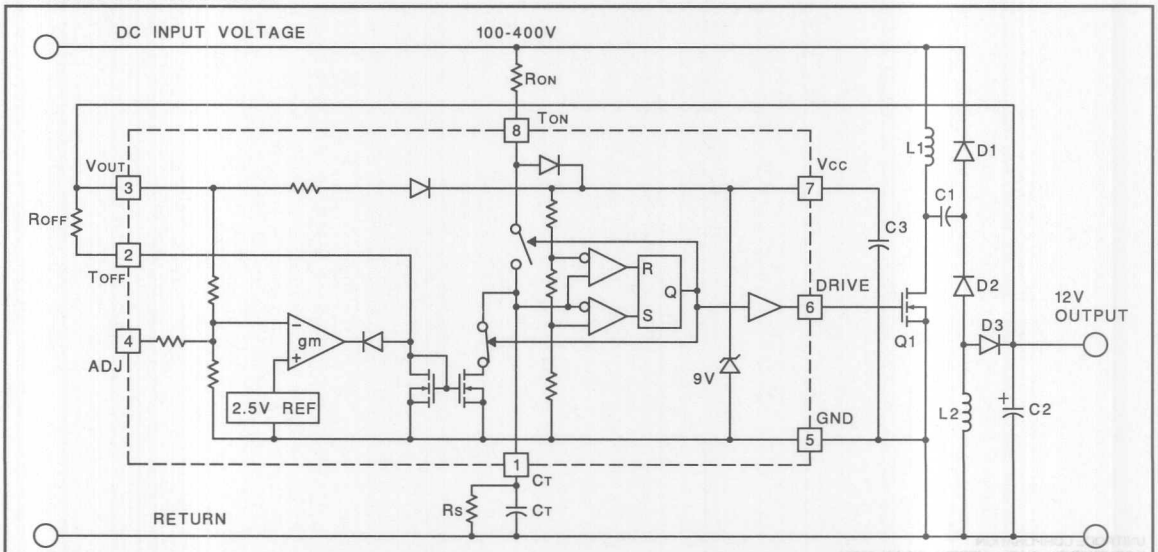
The control algorithm utilized by the UCC1889 is to force the switch on time to be inversely proportional to the input line voltage while the switch off time is made inversely proportional to the output voltage. This action is automatically controlled by an internal feedback loop and reference. The cascaded configuration allows a voltage conversion from 400V to 12V to be achieved with a switch duty cycle greater than 10%. This topology also offers inherent short circuit protection since as the output voltage falls to zero, the switch off time approaches infinity.

The output voltage can be easily set to 12V or 18V. Moreover, it can be programmed for other output voltages less than 18V with a few additional components. An isolated version can be achieved with this topology as described further in Unitrode Application Note U-149.

OPERATION

With reference to the application diagram below, when input voltage is first applied, the RON current into TON is directed to VCC where it charges the external capacitor, C3, connected to VCC. As voltage builds on VCC, an internal undervoltage lockout holds the circuit off and the output at DRIVE low until VCC reaches 8.4V. At this time, DRIVE goes high turning on the power switch, Q1, and redirecting the current into TON to the timing capacitor, CT. CT charges to a fixed threshold with a current $I_{CHG}=0.8 \bullet (V_{IN} - 4.5V)/R_{ON}$. Since DRIVE will only be high for as long as CT charges, the power switch on time will be inversely proportional to line voltage. This provides a constant line voltage-switch on time product.

TYPICAL APPLICATION



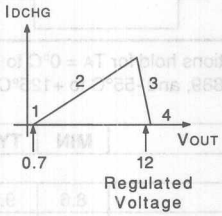
Note: This device incorporates patented technology used under license from Lambda Electronics, Inc.

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OPERATION (cont.)

At the end of the on time, Q1 is turned off and the RON current into TON is again diverted to VCC. Thus the current through RON, which charges CT during the on time, contributes to supplying control power during the off time.

The power switch off time is controlled by the discharge of CT which, in turn, is programmed by the regulated output voltage. The relationship between CT discharge current, IDCHG, and output voltage is illustrated as follows:



1. When VOUT = 0, the off time is infinite. This feature provides inherent short circuit protection. However, to ensure output voltage startup when the output is not a short, a high value resistor, RS, is placed in parallel with CT to establish a minimum switching frequency.
2. As VOUT rises above approximately 0.7V to its regulated value, IDCHG is defined by ROFF, and therefore is equal to:

$$I_{DCHG} = (V_{OUT} - 0.7V) / R_{OFF}$$

As VOUT increases, IDCHG increases resulting in the reduction of off time. The frequency of operation increases and VOUT rises quickly to its regulated value.

3. In this region, a transconductance amplifier reduces IDCHG in order to maintain VOUT in regulation.
4. If VOUT should rise above its regulation range, IDCHG falls to zero and the circuit returns to the minimum frequency established by RS and CT.

The range of switching frequencies is established by RON, ROFF, RS, and CT as follows:

$$Frequency = 1/(T_{ON} + T_{OFF})$$

$$T_{ON} = R_{ON} \bullet C_T \bullet 4.6\,V/(V_{IN} - 4.5V)$$

$$T_{OFF}\ (max) = 1.4 \bullet R_S \bullet C_T$$

Regions 1 and 4

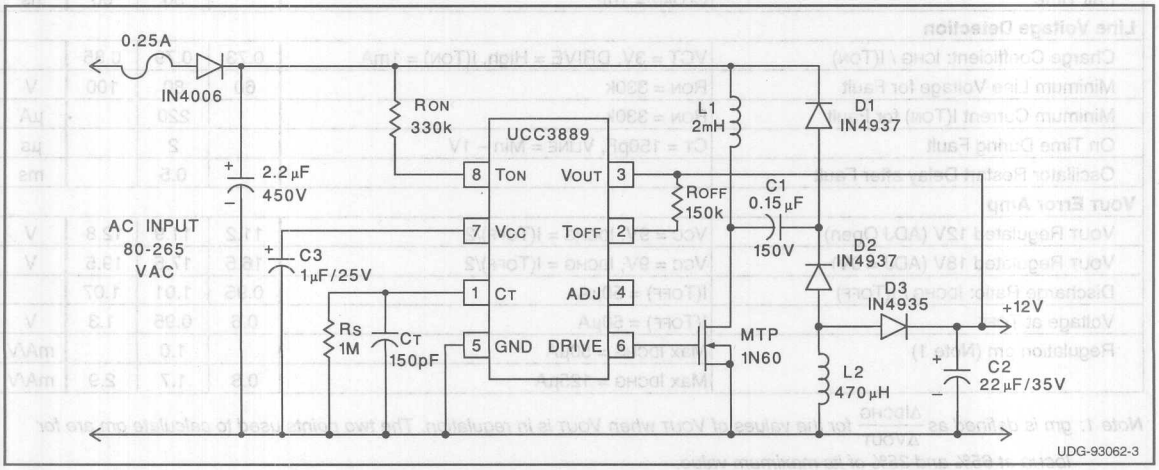
$$T_{OFF} = R_{OFF} \bullet C_T \bullet 3.7V\ /(V_{OUT} - 0.7V)$$

Region 2, excluding the effects of RS which have a minimal impact on TOFF.

The above equations assume that VCC equals 9V. The voltage at TON increases from approximately 2.5V to 6.5V while CT is charging. To take this into account, VIN is adjusted by 4.5V in the calculation of TON. The voltage at TOFF is approximately 0.7V.

DESIGN EXAMPLE

The UCC3889 regulates a 12 volt, 1 Watt nonisolated DC output from AC inputs between 80 and 265 volts. In this example, the IC is programmed to deliver a maximum on time gate drive pulse width of 2.4 microseconds which occurs at 80 VAC. The corresponding switching frequency is approximately 100kHz at low line, and overall efficiency is approximately 50%. Additional design information is available in Unitrode Application Note U-149.



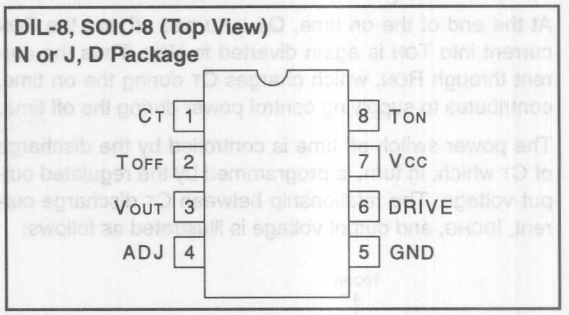
ABSOLUTE MAXIMUM RATINGS

Icc 5mA
Current into Ton Pin 1.5mA
Voltage on Vout Pin 20V
Current into Toff Pin 250µA
Storage Temperature ..... -65°C to +150°C

Note: Unless otherwise indicated, voltages are referenced to ground and currents are positive into, negative out of, the specified terminals.

CONNECTION DIAGRAM

DIL-8, SOIC-8 (Top View)
N or J, D Package



ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications hold for TA = 0°C to 70°C for the UCC3889, -40°C to +85°C for the UCC2889, and -55°C to +125°C for the UCC1889. No load at DRIVE pin (CLOAD=0).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
General					
Vcc Zener Voltage	Icc < 1.5mA	8.6	9.0	9.3	V
Startup Current	Vout = 0		150	250	µA
Operating Current I(Vout)	Vout = 11V, F = 150kHz		1.2	2.5	mA
Under-Voltage-Lockout					
Start Threshold	Vout = 0	8.0	8.4	8.8	V
Minimum Operating Voltage after Start	Vout = 0	6.0	6.3	6.6	V
Hysteresis	Vout = 0	1.8			V
Oscillator					
Amplitude	Vcc = 9V	3.5	3.7	3.9	V
CT to DRIVE high Propagation Delay	Overdrive = 0.2V		100	200	ns
CT to DRIVE low Propagation Delay	Overdrive = 0.2V		50	100	ns
Driver					
VOL	I = 20mA, Vcc = 9V		0.15	0.4	V
	I = 100mA, Vcc = 9V		0.7	1.8	V
VOH	I = –20mA, Vcc = 9V	8.5	8.8		V
	I = –100mA, Vcc = 9V	6.1	7.8		V
Rise Time	CLOAD = 1nF		35	70	ns
Fall Time	CLOAD = 1nF		30	60	ns
Line Voltage Detection					
Charge Coefficient: Ichg / I(Ton)	VCT = 3V, DRIVE = High, I(Ton) = 1mA	0.73	0.79	0.85	
Minimum Line Voltage for Fault	Ron = 330k	60	80	100	V
Minimum Current I(Ton) for Fault	Ron = 330k		220		µA
On Time During Fault	CT = 150pF, VLINE = Min – 1V		2		µs
Oscillator Restart Delay after Fault			0.5		ms
Vout Error Amp					
Vout Regulated 12V (ADJ Open)	Vcc = 9V, Idchg = I(Toff)/2	11.2	11.9	12.8	V
Vout Regulated 18V (ADJ = 0V)	Vcc = 9V, Idchg = I(Toff)/2	16.5	17.5	19.5	V
Discharge Ratio: Idchg / I(Toff)	I(Toff) = 50µA	0.95	1.01	1.07	
Voltage at Toff	I(Toff) = 50µA	0.6	0.95	1.3	V
Regulation gm (Note 1)	Max Idchg = 50µA		1.0		mA/V
	Max Idchg = 125µA	0.8	1.7	2.9	mA/V

Note 1: gm is defined as $\frac{\Delta I_{DCHG}}{\Delta V_{OUT}}$ *for the values of Vout when Vout is in regulation. The two points used to calculate gm are for Idchg at 65% and 35% of its maximum value.*

PIN DESCRIPTIONS

ADJ: The ADJ pin is used to provide a 12V or an 18V regulated supply without additional external components. To select the 12V option, ADJ pin is left open. To select the 18V option, ADJ pin must be grounded. For other output voltages less than 18V, a resistor divider between VOUT, ADJ and GND is needed. Note, however, that for output voltages less than VCC, the device needs additional bootstrapping to VCC from an external source such as the line voltage. If so, precautions must be taken to ensure that total ICC does not exceed 5mA.

CT (timing capacitor): The signal voltage across CT has a peak-to-peak swing of 3.7V for 9V VCC. As the voltage on CT crosses the oscillator upper threshold, DRIVE goes low. As the voltage on CT crosses the oscillator lower threshold, DRIVE goes high.

DRIVE: This output is a CMOS stage capable of sinking 200mA peak and sourcing 150mA peak. The output voltage swing is 0 to VCC.

GND (chip ground): All voltages are measured with respect to GND.

TOFF (regulated output control): TOFF sets the discharge current of the timing capacitor through an external resistor connected between VOUT and TOFF.

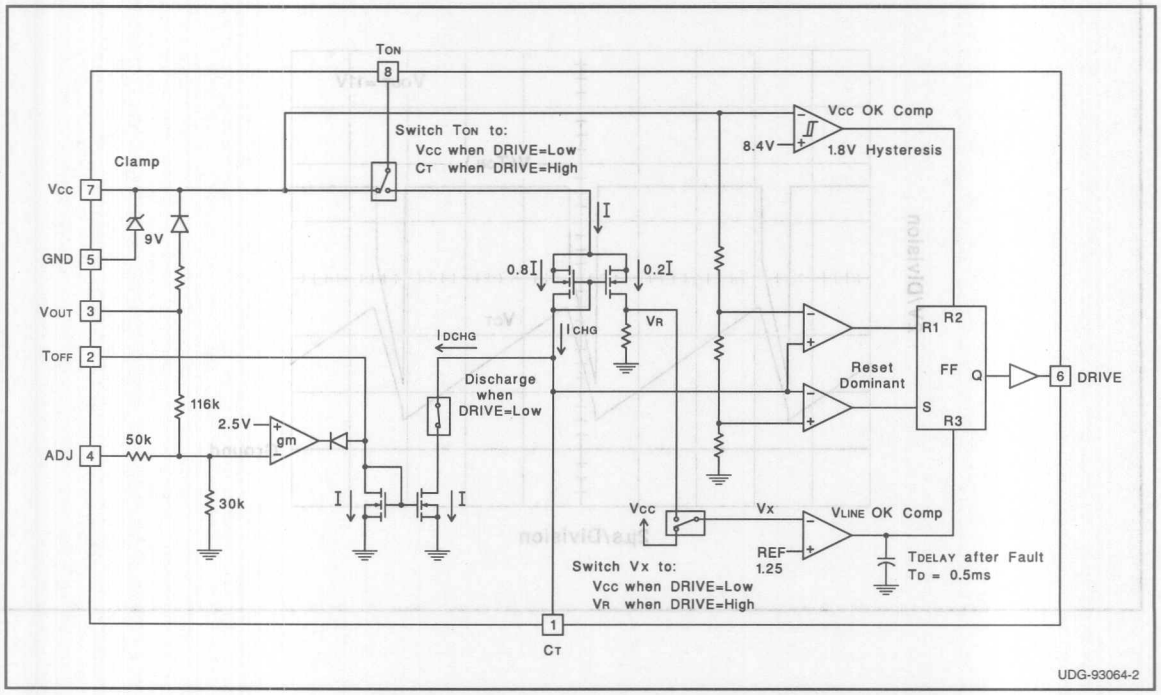
TON (line voltage control): TON serves three functions. When CT is discharging (off time), the current through TON is routed to VCC. When CT is charging (on time), the current through TON is split 80% to set the CT charge time and 20% to sense minimum line voltage which occurs for a TON current of 220µA. For a minimum line voltage of 80V, RON is 330kΩ.

The CT voltage slightly affects the value of the charge current during the on time. During this time, the voltage at the TON pin increases from approximately 2.5V to 6.5V.

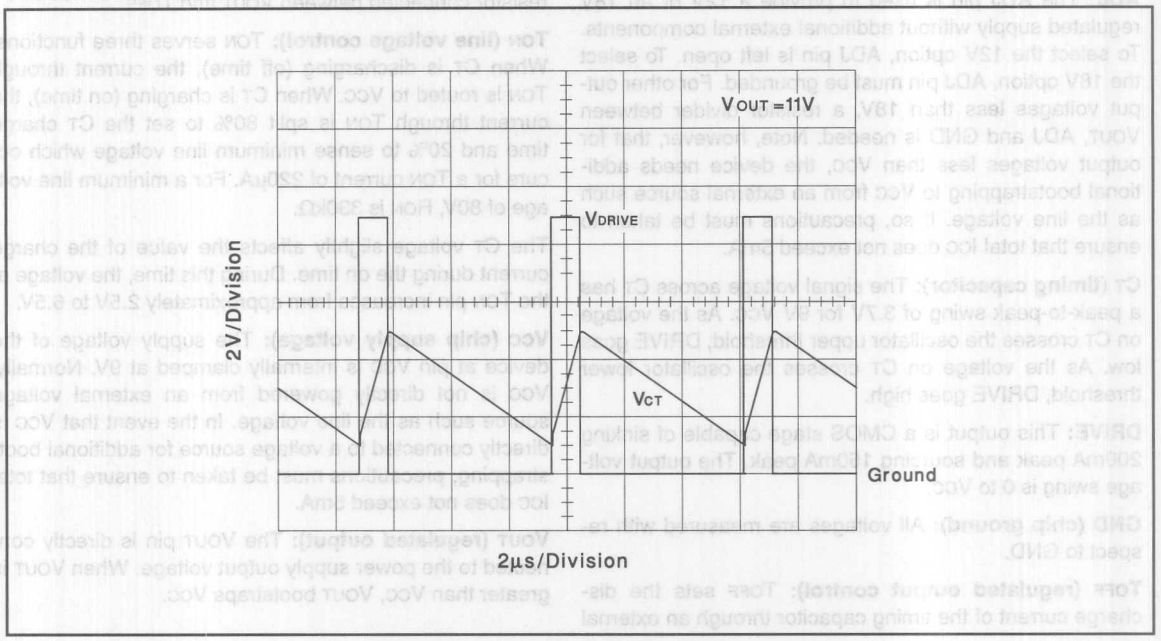
VCC (chip supply voltage): The supply voltage of the device at pin VCC is internally clamped at 9V. Normally, VCC is not directly powered from an external voltage source such as the line voltage. In the event that VCC is directly connected to a voltage source for additional bootstrapping, precautions must be taken to ensure that total ICC does not exceed 5mA.

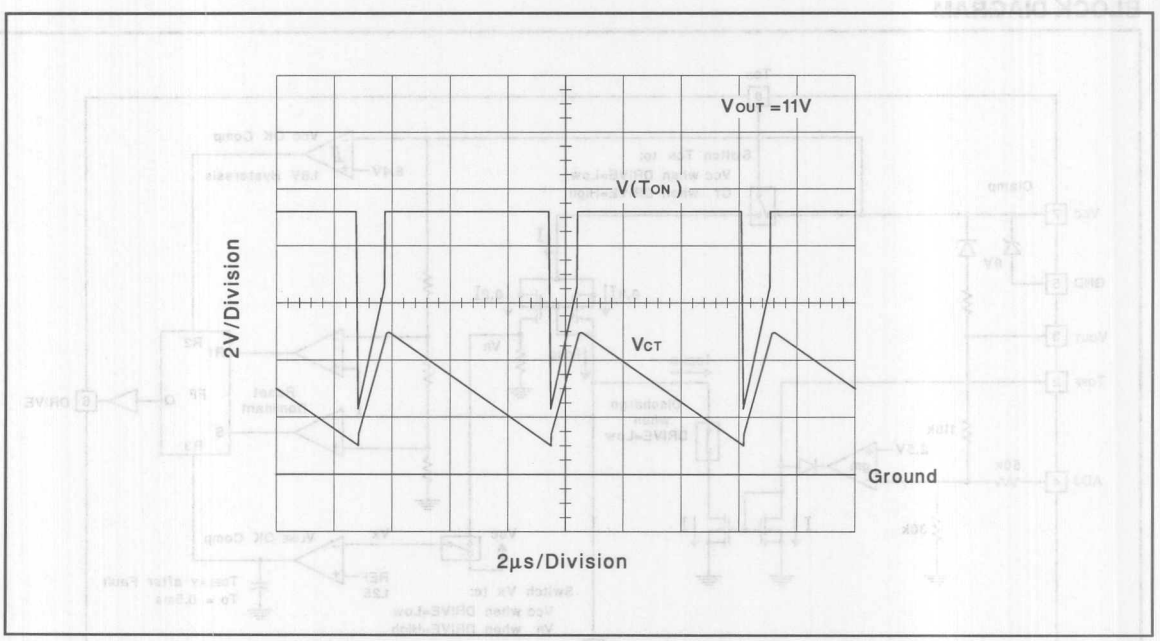
VOUT (regulated output): The VOUT pin is directly connected to the power supply output voltage. When VOUT is greater than VCC, VOUT bootstraps VCC.

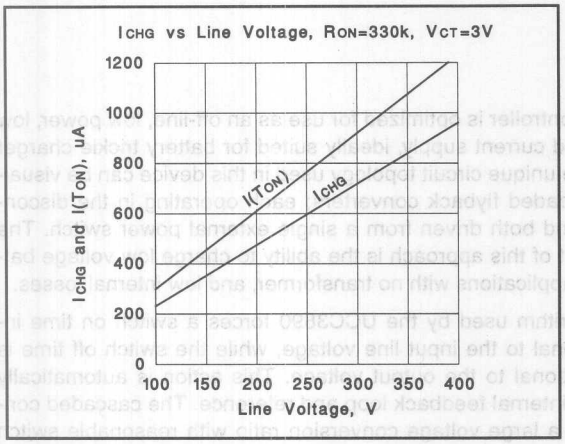
BLOCK DIAGRAM

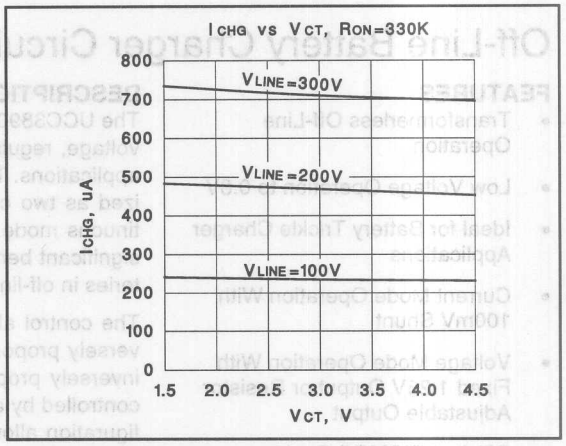


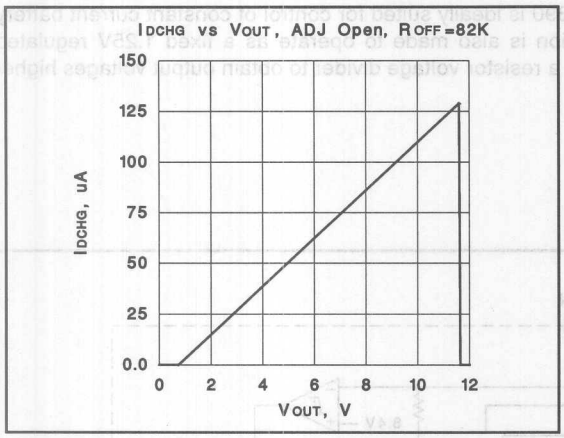
TYPICAL WAVEFORMS

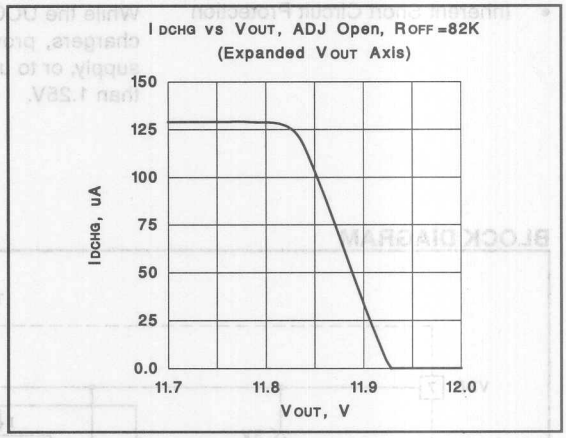


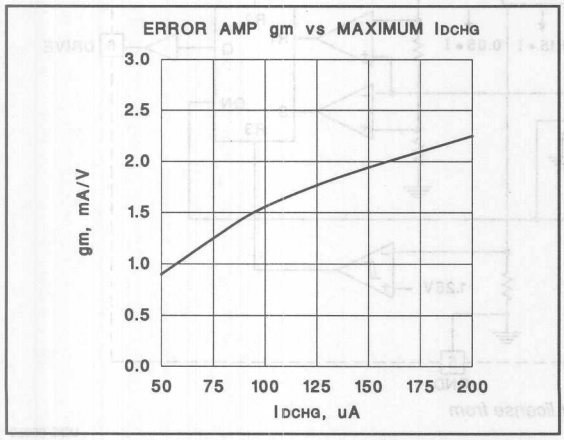


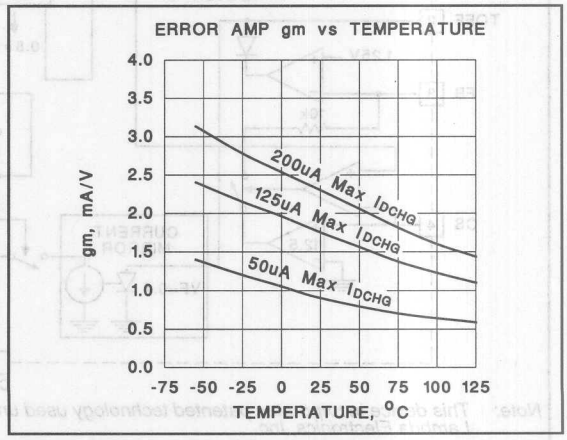












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Off-Line Battery Charger Circuit

FEATURES

- Transformerless Off-Line Operation
- Low Voltage Operation to 0.8V
- Ideal for Battery Trickle Charger Applications
- Current Mode Operation With 100mV Shunt
- Voltage Mode Operation With Fixed 1.25V Output or Resistor Adjustable Output
- Efficient BiCMOS Design
- Inherent Short Circuit Protection

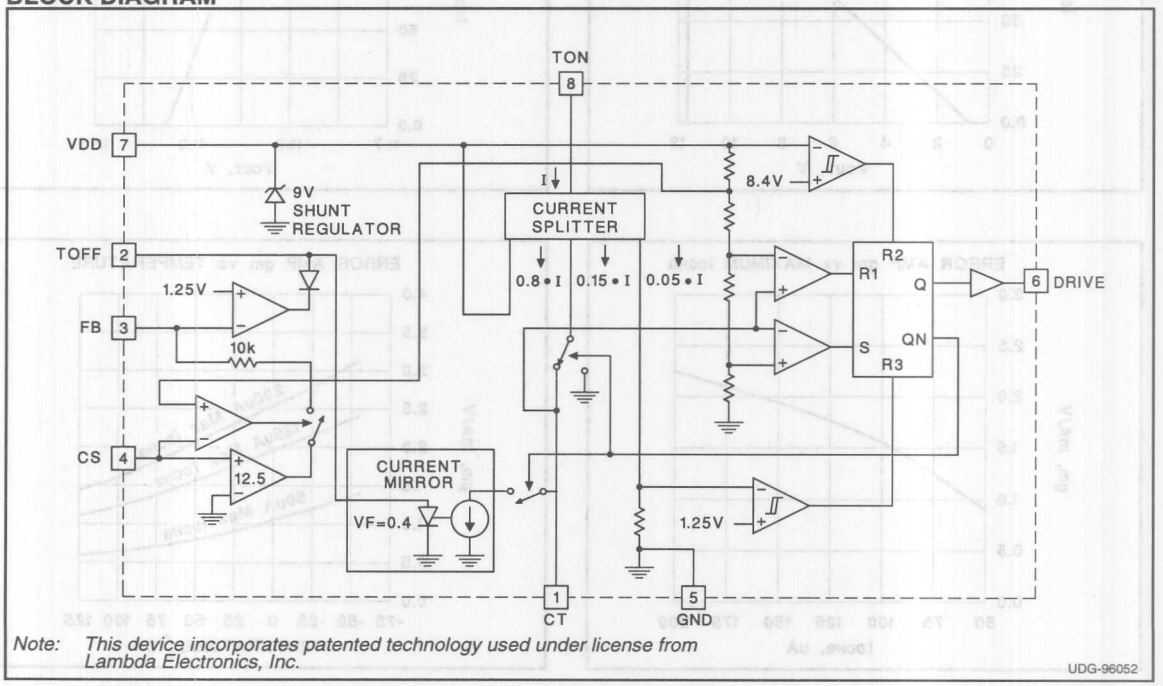
DESCRIPTION

The UCC3890 controller is optimized for use as an off-line, low power, low voltage, regulated current supply, ideally suited for battery trickle charger applications. The unique circuit topology used in this device can be visualized as two cascaded flyback converters; each operating in the discontinuous mode, and both driven from a single external power switch. The significant benefit of this approach is the ability to charge low voltage batteries in off-line applications with no transformer, and low internal losses.

The control algorithm used by the UCC3890 forces a switch on time inversely proportional to the input line voltage, while the switch off time is inversely proportional to the output voltage. This action is automatically controlled by an internal feedback loop and reference. The cascaded configuration allows a large voltage conversion ratio with reasonable switch duty cycle.

While the UCC3890 is ideally suited for control of constant current battery chargers, provision is also made to operate as a fixed 1.25V regulated supply, or to use a resistor voltage divider to obtain output voltages higher than 1.25V.

BLOCK DIAGRAM



Note: This device incorporates patented technology used under license from Lambda Electronics, Inc.

UDG-96052

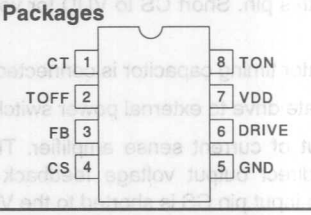
ABSOLUTE MAXIMUM RATINGS

IDD 7.5mA
Current into TON 7.5mA
Voltage on VOUT 20V
Current into TOFF 250µA
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAMS

DIL-8, SOIC-8 (Top View)
J, N, or D Packages



ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for TA = –55°C to 125°C for UCC1890, –40°C to 85°C for the UCC2890, and 0°C to 70°C for the UCC3890. No load at DRIVE pin (CLOAD = 0), TA = TJ.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
General					
VDD Zener Voltage	IDD = 4.75mA, ITON = 0mA	8.3	9.0	9.4	V
Minimum Operating Current ITON	IDD = –1mA, F = 150kHz		1.65	2.0	mA
Undervoltage Lockout					
Minimum Voltage to Start	FB = 0	7.8	8.6	9.2	V
Minimum Voltage after Start	FB = 0	5.75	6.3	6.65	V
Hysteresis	FB = 0	1.8	2.3	2.6	V
VDD – VSTART	FB = 0	0.2	0.4	0.7	V
Oscillator					
Amplitude	ITON = 3mA; ITOFF = 50µA; VFB = 0V CT = 100pF	3.1	3.4	3.7	V
CT to DRIVE High Delay	Overdrive = 200mV		80	200	ns
CT to DRIVE Low Delay	Overdrive = 200mV		50	100	ns
Charge Coefficient ICT/ITON	ITON = 3mA; VCT = 3.0V	0.135	0.15	0.165	µA/µA
Discharge Coefficent ICT/ITOFF	ITOFF = 50µA; VCT = 3.0V	0.95	1.00	1.05	µA/µA
Driver					
VOL	I = 100mA (Note 1)		0.7	1.8	V
VOH	I = –100mA referred to VDD (Note 1)	–2.9	–1.5		V
Rise Time	CL = 1nF		35	70	ns
Fall Time	CL = 1nF		30	60	ns
Line Voltage Detection					
Minimum ITON for Fault		1.0	1.5	2.0	mA
ITON Detector Hysteresis			110		µA
On Time During Fault			0.5		µs
VOUT Error Amplifier					
Reference Level	ITOFF = 50µA, ICT = 25µA, TJ = 25°C	1.20	1.25	1.30	V
	ITOFF = 50µA, ICT = 25µA, Over Temperature	1.15	1.25	1.35	V
Voltage at TOFF	ITOFF = 50µA	0.3	0.4	0.5	V
Regulation gm	ITOFF = 50µA (Note 2)	2.0	4.0	7.7	mA/V
Current Sense Amplifier					
Gain	VCS = 90 – 110mV	11.8	12.5	13.0	V/V
Input Offset Voltage	VCS = 90 – 110mV	–5	0	5	mV
Input Voltage for CS Amplifier Enabled	ITON = 3mA, Referred to VDD	–1.5	–0.8		V
Input Voltage for CS Amplifier Disabled	ITON = 3mA, Referred to VDD		–0.8	–0.3	V

Note 1: VDD forced to 100mV below VDD Zener Voltage

Note 2: gm is defined as $\frac{\Delta I_{CT}}{\Delta V_{FB}}$ *for the values of VFB where the error amp is in regulation. The two points used to calculate gm are for ICT at 65% amd 35% of its maximum value.*

PIN DESCRIPTIONS

CS: The high side of the current sense shunt is connected to this pin. Short CS to VDD for voltage feedback operation.

CT: Oscillator timing capacitor is connected to this pin.

DRIVE: Gate drive to external power switch.

FB: Output of current sense amplifier. This pin can be used for direct output voltage feedback if the current sense amp input pin CS is shorted to the VDD pin.

GND: Ground pin.

TOFF: Resistor ROFF connects from voltage output to this pin to provide a maximum capacitor discharge current proportional to output voltage.

TON: Resistor RON connects from line input to this pin to provide capacitor charge current proportional to line voltage. The current in RON also provides power for the 9V shunt regulator at VDD.

VDD: Output of 9V shunt regulator.

APPLICATION INFORMATION

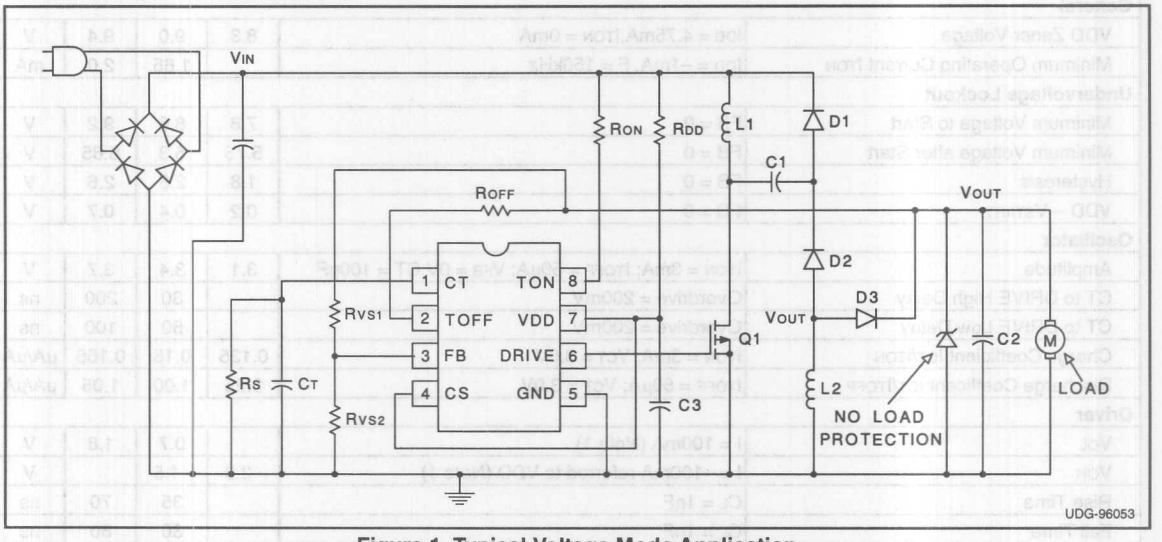


Figure 1. Typical Voltage Mode Application

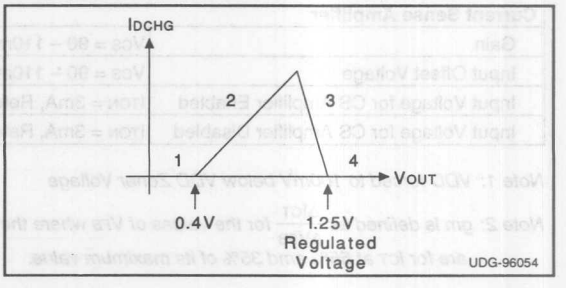
OPERATION (VOLTAGE OUTPUT)

Figure 1 shows a typical voltage mode application. When input voltage is first applied, all of the current through RDD and 80% of the current through RON, charge the external capacitor C3 connected to VDD. As the voltage builds on VDD, undervoltage lockout holds the circuit off and the output DRIVE low until VDD reaches 8.4V. At this time, DRIVE goes high, turning on the external power switch Q1, and 15% of the current into TON is directed to the timing capacitor CT. The voltage at TON is fixed at approximately 11V, so CT charges to a fixed threshold with current

$$I = 0.2 \bullet \frac{V_{IN} - 11V}{R_{ON}}$$

Since the input line is much greater than 11V, the charge current is approximately proportional to the input line voltage. DRIVE is only high while CT is charging, so the power switch on time is inversely proportional to line voltage. This provides a constant line voltage-switch on time product.

At the end of the switch on time, Q1 is turned off, and the 15% of the RON current which was charging CT is diverted to ground. The power switch off time is controlled by discharge of CT, which is determined by the outut voltage as described here:



APPLICATION INFORMATION (cont.)

1. When VOUT = 0, the off time is infinite. This feature provides inherent short circuit protection. However, to ensure output voltage startup when the output is not a short, a high value resistor, RS, is placed in parallel with CT to establish a minimum switching frequency.
2. As VOUT rises above approximately 0.4V, IDCHG is set by ROFF, and is defined by

$$I_{DCHG} = \frac{V_{OUT} - 0.4V}{R_{OFF}}$$

   As VOUT increases, IDCHG increases resulting in the reduction of off time. The frequency of operation increases and VOUT rises quickly to its regulated value.
3. In this region, a transconductance amplifier reduces IDCHG in order to maintain VOUT in regulation. The input to the transconductance amplifier is the pin FB. (In this mode the pin CS should be shorted to VDD.) FB can either be connected directly to VOUT to regulate at nominal VOUT = 1.25V or to be connected to VOUT through a resistor divider RVS1/RVS2 to regulate at nominal

$$V_{OUT} = \frac{1.25V \bullet (R_{VS1} + R_{VS2})}{R_{VS2}}$$

4. If VOUT should rise above its regulation range, IDCHG falls to zero and the circuit returns to the minimum frequency established by RS and CT.

   The range of switching frequencies is established by RON, ROFF, RS, and CT as follows:

$$\text{Frequency} = \frac{1}{TON + TOFF}$$

$$TON = \frac{CT \bullet 3.4V \bullet 0.15 \bullet R_{ON}}{V_{IN} - 11V}$$

$$TOFF_{(MAX)} = 1.5 \bullet R_S \bullet C_T \text{ (regions1 and 4)}$$

$$TOFF = \frac{C_T \bullet 3.4V \bullet R_{OFF}}{V_{OUT} - 0.4V} \text{ (region 2)}$$

The above equations assume VDD = 9, the voltage at TON = 11V, the voltage at TOFF = 0.4V.

OPERATION (CURRENT OUTPUT)

Figure 2 shows a typical current mode application. In current mode, operation is the same as in voltage mode, except that in region 3 the transconductance amplifier is controlled by the current sense amplifier which senses the voltage across a shunt resistor RSH. The circuit then regulates the current in the shunt to the nominal value

$$I_{SH} = \frac{100mV}{R_{SH}}$$

The circuit shown in this schematic would be suitable for an application which trickle charges a battery at a low current, (e.g. C/10), and has a battery load which draws a high current, (e.g. C), when turned on. In that case, RSH1 value is chosen so that

$$\frac{100mV}{R_{SH1}} = \frac{C}{10}$$

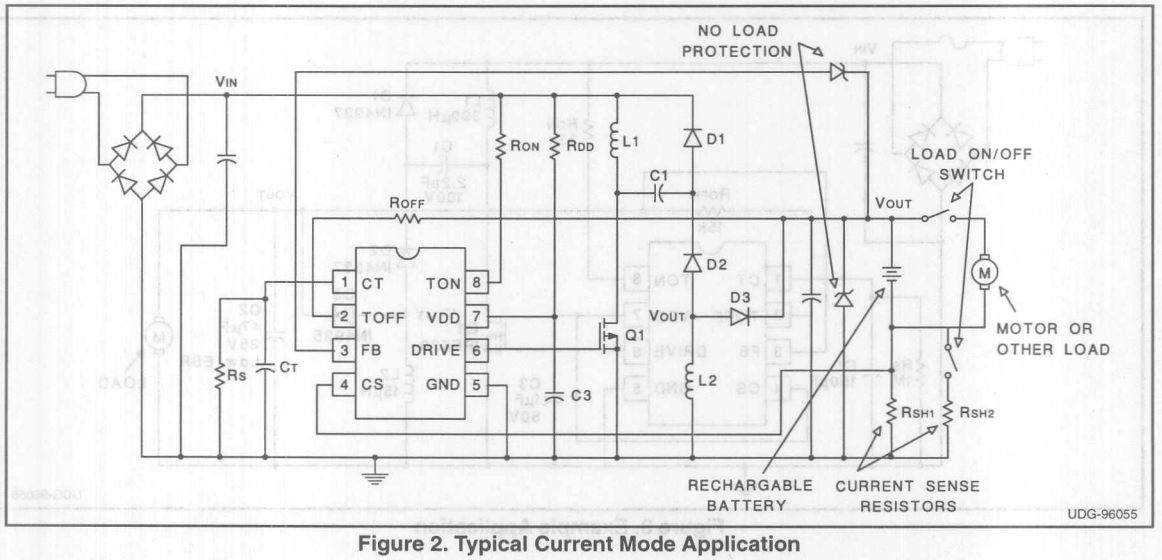


Figure 2. Typical Current Mode Application

APPLICATION INFORMATION (cont.)

If R_{SH2} is chosen so that

$$\frac{100mV}{R_{SH2}} = C$$

then the regulator output will assist the battery, minimizing or eliminating battery output current.

DESIGN EXAMPLE

A typical design has the following requirements:

V_{IN}	=	80 to 132 VAC or 100 to 180 VDC
V_{OUT}	=	1.25V
V_{OUT}'	=	2.0V (assumes 1.25 V_{OUT} with 750mV forward drop in D3)
I_{LOAD}	=	500mADC max
$F_{SWITCHING}$	=	100kHz
η (eff.)	=	50% (excluding efficiency losses in D3 which will be very large due to the low output voltage. Losses in D3 are accounted for by using V_{OUT}' in the calculations).

Component values are indicated in Figure 3. The explanation for the choices in component values follows.

First calculate the maximum duty cycle, d(max). To calculate this assume that at maximum load/minimum line conditions, the converter will be at the continuous conduction boundary and there will be no idle time after the inductors are discharged. For all other load/line conditions, the UCC3890 will stretch the off time, to create an idle time after the inductors are discharged, in order to maintain a constant output voltage. For a single flyback stage at continuous conduction boundary

$$d = \frac{1}{1 + \frac{V_{IN}}{V_{OUT}}}$$

For the cascaded flyback stages of the UCC3890 topology, the corresponding equation is

$$d(max) = \frac{1}{1 + \sqrt{\frac{V_{IN}}{V_{OUT}'}}}$$

in this case

$$d(max) = \frac{1}{1 + \sqrt{\frac{100V}{2V}}} = 0.125$$

Next using the operating frequency and the maximum duty cycle to calculate the maximum on time

$$TON(max) = \frac{d(max)}{F_{SWITCHING}}$$

in this case

$$TON(max) = \frac{0.125}{100kHz} = 1.25\mu s$$

correspondingly

$$TOFF(min) = \frac{1 - 0.125}{100kHz} = 8.75\mu s$$

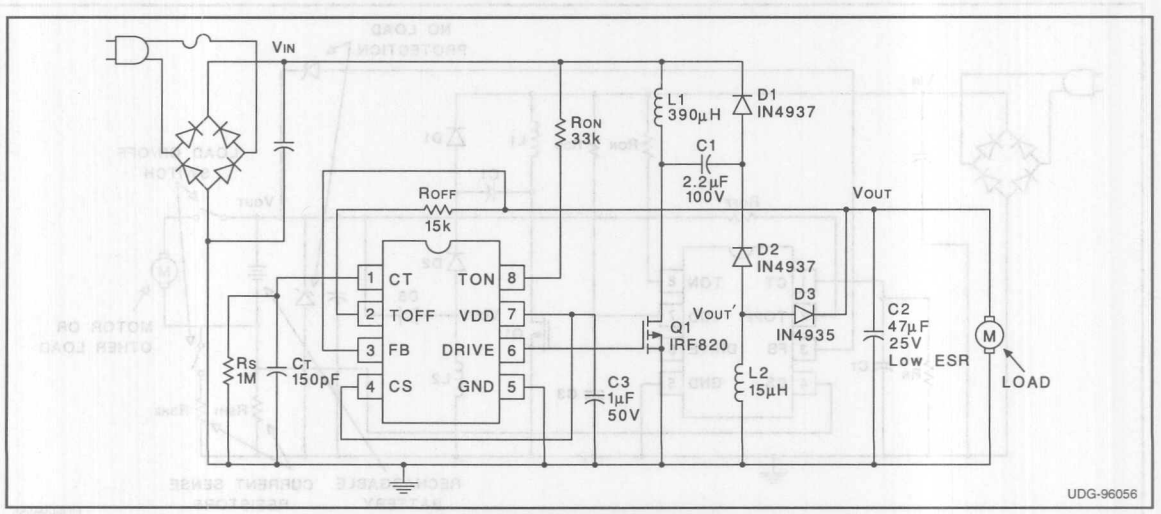


Figure 3. Example Application

APPLICATION INFORMATION (cont.)

The average input current at minimum line and maximum load will be

$$I_{IN} = \frac{I_{OUT}}{\eta} \bullet \frac{V_{OUT'}}{V_{IN}}$$

in this case

$$I_{IN} = \frac{500mA}{0.5} \bullet \frac{2V}{100V} = 20mA$$

Knowing that input current is drawn from the line only during TON, calculate the peak current in L1 to be

$$I_{L1}(pk) = 2 \bullet I_{IN} \bullet \frac{TON + TOFF}{TON}$$

in this case

$$I_{L1}(pk) = 2 \bullet 20mA \bullet \frac{1.25\mu s + 8.75\mu s}{1.25\mu s} = 320mA$$

Now calculate the value for L1

$$L_1 = V_{IN} \bullet \frac{TON}{I_{L1}(pk)}$$

in this case

$$L_1 = 100V \bullet \frac{1.25\mu s}{320mA} = 390\mu H$$

The output voltage of the first flyback stage is

$$V_{C1} = V_{IN} \bullet \frac{TON}{TOFF}$$

in this case

$$V_{C1} = 100V \bullet \frac{1.25\mu s}{8.75\mu s} = 14.3V$$

Knowing that output current is provided to the load only during TOFF, calculate the peak current in L2 to be

$$I_{L2}(pk) = 2 \bullet I_{OUT} \bullet \frac{TON + TOFF}{TOFF}$$

in this case

$$I_{L2}(pk) = 2 \bullet 0.5A \bullet \frac{1.25\mu s + 8.75\mu s}{8.75\mu s} = 1.14A$$

Now calculate the value of L2

$$L_2 = V_{OUT'} \bullet \frac{TOFF}{I_{L2}(pk)}$$

in this case

$$L_2 = 2V \bullet \frac{8.75\mu s}{1.14A} = 15\mu H$$

For all of the calculations so far only the maximum load/minimum line condition have been considered. The entire range of operation must be considered to choose values for the rest of the components.

Under all normal operating conditions the current ITON, (which is the current in RON), should be greater than 2mA and less than 7.5mA. In this case set RON to give ITON = 2.8mA at low line. The voltage at TON will be about 11V so

$$R_{ON} = \frac{100V - 11V}{2.8mA} = 33k\Omega$$

With RON = 33k, ITON at high line will be

$$I_{TON} = \frac{180V - 11V}{33k} = 5.1mA$$

At high line, the power dissipation in RON will be

$$P(R_{ON}) = (180V - 11V) \bullet 5.1mA = 860mW$$

RON will need to be at least a 1W resistor. Alternately it could be four 1/4W 8.2kΩ resistors in series.

Once RON is set, CT can be chosen. The charge current for CT is nominally 15% of ITON, and the nominal oscillator amplitude is 3.4V, so

$$TON = \frac{CT \bullet 3.4V}{0.15 \bullet I_{TON}}$$

solving for CT

$$CT = \frac{TON \bullet 0.15 \bullet I_{TON}}{3.4V}$$

ITON at low line is 2.8mA, and the target TON at low line is 1.25µs, so in this case

$$CT = \frac{1.25\mu s \bullet 0.15 \bullet 2.8mA}{3.4V} = 150pF$$

The final component to be chosen is ROFF, which determines the minimum value of TOFF. When the output voltage is below the regulation point, the discharge current for CT is equal to ITOFF (the current in ROFF). Under that condition

$$TOFF = \frac{CT \bullet 3.4V}{I_{TOFF}}$$

since the voltage at the TOFF pin = 0.4V

$$I_{TOFF} = \frac{V_{OUT} - 0.4V}{R_{OFF}}$$

substituting and solving for ROFF

$$R_{OFF} = \frac{T_{OFF} \bullet (V_{OUT} - 0.4V)}{CT \bullet 3.4V}$$

The largest discharge current, and hence the minimum off time, will occur when the output is about 10mV be-

APPLICATION INFORMATION (cont.)

low the regulation point of 1.25V. The minimum value for TOFF is 8.75µs. So in this case

$$R_{OFF} = \frac{8.75\mu s \bullet (1.24V - 0.4V)}{150pF \bullet 3.4V} = 15k$$

OTHER APPLICATION CONSIDERATIONS

Output Capacitor: For best regulation of the output voltage or current, the output capacitor should be a low ESR type. This is especially true when operating in current sense mode with a non-linear load such as a battery. If a low ESR capacitor cannot be used, excellent regulation can also be achieved by placing a low pass R/C filter between the current shunt and the CS input.

No Load Operation: The UCC3890 is inherently protected for short circuits, but not for open circuits. If the load is removed, the output voltage will quickly rise up to the regulation point. Once the output is above the regulation voltage, the oscillator will drop to the minimum frequency set by RS/CT. With no load on the output, even at this low frequency the output voltage can quickly rise to a dangerous level. To protect against this, it is recommended that a zener or other voltage clamp always be connected across the output. The clamp should be chosen to be above the normal range of output voltage, but low enough to protect the output capacitor. In current sense operation, removal of the load will also break the regulation loop, in which case a simple clamp on the output may not be adequate. In current sense mode it is recommended that a second zener be connected from the output to the FB pin, the breakdown voltage of this clamp chosen to be high enough so that it will not conduct during normal operation, but will conduct at least 2V lower than the breakdown voltage of the other clamp.

Gate Drive for the External FET: The UCC3890 is guaranteed to be able to deliver at least 1mA of steady state current to the gate of the external FET at ITON = 2mA. If ITON is higher than 2mA, 80% of the additional current is available to drive the FET gate. If, as in the design example above, a moderate sized FET such as the IRF820 is used, the operating frequency is 100kHz, and the minimum ITON at low line is 2.8mA, then the available gate drive current may be adequate. The IRF820 needs about 13nC to charge the gate on each cycle. At 100kHz, this is equivalent to 1.3mA steady state; below the minimum 1.64mA available. In some combinations of a larger FET, and/or higher frequency operation, the current available for driving the gate may not be adequate. In that case extra current may be provided by connecting a resistor RDD from the line input to the VDD pin. This resistor should be sized so that under all conditions the current input to VDD is below the 7.5mA absolute maximum limit. RDD will likely need to be a power resistor.

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UNITRODE

UC1901
UC2901
UC3901

Isolated Feedback Generator

FEATURES

- An Amplitude-Modulation System for Transformer Coupling an Isolated Feedback Error Signal
- Low-Cost Alternative to Optical Couplers
- Internal 1% Reference and Error Amplifier
- Internal Carrier Oscillator Usable to 5mHz
- Modulator Synchronizable to an External Clock
- Loop Status Monitor

DESCRIPTION

The UC1901 family is designed to solve many of the problems associated with closing a feedback control loop across a voltage isolation boundary. As a stable and reliable alternative to an optical coupler, these devices feature an amplitude modulation system which allows a loop error signal to be coupled with a small RF transformer or capacitor.

The programmable, high-frequency oscillator within the UC1901 series permits the use of smaller, less expensive transformers which can readily be built to meet the isolation requirements of today's line-operated power systems. As an alternative to RF operation, the external clock input to these devices allows synchronization to a system clock or to the switching frequency of a SMPS.

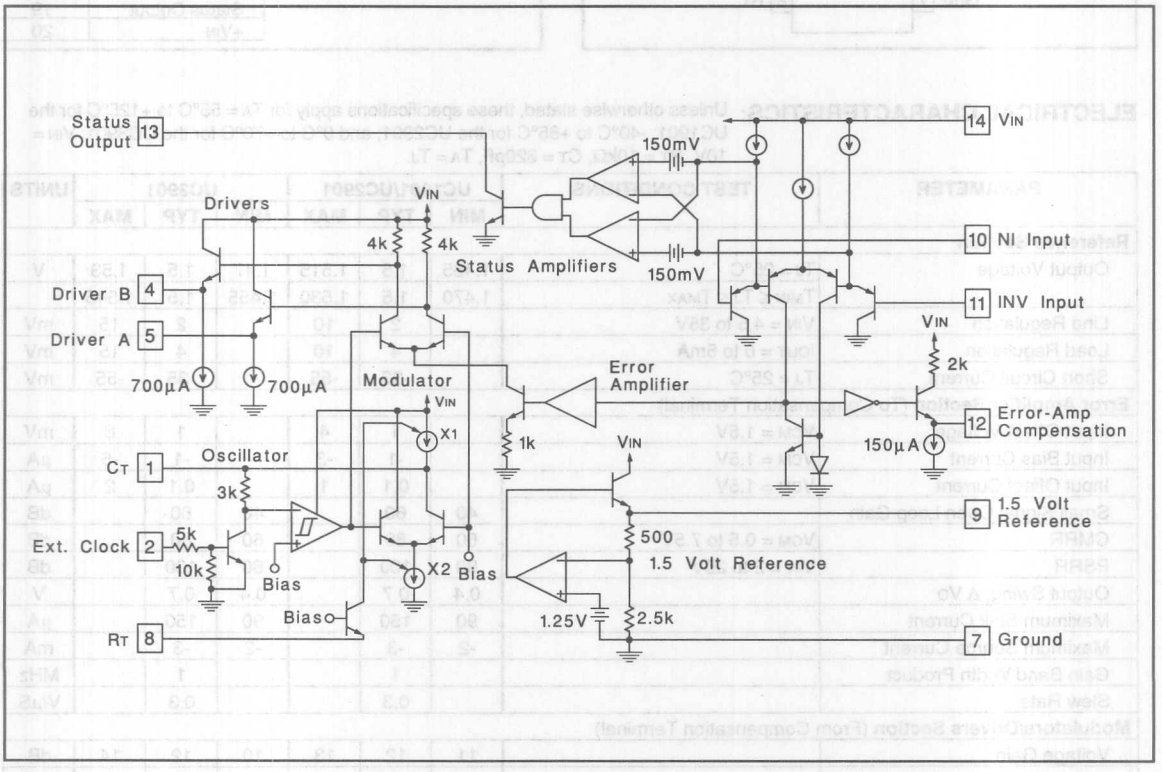
An additional feature is a status monitoring circuit which provides an active-low output when the sensed error voltage is within ±10% of the reference. The Driver A output, Driver B output, and Status Output are disabled until the input supply has reached a sufficient level to allow proper operation of the device.

Since these devices can also be used as a DC driver for optical couplers, the benefits of 4.5 to 40V supply operation, a 1% accurate reference, and a high gain general purpose amplifier offer advantages even though an AC system may not be desired.

3

GENERAL POWER SUPPLY

UC1901 SIMPLIFIED SCHEMATIC



8/94

ABSOLUTE MAXIMUM RATINGS (Note 1)

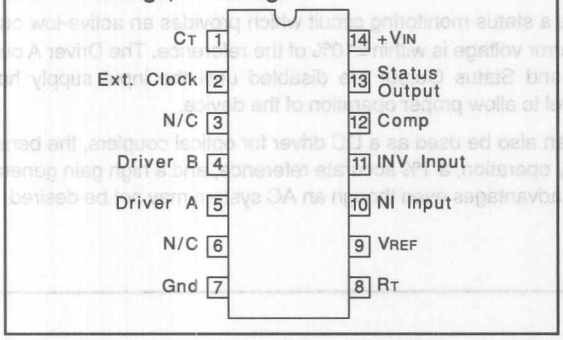
Input Supply Voltage, V_{IN} 40V
Reference Output Current . . . . . -10mA
Driver Output Currents . . . . . -35mA
Status Indicator Voltage 40V
Status Indicator Current 20mA
Ext. Clock Input. 40V
Error Amplifier Inputs . . . . . -0.5V to +35V
Power Dissipation at T_A = 25°C 1000mW
Power Dissipation at T_C = 25°C 2000mW
Operating Junction Temperature . . . . . -55°C to +150°C
Storage Temperature . . . . . -65°C to +150°C
Lead Temperature (Soldering, 10 seconds). . . . . 300°C

Note 1: Voltages are referenced to ground, Pin 7. Currents are positive into, negative out of the specified terminal.

Note 2: Consult Packaging section of Databook for thermal limitations and considerations of package.

CONNECTION DIAGRAMS

DIL-14, SOIC-14 (TOP VIEW)
J or N Package, D Package



PLCC-20, LCC-20
(TOP VIEW)
Q, L Packages



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
CT	2
N/C	3
Ext. Clock	4
Driver B	5
N/C	6
Driver A	7
N/C	8
N/C	9
Gnd	10
N/C	11
RT	12
VREF	13
N/C	14
NI Input	15
N/C	16
INV Input	17
Comp	18
Status Output	19
+VIN	20

ELECTRICAL CHARACTERISTICS:

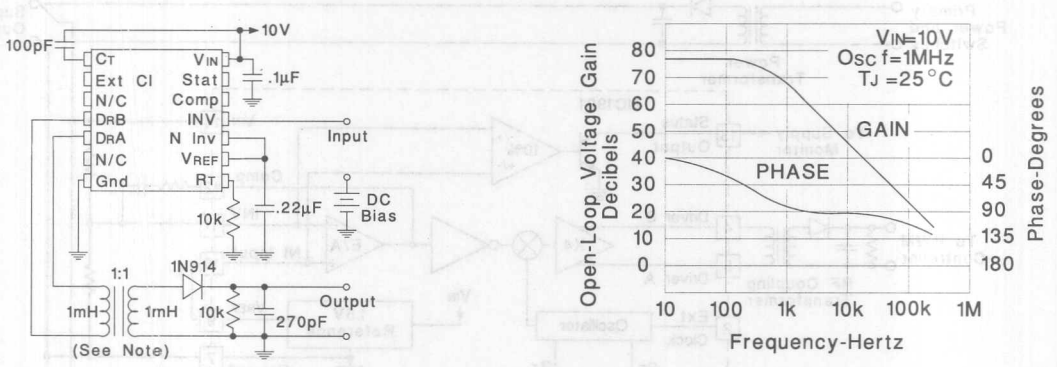
Unless otherwise stated, these specifications apply for T_A = 55°C to +125°C for the UC1901; -40°C to +85°C for the UC2901; and 0°C to +70°C for the UC3901; V_{IN} = 10V, R_T = 10kΩ, C_T = 820pF, T_A = T_J.

PARAMETER	TEST CONDITIONS	UC1901/UC2901			UC3901			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Reference Section								
Output Voltage	T_J = 25°C	1.485	1.5	1.515	1.47	1.5	1.53	V
	$T_{MIN} \le T_J \le T_{MAX}$	1.470	1.5	1.530	1.455	1.5	1.545	
Line Regulation	V_{IN} = 4.5 to 35V		2	10		2	15	mV
Load Regulation	I_{OUT} = 0 to 5mA		4	10		4	15	mV
Short Circuit Current	T_J = 25°C		-35	-55		-35	-55	mV
Error Amplifier Section (To Compensation Terminal)								
Input Offset Voltage	V_{CM} = 1.5V		1	4		1	8	mV
Input Bias Current	V_{CM} = 1.5V		-1	-3		-1	-6	µA
Input Offset Current	V_{CM} = 1.5V		0.1	1		0.1	2	µA
Small Signal Open Loop Gain		40	60		40	60		dB
CMRR	V_{CM} = 0.5 to 7.5V	60	80		60	80		dB
PSRR	V_{IN} = 2 to 25V	80	100		80	100		dB
Output Swing, Δ V_O		0.4	0.7		0.4	0.7		V
Maximum Sink Current		90	150		90	150		µA
Maximum Source Current		-2	-3		-2	-3		mA
Gain Band Width Product			1			1		MHz
Slew Rate			0.3			0.3		V/µS
Modulators/Drivers Section (From Compensation Terminal)								
Voltage Gain		11	12	13	10	12	14	dB
Output Swing		±1.6	±2.8		±1.6	±2.8		V

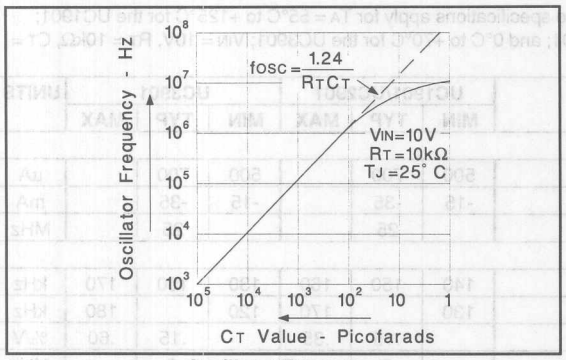
ELECTRICAL CHARACTERISTICS (cont.): Unless otherwise stated, these specifications apply for T_A = 55°C to +125°C for the UC1901; -40°C to +85°C for the UC2901; and 0°C to +70°C for the UC3901; V_{IN} = 10V, R_T = 10kΩ, C_T = 820pF, T_A = T_J.

PARAMETER	TEST CONDITIONS	UC1901/UC2901			UC3901			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Modulators/Drivers Section (cont.)								
Driver Sink Current		500	700		500	700		µA
Driver Source Current		-15	-35		-15	-35		mA
Gain Band Width Product			25			25		MHz
Oscillator Section								
Initial Accuracy	T_J = 25°C	140	150	160	130	150	170	kHz
	$T_{MIN} \le T_J \le T_{MAX}$	130		170	120		180	kHz
Line Sensitivity	V_{IN} = 5 to 35V		.15	.35		.15	.60	%/V
Maximum Frequency	R_T = 10k, C_T = 10pF		5			5		MHz
Ext. Clock Low Threshold	Pin 1 (C_T) = V_{IN}	0.5			0.5			V
Ext. Clock High Threshold	Pin 1 (C_T) = V_{IN}			1.6			1.6	V
Status Indicator Section								
Input Voltage Window	@ E/A Inputs, V_{CM} = 1.5V	±135	±150	±165	±130	±150	±170	mV
Saturation Voltage	E/A Δ Input = 0V, I_{SINK} = 1.6mA			0.45			0.45	V
Max. Output Current	Pin 13 = 3V, E/A Δ Input = 0.0V	8	15		8	15		mA
Leakage Current	Pin 13 = 40V, E/A ΔInput = 0.2V		.05	1		.05	5	µA
Supply Current	V_{IN} = 35V		5	8		5	10	mA
UVLO Section								
Drivers Enabled Threshold	At Input Supply V_{IN}		3.9	4.5		3.9	4.5	V
Status Output Enabled Threshold	At Input Supply V_{IN}		3.9	4.5		3.9	4.5	V
Change in Reference Output	When V_{IN} Reaches UVLO Threshold		-2	-30		-2	-30	mV

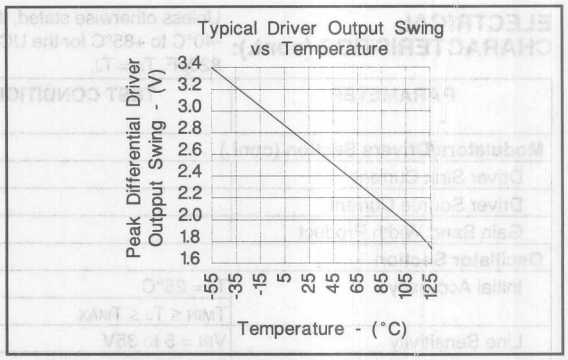
Transformer Coupled Open Loop Transfer Function



Transformer Data: N1 = N2 = 20TAWG 26
Core = Ferroxcube 3E2A Ferrite, 0.5" O.D. toroid
Carrier Frequency = 1MHz



Oscillator Frequency



Typical Driver Output Swing vs Temperature

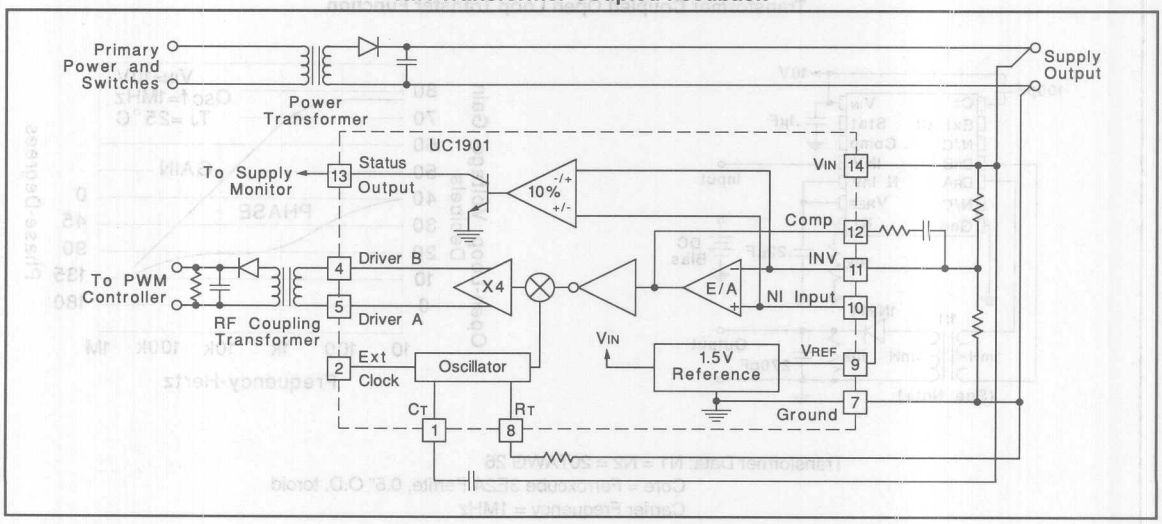
APPLICATION INFORMATION

The error amplifier compensation terminal, Pin 12, is intended as a source of feedback to the amplifier's inverting input at Pin 11. For most applications, a series DC blocking capacitor should be part of the feedback network. The amplifier is internally compensated for unity feedback.

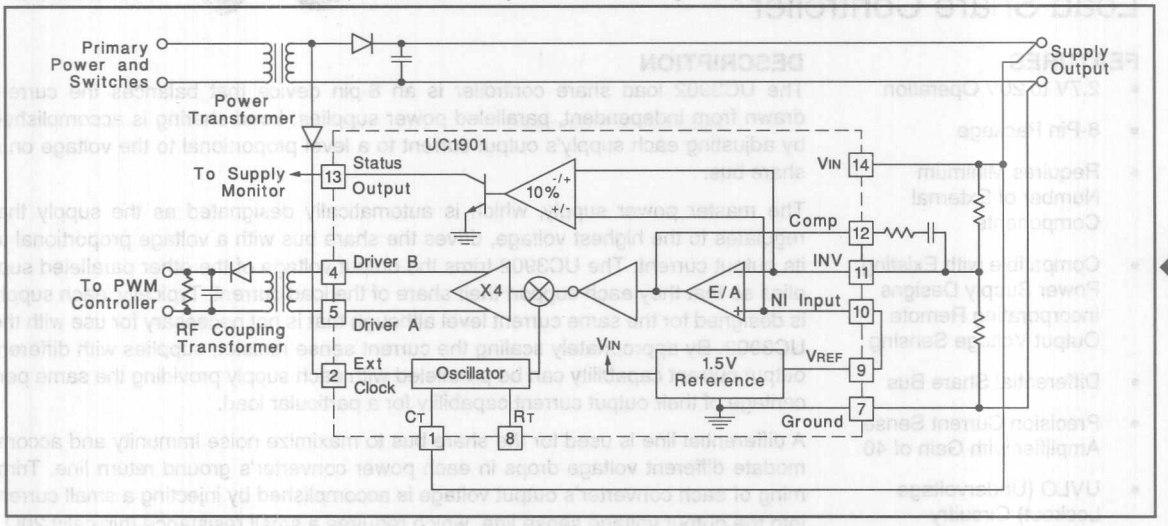
The waveform at the driver outputs is a squarewave with an amplitude that is proportional to the error amplifier input signal. There is a fixed 12dB of gain from the error amplifier compensation pin to the modulator driver outputs. The frequency of the output waveform is controlled by either the internal oscillator or an external clock signal. With the internal oscillator the squarewave will have a fixed 50% duty cycle. If the internal oscillator is disabled by connecting Pin 1, CR, to VIN then the frequency and duty cycle of the output will be determined by the input clock waveform at Pin 2. If the oscillator remains disabled and there is not clock input at Pin 2, there will be a linear 12dB of signal gain to one or the other of the driver outputs depending on the DC state of Pin 2.

The driver outputs are emitter followers which will source a minimum of 15mA of current. The sink current, internally limited at 700µA, can be increased by adding resistors to ground at the driver outputs.

R.F. Transformer Coupled Feedback

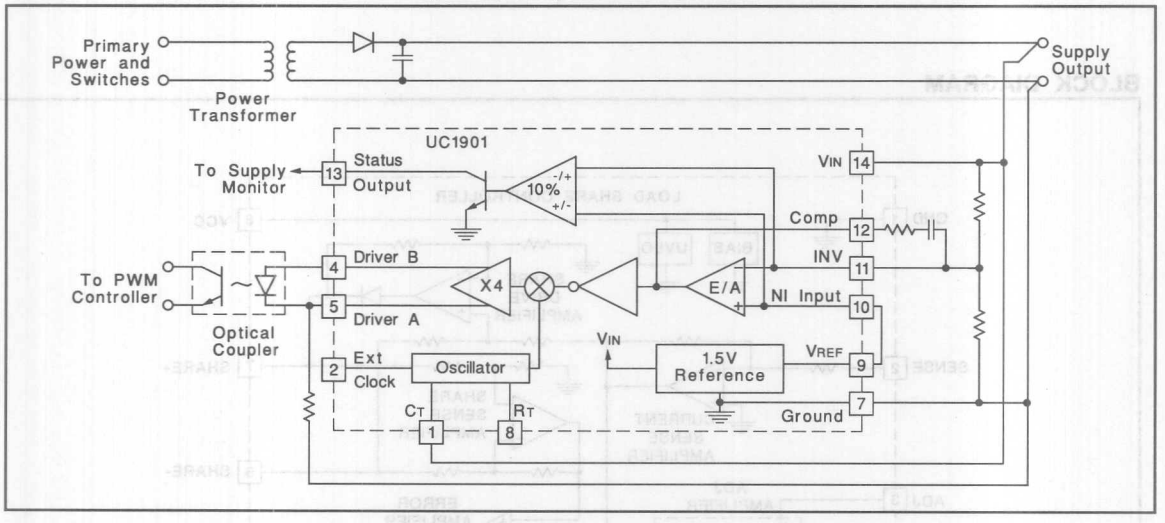


Feedback Coupled at Switching Frequency



TYPICAL APPLICATION

Optically Coupled DC Feedback



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UNITRODE

UC1902
UC2902
UC3902
PRELIMINARY

Load Share Controller

FEATURES

- 2.7V to 20V Operation
- 8-Pin Package
- Requires Minimum Number of External Components
- Compatible with Existing Power Supply Designs Incorporating Remote Output Voltage Sensing
- Differential Share Bus
- Precision Current Sense Amplifier with Gain of 40
- UVLO (Undervoltage Lockout) Circuitry
- User Programmable Share Loop Compensation

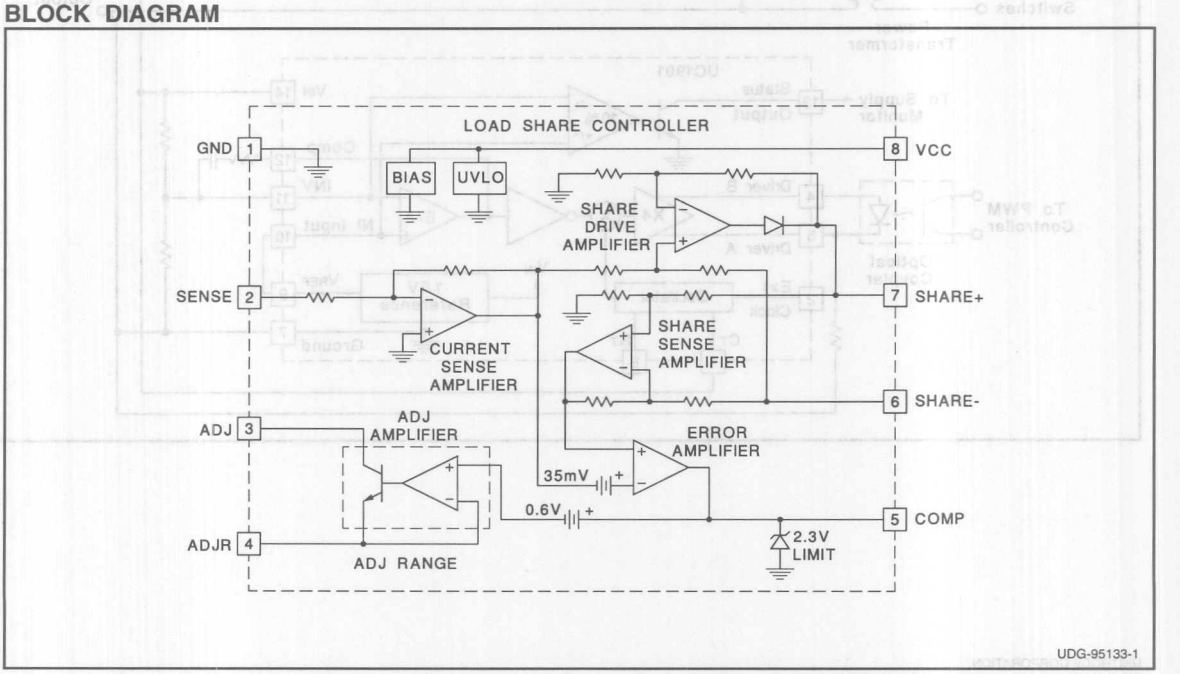
DESCRIPTION

The UC3902 load share controller is an 8-pin device that balances the current drawn from independent, paralleled power supplies. Load sharing is accomplished by adjusting each supply's output current to a level proportional to the voltage on a share bus.

The master power supply, which is automatically designated as the supply that regulates to the highest voltage, drives the share bus with a voltage proportional to its output current. The UC3902 trims the output voltage of the other paralleled supplies so that they each support their share of the load current. Typically, each supply is designed for the same current level although that is not necessary for use with the UC3902. By appropriately scaling the current sense resistor, supplies with different output current capability can be paralleled with each supply providing the same percentage of their output current capability for a particular load.

A differential line is used for the share bus to maximize noise immunity and accommodate different voltage drops in each power converter's ground return line. Trimming of each converter's output voltage is accomplished by injecting a small current into the output voltage sense line, which requires a small resistance (typically 20Ω - 100Ω) to be inserted.

BLOCK DIAGRAM



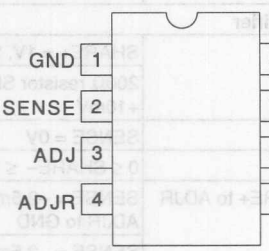
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (ADJ and VCC) . . . . . –0.3V to 20V
SENSE Voltage . . . . . –5V to +5V
ADJR, COMP Voltage . . . . . –0.3V to +4V
SHARE–, SHARE+ Voltages . . . . . –0.3V to 10V
SHARE+ Current . . . . . –100mA to +10mA
ADJ Current . . . . . –1mA to +30mA
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10sec.) . . . . . +300°C

All voltages are with respect to pin 1. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of the Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

DIL-8, SOIC-8 (Top View)
N, J and D Package



ELECTRICAL CHARACTERISTICS: Unless otherwise specified, T_A = –55°C to +125°C for UC1902, –40°C to+85°C for UC2902, 0°C to 70°C for UC3902, VCC = 5V, R_{ADJR} = 1kΩ, V_{ADJ} = 5V, COMP = 5nF capacitor to GND, V_{SHARE-} = 0V, T_A = T_J.

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Supply					
Supply Current	SHARE+ = 1V, SENSE = 0V		4	6	mA
	VCC = 20V		6	10	mA
Undervoltage Lockout					
Startup Voltage	SHARE+ = 0.2V, SENSE = 0V, COMP = 1V	2.3	2.5	2.7	V
Hysteresis	SHARE+ = 0.2V, SENSE = 0V, COMP = 1V	60	100	140	mV
Current Sense Amplifier					
Input Offset Voltage	0.1V ≤ SHARE+ ≤ 1.1V	–2.5	–0.5	1.5	mV
Gain SENSE to SHARE	0.1V ≤ SHARE+ ≤ 1.1V	–41	–40	-39	V/V
Input Resistance		0.6	1	1.5	kΩ
Share Drive Amplifier					
SHARE+ High	VCC = 2.5V, SENSE = –50mV, I_{SHARE+} = –1mA	1.2	1.4		V
	VCC = 12V, SENSE = –250mV, I_{SHARE+} = –1mA	9.6	10	10.4	V
	VCC = 20V, SENSE = –250mV, I_{SHARE+} = –1mA	9.6	10	10.4	V
SHARE+ Low	VCC = 2.5V, SENSE = +10mV, I_{SHARE+} = –1mA		20	50	mV
	VCC = 12V, SENSE = +10mV, I_{SHARE+} = –1mA		20	50	mV
	VCC = 20V, SENSE = +10mV, I_{SHARE+} = –1mA		20	50	mV
SHARE+ Output Voltage	Measures SHARE+, SENSE = 0mV, R_{SHARE+} = 200Ω resistor SHARE+ to GND		20	40	mV
CMRR	0 ≤ SHARE– ≤ 1V , SENSE used as input to amplifier	50	90		dB
Load Regulation	Load on SHARE+, –1mA ≤ I_{LOAD} ≤ –20mA, SENSE = –25mV		0	20	mV
Short Circuit Current	SHARE+ = 0V, SENSE = –25mV	–85	–50	–20	mA
Slew Rate	SENSE = +10mV to –90mV Step, 200Ω resistor SHARE+ to GND	0.16	0.27	0.37	V/µs
	SENSE = –90mV to +10mV Step, 200Ω resistor SHARE+ to GND	0.12	0.24	0.34	V/µs

ELECTRICAL CHARACTERISTICS (cont.): Unless otherwise specified, T_A = –55°C to +125°C for UC1902, –40°C to+85°C for UC2902, 0°C to 70°C for UC3902, VCC = 5V, R_{ADJR} = 1kΩ, V_{ADJ} = 5V, COMP = 5nF capacitor to GND, V_{SHARE-} = 0V, $T_A = T_J$.

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Share Sense Amplifier					
Input Impedance	SHARE+ = 1V, SHARE– = 1V, SENSE = +10mV	10	15		kΩ
	200Ω resistor SHARE+ to GND, SHARE– = 1V, SENSE = +10mV	15	17		kΩ
Threshold	SENSE = 0V	41	70	100	mV
CMRR SHARE	0 ≤ SHARE– ≤ 1V, SENSE = –2.5mV	50	60		dB
AVOL from SHARE+ to ADJR	SENSE = –2.5mV, 5nF capacitor COMP to GND, 1k resistor ADJR to GND	50	68		dB
	SENSE = –2.5mV, 5nF capacitor COMP to GND, 150Ω resistor ADJR to GND	50	66		dB
Slew Rate	SHARE+ = Step of 0mV to 300mV through a 200Ω resistor, R_{COMP} = 500Ω resistor to 1.5V, SENSE = 10mV	0.4	0.7	1	V/µs
Error Amplifier Section					
Transconductance, SHARE+ to COMP	200Ω resistor SHARE+ to GND	3.2	4.5	5.5	mS
IOH	COMP = 1.5V, SHARE+ ≥ +300mV, SENSE = +10mV	–400	–325	–230	µA
IOL	200Ω resistor SHARE+ to GND, COMP = 1.5V, SENSE = +10mV	100	150	200	µA
Input Offset Voltage		15	35	65	mV
Δ VIO/Δ V_{SENSE}	1k Resistor, ADJR to GND, –2.5mV < SENSE < –25mV	–6	0	6	mV/V
ADJ Amplifier					
ADJR Low Voltage	SENSE = +10mV, 200Ω resistor SHARE+ to GND	–1	0	1	mV
ADJR High Voltage	SENSE = +10mV, SHARE+ = 1V	1.4	1.8	2.1	V
Current Gain ADJR to ADJ	ADJR Current = –0.5mA, ADJ = 2.5V, SENSE = +10mV, SHARE+ = 1V	0.96	0.99	1	A/A
	ADJR Current = –0.5mA, ADJ = 20V, SENSE = +10mV, SHARE+ = 1V	0.96	0.99	1	A/A
	ADJR Current = –10mA, ADJ = 2.5V, SENSE = +10mV, SHARE+ = 1V	0.96	0.99	1	A/A
	ADJR Current = –10mA, ADJ = 20V, SENSE = +10mV, SHARE+ = 1V	0.96	0.99	1	A/A

PIN DESCRIPTIONS

ADJ: Current output of adjust amplifier circuit (NPN collector).

ADJR: Current adjust amplifier range set (NPN emitter).

COMP: Output of error amplifier, input of adjust amplifier. This is where the compensation capacitor is connected.

GND: Local power supply return and signal ground.

SENSE: Inverting input of current sense amplifier.

SHARE+: Positive input from share bus or drive to share bus.

SHARE-: Reference for SHARE+.

VCC: Local power supply (positive).

APPLICATION INFORMATION

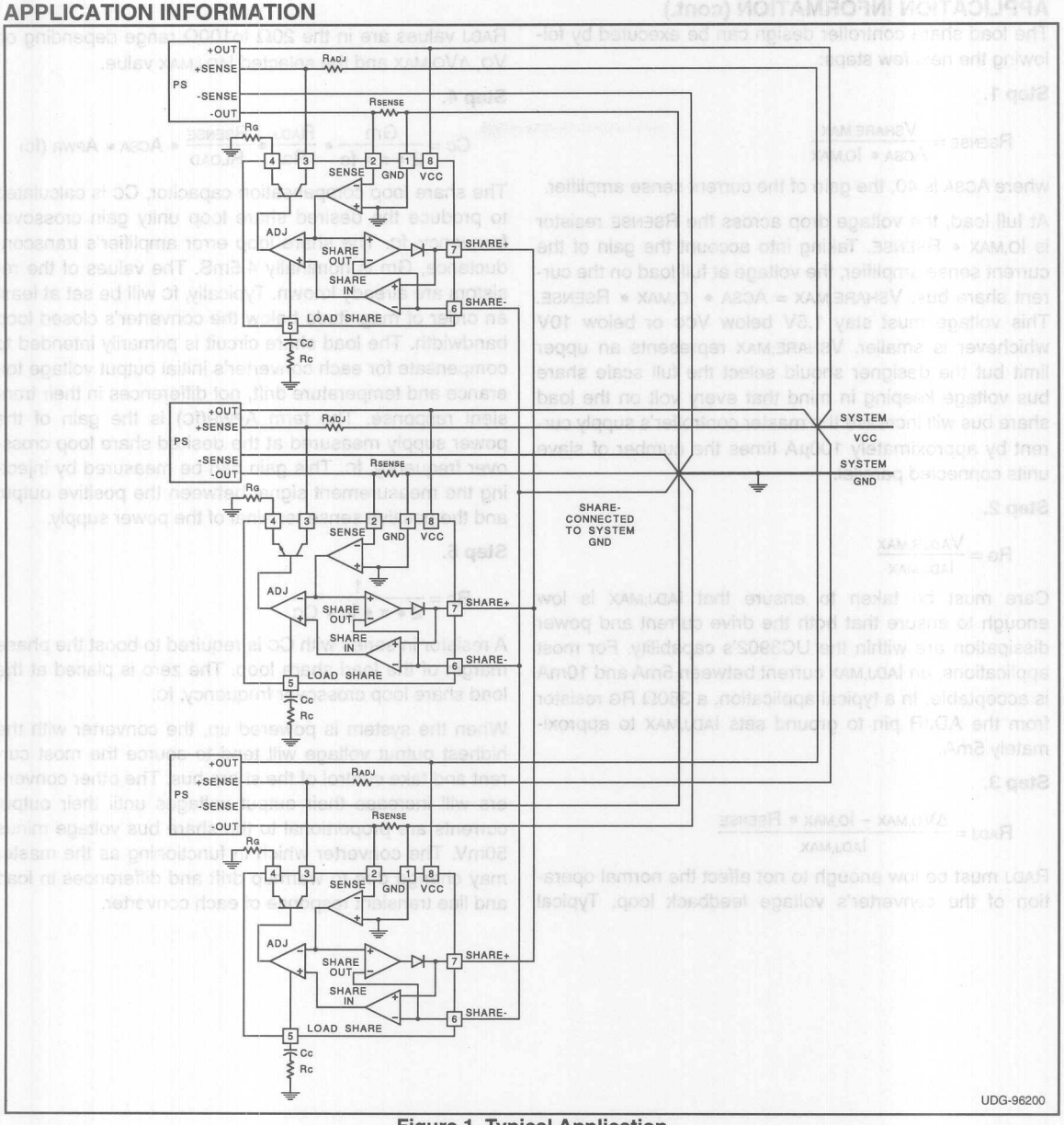


Figure 1. Typical Application

The values of five passive components must be determined to configure the UC3902 load share controller. The output and return lines of each converter are connected together at the load, with current sense resistor RSENSE inserted in each negative return line. Another resistor, RADJ, is also inserted in each positive remote sense line.

The differential share bus terminals (SHARE+ and SHARE–) of each UC3902 are connected together respectively, and the SHARE– node is also connected to the system ground. A typical application is illustrated in Figure 1.

APPLICATION INFORMATION (cont.)

The load share controller design can be executed by following the next few steps:

Step 1.

$$R_{SENSE} = \frac{V_{SHARE,MAX}}{A_{CSA} \bullet I_{O,MAX}}$$

where A_{CSA} is 40, the gain of the current sense amplifier.

At full load, the voltage drop across the R_{SENSE} resistor is $I_{O,MAX} \bullet R_{SENSE}$. Taking into account the gain of the current sense amplifier, the voltage at full load on the current share bus, $V_{SHARE,MAX} = A_{CSA} \bullet I_{O,MAX} \bullet R_{SENSE}$. This voltage must stay 1.5V below V_{CC} or below 10V whichever is smaller. $V_{SHARE,MAX}$ represents an upper limit but the designer should select the full scale share bus voltage keeping in mind that every volt on the load share bus will increase the master controller's supply current by approximately 100µA times the number of slave units connected parallel.

Step 2.

$$R_G = \frac{V_{ADJR,MAX}}{I_{ADJ,MAX}}$$

Care must be taken to ensure that $I_{ADJ,MAX}$ is low enough to ensure that both the drive current and power dissipation are within the UC3902's capability. For most applications, an $I_{ADJ,MAX}$ current between 5mA and 10mA is acceptable. In a typical application, a 360Ω R_G resistor from the ADJR pin to ground sets $I_{ADJ,MAX}$ to approximately 5mA.

Step 3.

$$R_{ADJ} = \frac{\Delta V_{O,MAX} - I_{O,MAX} \bullet R_{SENSE}}{I_{ADJ,MAX}}$$

R_{ADJ} must be low enough to not affect the normal operation of the converter's voltage feedback loop. Typical R_{ADJ} values are in the 20Ω to100Ω range depending on V_O, $\Delta V_{O,MAX}$ and the selected $I_{ADJ,MAX}$ value.

Step 4.

$$C_C = \frac{Gm}{2 \bullet \pi \bullet fc} \bullet \frac{R_{ADJ}}{R_G} \bullet \frac{R_{SENSE}}{R_{LOAD}} \bullet A_{CSA} \bullet A_{PWR}(fc)$$

The share loop compensation capacitor, C_C is calculated to produce the desired share loop unity gain crossover frequency, fc. The share loop error amplifier's transconductance, Gm is nominally 4.5mS. The values of the resistors are already known. Typically, fc will be set at least an order of magnitude below the converter's closed loop bandwidth. The load share circuit is primarily intended to compensate for each converter's initial output voltage tolerance and temperature drift, not differences in their transient response. The term $A_{PWR}(fc)$ is the gain of the power supply measured at the desired share loop crossover frequency, fc. This gain can be measured by injecting the measurement signal between the positive output and the positive sense terminal of the power supply.

Step 5.

$$R_C = \frac{1}{2 \bullet \pi \bullet fc \bullet C_C}$$

A resistor in series with C_C is required to boost the phase margin of the load share loop. The zero is placed at the load share loop crossover frequency, fc.

When the system is powered up, the converter with the highest output voltage will tend to source the most current and take control of the share bus. The other converters will increase their output voltages until their output currents are proportional to the share bus voltage minus 50mV. The converter which in functioning as the master may change due to warmup drift and differences in load and line transient response of each converter.

UNITRODE CORPORATION
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Quad Supply and Line Monitor

FEATURES

- Inputs for Monitoring up to Four Separate Supply Voltage Levels
- Internal Inverter for Sensing a Negative Supply Voltage
- Line/Switch Sense Input for Early Power Source Failure Warning
- Programmable Under- and Over-Voltage Fault Thresholds with Proportional Hysteresis
- A Precision 2.5V Reference
- General Purpose Op-Amp for Auxiliary Use
- Three High Current, >30mA, Open-Collector Outputs Indicate Over-Voltage, Under-Voltage and Power OK Conditions
- Input Supply Under-Voltage Sensing and Start-Latch Eliminate Erroneous Fault Alerts During Start-Up
- 8-40V Supply Operation with 7mA Stand-By Current

DESCRIPTION

The UC1903 family of quad supply and line monitor integrated circuits will respond to under- and over-voltage conditions on up to four continuously monitored voltage levels. An internal op-amp inverter allows at least one of these levels to be negative. A separate line/switcher sense input is available to provide early warning of line or other power source failures.

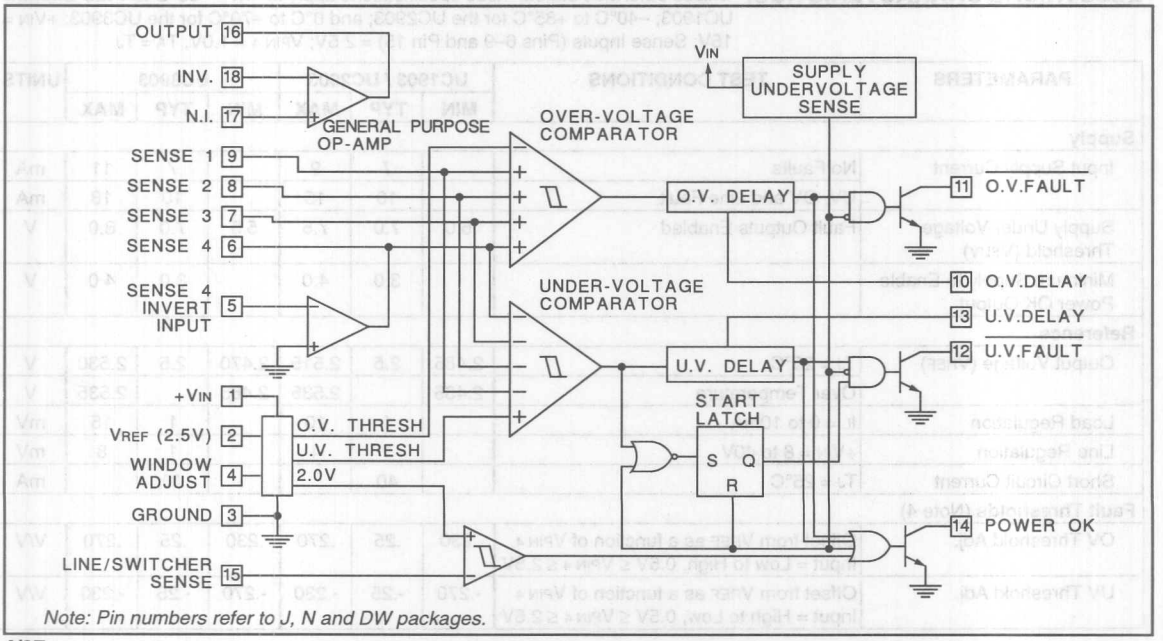
The fault window adjustment circuit on these devices provides easy programming of under- and over-voltage thresholds. The thresholds, centered around a precision 2.5V reference, have an input hysteresis that scales with the window width for precise, glitch-free operation. A reference output pin allows the sense input fault windows to be scaled independently using simple resistive dividers.

The three open collector outputs on these devices will sink in excess of 30mA of load current when active. The under- and over-voltage outputs respond after separate, user defined, delays to respective fault conditions. The third output is active during any fault condition including under- and over-voltage, line/switcher faults, and input supply under-voltage. The off state of this output indicates a "power OK" situation.

An additional, uncommitted, general purpose op-amp is also included. This op-amp, capable of sourcing 20mA of output current, can be used for a number of auxiliary functions including the sensing and amplification of a feedback error signal when the 2.5V output is used as a system reference.

In addition, these ICs are equipped with a start-latch to prevent erroneous under-voltage indications during start-up. These parts operate over an 8V to 40V input supply range and require a typical stand-by current of only 7mA.

BLOCK DIAGRAM



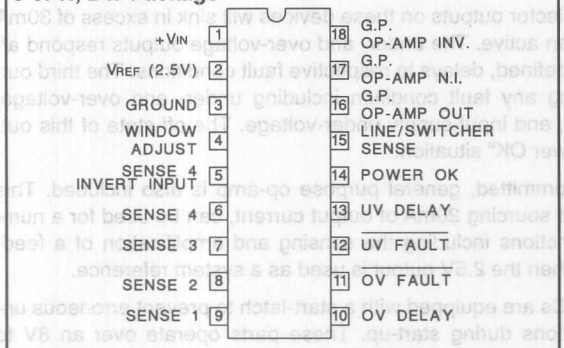
Note: Pin numbers refer to J, N and DW packages.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (+VIN) . . . . . +40V
Open Collector Output Voltages . . . . . +40V
Open Collector Output Currents 50mA
Sense 1-4 Input Voltages . . . . . -0.3V to +20V
Line/Switcher Sense Input Voltage . . . . . -0.3V to +40V
Op-Amp and Inverter Input Voltages . . . . . -0.3V to +40V
Op-Amp and Inverter Output Currents . . . . . -40mA
Window Adjust Voltage . . . . . 0.0V to +10V
Delay Pin Voltages . . . . . 0.0V to +5V
Reference Output Current . . . . . -40mA
Power Dissipation at TA = 25°C (Note 1) 1000mW
Power Dissipation at TC = 25°C (Note 1) 2000mW
Operating Junction Temperature . . . . . -55°C to +150°C
Storage Temperature . . . . . -65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) . . . . . 300°C

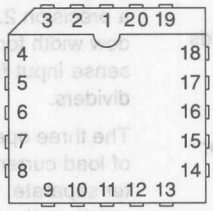
Note 1: Voltages are referenced to ground (Pin 3). Currents are positive into, negative out of, the specified terminals. Consult Packaging Section of Databook for thermal limitations and considerations of package.

DIL-18, SOIC-18 (TOP VIEW)
J or N, DW Package



CONNECTION DIAGRAMS

PLCC-20, LCC-20
(TOP VIEW)
Q, L Package



PACKAGE PIN FUNCTION	
FUNCTION	PIN
+VIN	1
VREF (2.5V)	2
GROUND	3
GROUND	4
WINDOW ADJUST	5
N/C	6
SENSE 4 INVERT INPUT	7
SENSE 4	8
SENSE 3	9
SENSE 2	10
SENSE 1	11
OV DELAY	12
$\overline{\text{OV FAULT}}$	13
$\overline{\text{UV FAULT}}$	14
UV DELAY	15
POWER OK	16
LINE/SWITCHER SENSE	17
G.P. OP-AMP OUT	18
G.P. OP-AMP N.I.	19
G.P. OP-AMP INV.	20

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, these specifications apply for TA = –55°C to +125°C for the UC1903; –40°C to +85°C for the UC2903; and 0°C to +70°C for the UC3903; +VIN = 15V; Sense Inputs (Pins 6–9 and Pin 15) = 2.5V; VPIN 4 = 1.0V, TA = TJ.

PARAMETERS	TEST CONDITIONS	UC1903 / UC2903			UC3903			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Supply								
Input Supply Current	No Faults		7	9		7	11	mA
	UV, OV and Line Fault		10	15		10	18	mA
Supply Under Voltage Threshold (VSUV)	Fault Outputs Enabled	6.0	7.0	7.5	5.5	7.0	8.0	V
Minimum Supply to Enable Power OK Output			3.0	4.0		3.0	4.0	V
Reference								
Output Voltage (VREF)	TJ = 25°C	2.485	2.5	2.515	2.470	2.5	2.530	V
	Over Temperature	2.465		2.535	2.465		2.535	V
Load Regulation	IL = 0 to 10mA		1	10		1	15	mV
Line Regulation	+VIN = 8 to 40V		1	4		1	8	mV
Short Circuit Current	TJ = 25°C		40			40		mA
Fault Thresholds (Note 4)								
OV Threshold Adj.	Offset from VREF as a function of VPIN 4 Input = Low to High, 0.5V ≤ VPIN 4 ≤ 2.5V	.230	.25	.270	.230	.25	.270	V/V
UV Threshold Adj.	Offset from VREF as a function of VPIN 4 Input = High to Low, 0.5V ≤ VPIN 4 ≤ 2.5V	-.270	-.25	-.230	-.270	-.25	-.230	V/V

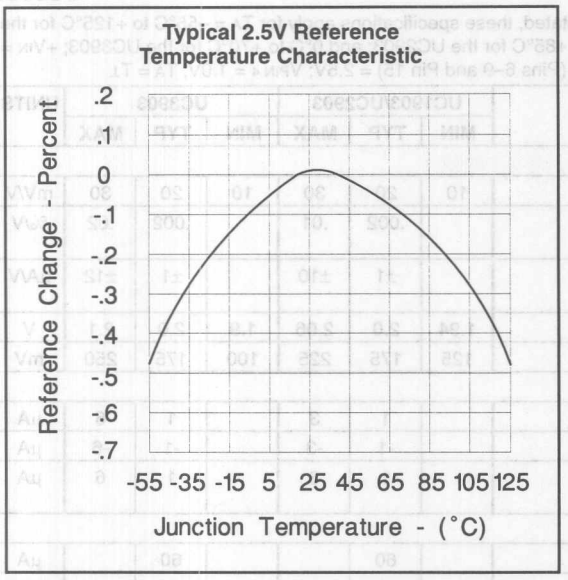
ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = –55°C to +125°C for the UC1903; –40°C to +85°C for the UC2903; and 0°C to +70°C for the UC3903; $+V_{IN}$ = 15V; Sense Inputs (Pins 6–9 and Pin 15) = 2.5V; $V_{PIN\ 4}$ = 1.0V, T_A = T_J.

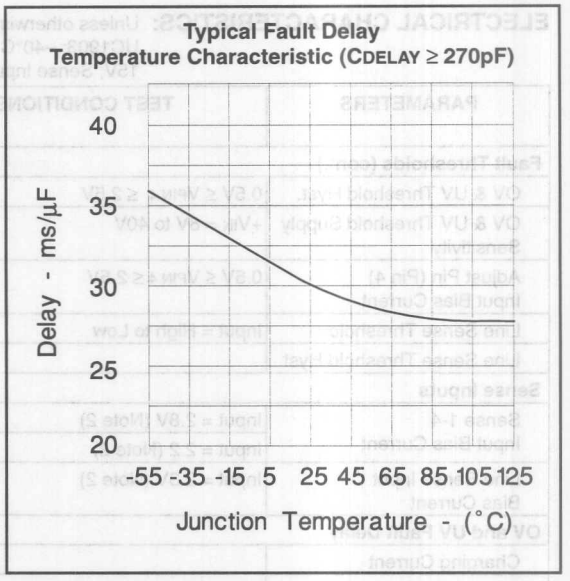
PARAMETERS	TEST CONDITIONS	UC1903/UC2903			UC3903			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Fault Thresholds (cont.)								
OV & UV Threshold Hyst.	0.5V ≤ $V_{PIN\ 4}$ ≤ 2.5V	10	20	30	10	20	30	mV/V
OV & UV Threshold Supply Sensitivity	$+V_{IN}$ = 8V to 40V		.002	.01		.002	.02	%/V
Adjust Pin (Pin 4) Input Bias Current	0.5V ≤ $V_{PIN\ 4}$ ≤ 2.5V		±1	±10		±1	±12	µA/V
Line Sense Threshold	Input = High to Low	1.94	2.0	2.06	1.9	2.0	2.1	V
Line Sense Threshold Hyst.		125	175	225	100	175	250	mV
Sense Inputs								
Sense 1-4 Input Bias Current	Input = 2.8V (Note 2)		1	3		1	6	µA
	Input = 2.2 (Note 2)		-1	-3		-1	-6	µA
Line Sense Input Bias Current	Input = 2.3V (Note 2)		1	3		1	6	µA
OV and UV Fault Delay								
Charging Current			60			60		µA
Threshold Voltage	Delay Pin = Low to High		1.8			1.8		V
Threshold Hysteresis	T_J = 25°C		250			250		mV
Delay	Ratio of Threshold Voltage to Charging Current	20	30	50	20	30	50	ms/µF
Fault Outputs ($\overline{OV}$, $\overline{UV}$, & Power 0K)								
Maximum Current	V_{OUT} = 2V	30	70		30	70		mA
Saturation Voltage	I_{OUT} = 12mA		.25	.40		.25	.40	V
Leakage Current	V_{OUT} = 40 V		3	25		3	25	µA
Sense 4 Inverter (Note 3)								
Input Offset Voltage			2	8		2	10	mV
Input Bias Current			.1	2		.1	4	µA
Open Loop Gain		65	80		65	80		dB
PSRR	$+V_{IN}$ = 8 to 40 V	65	100		65	100		dB
Unity Gain Frequency			1			1		MHz
Slew Rate			.4			.4		V/µs
Short Circuit Current	T_J = 25°C		40			40		mA
G.P. Op-Amp (Note 3)								
Input Offset Voltage			1	5		1	8	mV
Input Bias Voltage			.1	2		.1	4	µA
Input Offset Current			.01	.5		.01	1.0	µA
Open Loop Gain		65	120		65	120		dB
CMRR	V_{CM} = 0 to $+V_{IN}$ = 2.0V	65	100		65	100		dB
PSRR	$+V_{IN}$ = 8 to 40V	65	100		65	100		dB
Unity Gain Frequency			1			1		MHz
Slew Rate			.4			.4		V/µs
Short Circuit Current	T_J = 25°C		40			40		mA

Note 2: These currents represent maximum input bias currents required as the sense inputs cross appropriate thresholds.

Note 3: When either the G.P. OP-Amp, or the Sense 4 Inverter, are configured for sensing a negative supply voltage, the divider resistance at the inverting input should be chosen such that the nominal divider current is ≤ 1.4mA. With the divider current at or below this level possible latching of the circuit is avoided. Proper operation for currents at or below 1.4mA is 100% tested in production.

Note 4: Reference to pin numbers in this specification pertain to 18 pin DIL N and J packages and 18 pin SOIC DW package.





OPERATION AND APPLICATION INFORMATION

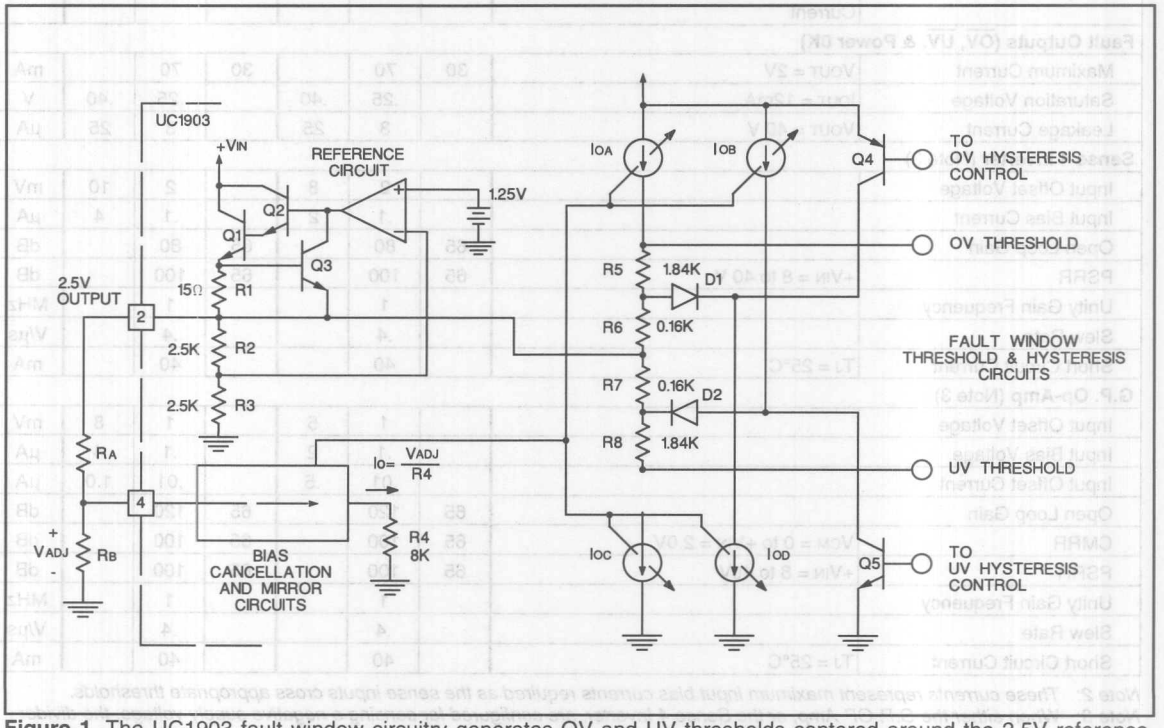


Figure 1. The UC1903 fault window circuitry generates OV and UV thresholds centered around the 2.5V reference. Window magnitude and threshold hysteresis are proportional to the window adjust input voltage at Pin 4.

OPERATION AND APPLICATION INFORMATION

Setting a Fault Window

The fault thresholds on the UC1903 are generated by creating positive and negative offsets, equal in magnitude, that are referenced to the chip's 2.5V reference. The resulting fault window is centered around 2.5V and has a magnitude equal to that of the applied offsets. Simplified schematics of the fault window and reference circuits are shown in Figure 1 (see previous page). The magnitude of the offsets is determined by the voltage applied at the window adjust pin, Pin 4. A bias cancellation circuit keeps the input current required at Pin 4 low, allowing the use of a simple resistive divider off the reference to set the adjust pin voltage.

The adjust voltage at Pin 4 is internally applied across R_4, and an 8k resistor. The resulting current is mirrored four times to generate current sources I_{OA}, I_{OB}, I_{OC}, and I_{OD}, all equal in magnitude. When all four of the sense inputs are inside the fault window, a no-fault condition, Q_4 and Q_5 are turned on. In combination with D_1 and D_2 this prevents L_{OB} and L_{OD} from affecting the fault thresholds. In this case, the OV and UV thresholds are equal to $V_{REF} + I_{OA}(R_5 + R_6)$ and $V_{REF} - I_{OC}(R_7 + R_8)$ respectively. The fault window can be expressed as:

$$(1) \qquad 2.5V \pm \frac{V_{ADJ}}{4}.$$

In terms of a sensed nominal voltage level, Vs, the window as a percent variation is:

$$(2) \qquad Vs \pm (10 \cdot V_{ADJ})\ \%.$$

When a sense input moves outside the fault window given in equation(1), the appropriate hysteresis control signal turns off Q_4 or Q_5. For the under-voltage case, Q_5 is disabled and current source I_{OB} flows through D_2. The net current through R_7 becomes zero as I_{OB} cancels I_{OC}, giving an 8% reduction in the UV threshold offset. The over-voltage case is the same, with Q_4 turning off, allowing I_{OD} to cancel the current flow, I_{OA}, through R_6. The result is a hysteresis at the sense inputs which is always 8% of the window magnitude. This is shown graphically in Figure 2.

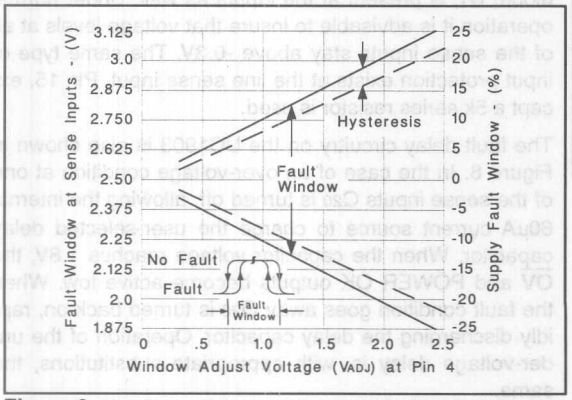


Figure 2. The fault window and threshold hysteresis scale as a function of the voltage applied at Pin 4, the window adjust pin.

Fault Windows Can Be Scaled Independently

In many applications, it may be desirable to monitor various supply voltages, or voltage levels, with varying fault windows. Using the reference output and external resistive dividers this is easily accomplished with the UC1903. Figures 3 and 4 illustrate how the fault window at any sense input can be scaled independently of the remaining inputs.

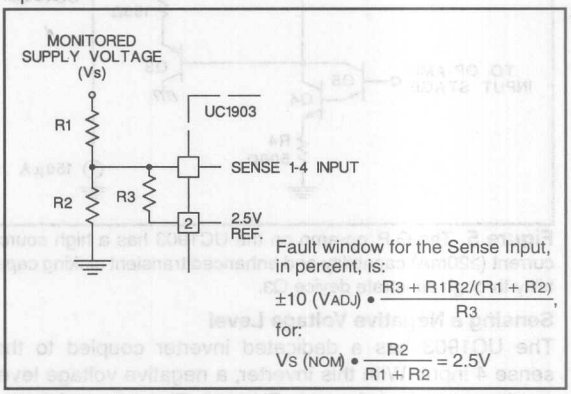


Figure 3. Using the reference output and a resistive divider, a sense input with an independently wider fault window can be generated.

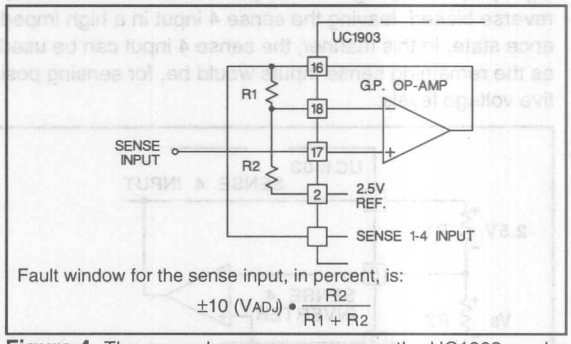


Figure 4. The general purpose op-amp on the UC1903 can be used to create a sense input with an independently tighter fault window.

Figure 4 demonstrates one of many auxiliary functions that the uncommitted op-amp on the UC1903 can be used for. Alternatively, this op-amp can be used to buffer high impedance points, perform logic functions, or for sensing and amplification. For example, the G.P. op-amp, combined with the 2.5V reference, can be used to produce and buffer an optically coupled feedback signal in isolated supplies with primary side control. The output stage of this op-amp is detailed in Figure 5. The NPN emitter follower provides high source current capability. ≥20mA while the substrate device, Q_3, provides good transient sinking capability.

OPERATION AND APPLICATION INFORMATION (continued)

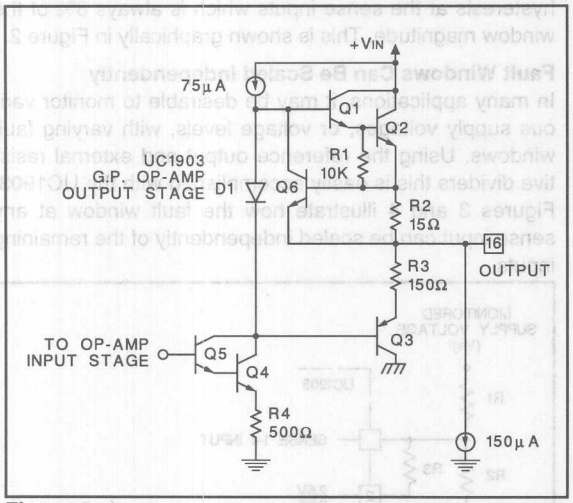
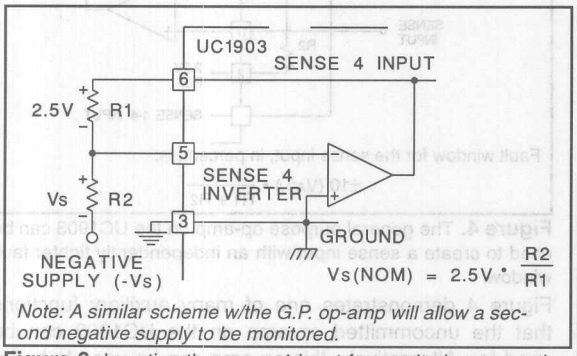


Figure 5. The G.P. op-amp on the UC1903 has a high source current (≥20mA) capability and enhanced transient sinking capability through substrate device Q3.

Sensing a Negative Voltage Level

The UC1903 has a dedicated inverter coupled to the sense 4 input. With this inverter, a negative voltage level can be sensed as shown in Figure 6. The output of the inverter is an unbiased emitter follower. By tying the inverting input, Pin 5, high the output emitter follower will be reverse biased, leaving the sense 4 input in a high impedance state. In this manner, the sense 4 input can be used, as the remaining sense inputs would be, for sensing positive voltage levels.



Note: A similar scheme w/the G.P. op-amp will allow a second negative supply to be monitored.

Figure 6. Inverting the sense 4 input for monitoring a negative supply is accommodated with the dedicated inverter.

Using The Line/Switcher Sense Output

The line switcher sense input to the UC1903 can be used for early detection of line, switcher, or other power source, failures. Internally referenced to 2.0V, the line sense comparator will cause the POWER OK output to indicate a fault (active low) condition when the LINE/SWITCHER SENSE input goes from above to below 2.0V. The line sense comparator has approximately 175mV of hysteresis requiring the line/switcher input to reach 2.175V before the POWER OK output device can be turned off, allowing a no-fault indication. In Figure 7 an example showing the use of the LINE/SWITCHER SENSE input for early switcher-fault detection is detailed. A sample signal is taken from the output of the power transformer, rectified and filtered, and used at the line/switcher input. By adjusting the R_2C time constant with respect to the switching frequency of the supply and the hold up time of the output capacitor, switcher faults can be detected before supply outputs are significantly affected.

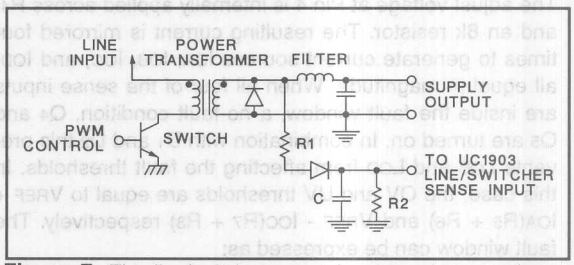


Figure 7. The line/switcher sense input can be used for an early line or switcher fault indication.

OV and UV Comparators Maintain Accurate Thresholds

The structure of the $\overline{OV}$ and $\overline{UV}$ comparators, shown in Figure 8 results in accurate fault thresholds even in the case where multiple sense inputs cross a fault threshold simultaneously. Unused sense inputs can be tied either to the 2.5V reference, or to another, utilized, sense input. The four under- and over-voltage sense inputs on the UC1903 are clamped as detailed on the Sense 1 input in Figure 8. The series 2k resistor, R_1, and zener diode Z_1, prevent extreme under- and over-voltage conditions from inverting the outputs of the fault comparators. A parasitic diode, D_1, is present at the inputs as well. Under normal operation it is advisable to insure that voltage levels at all of the sense inputs stay above -0.3V. The same type of input protection exists at the line sense input, Pin 15, except a 5k series resistor is used.

The fault delay circuitry on the UC1903 is also shown in Figure 8. In the case of an over-voltage condition at one of the sense inputs Q_{20} is turned off, allowing the internal 60µA current source to charge the user-selected delay capacitor. When the capacitor voltage reaches 1.8V, the $\overline{OV}$ and POWER OK outputs become active low. When the fault condition goes away Q_{20} is turned back on, rapidly discharging the delay capacitor. Operation of the under-voltage delay is, with appropriate substitutions, the same.

OPERATION AND APPLICATION INFORMATION (continued)

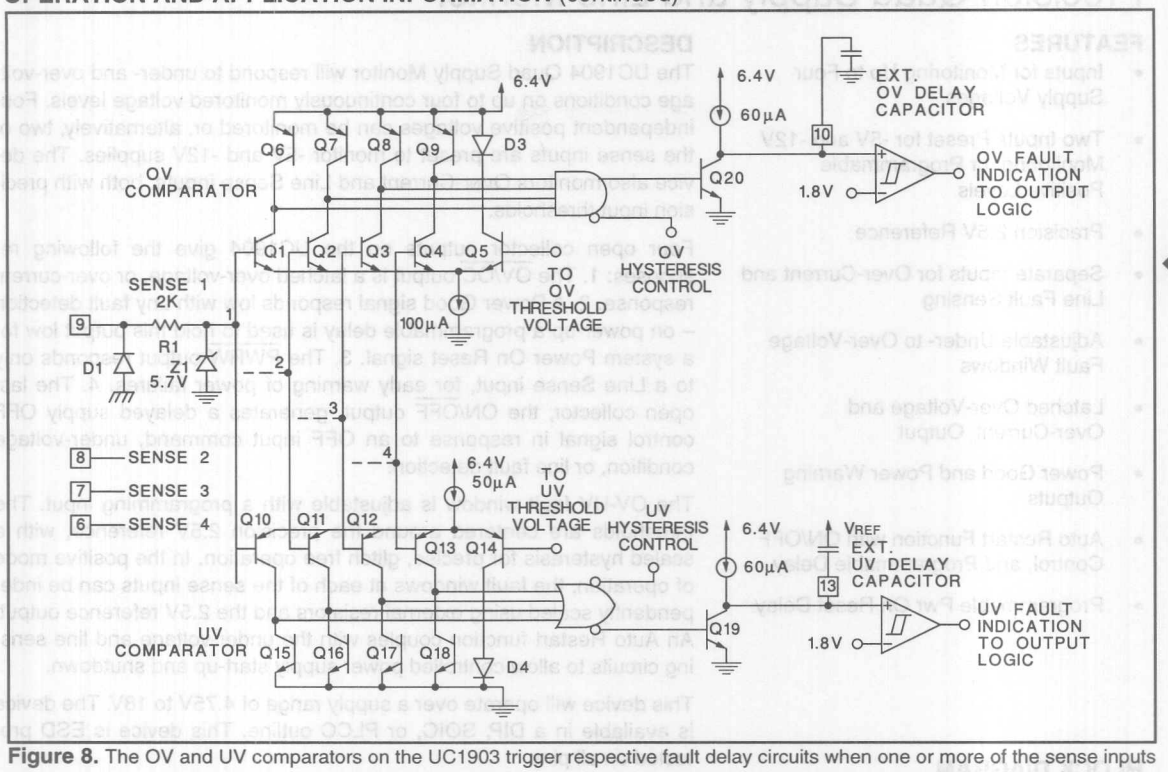


Figure 8. The OV and UV comparators on the UC1903 trigger respective fault delay circuits when one or more of the sense inputs move outside the fault window. Input clamps insure proper operation under extreme fault conditions. Terminating the UV delay capacitor to VREF assures correct logic at power up.

Start Latch and Supply Under-Voltage Sense Allow Predictable Power-Up

The supply under-voltage sense and start-latch circuitry on the UC1903 prevents fault indications during start-up or low input supply (+VIN) conditions. When the input supply voltage is below the supply under-voltage threshold the $\overline{OV}$ and $\overline{UV}$ fault outputs are disabled and the POWER OK output is active low. The POWER OK output will remain active until the input supply drops below approximately 3.0V. With +VIN below this level, all of the open collector outputs will be off.

When the input supply is low, the under-voltage sense circuitry resets the start-latch. With the start-latch reset, the UV fault output will remain disabled until the input supply rises to its normal operating level (8-40V), and all of the sense inputs are above the under-voltage threshold. This allows slow starting, or supply sequencing, without an artificial under-voltage fault indication. Once the latch is set, the UV fault output will respond if any of the sense inputs drop below the under-voltage threshold.

UNITRODE CORPORATION
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Precision Quad Supply and Line Monitor

FEATURES

- Inputs for Monitoring Up to Four Supply Voltages
- Two Inputs Preset for -5V and -12V Monitoring, or Programmable Positive Levels
- Precision 2.5V Reference
- Separate Inputs for Over-Current and Line Fault Sensing
- Adjustable Under- to Over-Voltage Fault Windows
- Latched Over-Voltage and Over-Current Output
- Power Good and Power Warning Outputs
- Auto Restart Function with ON/OFF Control, and Programmable Delay
- Programmable Pwr On Reset Delay

DESCRIPTION

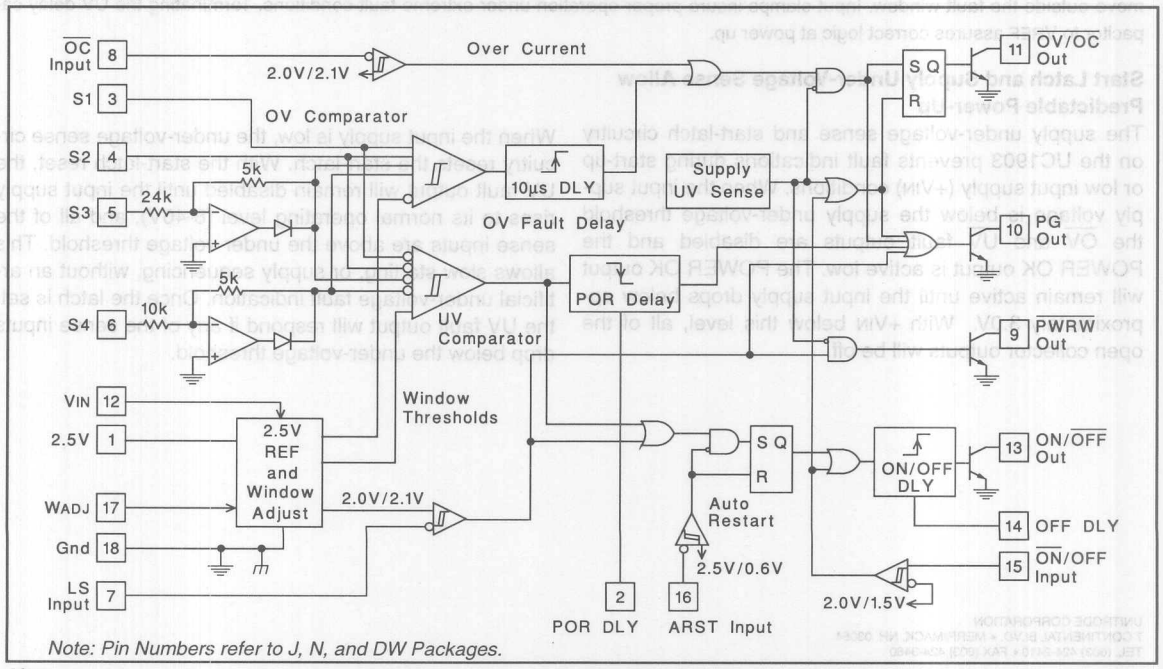
The UC1904 Quad Supply Monitor will respond to under- and over-voltage conditions on up to four continuously monitored voltage levels. Four independent positive voltages can be monitored or, alternatively, two of the sense inputs are preset to monitor -5V and -12V supplies. The device also monitors Over-Current and Line Sense inputs, both with precision input thresholds.

Four open collector outputs on the UC1904 give the following responses: 1. The $\overline{OV}/\overline{OC}$ output is a latched over-voltage, or over-current response. 2. A Power Good signal responds low with any fault detection – on power-up a programmable delay is used to hold this output low for a system Power On Reset signal. 3. The $\overline{PWRW}$ output responds only to a Line Sense input, for early warning of power failures. 4. The last open collector, the ON/$\overline{OFF}$ output, generates a delayed supply OFF control signal in response to an OFF input command, under-voltage condition, or line fault detection.

The OV-UV fault window is adjustable with a programming input. The thresholds are centered around the precision 2.5V reference, with a scaled hysteresis for precise, glitch free operation. In the positive mode of operation, the fault windows at each of the sense inputs can be independently scaled using external resistors and the 2.5V reference output. An Auto Restart function couples with the under-voltage and line sensing circuits to allow controlled power supply start-up and shutdown.

This device will operate over a supply range of 4.75V to 18V. The device is available in a DIP, SOIC, or PLCC outline. This device is ESD protected on all pins.

BLOCK DIAGRAM



Note: Pin Numbers refer to J, N, and DW Packages.

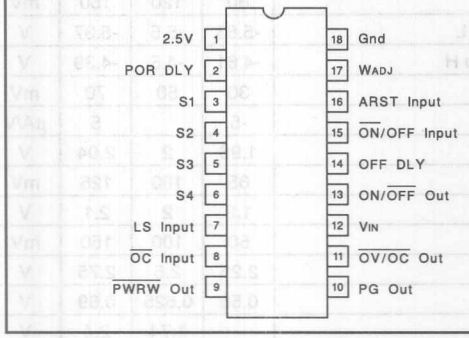
ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Supply Voltage 20V
Sense Inputs, S1 And S2, Other Analog And Logic Inputs
Maximum Forced Voltage . . . . . -0.3V to 10V
Maximum Forced Current . . . . . ±10mA
Sense Input S3, (-12V Sense Input)
Maximum Forced Voltage . . . . . -18V to 10V
Maximum Forced Current . . . . . ±10mA
Sense Input S4, (-5V Sense Input)
Maximum Forced Voltage . . . . . -10V to 10V
Maximum Forced Current . . . . . ±10mA
Open Collector Outputs
Maximum Voltage 20V
Maximum Current 50mA
Reference Output Current . . . . . Internally Limited
Operating Junction Temperature . . . . . -55°C to +150°C
Storage Temperature . . . . . -65°C to +150°C

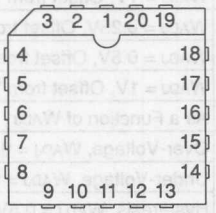
Note 1: Unless otherwise indicated, voltages are reference to ground and currents are positive into, negative out of, the specified terminals.

CONNECTION DIAGRAMS

DIL-18, SOIC-18 (TOP VIEW)
J or N PACKAGE, DW PACKAGE



PLCC-20 (TOP VIEW)
Q PACKAGE



PACKAGE PIN FUNCTION	
FUNCTION	PIN
2.5V	1
POR DLY	2
N.C.	3
S1	4
S2	5
S3	6
S4	7
N.C.	8
LS Input	9
$\overline{OC}$ Input	10
$\overline{PWRW}$ Out	11
PG Out	12
$\overline{OV/OC}$ Out	13
VIN	14
ON/$\overline{OFF}$ Out	15
OFF DLY	16
$\overline{ON}$/OFF Input	17
ARST Input	18
WADJ	19
Gnd	20

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, these specifications hold for T_A = 0 to 70°C for the UC3904, -40 to +85°C for the UC2904, and -55 to +125°C for the UC1904, +VIN = 15V, WADJ = 0.5V, Sense Inputs 1-4, $\overline{OC}$ and LS Inputs = 2.5V. The $\overline{ON}$/OFF Input and the ARST Input = 0V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply					
VIN Supply Current	VIN = 15V		3.2	4.5	mA
VIN UVLO Threshold	Low to High		4.5	4.75	V
UVLO Threshold Hysteresis			50		mV
Minimum VIN to Enable PG Out			0.8	1.5	V
Reference					
Output Voltage(VREF)	T_J = 25°C	2.475	2.5	2.525	V
	Over Temperature, UC3904	2.47		2.53	V
	Over Temperature, UC2904 & UC1904	2.465		2.535	V
Load Regulation	IOUT = 0 to 4mA			6	mV
Line Regulation	VIN = 4.75 to 18V			5	mV
Short Circuit Current	VREF = 0V		17		mA
OV UV Window, LS Input, OC Input, ARST Input, and $\overline{ON}$/OFF Input Thresholds					
Over-Voltage Thresholds S1, S2	WADJ = 0.25V, Offset from VREF, Input L to H	110	125	140	mV
	WADJ = 0.5V, Offset from VREF, Input L to H	230	250	270	mV
	WADJ = 1V, Offset from VREF, Input L to H	460	500	540	mV
Over-Voltage Thresholds S3, S4 Positive Mode	WADJ = 0.25V, Offset from VREF, Input L to H	110	125	145	mV
	WADJ = 0.5V, Offset from VREF, Input L to H	230	250	280	mV
	WADJ = 1V, Offset from VREF, Input L to H	460	500	550	mV

ELECTRICAL CHARACTERISTICS (cont): Unless otherwise stated, these specifications hold for T_A = 0 to 70°C for the UC3904, -40 to +85°C for the UC2904, and -55 to +125°C for the UC1904, +V_{IN} = 15V, W_{ADJ} = 0.5V, Sense Inputs 1-4, $\overline{OC}$ and LS Inputs = 2.5V. The $\overline{ON}$/OFF Input and the ARST Input = 0V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
OV UV Window, LS Input, OC Input, ARST Input, and $\overline{ON}$/OFF Input Thresholds (cont.)					
Under-Voltage Thresholds S1, S2	W_{ADJ} = 0.25V, Offset from V_{REF}, Input H to L	-140	-125	-110	mV
	W_{ADJ} = 0.5V, Offset from V_{REF}, Input H to L	-270	-250	-230	mV
	W_{ADJ} = 1V, Offset from V_{REF}, Input H to L	-540	-500	-460	mV
Under-Voltage Thresholds S3, S4 Positive Mode	W_{ADJ} = 0.25V, Offset from V_{REF}, Input H to L	-150	-125	-110	mV
	W_{ADJ} = 0.5V, Offset from V_{REF}, Input H to L	-285	-250	-230	mV
	W_{ADJ} = 1V, Offset from V_{REF}, Input H to L	-555	-500	-460	mV
OV and UV Threshold Hysteresis	As a Function of W_{ADJ}	30	50	70	mV/V
S3 Negative Mode Thresholds	Over-Voltage, W_{ADJ} = 0.5V, Input H to L	-13.52	-13.2	-12.88	V
	Under-Voltage, W_{ADJ} = 0.5V, Input L to H	-11.06	-10.8	-10.54	V
	Hysteresis, W_{ADJ} = 0.5V	80	120	160	mV
S4 Negative Mode Thresholds	Over-Voltage, W_{ADJ} = 0.5V, Input H to L	-5.63	-5.5	-5.37	V
	Under-Voltage, W_{ADJ} = 0.5V, Input L to H	-4.61	-4.5	-4.39	V
	Hysteresis, W_{ADJ} = 0.5V	30	50	70	mV
W_{ADJ} Input Bias Current	0.25V < W_{ADJ} <1.0V	-5		5	µA/V
LS Threshold	Input = H to L	1.96	2	2.04	V
	Threshold hysteresis	65	100	125	mV
$\overline{OC}$ Threshold	Input = H to L	1.9	2	2.1	V
	Threshold hysteresis	50	100	150	mV
ARST Input Threshold	Input = L to H	2.25	2.5	2.75	V
	Input = H to L	0.56	0.625	0.69	V
$\overline{ON}$/OFF Input Threshold	Input high level		1.74	2.4	V
	Input low level	0.6	1.35		V
Sense and Logic Input Bias Currents					
Sense 1-4, Positive Mode	Input = 2.8V		250	800	nA
	Input = 2.2V	-1000	-250		nA
Sense 3 Negative Mode	Input = -12V	-700	-500	-300	µA
Sense 4 Negative Mode	Input = -5V	-700	-500	-300	µA
Line, and OC Inputs	Input = 2.2V		300	1000	nA
$\overline{ON}$/OFF Input	Input = 2.5V		150	600	nA
ARST Input	Input = 0.5	-2000	-700		nA
Open Collector Outputs ($\overline{OV}$/$\overline{OC}$ Out, PG Out, $\overline{PWRW}$ Out, $\overline{ON}$/$\overline{OFF}$ Out)					
Saturation Voltage	I_{OUT} = 10mA		0.2	0.4	V
Leakage current	V_{OUT} = 20V			5	µA
POR Delay					
Delay		160	250	350	ms/µF
Internal Pullup Current			9		µA
Threshold Low to High			2.25		V
OFF Delay					
Delay		120	185	250	ms/µF
Internal Pullup current			12		µA
Threshold Low to High			2.25		V
OV Fault Delay					
Delay		10	20	50	µs

PIN FUNCTIONAL DESCRIPTION

2.5V: This is the output of the precision 2.5V reference.

ARST Input: This input, with a 4:1 hysteretic threshold, is used to sequence a power system through the **A**uto **R**e**S**tar**T** cycle. A delayed representation of a supply output voltage is used at this pin to provide adequate startup time for the power system, and a minimum power-off period.

Gnd: Reference point for the internal reference and all thresholds, as well as the return for the remainder of the device.

LS Input: The **L**ine **S**ense input is used to monitor a voltage that varies with the input line voltage to a system. The input is compared to a precision 2.0V level and is used to activate the $\overline{\text{PWRW}}$ and PG outputs, as well as triggering the Auto Restart sequence.

$\overline{\text{OC}}$ Input: The **O**ver-**C**urrent input can be used to respond to an inverted over-current signal. A low level signal at this input latches in a fault indication at the **$\overline{\text{OV/OC}}$** output.

OFF DLY: This pin functions similarly to the **POR DLY** pin to delay the turn-on of the ON/$\overline{\text{OFF}}$ output transistor. The charging current and upper threshold are 12µA and 2.1V.

$\overline{\text{ON/OFF}}$ Input: With a high level at this input the **ON/$\overline{\text{OFF}}$ Out** pin is activated after a user-programmable delay. A high level also activates the **PG Out** pin, and resets the **OV/OC** fault latch.

On/$\overline{\text{Off}}$ Out: This output is an open collector output that is activated by the **$\overline{\text{ON/OFF}}$ Input**, or the Auto Restart circuitry. Saturation voltage on this and all the open collector outputs is rated at 10mA of current.

$\overline{\text{OV/OC}}$ Out: In response to either an **O**ver-**V**oltage or **O**ver-**C**urrent situation this output is latched active low. There is nominal 20µs delay in the OV path to the fault latch, providing rejection to transient overshooting on the monitored voltages. The low condition is cleared when the fault latch is reset by the **$\overline{\text{ON/OFF}}$ Input**, or a **UVLO** condition on the device.

POR DLY: This pin is used, with an external capacitor, to program a **P**ower-**O**n-**R**eset delay. This delay is reset whenever there is a UV condition at one of the S1-S4 inputs, and then triggered upon the clearing of the UV condition. When reset, the voltage across the capacitor is quickly discharged to near zero volts, and the **PG Out** pin goes active low. Once triggered the capacitor is charged by a 9µA current source. The **PG Out** pin remains active low until the delay capacitor voltage reaches a 2.1V threshold.

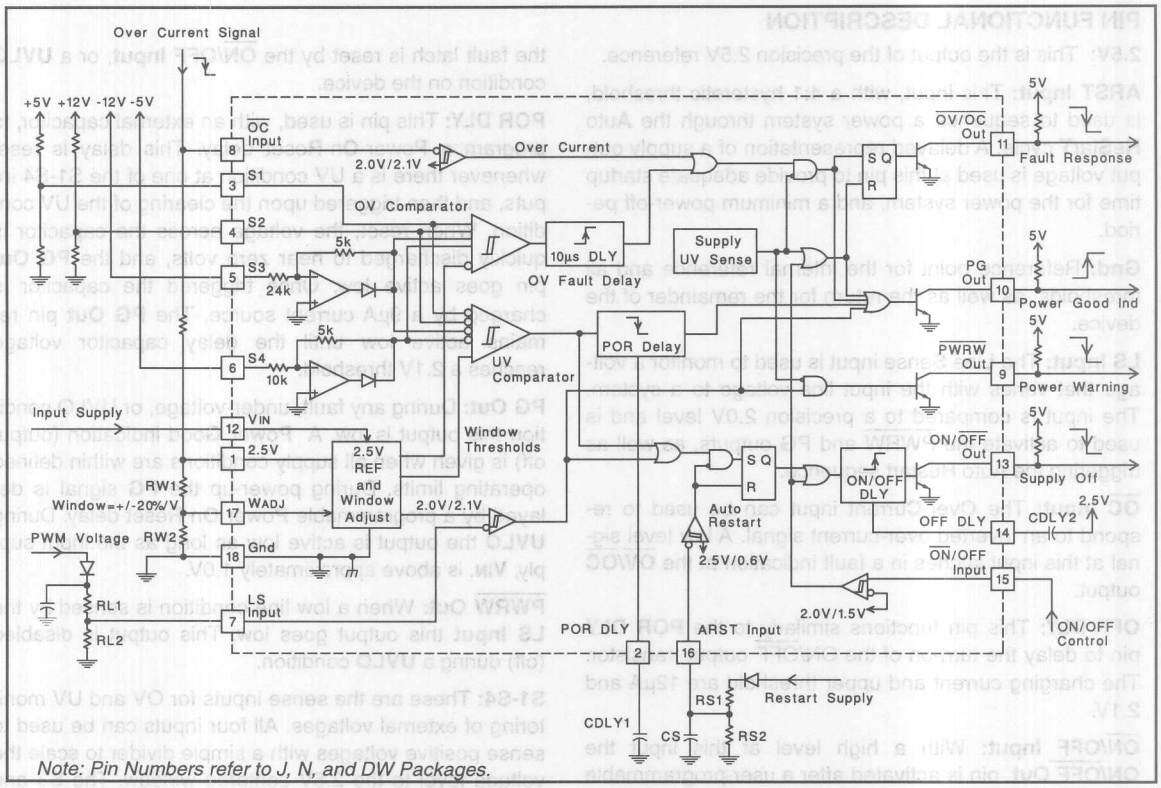
PG Out: During any fault, under-voltage, or UVLO condition this output is low. A **P**ower **G**ood indication (output off) is given when all supply conditions are within defined operating limits. During power-up the **PG** signal is delayed by a programmable **P**ower **O**n **R**eset delay. During **UVLO** the output is active low as long as the input supply, **VIN**, is above approximately 1.0V.

$\overline{\text{PWRW}}$ Out: When a low line condition is sensed by the **LS Input** this output goes low. This output is disabled (off) during a **UVLO** condition.

S1-S4: These are the sense inputs for OV and UV monitoring of external voltages. All four inputs can be used to sense positive voltages with a simple divider to scale the voltage level to the 2.5V centered window. The **S3** and **S4** inputs can also be used to sense -12V and -5V supplies respectively with no external components. This is done with internal precision resistor dividers and two source only op-amps that are disabled when the pins are used in the positive mode.

VIN: Input supply for the UC1904. The device is operational with 4.75V to 18V on this pin.

WADJ: The **WADJ** input is used to program the OV and UV window thresholds. The OV-UV window is centered around the 2.5V reference and is nominally ±20% per volt on the **WADJ** input pin.



Note: Pin Numbers refer to J, N, and DW Packages.

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

Load Share Controller

FEATURES

- Fully Differential High Impedance Voltage Sensing
- Accurate Current Amplifier for Precise Current Sharing
- Opto Coupler Driving Capability
- 1.25% Trimmed Reference
- Master Status Indication
- Compatible with JIAWG 88-M7A Specification
- 4.5V TO 35V Operation

DESCRIPTION

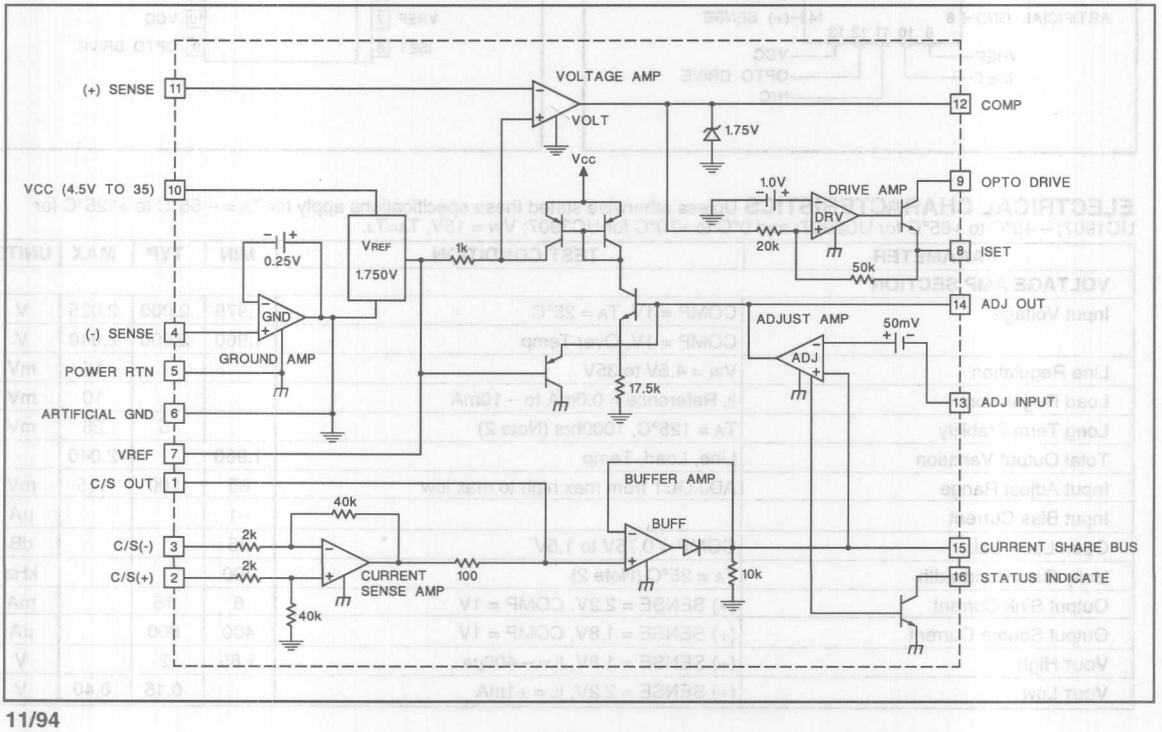
The UC3907 family of Load Share Controller ICs provides all the necessary features to allow multiple independent power modules to be paralleled such that each module supplies only its proportionate share to total load current.

This sharing is accomplished by controlling each module's power stage with a command generated from a voltage feedback amplifier whose reference can be independently adjusted in response to a common share bus voltage. By monitoring the current from each module, the current share bus circuitry determines which paralleled module would normally have the highest output current and, with the designation of this unit as the master, adjusts all the other modules to increase their output current to within 2.5% of that of the master.

The current share bus signal interconnecting all the paralleled modules is a low-impedance, noise-insensitive line which will not interfere with allowing each module to act independently should the bus become open or shorted to ground. The UC3907 controller will reside on the output side of each power module and its overall function is to supply a voltage feedback loop. The specific architecture of the power stage is unimportant. Either switching or linear designs may be utilized and the control signal may be either directly coupled or isolated though the use of an opto coupler or other isolated medium. The load sharing technique implemented with the UC3907 is compatible with the requirements of JIAWG 88-M7A specifications.

Other features of the UC3907 include 1.25% accurate reference: a low-loss, fixed gain current sense amplifier, a fully differential, high-impedance voltage sensing capability, and a status indicator to designate which module is performing as master.

BLOCK DIAGRAM



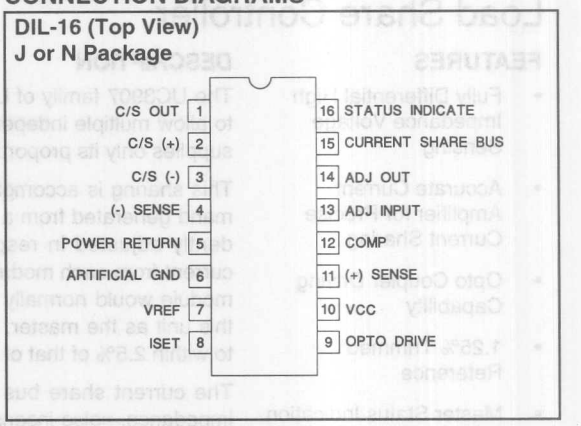
ABSOLUTE MAXIMUM RATINGS

Supply Voltage.....+35V
Opto Out Voltage.....+35V
Opto Out Current.....+20mA
Status Indicate Sink Current.....+20mA
C/S Input Voltage.....+35V
Share Bus Voltage.....– 0.3V to +35V
Other Analog Inputs and Outputs (Zener clamped)
Maximum Forced Voltage.....– 0.3V to +10V
Maximum Forced Current.....±10mA
Ground Amp Sink Current.....+50mA
Pins 1, 9, 12, 15 Sink Current.....+20mA
Storage Temperature Range.....– 65°C to +150°C
Junction Temperature.....– 55°C to +150°C
Lead Temperature (Solder 10 Seconds).....+300°C

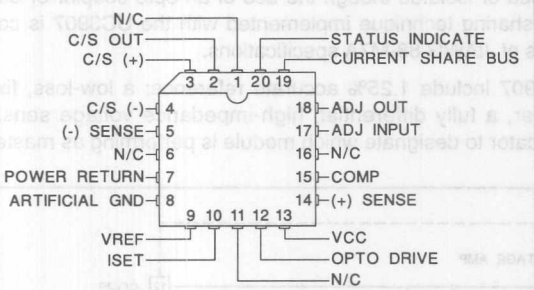
Pin Nos. refer to 16 Pin DIL Package
Currents are positive into, negative out of the specified terminal.
Consult packaging section of databook for thermal limitations and considerations of package.

CONNECTION DIAGRAMS

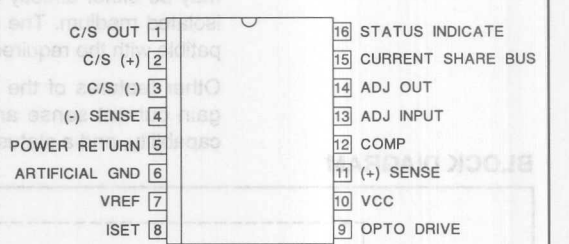
DIL-16 (Top View)
J or N Package



PLCC–20, LCC–20 (Top View)
Q PACKAGE, L PACKAGE



SOIC-16 (Top View)
DW Package



ELECTRICAL CHARACTERISTICS

Unless otherwise stated these specifications apply for T_A = – 55°C to +125°C for UC1907; – 40°C to +85°C for UC2907; and 0°C to +70°C for UC3907; V_{IN} = 15V, T_A=T_J.

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
VOLTAGE AMP SECTION					
Input Voltage	COMP = 1V, T_A = 25°C	1.975	2.000	2.025	V
	COMP = 1V, Over Temp	1.960	2.000	2.040	V
Line Regulation	V_{IN} = 4.5V to 35V			15	mV
Load Regulation	I_L Reference = 0.0mA to – 10mA			10	mV
Long Term Stability	T_A = 125°C, 1000hrs (Note 2)		5	25	mV
Total Output Variation	Line, Load, Temp	1.960		2.040	
Input Adjust Range	ADJ OUT from max high to max low	85	100	115	mV
Input Bias Current		–1			µA
Open Loop Gain	COMP = 0.75V to 1.5V	65			dB
Unity Gain Bandwidth	T_A = 25°C (Note 2)	700			kHz
Output Sink Current	(+) SENSE = 2.2V, COMP = 1V	6	15		mA
Output Source Current	(+) SENSE = 1.8V, COMP = 1V	400	600		µA
V_{OUT} High	(+) SENSE = 1.8V, I_L= – 400µa	1.85	2		V
V_{OUT} Low	(+) SENSE = 2.2V, I_L = +1mA		0.15	0.40	V

ELECTRICAL CHARACTERISTICS (cont.) Unless otherwise stated these specifications apply for T_A = – 55°C to +125°C for UC1907; – 40°C to +85°C for UC2907; and 0°C to +70°C for UC3907; V_{IN} = 15V, T_A=T_J.

PARAMETER	TEST CONDITION		MIN	TYP	MAX	UNITS
REFERENCE SECTION						
Output Voltage	T_A = 25°C		1.970	2.000	2.030	V
	Over Operating Temp		1.955	2.000	2.045	V
Short Circuit Current	VREF = 0.0V		– 15	– 30	– 60	mA
GROUND AMP SECTION						
Output Voltage			200	250	300	mV
Common Mode Variation	(–) SENSE from 0.0V to 2V				5	mV
Load Regulation	I_L = 0.0mA to 20mA, T_A = 25°C				10	mV
	I_L = 0.0mA to 20mA, Over Temp				15	mV
ADJUST AMP SECTION						
Input Offset Voltage	ADJ OUT = 1.5V, Vcm = 0.0V		40	50	60	mV
Input Bias Current			– 2			µA
Open Loop Gain	1.5V≤ ADJ OUT≤ 2.25V		65			dB
Unity Gain Bandwidth	T_A = 25°C, C_{OUT} =1µF (Note 2)			500		Hz
Transconductance	I_{OUT} = – 10µA to +10µA, V_{OUT} = 1.5V		1.7	3	4.5	ms
Output Sink Current	Vid = 0.0V, ADJ OUT = 1.5V		55	135	225	µA
Output Source Current	Vid = 250mV, ADJ OUT = 1.5V		110	200	350	µA
V_{OUT} High	Vid = 250mV, I_{OUT} = – 50µA		2.20	2.70	2.90	V
V_{OUT} Low	Vid = 0.0V, I_{OUT} = 50µA			0.75	1.15	V
Common Mode Rejection Ratio	Vcm = 0.0 to 10V		70			dB
Output Gain to V/A	V_{OUT} ADJ OUT = 1.5V to 2V		50	57	64	mV/V
	Δ(+) SENSE/ ΔADJ OUT					
CURRENT AMP SECTION						
Gain	Vcm = 0.0V, Vid = 50mV to 100mV		19.2	19.6	20.1	V/V
Output Voltage	Vc/s (+) = Vc/s (-) = 0.0V	T_A = 25°C	210	250	290	mV
		Over Temp	180	250	330	mV
Input Offset Change with Common Mode Input	Vcm = 0V to 13V				600	µV/V
V_{OUT} High	Vid = 1V		10	14.5		V
V_{OUT} Low	Vid = – 1V, I_L = 1mA			350	450	mV
Power Supply Rejection Ratio	V_{IN} = 4.5V to 35V, Vcm = 0.0V		60			dB
Slew Rate				0.4		V/µs
DRIVE AMP SECTION Rset = 500 ohms to Artificial Gnd, Opto Drive = 15V						
Voltage Gain	COMP = 0.5V to 1V		2.3	2.5	2.6	V/V
ISET V_{OUT} High	(+) SENSE = 2.2V		3.8	4.1	4.4	V
ISET V_{OUT} Low	(+) SENSE = 1.8V			270	300	mV
Opto out Voltage Range			4		35	V
Zero Current Input Threshold			1.55	1.65	1.75	V
BUFFER AMP SECTION						
Input Offset Voltage	Input = 1V				5	mV
Output Off Impedance	Input = 1V, Output = 1.5V to 2V		5	10	20	kΩ
Output Source Current	Input = 1V, Output = 0.5V		6	15		mA
Common Mode Rejection Ratio	Vcm = 0.3V to 10V		70			dB
Power Supply Rejection Ratio	V_{IN} = 4.5V to 35V		70			dB

ELECTRICAL CHARACTERISTICS (cont.) Unless otherwise stated these specifications apply for T_A = – 55°C to +125°C for UC1907; – 40°C to +85°C for UC2907; and 0°C to +70°C for UC3907; V_{IN} = 15V, T_A=T_J

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
UNDER VOLTAGE LOCKOUT SECTION					
Startup Threshold			3.7	4.4	V
Threshold Hysteresis			200		mV
STATUS INDICATE SECTION					
V_{OUT} Low	ADJ OUT = Current Share Bus		0.2	0.5	V
Output Leakage	ADJ OUT = 1V, V_{OUT} = 35V		0.1	5	µA
TOTAL STAND BY CURRENT SECTION					
Startup Current	V_{IN} = UVLO – 0.2V		3	5	mA
Operating Current	V_{IN} = 35V		6	10	mA

NOTE 1: Unless otherwise specified all voltages are with respect to (–) SENSE. Currents are positive into, negative out of the specified terminal.

NOTE 2: Guaranteed by design. Not 100% tested in production.

PIN/BLOCK DESCRIPTIONS

(–) SENSE (Pin 4) - This is a high-impedance pin intended to allow remote sensing of the system ground, bypassing any voltage drops which might appear in the power return line. **This point should be considered as the "true" ground. Unless otherwise stated, all voltages are with respect to this point.**

ARTIFICIAL GROUND (Pin 6) - This is a low impedance circuit ground which is exactly 250 millivolts above the (–) SENSE terminal. This offset allows the Ground Buffer Amplifier negative headroom to return all the control bias and operating currents while maintaining a high impedance at the (–) SENSE input.

POWER RTN (Pin 5) - This should be the most negative voltage available and can range from zero to 5V below the (–) SENSE terminal. It should be connected as close to the power source as possible so that voltage drops across the return line and current sensing impedances lie between this terminal and the (–) SENSE point.

VREF (Pin 7) - The internal Voltage Reference is a band-gap circuit set at 2.0 Volts with respect to the (–) SENSE input (1.75V above the ARTIFICIAL GROUND), and an accuracy of ± 1.5%. This circuit, as well as all the other chip functions, will work over a supply voltage range of 4.5V to 35V allowing operation from unregulated DC, an auxiliary voltage, or the same output voltage that it is controlling. Under voltage lockout has been included to insure proper startup by disabling internal bias currents until the reference rises into regulation.

VOLTAGE AMPLIFIER (Pins 11, 12) - This circuit is the feedback control gain stage for the power module's output voltage regulation, and overall loop compensation will normally be applied around this amplifier. Its output will swing from slightly above the ground return to an internal clamp of 2.0 Volts. The reference trimming is performed closed loop, and measured at pin 11, (+) SENSE. The value is trimmed to 2V ±1.25%.

DRIVE AMPLIFIER (Pins 8, 9, 12) - This amplifier is used as an inverting buffer between the Voltage Amplifier's output and the medium used to couple the feedback signal to the power controller. It has a fixed voltage gain of 2.5 and is usually configured with a current-setting resistor to ground. This establishes a current - sinking output optimized to drive optical couplers biased at any voltage from 4.5V to 35V, with current levels up to 20mA. The polarity of this stage is such that an increasing voltage at the Voltage Amplifier's sense input (as, for example, at turn on) will increase the opto's current. In a nonisolated application, a voltage signal ranging from 0.25V to 4.1V may be taken from the current-setting output but it should be noted that this voltage will also increase with increasing sense voltage and an external inverter may be required to obtain the correct feedback polarity.

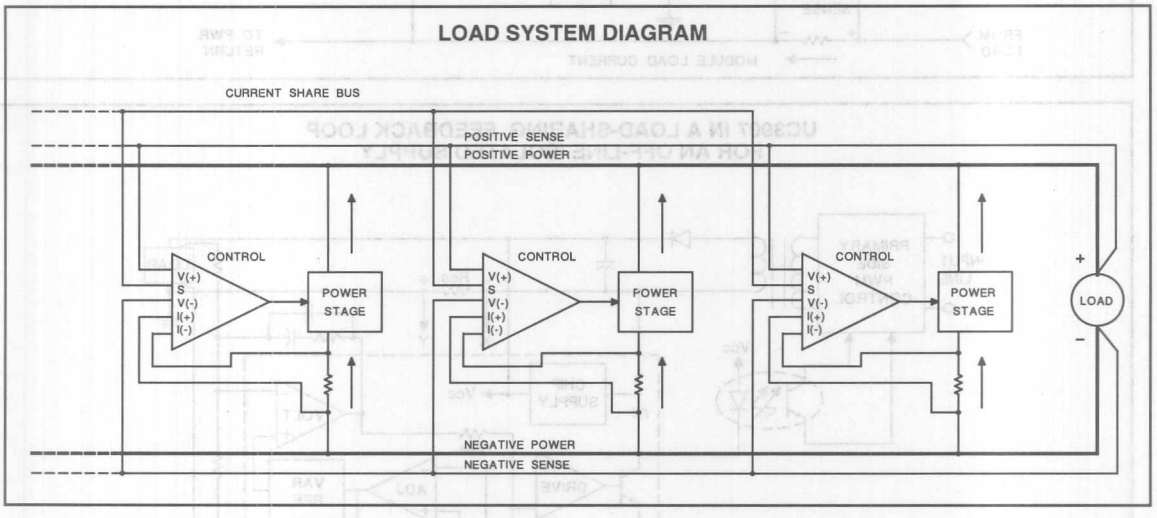
CURRENT AMPLIFIER (Pins 1, 2, 3) - This amplifier has differential sensing capability for use with an external shunt in the power return line. The common-mode range of its input will accommodate the full range between the Power Return point and VCC–2V which will allow undefined line impedances on either side of the current shunt. The gain is internally set at 20 giving the user the ability to establish the maximum voltage drop across the current sense resistor at any value between 50 and 500 millivolts. While the band-width of this amplifier may be reduced with the addition of an external output capacitor to ground, in most cases this is not required as the compensation of the Adjust Amplifier will typically form the dominant pole in the adjust loop.

PIN/BLOCK DESCRIPTIONS (cont.)

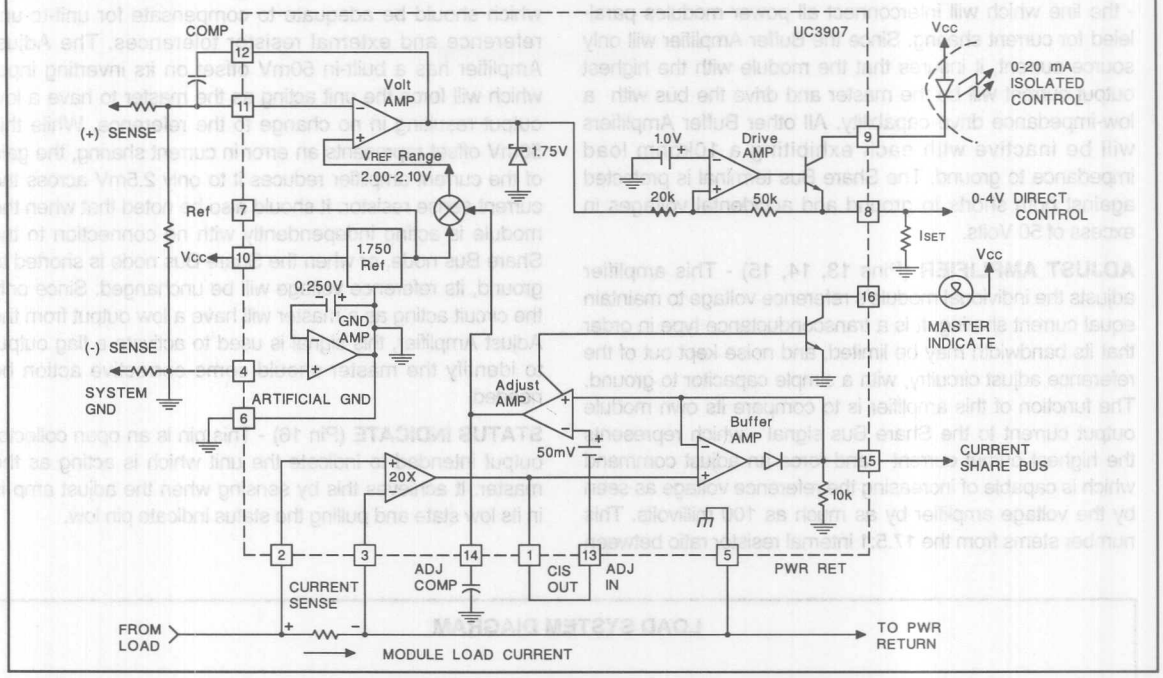
BUFFER AMPLIFIER (Pins 1, 15) - This amplifier is a unidirectional buffer which drives the CURRENT SHARE BUS - the line which will interconnect all power modules paralleled for current sharing. Since the Buffer Amplifier will only source current, it insures that the module with the highest output current will be the master and drive the bus with a low-impedance drive capability. All other Buffer Amplifiers will be inactive with each exhibiting a 10kohm load impedance to ground. The Share Bus terminal is protected against both shorts to ground and accidental voltages in excess of 50 Volts.

ADJUST AMPLIFIER (Pins 13, 14, 15) - This amplifier adjusts the individual module's reference voltage to maintain equal current sharing. It is a transconductance type in order that its bandwidth may be limited, and noise kept out of the reference adjust circuitry, with a simple capacitor to ground. The function of this amplifier is to compare its own module output current to the Share Bus signal - which represents the highest output current - and force an adjust command which is capable of increasing the reference voltage as seen by the voltage amplifier by as much as 100 millivolts. This number stems from the 17.5:1 internal resistor ratio between the Adjust Amplifier's clamped output and the reference, and represents a 5% total range of adjustment - a value which should be adequate to compensate for unit-to-unit reference and external resistor tolerances. The Adjust Amplifier has a built-in 50mV offset on its inverting input which will force the unit acting as the master to have a low output resulting in no change to the reference. While this 50mV offset represents an error in current sharing, the gain of the current amplifier reduces it to only 2.5mV across the current sense resistor. It should also be noted that when the module is acting independently with no connection to the Share Bus node, or when the Share Bus node is shorted to ground, its reference voltage will be unchanged. Since only the circuit acting as a master will have a low output from the Adjust Amplifier, this signal is used to activate a flag output to identify the master should some corrective action be needed.

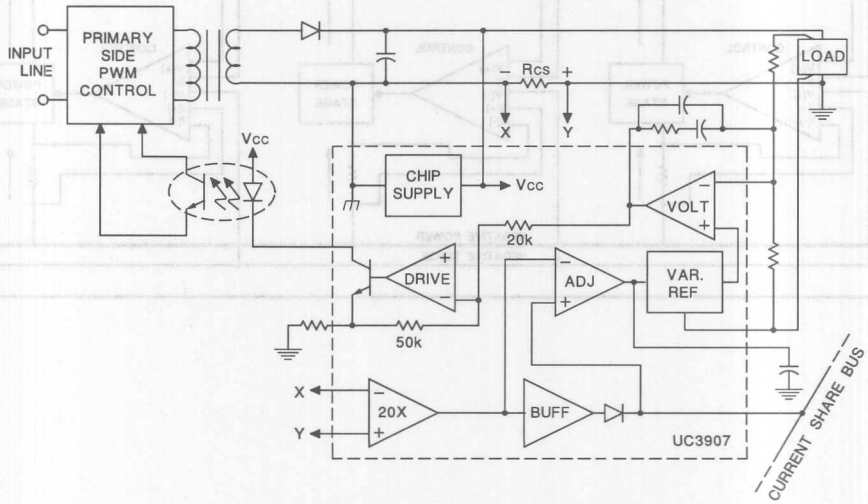
STATUS INDICATE (Pin 16) - This pin is an open collector output intended to indicate the unit which is acting as the master. It achieves this by sensing when the adjust amp is in its low state and pulling the status indicate pin low.



LOAD SHARE CONNECTION DIAGRAM



UC3907 IN A LOAD-SHARING FEEDBACK LOOP FOR AN OFF-LINE ISOLATED SUPPLY



UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. 603-424-2410 • FAX 603-424-3460

Programmable Voltage Clamp

FEATURES

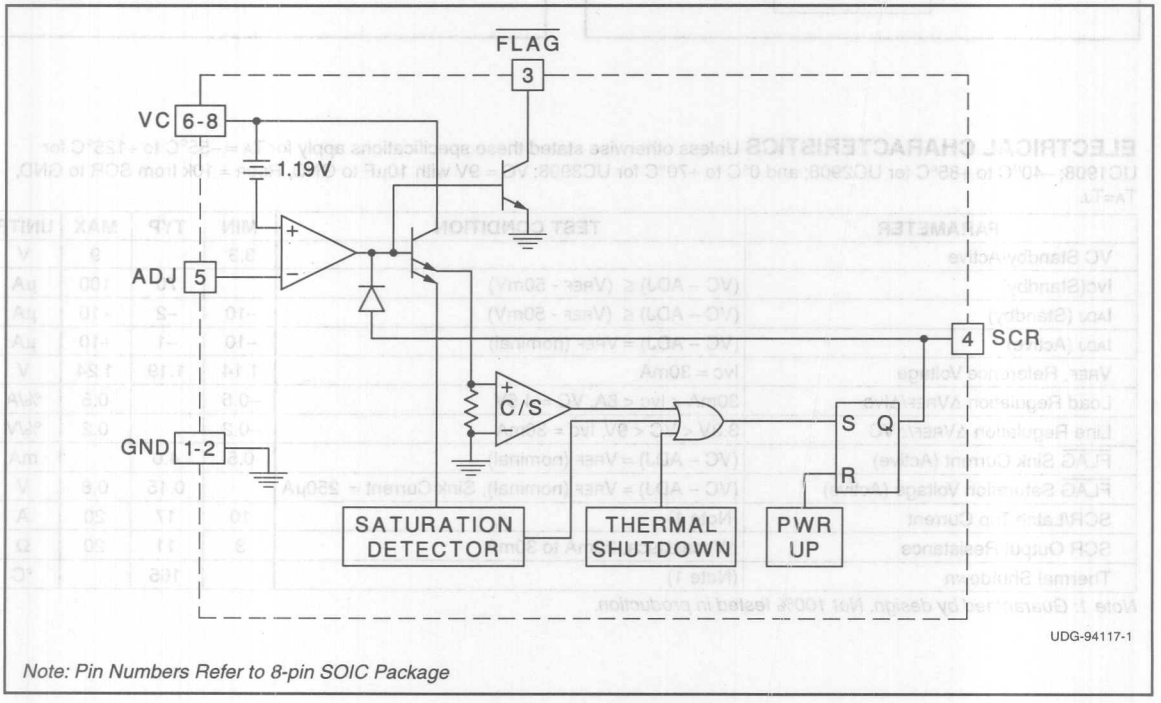
- Shunt Regulator Keeps Power Supply Overvoltage to a Predetermined Level
- Programmable Input From 3.3V to 9V
- Internal 1.19V Floating Reference from VC Accurate to ±4.2%
- Up to 17A Shunt Regulator Automatically Activated
- Gate Drive to External SCR Provided if Fault Persists
- Overvoltage Flag Available for Duration of Fault
- Requires Less Than 100µA in Standby Mode

DESCRIPTION

The UC3908 is a programmable voltage clamp designed to protect a power supply load in the event of an overvoltage. The UC3908 is a shunt regulator which, under an overvoltage condition, regulates the output voltage to programmed maximum value. It also provides a gate signal to an external SCR which crowbars the output if the shunted current exceeds a maximum value, if the chip's thermal shutdown circuitry is activated, or if the shunt regulator is saturated.

The UC3908 compares a divided down portion of the power supply output to an internal reference. If the output is below the trip point, the UC3908 remains in standby mode, draws less than 100µA, and no action occurs. If the monitored voltage is above the trip point, the UC3908 shunts up to 17A of current to keep the output voltage within its prescribed limit and activates the $\overline{\text{FLAG}}$ signal. In effect the UC3908 acts as a dynamic filter to reduce power supply output voltage transients to acceptable levels. If the shunted current exceeds the maximum value, if chip junction temperature exceeds 165°C, or if the shunt transistor is saturated, a gate drive signal is sent to an external SCR to short circuit the output to ground. An internal latch is also activated to turn on the shunt transistor fully to minimize power dissipation under these conditions.

BLOCK DIAGRAM



Note: Pin Numbers Refer to 8-pin SOIC Package

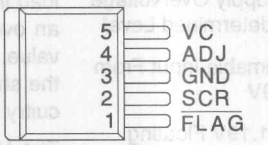
ABSOLUTE MAXIMUM RATINGS

Supply Voltage, VC 9V
Supply Current, IVC 20A
Input Voltage Range .....–0.3V to 9V
SCR/Latch Trip Current 20A
Storage Temperature .....–65°C to +150°C
Operating Junction Temperature .....–55°C to +150°C
Lead Temperature (Soldering, 10 sec.) .....+300°C

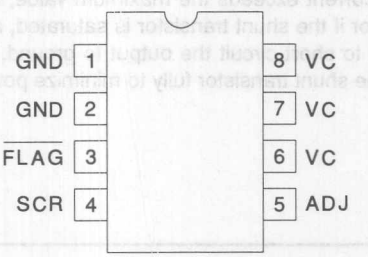
Unless otherwise indicated, voltages are referenced to ground and currents are positive into, negative out of, the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAMS

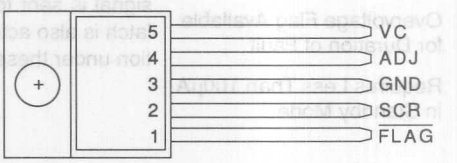
5-PIN TO-263 (FRONT VIEW)
TD PACKAGE



SOIC-8 (TOP VIEW)
D PACKAGE



5-PIN TO-220 (TOP VIEW)
T PACKAGE



ELECTRICAL CHARACTERISTICS

Unless otherwise stated these specifications apply for T_A = –55°C to +125°C for UC1908; –40°C to +85°C for UC2908; and 0°C to +70°C for UC3908; VC = 9V with 10µF to GND, R_{SCR} = 10k from SCR to GND, T_A=T_J.

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
VC Standby/Active		3.3		9	V
IVC(Standby)	(VC – ADJ) ≤ (V_{REF} - 50mV)		70	100	µA
I_{ADJ} (Standby)	(VC – ADJ) ≤ (V_{REF} - 50mV)	–10	–2	+10	µA
I_{ADJ} (Active)	(VC – ADJ) = V_{REF} (nominal)	–10	–1	+10	µA
V_{REF}, Reference Voltage	IVC = 30mA	1.14	1.19	1.24	V
Load Regulation $\Delta V_{REF}/\Delta I_{VC}$	30mA < IVC < 8A, VC = 4.5V	–0.5		0.5	%/A
Line Regulation $\Delta V_{REF}/\Delta VC$	3.3V < VC < 9V, IVC = 30mA	–0.2		0.2	%/V
$\overline{FLAG}$ Sink Current (Active)	(VC – ADJ) = V_{REF} (nominal)	0.5	4.0		mA
$\overline{FLAG}$ Saturation Voltage (Active)	(VC – ADJ) = V_{REF} (nominal), Sink Current = 250µA		0.15	0.8	V
SCR/Latch Trip Current	(Note 1)	10	17	20	A
SCR Output Resistance	$\Delta V_{SCR}/\Delta I_{SCR}$, 20mA to 30mA	3	11	20	Ω
Thermal Shutdown	(Note 1)		165		°C

Note 1: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

ADJ: ADJ pin is used for the voltage divider from VC to set up the maximum VC value (VCmax) as calculated below. V_{REF}, nominally 1.19V, is the reference voltage which controls the shunt regulator and whether the UC3908 is in its inactive (standby) or active state. When VC is less than

$$(V_{REF} - 50mV) \cdot \frac{(R1+R2)}{R1},$$

UC3908 is in the standby state. In this state, the device draws only 70µA and the shunt regulator is turned off. Above this point, as VC approaches

$$V_{REF} \cdot \frac{(R1+R2)}{R1} \text{ (or VCmax)},$$

the UC3908 smoothly transitions into its active state and controls the shunt regulator to maintain VC at this pre-programmed maximum voltage.

Referring to Figure 11, the resistor divider between VC and GND which forms the feedback control for ADJ is calculated as follows:

$$VCmax = V_{REF} \cdot \frac{(R1+R2)}{R1}$$

where the user selects one resistor value and VCmax and solves for the other resistor value. Since the signal at ADJ is compared to a VC referenced voltage, any voltage error induced by the shunt regulator and its ground return are eliminated from the feedback path.

FLAG: FLAG is an open collector output which becomes active low during an overvoltage condition. This pin can typically sink 1mA.

GND: This pin is the return point for all device currents. It carries the full current shunted by the UC3908.

SCR: The gate of an external SCR is connected to this pin. Normally, the SCR pin is in an inactive state (low). When active, the SCR pin is pulled to within 1V of VC. This pin then produces enough drive current to trigger the gate of the external SCR. Figure 10 illustrates the relationship between available gate current and the difference between Vc and the SCR pin voltage (Vc - V_{SCR}). An external SCR is recommended to guarantee that the system stays at a safe shutdown voltage during a catastrophic fault until the system can be turned off and repaired. An external SCR is also needed for its ability to sink greater current levels at lower voltages than the UC3908 and to provide a clamp in a situation where the UC3908 can fail. The UC3908 fails open circuit.

VC: VC is the power input connection for this device. Its input range is from 3.3V to 9V. The quiescent VC current is typically 70µA when inactive, but the UC3908 can draw up to 17A when the shunt regulator is active. The instantaneous current is a function of the control loop sensing the changes at VC. VC is the reference point for the 1.19V reference.

APPLICATION INFORMATION

Protecting sensitive circuitry from power supply overvoltage conditions is a concern for any system designer. Overvoltage conditions can be caused by transient load changes, loss of the power supply control loop, accidental miswiring or incorrect module installation. An intelligent protection scheme can be accomplished utilizing the UC3908 programmable voltage clamp.

The UC3908 monitors a power supply output voltage and draws less than 100µA if no overvoltage condition is present. If an overvoltage condition occurs, the UC3908 will act as a shunt regulator and attempt to regulate the power supply to a programmed level by internally shunting current from VC to ground. An internal latch is activated and SCR signal is asserted under one of the following three conditions :

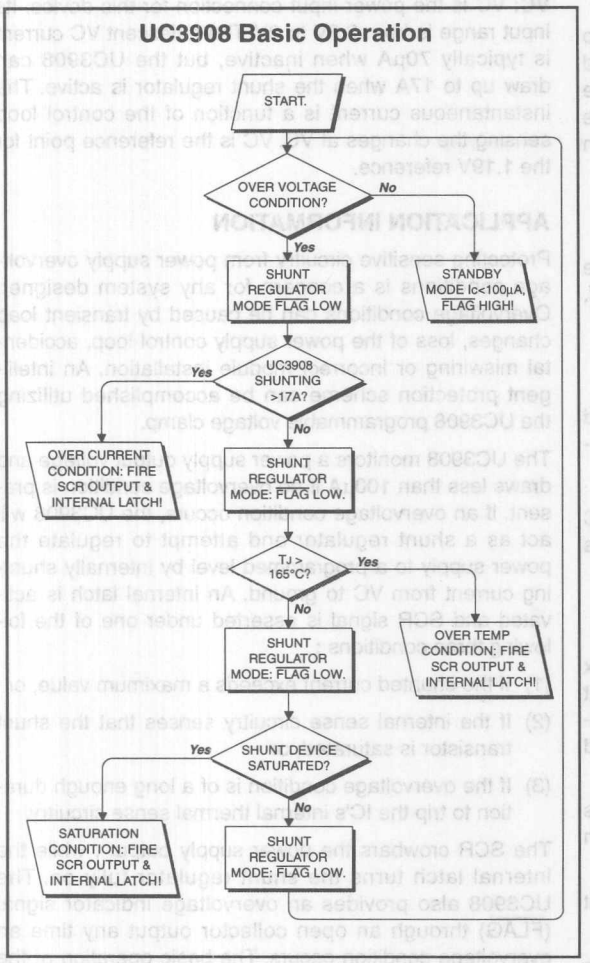
(1) If the shunted current exceeds a maximum value, or

(2) If the internal sense circuitry senses that the shunt transistor is saturated, or

(3) If the overvoltage condition is of a long enough duration to trip the IC's internal thermal sense circuitry.

The SCR crowbars the power supply output , while the internal latch turns the shunt regulator fully on. The UC3908 also provides an overvoltage indicator signal ($\overline{FLAG}$) through an open collector output any time an overvoltage condition occurs. The basic operation of the UC3908 is captured in the accompanying flowchart.

The UC3908 can be applied in an application with or without an external SCR. It is highly recommended that the external SCR be used in most applications excepting some low current applications. Due to its saturation voltage levels and thermal limitations, the UC3908 will not reliably provide overvoltage protection at high current levels. Its main purpose is to provide filtering against transient overvoltage situations which unnecessarily latch SCR crowbars in conventional circuits. The UC3908 allows the power supply to ride through these transients while still maintaining an acceptable level of voltage on the output.



DESIGN CONSIDERATIONS

In a 5V output application, with total tolerance of ±4%, the clamp circuit should not be active below 5.2V. When VC is less than

$$(V_{REF}(min) - 50mV) \bullet \frac{(R1+R2)}{R1},$$

UC3908 is guaranteed to be inactive. With the worst case V_{REF} of 1.14V, (R1+R2)/R1 can be calculated to be 4.775. Selecting R1 to be 10k, R2 is calculated to be 37.75k and selected to be 37.4k. Under worst-case conditions, the regulated voltage will be

$$V_{REF}(max) \bullet \frac{(R1+R2)}{R1}$$

which equals 5.877V in this case.

The lowest voltage that the UC3908 can regulate at is determined by the saturation voltage on the shunt transistor. This voltage is plotted in Figure 9 as a function of shunt current. In order to prevent an overvoltage situation, there is internal circuitry which senses when the shunt transistor reaches saturation and asserts the SCR output. In this case, the presence of an external SCR is an absolute necessity. Note however that at lower current and/or higher voltage levels, the saturation detect circuit is dormant.

Another consideration required in designing a system with the UC3908 is the external SCR drive requirement. The drive signal provided by the UC3908 (on the SCR pin) is approximately 1V below the VC voltage at no load on SCR. In addition, there is an internal series power limiting resistance of approximately 11 ohms which contributes to additional voltage drop when required gate current is being supplied. In order to ensure that the external SCR is fired, a certain minimum gate voltage and minimum drive current must be provided by the drive circuit. The UC3908 is designed to provide 1.5V minimum gate voltage with a gate current of 40mA, which is sufficient to drive a wide range of SCRs. For higher output (VC) voltage levels, external series resistance may be needed to limit the power in the drive circuit. Also, in many applications, it may be necessary to include a bypass resistor from the gate to the cathode of the SCR to prevent false triggering due to noise. This resistor adds to the voltage drop through the UC3908 and must be taken into account when selecting the external SCR.

Figures 1 - 4 illustrate typical behavior of the UC3908 under different operating conditions. In Figure 1, the part is made to shunt less than 17A (6A, in this example) during a short overvoltage situation and thermal shutdown and saturation are also averted. In this case, the part is shown regulating VC at a preset level which is set at 5.59V in the given design example. The FLAG output is low during this mode and SCR output is not activated. Ic is pulsed back down to zero after some duration to indicate that the external pulse has disappeared and the UC3908 becomes inactive again.

In Figure 2, the overvoltage condition of Figure 1 is shown to persist long enough for the internal thermal shutdown to be activated. As a result, the SCR output is asserted and the internal latch is also activated. The voltage (VC) is shown falling to about 2V which is the saturation voltage for the UC3908 at this level of current (6A). With an external SCR, the VC voltage could have been pulled to a much lower level.

In Figure 3, the overvoltage condition results in the UC3908 sinking more than 17A of current in a short time. As a result, the overcurrent comparator activates

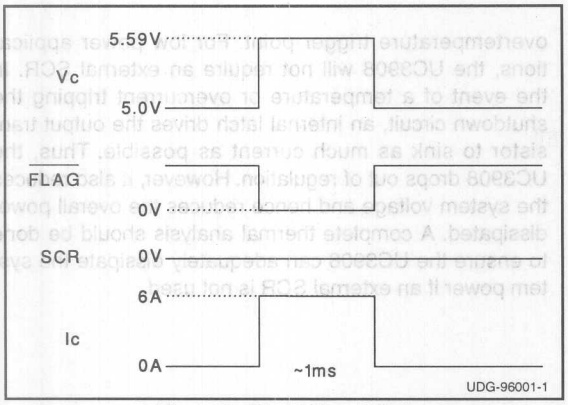


Figure 1. Shunt Regulation

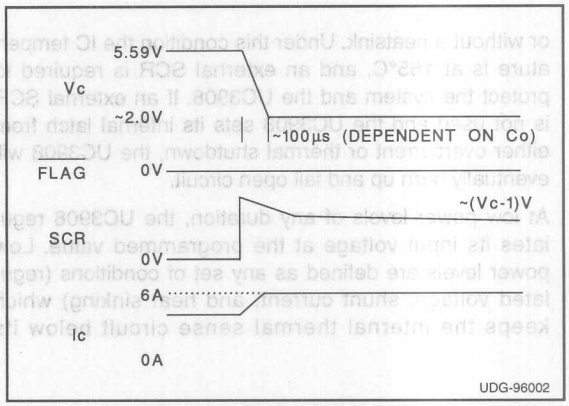


Figure 2. Thermal Shutdown

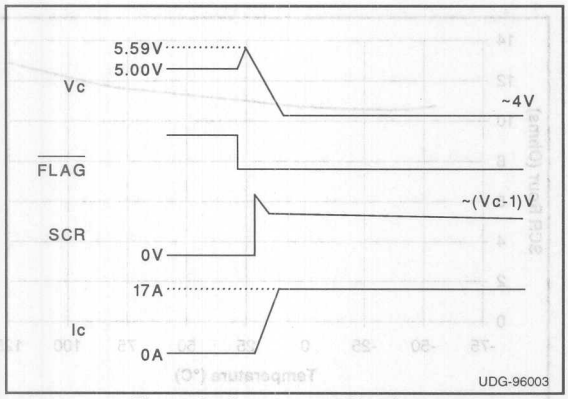


Figure 3. Overcurrent Shutdown

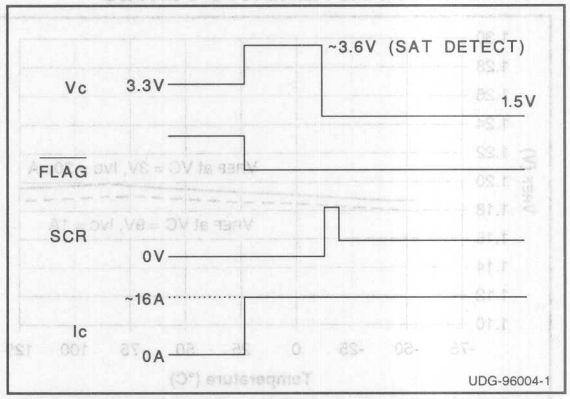


Figure 4. Saturation Detect Feature Resulting in External SCR Firing at Low VC Levels

the SCR output almost immediately after the $\overline{\text{FLAG}}$ is activated. Due to firing of the internal latch, VC drops out of regulation to the saturation level at the given Ic. In this situation, it is very desirable to have an external SCR for thermal reasons. The power dissipation at such a high current is extremely high and even though the UC3908 reduces voltage to reduce dissipation, its saturation voltage is high enough to cause excessive heating.

Finally, Figure 4 illustrates the effect of internal saturation detect circuitry. This circuitry is effective in preventing overvoltage situations at low values of regulated voltage and high current level. By looking at the characteristic curves for VC(sat) at different levels as shown in Figure 9, it can be seen that the saturation voltage of the UC3908 shunt transistor can reach about 3.6V at 16A current levels. The saturation detector senses the saturation level of the shunt transistor and activates the external SCR drive.

THERMAL CONSIDERATIONS

The internal thermal shutdown circuit of the UC3908 is activated at approximately 165°C. The time taken to reach the thermal shutdown is inversely proportional to the power dissipation in the chip.

For short high power pulses or longer periods of moderate power levels, the UC3908 regulates the line at the programmed clamp voltage, shunting excess current to ground. Thus the UC3908 in effect filters voltage transients. For example, a UC3908 in a TO-220 package without any additional heatsinking and starting initially at 25°C takes approximately 1 second at 40 Watts of dissipation before triggering the thermal shutdown circuit. With a clip-on heatsink (e.g. Avid Engineering's clip on cooler for TO-220 packages rated at 5W, #574204B00000), thermal shutdown occurs after 4.7 seconds. At 90 Watts of dissipation thermal shutdown occurs after 160ms, but with a heatsink it takes 210ms. At 100 Watts, the UC3908 shuts down in under 2ms with

or without a heatsink. Under this condition the IC temperature is at 165°C, and an external SCR is required to protect the system and the UC3908. If an external SCR is not used and the UC3908 sets its internal latch from either overcurrent or thermal shutdown, the UC3908 will eventually burn up and fail open circuit.

At low power levels of any duration, the UC3908 regulates its input voltage at the programmed value. Low power levels are defined as any set of conditions (regulated voltage, shunt current, and heat sinking) which keeps the internal thermal sense circuit below its overtemperature trigger point. For low power applications, the UC3908 will not require an external SCR. In the event of a temperature or overcurrent tripping the shutdown circuit, an internal latch drives the output transistor to sink as much current as possible. Thus, the UC3908 drops out of regulation. However, it also reduces the system voltage and hence reduces the overall power dissipated. A complete thermal analysis should be done to ensure the UC3908 can adequately dissipate the system power if an external SCR is not used.

TYPICAL CHARACTERISTICS CURVES

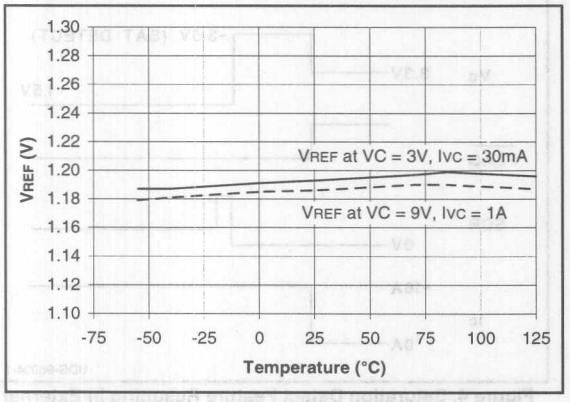


Figure 5. Reference vs. Temperature

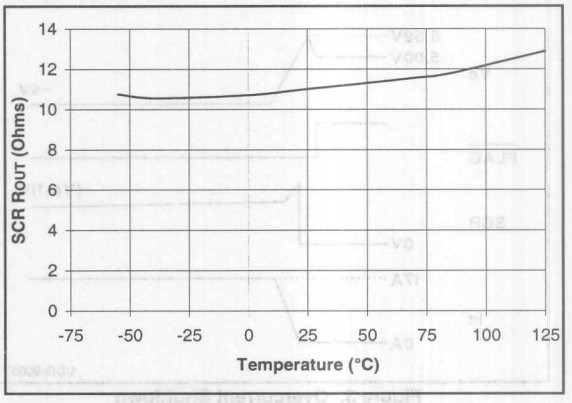


Figure 6. SCR Output Resistance

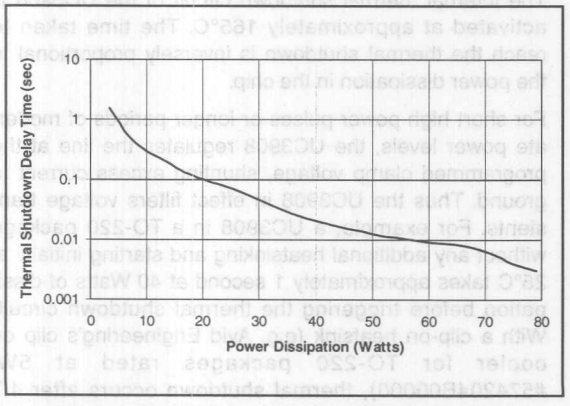


Figure 7. Thermal Shutdown Delay Time vs. Power Dissipation SOIC 8 pin Package (Without any Heatsinking)

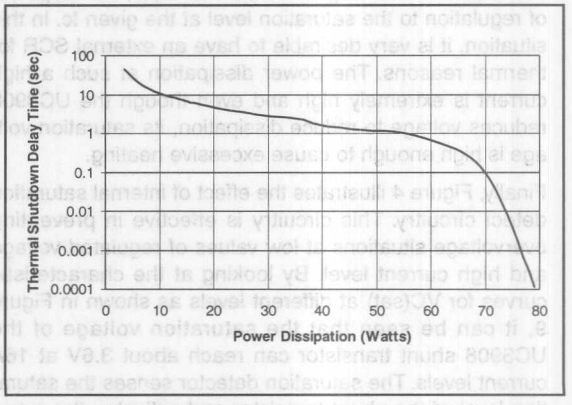


Figure 8. Thermal Shutdown Delay Time vs. Power Dissipation TO-220 Package (Without any Heatsinking)

TYPICAL CHARACTERISTICS CURVES (cont.)

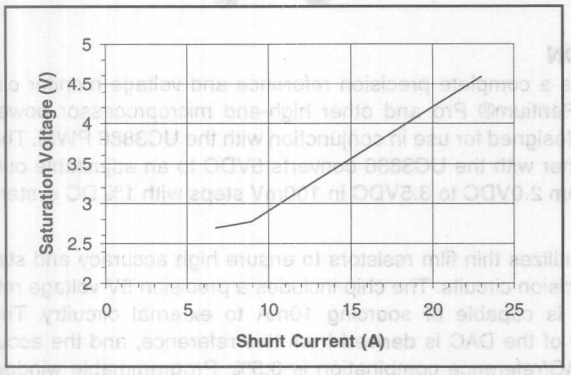


Figure 9. Typical Saturation Characteristics of the Shunt Transistor

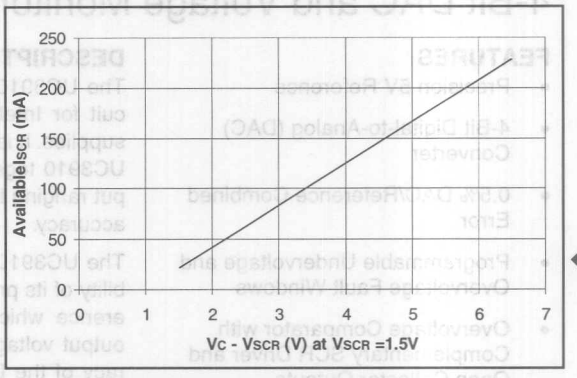


Figure10. SCR Drive Current Characteristics

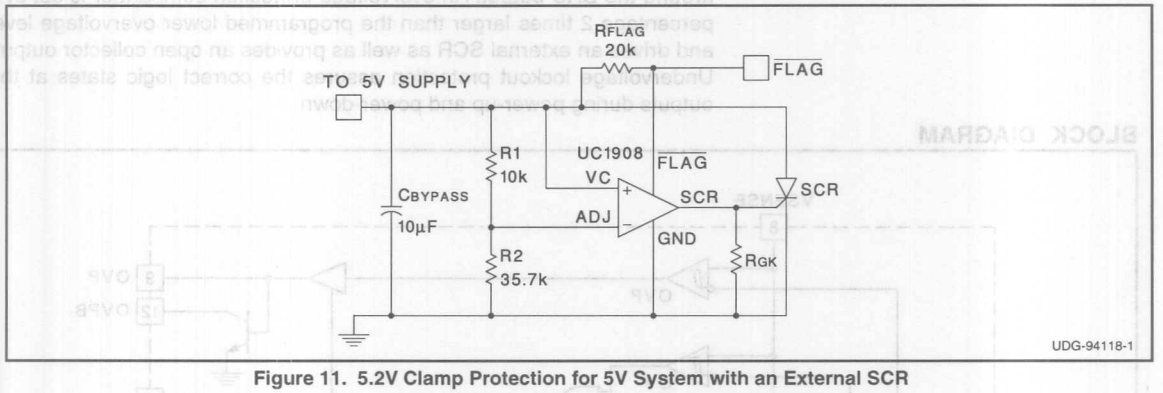


Figure 11. 5.2V Clamp Protection for 5V System with an External SCR

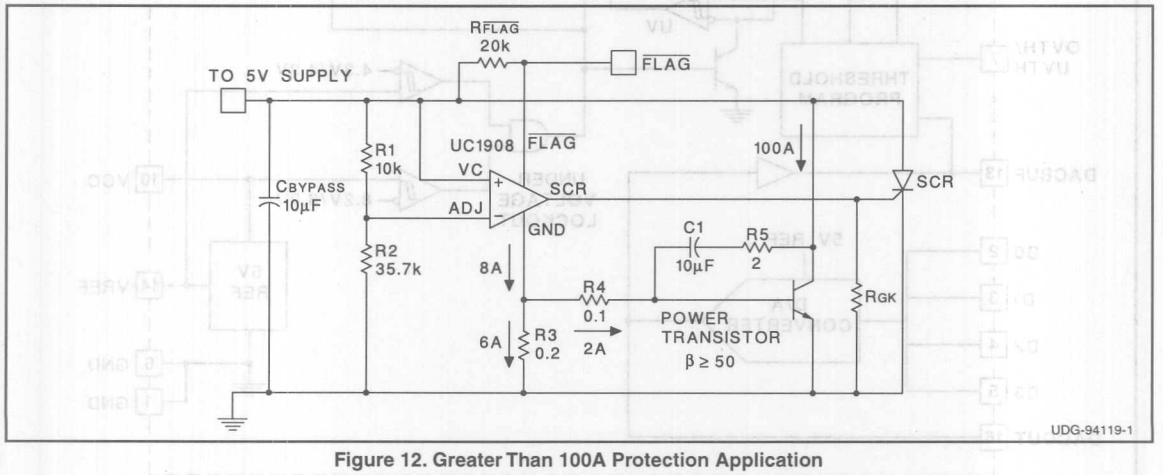


Figure 12. Greater Than 100A Protection Application

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UNITRODE

APPLICATION INFORMATION

UC1910
UC2910
UC3910

4-Bit DAC and Voltage Monitor

FEATURES

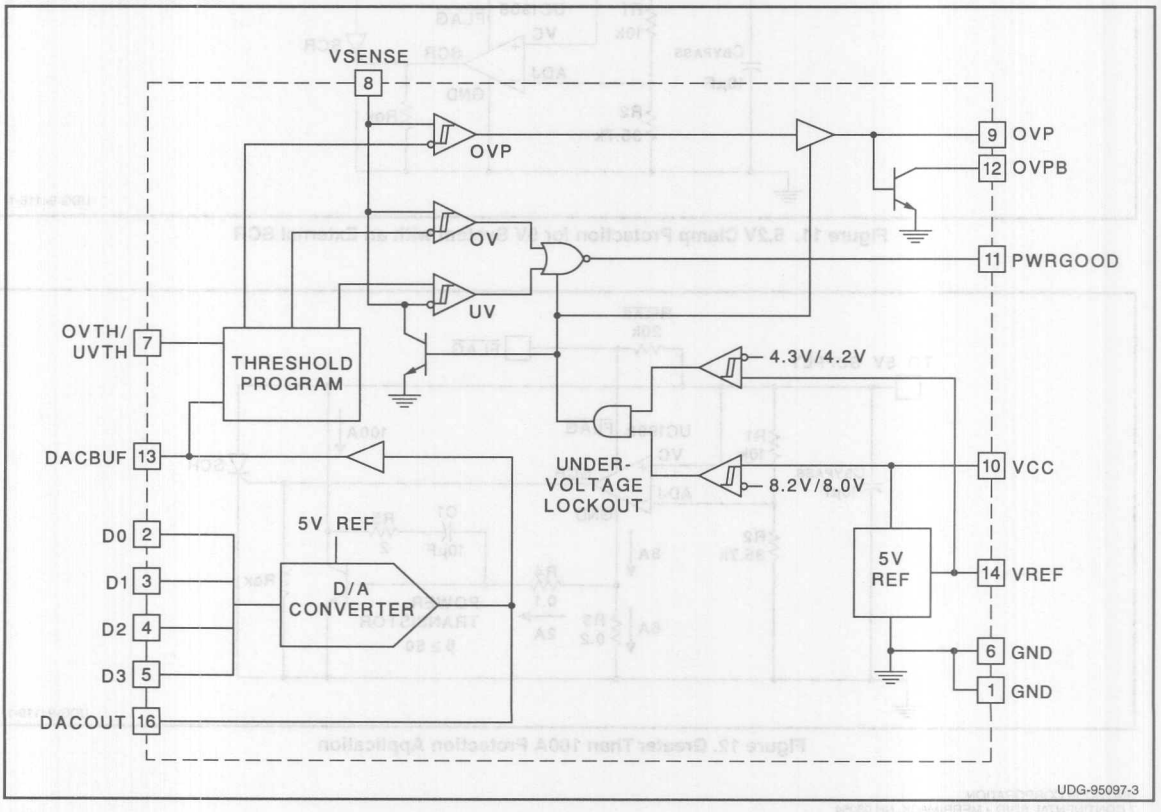
- Precision 5V Reference
- 4-Bit Digital-to-Analog (DAC) Converter
- 0.5% DAC/Reference Combined Error
- Programmable Undervoltage and Overvoltage Fault Windows
- Overvoltage Comparator with Complementary SCR Driver and Open Collector Outputs
- Undervoltage Lockout

DESCRIPTION

The UC3910 is a complete precision reference and voltage monitor circuit for Intel Pentium® Pro and other high-end microprocessor power supplies. It is designed for use in conjunction with the UC3886 PWM. The UC3910 together with the UC3886 converts 5VDC to an adjustable output ranging from 2.0VDC to 3.5VDC in 100mV steps with 1% DC system accuracy.

The UC3910 utilizes thin film resistors to ensure high accuracy and stability of its precision circuits. The chip includes a precision 5V voltage reference which is capable of sourcing 10mA to external circuitry. The output voltage of the DAC is derived from this reference, and the accuracy of the DAC/reference combination is 0.5%. Programmable window comparators monitor the supply voltage to indicate that it is within acceptable limits. The window is programmed as a percentage centered around the DAC output. An overvoltage protection comparator is set at a percentage 2 times larger than the programmed lower overvoltage level and drives an external SCR as well as provides an open collector output. Undervoltage lockout protection assures the correct logic states at the outputs during power-up and power-down.

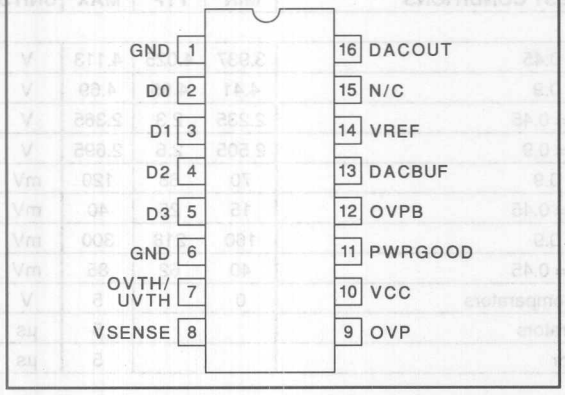
BLOCK DIAGRAM



3/97

CONNECTION DIAGRAM

DIL-16, SOIC-16 (Top View)
J, N, or D Packages



ELECTRICAL CHARACTERISTICS

Unless otherwise specified, VCC = 12V, VSENSE = 3.5V, $V_{OVTH/UVTH}$ = 1.26V, $V_{D0} = V_{D1} = V_{D2} = V_{D3}$ = 0V, 0°C < T_A < 70°C for the UC3910, –25°C < T_A < 80°C for the UC2910, –55°C < T_A < 125°C for the UC1910 $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Undervoltage Lockout					
V_{IN} UVLO Turn-on Threshold		7	8	9	V
UVLO Threshold Hysteresis		50	200	500	mV
Supply Current					
I_{IN} Startup	VCC = 5V		2	3.5	mA
I_{IN}	VCC = 12V		10	12	mA
DAC/Reference					
DACOUT Voltage Accuracy	Line, Load, 0°C < T_A < 70°C (Note 1)	–0.9		0.9	%
	Line, Load, –55°C < T_A < 125°C	–1.5		1.5	%
D0-D3 Voltage High	Dx Pin Floating	4.6	4.85		V
D0-D3 Input Bias Current	Dx Pin Tied to GND	–140	–105		µA
VREF Output Voltage	I_{VREF} = 0mA, 0°C < T_A < 70°C	4.97	5	5.03	V
VREF Total Variation	Line, Load, 0°C < T_A < 70°C (Note 1)	4.96	5	5.04	V
	Line, Load, –55°C < T_A < 125°C	4.925	5	5.075	V
VREF Sourcing Current	VREF = 0V	10			mA
DAC Buffer					
Input Offset Voltage	I_{DACBUF} = –1mA, 0°C < T_A < 70°C	–25		25	mV
Output Sourcing Current		–12		–1	mA
Monitor Circuitry (Note 2)					
VSENSE UV Threshold Voltage	Code 0, Ratio = 0.45 (Note 3)	3.174	3.237	3.3	V
	Code 0, Ratio = 0.9	2.87	2.975	3.08	V
	Code 15, Ratio = 0.45	1.816	1.85	1.884	V
	Code 15, Ratio = 0.9	1.635	1.7	1.765	V
VSENSE OV Threshold Voltage	Code 0, Ratio = 0.45	3.7	3.763	3.826	V
	Code 0, Ratio = 0.9	3.92	4.025	4.13	V
	Code 15, Ratio = 0.45	2.116	2.15	2.184	V
	Code 15, Ratio = 0.9	1.635	2.3	2.365	V

ELECTRICAL CHARACTERISTICS (cont.) Unless otherwise specified, VCC = 12V, VSENSE = 3.5V, $V_{OVTH/UVTH}$ = 1.26V, $V_{D0} = V_{D1} = V_{D2} = V_{D3}$ = 0V, 0°C < T_A < 70°C for the UC3910, –25°C < T_A < 80°C for the UC2910, –55°C < T_A < 125°C for the UC1910 $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Monitor Circuitry (Note 2) (cont.)					
VSENSE OVP Threshold Voltage	Code 0, Ratio = 0.45	3.937	4.025	4.113	V
	Code 0, Ratio = 0.9	4.41	4.55	4.69	V
	Code 15, Ratio = 0.45	2.235	2.3	2.365	V
	Code 15, Ratio = 0.9	2.505	2.6	2.695	V
OV, UV Comparator Hysteresis	Code 0, Ratio = 0.9	70	88	120	mV
	Code 15, Ratio = 0.45	15	25	40	mV
OVP Comparator Hysteresis	Code 0, Ratio = 0.9	160	218	300	mV
	Code 15, Ratio = 0.45	40	62	85	mV
Input Common Mode Range	OV, UV, OVP Comparators	0		5	V
Propagation Delay	OV, UV Comparators			5	µs
	OVP Comparator			5	µs
PWRGOOD, OVP, OVPB Outputs					
PWRGOOD Voltage Low	$I_{PWRGOOD}$ = 10mA			0.4	V
OVP Sourcing Current	V_{OVP} = 1.4V	65			mA
OVPB Voltage Low	I_{OVPB} = 1mA			0.4	V

Note 1: "Line, Load" implies that the parameter is tested at all combinations of the conditions: 10.8V < VCC < 13.2V, –2mA < I_{VREF} < 0mA.

Note 2: These are the actual voltages on VSENSE which will cause the OVPB and PWRGOOD outputs to switch, assuming the DACOUT voltage is perfect. These limits apply for 0°C < T_A < 70°C.

Note 3: "Code 0" means pins D0 - D4 are all low; "Code 15" means they are all floating or high (See Table 1). "Ratio" is the divider ratio of the resistor string between DACBUF and OVTH/UVTH (See Figure 1).

PIN DESCRIPTIONS

D0-D3 (DAC Digital Input Control Codes): These are the DAC digital input control codes, with D0 representing the least significant bit (LSB) and D3, the most significant bit (MSB) (See Table 1). A bit is set low by being connected to GND; a bit is set high by floating it, or connecting it to a 3V to 5V voltage source. Each control pin is pulled up to approximately 4.8V by an internal 40µA current source.

DACBUF (Buffered DACOUT Voltage): This pin provides a buffered version of the DACOUT voltage to allow external programming of the OV/UV thresholds (see OVTH/UVTH below).

DACOUT (Digital-to-Analog Converter Output Voltage): This pin is the output of the 4-bit digital to analog (DAC) converter. Setting all input control codes low produces 3.5V at DACOUT; setting all codes high produces 2.0V at DACOUT. The LSB step size (i.e. resolution) is 100mV (See Table 1). The DACOUT source impedance is typically 3kΩ and must therefore drive a high impedance input. Bypass DACOUT at the driven input with a 0.01µF, low ESR, low ESL capacitor for best circuit noise immunity.

GND (Signal Ground): All voltages are measured with respect to GND. The two GND pins are connected together internally but should also be connected externally using a short PC board trace. Bypass capacitors on the VCC and VREF pins should be connected directly to the ground plane near one of the signal ground

Decimal Code	D3	D2	D1	D0	DACOUT Voltage
15	1	1	1	1	2.0
14	1	1	1	0	2.1
13	1	1	0	1	2.2
12	1	1	0	0	2.3
11	1	0	1	1	2.4
10	1	0	1	0	2.5
9	1	0	0	1	2.6
8	1	0	0	0	2.7
7	0	1	1	1	2.8
6	0	1	1	0	2.9
5	0	1	0	1	3.0
4	0	1	0	0	3.1
3	0	0	1	1	3.2
2	0	0	1	0	3.3
1	0	0	0	1	3.4
0	0	0	0	0	3.5

Table 1. Programming the DACOUT Voltage

PIN DESCRIPTIONS (cont.)

pins.

OVP (Overvoltage Comparator Output): This output pin drives an external SCR circuit with up to 65mA when the voltage on VSENSE rises above its nominal value by a percentage set by the voltage on the OVTH/UVTH pin (see below). The OVP comparator hysteresis is a function of both the DACBUF voltage and the OV/UV percentage programmed.

OVPB (Overvoltage Comparator Complementary Output): This output is a complement to the OVP output (see above) and provides an open collector capable of sinking 1mA when the voltage on VSENSE rises above its nominal value by a percentage set by the voltage on the OVTH/UVTH pin (see below).

OVTH/UVTH (Undervoltage and Lower Overvoltage Threshold Input): This pin is used to program the window thresholds for the OV and UV comparators. The OV-UV window is centered around the DACBUF voltage and can be programmed from ±5% to ±15% about DACBUF. Connect a resistor divider between DACBUF and GND to set the percentage. The threshold for the OVP comparator is internally set to a percentage 2 times larger than the programmed OV percentage; therefore, its range extends from 10% to 30% above DACBUF.

PWRGOOD (Undervoltage/Lower Overvoltage Output): This pin is an open collector output which is driven low to reset the microprocessor when VSENSE rises above or falls below its nominal value by a percentage programmed by OVTH/UVTH. The OV and UV comparators' hysteresis is a function of the DACBUF voltage and the OV/UV programmed percentage.

VCC (Positive Supply Voltage): This pin supplies power to the chip. Connect VCC to a stable voltage source of at least 9V and capable of sourcing at least 15mA. The OVP and PWRGOOD outputs are held low, the OVPB output is in a high impedance state, and the VSENSE pin is pulled low until VCC exceeds the upper undervoltage lockout threshold. This pin should be bypassed directly to the GND pin with a 0.1µF low ESR, low ESL capacitor.

VREF (Voltage Reference Output): This pin provides an accurate 5V reference, capable of delivering up to 10mA to external circuitry, and is internally short circuit current limited. For best reference stability, bypass VREF directly to the GND pin with a 0.1µF, low ESR, low ESL capacitor.

VSENSE (Output Voltage Sensing Input): This pin is the input to the OVP and PWRGOOD comparators and is connected to the system output voltage through a lowpass filter. When choosing the resistor value for this filter, make sure that no more than 500µA will flow

APPLICATION INFORMATION

The Overvoltage (OV), Undervoltage (UV) and Overvoltage Protection Voltage (OVP) threshold detection voltages are programmed as a percentage about the nominal DAC output voltage, DACOUT. Figure 1 illustrates how to program the UC3910 by setting a voltage divider, RDIV, at the OVTH/UVTH pin. The voltage divider ratio is defined as

$$R_{DIV} = \frac{RS1}{RS1 + RS2}$$

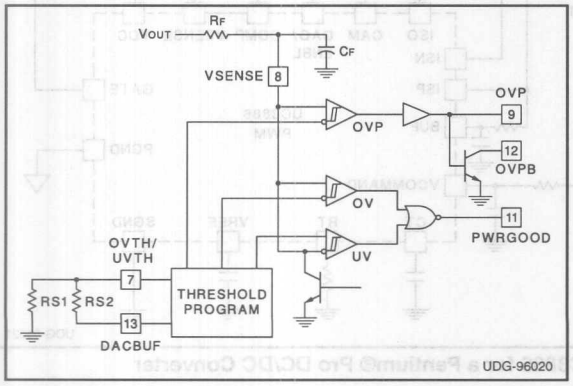


Figure 1. Setting the OV/UV/OVP Threshold Percentages

The UC3910 allows a ratio RDIV at the OVTH/UVTH pin from 0.3 to 0.9, which corresponds to overvoltage and undervoltage percentage thresholds from 5% to 15% and an OVP percentage threshold from 10% to 30%. These thresholds are shown in Figure 2.

The OV, UV and OVP percentage thresholds are given by

$$\%V_{OV} = R_{DIV} \bullet 16.7$$
$$\%V_{UV} = -(R_{DIV} \bullet 16.7)$$
$$\%V_{OVP} = \%V_{OV} \bullet 2.0 = R_{DIV} \bullet 33.4$$

An R-C filter is added to the VSENSE pin to filter noise and ripple at the comparator inputs. An R-C filter frequency of FSWITCH/10 is recommended. Choose the

APPLICATION INFORMATION (cont.)

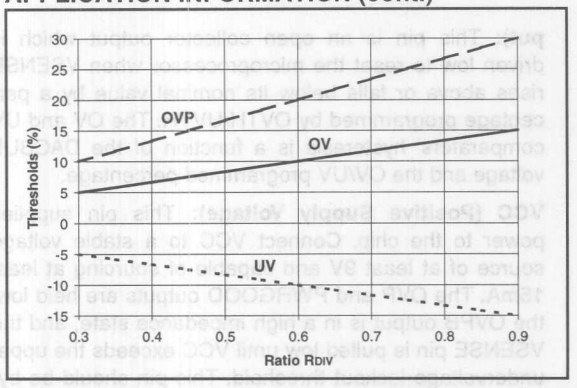


Figure 2. OV, UV and OVP Percentage Thresholds as a Function of the Divider Ratio RDIV

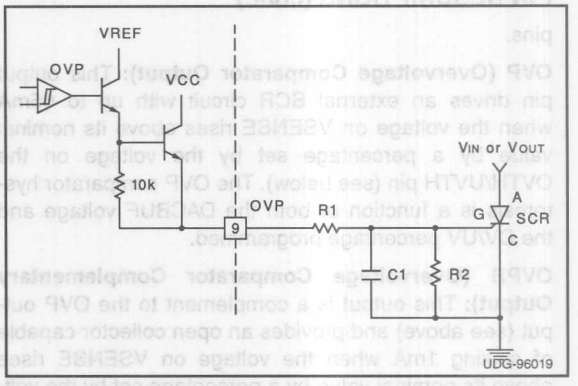


Figure 3. Driving and SCR Using the UC3910 OVP Signal

value of RF such that it limits the current into VSENSE to ≤ 0.5mA.

$$R_F \bullet C_F = \frac{1}{2 \bullet \pi \bullet \left(\frac{F_{SWITCH}}{10}\right)}$$

$$R_F \geq \frac{V_{OUT}}{0.5mA}$$

The Overvoltage Protection output, OVP, can be used to directly drive a crowbarring SCR, as shown in Figure 3.

A typical application is shown in Figure 4 using the UC3910 together with the UC3886 Average Current Mode PWM Controller IC for a power supply to drive Intel's Pentium®Pro processor.

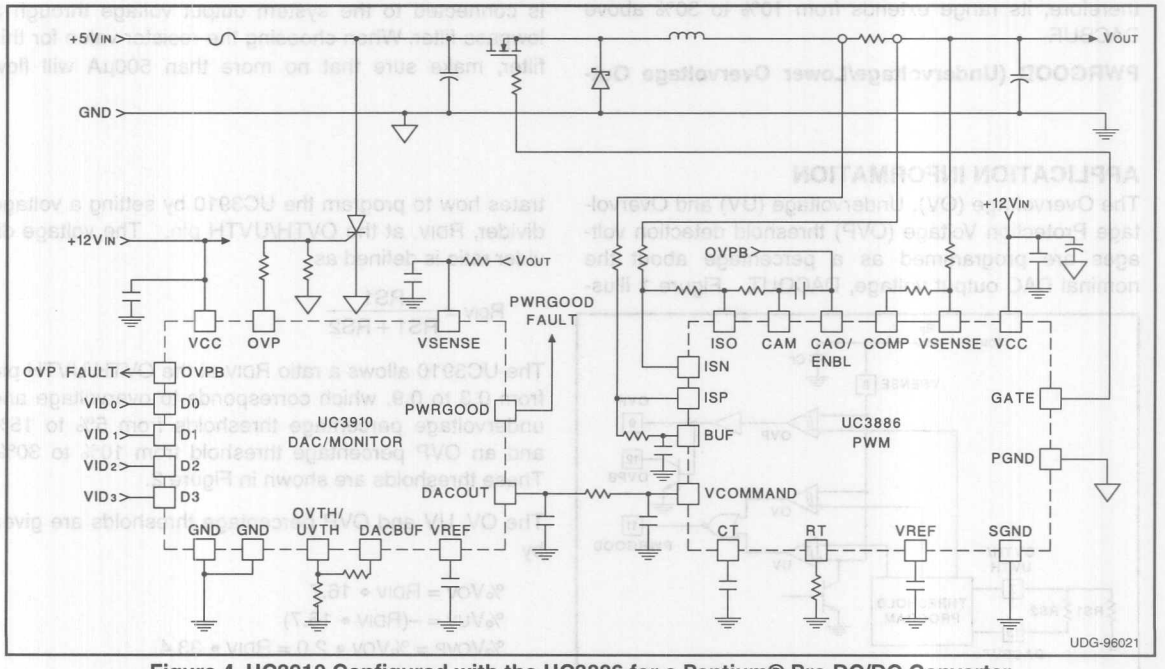


Figure 4. UC3910 Configured with the UC3886 for a Pentium® Pro DC/DC Converter

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Precision Adjustable Shunt Regulator

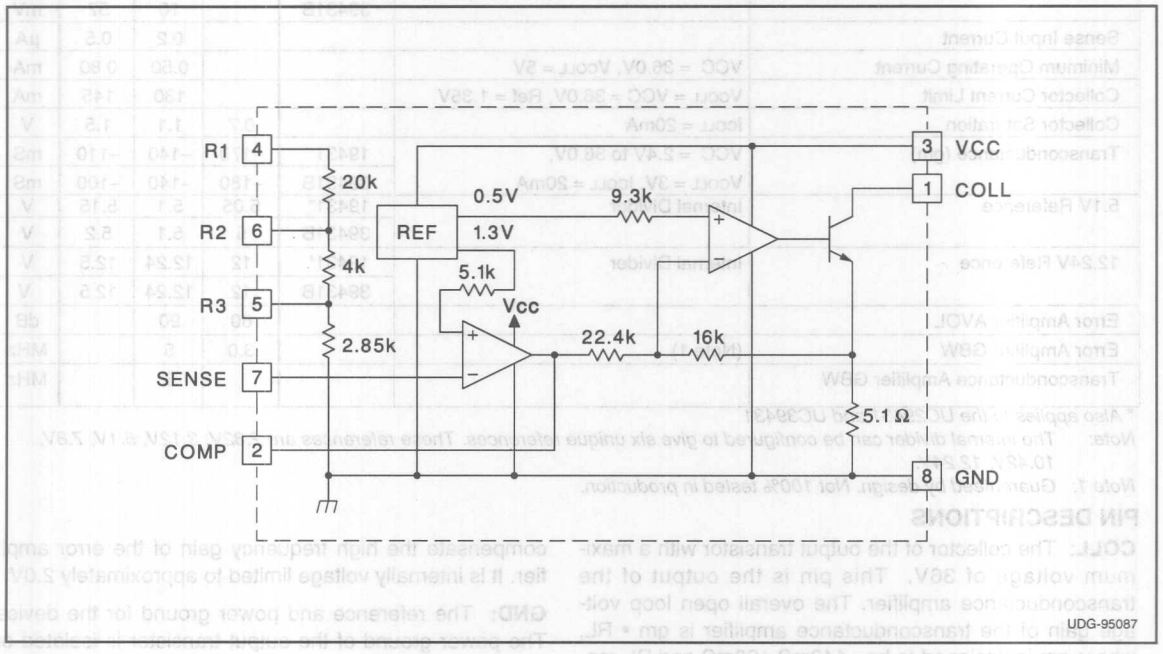
FEATURES

- Multiple On-Chip Programmable Reference Voltages
- 0.4% Initial Accuracy
- 0.7% Overall Reference Tolerance
- 2.2V to 36.0V Operating Supply Voltage and User Programmable Reference
- 36.0V Operating Supply Voltage
- Reference Accuracy Maintained For Entire Range of Supply Voltage
- Superior Accuracy and Easier Compensation for Optoisolator Application
- Improved Architecture Provides a Known Linear Transconductance with a +5% Typical Tolerance

DESCRIPTION

The UC39431 is an adjustable shunt voltage regulator with 100mA sink capability. The architecture, comprised of an error amplifier and transconductance amplifier, gives the user separate control of the small signal error voltage frequency response along with a fixed linear transconductance. A minimum 3MHz gain bandwidth product for both the error and transconductance amplifiers assures fast response. In addition to external programming, the IC has three internal resistors that can be connected in six different configurations to provide regulated voltages of 2.82V, 3.12V, 5.1V, 7.8V, 10.42V, and 12.24V. A sister device (UC39432) provides access to the non-inverting error ampilifer input and reference, while eliminating the three internal resistors.

BLOCK DIAGRAM



UDG-95087

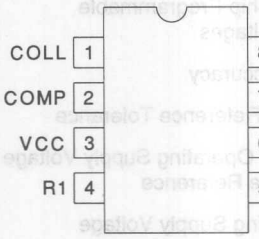
ABSOLUTE MAXIMUM RATINGS

Supply Voltage: V 36V
Regulated Output: V 36V
Internal Resistors: R1, R2, R3 ..... 13V
E/A Input: SENSE 6V
E/A Compensation: COMP 6V
Output Sink Current: I 140mA
Power Dissipation at $T_A \leq 25°C$ (DIL-8) 1W
Derate 8mW/°C for $T_A > 25°C$
Storage Temperature Range ..... –65°C to +150°C
Junction Temperature ..... –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

Currents are positive into negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAMS

DIL-8, SOIC-8 (Top View)
N or J, D Package



ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply for T_A = –55°C to +125°C and COLL Output = 2.4V to 36.0V for the UC19431, T_A = –25°C to +85°C and COLL Output = 2.3V to 36.0V for the UC29431, and T_A = 0°C to +70°C and COLL Output = 2.3V to 36.0V for the UC39431/B, VCC = 15V, I_{COLL} = 10mA, $T_A = T_J$.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Reference Voltage Tolerance	T_A = 25°C	19431*	1.295	1.3	1.305	V
		39431B	1.29	1.3	1.31	V
Reference Temperature Tolerance	V_{COLL} = 5.0	19431*	1.291	1.3	1.309	V
		39431B	1.286	1.3	1.314	V
Reference Line Regulation	VCC = 2.2V to 36.0V, V_{COLL} = 5V	19431*		10	38	mV
		39431B		10	57	mV
Reference Load Regulation	I_{COLL} = 10mA to 50mA, V_{COLL} = 5V	19431*		10	38	mV
		39431B		10	57	mV
Sense Input Current				0.2	0.5	µA
Minimum Operating Current	VCC = 36.0V, V_{COLL} = 5V			0.50	0.80	mA
Collector Current Limit	V_{COLL} = VCC = 36.0V, Ref = 1.35V			130	145	mA
Collector Saturation	I_{COLL} = 20mA		0.7	1.1	1.5	V
Transconductance (gm)	VCC = 2.4V to 36.0V,	19431*	–170	–140	–110	mS
	V_{COLL} = 3V, I_{COLL} = 20mA	39431B	–180	–140	–100	mS
5.1V Reference	Internal Divider	19431*	5.05	5.1	5.15	V
		39431B	5	5.1	5.2	V
12.24V Reference	Internal Divider	19431*	12	12.24	12.5	V
		39431B	12	12.24	12.5	V
Error Amplifier AVOL			60	90		dB
Error Amplifier GBW	(Note 1)		3.0	5		MHz
Transconductance Amplifier GBW				3		MHz

** Also applies to the UC29431 and UC39431*

Note: The internal divider can be configured to give six unique references. These references are 2.82V, 3.12V, 5.1V, 7.8V, 10.42V, 12.24V.

Note 1: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

COLL: The collector of the output transistor with a maximum voltage of 36V. This pin is the output of the transconductance amplifier. The overall open loop voltage gain of the transconductance amplifier is gm • RL, where gm is designed to be –140mS ±30mS and RL represents the output load.

COMP: The output of the error amplifier and the input to the transconductance amplifier. This pin is available to compensate the high frequency gain of the error amplifier. It is internally voltage limited to approximately 2.0V.

GND: The reference and power ground for the device. The power ground of the output transistor is isolated on the chip from the substrate ground used to bias the remainder of the device.

R1, R2, R3: Connection points to the three internal resistors.

PIN DESCRIPTIONS (cont.)

SENSE: The inverting terminal of the error amplifier used as both the voltage sense input to the error amplifier and its other compensation point. The error amplifier uses the SENSE input to compare against the 1.3V on-chip reference.

The SENSE pin is also used as the undervoltage lockout (UVLO). It is intended to keep the chip from operating until the internal reference is properly biased. The threshold is approximately 1V. It is important that once the UVLO is released, the error amplifier can drive the transconductance amplifier to stabilize the loop. If a capacitor is connected between the SENSE and COMP pins to create a pole, it will limit the slew rate of the error amplifier. To increase the bandwidth and ensure startup at low load current, it is recommended to create a zero along with the pole as shown in the shunt regulator application. The error amplifier must slew 2.0V to drive the transconductance amplifier initially on.

VCC: The power connection for the device. The minimum to maximum operating voltage is 2.2V to 36.0V. The quiescent current is typically 0.50mA.

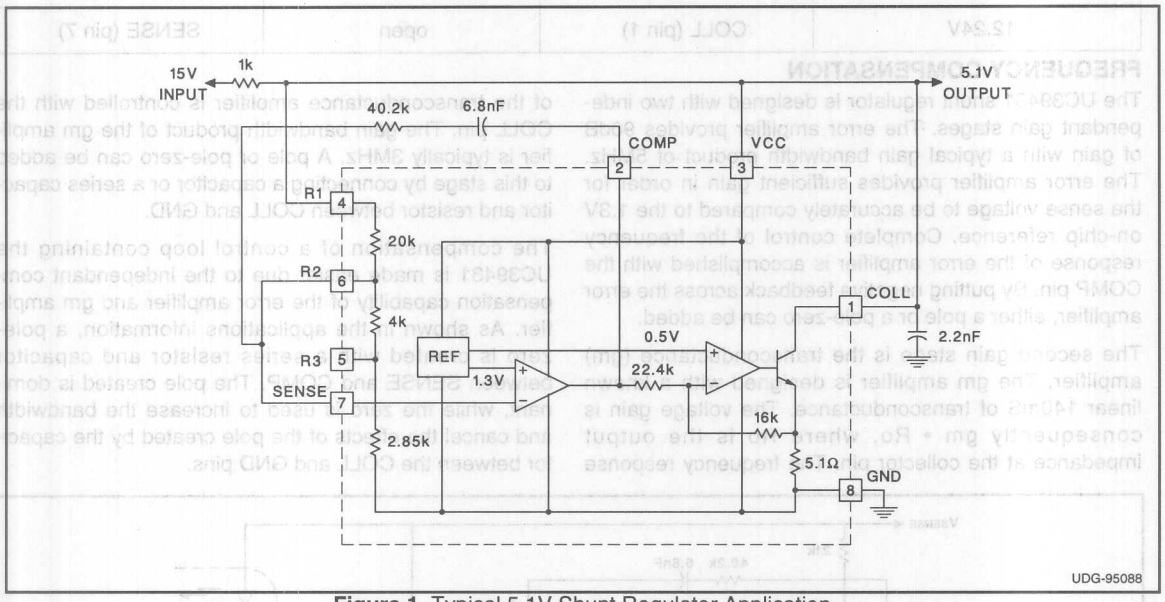


Figure 1. Typical 5.1V Shunt Regulator Application

MAGNETIC AMPLIFIER CONTROLLER APPLICATION

The 0.4% initial reference makes the UC39431 ideal as a programmable shunt regulator. By adding two external resistors, the on-chip 1.3V reference can be gained to any voltage between 2.2V (2.4V for the UC39431) and 36.0V. The input bias current is typically maintained at 0.2µA for the output voltage range. Since the non-inverting error amplifier input is not available, a 5.1k non-inverting input impedance is added to the input of the error amplifier. This allows the user to choose the SENSE pin input impedance to cancel the minimal offset voltage caused by the input bias current.

RESISTOR DIVIDER CONNECTION TABLE FOR SHUNT AND OPTO APPLICATIONS

To obtain the shunt regulated or optocoupler sensed voltage specified in the left column, connect the internal resistors (R1, R2, R3) as indicated.

REGULATED VOLTAGE	CONNECT R1 TO:	CONNECT R2 TO:	CONNECT R3 TO:
2.82V	SENSE (pin 7)	COLL (pin 1)	SENSE (pin 7)
3.12V	open	COLL (pin 1)	SENSE (pin 7)
5.1V	COLL (pin 1)	SENSE (pin 7)	open
7.8V	COLL (pin 1)	SENSE (pin 7)	GND (pin 8)
10.42V	COLL (pin 1)	SENSE (pin 7)	SENSE (pin 7)
12.24V	COLL (pin 1)	open	SENSE (pin 7)

FREQUENCY COMPENSATION

The UC39431 shunt regulator is designed with two independant gain stages. The error amplifier provides 90dB of gain with a typical gain bandwidth product of 5MHz. The error amplifier provides sufficient gain in order for the sense voltage to be accurately compared to the 1.3V on-chip reference. Complete control of the frequency response of the error amplifier is accomplished with the COMP pin. By putting negative feedback across the error amplifier, either a pole or a pole-zero can be added.

The second gain stage is the transconductance (gm) amplifier. The gm amplifier is designed with a known linear 140mS of transconductance. The voltage gain is consequently gm • Ro, where Ro is the output impedance at the collector pin. The frequency response of the transconductance amplifier is controlled with the COLL pin. The gain bandwidth product of the gm amplifier is typically 3MHz. A pole or pole-zero can be added to this stage by connecting a capacitor or a series capacitor and resistor between COLL and GND.

The compensation of a control loop containing the UC39431 is made easier due to the independant compensation capability of the error amplifier and gm amplifier. As shown in the applications information, a pole-zero is created with a series resistor and capacitor between SENSE and COMP. The pole created is dominant, while the zero is used to increase the bandwidth and cancel the effects of the pole created by the capacitor between the COLL and GND pins.

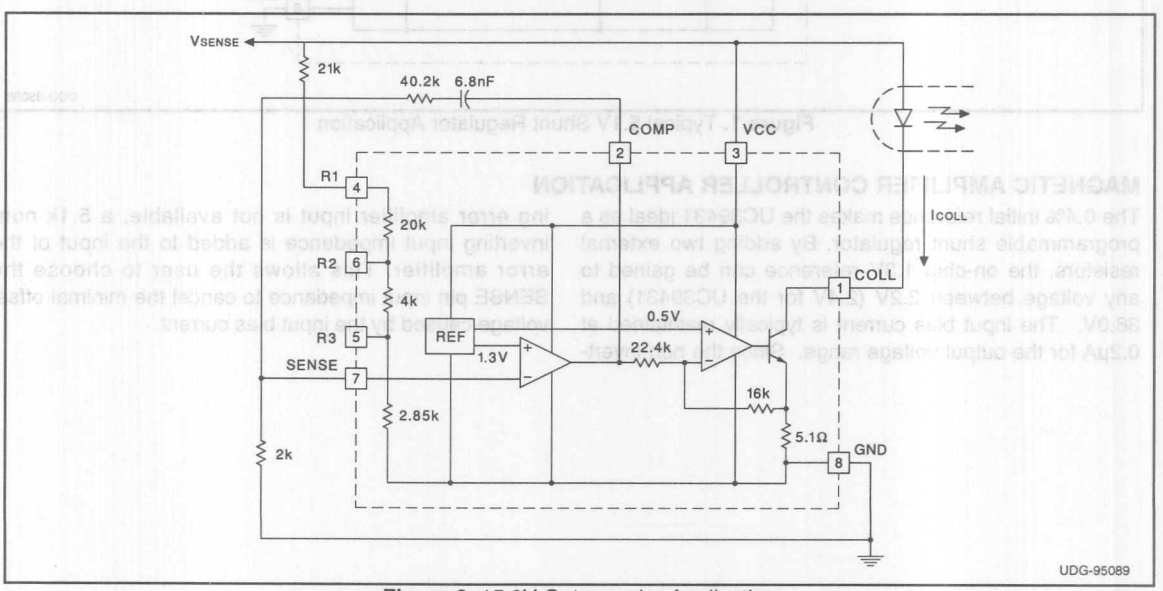


Figure 2. 15.0V Optocoupler Application

OPTOCOUPLER APPLICATION

The two amplifier circuit architecture employed in the UC39431 is most advantageous for the optocoupler application. The error amplifier provides a fixed open loop gain that is available to apply flexible loop compensation of either poles or zeroes. A fixed transconductance amplifier provides a linear current source compared to the typical transistor's exponential output characteristics. It also eliminates the traditional optocoupler's CTR variations with power supply and voltage, and the need to suffer the additional voltage drop of a series resistor.

MAGNETIC AMPLIFIER CONTROLLER APPLICATION

The UC39431 makes an excellent controller for magnetic amplifier regulated outputs. Working from either a square wave drive or from a PWM signal controlled by another output, a saturable reactor provides highly efficient control, requiring only a reset current which can be generated from its own output.

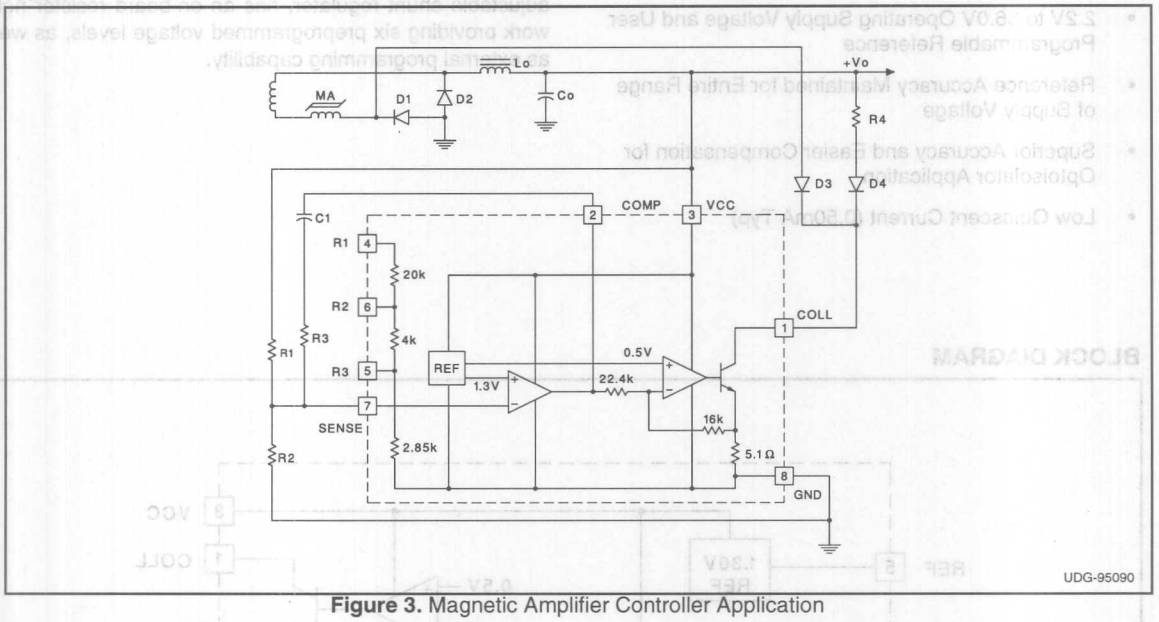


Figure 3. Magnetic Amplifier Controller Application

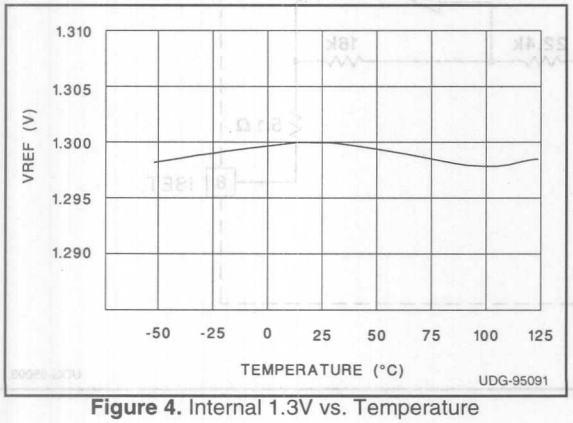


Figure 4. Internal 1.3V vs. Temperature

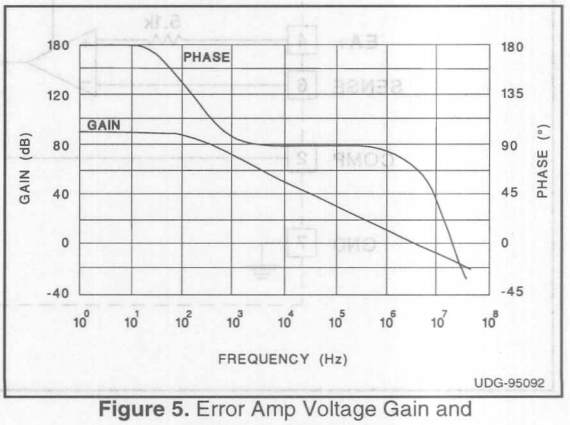


Figure 5. Error Amp Voltage Gain and Phase vs. Frequency

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UNITRODE

Precision Analog Controller

UC19432
UC29432
UC39432
UC39432B

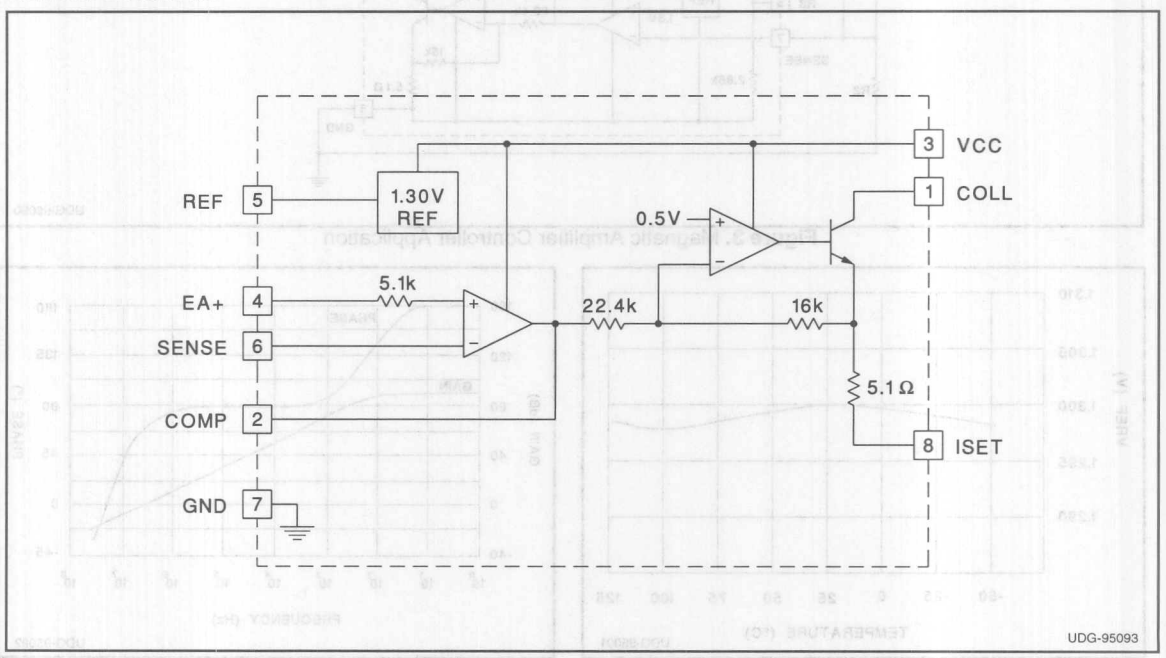
FEATURES

- Programmable Transconductance for Optimum Current Drive
- Accessible 1.3V Precision Reference
- Both Error Amplifier Inputs Available
- 0.7% Overall Reference Tolerance
- 0.4% Initial Accuracy
- 2.2V to 36.0V Operating Supply Voltage and User Programmable Reference
- Reference Accuracy Maintained for Entire Range of Supply Voltage
- Superior Accuracy and Easier Compensation for Optoisolator Application
- Low Quiescent Current (0.50mA Typ)

DESCRIPTION

The UC39432 is an adjustable precision analog controller with 100mA sink capability if the ISET pin is grounded. A resistor between ISET and ground will modify the transconductance while decreasing the maximum current sink. This will add further control in the optocoupler configuration. The trimmed precision reference along with the non-inverting error amplifier inputs are accessible for custom configuration. A sister device, the UC39431 adjustable shunt regulator, has an on-board resistor network providing six preprogrammed voltage levels, as well as external programming capability.

BLOCK DIAGRAM



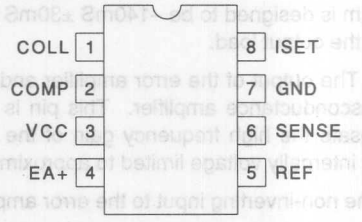
ABSOLUTE MAXIMUM RATINGS

Supply Voltage: VCC 36V
Regulated Output: VCOLL 36V
EA Input: SENSE, EA+ 6V
EA Compensation: COMP 6V
Reference Output: REF 6V
Output Sink Current: ICOLL 140mA
Output Source Current: ISET . . . . . .–140mA
Power Dissipation at TA ≤ 25°C (DIL-8) 1W
Derate 8mW/°C for TA > 25°C
Storage Temperature Range . . . . . .–65°C to +150°C
Junction Temperature . . . . . .–55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . .+300°C

Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAMS

DIL-8, SOIC-8 (Top View)
N or J, D Package



ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply for TA = –55°C to +125°C and COLL Output = 2.4V to 36.0V for the UC19432, TA = –25°C to +85°C and COLL Output = 2.3V to 36.0V for the UC29432, and TA = 0°C to +70°C and COLL Output = 2.3V to 36.0V for the UC39432, VCC = 15V, ICOLL = 10mA, TA = TJ.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Reference Voltage Tolerance	TA = 25°C	19432*	1.295	1.3	1.305	V
		39432B	1.29	1.3	1.31	V
Reference Temperature Tolerance	VCOLL = 5.0V	19432*	1.291	1.3	1.309	V
		39432B	1.286	1.3	1.314	V
Reference Line Regulation	VCC = 2.4V to 36.0V, VCOLL = 5V	19432*		10	38	mV
		39432B		10	57	mV
Reference Load Regulation	ICOLL = 10mA to 50mA, VCOLL= 5V	19432*		10	38	mV
		39432B		10	57	mV
Reference Sink Current					10	µA
Reference Source Current					–10	µA
EA Input Bias Current				0.2	0.5	µA
EA Input Offset Voltage		19432*			4.0	mV
		39432B			4.0	mV
EA Output Current Sink (Internally Limited)					16	µA
EA Output Current Source					–1	mA
Minimum Operating Current	VCC = 36.0V, VCOLL = 5V			0.50	0.80	mA
Collector Current Limit (Note)	VCOLL = VCC = 36.0V, Ref = 1.35V ISET = GND			130	145	mA
Collector Saturation	ICOLL = 20mA		0.7	1.1	1.5	V
Transconductance (gm) (Note)	VCC = 2.4V to 36.0V,	19432*	–170	–140	–110	mS
	VCOL = 3V, ICOLL = 20mA	39432B	–180	–140	–100	mS
	ISET = GND					
Error Amplifier AVOL			60	90		dB
Error Amplifier GBW	(Note 1)		3.0	5		MHz
Transconductance Amplifier GBW				3		MHz

** Also applies to the UC29432 and UC39432*
Note: Programmed transconductance and collector current limit equations are specified in the ISET pin description.
Note1: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

COLL: The collector of the output transistor with a maximum voltage of 36V. This pin is the output of the transconductance amplifier. The overall open loop voltage gain of the transconductance amplifier is gm • RL, where gm is designed to be –140mS ±30mS and RL represents the output load.

COMP: The output of the error amplifier and the input to the transconductance amplifier. This pin is available to compensate the high frequency gain of the error amplifier. It is internally voltage limited to approximately 2.0V.

EA+: The non-inverting input to the error amplifier.

GND: The reference and power ground for the device. The power ground of the output transistor is isolated on the chip from the substrate ground used to bias the remainder of the device.

ISET: The current set pin for the transconductance amplifier. The transconductance will be –140mS as specified in the electrical table if this pin is grounded. If a resistance RL is added to the ISET pin, the resulting new transconductance is calculated using the following equation: gm = –0.714V • (5.1Ω + RL). The maximum current will be approximately

$$I_{MAX} = \frac{0.6V}{5.1\Omega + R_L}$$

REF: The output of the trimmed precision reference. It can source or sink 10μA and still maintain the 1% temperature specification.

SENSE: The inverting terminal of the error amplifier used as both the voltage sense input to the error amplifier and its other compensation point. The error amplifier uses the SENSE input to compare against the 1.3V on-chip reference.

The SENSE pin is also used as the undervoltage lockout (UVLO). It is intended to keep the chip from operating until the internal reference is properly biased. The threshold is approximately 1V. It is important that once the UVLO is released, the error amplifier can drive the transconductance amplifier to stabilize the loop. If a capacitor is connected between the SENSE and COMP pins to create a pole, it will limit the slew rate of the error amplifier. To increase the bandwidth and ensure startup at low load current, it is recommended to create a zero along with the pole as shown in the UC39431 shunt regulator application. The error amplifier must slew 2.0V to drive the transconductance amplifier initially on.

VCC: The power connection for the device. The minimum to maximum operating voltage is 2.2V to 36.0V. The quiescent current is typically 0.50mA.

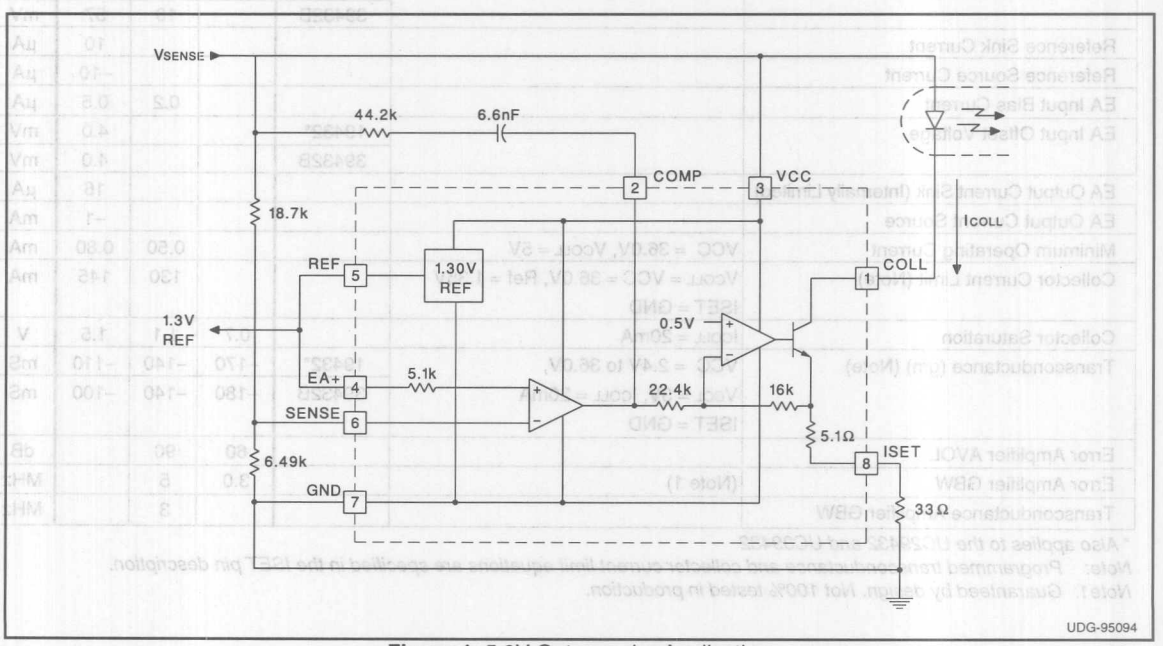


Figure 1. 5.0V Optocoupler Application

OVERVOLTAGE COMPARATOR APPLICATION

The signal VIN senses the input voltage. As long as the input voltage is less than 5.5V, the output is equal to the voltage on VIN. During this region of operation, the diode is reversed biased which keeps the EA+ pin at 1.3V. When VIN exceeds the over voltage threshold of 5.5V, the output is driven low. This forward biases the diode and creates hysteresis by changing the threshold to 4.5V.

OPTOCOUPLER APPLICATION

The optocoupler application shown takes advantage of the accessible pins REF and ISET. The ISET pin has a 33 ohm resistor to ground that protects the opto-coupler by limiting the current to about 16mA. This also lowers the transconductance to approximately 19mS. The ability to adjust the transconductance gives the designer further control of the loop gain. The REF pin is available to satisfy any high precision voltage requirements.

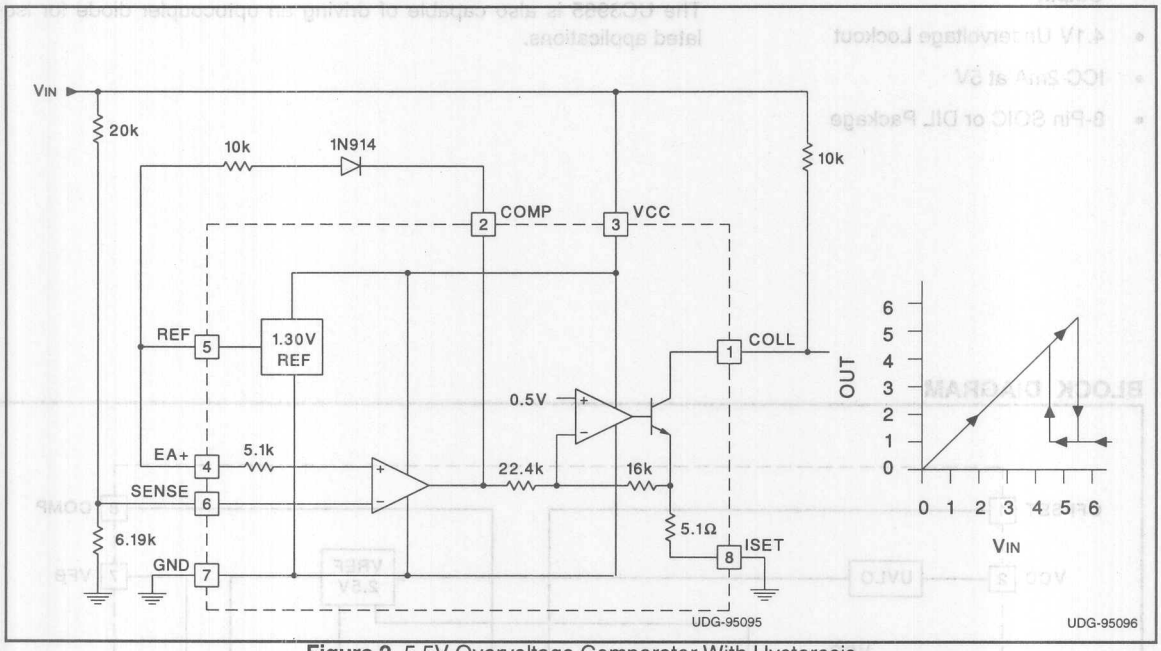


Figure 2. 5.5V Overvoltage Comparator With Hysteresis

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UNITRODE

UC1965
UC2965
UC3965

Precision Reference with Low Offset Error Amplifier

PRELIMINARY

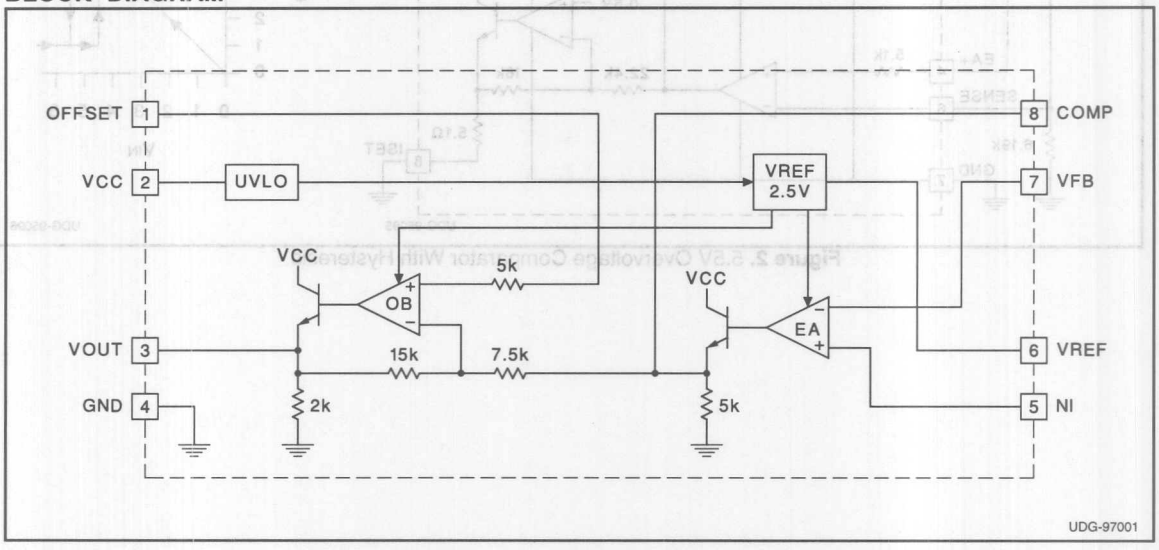
FEATURES

- Accessible 2.5V Precision Reference
- 0.4% Initial Reference Accuracy
- Low 1mV Offset Error Amplifier
- 2X Inverting Amplifier / Buffer Output
- 4.1V Undervoltage Lockout
- ICC 2mA at 5V
- 8-Pin SOIC or DIL Package

DESCRIPTION

The UC3965 includes an accessible 2.5V precision reference, a low offset error amplifier, a 2X inverting amplifier/buffer and an undervoltage lockout circuit. The IC is ideally suited for applications where high precision PWM power supply regulation is required. Typically, the error amplifier is connected to compare a fraction of the "to be regulated" power supply voltage to the on-chip 2.5V reference. The 2X amplifier/buffer output is then used to drive a PWM controller or regulator. The UC3965 is also capable of driving an optocoupler diode for isolated applications.

BLOCK DIAGRAM



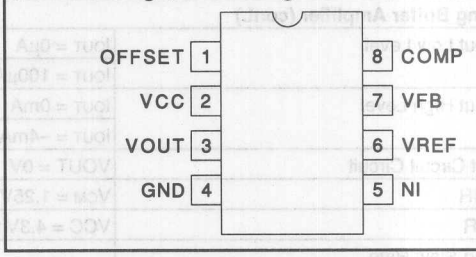
ABSOLUTE MAXIMUM RATINGS

VCC ..... –0.3V to 20V
VREF ..... –0.3V to 6V
VFB, COMP, NI, VOUT ..... –0.3V TO 6V
Storage Temperature ..... –65°C to +150°C
Junction Temperature ..... –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

Currents are positive into, negative out of the specified terminal. All voltages are with respect to ground. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

DIL-8, SOIC-8 (Top View)
J or N Package, DP Package



ELECTRICAL CHARACTERISTICS

Unless otherwise specified, T_A = 0°C to 70°C for the UC3965, –40°C to 85°C for the UC2965 and –55°C to 125°C for the UC1965; VCC = 5V, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
General					
VCC		4.3	5	20	V
Operating Current	VCC = 5V	1.5	2	4	mA
Undervoltage Current				200	µA
Minimum Voltage to Start		3.9	4.1	4.3	V
Hysteresis		200	300	400	mV
VREF					
VREF Initial Accuracy	25°C	2.49	2.5	2.51	V
VREF Over Temperature	–55°C to 125°C	2.48	2.5	2.52	V
Total Output Variation	Line, Load, Temperature	2.475	2.5	2.525	V
Line Regulation	VCC = 4.3V to 20V		2	10	mV
Load Regulation	0µA to 500µA		2	10	mV
Short Circuit Current	VREF = 0V		2		mA
Error Amplifier					
Input Bias	V_{CM} = 2.5V		200	400	nA
Input Offset Voltage	V_{CM} = 2.5V		1	2	mV
Input Offset Current	V_{CM} = 2.5V	–100	0	100	nA
Gain Bandwidth Product	V_{IN} = 50mV P-P (Note 1)		6		MHz
Open Loop Gain	VOUT = 1V to 3.75V	80	100		dB
Output Low Level	I_{OUT} = 0µA		0.8		V
	I_{OUT} = 100µA		1.2		V
Output High Level	I_{OUT} = 0µA		4		V
	I_{OUT} = –500µA		4		V
Short Circuit Circuit	V_{COMP} = 0V		8		mA
CMRR	V_{CM} = 1.25V to 3.75V	70	100		dB
PSRR	VCC = 4.3V to 20V	70	100		dB
Rising Slew Rate			2		V/µs
Falling Slew Rate			0.4		V/µs
Inverting Buffer Amplifier					
Input Bias	V_{CM} = 2.5V		1	2	µA
Output Offset Voltage	V_{CM} = 2.5V	–20	0	20	mV
Gain Bandwidth Product	V_{IN} = 50mV P-P (Note 1)		1.5		MHz
Closed Loop Gain	Inverting Gain	–2.04	–2	–1.96	V/V

ELECTRICAL CHARACTERISTICS (cont.) Unless otherwise specified, T_A = 0°C to 70°C for the UC3965, –40°C to 85°C for the UC2965 and –55°C to 125°C for the UC1965; VCC = 5V; $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Inverting Buffer Amplifier (cont.)					
Output Low Level	I_{OUT} = 0µA		0.3		V
	I_{OUT} = 100µA		0.5		V
Output High Level	I_{OUT} = 0mA		4		V
	I_{OUT} = –4mA		4		V
Short Circuit Circuit	VOUT = 0V		18		mA
CMRR	V_{CM} = 1.25V to 3.75V	70	100		dB
PSRR	VCC = 4.3V to 20V	70	100		dB
Rising Slew Rate			0.9		V/µs
Falling Slew Rate			0.9		V/µs

Note 1: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

COMP: Error amplifier output.

GND: Ground.

NI: Error amplifier non-inverting input.

OFFSET: Inverting buffer non-inverting input.

VCC: VCC supply and UVLO input.

VFB: Error amplifier inverting input.

VOUT: Inverting buffer output.

VREF: VREF output.

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Advanced Regulating Pulse Width Modulators

FEATURES

- Dual Uncommitted 40V, 200mA Output Transistors
- 1% Accurate 5V Reference
- Dual Error Amplifiers
- Wide Range, Variable Deadtime
- Single-ended or Push-pull Operation
- Under-voltage Lockout With Hysteresis
- Double Pulse Protection
- Master or Slave Oscillator Operation
- UC495A: Internal 39V Zener Diode
- UC495A: Buffered Steering Control

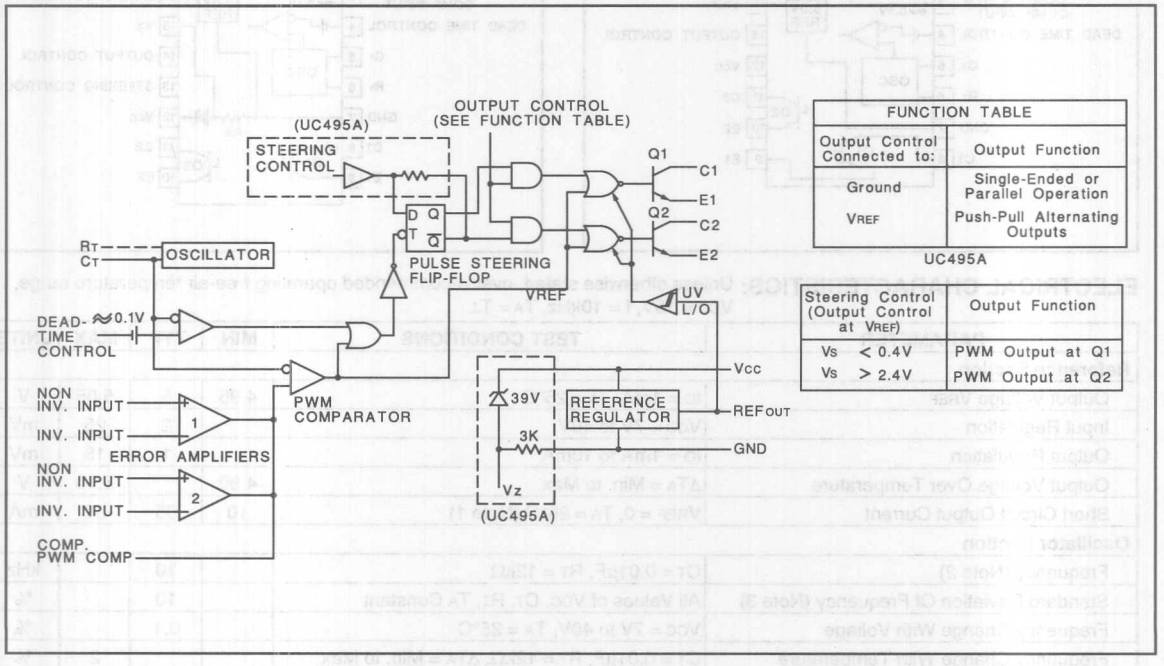
DESCRIPTION

This entire series of PWM modulators each provide a complete pulse width modulation system in a single monolithic integrated circuit. These devices include a 5V reference accurate to ±1%, two independent amplifiers usable for both voltage and current sensing, an externally synchronizable oscillator with its linear ramp generator, and two uncommitted transistor output switches. These two outputs may be operated either in parallel for single-ended operation or alternating for push-pull applications with an externally controlled dead-band. These units are internally protected against double-pulsing of a single output or from extraneous output signals when the input supply voltage is below minimum.

The UC495A contains an on-chip 39V zener diode for high-voltage applications where Vcc would be greater than 40V, and a buffered output steering control that overrides the internal control of the pulse steering flip-flop.

The UC494A is packaged in a 16-pin DIP, while the UC495A is packaged in an 18 pin DIP. The UC494A, UC495A are specified for operation over the full military temperature range of -55°C to +125°C, while the UC494AC, UC495AC are designed for industrial applications from 0°C to +70°C.

BLOCK DIAGRAM



FUNCTION TABLE	
Output Control Connected to:	Output Function
Ground	Single-Ended or Parallel Operation
VREF	Push-Pull Alternating Outputs

UC495A

Steering Control (Output Control at VREF)	Output Function
Vs < 0.4V	PWM Output at Q1
Vs > 2.4V	PWM Output at Q2

ABSOLUTE MAXIMUM RATINGS (Note 1, 2, 3)

Supply Voltage, V_{CC} (Note 2) 45V
Amplifier Input Voltages . . . . . V_{CC} + 0.3V
Collector Output Voltage 41V
Collector Output Current. 250mA
Continuous Total Dissipation 1000mW
@ (or below) 25°C free air temperature range (Note 3)
Storage Temperature Range . . . . . -65° to +150°C
Lead Temperature 1/16" (1.6mm) from case for 60 seconds,
J Package . . . . . 300°C
Lead Temperature 1/16" (1.6mm) from case for 10 seconds,
N Package . . . . . 260°C

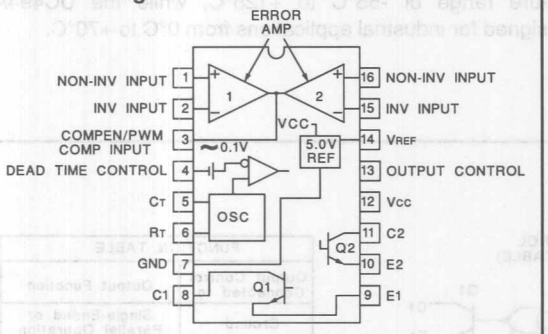
Note 1: Over operating free air temperature range unless otherwise noted.
Note 2: All voltage values are with respect to network ground terminal 3.
Note 3: Consult Packaging Section of Databook regarding thermal specifications and limitations of packages.

RECOMMENDED OPERATING CONDITIONS

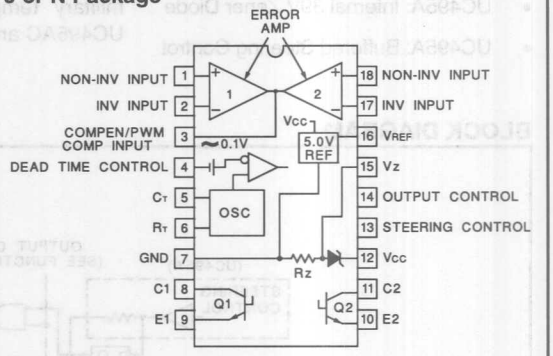
Supply Voltage V_{CC} . . . . . 7V to 40V
Error Amplifier Input Voltages . . . . . -0.3V to V_{CC}-2V
Collector Output Voltage 40V
Collector Output Current (each transistor) 200mA
Current into Feedback Terminal. 0.3mA
Timing Capacitor, C_T . . . . . 0.47nF to 10,000nF
Timing Resistor, R_T . . . . . 1.8kΩ to 500kΩ
Oscillator Frequency . . . . . 1kHz to 300kHz
Operating Free Air Temperature
UC494A, UC495A . . . . . -55°C to +125°C
UC494AC, UC495AC . . . . . 0°C to +70°C

CONNECTION DIAGRAMS

DIL-18 (TOP VIEW) UC494A/AC
J or N Package



DIL-18 (TOP VIEW) UC495A/AC
J or N Package



ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, over recommended operating free-air temperature range, V_{CC} = 15V, f = 10kHz, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Reference Section					
Output Voltage V_{REF}	I_O = 1mA, T_A = 25°C	4.95	5	5.05	V
Input Regulation	V_{CC} = 7V to 40V		2	25	mV
Output Regulation	I_O = 1mA to 10mA		1	15	mV
Output Voltage Over Temperature	ΔT_A = Min. to Max.	4.90		5.10	V
Short Circuit Output Current	V_{REF} = 0, T_A = 25°C (Note 1)	10	35	50	mA
Oscillator Section					
Frequency (Note 2)	C_T = 0.01µF, R_T = 12kΩ		10		kHz
Standard Deviation Of Frequency (Note 3)	All Values of V_{CC}, C_T, R_T, T_A Constant		10		%
Frequency Change With Voltage	V_{CC} = 7V to 40V, T_A = 25°C		0.1		%
Frequency Change With Temperature	C_T = 0.01µF, R_T = 12kΩ, ΔT_A = Min. to Max.			2	%
Deadtime Control Section (Output Control Connected to V_{REF})					
Input Bias Current (Pin 4)	$V_{(PIN\ 4)}$ = 0V to 5.25V		-2	-10	µA
Maximum Duty-Cycle (Each Output)	$V_{(PIN\ 4)}$ = 0V	45			%

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, over recommended operating free-air temperature range, V_{CC} = 15V, f = 10kHz, $T_A = T_J$.

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNITS
Deadtime Control Section (cont.) (Output Control Connected to V_{REF})							
Input Threshold Voltage (Pin 4)		Zero Duty-Cycle			3	3.3	V
		Maximum Duty-Cycle		0			V
Amplifier Section							
Input Offset Voltage		$V_{O\ (PIN\ 3)}$ = 2.5V			2	10	mV
Input Offset Current		$V_{O\ (PIN\ 3)}$ =2.5V			25	250	nA
Input Bias Current		$V_{O\ (PIN\ 3)}$ = 2.5V			-0.2	-1	µA
Common-Mode Input Voltage Range		V_{CC} = 7V to 40V		.03 to V_{CC} -2			V
Open Loop Voltage Gain		ΔV_O = 3V, V_O = 0.5V to 3.5 V		70	95		dB
Unity Gain Bandwidth					800		kHz
Common-Mode Rejection Ratio		V_{CC} = 40V, T_A = 25°C		65	80		dB
Output Sink Current (Pin 3)		V_{ID} = -15mV to -5V, $V_{(PIN\ 3)}$ = 0.7V		0.3	0.7		mA
Output Source Current (Pin 3)		V_{ID} = 15mV to 5V, $V_{(PIN\ 3)}$ = 3.5V		-2			mA
Output Section							
Collector Off-State Current		V_{CE} = 40V, V_{CC} = 40V			2	100	µA
Emitter Off-State Current		V_{CC} = V_C = 40V, V_E = 0				-100	µA
Collector - Emitter Saturation Voltage	Common-Emitter	V_E = 0, I_C = 200mA			1.1	1.3	V
	Emitter-Follower	V_C = 15V, I_E = -200mA			1.5	2.5	V
Output Control Input Current		$V_I = V_{REF}$				3.5	mA
PWM Comparator Section							
Input Threshold Voltage (Pin 3)		Zero Duty-Cycle			4	4.5	V
Input Sink Current (Pin 3)		$V_{(PIN\ 3)}$ = 0.7V		0.3	0.7		mA
Steering Control (UC495A, See Function Table)							
Input Current		$V_{(PIN\ 13)}$ = 0.4V, Q_1 ACTIVE				-200	µA
		$V_{(PIN\ 13)}$ = 2.4V, Q_2 ACTIVE				300	µA
Deadband					500		mV
Zener Diode Circuit (UC495A)							
Breakdown Voltage		V_{CC} = 45V, I_Z = 2mA		36	39	45	V
Sink Current		$V_{(PIN\ 15)}$ = 1V		0.2	0.3	0.6	mA
Total Device							
Standby Supply Current		Pin 6 at V_{REF}, All other inputs and outputs open	V_{CC} = 15V		6	10	mA
			V_{CC} = 40V		9	15	mA
Under Voltage Lockout				3.5		6.5	V
Hysteresis					300		mV
Switching Characteristics (T_A = 25°C)							
Output Voltage Rise Time		Common-Emitter Configuration			100	200	ns
Output Voltage Fall Time		R_L = 68Ω, C_L = 15pF			25	100	ns
Output Voltage Rise Time		Emitter-Follower Configuration			100	200	ns
Output Voltage Fall Time		R_L = 68Ω, C_L=15pF			40	100	ns

Note 1: Duration of the short circuit should not exceed one second.

Note 2: Frequency for other values of C_T and R_T is approximately $f = \frac{1.1}{RTCT}$

Note 3: Standard deviation is a measure of the statistical distribution about the mean as derived from the formula:

$$\sigma = \sqrt{\frac{\sum_{n=1}^{n} (X_n - X)^2}{n-1}}$$

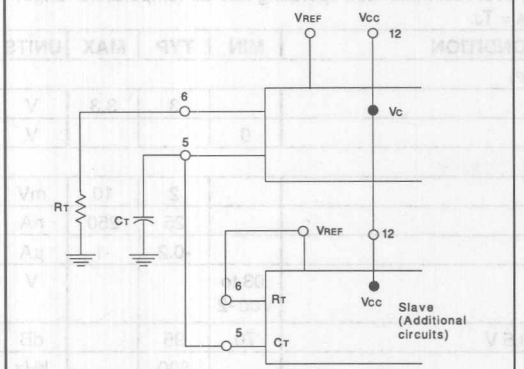


Figure 1. Slaving Two or More Control Circuits

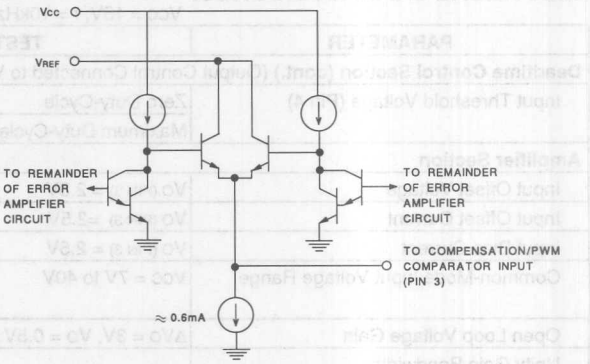


Figure 2. Output Circuit of Error Amplifiers

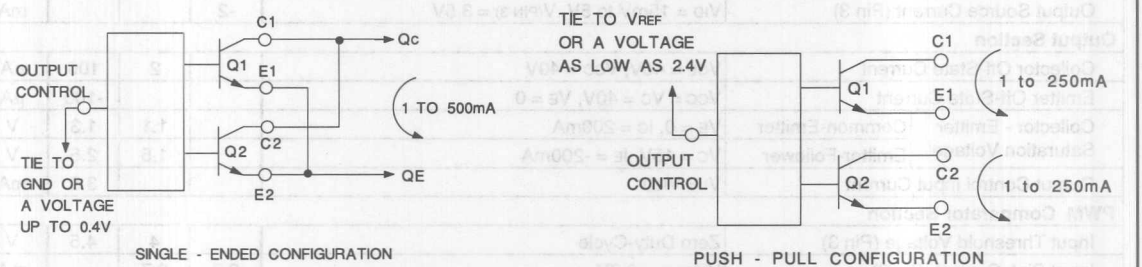


Figure 3. Output Connections for Single-Ended and Push-Pull Configurations

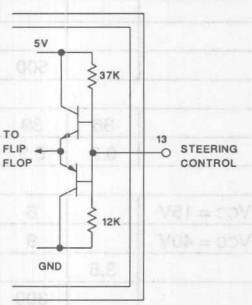


Figure 4. Internal Buffer with Deadband for Steering Control on UC495A

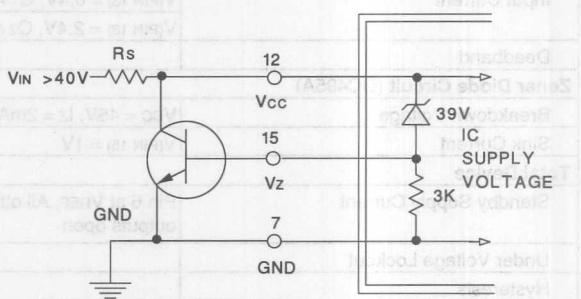


Figure 5. Operation with VIN > 40V Using Internal Zener

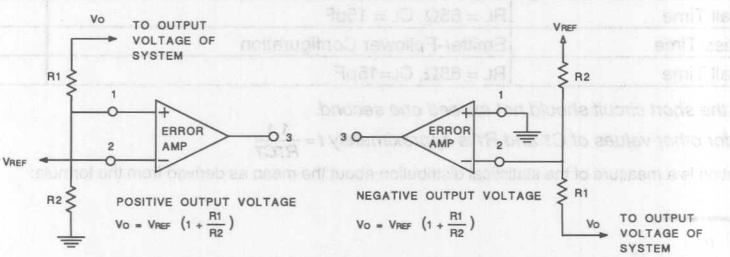


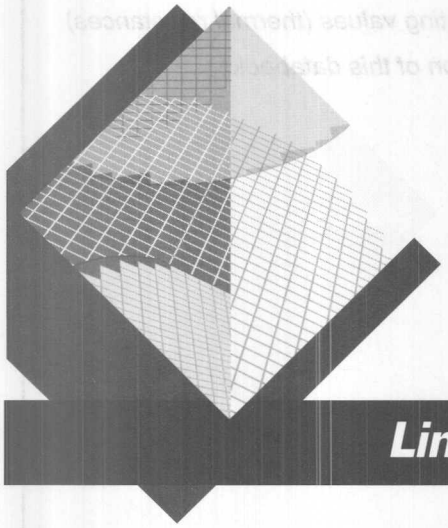
Figure 6. Error Amplifier Sensing Techniques

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Consult Applications Handbook for available applications/design notes.

Datasheets in this section are organized in numeric order using the commercial part number.



Linear Regulators

4

Packaging Note:

- *Values listed for recommended lead soldering time and temperature apply to ceramic thru-hole components only. Please consult the Packaging Section of this databook for recommendations on plastic SMD board attach processing.*

- *Unless otherwise noted, thermal resistance values listed on individual data sheets are for the device as it operates in a plastic thru-hole package. Results for other packaging options can be inferred by scaling the package rating values (thermal resistances) presented in the Packaging Section of this databook.*

Linear Controllers & Linear Regulators

Linear Controllers	UNITRODE PART NUMBER		
	UC3832	UC3833	UC3834
Type of Output	Positive Adjustable	Positive Adjustable	Positive/Negative Adjustable
Maximum Input Voltage	36V	36V	40V
Minimum Output Voltage	2.0V	2.0V	+1.5V/–2.0V
Output Drive	300mA	300mA	350mA
Type of Short Circuit Limit	Duty Cycle	Duty Cycle	Foldback
Reference Voltage Accuracy	2%	2%	3%/4%
Special Features	Multiple Pins Accessible	8-Pin Package	
Application/Design Note	DN-61, U-116, U-152	DN-32, DN-61, U-116, U-152	U-95

Linear Controllers (cont'd)	UNITRODE PART NUMBER		
	UC3835	UC3836	UCC3837 +
Type of Output	5V Fixed	Positive Adjustable	Positive Adjustable
Maximum Input Voltage	40V	40V	12V
Minimum Output Voltage		2.5V	1.5V
Output Drive	500mA	500mA	1.5mA
Type of Short Circuit Limit	Foldback	Foldback	Duty Cycle
Reference Voltage Accuracy	2%	2%	2%
Special Features	Built-in R_{SENSE}	Built-in R_{SENSE}	Internal Charge Pump Direct N-FET Drive

Linear Regulators	UNITRODE PART NUMBER		
	UCC381 +	UCC383 +	UCC384 +
Output Voltage	3.3, 5, ADJ	3.3, 5, ADJ	5, 12, ADJ
Dropout Voltage	0.45V at 1A	0.45V at 3A	0.2V at 500mA
Quiescent Current	400µA	400µA	240µA
Maximum Input Voltage	9V	9V	–16V
Shutdown Current	10µA	10µA	20µA
Voltage Tolerance	2.5%	2.5%	2.5%
Line Regulation	0.01%/V	0.01%/V	0.01%/V
Load Regulation	0.1%, I_{OUT} = 0 to 1A	0.2%, I_{OUT} = 10mA to 3A	0.1%, I_{OUT} = 0 to 500mA

+ New Product

Low Dropout Linear Regulators	UNITRODE PART NUMBER			
	UC382-1	UC382-2	UC382-3	UC382-ADJ
Output Voltage	1.5V	2.1V	2.5V	1.2V/Adjustable
Dropout Voltage	450mV at 3A	450mV at 3A	450mV at 3A	450mV at 3A
Output Voltage Accuracy	1%	1%	1%	1%
Maximum Input Voltage	7.5V	7.5V	7.5V	7.5V
Special Features	Fast Transient Response	Fast Transient Response	Fast Transient Response	Fast Transient Response

Low Dropout Linear Regulators (cont'd)	UNITRODE PART NUMBER			
	UC385-1 +	UC385-2 +	UC385-3 +	UC385-ADJ +
Output Voltage	1.5V	2.1V	2.5V	1.2V/Adjustable
Dropout Voltage	450mV at 5A	450mV at 5A	450mV at 5A	450mV at 5A
Output Voltage Accuracy	1%	1%	1%	1%
Maximum Input Voltage	7.5V	7.5V	7.5V	7.5V
Special Features	Fast Transient Response	Fast Transient Response	Fast Transient Response	Fast Transient Response

Special Function Circuits	UNITRODE PART NUMBER	
	UCC3831 +	UC560
Part Name	Universal Serial Bus Power Controller	SCSI Single Ended Source/ Sink Regulator
Description	Powers Four 5V Peripherals and One 3.3V USB Controller	18 and 27 Line SCSI Termination Applications

+ New Product

Low Dropout 1 Ampere Linear Regulator Family

FEATURES

- Precision Positive Linear Voltage Regulation
- 0.5V Dropout at 1A
- Guaranteed Reverse Input/ Output Voltage Isolation with Low Leakage
- Low Quiescent Current Irrespective of Load
- Adjustable Output Voltage Version
- Fixed Versions for 3.3V and 5V Outputs
- Logic Shutdown Capability
- Short Circuit Power Limit of 3% • VIN • Current Limit
- Remote Load Voltage for Accurate Load Regulation

DESCRIPTION

The UCC381-3/-5/-ADJ family of positive linear series pass regulators is tailored for low drop out applications where low quiescent power is important. Fabricated with a BiCMOS technology ideally suited for low input to output differential applications, the UCC381 will pass 1A while requiring only 0.5V of input voltage headroom. Dropout voltage decreases linearly with output current, so that dropout at 200mA is less than 100mV. Quiescent current is always less than 450µA. To prevent reverse current conduction, on-chip circuitry limits the minimum forward voltage to typically 50mV. Once the forward voltage limit is reached, the input-output differential voltage is maintained as the input voltage drops until undervoltage lockout disables the regulator.

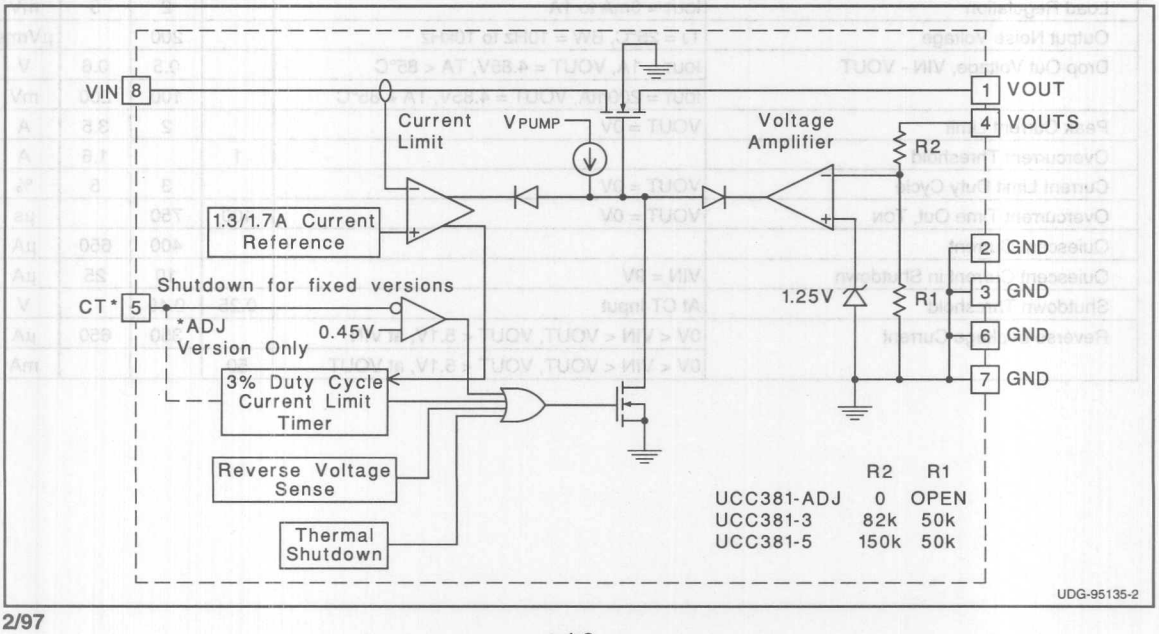
UCC381-3 and UCC381-5 versions have on-chip resistor networks preset to regulate either 3.3V or 5.0V, respectively. Furthermore, remote sensing of the load voltage is possible by connecting the VOUTS pin directly at the load. The output voltage is then regulated to 1.5% at room temperature and better than 2.5% over temperature. The UCC381-ADJ version has a regulated output voltage programmed by an external user-definable resistor ratio.

Short circuit current is internally limited. The device responds to a sustained overcurrent condition by turning off after a TON delay. The device then stays off for a period, TOFF, that is 32 times the TON delay. The device then begins pulsing on and off at the TON/(TON+TOFF) duty cycle of 3%. This drastically reduces the power dissipation during short circuit such that heat sinking, if at all required, must only accommodate normal operation. On the fixed output versions of the device TON is fixed at 400µs – a guaranteed minimum. On the adjustable version an external capacitor sets the on time. The off time is always 32 times TON.

The UCC381 can be shutdown to 25µA (max) by pulling the CT pin low.

continued

BLOCK DIAGRAM



DESCRIPTION (cont.)

Internal power dissipation is further controlled with thermal overload protection circuitry. Thermal shutdown occurs if the junction temperature exceeds 165°C. The chip will remain off until the temperature has dropped 20°C.

The UCC281 series is specified for operation over the industrial range of –40°C to +85°C, and the UCC383 series is specified from 0°C to +70°C. These devices are available in the 8 pin DP surface mount power package. For other packaging options consult the factory.

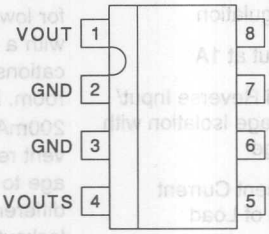
ABSOLUTE MAXIMUM RATINGS

VIN 9V
CT . . . . . –0.3 to 3V
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages. All voltages are referenced to GND.

CONNECTION DIAGRAMS

SOIC-8 (Top View)
DP Package



* ADJ version only

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, these specifications hold for T_A = 0°C to 70°C for the UCC381-X series and –40°C to +85°C for the UCC283-X series, VIN = VOUT + 1.5V, I_{OUT} = 0mA, C_{OUT} = 2.2µF. CT = 1500pF for the UCC381-ADJ version and VOUT set to 5V. $T_J = T_A$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
UCC381-5 Fixed 5V, 1A Family					
Output Voltage	T_J = 25°C	4.925	5	5.075	V
	Over Temperature	4.875		5.125	V
Line Regulation	VIN = 5.15V to 9V		1	3	mV
Load Regulation	I_{OUT} = 0mA to 1A		2	5	mV
Output Noise Voltage	T_J = 25°C, BW = 10Hz to 10kHz		200		µVrms
Drop Out Voltage, VIN - VOUT	I_{OUT} = 1A, VOUT = 4.85V, TA < 85°C		0.5	0.6	V
	I_{OUT} = 200mA, VOUT = 4.85V, TA < 85°C		100	200	mV
Peak Current Limit	VOUT = 0V		2	3.5	A
Overcurrent Threshold		1		1.6	A
Current Limit Duty Cycle	VOUT = 0V		3	5	%
Overcurrent Time Out, T_{ON}	VOUT = 0V	400	750		µs
Quiescent Current			400	650	µA
Quiescent Current in Shutdown	VIN = 9V		10	25	µA
Shutdown Threshold	At CT Input	0.25	0.45		V
Reverse Leakage Current	0V < VIN < VOUT, VOUT < 5.1V, at VIN		350	650	µA
	0V < VIN < VOUT, VOUT < 5.1V, at VOUT	50			mA

ELECTRICAL CHARACTERISTICS (cont.): Unless otherwise stated, these specifications hold for T_A = 0°C to 70°C for the UCC381-X series and –40°C to +85°C for the UCC283-X series, VIN = VOUT + 1.5V, I_{OUT} = 0mA, C_{OUT} = 2.2µF. CT = 1500pF for the UCC381-ADJ version and VOUT set to 5V. $T_J = T_A$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
UCC381-3 Fixed 3.3V, 1A Family					
Output Voltage	T_J = 25°C	3.25	3.3	3.35	V
	Over Temperature	3.22		3.38	V
Line Regulation	VIN = 3.45V to 9V		1	3	mV
Load Regulation	I_{OUT} = 0mA to 1A		2	5	mV
Output Noise Voltage	T_J = 25°C, BW = 10Hz to 10kHz		200		µVrms
Dropout Voltage, VIN - VOUT	I_{OUT} = 1A, VOUT = 3.15V, T_A < 85°C		0.6	0.8	V
	I_{OUT} = 200mA, VOUT = 3.15V, TA < 85°C		100	200	mV
Peak Current Limit	VOUT = 0V		2	3.5	A
Overcurrent Threshold		1		1.6	A
Current Limit Duty Cycle	VOUT = 0V		3	5	%
Overcurrent Time Out, T_{ON}	VOUT = 0V	400	750		µs
Quiescent Current			400	650	µA
Quiescent Current in Shutdown	VIN = 9V		10	25	µA
Shutdown Threshold	At CT Input	0.25	0.45		V
Reverse Leakage Current	0V < VIN < VOUT, VOUT < 3.35V, at VIN		350	650	µA
	0V < VIN < VOUT, VOUT < 3.35V, at VOUT	50			µA
UCC381-ADJ Adjustable Output, 1A Family					
Regulating Voltage at ADJ Input	T_J = 25°C	1.23	1.25	1.27	V
	Over Temperature	1.22		1.28	V
Line Regulation, at ADJ Input	VIN = VOUT + 150mV to 9V		1	3	mV
Load Regulation, at ADJ Input	IOUT = 0mA to 1A		2	5	mV
Output Noise Voltage	T_J = 25°C, BW = 10Hz to 10kHz		200		µVrms
Dropout Voltage, VIN - VOUT	IOUT = 1A, VOUT = 4.85V		0.5	0.6	V
	IOUT = 200mA, VOUT = 4.85V		100	200	mV
Peak Current Limit	VOUT = 0V		2	3.5	A
Overcurrent Threshold		1		1.6	A
Current Limit Duty Cycle	VOUT = 0V		3	5	%
Overcurrent Time Out, TON	VOUT = 0V, CT = 1500pF	400	1000		µs
Quiescent Current			400	650	µA
Quiescent Current in Shutdown	VIN = 9V		10	25	µA
Shutdown Threshold	At CT Input	0.25	0.45		V
Reverse Leakage Current	0V < VIN < VOUT, VOUT < 5.1V, at VIN		350	650	µA
	0V < VIN < VOUT, VOUT < 5.1V, at VOUT	50			µA
Bias Current at ADJ Input			100	250	nA

PIN DESCRIPTIONS

CT: For UCC381-3 and UCC381-5 versions, this is the shutdown pin which, when pulled low, turns off the regulator output and puts the device in a low current state. For the UCC381-ADJ version, a capacitor is required between the CT pin and GND to set the TON time during overcurrent according to the following (typical) equation:

$$T_{ON} = 660{,}000 \bullet C_{CT}.$$

GND: All voltages are measured with respect to this pin. This is the low noise ground reference input for regulation. The output decoupling capacitor should be tied to Pin 7.

VIN: Positive supply input for the regulator. Bypass this pin to GND with at least 1µF of low ESR, ESL capacitance if the source is located further than 1 inch from the device.

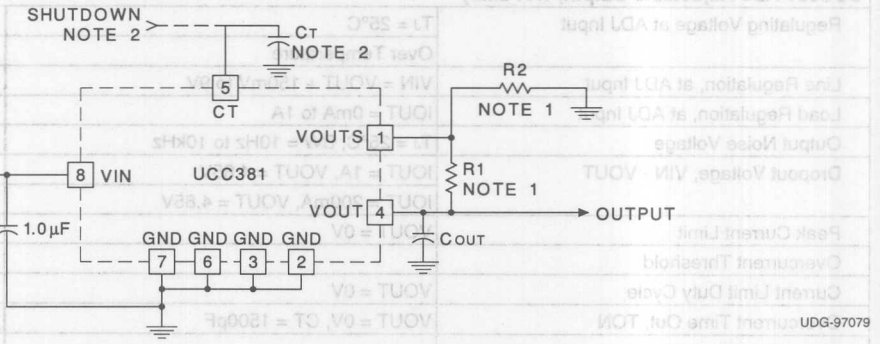
VOUT: Output for regulator. Regulator does not require a minimum output capacitor for stability. Choose the appropriate size capacitor for the application with respect to the required transient loading. For example, if the load is very dynamic, a large capacitor will smooth out the response to load steps.

VOUTS: Feedback for regulator sensing of the output voltage. For loads which are a considerable resistive distance from the VOUT pin, the VOUTS pin can be used to move the resistance into the control loop of the regulator, thereby effectively canceling the IR drop associated with the load path. For local regulation, merely connect this pin directly to the VOUT pin. For the UCC381-ADJ version, the output voltage can be set by two external resitors according to the following relationship:

$$V_{OUT} = 1.25 \bullet \left(1 + \frac{R1}{R2}\right)$$

where R1 is a resistor connected between VOUT and VOUTS and R2 is a resistor connected between VOUTS and GND.

TYPICAL APPLICATION CIRCUIT



Note 1: R1 and R2 for adjustable version only.
For 3.3V and 5V versions connect VOUT to VOUTS. See Pin Descriptions.
Note 2: CT timing capacitor is for adjustable version only.
For 3.3V and 5V versions, the CT pin is used to enable or shutdown the part. See Pin Descriptions.

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

Fast LDO Linear Regulator

FEATURES

- Fast Transient Response
- 10mA to 3A Load Current
- Short Circuit Protection
- Maximum Dropout of 450mV at 3A Load Current
- Separate Bias and VIN Pins
- Available in Adjustable or Fixed Output Voltages
- 5 Pin Package allows Kelvin Sensing of Load Voltage
- Reverse Current Protection

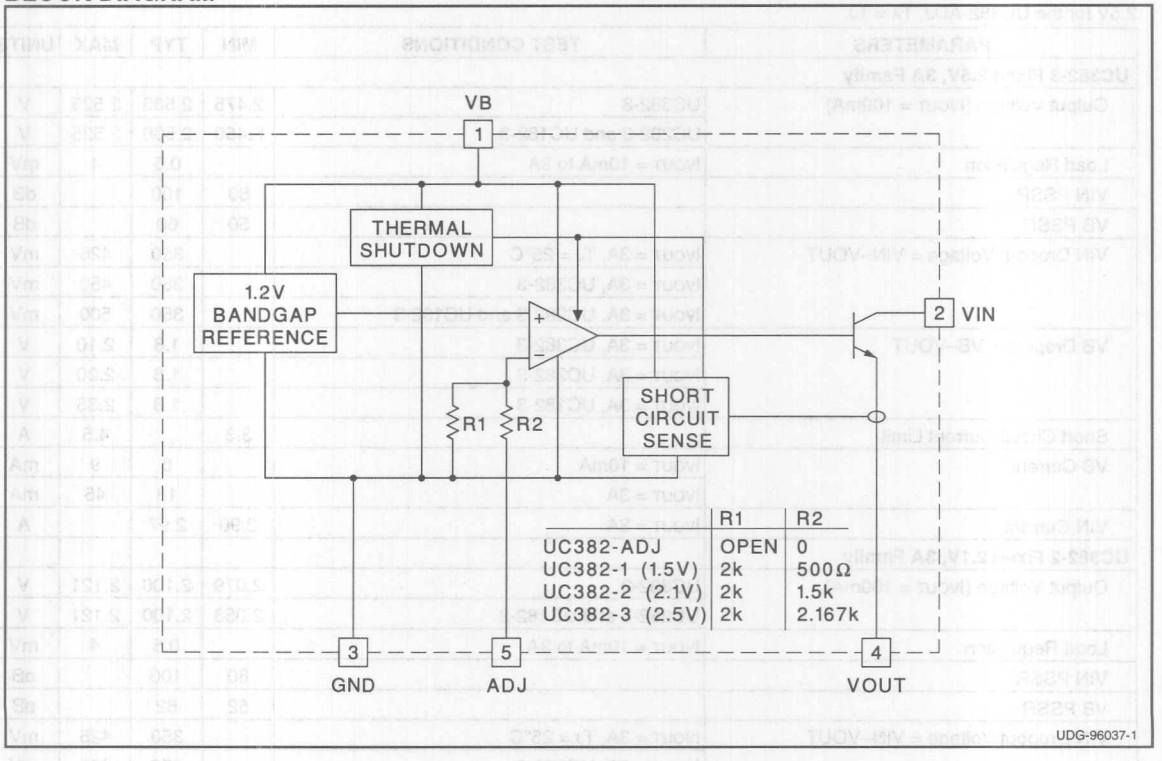
DESCRIPTION

The UC382 is a low dropout linear regulator providing a quick response to fast load changes. Combined with its precision on-board reference, the UC382 excels at driving GTL and BTL buses. Due to its fast response to load transients, the total capacitance required to decouple the regulator's output can be significantly decreased when compared to standard LDO linear regulators.

Dropout voltage (VIN to VOUT) is only 450mV maximum at 100°C and 350mV typical at 3A load.

The on-board bandgap reference is stable with temperature and scaled for a 1.200V input to the internal power amplifier. The UC382 is available in fixed output voltages of 1.5V, 2.1V, or 2.5V. The output voltage of the adjustable version can be set with two external resistors. If the external resistors are omitted, the output voltage defaults to 1.2V.

BLOCK DIAGRAM



	R1	R2
UC382-ADJ	OPEN	0
UC382-1 (1.5V)	2k	500Ω
UC382-2 (2.1V)	2k	1.5k
UC382-3 (2.5V)	2k	2.167k

ABSOLUTE MAXIMUM RATINGS

VB 13V
VIN ..... +7.5V
Output Voltage ..... +1.2V to 6.0V
Storage Temperature ..... –65°C to +150°C
Junction Temperature ..... –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

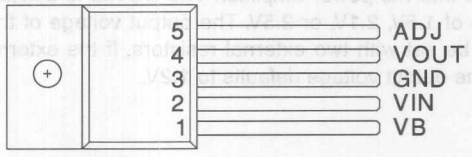
ORDERING INFORMATION

UC □ 82 □ - □
- Output Voltage
- Package
- Temperature Range

Temperature Range	Package	Output Voltage
1: –55°C to +125°C	T: TO-220	1: 1.5V
2: –25°C to +100°C	TD: TO-263	2: 2.1V
3: 0°C to +100°C		3: 2.5V
		ADJ: 1.2V or Adjustable

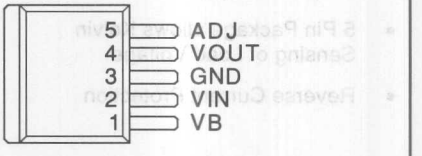
CONNECTION DIAGRAMS

5-Pin TO-220 (Top View)
T Package



Note: Tab tied to Pin 3.

5-Pin TO-263 (Top View)
TD Package



Note: Tab tied to Pin 3.

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these parameters apply for T_A = –55°C to 125°C for the UC182-X series, –25°C to +100°C for the UC282-X series and 0°C to +100°C for the UC382-X, VB = 5V; VIN = 3.3V, VOUT = 2.5V for the UC382-ADJ, T_A = T_J.

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
UC382-3 Fixed 2.5V, 3A Family					
Output Voltage (I_{VOUT} = 100mA)	UC382-3	2.475	2.500	2.525	V
	UC282-3 and UC182-3	2.450	2.500	2.525	V
Load Regulation	I_{VOUT} = 10mA to 3A		0.5	4	mV
VIN PSSR		80	100		dB
VB PSSR		50	60		dB
VIN Dropout Voltage = VIN–VOUT	I_{VOUT} = 3A, T_J = 25°C		350	425	mV
	I_{VOUT} = 3A, UC382-3		350	450	mV
	I_{VOUT} = 3A, UC282-3 and UC182-3		350	500	mV
VB Dropout = VB–VOUT	I_{VOUT} = 3A, UC382-3		1.8	2.10	V
	I_{VOUT} = 3A, UC282-3		1.8	2.20	V
	I_{VOUT} = 3A, UC182-3		1.8	2.35	V
Short Circuit Current Limit		3.3		4.5	A
VB Current	I_{VOUT} = 10mA		6	9	mA
	I_{VOUT} = 3A		18	45	mA
VIN Current	I_{VOUT} = 3A	2.96	2.97		A
UC382-2 Fixed 2.1V, 3A Family					
Output Voltage (I_{VOUT} = 100mA)	UC382-2	2.079	2.100	2.121	V
	UC282-2 and UC182-2	2.058	2.100	2.121	V
Load Regulation	I_{VOUT} = 10mA to 3A		0.5	4	mV
VIN PSSR		80	100		dB
VB PSSR		52	62		dB
VIN Dropout Voltage = VIN–VOUT	I_{VOUT} = 3A, T_J = 25°C		350	425	mV
	I_{VOUT} = 3A, UC382-2		350	450	mV
	I_{VOUT} = 3A, UC282-2 and UC182-2		350	500	mV

ELECTRICAL CHARACTERISTICS (cont.): Unless otherwise stated, these parameters apply for T_A = –55°C to 125°C for the UC182-X series, –40°C to +100°C for the UC282-X series and 0°C to +100°C for the UC382-X, VB = 5V; VIN = 3.3V, VOUT = 2.5V for the UC382-ADJ, $T_A = T_J$.

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
UC382-2 Fixed 2.1V, 3A Family (cont.)					
VB Dropout = VB–VOUT	I_{VOUT} = 3A, UC382-2		1.8	2.10	V
	I_{VOUT} = 3A, UC282-2		1.8	2.20	V
	I_{VOUT} = 3A, UC182-2		1.8	2.35	V
Short Circuit Current Limit		3.3		4.5	A
VB Current	I_{VOUT} = 10mA		6	9	mA
	I_{VOUT} = 3A		18	45	mA
VIN Current	I_{VOUT} = 3A	2.96	2.97		A
UC382-1 Fixed 1.5V, 3A Family					
Output Voltage (I_{VOUT} = 100mA)	UC382-1	1.485	1.500	1.515	V
	UC282-1 and UC182-1	1.470	1.500	1.515	V
Load Regulation	I_{VOUT} = 10mA to 3A		0.5	4	mV
VIN PSSR		80	100		dB
VB PSSR		55	65		dB
VIN Dropout Voltage = VIN–VOUT	I_{VOUT} = 3A, TJ = 25°C		350	425	mV
	I_{VOUT} = 3A, UC282-1		350	450	mV
	I_{VOUT} = 3A, UC282-2 and UC182-1		350	500	mV
VB Dropout = VB–VOUT	I_{VOUT} = 3A, UC382-1		1.8	2.10	V
	I_{VOUT} = 3A, UC282-1		1.8	2.20	V
	I_{VOUT} = 3A, UC182-1		1.8	2.35	V
Short Circuit Current Limit		3.3		4.5	A
VB Current	I_{VOUT} = 10mA		6	9	mA
	I_{VOUT} = 3A		18	45	mA
VIN Current	I_{VOUT} = 3A	2.96	2.97		A
UC382-ADJ Adjustable, 3A Family					
ADJ Voltage (I_{VOUT} = 100 mA)	UC382-ADJ	1.188	1.200	1.212	V
	UC282-ADJ and UC182-ADJ	1.176	1.200	1.212	V
Load Regulation	I_{VOUT} = 10mA to 3A		0.5	4	mV
VIN PSSR	VOUT Programmed for 2.5V	80	100		dB
VB PSSR	VOUT Programmed for 2.5V	50	60		dB
VIN Dropout Voltage = VIN–VOUT	I_{VOUT} = 3A, TJ = 25°C		350	425	mV
	I_{VOUT} = 3A, UC382-ADJ		350	450	mV
	I_{VOUT} = 3A, UC282-ADJ and UC182-ADJ		350	500	mV
VB Dropout = VB–VOUT	I_{VOUT} = 3A, UC382-ADJ		1.8	2.10	V
	I_{VOUT} = 3A, UC282-ADJ		1.8	2.20	V
Short Circuit Current Limit		3.3		4.5	A
VB Current	I_{VOUT} = 10mA		6	9	mA
	I_{VOUT} = 3A		18	45	mA
VIN Current	I_{VOUT} = 3A	2.96	2.97		A

PIN DESCRIPTIONS

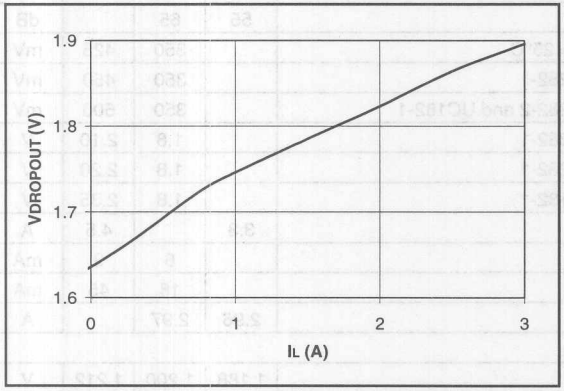
ADJ: In the adjustable version, the user programs the output voltage with two external resistors. The resistors should be 0.1% for high accuracy. The output amplifier is configured as a non-inverting operational amplifier. The resistors should meet the criteria of R3 || R4 < 100Ω. Connect ADJ to VOUT for an output voltage of 1.2V. Note that the point at which the feedback network is connected to the output is the Kelvin sense point.

GND: For accurate results, the GND pin should be referenced to the load ground.

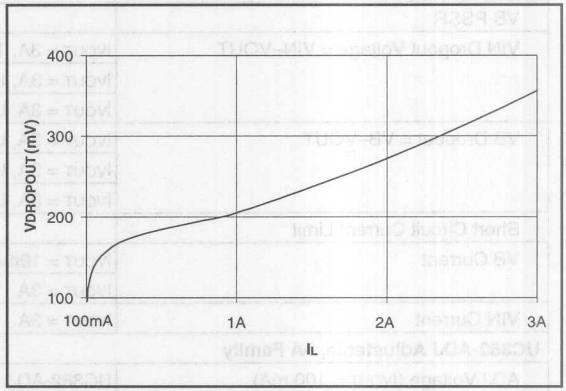
VB: Supplies power to all circuits of the regulator except the collector of the output power transistor. The 2V headroom from VB to VOUT allows the use of a Darlington output stage for inherently low output impedance and fast response. (Dropout is derated for junction temperatures below 0°C.)

VIN: Supplies the current to the collector of the output power transistor only. The dropout (VIN-VOUT) is under 100mV for light loads; maximum dropout is 450mV at 3A for T_J = 0°C to +110°C. (Dropout is derated for junction temperatures over 110°C.) At full load, the majority of the VB current is going to the load.

VOUT: This pin should be connected to the load via a low impedance path. Avoid connectors which add significant inductance and resistance. Note that even though a Kelvin sense is available through a 5 pin package, care must be taken since voltage drops along wire traces add to the dropout voltage.



Typical Dropout (V_B - V_{OUT}), T_J = 27°C



Typical Dropout (V_{IN} - V_{OUT}), T_J = 27°C

APPLICATION INFORMATION

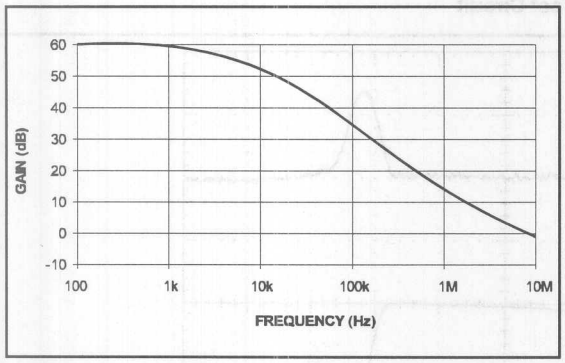
The UC382 is easy to use. The adjustable version requires two 0.1% resistors to set the output voltage. The fixed versions of the UC382 require no external resistors. All versions of the UC382 require decoupling capacitors on the input and output. In a typical application, VB and VIN are driven from switching power supplies which may have large filter capacitors at their outputs. If the UC382 is further than 12 inches from the power supply, it is recommended to add local decoupling as close as possible to the linear regulator.

Decouple the output of the UC382 with at least 100µF of high quality tantalum or Sanyo OSCON capacitors close to the VOUT pin for maximum stability. Many applications involving ultra fast GTL or BTL applications require additional capacitance close to the load. The exact amount will vary according to speed and magnitude of the load transients and the tolerance allowed for transients on VOUT. When specifying the decoupling capacitors, the series resistance of the capacitor bank is an important factor in its ability to filter load transients.

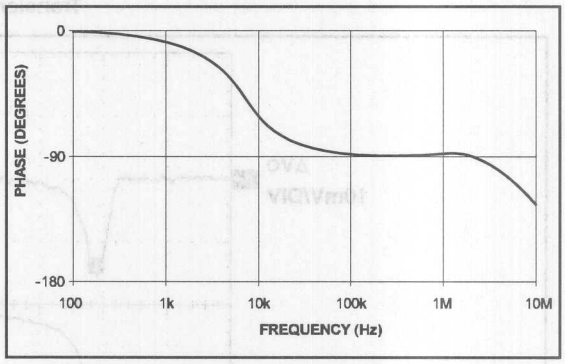
APPLICATION INFORMATION (cont.)

The UC382 allows for Kelvin sensing the voltage at the load. This improves regulation performance and eliminates the voltage drops due to wire trace resistance. This voltage drop must be added to the headroom (VIN to VOUT and VB to VOUT). The dropout of 450mV is measured at the pins and does not include additional drops due to trace resistance. The minimum load current is 10mA.

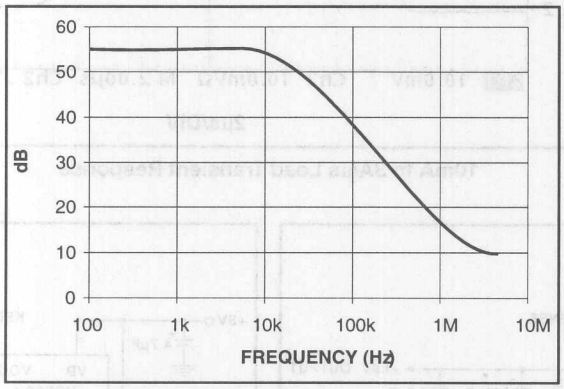
Two or more UC382's may be used in parallel. While stable, this arrangement does degrade the transient response.



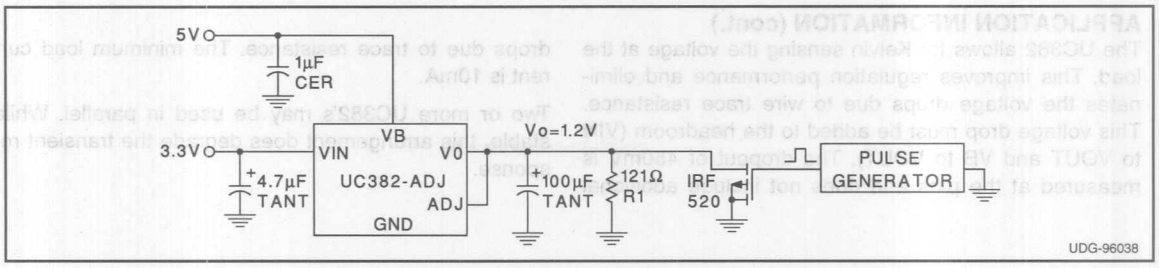
Open Loop Gain
(100μF Output Capacitance, 1A Load)



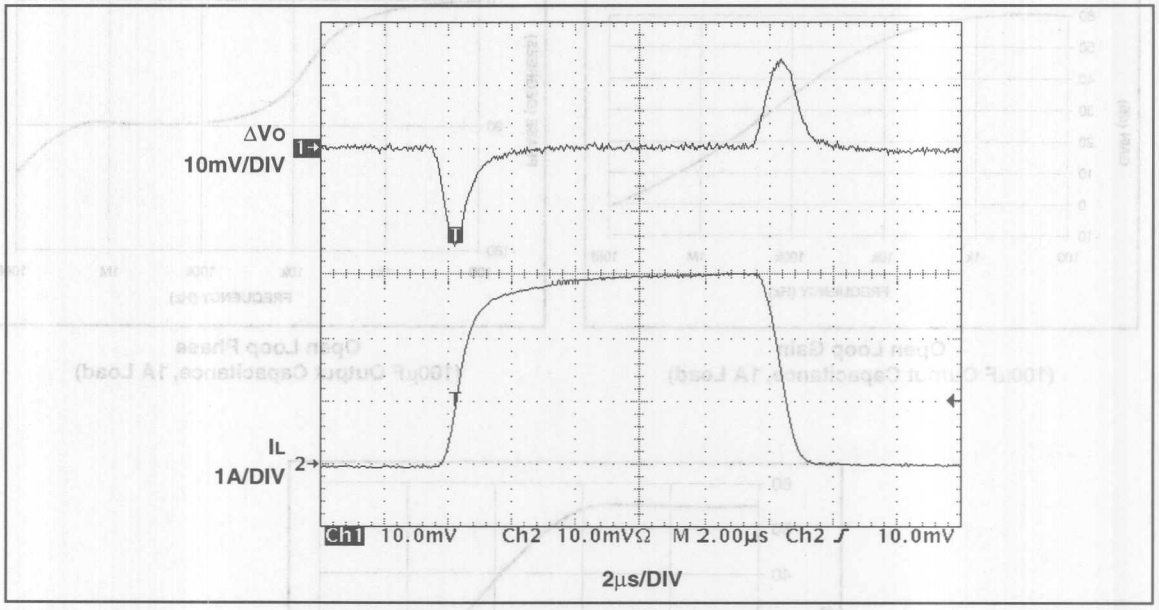
Open Loop Phase
(100μF Output Capacitance, 1A Load)



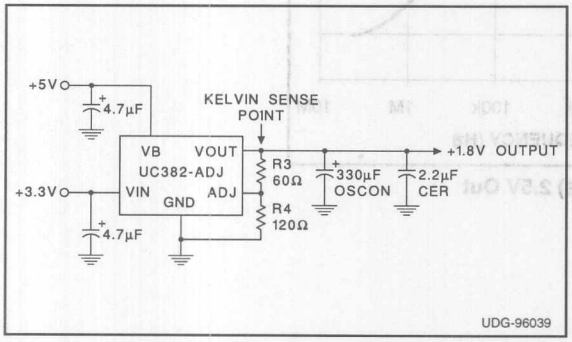
PSRR (V_B) 2.5V Out



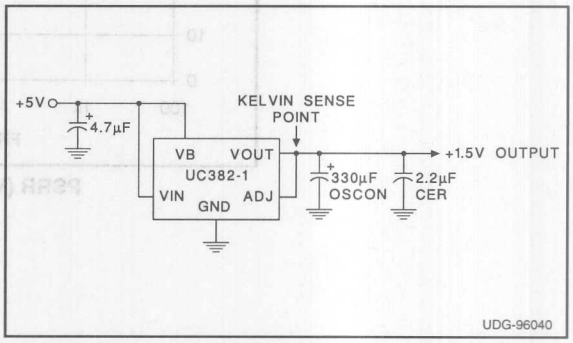
Transient Test Circuit



10mA to 3A/µs Load Transient Response



Typical UC382-ADJ Application



Typical UC382-1, -2, or -3 Application

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Low Dropout 3 Ampere Linear Regulator Family

FEATURES

- Precision Positive Series Pass Voltage Regulation
- 0.45V Dropout at 3A
- 50mV Dropout 10mA
- Quiescent Current Under 400µA Irrespective of Load
- Adjustable (5 Lead) Output Voltage Version
- Fixed (3 Lead) Versions for 3.3V and 5V Outputs
- Logic Shutdown Capability
- Short Circuit Power Limit of 3% • VIN • ISHORT
- Low VOUT to VIN Reverse Leakage
- Thermal Shutdown

DESCRIPTION

The UCC283-3/-5/-ADJ family of positive linear series pass regulators are tailored for low drop out applications where low quiescent power is important. Fabricated with a BiCMOS technology ideally suited for low input to output differential applications, the UCC283-5 will pass 3A while requiring only 0.45V of typical input voltage headroom (guaranteed 0.6V dropout). These regulators include reverse voltage sensing that prevents current in the reverse direction. Quiescent current is always less than 650µA. These devices have been internally compensated in such a manner that the need for a minimum output capacitor has been eliminated.

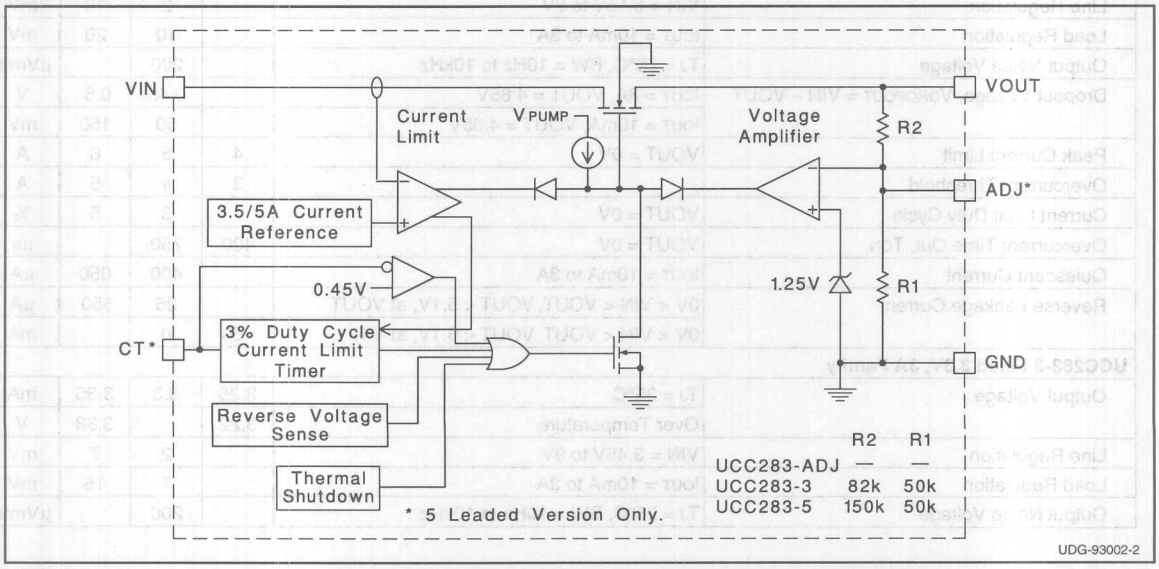
UCC283-3 and UCC283-5 versions are in 3 lead packages and have preset outputs at 3.3V and 5.0V respectively. The output voltage is regulated to 1.5% at room temperature. The UCC283-ADJ version, in a 5 lead package, regulates the output voltage programmed by an external resistor ratio.

Short circuit current is internally limited. The device responds to a sustained overcurrent condition by turning off after a TON delay. The device then stays off for a period, TOFF, that is 32 times the TON delay. The device then begins pulsing on and off at the TON/(TON+TOFF) duty cycle of 3%. This drastically reduces the power dissipation during short circuit and means heat sinks need only accommodate normal operation. On the 3 leaded versions of the device TON is fixed at 750µs, on the adjustable 5 leaded versions an external capacitor sets the on time -- the off time is always 32 times TON. The external timing control pin, CT, on the five leaded versions also serves as a shutdown input when pulled low.

Internal power dissipation is further controlled with thermal overload protection circuitry. Thermal shutdown occurs if the junction temperature exceeds 165°C. The chip will remain off until the temperature has dropped 20°C.

The UCC283 series is specified for operation over the industrial range of –40°C to +85°C, and the UCC383 series is specified from 0°C to +70°C. These devices are available in 3 and 5 pin TO-220 and TO-263 power packages.

BLOCK DIAGRAM



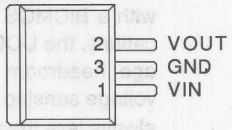
ABSOLUTE MAXIMUM RATINGS

VIN 9V
CT ..... –0.3 to 3V
ADJ ..... –0.3 to 9V
Storage Temperature ..... –65°C to +150°C
Junction Temperature ..... –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

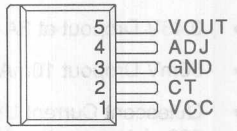
Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages. All voltages are referenced to GND.

CONNECTION DIAGRAMS

3-PIN TO-263 (Front View) TD Package

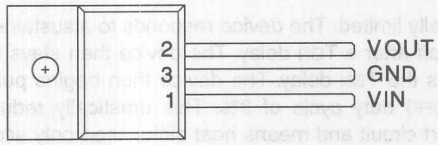


5-PIN TO-263 (Front View) TD Package



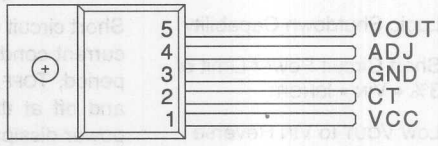
See Note 1

3-PIN TO-220 (Front View) T Package



See Note 1

5-PIN TO-220 (Front View) T Package



See Note 1

NOTE 1: Tab = GND

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications hold for T_A = 0°C to 70°C for the UCC383-X series, –40°C to +85°C for the UCC283-X, VIN = VOUT + 1.5V, I_{OUT} = 10mA, C_{IN} = 10µF, C_{OUT} = 22µF, CT = 1500pF for the UCC283-ADJ, T_J = T_A.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
UCC283-5 Fixed 5V, 3A Family					
Output Voltage	T_J = 25°C	4.925	5	5.075	V
	Over Temperature	4.875		5.125	V
Line Regulation	VIN = 5.15V to 9V		2	10	mV
Load Regulation	I_{OUT} = 10mA to 3A		10	20	mV
Output Noise Voltage	T_J = 25°C, BW = 10Hz to 10kHz		200		µVrms
Dropout Voltage, $V_{DROPOUT}$ = VIN – VOUT	I_{OUT} = 3A, VOUT = 4.85V		0.45	0.6	V
	I_{OUT} = 10mA, VOUT = 4.85V		50	150	mV
Peak Current Limit	VOUT = 0V	4	5	6	A
Overcurrent Threshold		3	4	5	A
Current Limit Duty Cycle	VOUT = 0V		3	5	%
Overcurrent Time Out, T_{ON}	VOUT = 0V	400	750		µs
Quiescent Current	I_{OUT} = 10mA to 3A		400	650	µA
Reverse Leakage Current	0V < VIN < VOUT, VOUT < 5.1V, at VOUT		25	650	µA
	0V < VIN < VOUT, VOUT < 5.1V, at VIN	–50	0		mA
UCC283-3 Fixed 3.3V, 3A Family					
Output Voltage	T_J = 25°C	3.25	3.3	3.35	mA
	Over Temperature	3.22		3.38	V
Line Regulation	VIN = 3.45V to 9V		2	7	mV
Load Regulation	I_{OUT} = 10mA to 3A		7	15	mV
Output Noise Voltage	T_J = 25°C, BW = 10Hz to 10kHz		200		µVrms

ELECTRICAL CHARACTERISTICS (cont.): Unless otherwise stated, these specifications hold for T_A = 0°C to 70°C for the UCC383-X series, -40°C to +85°C for the UCC283-X, VIN = VOUT + 1.5V, I_{OUT} = 10mA, C_{IN} = 10µF, C_{OUT} = 22µF, CT = 1500pF for the UCC283-ADJ, $T_J = T_A$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
UCC283-3 Fixed 3.3V, 3A Family (cont.)					
Dropout Voltage, $V_{DROPOUT}$ = VIN – VOUT	I_{OUT} = 3A, VOUT = 3.15V		0.7	1	V
	I_{OUT} = 1.5A, VOUT = 3.15V		0.45	0.6	V
	I_{OUT} = 10mA, VOUT = 3.15V		50	150	mV
Peak Current Limit	VOUT = 0V	4	5	6	A
Overcurrent Threshold		3	4	5	A
Current Limit Duty Cycle	VOUT = 0V		3	5	%
Overcurrent Time Out, T_{ON}	VOUT = 0V	400	750		µs
Quiescent Current	I_{OUT} = 10mA to 3A		400	650	µA
Reverse Leakage Current	0V < VIN < VOUT, VOUT < 3.35V, at VOUT		25	650	µA
	0V < VIN < VOUT, VOUT < 3.35V, at VIN	–50	0		mA
UCC283-ADJ Adjustable Output, 3A Family					
Regulating Voltage at ADJ Pin	T_J = 25°C	1.23	1.25	1.27	mA
	Over Temperature	1.22		1.28	V
Line Regulation, at ADJ Input	VIN = VOUT + 150mV to 9V		1	3	mV
Load Regulation, at ADJ Input	I_{OUT} = 10mA to 3A		2	5	mV
Output Noise Voltage	T_J = 25°C, BW = 10Hz to 10kHz		200		µVrms
Dropout Voltage, $V_{DROPOUT}$ = VIN – VOUT	VIN > 4V, I_{OUT} = 3A		0.45	0.6	V
	VIN > 3V, I_{OUT} = 1.5A		0.45	0.6	V
	VIN > 3V, I_{OUT} = 10mA		50	150	mV
Peak Current Limit	VOUT = 0V, VIN = 6.5V	4	5	6	A
Overcurrent Threshold	VIN = 6.5V	3	4	5	A
Current Limit Duty Cycle	VOUT = 0V		3	5	%
Overcurrent Time Out, T_{ON}	VOUT = 0V, CT = 1500pF		750		µs
Reverse Leakage Current	0V < VIN < VOUT, VOUT < 9V, at VOUT		25	650	µA
	0V < VIN < VOUT, VOUT < 9V, at VIN	–50	0		mA
Bias current at ADJ Input			100	250	nA
Quiescent Current	I_{OUT} = 10mA to 3A		400	650	µA
Shutdown Threshold	At CT Input	0.25	0.45		V
Quiescent Current in Shutdown	VIN = 10V		10	25	µA

PIN DESCRIPTIONS

ADJ: Adjust pin for the UCC283-ADJ version only. Feedback pin for the linear regulator. Program the output voltage with R1 connected from ADJ to GND and R2 connected from VOUT to ADJ. Output voltage is given by:

$$VOUT = \frac{1.25V \bullet (R1 + R2)}{R1}$$

CT: Short circuit timing capacitor and shutdown input for the UCC283-ADJ version. Pulling CT below 0.25V turns off the regulator and places it in a low quiescent current mode. A timing capacitor, C, from CT to GND programs the duration of the pulsed short circuit on-time. On-time, T_{ON}, is approximately given by: T_{ON} = 500k • C.

GND: Reference ground.

VIN: Input voltage, This pin must be bypassed with a low ESL/ESR 1µF or larger capacitor to GND. VIN can range from (VOUT + $V_{DROPOUT}$) to 9V. If VIN is reduced to zero while VOUT is held high, the reverse leakage from VOUT to VIN is less than 50µA.

VOUT: Regulated output voltage. A bypass capacitor is not required at VOUT, but may be desired for good transient response. The bypass capacitor must not exceed a maximum value in order to insure the regulator can start. At startup, the bypass capacitor appears as a short circuit to the regulator. The combination of the minimum value of

PIN DESCRIPTIONS (cont.)

the peak current limit less the current taken by the load must be sufficient to charge the bypass capacitor in less than TON (the pulse width of the short circuit current). Otherwise the UCC283 will not start.

If the load is resistive, the minimum value of the bypass capacitor, COUT, is:

$$COUT < \frac{TON}{RL \bullet \ln \bullet \left(\frac{4A \bullet RL}{VOUT}\right)}$$

If the load behaves as a current source, IL, with zero volt compliance, then COUT can be no larger than:

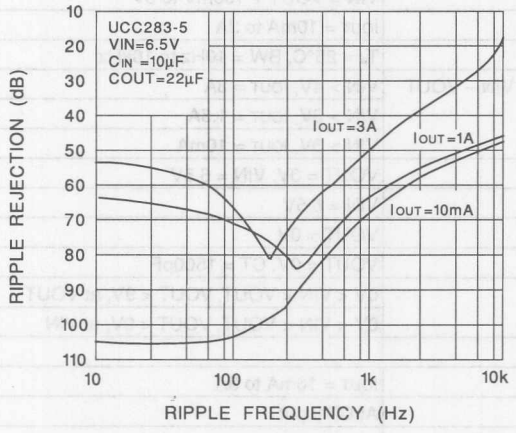
$$COUT < \frac{(4A - IL) \bullet TON}{VOUT}$$

If VOUT is shorted to GND, the regulator delivers peak current pulses with a width of TON at a 3% typical duty cycle. In most cases, under short circuit conditions the short circuit power dissipation is less than the nominal power dissipation under normal conditions. During the short circuit, the average power dissipation is given by:

$$PD \text{ (short circuit)} = VIN \bullet IPEAK \bullet \text{Duty Cycle}$$

For worst case values of 9V, 6A, and 5%, PD(short circuit) = 2.7W.

Ripple Rejection vs. Frequency



UDG-94093

ORDERING INFORMATION

UCC□83□-□
- Output Voltage
- Package
- Temperature Range

Temperature Range	Package	Output Voltage
2: –40°C to +85°C	T: TO-220	3: 3.3V
3: 0°C to +70°C	TD: TO-263	5: 5V
		ADJ: Adjustable

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Universal Serial Bus Power Controller

FEATURES

- Fully USB Compliant
- Support Four 5V Peripherals and One USB 3.3V Controller
- Separate Power Enables
- 500mA Current Limiting per Channel
- Separate Open Drain Fault Indicator for Each Channel
- 3.3V Output for USB Controller
- Available in 28 Pin Wide Surface Mount and DIP

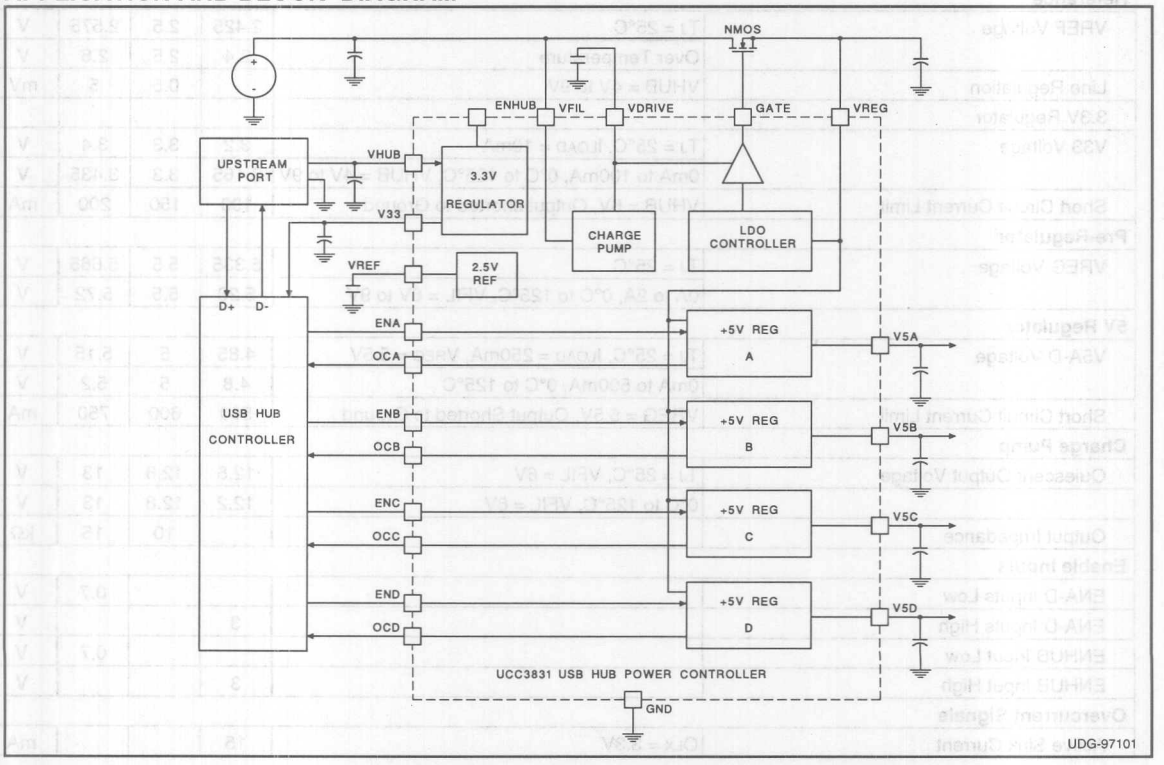
DESCRIPTION

The UCC3831 Power Controller is designed to provide a self powered USB hub with a local 3.3V regulated voltage as well as four 5V regulated voltages for USB ports. Each of the 5V output ports is individually enabled for optimal port control. Each port also provides an overcurrent fault signal indicating that the port has exceeded a 500mA current limit. The 3.3V linear regulator is used to provide power to the local USB microcontroller. This regulator is protected with a 100mA current limit and has a logic level enable input.

The UCC3831 can be configured to provide USB port power from a loosely regulated voltage such as a Filament voltage internal to a monitor. Pre-regulation is provided by an internal linear regulator controller and one external N-channel MOSFET. The UCC3831 can also be configured without a using the pre-regulator stage by connecting the VREG pins to a regulated 5.5V 2A source.

The UCC3831 comes in a 28-pin wide SOIC power package optimized for power dissipation, and is protected by internal over-temperature shutdown mechanism, which disables the outputs should the internal junction temperature exceed 150°C.

APPLICATION AND BLOCK DIAGRAM



3/97

ABSOLUTE MAXIMUM RATINGS

VFIL 9V
VCON Supply Votage 9V
Logic Inputs (ENA-D, ENHUB)
  Maximum Forced Voltage ..... –0.3V to 7V
  Maximum Forced Current ..... ±1mA
V33
  Maximum Forced Voltage 5V
  Maximum Current 200mA
V5A-D
  Maximum Voltage 9V
  Maximum Current 750mA
Storage Temperature ..... –65°C to +150°C
Junction Temperature ..... –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

Unless otherwise indicated, voltages are reference to ground. Pulsed is defined as a less than 10% duty cycle with a maximum duration of 500µS. Currents are positive into, negative out of the specified terminal. All voltages are with respect to ground. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

ELECTRICAL CHARACTERISTICS Unless otherwise specified, T_J = 0°C to 125°C for the UCC3831. VFIL = 6.5V, VHUB = 5V. $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply Currents					
VHUB Supply Current	No External Load on V33		1	3	mA
VFIL Supply Current			1	3	mA
Reference					
VREF Voltage	T_J = 25°C	2.425	2.5	2.575	V
	Over Temperature	2.4	2.5	2.6	V
Line Regulation	VHUB = 4V to 9V		0.5	5	mV
3.3V Regulator					
V33 Voltage	T_J = 25°C, I_{LOAD} = 10mA	3.2	3.3	3.4	V
	0mA to 100mA, 0°C to 125°C, VHUB = 4V to 9V	3.165	3.3	3.435	V
Short Circuit Current Limit	VHUB = 6V, Output shorted to Ground	100	150	200	mA
Pre-Regulator					
VREG Voltage	T_J = 25°C	5.335	5.5	5.665	V
	0A to 2A, 0°C to 125°C, VFIL = 6V to 9V	5.28	5.5	5.72	V
5V Regulator					
V5A-D Voltage	T_J = 25°C, I_{LOAD} = 250mA, V_{REG} = 5.5V	4.85	5	5.15	V
	0mA to 500mA, 0°C to 125°C	4.8	5	5.2	V
Short Circuit Current Limit	VREG = 5.5V, Output Shorted to Ground	500	600	750	mA
Charge Pump					
Quiescent Output Voltage	T_J = 25°C, VFIL = 6V	12.5	12.8	13	V
	0°C to 125°C, VFIL = 6V	12.2	12.8	13	V
Output Impedance			10	15	kΩ
Enable Inputs					
ENA-D Inputs Low				0.7	V
ENA-D Inputs High		3			V
ENHUB Input Low				0.7	V
ENHUB Input High		3			V
Overcurrent Signals					
Active Sink Current	O_{LX} = 3.3V	15			mA

PIN DESCRIPTIONS

ENA-D: Separate enables pins for each of the four 5V supplies.

ENHUB: Enables the 3.3V output V33. Pulling this pin low disables V33.

GATE: Gate drive for an external NMOS used to regulate the 5.5V VREG supply. Minimum available drive is 11V.

GND: All 6 GND pins must be tied to the system ground. In addition to serving as electrical conductors, these 6 pins are heat sinks. Refer to the Packaging Device Temperature Management guide in the Packaging section of the Unitrode Databook.

OCA-D: Open drain overcurrent indicator with an internal 40µA current source pull-up to V33. Active low capable of sinking 1mA with $V_{OL MAX}$ = 500mV. OCA-D can be wire OR'ed by the user to create a single overcurrent indicator.

V5A-D: 5V regulated output with enable, 500mA (minimum) current limit, and overcurrent indicator.

V33: 3.3V regulator output. Enable when ENHUB is high. Current limit is 100mA minimum.

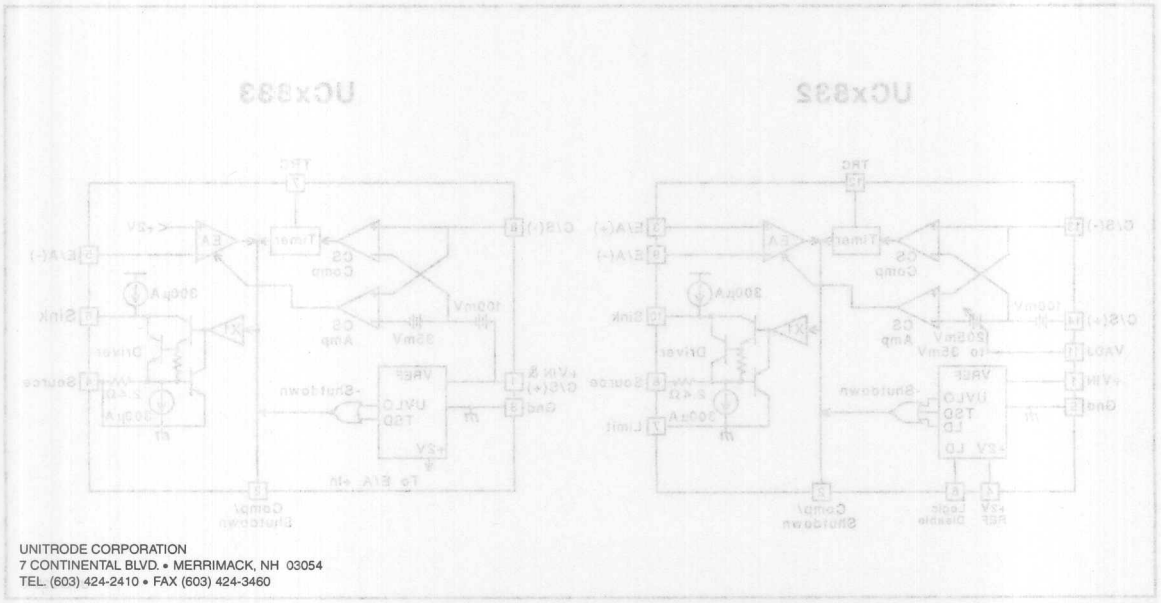
VDRIVE: Internal charge pump voltage is brought out for external decoupling. Nominal voltage is between 11V and 13V. No external loading permitting. Decouple with at least 0.001µF capacitor.

VFIL: Bias supply for all four of the 5V regulators. VFIL voltage must be between 6V and 9V.

VHUB: Supply for the 3.3V USB controller power supply and bandgap reference.

VREF: Internal 2.5V reference is brought out for external decoupling only. Decouple with 0.01µF capacitor.

VREG: Regulated to 5.5V by means of an external NMOS. 2 pins supply up to a total of 2.5A to the four 5V bus voltages (V5A, V5B, V5C, V5D).



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Precision Low Dropout Linear Controllers

FEATURES

- Precision 1% Reference
- Over-Current Sense Threshold Accurate to 5%
- Programmable Duty-Ratio Over-Current Protection
- 4.5V to 36V Operation
- 100mA Output Drive, Source or Sink
- Under-Voltage Lockout

Additional Features of the UC1832 series:

- Adjustable Current Limit to Current Sense Ratio
- Separate +VIN terminal
- Programmable Driver Current Limit
- Access to V_{REF} and E/A(+)
- Logic-Level Disable Input

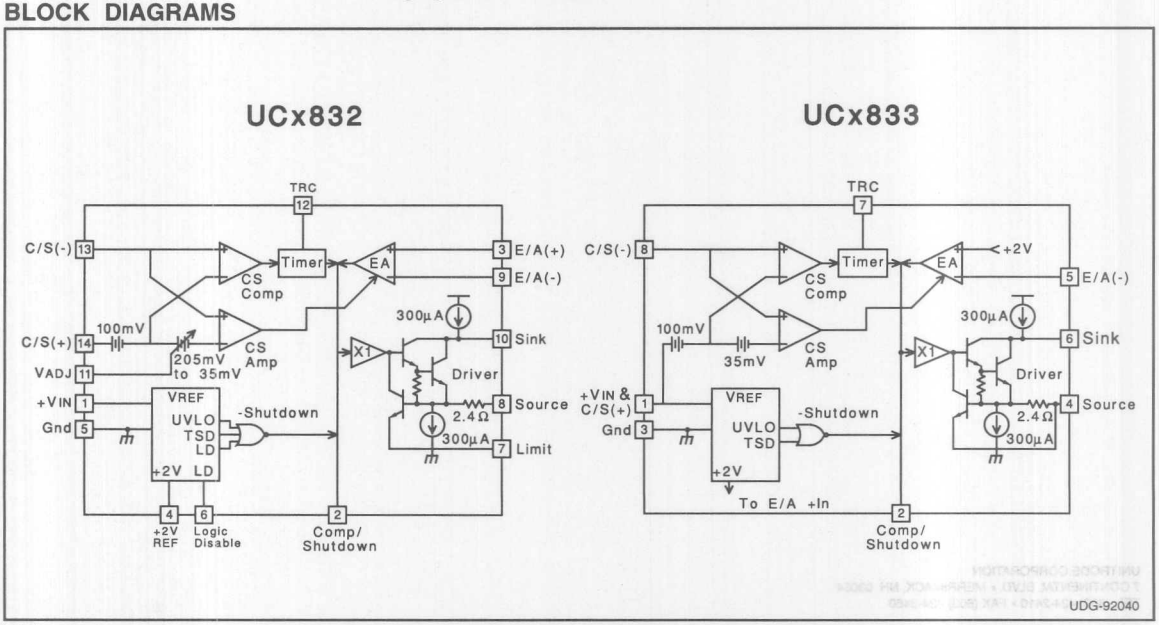
DESCRIPTION

The UC1832 and UC1833 series of precision linear regulators include all the control functions required in the design of very low dropout linear regulators. Additionally, they feature an innovative duty-ratio current limiting technique which provides peak load capability while limiting the average power dissipation of the external pass transistor during fault conditions. When the load current reaches an accurately programmed threshold, a gated-astable timer is enabled, which switches the regulator's pass device off and on at an externally programmable duty-ratio. During the on-time of the pass element, the output current is limited to a value slightly higher than the trip threshold of the duty-ratio timer. The constant-current-limit is programmable on the UCx832 to allow higher peak current during the on-time of the pass device. With duty-ratio control, high initial load demands and short circuit protection may both be accommodated without extra heat sinking or foldback current limiting. Additionally, if the timer pin is grounded, the duty-ratio timer is disabled, and the IC operates in constant-voltage/constant-current regulating mode.

These IC's include a 2 Volt (±1%) reference, error amplifier, UVLO, and a high current driver that has both source and sink outputs, allowing the use of either NPN or PNP external pass transistors. Safe operation is assured by the inclusion of under-voltage lockout (UVLO) and thermal shutdown.

The UC1833 family includes the basic functions of this design in a low-cost, 8-pin mini-dip package, while the UC1832 series provides added versatility with the availability of 14 pins. Packaging options include plastic (N suffix), or ceramic (J suffix). Specified operating temperature ranges are: commercial (0°C to 70°C), order UC3832/3 (N or J); industrial (–25°C to 85°C), order UC2832/3 (N or J); and military (–55°C to 125°C), order UC1832/3J. Surface mount packaging is also available.

BLOCK DIAGRAMS



ABSOLUTE MAXIMUM RATINGS

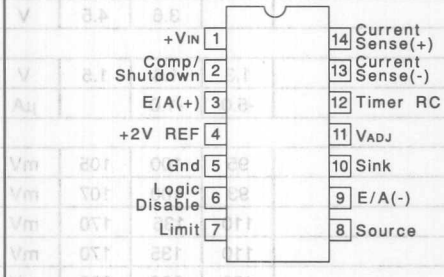
Supply Voltage +VIN 40V
Driver Output Current (Sink or Source) 450mA
Driver Sink to Source Voltage 40V
TRC Pin Voltage . . . . . –0.3V to 3.2V
Other Input Voltages . . . . . –0.3V to +VIN
Operating Junction Temperature (note 2) . . . –55°C to +150°C
Storage Temperature . . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) . . . . . 300°C

Note 1: Unless otherwise indicated, voltages are referenced to ground and currents are positive into, negative out of, the specified terminals.
Note 2: See Unitrode Integrated Circuits databook for information regarding thermal specifications and limitations of packages.

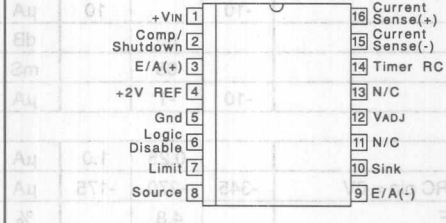
CONNECTION DIAGRAMS

UC1832

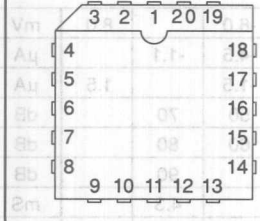
DIL-14 (Top View)
J Or N Package



SOIC-16 (Top View)
DW Package



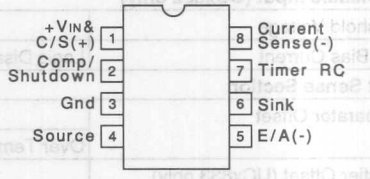
LCC-20 & PLCC-20
L & Q Package
(Top View)



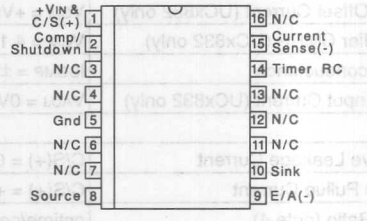
PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
+VIN	2
Comp/Shutdown	3
E/A(+)	4
+2V REF	5
N/C	6
Gnd	7
Logic Disable	8
Limit	9
Source	10
N/C	11
E/A(-)	12
Sink	13
VADJ	14
N/C	15-17
Timer RC	18
Current Sense(-)	19
Current Sense(+)	20

UC1833

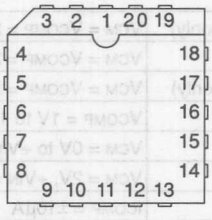
DIL-8 (Top View)
J Or N Package



SOIC-16 (Top View)
DW Package



LCC-20 & PLCC-20
L & Q Package
(Top View)



PACKAGE PIN FUNCTION	
FUNCTION	PIN
+VIN & C/S(+)	1
N/C	2
N/C	3
N/C	4
Comp/Shutdown	5
Gnd	6
N/C	7
N/C	8
N/C	9
Source	10
N/C	11
E/A(-)	12
N/C	13
N/C	14
Sink	15
Timer RC	16
Current Sense(+)	17
N/C	18-20

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, specifications hold for T_A = 0°C to 70°C for the UC3832/3, –25°C to 85°C for the UC2832/3, and –55°C to 125°C for the UC1832/3, $+V_{IN}$ = 15V, Driver sink = $+V_{IN}$, C/S(+) voltage = $+V_{IN}$. T_A=T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply					
Supply Current	$+V_{IN}$ = 6V		6.5	10	mA
	$+V_{IN}$ = 36V		9.5	15	mA
	Logic Disable = 2V (UCx832 only)		3.3		mA
Reference Section					
Output Voltage (Note 3)	T_J = 25°C, I_{DRIVER} = 10mA	1.98	2.00	2.02	V
	over temperature, I_{DRIVER} = 10mA	1.96	2.00	2.04	V
Load Regulation (UCx832 only)	I_{OUT} = 0 to 10mA	-10	-5.0		mV
Line Regulation	$+V_{IN}$ = 4.5 to 36V, I_{DRIVER} = 10mA		0.033	0.5	mV/V
Under-Voltage Lockout Threshold			3.6	4.5	V
Logic Disable Input (UCx832 only)					
Threshold Voltage		1.3	1.4	1.5	V
Input Bias Current	Logic Disable = 0V	-5.0	-1.0		µA
Current Sense Section					
Comparator Offset		95	100	105	mV
	Over Temperature	93	100	107	mV
Amplifier Offset (UCx833 only)		110	135	170	mV
Amplifier Offset (UCx832 only)	V_{ADJ} = Open	110	135	170	mV
	V_{ADJ} = 1V	180	235	290	mV
	V_{ADJ} = 0V	250	305	360	mV
Input Bias Current	V_{CM} = $+V_{IN}$	65	100	135	µA
Input Offset Current (UCx832 only)	V_{CM} = $+V_{IN}$	-10		10	µA
Amplifier CMRR (UCx832 only)	V_{CM} = 4.1V to $+V_{IN}$+0.3V		80		dB
Transconductance	I_{COMP} = ±100µA		65		mS
V_{ADJ} Input Current (UCx832 only)	V_{ADJ} = 0V	-10	-1		µA
Timer					
Inactive Leakage Current	C/S(+) = C/S(-) = $+V_{IN}$; TRC pin = 2V		0.25	1.0	µA
Active Pullup Current	C/S(+) = $+V_{IN}$, C/S(-) = $+V_{IN}$ - 0.4V; TRC pin = 0V	-345	-270	-175	µA
Duty Ratio (note 4)	ontime/period, R_T = 200k, C_T = 0.27µF		4.8		%
Period (notes 4,5)	ontime + offtime, R_T = 200k, C_T = 0.27µF		36		ms
Upper Trip Threshold (Vu)			1.8		V
Lower Trip Threshold (Vl)			0.9		V
Trip Threshold Ratio	Vu/Vl		2.0		V/V
Error Amplifier					
Input Offset Voltage (UCx832 only)	V_{CM} = V_{COMP} = 2V	-8.0		8.0	mV
Input Bias Current	V_{CM} = V_{COMP} = 2V	-4.5	-1.1		µA
Input Offset Current (UCx832 only)	V_{CM} = V_{COMP} = 2V	-1.5		1.5	µA
AVOL	V_{COMP} = 1V to 13V	50	70		dB
CMRR (UCx832 only)	V_{CM} = 0V to $+V_{IN}$ - 3V	60	80		dB
PSRR (UCx832 only)	V_{CM} = 2V, $+V_{IN}$ = 4.5 to 36V		90		dB
Transconductance	I_{COMP} = ±10µA		4.3		mS
VOH	I_{COMP} = 0, Volts below $+V_{IN}$		.95	1.3	V
VOL	I_{COMP} = 0		.45	0.7	V
IOH	V_{COMP} = 2V	-700	-500	-100	µA

ELECTRICAL CHARACTERISTICS (cont.)

Unless otherwise stated, specifications hold for T_A = 0°C to 70°C for the UC3832/3, –25°C to 85°C for the UC2832/3, and –55°C to 125°C for the UC1832/3, +V_{IN} = 15V, Driver sink = +V_{IN}, C/S(+) voltage = +V_{IN}. T_A=T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Error Amplifier (cont.)					
IOL	V_{COMP} = 2V, C/S(-) = +V_{IN}	100	500	700	µA
	V_{COMP} = 2V, C/S(-) = +V_{IN} - 0.4V	2	6		mA
Driver					
Maximum Current	Driver Limit & Source pins common; T_J = 25°C	200	300	400	mA
	Over Temperature	100	300	450	mA
Limiting Voltage (UCx832 only)	Driver Limit to Source voltage at current limit, I_{SOURCE} = -10mA; T_J = 25°C (Note 6)		.72		V
Internal Current Sense Resistance	T_J = 25°C (Note 6)		2.4		Ω
Pull-Up Current at Driver Sink	Compensation/Shutdown = 0.4V; Driver Sink = +V_{IN} - 1V	-800	-300	-100	µA
	Compensation/Shutdown = 0.4V, +V_{IN} = 36V; Driver Sink = 35V	-1000	-300	-75	µA
Pull-Down Current at Driver Source	Compensation/Shutdown = 0.4V; Driver Source = 1V	150	300	700	µA
Saturation Voltage Sink to Source	Driver Source = 0V; Driver Current = 100mA		1.5		V
Maximum Source Voltage	Driver Sink = +V_{IN}, Driver Current = 100mA Volts below +V_{IN}		3.0		V
UVLO Sink Leakage	+V_{IN} = C/S(+) = C/S(-) = 2.5V, Driver Sink = 15V, Driver Source = 0V, TA = 25°C		25		µA
Maximum Reverse Source Voltage	Compensation/Shutdown = 0V; I_{SOURCE} = 100µA, +V_{IN} = 3V		1.6		V
Thermal Shutdown			160		°C

Note 3: On the UCx833 this voltage is defined as the regulating level at the error amplifier inverting input, with the error amplifier driving V_{SOURCE} to 2V.

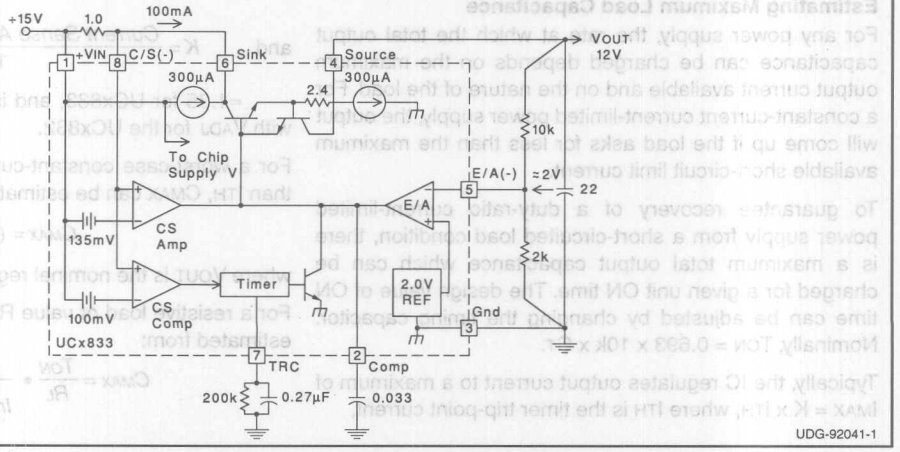
Note 4: These parameters are first-order supply-independent, however both may vary with supply for +V_{IN} less than about 4V. This supply variation will cause a slight change in the timer period and duty cycle, although a high off-time/on-time ratio will be maintained.

Note 5: With recommended R_T value of 200k, $T_{OFF} \approx R_T C_T * \ln(Vu/Vl) \pm 10\%$.

Note 6: The internal current limiting voltage has a temperature dependence of approximately -2.0mV/°C, or -2800ppm/°C. The internal 2.4 Ω sense resistor has a temperature dependance of approximately +1500ppm/°C.

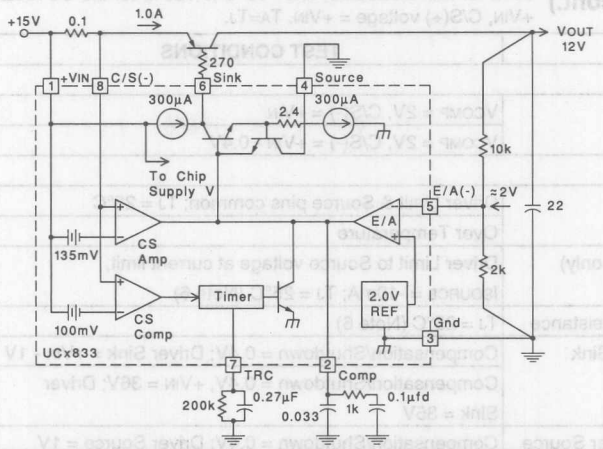
APPLICATION AND OPERATION INFORMATION

NPN Pass (Local 100mA Regulator) (UCx833)



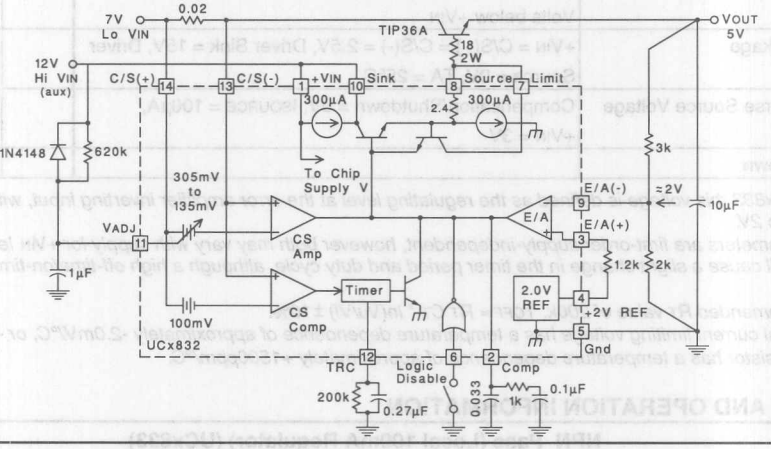
APPLICATION AND OPERATION INFORMATION (cont.)

PNP Pass (Low Drop-Out Regulator) (UCx833)



UDG-92042-1

NPN Pass (Medium Power, Low Drop-Out Regulator) (UCx832)



UDG-92043-1

Estimating Maximum Load Capacitance

For any power supply, the rate at which the total output capacitance can be charged depends on the maximum output current available and on the nature of the load. For a constant-current current-limited power supply, the output will come up if the load asks for less than the maximum available short-circuit limit current.

To guarantee recovery of a duty-ratio current-limited power supply from a short-circuited load condition, there is a maximum total output capacitance which can be charged for a given unit ON time. The design value of ON time can be adjusted by changing the timing capacitor. Nominally, $T_{ON} = 0.693 \times 10k \times C_T$.

Typically, the IC regulates output current to a maximum of $I_{MAX} = K \times I_{TH}$, where I_{TH} is the timer trip-point current,

and $$K = \frac{\textit{Current Sense Amplifier Offset Voltage}}{100mA}$$

≈1.35 for UCx833, and is variable from 1.35 to 3.05 with V_{ADJ} for the UCx832.

For a worst-case constant-current load of value just less than I_{TH}, C_{MAX} can be estimated from:

$$C_{MAX} = ((K-1)I_{TH})\left(\frac{T_{ON}}{V_{OUT}}\right),$$

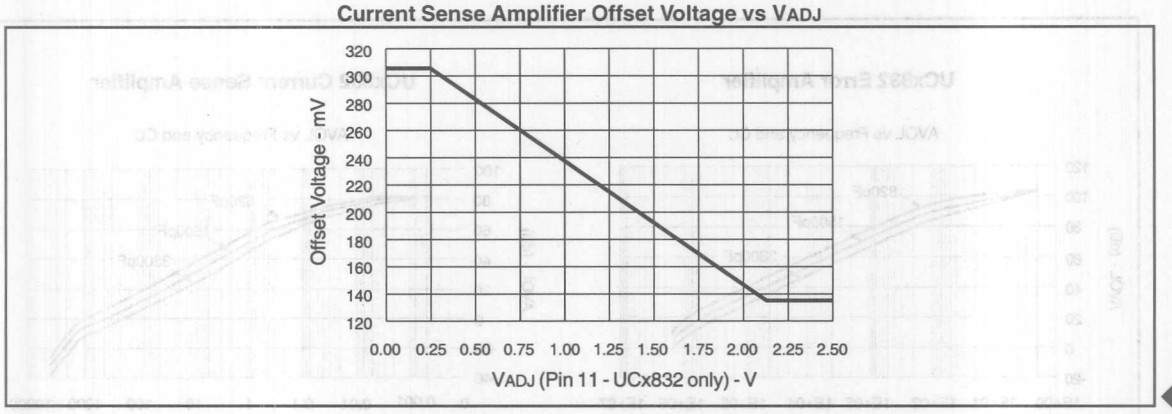
where V_{OUT} is the nominal regulator output voltage.

For a resistive load of value R_L, the value of C_{MAX} can be estimated from:

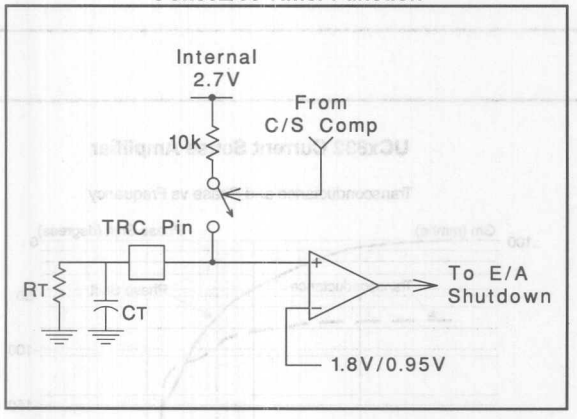
$$C_{MAX} = \frac{T_{ON}}{R_L} \bullet \frac{1}{ln\left[\left(1-\frac{V_{OUT}}{K \bullet I_{TH} \bullet R_L}\right)^{-1}\right]}.$$

APPLICATION AND OPERATION INFORMATION (cont.)

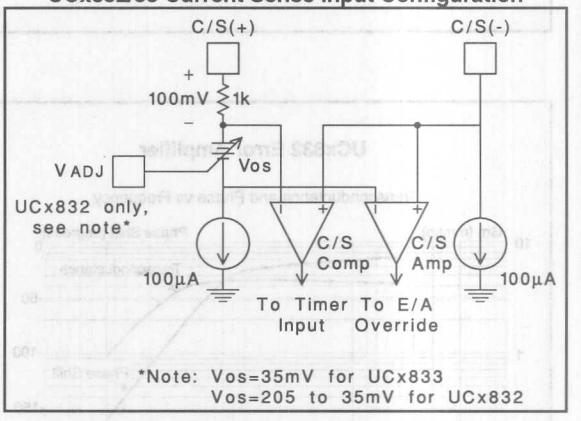
Current Sense Amplifier Offset Voltage vs VADJ



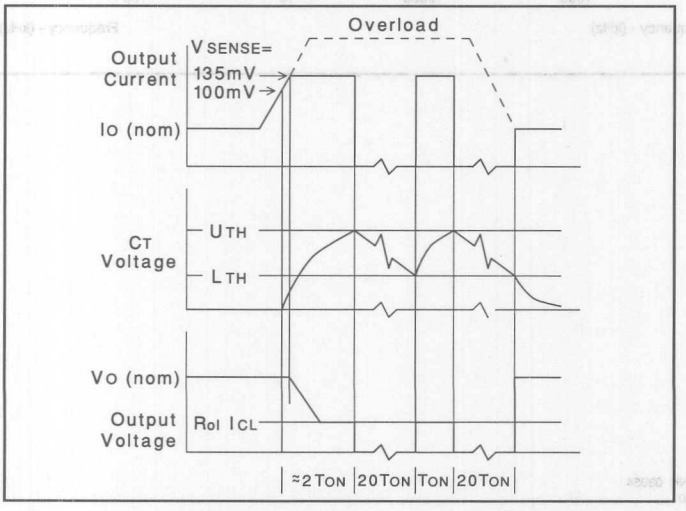
UCx832/33 Timer Function



UCx832/33 Current Sense Input Configuration

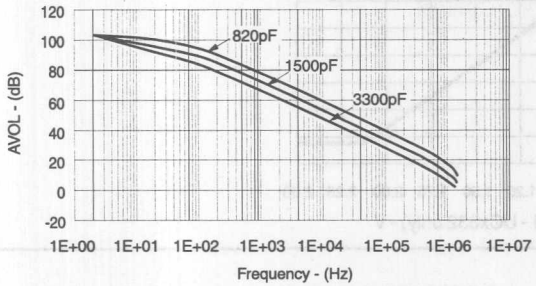


Load current, timing capacitor voltage, and output voltage of the regulator under fault conditions.



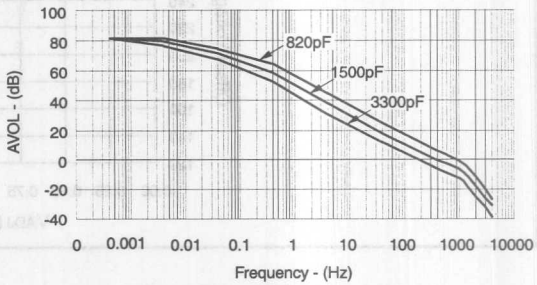
UCx832 Error Amplifier

AVOL vs Frequency and Cc



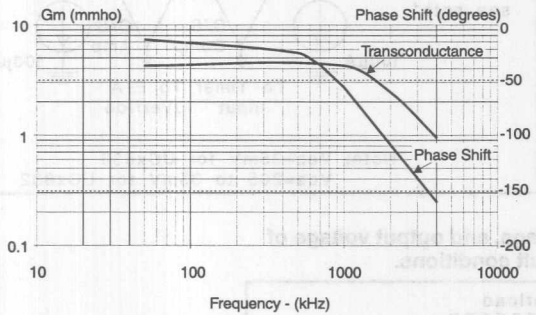
UCx832 Current Sense Amplifier

AVOL vs Frequency and Cc



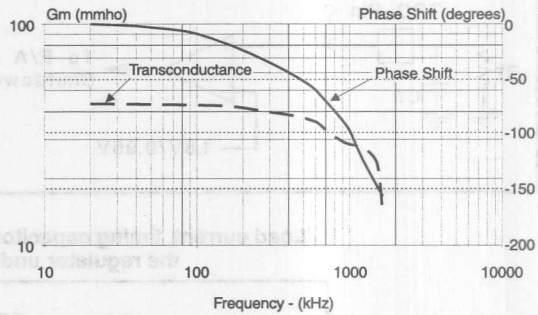
UCx832 Error Amplifier

Transconductance and Phase vs Frequency



UCx832 Current Sense Amplifier

Transconductance and Phase vs Frequency



UNITRODE CORPORATION
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High Efficiency Linear Regulator

FEATURES

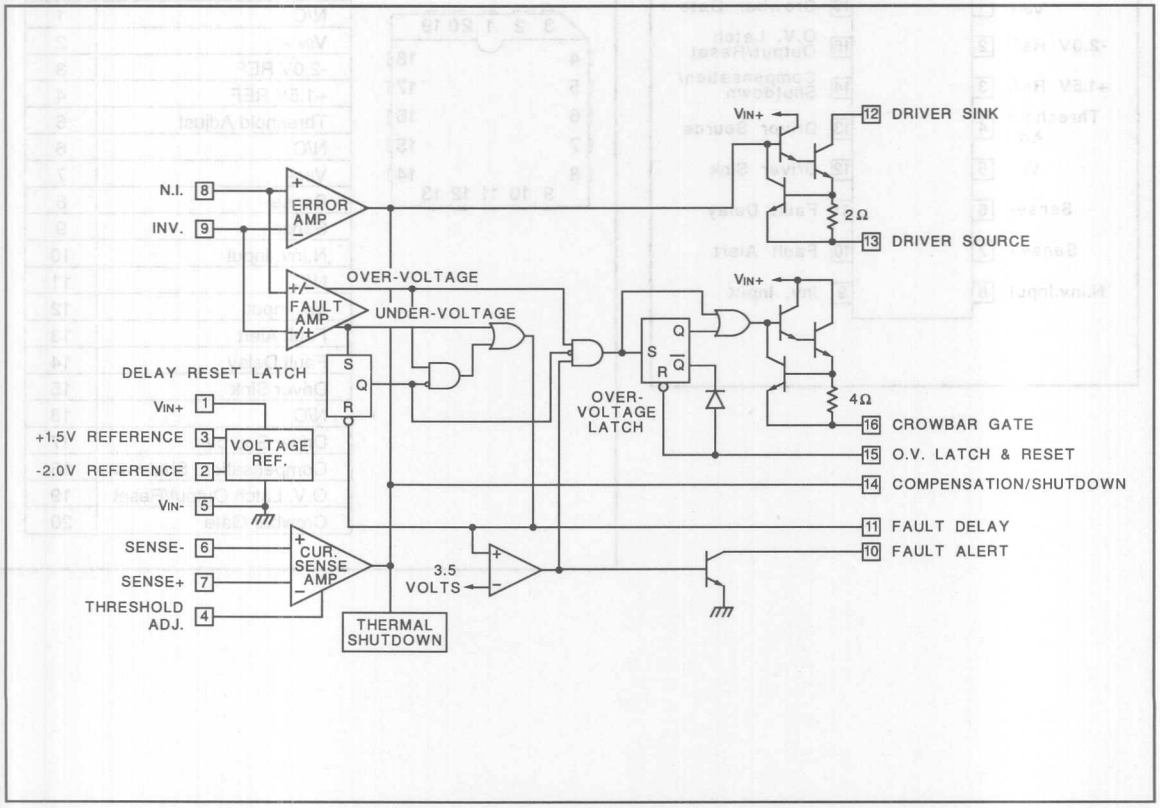
- Minimum VIN - VOUT Less Than 0.5V At 5A Load With External Pass Device
- Equally Usable For Either Positive or Negative Regulator Design
- Adjustable Low Threshold Current Sense Amplifier
- Under And Over-Voltage Fault Alert With Programmable Delay
- Over-Voltage Fault Latch With 100mA Crowbar Drive Output

DESCRIPTION

The UC1834 family of integrated circuits is optimized for the design of low input-output differential linear regulators. A high gain amplifier and 200mA sink or source drive outputs facilitate high output current designs which use an external pass device. With both positive and negative precision references, either polarity of regulator can be implemented. A current sense amplifier with a low, adjustable, threshold can be used to sense and limit currents in either the positive or negative supply lines.

In addition, this series of parts has a fault monitoring circuit which senses both under and over-voltage fault conditions. After a user defined delay for transient rejection, this circuitry provides a fault alert output for either fault condition. In the over-voltage case, a 100mA crowbar output is activated. An over-voltage latch will maintain the crowbar output and can be used to shutdown the driver outputs. System control to the device can be accommodated at a single input which will act as both a supply reset and remote shutdown terminal. These die are protected against excessive power dissipation by an internal thermal shutdown function.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Note 1)

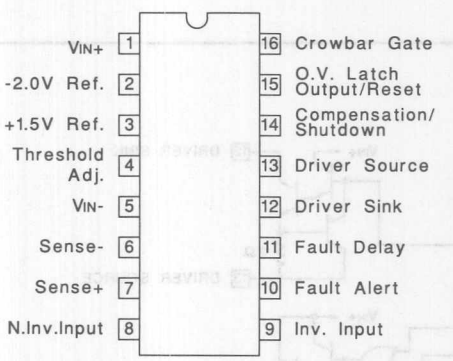
Input Supply Voltage, V_{IN} + ... 40V
Driver Current 400mA
Driver Source to Sink Voltage 40V
Crowbar Current ..... –200mA
+1.5V Reference Output Current ..... –10mA
Fault Alert Voltage 40V
Fault Alert Current 15mA
Error Amplifier Inputs ..... –0.5V to 35V
Current Sense Inputs ..... –0.5V to 40V
O.V. Latch Output Voltage ..... –0.5V to 40V
O.V. Latch Output Current 15mA

Power Dissipation at T_A = 25°C 1000mW
Power Dissipation at Tc = 25°C 2000mW
Operating Junction Temperature ..... –55°C to +150°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (soldering, 10 seconds) ..... 300°C

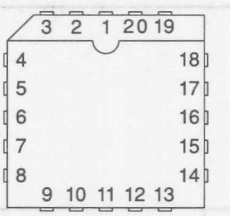
Note 1: Voltages are reference to V_{IN}–, Pin 5.
Currents are positive into, negative out of the specified terminals.
Consult Packaging section of Databook for thermal limitations and considerations of package.

CONNECTION DIAGRAMS

DIL-16, SOIC-16 (TOP VIEW)
J or N Package, DW Package



PLCC-20, LCC-20 (TOP VIEW)
Q, L Packages



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
VIN +	2
-2.0V REF	3
+1.5V REF	4
Threshold Adjust	5
N/C	6
VIN–	7
Sense–	8
Sense+	9
N.Inv. Input	10
N/C	11
Inv. Input	12
Fault Alert	13
Fault Delay	14
Driver Sink	15
N/C	16
Driver Source	17
Compensation/ Shutdown	18
O.V. Latch Output/Reset	19
Crowbar Gate	20

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A=–55°C to +125°C for the UC1834, –40°C to +85°C for the UC2834, and 0°C to +70°C for the

PARAMETER	TEST CONDITIONS	UC1834 UC2834			UC3834			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Turn-on Characteristics								
Standby Supply Current			5.5	7		5.5	10	mA
+1.5 Volt Reference								
Output Voltage	T_J = 25°C	1.485	1.5	1.515	1.47	1.5	1.53	V
	$T_{J(MIN)} \le T_J \le T_{J(MAX)}$	1.47		1.53	1.455		1.545	
Line Regulation	V_{IN+} = 5 to 35V		1	10		1	15	mV
Load Regulation	I_{OUT} = 0 to 2mA		1	10		1	15	mV
-2.0 Volt Reference (Note 2)								
Output Voltage (Referenced to V_{IN}^+)	T_J = 25°C	–2.04	–2	–1.96	–2.06	–2	–1.94	V
	$T_{J(MIN)} \le T_J \le T_{J(MAX)}$	–2.06		–1.94	–2.08		–1.92	
Line Regulation	V_{IN+} = 5 to 35V		1.5	15		1.5	20	mV
Output Impedance			2.3			2.3		kΩ
Error Amplifier Section								
Input Offset Voltage	V_{CM} = 1.5V		1	6		1	10	mV
Input Bias Current	V_{CM} = 1.5V		–1	–4		–1	–8	µA
Input Offset Current	V_{CM} = 1.5V		0.1	1		0.1	2	µA
Small Signal Open Loop Gain	Output @ Pin 14, Pin 12 = V_{IN+} Pin 13, 20Ω to V_{IN-}	50	65		50	65		dB
CMRR	V_{CM} = 0.5 to 33V, V_{IN+} = 35V	60	80		60	80		dB
PSRR	V_{IN+} = 5 to 35V, V_{CM} = 1.5V	70	100		70	100		dB
Driver Section								
Maximum Output Current		200	350		200	350		mA
Saturation Voltage	I_{OUT} = 100mA		0.5	1.2		0.5	1.5	V
Output Leakage Current	Pin 12 = 35V, Pin 13 = V_{IN-}, Pin 14 = V_{IN-}		0.1	50		0.1	50	µA
Shutdown Input Voltage at Pin 14	$I_{OUT} \le$ 100µA, Pin 13 = V_{IN-}, Pin 12 = V_{IN+}	0.4	1		0.4	1		V
Shutdown Input Current at Pin 14	Pin 14 = V_{IN-}, Pin 12 = V_{IN+} $I_{OUT} \le$ 100µA, Pin 13 = V_{IN-}		–100	–150		–100	–150	µA
Thermal Shutdown (Note 3)			165			165		°C
Fault Amplifier Section								
Under- and Over-Voltage Fault Threshold	V_{CM} = 1.5V, @ E/A Inputs	120	150	180	110	150	190	mV
Common Mode Sensitivity	V_{IN+} = 35V, V_{CM} = 1.5 to 33V		–0.4	–0.8		–0.4	–1.0	%/v
Supply Sensitivity	V_{CM} = 1.5V, V_{IN+} = 5 to 35V		–0.5	–1.0		–0.5	–1.2	%/V
Fault Delay		30	45	60	30	45	60	ms/µF
Fault Alert Output Current		2	5		2	5		mA
Fault Alert Saturation Voltage	I_{OUT} = 1mA		0.2	0.5		0.2	0.5	V
O.V. Latch Output Current		2	4		2	4		mA
O.V. Latch Saturation Voltage	I_{OUT} = 1mA		1.0	1.3		1.0	1.3	V
O.V. Latch Output Reset Voltage		0.3	0.4	0.6	0.3	0.4	0.6	V
Crowbar Gate Current		–100	–175		–100	–175		mA
Crowbar Gate Leakage Current	V_{IN+} = 35V, Pin 16 = V_{IN-}		–0.5	–50		–0.5	–50	µA

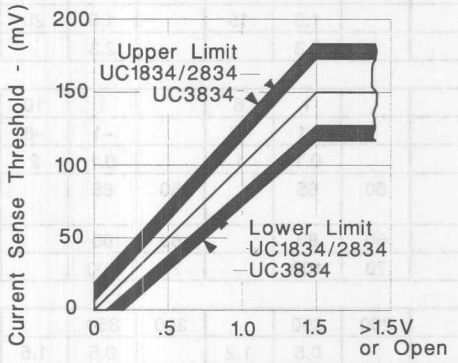
Note 2: When using both the 1.5V and –2.0V references the current out of pin 3 should be balanced by an equivalent current into Pin 2. The –2.0V output will change –2.3mV per µA of imbalance.

Note 3: Thermal shutdown turns off the driver. If Pin 15 (O.V. Latch Output) is tied to Pin 14 (Compensation/Shutdown) the O.V. Latch will be reset.

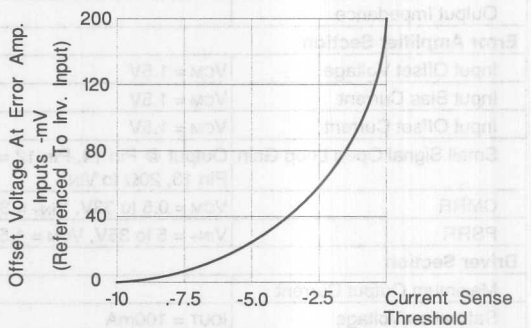
for the UC1834, –40°C to +85°C for the UC2834, and 0°C to +70°C for the

PARAMETER	TEST CONDITIONS	UC1834 UC2834			UC3834			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Current Sense Amplifier Section								
Threshold Voltage	Pin 4 Open, $V_{CM} = V_{IN+}$ or V_{IN-}	130	150	170	120	150	180	mV
	Pin 4 = 0.5V, $V_{CM} = V_{IN+}$ or V_{IN-}	40	50	60	30	50	70	
Threshold Supply Sensitivity	Pin 4 Open, $V_{CM} = V_{IN-}$, V_{IN+} = 5 to 35V		–0.1	–0.3		–0.1	–0.5	%/V
Adj. Input Current	Pin 4 = 0.5V		–2	–10		–2	–10	µA
Sense Input Bias Current	$V_{CM} = V_{IN+}$		100	200		100	200	µA
	$V_{CM} = V_{IN-}$		–100	–200		–100	–200	

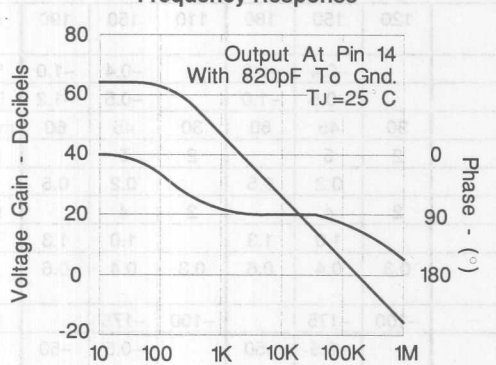
Current Sense Threshold Adjustment



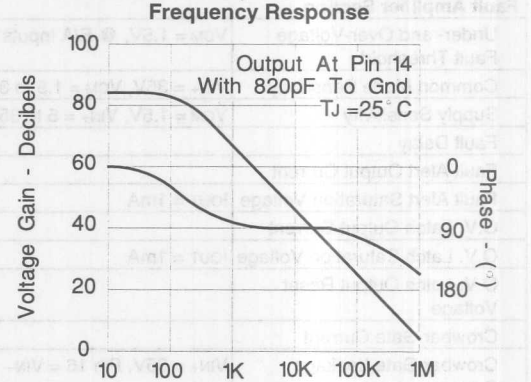
Current Limiting Knee Characteristics



Error Amplifier Gain and Phase Frequency Response

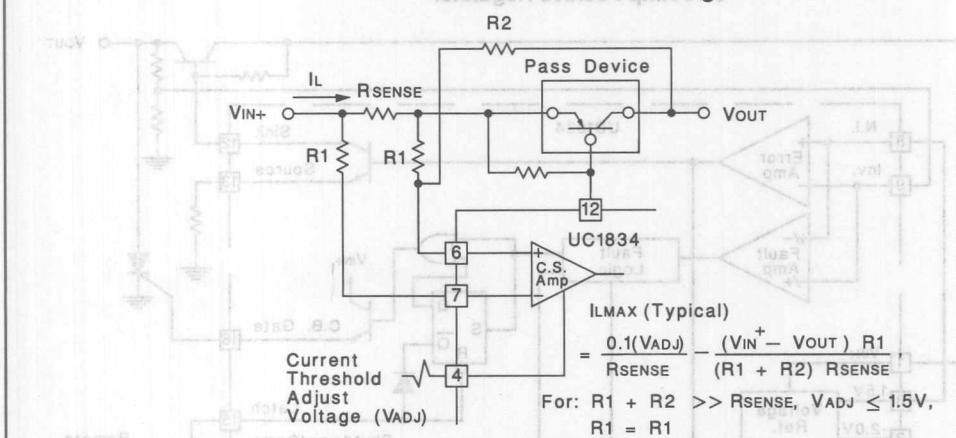


Current Sense Amplifier Gain and Phase Frequency Response



APPLICATION INFORMATION

Foldback Current Limiting



$$I_{LMAX}\ (Typical) = \frac{0.1(V_{ADJ})}{R_{SENSE}} - \frac{(V_{IN}^{+} - V_{OUT})\ R1}{(R1 + R2)\ R_{SENSE}},$$

For: $R1 + R2 >> R_{SENSE}$, $V_{ADJ} \leq 1.5V$, $R1 = R1$

Both the current sense and error amplifiers on the UC1834 are transconductance type amplifiers. As a result, their voltage gain is a direct function of the load impedance at their shared output pin, Pin 14. Their small signal voltage gain as a function of load and frequency is nominally given by;

$$A_{V\ E/A} = \frac{Z_L(f)}{700\Omega} \text{ and } A_{V\ C.S./A} = \frac{Z_L(f)}{70\Omega}$$

for: $f \leq 500kHz$ and $|Z_L(f)| \leq 1\ M\Omega$

Where:

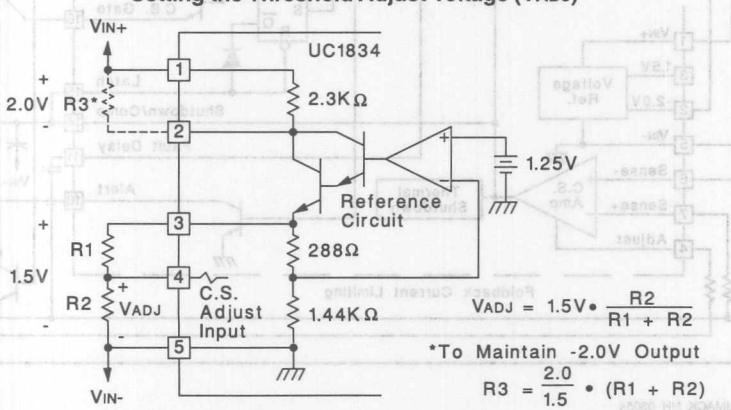
A_V=Small Signal Voltage Gain to pin 14.

$Z_L(f)$ = Load Impedance at Pin 14.

The UC1834 fault delay circuitry prevents the fault outputs from responding to transient fault conditions. The delay reset latch insures that the full, user defined, delay passes before an over-voltage fault response occurs. This prevents unnecessary crowbar, or latched-off conditions, from occurring following sharp under-voltage to over-voltage transients.

The crowbar output on the UC1834 is activated following a sustained over-voltage condition. The crowbar output remains high as long as the fault condition persists, or, as long as the over-voltage latch is set. The latch is set with an over-voltage fault if the voltage at Pin 15 is above the latch reset threshold, typically 0.4V. When the latch is set, its Q– output will pull Pin 15 low through a series diode. As long as a nominal pull-up load exists, the series diode prevents Q– from pulling Pin 15 below the reset threshold. However, Pin 15 is pulled low enough to disable the driver outputs if Pins 15 and 14 are tied together. With Pin 15 and 14 common, the regulator will latch off in response to an over-voltage fault. If the fault condition is cleared and Pins 14 and 15 are momentarily pulled below the latch reset threshold, the driver outputs are re-enabled.

Setting the Threshold Adjust Voltage (V_{ADJ})



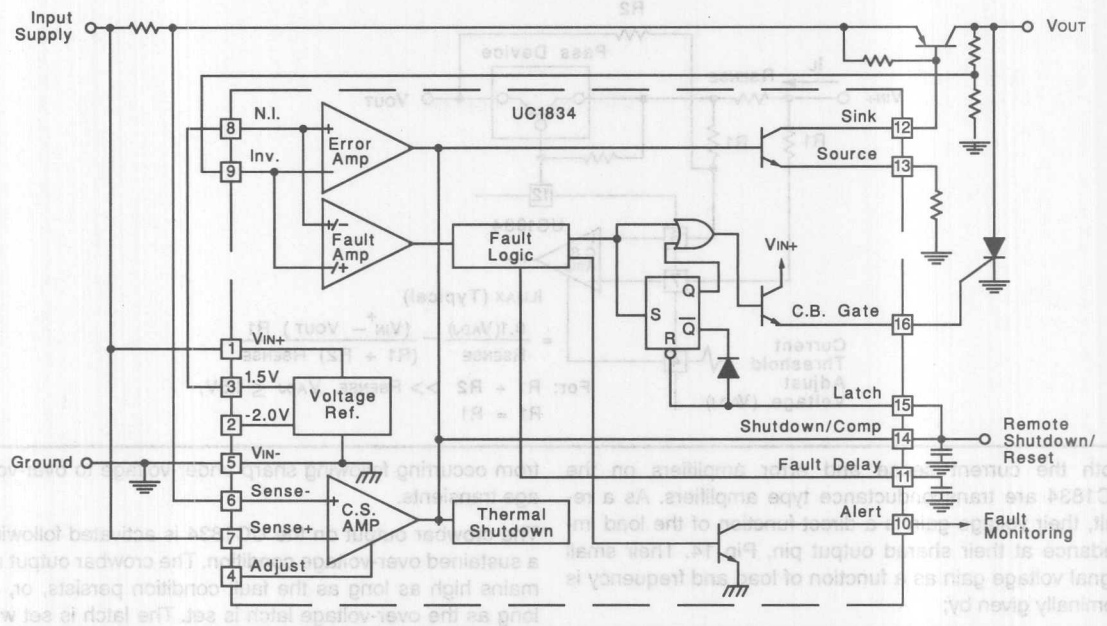
$$V_{ADJ} = 1.5V \bullet \frac{R2}{R1 + R2}$$

*To Maintain -2.0V Output

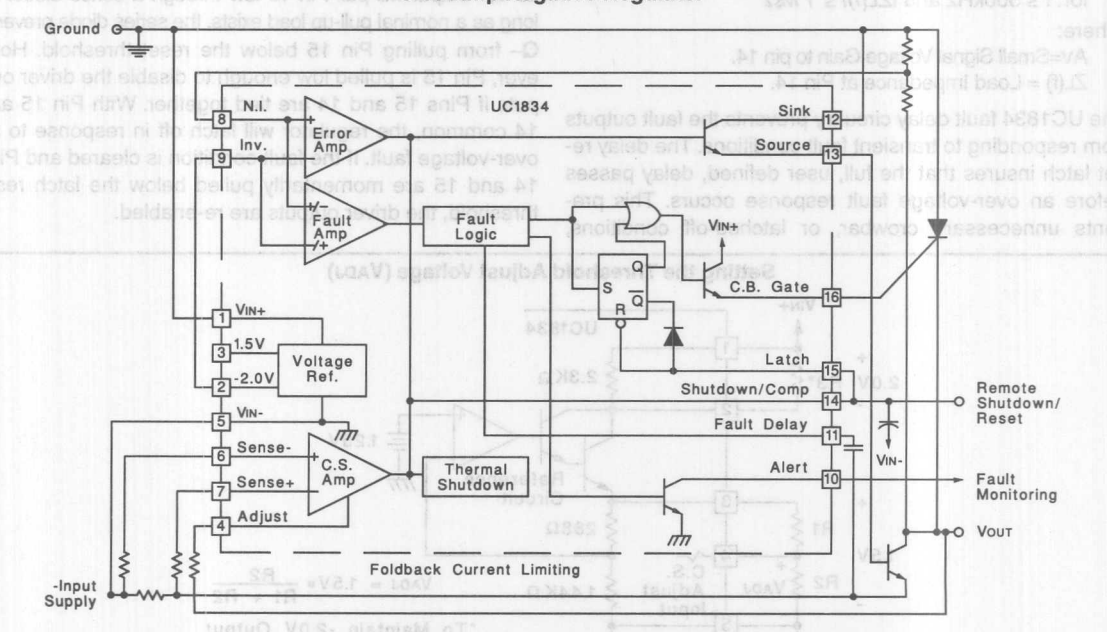
$$R3 = \frac{2.0}{1.5} \bullet (R1 + R2)$$

TYPICAL APPLICATIONS

5-10 Amp Positive Regulator



5-10 Amp Negative Regulator



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High Efficiency Regulator Controller

FEATURES

- Complete Control for a High Current, Low Dropout, Linear Regulator
- Fixed 5V or Adjustable Output Voltage
- Accurate 2.5A Current Limiting with Foldback
- Internal Current Sense Resistor
- Remote Sense for Improved Load Regulation
- External Shutdown
- Under-Voltage Lockout and Reverse Voltage Protection
- Thermal Shutdown Protection
- 8 Pin Mini-Dip Package (Surface Mount also Available)

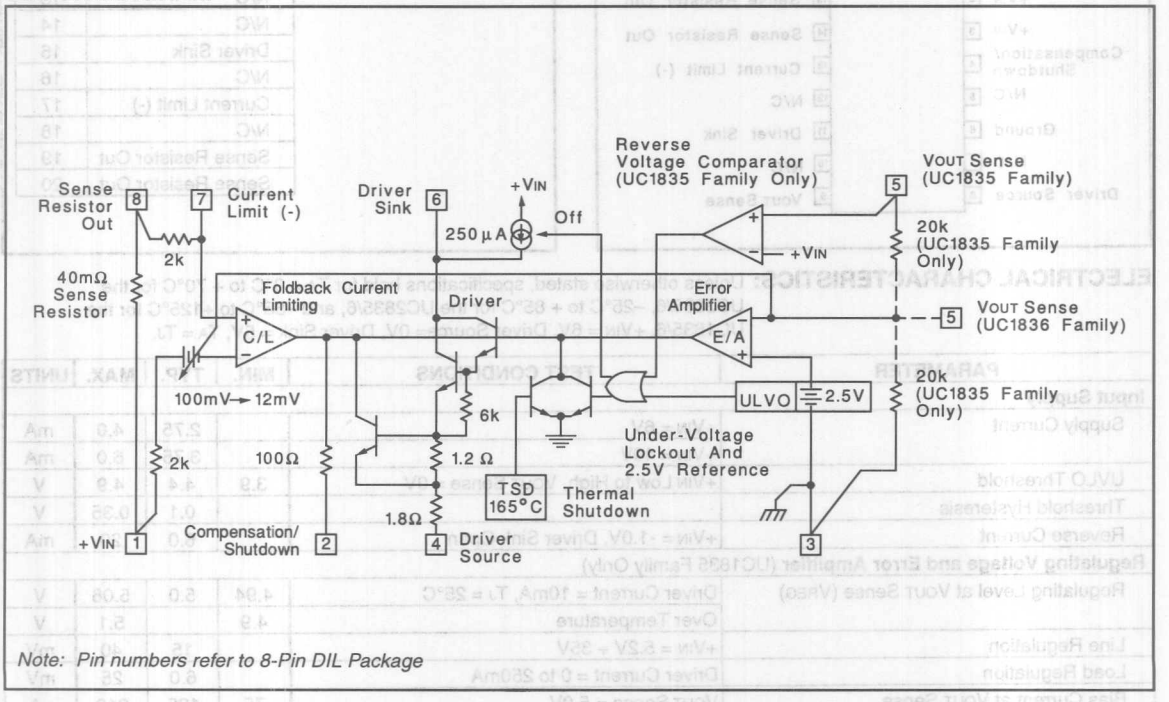
DESCRIPTION

The UC1835/6 families of linear controllers are optimized for the design of low cost, low dropout, linear regulators. Using an external pass element, dropout voltages of less than 0.5V are readily obtained. These devices contain a high gain error amplifier, a 250mA output driver, and a precision reference. In addition, current sense with foldback provides for a 2.5A peak output current dropping to less than 0.5A at short circuit.

These devices are available in fixed, 5V, (UC1835), or adjustable, (UC1836), versions. In the fixed 5 volt version, the only external parts required are an external pass element, an output capacitor, and a compensation capacitor. On the adjustable version the output voltage can be set anywhere from 2.5V to 35V with two external resistors.

Additional features of these devices include under-voltage lockout for predictable start-up, thermal shutdown and short circuit current limiting to protect the driver device. On the fixed voltage version, a reverse voltage comparator minimizes reverse load current in the event of a negative input to output differential.

BLOCK DIAGRAM



Note: Pin numbers refer to 8-Pin DIL Package

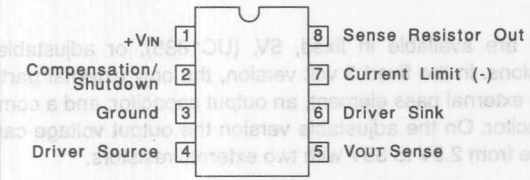
8/94

Driver Output Current (Sink or Source) 600mA
Driver Source to Sink Voltage ..... + 40V
Maximum Current Through Sense Resistor..... 4A
VOUT Sense Input Voltage ..... –.3V to + 40V
Power Dissipation at TA = 25°C (Note 2) 1000mW
Power Dissipation at TC = 25°C (Note 2)..... 2000mW
Storage Temperature..... -65°C to +150°C
Lead Temperature (Soldering, 10 Seconds)..... 300°C

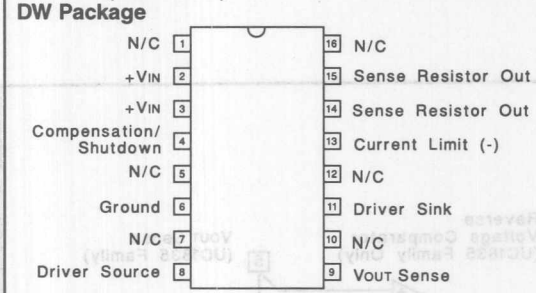
Note 1: Voltages are referenced to ground, (Pin 3). Currents are positive into, negative out of, the specified terminals. Consult Packaging Section of Databook for thermal considerations and limitations of packages.

CONNECTION DIAGRAMS

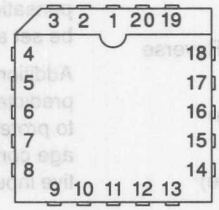
DIL-8, SOIC-8 (TOP VIEW)
N or J Package, D Package



SOIC-16 (TOP VIEW)
DW Package



PLCC-20, LCC-20
(TOP VIEW)
Q, L Packages



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
+VIN	2
+VIN	3
N/C	4
Compensation/ Shutdown	5
N/C	6
Ground	7
N/C	8
N/C	9
Driver Source	10
N/C	11
VOUT Sense	12
N/C	13
N/C	14
Driver Sink	15
N/C	16
Current Limit (-)	17
N/C	18
Sense Resistor Out	19
Sense Resistor Out	20

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, specifications hold for TA = 0°C to + 70°C for the UC3835/6, –25°C to + 85°C for the UC2835/6, and –55°C to +125°C for the UC1835/6, +VIN = 6V, Driver Source= 0V, Driver Sink = 5V, TA = TJ.

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Supply					
Supply Current	+VIN = 6V		2.75	4.0	mA
	+VIN = 40V		3.75	6.0	mA
UVLO Threshold	+VIN Low to High, VOUT Sense = 0V	3.9	4.4	4.9	V
Threshold Hysteresis			0.1	0.35	V
Reverse Current	+VIN = -1.0V, Driver Sink Open		6.0	20	mA
Regulating Voltage and Error Amplifier (UC1835 Family Only)					
Regulating Level at VOUT Sense (VREG)	Driver Current = 10mA, TJ = 25°C	4.94	5.0	5.06	V
	Over Temperature	4.9		5.1	V
Line Regulation	+VIN = 5.2V + 35V		15	40	mV
Load Regulation	Driver Current = 0 to 250mA		6.0	25	mV
Bias Current at VOUT Sense	VOUT Sense = 5.0V	75	125	210	µA
Error Amp Transconductance	±100µA at Compensation/Shutdown Pin	0.8	1.3	2.0	mS
Maximum Compensation Output Current	Sink or Source, Driver Source Open	90	200	260	µA

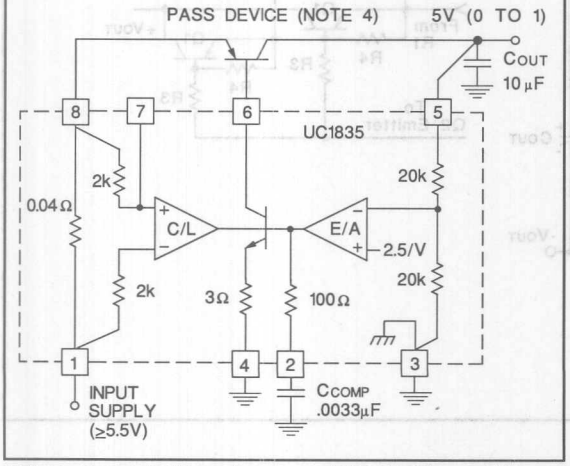
ELECTRICAL CHARACTERISTICS: Unless otherwise stated, specifications hold for T_A = 0°C to + 70°C for the UC3835/6, –25°C to + 85°C for the UC2835/6, and –55°C to +125°C for the UC1835/6, +V_{IN} = 6V, Driver Source= 0V, Driver Sink = 5V, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Regulating Voltage and Error Amplifier (UC1836 Family Only)					
Regulating Level at V_{OUT} Sense (V_{REG})	Driver Current = 10mA, T_J = 25°C	2.47	2.5	2.53	V
	Over Temperature	2.45		2.55	V
Line Regulation	+V_{IN} = 5.2V to 35V		6.0	20	mV
Load Regulation	Driver Current = 0 to 250mA		3.0	15	mV
Bias Current at V_{OUT} Sense	V_{OUT} Sense =2.5V	-1.0	-0.2		µA
Error Amp Transconductance	±100µA at Compensation/Shutdown Pin	0.8	1.3	2.0	mS
Maximum Compensation Output Current	Sink or Source, Driver Source Open	90	200	260	µA
Driver					
Maximum Current		250	500		mA
Saturation Voltage	Driver Current = 250mA, Driver Sink		2.0	2.8	V
Pull-Up Current at Driver Sink	Compensation/Shutdown=0.45V	140	250	300	µA
Driver Sink Leakage	In UVLO			10	µA
	In Reverse Voltage (UC1835 Family Only)			10	µA
Thermal Shutdown			165		°C
Foldback Current Limit					
Current Limit Levels at Sense Resistor Out	V_{OUT} Sense = (0.99) V_{REG}	2.2	2.5	2.8	A
	V_{OUT} Sense = (0.5) V_{REG}	1.3	1.5	1.7	A
	V_{OUT} Sense = 0V	0.25	0.4	0.55	A
Current Limit Amp Tansconductance	±100µA at Compensation/Shutdown, V_{OUT} Sense = (0.9) V_{REG}	12	24	42	mS
Limiting Voltage at Current Limit (-) (Note 2)	V_{OUT} Sense = (0.9) V_{REG} Volts Below +V_{IN}, T_J = 25°C	80	100	140	mV
Sense Resistor Value (Note 3)	V_{OUT} Sense = (0.9) V_{REG}, I_{OUT} = I_A, T_J = 25°C		40		mΩ

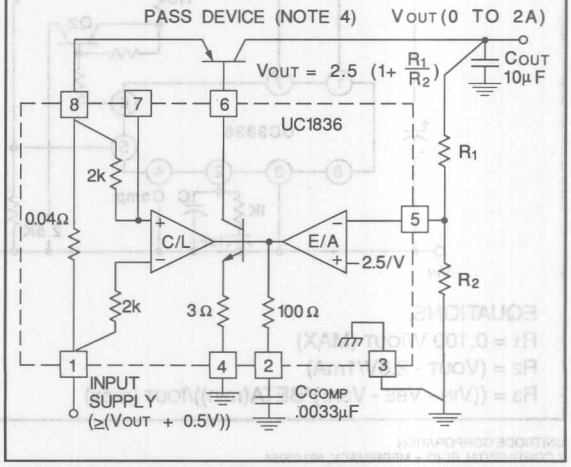
Note 2: This voltage has a positive temperature coefficient of approximately 3500ppm/°C.
Note 3: This resistance has a positive temperature coefficient of approximately 3500ppm/°C. The total resistance from Pin 1 to Pin 8 will include an additional 60 to 100mΩ of package resistance.

APPLICATION AND OPERATION INFORMATION

UC 1835 – Typical configurations for a 2A, Low Dropout 5V Regulator



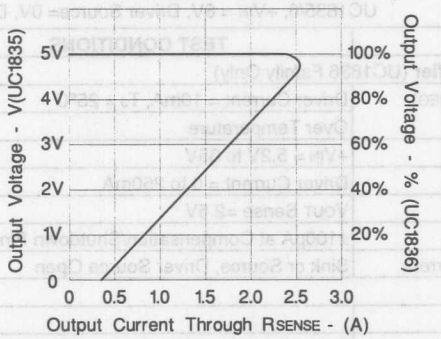
UC1836 – Typical Configuration for a 2A, Low Dropout Adjustable Regulator



Note 4: Suggested Pass devices are TIP 32B. (Dropout Voltage ≤0.75V) or, D45H, (Dropout Voltage ≤0.5V), or equivalents.

APPLICATION AND OPERATION INFORMATION (cont.)

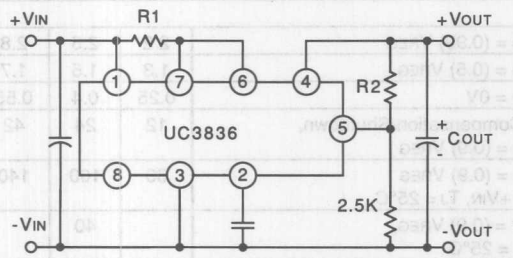
UC1835/6 Foldback Current Limiting



UC3835/36 TYPICAL APPLICATIONS

Low Current Application

using the UC3836 internal drive transistor



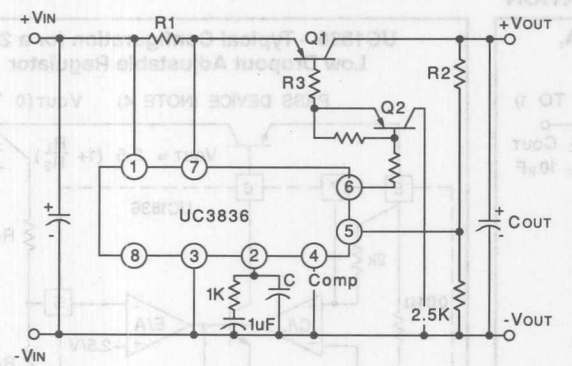
Typical Output Current vs VIN and VOUT

of the UC3836 internal drive transistor
for PDISS = 0.5W (approx.)

		VIN					
	Volts	5	9	12	15	18	24
VOUT	2	150	60	40	30	20	12
	5		105	55	35	25	15
	9			130	60	35	20
	12				120	55	25
	15	Current in mA				110	30

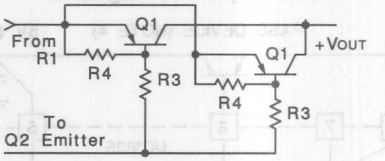
High Current Application

using drive transistor Q2 to increase Q1 base drive
and reduce UC3836 power dissipation



Parallel Pass Transistors

can be added for high current or
high power dissipation applications



EQUATIONS:

$R_1 = 0.100\ V/I_{OUT}$ (MAX)

$R_2 = (V_{OUT} - 2.5V/1mA)$

$R_3 = ((V_{IN} - V_{BE} - V_{SAT})*BETA(min))/I_{OUT}$ (max)

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8-Pin N-FET Linear Regulator Controller

PRELIMINARY

FEATURES

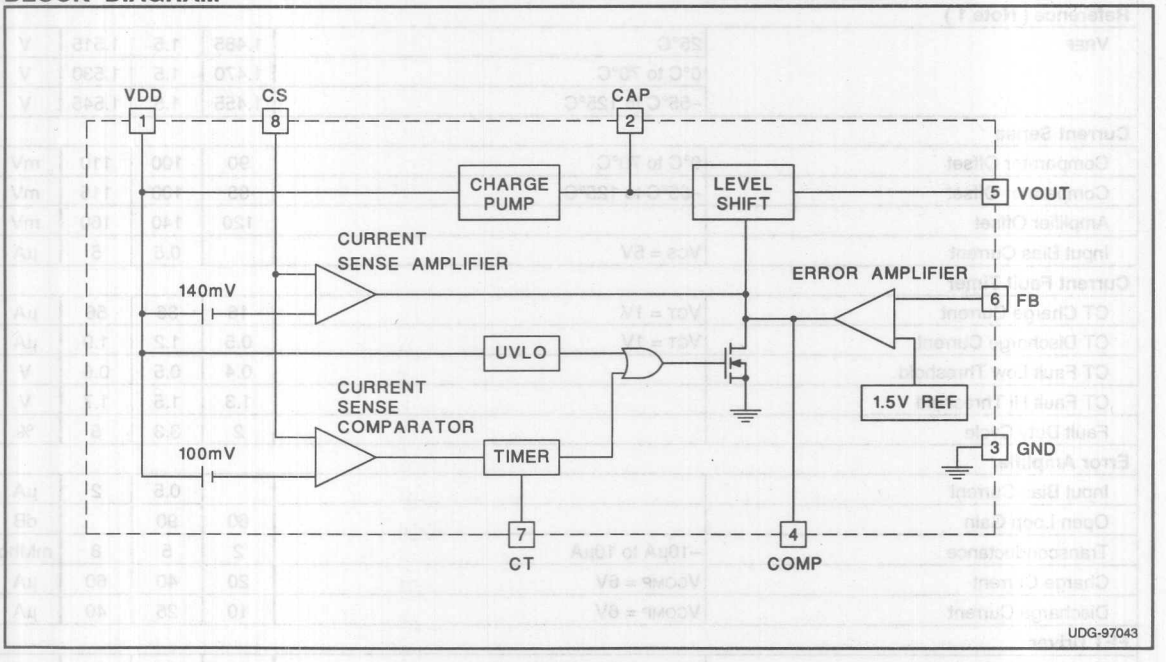
- On Board Charge Pump to Drive External N-MOSFET
- Input Voltage as Low as 3V
- Duty Ratio Mode Over Current Protection
- Extremely Low Dropout Voltage
- Low External Parts Count
- Output Voltages as Low as 1.5V

DESCRIPTION

The UCC3837 Linear Regulator Controller includes all the features required for an extremely low dropout linear regulator that uses an external N-channel MOSFET as the pass transistor. The device can operate from input voltages as low as 3V and can provide high current levels, thus providing an efficient linear solution for custom processor voltages, bus termination voltages, and other logic level voltages below 3V. The on board charge pump creates a gate drive voltage capable of driving an external N-MOSFET which is optimal for low dropout voltage and high efficiency. The wide versatility of this IC allows the user to optimize the setting of both current limit and output voltage for applications beyond or between standard 3-terminal linear regulator ranges.

This 8-pin controller IC features a duty ratio current limiting technique that provides peak transient loading capability while limiting the average power dissipation of the pass transistor during fault conditions. See the Application Section for detailed information.

BLOCK DIAGRAM



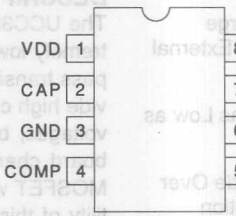
ABSOLUTE MAXIMUM RATINGS

All pins referenced to GND . . . . . –0.3V to +15V
CS, CT, FB . . . . . –0.3V to VDD + 0.3V
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10sec.) . . . . . +300°C

Currents are positive into, negative out of the specified terminal.
Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

DIL-8, SOIC-8 (Top View)
J or N Package, D Package



ELECTRICAL CHARACTERISTICS: Unless otherwise specified, T_A = –55°C to 125°C for the UCC1837, –25°C to 85°C for the UCC2837 and 0°C to 70°C for UCC3837; VDD = 5V, C_T = 10nF, C_{CAP} = 100nF.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply					
Supply Current	VDD = 5V		1	1.5	mA
	VDD = 10V		1.2	2	mA
Under Voltage Lockout					
Minimum Voltage to Start		2.2	2.65	3	V
Minimum Voltage After Start		1.8	2.2	2.6	V
Hysteresis		0.25	0.45	0.65	V
Reference (Note 1)					
V_{REF}	25°C	1.485	1.5	1.515	V
	0°C to 70°C	1.470	1.5	1.530	V
	–55°C to 125°C	1.455	1.5	1.545	V
Current Sense					
Comparator Offset	0°C to 70°C	90	100	110	mV
Comparator Offset	–55°C to 125°C	85	100	115	mV
Amplifier Offset		120	140	160	mV
Input Bias Current	V_{CS} = 5V		0.5	5	µA
Current Fault Timer					
CT Charge Current	V_{CT} = 1V	16	36	56	µA
CT Discharge Current	V_{CT} = 1V	0.5	1.2	1.9	µA
CT Fault Low Threshold		0.4	0.5	0.6	V
CT Fault Hi Threshold		1.3	1.5	1.7	V
Fault Duty Cycle		2	3.3	5	%
Error Amplifier					
Input Bias Current			0.5	2	µA
Open Loop Gain		60	90		dB
Transconductance	–10µA to 10µA	2	5	8	mMho
Charge Current	V_{COMP} = 6V	20	40	60	µA
Discharge Current	V_{COMP} = 6V	10	25	40	µA
FET Driver					
Peak Output Current	V_{CAP} = 10V, VOUT = 1V	0.5	1.5	2.5	mA
Average Output Current	VOUT = 1V	25	100	175	µA
Max Output Voltage	V_{IN} = 4.5V, I_{OUT} = 0µA	8.4	9.7		V
	V_{IN} = 4.5V, I_{OUT} = 10µA, 0°C to 70°C	8	9		V
	V_{IN} = 4.5V, I_{OUT} = 10µA, –55°C to 125°C	7.5	9		V

ELECTRICAL CHARACTERISTICS (cont.): Unless otherwise specified, T_A = –55°C to 12°C for the UCC1837, –25°C to 85°C for the UCC2837 and 0°C to 70°C for UCC3837; VDD = 5V, C_T = 10nF, C_{CAP} = 100nF.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Charge Pump					
CAP Voltage	V_{IN} = 4.5V, C/S = 0V	11	12.5		V
	V_{IN} = 12V, C/S = 0V		15	16.5	V

Note 1: This is defined as the voltage on FB which results in a DC voltage of 8V on VOUT.

PIN DESCRIPTIONS

CAP: The output of the charge pump circuit. A capacitor is connected between this pin and GND to provide a floating bias voltage for an N-Channel MOSFET gate drive. A minimum of a 0.01µF ceramic capacitor is recommended. CAP can be directly connected to an external regulated source such as +12V, in which case the external voltage will be the source for driving the N-Channel MOSFET.

COMP: The output of the transconductance error amplifier and current sense amplifier. Used for compensating the small signal characteristics of the voltage loop (and current loop when Current Sense Amplifier is active in over curret mode).

CS: The negative current sense input signal. This pin should be connected through a low noise path to the low side of the current sense resistor.

CT: The input to the duty cycle timer circuit. A capacitor is connected from this pin to GND, setting the maximum ON time of the over current protection circuits. See the Application Section for programming instructions.

FB: The inverting terminal of the voltage error amplifier, used to feedback the output voltage for comparison with the internal reference voltage. The nominal DC operating voltage at this pin is 1.5V

GND: Ground reference for the device. For accurate output voltage regulation, GND should be referenced to the output load ground.

VDD: The system input voltage is connected to this point. VDD must be above 3V. VDD also acts as one side of the Current Sense Amplifier and Comparator.

VOUT: This pin directly drives the gate of the external N-MOSFET pass element. The typical output impedance of this pin is 6.5kΩ.

APPLICATION INFORMATION

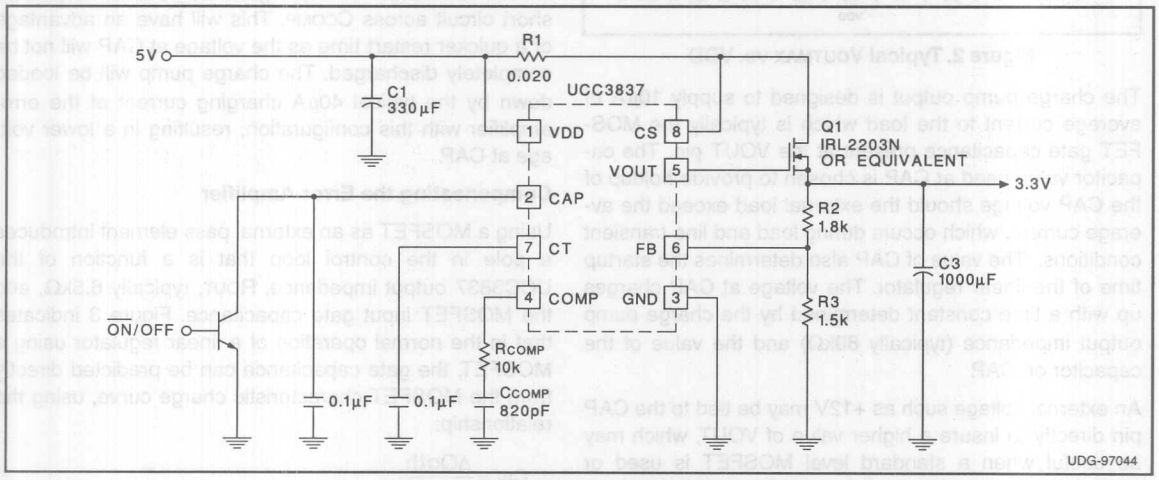


Figure 1. Typical Application 5V to 3.3V, 5A Regulator

Topology and General Operation

Unitrode Application Note U-152 is a detailed design of a low dropout linear regulator using an N-Channel MOSFET as a pass element, and should be used as a guide for understanding the operation of the circuit shown in Figure 1.

APPLICATION INFORMATION (cont.)

Charge Pump Operation

The internal charge pump of the UCC3837 is designed to create a voltage equal to 3 times the input VDD voltage at the CAP pin. There is an internal 5V clamp at the input of the charge pump however that insures the voltage at CAP does not exceed the ratings of the IC. This CAP voltage is used to provide gate drive current to the external pass element as well as bias current to internal sections of the UCC3837 itself. The charge pump output has a typical impedance of 80kΩ and therefore the loading of the IC and the external gate drive reduces the voltage from its ideal level. The UCC3837 can operate in several states including having the error amplifier disabled (shut down), in normal linear regulation mode, and in overdrive mode where the linear regulator is responding to a transient load or line condition. The maximum output voltage available at VOUT is shown in Figure 2 for these various modes of operation.

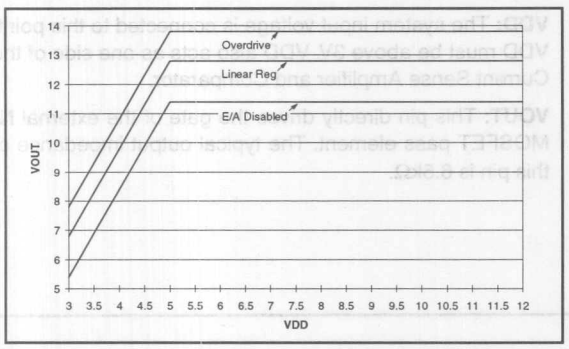


Figure 2. Typical V_{OUTMAX} vs. VDD

The charge pump output is designed to supply 10µA of average current to the load which is typically the MOSFET gate capacitance present at the VOUT pin. The capacitor value used at CAP is chosen to provide holdup of the CAP voltage should the external load exceed the average current, which occurs during load and line transient conditions. The value of CAP also determines the startup time of the linear regulator. The voltage at CAP charges up with a time constant determined by the charge pump output impedance (typically 80kΩ) and the value of the capacitor on CAP.

An external voltage such as +12V may be tied to the CAP pin directly to insure a higher value of VOUT, which may be useful when a standard level MOSFET is used or when VDD is very low and the resulting VOUT voltage may need to be higher. With an external source applied to CAP, the maximum voltage at VOUT will be approximately 1V below the external source. The external +12V source should be decoupled to GND using a minimum of a 0.01µF capacitor.

Choosing a Pass Element

The UCC3837 is designed for use with an N-Channel MOSFET pass element only. The designer may choose a logic level or standard gate level MOSFET depending on the input voltage, the required gate drive, and the available voltage at VOUT as discussed previously. MOSFET selection should be based on required dropout voltage and gate drive characteristics. A lower R_{DSON} MOSFET is used when low dropout is required, but this type of MOSFET will have higher gate capacitance which may result in a slower transient response.

A MOSFET used in linear regulation is typically operated at a gate voltage between the threshold voltage and the gate plateau voltage in order to maintain high gain. This mode of operation is linear, and therefore the channel resistance is higher than the manufacturer's published R_{DSON} value. The MOSFET should only be operated in the non-linear (switch) mode under transient conditions, when minimum dropout voltage is required.

Disabling the UCC3837

Grounding the CAP pin will remove the drive voltage and effectively disable the output voltage. The device used to short the output of CAP should have a very low leakage current when in the OPEN state, since even a few microamps will lower the charge pump voltage.

A second method of disabling the UCC3837 is to place a short circuit across C_{COMP}. This will have an advantage of a quicker restart time as the voltage at CAP will not be completely discharged. The charge pump will be loaded down by the typical 40µA charging current of the error amplifier with this configuration, resulting in a lower voltage at CAP.

Compensating the Error Amplifier

Using a MOSFET as an external pass element introduces a pole in the control loop that is a function of the UCC3837 output impedance, R_{OUT}, typically 6.5kΩ, and the MOSFET input gate capacitance. Figure 3 indicates that in the normal operation of a linear regulator using a MOSFET, the gate capacitance can be predicted directly from the MOSFET characteristic charge curve, using the relationship:

$$C_{IN} = \frac{\Delta Qgth}{\Delta Vgth}$$

This pole can be canceled by programming a zero frequency on the output of the UCC3837 error amplifier equal to the pole frequency. Therefore:

APPLICATION INFORMATION (cont.)

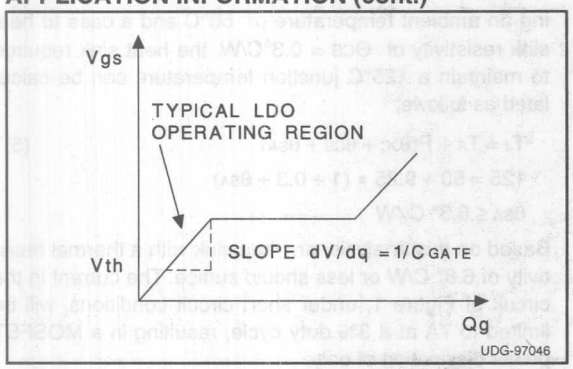


Figure 3.

$$F_{POLE} = \frac{1}{2 \bullet \pi \bullet C_{IN} \bullet R_{OUT}}$$

$$F_{ZERO} = F_{POLE} = \frac{1}{2 \bullet \pi \bullet R_{COMP} \bullet C_{COMP}}$$

$$R_{COMP}C_{COMP} = \frac{1}{2 \bullet \pi \bullet F_{POLE}}$$

where C_{IN} is the MOSFET input capacitance and R_{OUT} is the output impedance of VOUT.

The value of C_{COMP} should be large enough that parasitics connected to COMP do not effect the zero frequency. A minimum of 220pF is recommended.

Transient Response

The transient performance of a linear regulator built using the UCC3837 can be predicted by understanding the dynamics of the transient event. Consider a load transient on the application circuit of Figure 1, where the output current steps from a low value to a high value. Initially, the output voltage will drop as a function of the output capacitors ESR times the load current change. In response to the decrease in feedback voltage at FB, the UCC3837 error amplifier will increase its charge current to a typical value of 40µA. The output of the amplifier will therefore respond by first stepping the voltage proportional to 40µA times R_{COMP}, and then ramping up proportional to 40µA and the value of C_{COMP}. Dynamic response can therefore be improved by increasing R_{COMP} and decreasing C_{COMP}.

The value of VOUT will increase the same amount as the increase in the error amplifier output. The UCC3837 output gate drive current, however, is internally limited to 1.5mA. The response of the voltage at the gate of the external pass element is therefore a function of the 1.5mA drive current and the external gate charge, as obtained from the MOSFET data sheet gate charge curve.

For the application circuit shown in Figure 1, the voltage at the error amplifier output will increase quickly by 400mV due to the 40µA current through R_{COMP}. The error amplifier will then slew at approximately 50mV per microsecond as the 40µA charges C_{COMP}.

From the IRL2203N data sheet, the typical required gate voltage at room temperature, to deliver 5A is 2.6V. The threshold for the device is approximately 1.5V. From the gate charge curve for the IRL2203N, approximately 7nC charge is required to change the gate voltage from 1.5V to 2.6V. With 1.5mA gate drive current, the required time to charge the gate is therefore 4.7µs.

Overcurrent Protection and Thermal Management:

Overcurrent protection is provided via the UCC3837's internal current amplifier and overcurrent comparator. If at any time the voltage across the current sense resistor crosses the comparator threshold, the UCC3837 begins to modulate the output driver at a 3% duty cycle. During the 3% on time, if the current forces 140mV across the sense amplifier, the UCC3837 will enter a constant output current mode. Figure 4 illustrates the cyclical retry of the UCC3837 under fault conditions. Note that the initial fault time is longer than subsequent cycles due to the fact that the timing capacitor is completely discharged and must initially charge to the reset threshold of 0.5V.

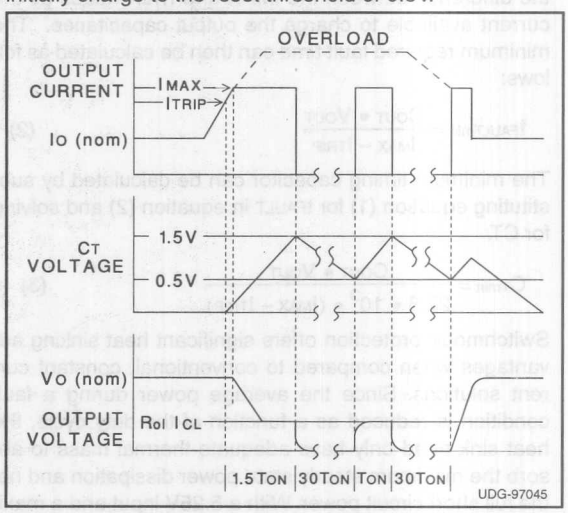


Figure 4. Load Current, Timing Capacitor Voltage and Output Voltage Under Fault Conditions

Fault time duration is controlled by the value of the timing capacitor, C_T, according to the following equation:

$$t_{FAULT} = C_T \bullet \frac{\Delta V}{I} = C_T \bullet \frac{1.5 - 0.5}{36 \bullet 10^{-6}} = 27.8 \bullet 10^3 \bullet C_T \quad (1)$$

APPLICATION INFORMATION (cont.)

Figure 5 provides a plot of fault time vs. timing capacitance. The fault time duration is set based upon the load capacitance, load current, and the maximum output current. The "on" or fault time must be of sufficient duration to charge the load capacitance during a normal startup sequence or when recovering from a fault. If not, the charge accumulated on the output capacitance will be depleted by the load during the "off" time. The cycle will then repeat, preventing the output from turning on.

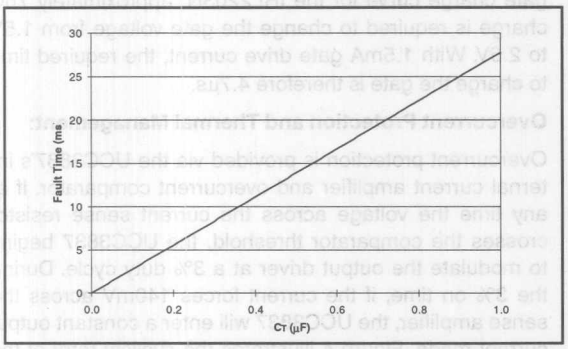


Figure 5. Fault Time vs. Timing Capacitance

To determine the minimum fault time, assume a maximum load current just less than the trip limit. This leaves the difference between the IMAX and ITRIP values as the current available to charge the output capacitance. The minimum required fault time can then be calculated as follows:

$$t_{FAULTmin} = \frac{C_{OUT} \bullet V_{OUT}}{I_{MAX} - I_{TRIP}} \quad (2)$$

The minimum timing capacitor can be calculated by substituting equation (1) for tFAULT in equation (2) and solving for CT.

$$C_{Tmin} = \frac{C_{OUT} \bullet V_{OUT}}{27.8 \bullet 10^3 \bullet (I_{MAX} - I_{TRIP})} \quad (3)$$

Switchmode protection offers significant heat sinking advantages when compared to conventional, constant current solutions. Since the average power during a fault condition is reduced as a function of the duty cycle, the heat sink need only have adequate thermal mass to absorb the maximum steady state power dissipation and not the full short circuit power. With a 5.25V input and a maximum output current of 5A, the power dissipated in the MOSFET is given by:

$$P = (V_{IN} - V_{RSENSE} - V_{OUT}) \bullet I_{OUT} \quad (4)$$

$$P = (5.25 - (5.002) - 3.3) \bullet 5 = 9.25W$$

Given that the thermal resistivity of the MOSFET is specified as 1°C/W for the TO-220 package style and assuming an ambient temperature of 50°C and a case to heat sink resistivity of Θ_{CS} = 0.3°C/W, the heat sink required to maintain a 125°C junction temperature can be calculated as follows:

$$T_J = T_A + P(\theta_{JC} + \theta_{CS} + \theta_{SA}) \quad (5)$$

$$125 = 50 + 9.25 \bullet (1 + 0.3 + \theta_{SA})$$

$$\theta_{SA} \leq 6.8° \text{ C/W}$$

Based on this analysis, any heatsink with a thermal resistivity of 6.8° C/W or less should suffice. The current in the circuit of Figure 1, under short circuit conditions, will be limited to 7A at a 3% duty cycle, resulting in a MOSFET power dissipation of only:

$$P = [(V_{INmax} - I_{OUT} \bullet (R_{SENSE})) \bullet I_{OUT}] \bullet Duty \quad (6)$$

$$P = [(5.25 - 7 \bullet (0.02)) \bullet 7] \bullet 0.03 = 1.07W$$

Without switchmode protection, the short circuit power dissipation would be 35.8W, almost four times the nominal dissipation.

Using Printed Circuit Board Etch as a Sense Resistor

Unitrode Design Note 71 discusses the use of printed circuit board copper etch as a low ohm sense resistor. This technique can easily be applied when using the UCC3837. The application circuit shown in Figure 1 can be used as an example. This linear regulator is designed with a 5A average load current, demanding a 20mΩ sense resistor to result in a 100mV current sense comparator signal for the UCC3837. The maximum ambient temperature of the linear regulator is 70°C.

Using DN-71, a 1 ounce outer layer etch of 0.05 inches wide and 1.57 inches long results in a resistance of 20mΩ at an ambient temperature of 70°C and an operating current of 5A. Because the resistivity of copper is a function of temperature, the current limit at lower temperatures will be higher, as shown in Figure 6.

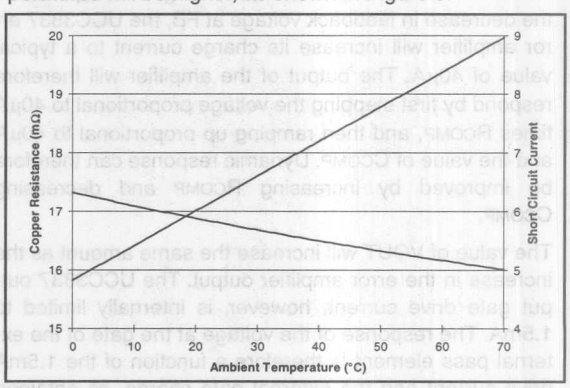


Figure 6. Copper Resistance and Short Circuit Limit for Example Resistor

APPLICATION INFORMATION (cont.)

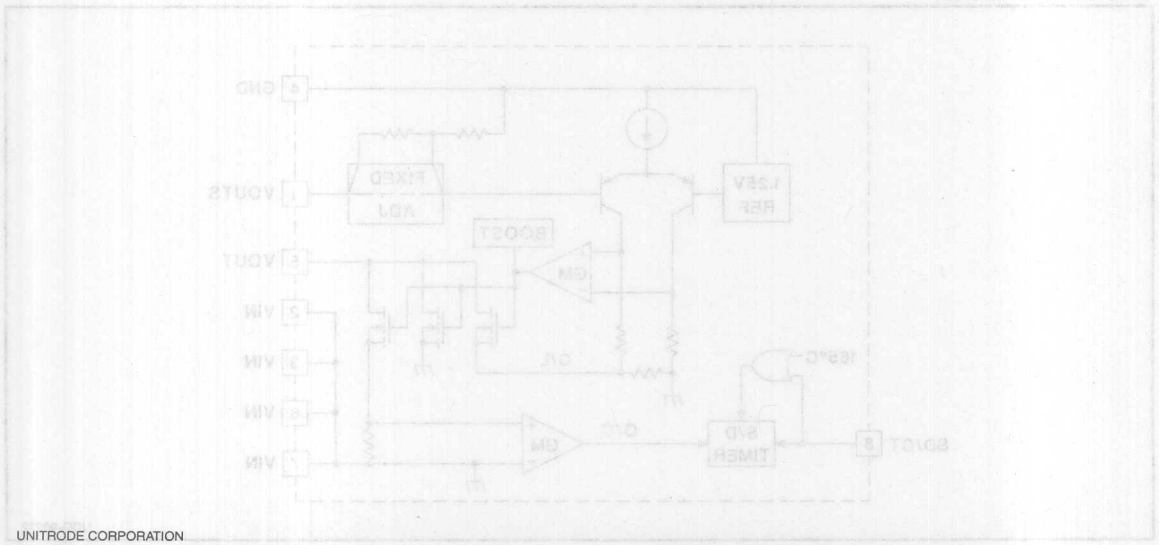
Practical Considerations

In order to achieve the expected performance, careful attention must be paid to circuit layout. The printed circuit board should be designed using a single point ground, referenced to the return of the output capacitor. All traces carrying high current should be made as short and wide as possible in order to minimize parasitic resistance and inductance effects.

To illustrate the importance of these concepts, consider the effects of a 1.5" PCB trace located between the output capacitor and the UCC3837 feedback reference. A 0.07" wide trace of 1oz. copper results in an equivalent resistance of 10.4mΩ. At a load current of 3A, 31.2mV is dropped across the trace, contributing almost 1% error to the DC regulation. Likewise, the inductance of the trace is approximately 3.24nH, resulting in a 91mV spike during the 100ns it takes the load current to slew from 200mA to 3A.

The dropout voltage of a linear regulator is often a key design parameter. Calculations of the dropout voltage of a linear regulator based on the UCC3837 Controller should consider all of the following:

- Sense resistor drop, including temperature and tolerance effects,
- Path resistance drops on both the input and output voltages,
- MOSFET resistance as a function of temperature and gate drive, including transient performance,
- Ground path drops.



UNITRODE CORPORATION
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UNITRODE

UCC284-5/-12/-ADJ
UCC384-5/-12/-ADJ

PRELIMINARY

Low Dropout 0.5A Negative Linear Regulator

FEATURES

- Precision Negative Series Pass Voltage Regulation
- 0.2V Drop Out at 0.5A
- Wide Input voltage Range -3.2V to -15V
- Low Quiescent Current Irrespective of Load
- Simple Logic Shutdown Interfacing
- -5V, -12V and Adjustable Output
- 3% Duty Cycle Short Circuit Protection
- Remote Load Sensing for Accurate Load Regulation
- 8-Pin DP Package

DESCRIPTION

The UCC384 family of negative linear series pass regulators is tailored for low drop out applications where low quiescent power is important. Fabricated with a BCDMOS technology ideally suited for low input to output differential applications, the UCC384 will pass 0.5A while requiring only 0.2V of input voltage headroom. Drop out voltage decreases linearly with output current, so that drop out at 50mA is less than 20mV.

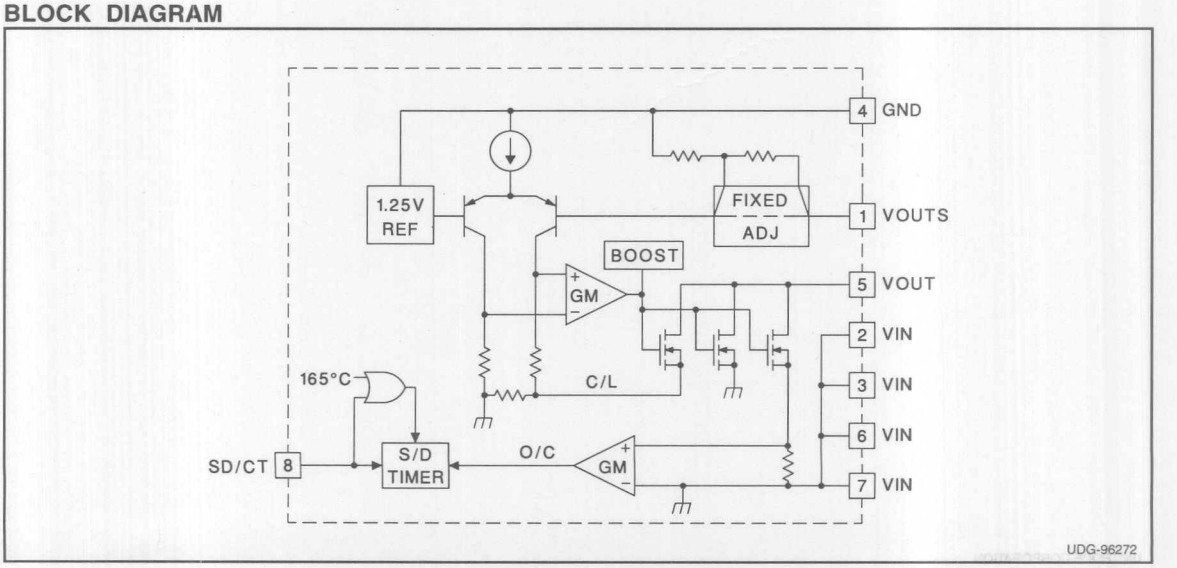
Quiescent current consumption for the device under normal (non-drop out) conditions is typically 200µA. An integrated charge pump is internally enabled only when the device is operating near drop out with low VIN. This guarantees that the device will meet the drop out specifications even for maximum load current and a VIN of –3.2V with only a modest increase in quiescent current. Quiescent current is always less than 350µA, with the charge pump enabled. Quiescent current of the UCC384 does not increase with load current.

Short circuit current is internally limited. The device responds to a sustained over current condition by turning off after a TON delay. The device then stays off for a period, TOFF, that is 32 times the TON delay. The device then begins pulsing on and off at the TON/TOFF duty cycle of 3%. This drastically reduces the power dissipation during short circuit such that heat sinking, if at all required, must only accommodate normal operation. An external capacitor sets the on time. The off time is always 32 times TON.

The UCC384 can be shutdown to 40µA (maximum) by pulling the SD/CT pin greater than –0.6V. To allow for simpler interfacing, the SD/CT pin may be pulled above the ground pin without turning on clamping diodes.

Internal power dissipation is further controlled with thermal overload protection circuitry. Thermal shutdown occurs if the junction temperature exceeds 165°C. The chip will remain off until the temperature has dropped 20°C.

BLOCK DIAGRAM



1/97

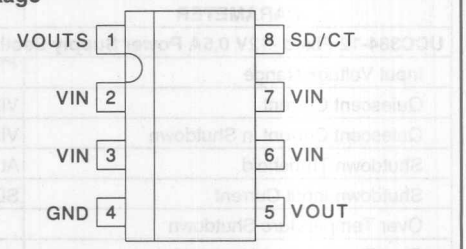
ABSOLUTE MAXIMUM RATINGS

Supply Voltage, VIN ..... –16VV
Shutdown Voltage ..... +6V to –5V
Storage Temperature ..... –65°C to +150°C
Junction Temperature ..... –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

All voltages are with respect to ground. Currents are positive into, negative out of the specified terminal. All voltages are with respect to ground. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

SOIC-8 (Top View)
DP Package



ELECTRICAL CHARACTERISTICS

Unless otherwise specified, T_A = 0°C to 70°C for the UCC384 and –40°C to 85°C for the UCC284, VIN = VOUT – 1.5V, I_{OUT} = 0mA, C_{OUT} = 4.7µF, and CT = 0.015µF. For UCC384-ADJ, VOUT is set to –3.3V. $T_J = T_A$.

PARAMETER	TEST CONDITIONS	MIN	TYPE	MAX	UNITS
UCC384-5 Fixed -5V 0.5A Regulation Section					
Output Voltage	T_A = 25°C	–5.075	–5	–4.925	V
	Overall Conditions	–5.125		–4.875	V
Line Regulation	VIN = –5.3V to –15V		0.004	0.011	%/V
Load Regulation	I_{OUT} = 0mA to 0.5A		0.1	0.25	%
Output Noise Voltage	T_A = 25°C, BW = 10Hz to 10kHz		200		µVRMS
Drop Out Voltage, VOUT - VIN	I_{OUT} 0.5A, VOUT = –4.85V		0.2	0.5	V
	I_{OUT} 50mA, VOUT = –4.85V		20	50	mV
UCC384-5 Fixed -5V 0.5A Power Supply Section					
Input Voltage Range		–15		–5.2	V
Quiescent Current Charge Pump On	VIN = –4.85V (Note 1)		240	350	µA
Quiescent Current	VIN = –15V		200	250	µA
Quiescent Current in Shutdown	VIN = –15V, SD/CT = 0		19	40	µA
Shutdown Threshold	At Shutdown Pin	–0.8	–0.6	–0.4	V
Shutdown Input Current	SD/CT = 0		17	25	µA
Over Temperature Shutdown			165		°C
Over Temperature Hysteresis			20		°C
UCC384-5 Fixed -5V 0.5A Current Limit Section					
Peak Current Limit	VOUT = 0V	0.7		1.5	A
Over Current Threshold		0.55		0.9	A
Current Limit Duty Cycle	VOUT = 0V		3		%
Overcurrent Time Out, T_{ON}	VOUT = 0V	300	410	550	µs
UCC384-12 Fixed 12V 0.5A Regulation Section					
Output Voltage	T_A = 25°C	–12.18	–12	–11.82	V
	Overall Conditions	–12.30		–11.70	V
Line Regulation	VIN = –12.3V to –15V		0.010	0.027	%/V
Load Regulation	I_{OUT} = 0mA to 0.5A		0.24	0.60	%
Output Noise Voltage	T_A = 25°C, BW = 10Hz to 10kHz		200		µVRMS
Drop Out Voltage, VOUT - VIN	I_{OUT} 0.5A, VOUT = –11.85V		0.2	0.5	V
	I_{OUT} 50mA, VOUT = –11.85V		20	50	mV

ELECTRICAL CHARACTERISTICS (cont.) Unless otherwise specified, T_A = 0°C to 70°C for the UCC384 and –40°C to 85°C for the UCC284x, VIN = VOUT – 1.5V, I_{OUT} = 0mA, C_{OUT} = 4.7µF, and CT = 0.015µF. For UCC384-ADJ, VOUT is set to –3.3V. $T_J = T_A$.

PARAMETER	TEST CONDITIONS	MIN	TYPE	MAX	UNITS
UCC384-12 Fixed -12V 0.5A Power Supply Section					
Input Voltage Range		–15		–12.2	V
Quiescent Current	VIN = –15V, SD/CT = 0		240	350	µA
Quiescent Current in Shutdown	VIN = –15V		19	40	µA
Shutdown Threshold	At Shutdown Pin	–0.8	–0.6	–0.4	V
Shutdown Input Current	SD/CT = 0		17	25	µA
Over Temperature Shutdown			165		°C
Over Temperature Hysteresis			20		°C
UCC384-12 Fixed -12V 0.5A Current Limit Section					
Peak Current Limit	VOUT = 0V	0.7		1.5	A
Over Current Threshold		0.55		0.9	A
Current Limit Duty Cycle	VOUT = 0V		3		%
Over Current Time Out, T_{ON}	VOUT = 0V	300	410	550	µs
UCC384-ADJ Adjustable 0.5A Regulation Section					
Reference Voltage	T_A = 25°C	–1.27	–1.25	–1.23	V
	Over Temperature	–1.28		–1.22	V
Line Regulation	VIN = –3.5V to –15V, VOUT = VOUTS		0.003	0.008	%/V
Load Regulation	I_{OUT} = 0mA to 0.5A		0.07	0.17	%
Output Noise Voltage	T_A = 25°C, BW = 10Hz to 10kHz		200		µVRMS
Drop Out Voltage, VOUT - VIN	I_{OUT} 0.5A, VOUT = –3.15V		0.2	0.5	V
	I_{OUT} 50mA, VOUT = 3.15V		20	50	mV
Sense Pin Input Current			100	250	nA
UCC384-ADJ Adjustable 0.5A Power Supply Section					
Input Voltage Range		–15		–3.5	V
Undervoltage Lockout		–3.2		–2.8	V
Quiescent Current Charge Pump On	VIN = –3.15V (Note 1)		230	350	µA
Quiescent Current	VIN = –15V		190	250	µA
Quiescent Current in Shutdown	VIN = –15V, SD/CT = 0		19	40	µA
Shutdown Threshold	At Shutdown Pin	–0.8	–0.6	–0.4	V
Shutdown Input Current	SD/CT = 0		17	25	µA
Over Temperature Shutdown			165		°C
Over Temperature Hysteresis			20		°C
UCC384-ADJ Adjustable 0.5A Current Limit Section					
Peak Current Limit	VOUT = 0V	0.7		1.5	A
Over Current Threshold		0.55		0.9	A
Current Limit Duty Cycle	VOUT = 0V		3		%
Over Current Time Out, T_{ON}	VOUT = 0V	300	410	550	µs

Note 1: Internal Charge Pump is enabled only for drop-out condition with low VIN. Only in this condition is the Charge Pump required to provide additional output FET gate drive to maintain drop-out specifications. For conditions where the Charge Pump is not required, it is disabled, which lowers overall device power consumption.

PIN DESCRIPTIONS

GND: This is the low noise ground reference input for regulation. All voltages are measured with respect to this pin.

SD/CT: For the UCC384-5/-12, this is the shutdown pin which, when pulled greater than –0.6V relative to GND, puts the device in a low current state. This pin is internally clamped to –1.5V via a 50kΩ source impedance. This input should not be externally driven more negative than –5V; otherwise device damage will result. For all versions, a capacitor is required between the SD/CT pin and GND to set the short circuit charging time, T_{ON} during overcurrent according to the following (typical) equation:

$$T_{ON} = 27{,}300 \bullet C_{CT}$$

Note: The SD/CT capacitor must be connected to ground, not VIN, to assure that SD/CT is not pulled significantly negative during power-up.

VIN: Negative input supply for the regulator. Bypass this pin to GND with at least 1µF of low ESR, ESL capacitance.

VOUT: This is the regulator output. A single 4.7µF output capacitor connected to GND will generally provide adequate loop compensation and load step transient response. Smaller output capacitors will degrade the load step performance of the regulator.

For a given compensation capacitor, regulator loop stability generally improves as the output load current increases. As well, there exists an inverse relationship between capacitance value and ESR. Namely, as the capacitor value decreases (tantalums and electrolytic), the ESR increases, which tends to keep the effective zero confined to a range of 1kHz to 100kHz. Thus, for load currents above 5mA, the device is stable for capacitor values below 1µF, as the increasing ESR keeps the zero frequency near the location of the on chip pole, which occurs at approximately 10kHz. Similarly, large capacitors also provide stability since their ESR's are falling.

The exact range of capacitor values and ESR's over which stability can be guaranteed is difficult to determine, because the load current becomes a variable in the equation. However, the device is stable for capacitor values ranging form 1µF and up, with ESR's up to 5Ω. Under some circumstances, even sub 1µF stability is possible for ESR's consistent with this size of capacitor.

VOUTS: Feedback for regulator sensing of the output voltage. For loads which are a considerable resistive distance form the VOUT pin, the VOUTS pin can be used to move the resistance into the control loop of the regulator, thereby effectively canceling the IR drop associated with the load path. For local regulation, merely connect this pin directly to VOUT. For the -ADJ (adjustable) device, the output voltage can be set by two external resistors according to the following relationship:

$$VOUT = -1.25 \bullet \left(1 + \frac{R1}{R2}\right)$$

where R1 is a resistor connected between VOUT and VOUTS and R2 is a resistor connected between VOUTS and GND. Because R1 and R2 will generally be quite large, a small lead cap should be placed across R1 to cancel the input pole created by R1 and the parasitic capacitance appearing on VOUTS. Values of approximately 20pF should be adequate.

APPLICATION INFORMATION

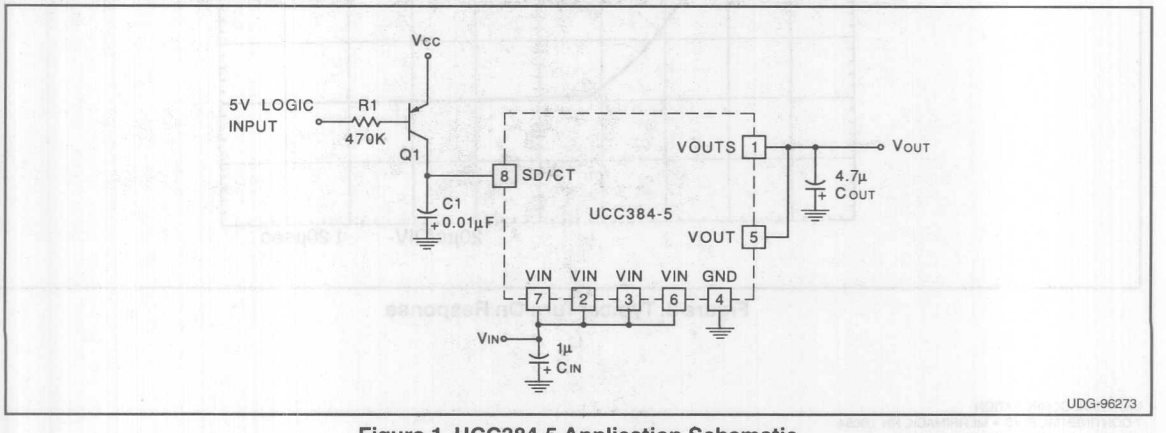


Figure 1. UCC384-5 Application Schematic

APPLICATION INFORMATION (cont.)

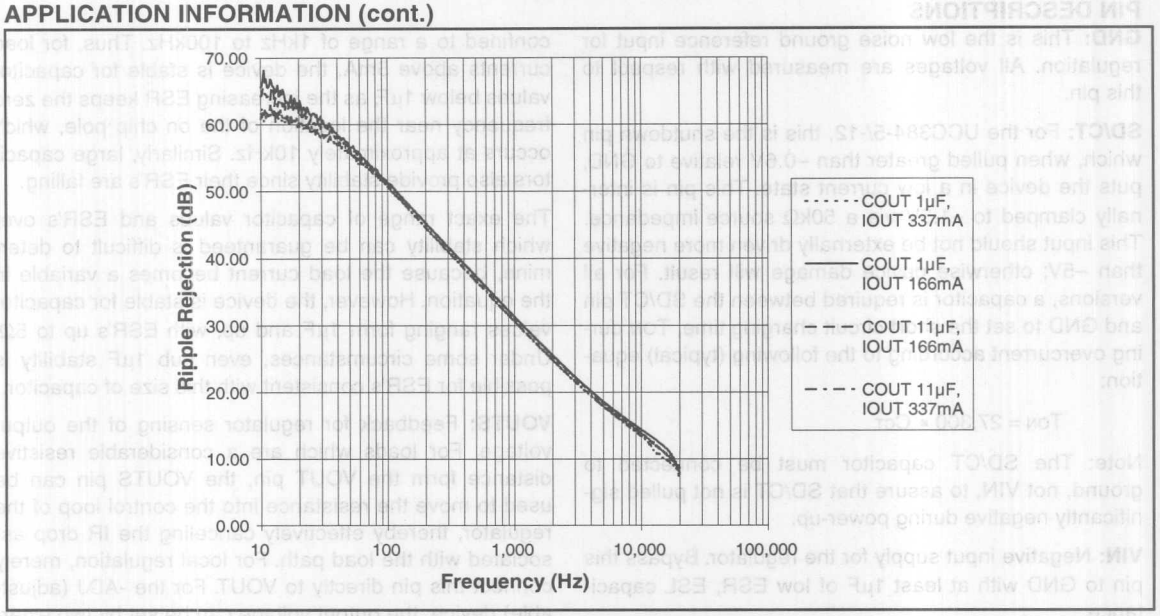


Figure 2. Ripple Rejection vs Frequency

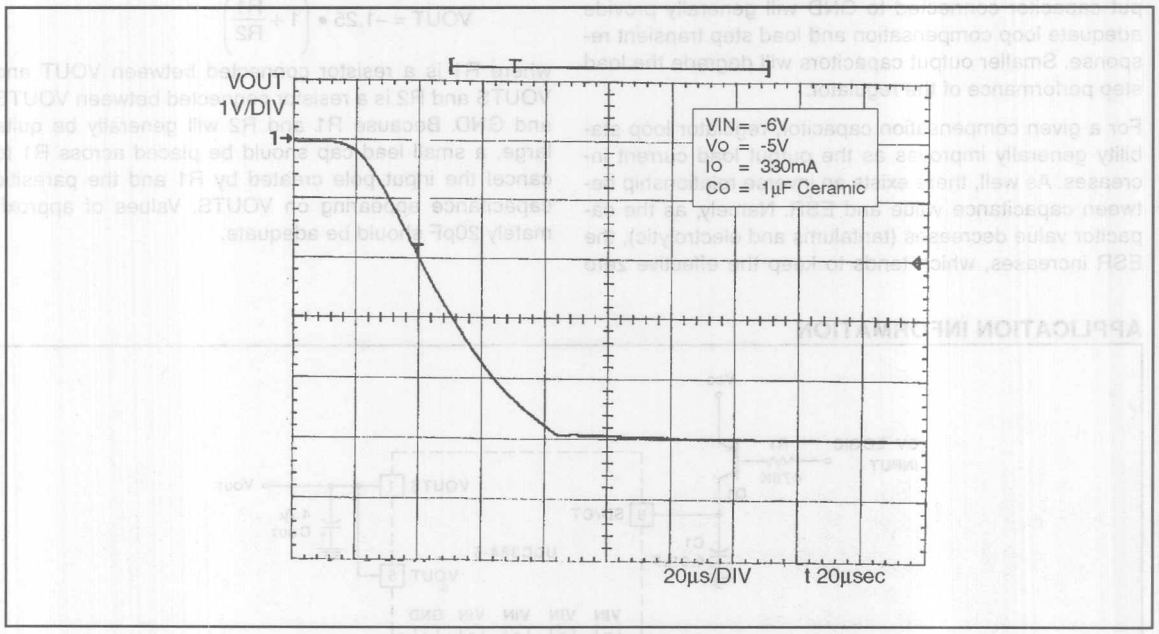


Figure 3. Typical Turn On Response

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Fast LDO Linear Regulator

FEATURES

- Fast Transient Response
- 10mA to 5A Load Current
- Short Circuit Protection
- Maximum Dropout of 450mV at 5A Load Current
- Separate Bias and VIN Pins
- Available in Adjustable or Fixed Output Voltages
- 5 Pin Package allows Kelvin Sensing of Load Voltage
- Reverse Current Protection

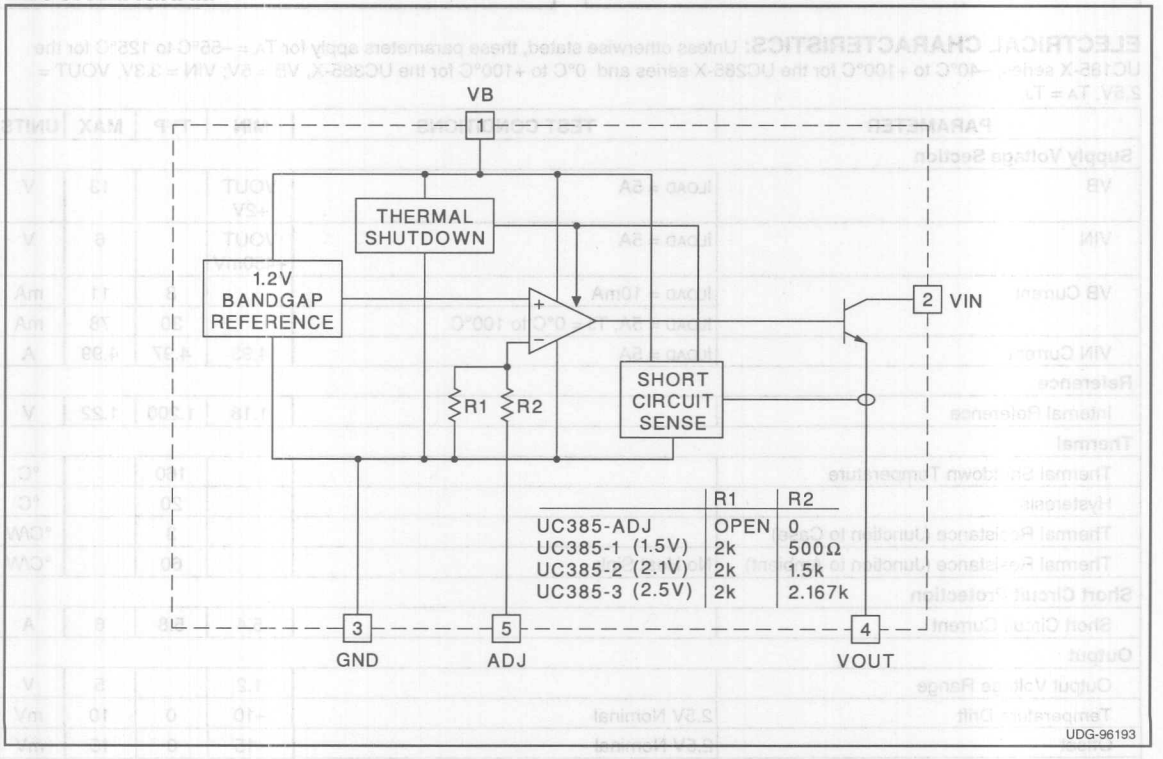
DESCRIPTION

The UC385 is a low dropout linear regulator providing a quick response to fast load changes. Combined with its precision on-board reference, the UC385 excels at driving GTL and BTL buses. Due to its fast response to load transients, the total capacitance required to decouple the regulator's output can be significantly decreased when compared to standard LDO linear regulators.

Dropout voltage (VIN to VOUT) is only 450mV maximum and 350mV typical at 5A load (–40°C to +100°C).

The on-board bandgap reference is stable with temperature and scaled for a 1.200V input to the internal power amplifier. The UC385 is available in fixed output voltages of 1.5V, 2.1V, or 2.5V. The output voltage of the adjustable version can be set with two external resistors. If the external resistors are omitted, the output voltage defaults to 1.2V.

BLOCK DIAGRAM



	R1	R2
UC385-ADJ	OPEN	0
UC385-1 (1.5V)	2k	500Ω
UC385-2 (2.1V)	2k	1.5k
UC385-3 (2.5V)	2k	2.167k

ABSOLUTE MAXIMUM RATINGS

VIN ..... +7.5V
Output Voltage ..... +1.2V to 6.0V
Storage Temperature ..... –65°C to +150°C
Junction Temperature ..... –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

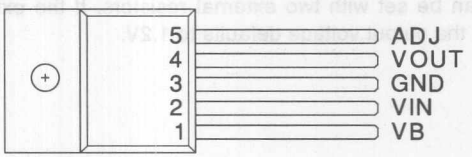
ORDERING INFORMATION

UC □ 85 □ - □
- Output Voltage
- Package
- Temperature Range

Temperature Range	Package	Output Voltage
1: –55°C to +125°C	T: TO-220	1: 1.5V
2: –40°C to +100°C	TD: TO-263	2: 2.1V
3: 0°C to +100°C		3: 2.5V
		ADJ: 1.2V orAdjustable

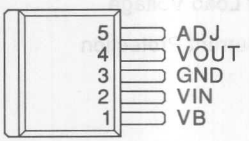
CONNECTION DIAGRAMS

5-Pin TO-220 (Top View)
T Package



Note: Tab = Ground

5-Pin TO-263 (Top View)
TD Package



Note: Tab = Ground

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these parameters apply for T_A = –55°C to 125°C for the UC185-X series, –40°C to +100°C for the UC285-X series and 0°C to +100°C for the UC385-X, VB = 5V; VIN = 3.3V, VOUT = 2.5V, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Section					
VB	I_{LOAD} = 5A	VOUT +2V		13	V
VIN	I_{LOAD} = 5A	VOUT +450mV		6	V
VB Current	I_{LOAD} = 10mA		8	11	mA
	I_{LOAD} = 5A, T_J = 0°C to 100°C		30	78	mA
VIN Current	I_{LOAD} = 5A	4.93	4.97	4.99	A
Reference					
Internal Reference		1.18	1.200	1.22	V
Thermal					
Thermal Shutdown Temperature			160		°C
Hysteresis			20		°C
Thermal Resistance (Junction to Case)			3		°C/W
Thermal Resistance (Junction to Ambient)	No Heat Sink		60		°C/W
Short Circuit Protection					
Short Circuit Current		5.4	5.8	6	A
Output					
Output Voltage Range		1.2		5	V
Temperature Drift	2.5V Nominal	–10	0	10	mV
Offset	2.5V Nominal	–15	0	15	mV
Load Current		0.010		5	A
PSRR (VB)		50	60	70	dB
PSRR (VIN)		80	100		dB

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these parameters apply for T_A = –55°C to 125°C for the UC185-X series, –40°C to +100°C for the UC285-X series and 0°C to +100°C for the UC385-X, VB = 5V; VIN = 3.3V, VOUT = 2.5V, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output (cont.)					
Dropout to VIN (VIN - VOUT)	I_{LOAD} = 5A, T_J = 0°C to +100°C	300	350	450	mV
	I_{LOAD} = 5A, T_J = –55°C to +125°C			475	mV
Dropout to VB (VB - VOUT)	I_{LOAD} = 5A, T_J = 0°C to +100°C	1.8	1.9	2.0	V
	I_{LOAD} = 5A, T_J = –55°C to +125°C	1.5	1.9	2.2	V
Minimum Output Capacitance		100			µF
Load Regulation	I_{LOAD} = 10mA to 5A		1	3	mV

PIN DESCRIPTIONS

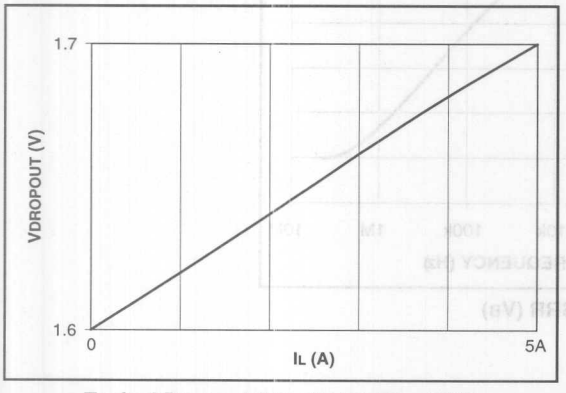
ADJ: In the adjustable version, the user programs the output voltage with two external resistors. The resistors should be 0.1% for high accuracy. The output amplifier is configured as a non-inverting operational amplifier. The resistors should meet the criteria of R3 || R4 < 100Ω. Connect ADJ to VOUT for an output voltage of 1.2V. Note that the point at which the feedback network is connected to the output is the Kelvin sense point.

GND: For accurate results, the GND pin should be referenced to the load ground.

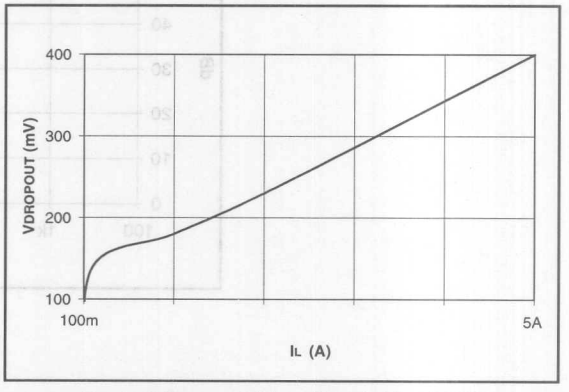
VB: Supplies power to all circuits of the regulator except the output power transistor. The 2V headroom from VB to VOUT allows the use of a Darlington output stage for inherently low output impedance and fast response. (Dropout is derated for junction temperatures below 0°C.)

VIN: Supplies the current to the collector of the output power transistor only. The dropout (VIN-VOUT) is under 100mV for light loads; maximum dropout is 450mV at 5A for T_J = 0°C to +110°C. (Dropout is derated for junction temperatures over 110°C.)

VOUT: This pin should be connected to the load via a low impedance path. Avoid connectors which add significant inductance and resistance. Note that even though a Kelvin sense is available through a 5 pin package, care must be taken since voltage drops along wire traces add to the dropout voltage.



Typical Dropout (V_B - V_{OUT}), T_J = 27°C



Typical Dropout (V_{IN} - V_{OUT}), T_J = 27°C

APPLICATION INFORMATION

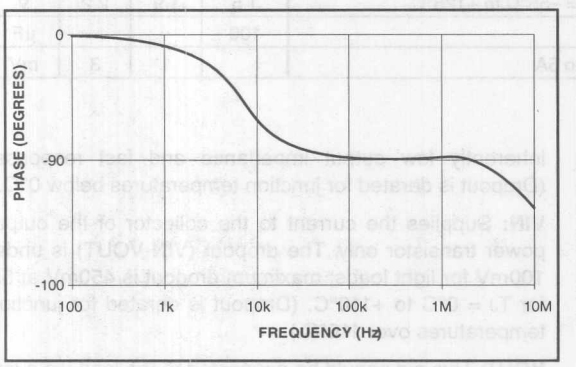
The UC385 is easy to use. The adjustable version requires two resistors to set the output voltage. The fixed versions of the UC385 require no external resistors. All versions of the UC385 require decoupling capacitors on the input and output. In a typical application, VB and VIN are driven from switching power supplies which may have large filter capacitors at their outputs. If the UC385 is further than 12 inches from the power supply, it is recommended to add local decoupling as close as possible to the linear regulator.

Decouple the output of the UC385 with at least 100µF of high quality tantalum or Sanyo OSCON capacitors close to the VOUT pin for maximum stability. Many ap-

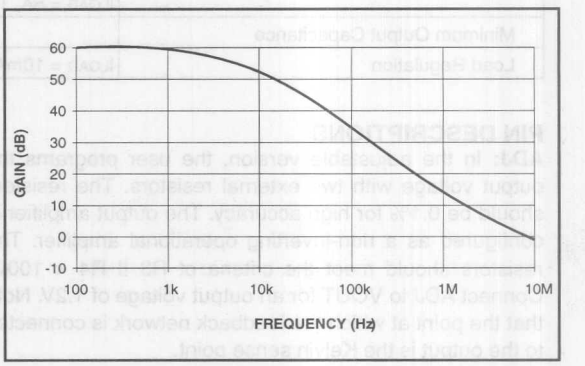
APPLICATION INFORMATION (cont.)

plications involving ultra fast GTL or BTL applications require additional capacitance close to the load. The exact amount will vary according to speed and magnitude of the load transients and the tolerance allowed for transients on VOUT. When specifying the decoupling capacitors, the series resistance of the capacitor bank is an important factor in its ability to filter load transients.

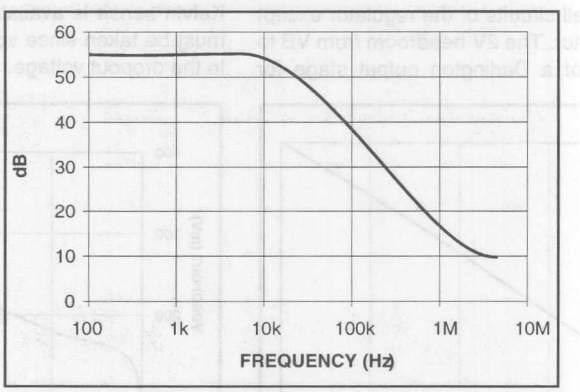
The UC385 allows for Kelvin sensing the voltage at the load. This improves regulation performance and eliminates the voltage drops due to wire trace resistance. This voltage drop must be added to the headroom (VIN to VOUT and VB to VOUT). The dropout of 450mV is measured at the pins and does not include additional drops due to trace resistance.



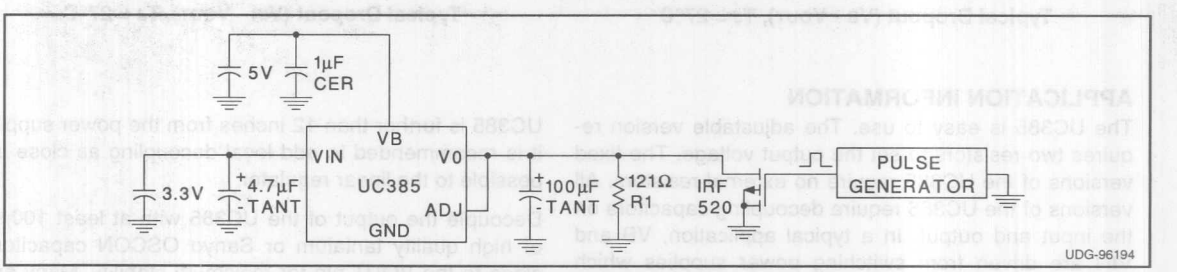
Open Loop Phase
(100µF Output Capacitance, 1A Load)



Open Loop Gain
(100µF Output Capacitance, 1A Load)

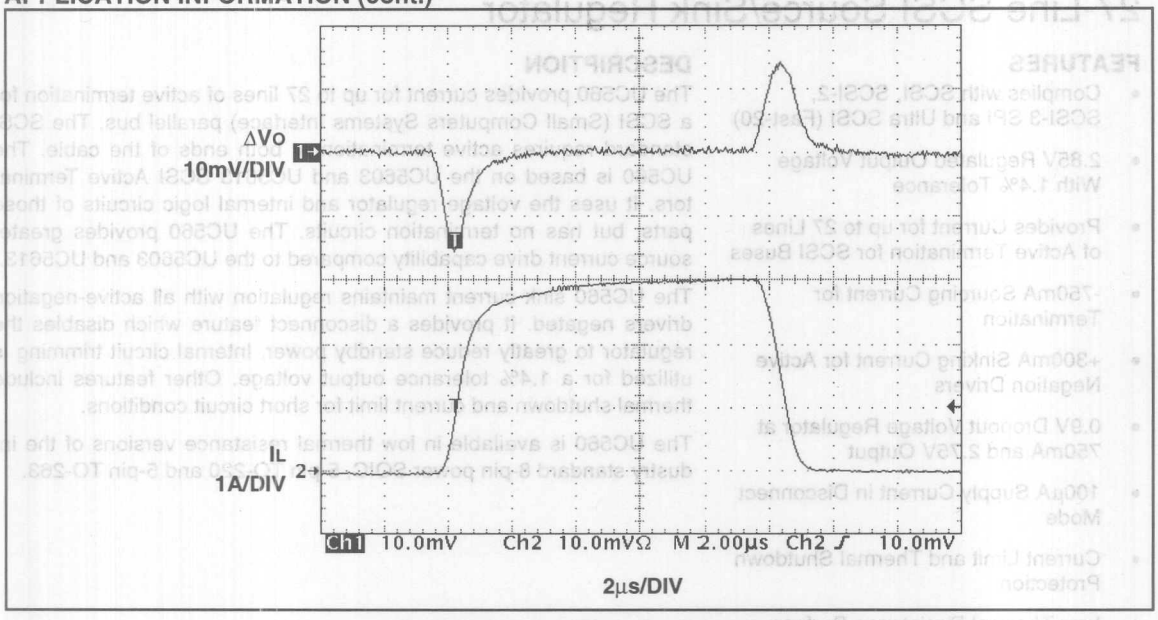


PSRR (V_B)

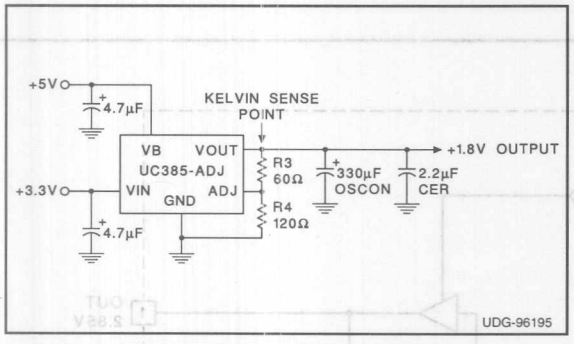


Transient Test Circuit

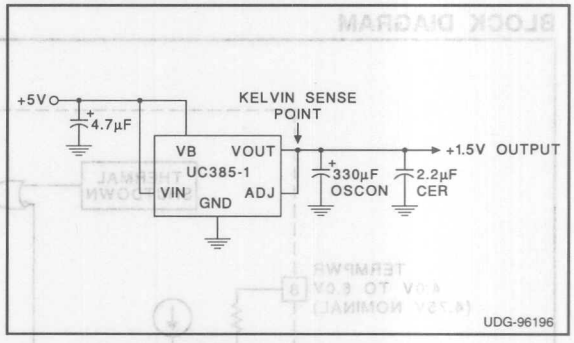
APPLICATION INFORMATION (cont.)



10mA to 3A/µs Load Transient Response



Typical UC385-ADJ Application



Typical UC385-1, -2, or -3 Application

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27-Line SCSI Source/Sink Regulator

FEATURES

- Complies with SCSI, SCSI-2, SCSI-3 SPI and Ultra SCSI (Fast-20)
- 2.85V Regulated Output Voltage With 1.4% Tolerance
- Provides Current for up to 27 Lines of Active Termination for SCSI Buses
- -750mA Sourcing Current for Termination
- +300mA Sinking Current for Active Negation Drivers
- 0.9V Dropout Voltage Regulator at 750mA and 2.75V Output
- 100µA Supply Current in Disconnect Mode
- Current Limit and Thermal Shutdown Protection
- Low Thermal Resistance Surface Mount Packages

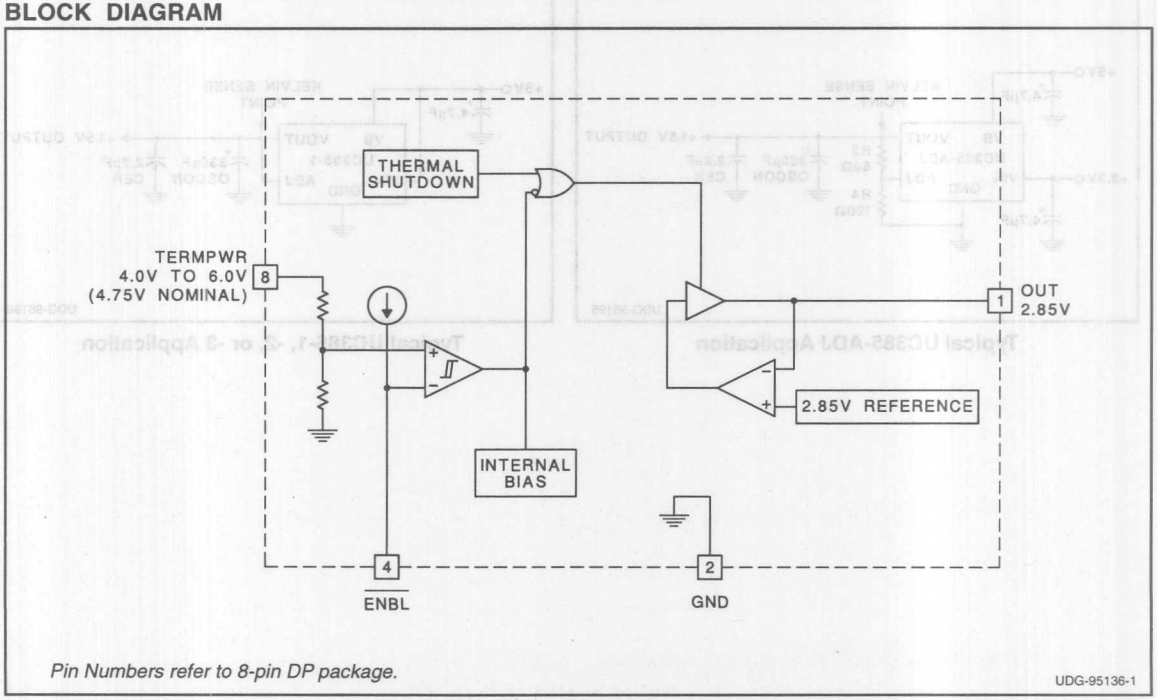
DESCRIPTION

The UC560 provides current for up to 27 lines of active termination for a SCSI (Small Computers Systems Interface) parallel bus. The SCSI standard requires active termination at both ends of the cable. The UC560 is based on the UC5603 and UC5613 SCSI Active Terminators. It uses the voltage regulator and internal logic circuits of those parts, but has no termination circuits. The UC560 provides greater source current drive capability compared to the UC5603 and UC5613.

The UC560 sink current maintains regulation with all active-negation drivers negated. It provides a disconnect feature which disables the regulator to greatly reduce standby power. Internal circuit trimming is utilized for a 1.4% tolerance output voltage. Other features include thermal shutdown and current limit for short circuit conditions.

The UC560 is available in low thermal resistance versions of the industry standard 8-pin power SOIC, 5-pin TO-220 and 5-pin TO-263.

BLOCK DIAGRAM



Pin Numbers refer to 8-pin DP package.

UDG-95136-1

ABSOLUTE MAXIMUM RATINGS

TERMPWR Voltage 7V
ENBL Voltage ..... –0.3V to TERMPWR + 0.3V
Regulator Output Current 1.4A
Power Dissipation 2.5W
Storage Temperature ..... –65°C to +150°C
Junction Temperature ..... –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

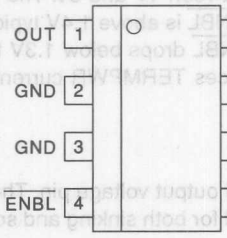
Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

RECOMMENDED OPERATING CONDITIONS

TERMPWR Voltage ..... 4.0V to 6.0V
ENBL Voltage ..... 0V to TERMPWR

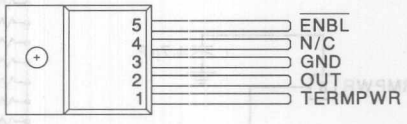
CONNECTION DIAGRAMS

SOIC-8 (Top View)
DP Package



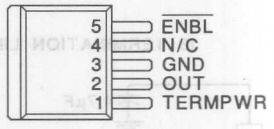
Note: Pins 2,3,6, and 7 are heat sinking pins. Pin 2 is the connect point for electrical ground.

5-Pin TO-220 (Top View)
T Package



Note: TAB is ground.

5-Pin TO-263 (Top View)
TD Package



Note: TAB is ground.

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, T_A = 0°C to 70°C, TERMPWR = 4.75V, $\overline{ENBL}$ = 0V, C_{OUT} = 4.7µF, $C_{TERMPWR}$ = 4.7µF, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current Section					
TERMPWR Supply Current	No Load		16	22	mA
	I_{OUT} = –700mA		710	750	mA
Power Down Mode	$\overline{ENBL}$ = 2.0V		100	140	µA
Regulator Section					
Regulator Output Voltage	25°C, No Load	2.81	2.85	2.89	V
Load Regulation	I_{OUT} = 300mA to –750mA (Note 2)		25	30	mV
Line Regulation	TERMPWR = 4.0V to 6.0V, No Load (Note 2)		10	20	mV
Dropout Voltage	I_{OUT} = –750mA, V_{OUT} = 2.75V		0.9	1.2	V
Short Circuit Current	V_{OUT} = 0.0V	–0.85	–1.3		A
Sinking Current	V_{OUT} = 3.5V		500	600	mA
	$\overline{ENBL}$ = 2.0V, V_{OUT} = 3.0V		1	2	mA
Thermal Shutdown	(Note 1)		170		°C
Thermal Shutdown Hysteresis	(Note 1)		10		°C
Shutdown Section					
$\overline{ENBL}$ Threshold		1.1	1.4	1.7	V
Threshold Hysteresis			100		mV
$\overline{ENBL}$ Output Current			–10	–15	µA

Note 1: Guaranteed by design. Not 100% tested in production.
Note 2: Tested at a constant junction temperature by low duty cycle pulse testing.

PIN DESCRIPTIONS

ENBL: Enable Bar pin. The $\overline{\text{ENBL}}$ function is active low, and the pin will source 10µA typically when at ground and TERMPWR is between 4V and 6V. The part will go into disable mode if $\overline{\text{ENBL}}$ is above 1.4V typical, and will turn back on when $\overline{\text{ENBL}}$ drops below 1.3V typical. The part also greatly reduces TERMPWR current when disabled (100µA typical).

GND: Ground pin.

OUT: 2.85V regulated output voltage pin. The part is internally current limited for both sinking and sourcing current to prevent damage. When the part is in disabled mode ($\overline{\text{ENBL}} \geq 1.4$V typical), the output goes to 0V with no external supply source on OUT. The part will sink current, though, if there is an external supply voltage applied to OUT when in disabled mode. For best perfomance, a 4.7µF low ESR capacitor is recommended.

TERMPWR: Supply voltage pin. The pin should be decoupled with at least a 2.2µF low ESR output capacitor. For best perfomance, a 4.7µF low ESR capacitor is recommended. Lead lengths should be kept at a minimum.

APPLICATIONS INFORMATION

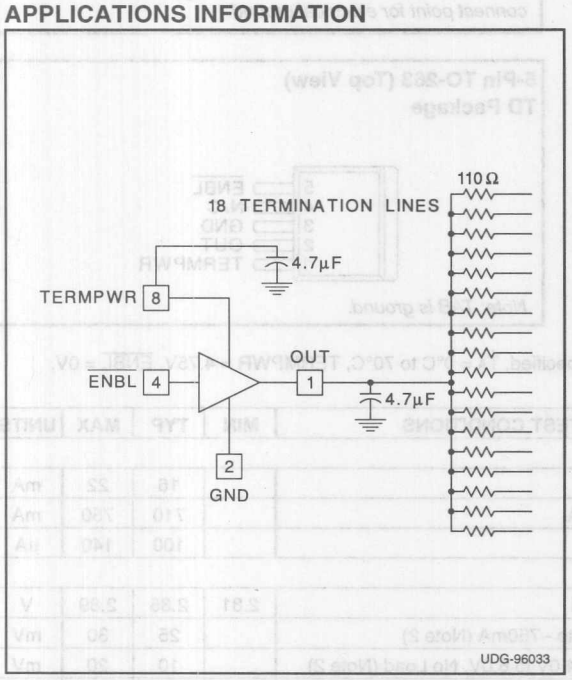


Figure 1. Typical SCSI Bus Configuration Utilizing UC560 Device

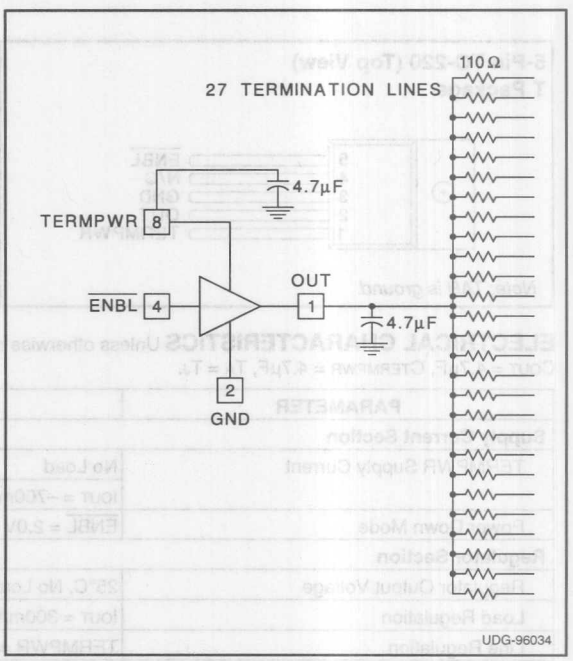
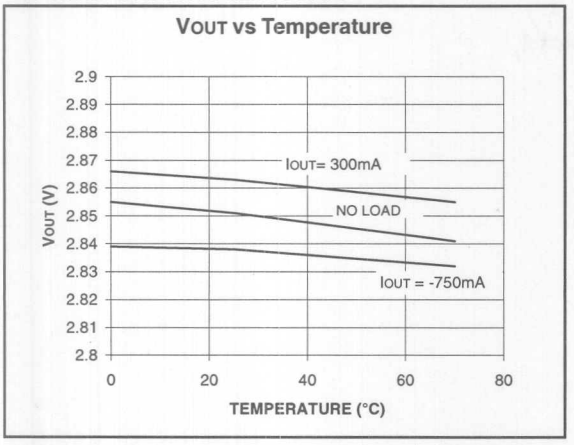
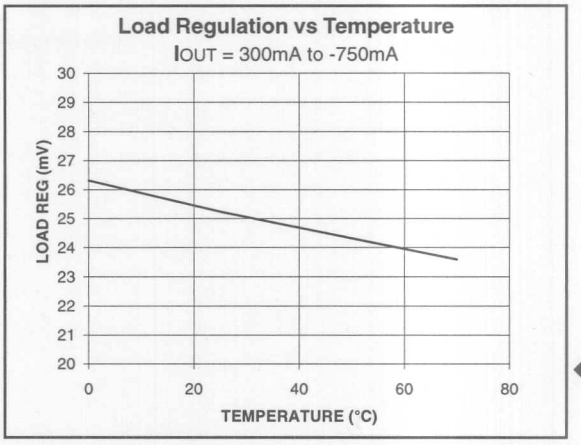
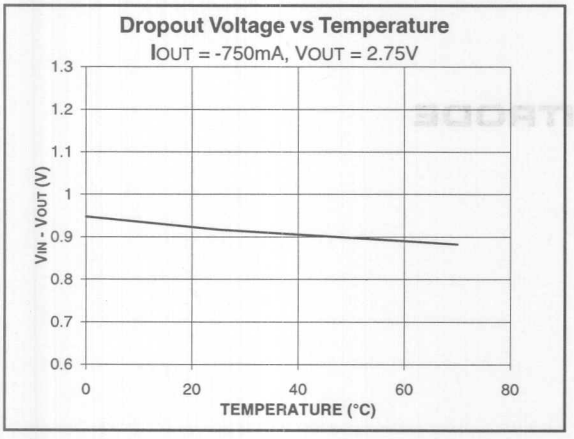


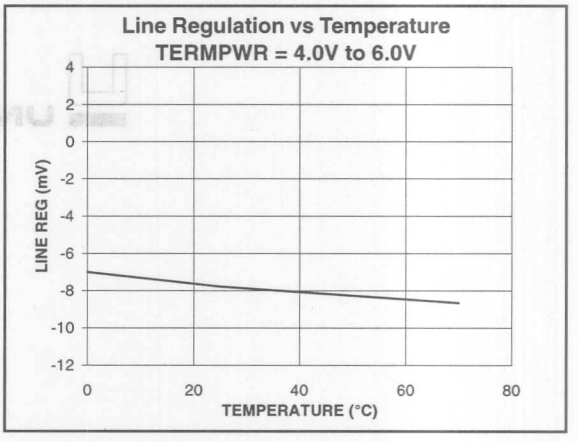
Figure 2. Typical Wide SCSI Bus Configuration Utilizing UC560 Device

TYPICAL CHARACTERISTICS









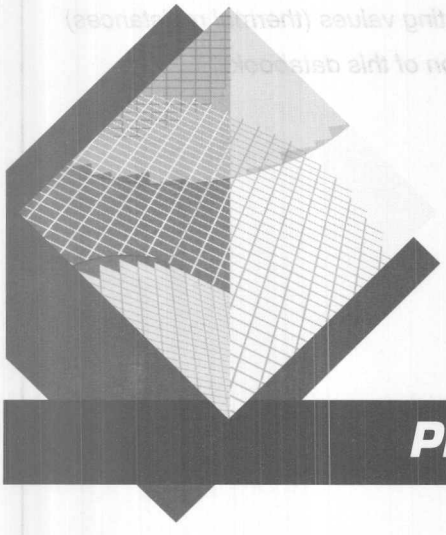
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Consult Applications Handbook for available applications/design notes.

Datasheets in this section are organized in numeric order using the commercial part number.



PFC Controllers

5

Packaging Note:

- *Values listed for recommended lead soldering time and temperature apply to ceramic thru-hole components only. Please consult the Packaging Section of this databook for recommendations on plastic SMD board attach processing.*

- *Unless otherwise noted, thermal resistance values listed on individual data sheets are for the device as it operates in a plastic thru-hole package. Results for other packaging options can be inferred by scaling the package rating values (thermal resistances) presented in the Packaging Section of this databook.*

Power Factor Correction Circuits

Power Factor Correction Products	UNITRODE PART NUMBER				
	UC3852	UC3853	UC3854	UC3854A	UC3854B
Soft Switching	ZCT				
Maximum Practical Operating Frequency	Variable	125kHz	200kHz	200kHz	200kHz
Current Error Amplifier Bandwidth	N/A	1MHz	800kHz	5MHz	5MHz
Average Current Mode		Y	Y	Y	Y
Worldwide AC Input Voltage Operation		Y	Y	Y	Y
Output Drive	0.5A	1A	1A	1A	1A
Startup Current	1mA	0.25mA	1.5mA	0.3mA	0.3mA
Undervoltage Lockout	16.3V/11.5V	11.5V/9.5V	16V/10V	16V/10V	10.5V/10V
Overvoltage Protection		Y			
Enable Input			Y	Y	Y
Multiplier/Divider Feedforward	N/A	Y	Y	Y	Y
Special Features	8-Pin	8-Pin			
Application/Design Note	U-132	U-159	DN-39E, DN-41, U-134	DN-44, DN-66	DN-44, DN-66

Power Factor Correction Products (cont'd)	UNITRODE PART NUMBER			
	UC3855A	UC3855B	UCC3857+	UCC3858+
Soft Switching	ZVT	ZVT	ZCT	
Maximum Practical Operating Frequency	500kHz	500kHz	500kHz	500kHz
Current Error Amplifier Bandwidth	5MHz	5MHz	5MHz	5MHz
Average Current Mode	Y	Y	Y	Y
Worldwide AC Input Voltage Operation	Y	Y	Y	Y
Output Drive	1.5A	1.5A	1A	0.5A
Startup Current	0.15mA	0.15mA	0.06mA	0.1mA
Undervoltage Lockout	16V/10V	10.5V/10V	13.8V/10V	13.8V/10V
Overvoltage Protection	Y	Y		Y
Enable Input	Y	Y		Y
Multiplier/Divider Feedforward	Y	Y	Y	Y
Special Features	Current Synthesizer	Current Synthesizer	Isolated Output	Improved Efficiency at Light Load
Application/Design Note	DN-66, U-153	DN-66, U-153		

+ New Product

Soft Switching	ZCT				
Maximum Practical Operating Frequency	Variable	125kHz	200kHz	200kHz	200kHz
Current Error Amplifier Bandwidth	MIA	1MHz	800kHz	5MHz	5MHz
Average Current Mode		Y	Y	Y	Y
Worldwide AC Input Voltage Operation		Y	Y	Y	Y
Output Drive	0.5A	1A	1A	1A	1A
Startup Current	1mA	0.25mA	1.5mA	0.3mA	0.3mA
Undervoltage Lockout	10.3V/11.5V	11.5V/9.5V	18V/10V	18V/10V	10.5V/10V
Overvoltage Protection			Y		
Enable Input				Y	Y
Multiplier/Divider Feedforward	MIA	Y	Y	Y	Y
Special Features		3-Pin			
Application/Design Note	U-132	U-158	DN-94_2, DN-41, U-134	DN-94_DK-59	DN-94_DN-99

UNITRODE

Soft Switching	ZVT	ZVT	ZCT	
Maximum Practical Operating Frequency	500kHz	500kHz	500kHz	500kHz
Current Error Amplifier Bandwidth	5MHz	5MHz	5MHz	5MHz
Average Current Mode	Y	Y	Y	Y
Worldwide AC Input Voltage Operation	Y	Y	Y	Y
Output Drive	1.0A	1.5A	1A	0.5A
Startup Current	0.15mA	0.15mA	0.09mA	0.1mA
Undervoltage Lockout	10V/10V	10.5V/10V	13.8V/10V	13.8V/10V
Overvoltage Protection	Y	Y		Y
Enable Input	Y	Y		Y
Multiplier/Divider Feedforward	Y	Y	Y	Y
Special Features	Current Synthesizer	Current Synthesizer	Isolated Output	Improved Efficiency at Light Load
Application/Design Note	DN-86, U-153	DN-86, U-153		

* New Product

High Power-Factor Preregulator

FEATURES

- Low-Cost Power Factor Correction
- Power Factor Greater Than 0.99
- Few External Parts Required
- Controlled On-Time Boost PWM
- Zero-Current Switching
- Limited Peak Current
- Min and Max Frequency Limits
- Starting Current Less Than 1mA
- High-Current FET Drive Output
- Under-Voltage Lockout

DESCRIPTION

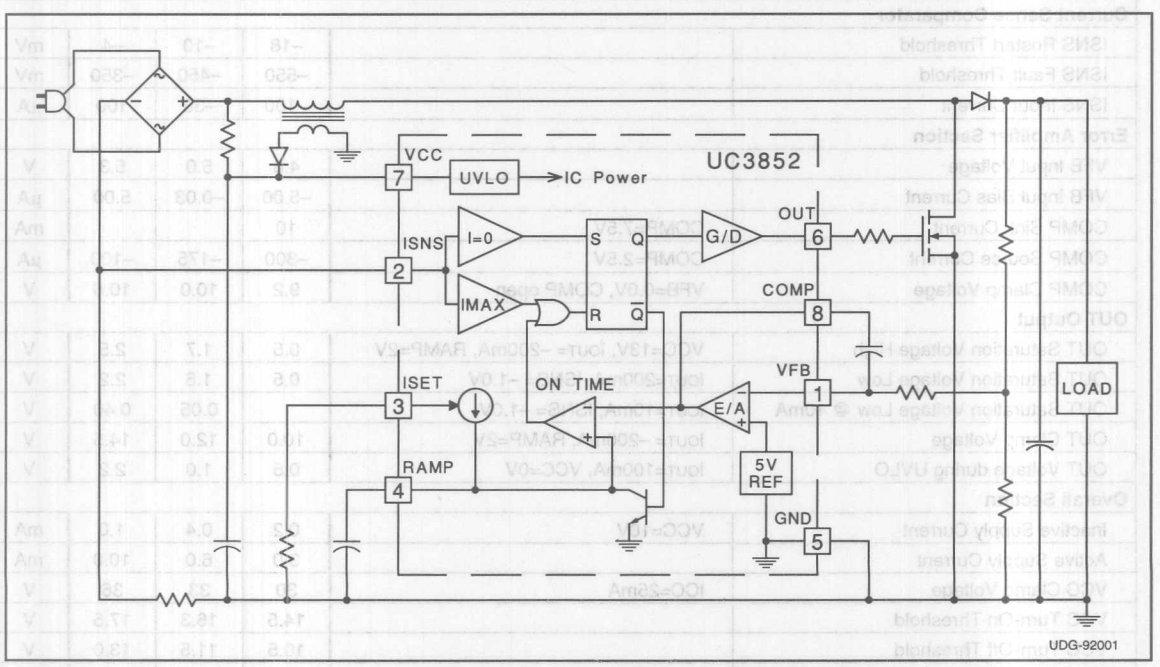
The UC1852 provides a low-cost solution to active power-factor correction (PFC) for systems that would otherwise draw high peak current pulses from AC power lines. This circuit implements zero-current switched boost conversion, producing sinusoidal input currents with a minimum of external components, while keeping peak current substantially below that of fully-discontinuous converters.

The UC1852 provides controlled switch on-time to regulate the output bulk DC voltage, an off-time defined by the boost inductor, and a zero-current sensing circuit to reactivate the switch cycle. Even though switching frequency varies with both load and instantaneous line voltage, it can be maintained within a reasonable range to minimize noise generation.

While allowing higher peak switch currents than continuous PFCs such as the UC1854, this device offers less external circuitry and smaller inductors, yet better performance and easier line-noise filtering than discontinuous current PFCs with no sacrifice in complexity or cost. The ability to obtain a power factor in excess of 0.99 makes the UC1852 an optimum choice for low-cost applications in the 50 to 500 watt power range. Protection features of these devices include under-voltage lockout, output clamping, peak-current limiting, and maximum-frequency clamping.

The UC1852 family is available in 8-pin plastic and ceramic dual in-line packages, and in the 8-pin small outline IC package (SOIC). The UC1852 is specified for operation from -55°C to +125°C, the UC2852 is specified for operation from -40°C to +85°C, and the UC3852 is specified for operation from 0°C to +70°C.

TYPICAL APPLICATION



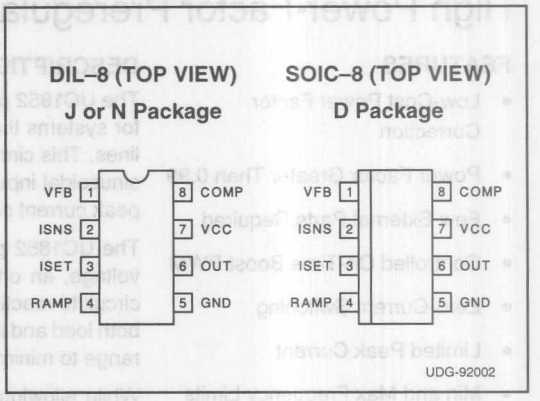
10/94

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Low-impedance Source) 30.0V
Supply Current (High-impedance Source) 30.0mA
OUT Current, Peak ..... ±1.0A
OUT Energy, Capacitive Load 5.0µJ
Input Voltage, ISNS ..... ±5.0V
Input Voltage, VFB ..... –0.3V to +10.0V
COMP Current ..... ±10.0mA
ISET Current ..... –10.0mA
Power Dissipation at Ta≤25°C (Note 3) 1.0W
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) ..... +300°C

Note 1: All voltages with respect to GND (Pin 1).
Note 2: All currents are positive into the specified terminal.
Note 3: Refers to DIL-8 Package. Consult Packaging Section of Unitrode Integrated Circuits databook for thermal limitations and considerations of package.

CONNECTION DIAGRAM

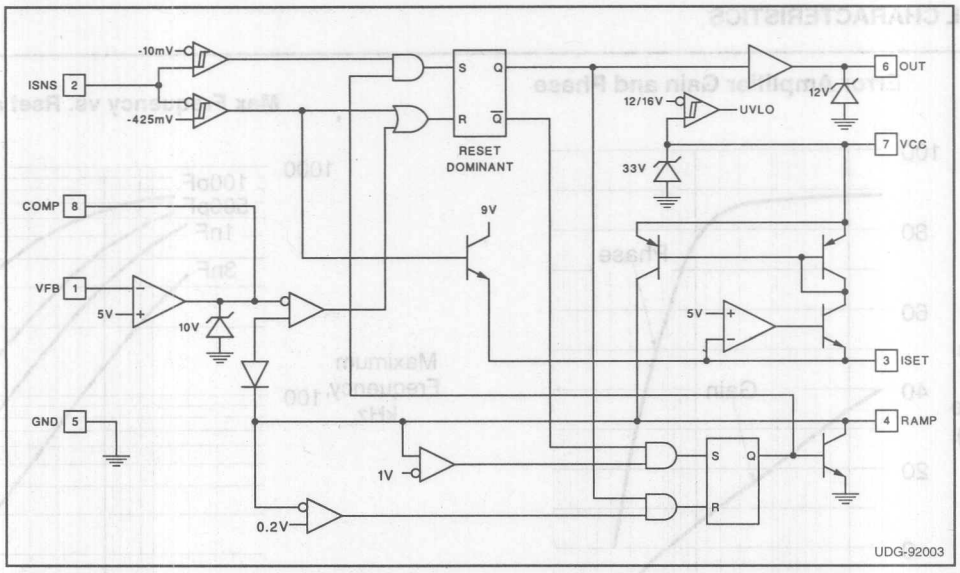


ELECTRICAL CHARACTERISTICS

Unless otherwise stated, VCC=24V, ISET=50kΩ to GND, RAMP=1nF to GND, ISNS=–0.1V, VFB connected to COMP, no load on OUT, –55°C<Ta<+125°C for the UC1852, –40°C<Ta<+85°C for the UC2852, and 0°C<Ta<+70°C for the UC3852, and Ta=Tj.

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Timer Section					
ISET Voltage		4.5	5.0	5.5	V
RAMP Charge Current	RAMP=2.5V	88	98	108	µA
RAMP Discharge Current	ISNS= –1.0V, RAMP=1.0V	12	28	50	mA
RAMP Saturation Voltage	ISNS= –1.0V, I_{RAMP}=100µA		0.006	0.200	V
RAMP Threshold - Maximum Frequency	VFB=10V, COMP open	0.92	1.02	1.12	V
RAMP Threshold - PWM Comparator		3.9	4.3	4.8	V
Current Sense Comparator					
ISNS Restart Threshold		–18	–10	–4	mV
ISNS Fault Threshold		–550	–450	–350	mV
ISNS Input Current		–100	–30	100	µA
Error Amplifier Section					
VFB Input Voltage		4.6	5.0	5.3	V
VFB Input Bias Current		–5.00	–0.03	5.00	µA
COMP Sink Current	COMP=7.5V	10			mA
COMP Source Current	COMP=2.5V	–300	–175	–100	µA
COMP Clamp Voltage	VFB=0.0V, COMP open	9.2	10.0	10.6	V
OUT Output					
OUT Saturation Voltage High	VCC=13V, I_{OUT}= –200mA, RAMP=2V	0.5	1.7	2.5	V
OUT Saturation Voltage Low	I_{OUT}=200mA, ISNS= –1.0V	0.5	1.6	2.2	V
OUT Saturation Voltage Low @ 10mA	I_{OUT}=10mA, ISNS= –1.0V		0.05	0.40	V
OUT Clamp Voltage	I_{OUT}= –200mA, RAMP=2V	10.0	12.0	14.5	V
OUT Voltage during UVLO	I_{OUT}=100mA, VCC=0V	0.5	1.0	2.2	V
Overall Section					
Inactive Supply Current	VCC=10V	0.2	0.4	1.0	mA
Active Supply Current		3.0	6.0	10.0	mA
VCC Clamp Voltage	ICC=25mA	30	33	36	V
VCC Turn-On Threshold		14.5	16.3	17.5	V
VCC Turn-Off Threshold		10.5	11.5	13.0	V
VCC Threshold Hysteresis		3	5	7	V

DETAILED BLOCK DIAGRAM



PIN DESCRIPTIONS

COMP: COMP is the output of the error amplifier and the input of the PWM comparator. To limit PWM on-time, this pin is clamped to approximately 10V. To implement soft start, the COMP pin can be pulled low and ramped up with a PNP transistor, a capacitor, and a resistor.

GND: Ground for all functions is through this pin.

ISET: The dominant function is of this pin is to program RAMP charging current. RAMP charging current is approximately 5V divided by the external resistor placed from ISET to ground. Resistors in the range of 10kΩ to 50kΩ are recommended, producing currents in the range of 100μA to 500μA.

A second function of ISET is as reference output. The ISET pin is normally regulated to 5V ±10%. It is critical that this pin only see the loading of the RAMP programming resistor, but a high input-impedance comparator or amplifier may be connected to this pin or to a tap on the RAMP programming resistor if required.

The third function of the ISET pin is as a FAULT output. In the event of an over-current fault, the ISET pin is forced to approximately 9V by the fault comparator. This can be used to trip an external protection circuit which can disable the load or start a fault restart cycle.

ISNS: This input to the zero and over current comparators is specially built to allow operation over a ±5V dynamic range. In noisy systems or systems with very high Q inductors, it is desirable to filter the signal entering the ISNS input to prevent premature restart or fault cycles. For best accuracy, ISNS should be connected to a current sense resistor through no more than 200 ohms.

OUT: The output of a high-current power driver capable of driving the gate of a power MOSFET with peak currents exceeding ±500mA. To prevent damage to the power MOSFET, the OUT pin is internally driven by a 12V supply. However, lead inductance between the OUT pin and the load can cause overshoot and ringing. External current boost transistors will increase this overshoot and ringing. If there is any significant distance between the IC and the MOSFET, external clamp diodes and/or series damping resistors may be required. OUT is actively held low when the VCC is below the UVLO threshold.

RAMP: A controlled on-time PWM requires a timer whose time can be modulated by an external voltage. The timer current is programmed by a resistor from ISET to GND. A capacitor from RAMP to GND sets the on time in conjunction with the voltage on COMP. Recommended values for the timer capacitors are between 100pF and 1nF.

VCC: VCC is the logic and control power connection for this device. VCC current is the sum of active device supply current and the average OUT current. Knowing the maximum operating frequency and the MOSFET gate charge (Qg), average OUT current can be estimated by:

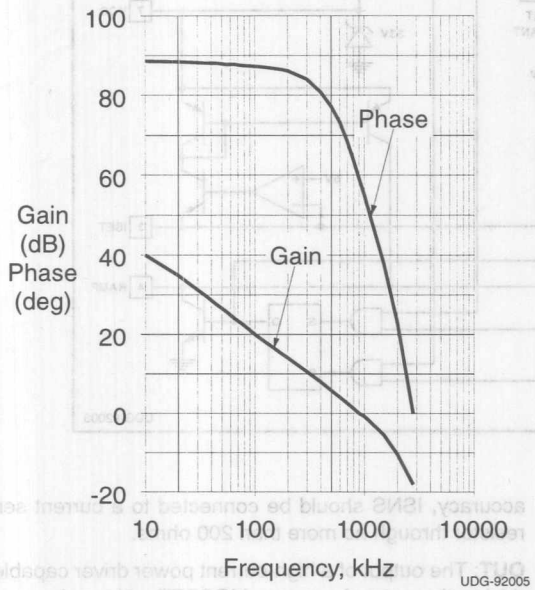
$$I_{OUT} = Q_g \times F$$

To prevent noise problems, bypass VCC to GND with both a ceramic and an electrolytic capacitor.

VFB: VFB is the error amplifier inverting input. This input serves as both the voltage sense input to the error amplifier

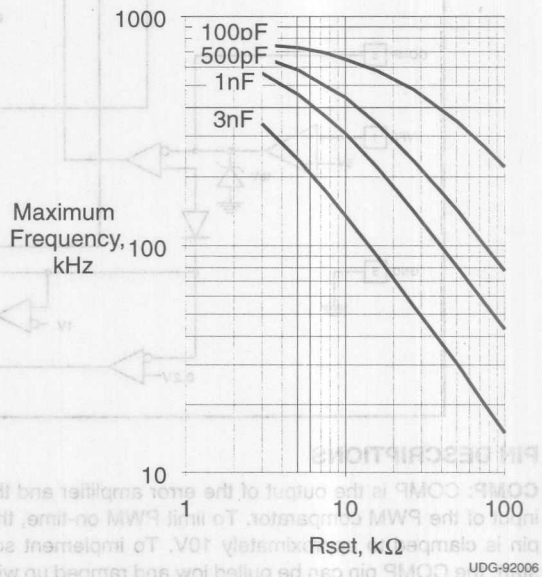
TYPICAL CHARACTERISTICS

Error Amplifier Gain and Phase



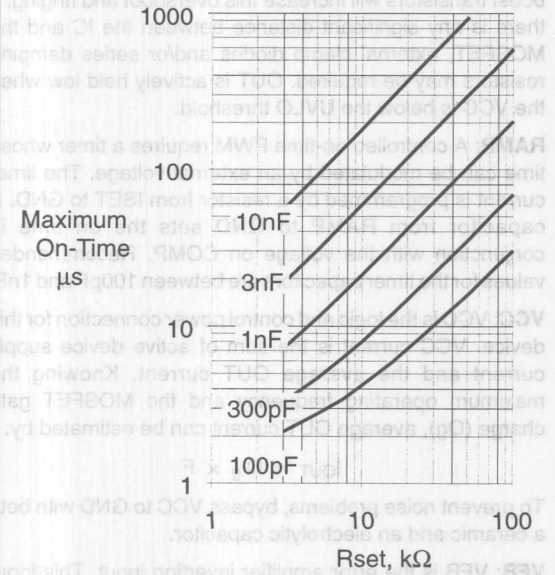
UDG-92005

Max Frequency vs. Rset and Ct



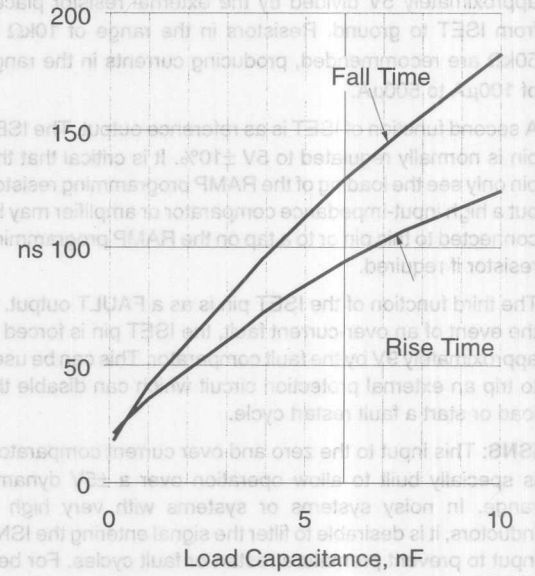
UDG-92006

Max On-Time vs. Rset and Ct



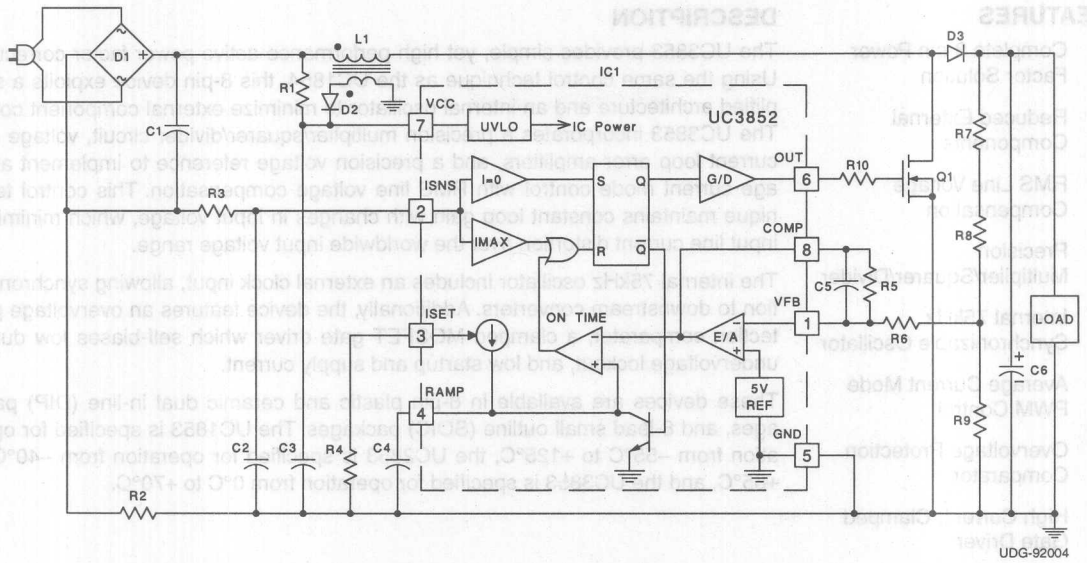
UDG-92007

OUT Rise and Fall Time



UDG-92008

APPLICATION INFORMATION: A 100 Watt Power Factor Preregulator



This circuit demonstrates a complete power factor preregulator based on the UC3852. This preregulator will supply up to 100 watts at 400VDC and exhibit power factor greater than 0.995 with less than 10% total harmonic distortion. Operating input range is 90V to 160V RMS at 50Hz to 60Hz.

This design is intentionally simple, yet fully functional. The UC3852 can also be used in designs featuring soft start, over-voltage protection, wide power-line voltage operation, and fault latching. For more information on applying the UC3852, refer to Unitrode Application Note U–132.

PARTS LIST

C1	0.47µF/250VAC X2 Class Polyester	Q1	IRF830 4.5A/500V 1.5Ω Power FET
C2	1nF/16V Ceramic	L1	680µH (Renco RL3792 with 10 Turn 24 AWG Secondary)
C3	68µF/35V Aluminum Electrolytic	R1	150kΩ, ¼W
C4	180pF/16V Ceramic	R2	0.2Ω, ½W Carbon Composition
C5	0.1µF/16V Polyester or Ceramic	R3	10Ω, ¼W
C6	82µF/450V Aluminum Electrolytic	R4	13.3kΩ, ¼W
D1	2A/500V Bridge Rectifier (Collmer KBPC106 or Powertex MB11A02V60)	R5	1MΩ, ¼W
D2	100mA/50V Switching Diode (1N4148)	R6	20kΩ, ¼W
D3	2A/500V 250ns Recovery-Time Rectifier (Motorola MR856)	R7	200kΩ, ½W
IC1	UC3852N Power Factor Controller IC	R8	200kΩ, ½W

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UNITRODE

UC1853
UC2853
UC3853
PRELIMINARY

High Power Factor Preregulator

FEATURES

- Complete 8-pin Power Factor Solution
- Reduced External Components
- RMS Line Voltage Compensation
- Precision Multiplier/Squarer/Divider
- Internal 75kHz Synchronizable Oscillator
- Average Current Mode PWM Control
- Overvoltage Protection Comparator
- High Current, Clamped Gate Driver

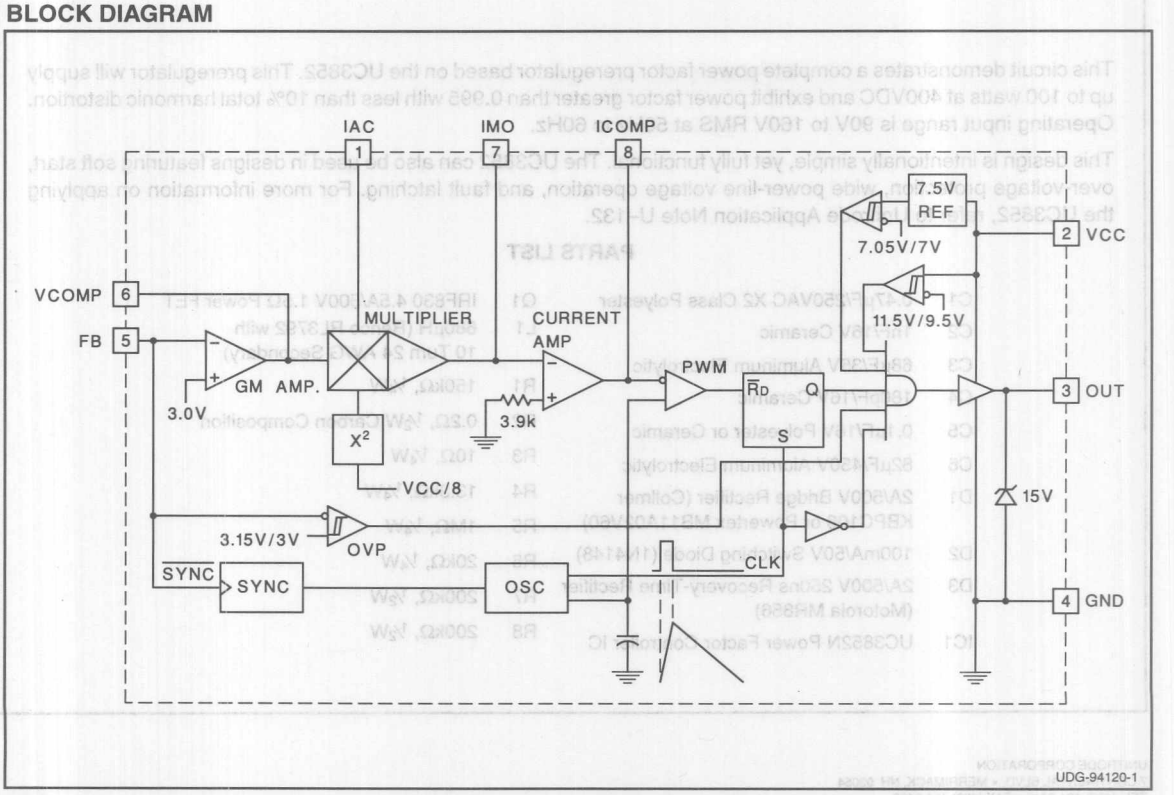
DESCRIPTION

The UC3853 provides simple, yet high performance active power factor correction. Using the same control technique as the UC1854, this 8-pin device exploits a simplified architecture and an internal oscillator to minimize external component count. The UC3853 incorporates a precision multiplier/squarer/divider circuit, voltage and current loop error amplifiers, and a precision voltage reference to implement average current mode control with RMS line voltage compensation. This control technique maintains constant loop gain with changes in input voltage, which minimizes input line current distortion over the worldwide input voltage range.

The internal 75kHz oscillator includes an external clock input, allowing synchronization to downstream converters. Additionally, the device features an overvoltage protection comparator, a clamped MOSFET gate driver which self-biases low during undervoltage lockout, and low startup and supply current.

These devices are available in 8-pin plastic and ceramic dual in-line (DIP) packages, and 8-lead small outline (SOIC) packages. The UC1853 is specified for operation from –55°C to +125°C, the UC2853 is specified for operation from –40°C to +85°C, and the UC3853 is specified for operation from 0°C to +70°C.

BLOCK DIAGRAM



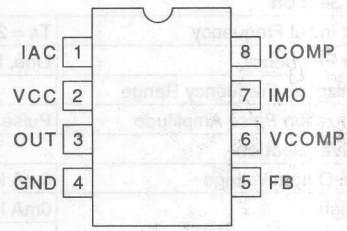
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ABSOLUTE MAXIMUM RATINGS

Supply Voltage (VDD) 40V
Output Drive Current,
Continuous 0.125A
Peak 0.5A
IAC Maximum Input Current 1mA
IMO Maximum Output Current . . . . . .–2mA
FB Maximum Input Voltage 5V
VCOMP Maximum Voltage 6.2V
ICOMP Sourcing Current . . . . . .Self-Limiting
ICOMP Sinking Current 20mA
Storage Temperature . . . . . .–65°C to +150°C
Junction Temperature . . . . . .–55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . .+300°C
All voltages with respect to GND. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

DIL-8, SOIC-8 (Top View)
J or N, D Packages



ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these parameters apply for T_A = –55°C to +125°C for the UC1853; –25°C to +85°C for the 2853; and 0°C to +70°C for the UC3853; VCC = 16V, V_{FB} = 3V, IAC = 100µA, V_{VCOMP} = 3.75V, V_{ICOMP} = 3V, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Undervoltage Lockout Section					
V_{IN} Turn-on Threshold	V_{VCOMP}, V_{ICOMP} Open		11.5		V
V_{IN} Turn-off Threshold			9.5		V
Supply Current Section					
I_{IN} Startup	VCC = 8V, IAC = 100µA; V_{VCOMP}, V_{ICOMP} Open		250	500	µA
I_{IN}	IAC = 0µA, V_{ICOMP} = 0V		10		mA
Voltage Loop Error Amplifier Section					
Transconductance			485		µmho
Input Voltage			3		V
AVOL	V_{VCOMP} = 1V - 4V		60		dB
Output Sink Current	V_{FB} = 3.2V, V_{VCOMP} = 3.75V		50		µA
Output Source Current	V_{FB} = 2.8V, V_{VCOMP} = 3.75V		–50		µA
Output Voltage High			6		V
Output Voltage Low			0.6		V
Current Loop Error Amplifier Section					
Offset Voltage		0		6	mV
GBW	F_{IN} = 100kHz, 20mV p-p		1		MHz
Voltage Gain	V_{ICOMP} = 1V - 4V		70		dB
Sink Current	V_{IMO} = 100mV, V_{ICOMP} = 3V	1			mA
Source Current	V_{IMO} = –0.1V, V_{ICOMP} = 3V		–150		µA
Output High	I_{ICOMP} = –50µA		6.8		V
Output Low	I_{ICOMP} = 50µA		0.3		V
PWM Modulator Gain	V_{ICOMP} = 2V - 3V (Note 1)		20		%/V
Multiplier Section					
Output Current – IAC Limited	VCC = 11V, V_{VCOMP} = 6V	–230	–200	–170	µA
Output Current – Zero	IAC = 0µA	–2	–0.2	2	µA
Output Current – Power Limited	VCC = 12V, V_{VCOMP} = 5.5V	–236	–178	–168	µA
Output Current	VCC = 12V, V_{VCOMP} = 2V		–22		µA
	VCC = 12V, V_{VCOMP} = 5V		–156		µA
	VCC = 40V, V_{VCOMP} = 2V		–2		µA
	VCC = 40V, V_{VCOMP} = 5V		–14		µA
Multiplier Gain Constant	VCC = 12V, V_{VCOMP} = 5.5V (Note 2)	–1.05	–0.9	–0.75	V^{-2}

ELECTRICAL CHARACTERISTICS (cont.) Unless otherwise stated, these parameters apply for T_A = –55°C to +125°C for the UC1853; –25°C to +85°C for the 2853; and 0°C to +70°C for the UC3853; VCC = 16V, V_{FB} = 3V, IAC = 100µA, V_{VCOMP} = 3.75V, V_{ICOMP} = 3V, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator Section					
Oscillator Initial Frequency	T_A = 25°C	67.5	75	82.5	kHz
Oscillator Frequency	Line, Load, Temperature	56	75	94	kHz
Synchronization Frequency Range				100	kHz
Synchronization Pulse Amplitude	Pulse slew rate = 100V/µsec (Note 3)		2		V
Output Driver Section					
Maximum Output Voltage	0mA load, VCC = 20V	13	15	17.5	V
Output High	0mA load, VCC = 12V, ref. to VCC	-2.5	-1.7		V
	–50mA load, VCC = 12V, ref. to VCC	–3	–2.2		V
Output Low (Device Inactive)	VCC = 0V, 20mA load (Sinking)		0.9	2.0	V
Output Low (Device Active)	50mA load (Sinking)		0.5	1	V
OUT Rise Time	1nF from OUT to GND		55		ns
OUT Fall Time	1nF from OUT to GND		35		ns
OUT Maximum Duty Cycle	V_{ICOMP} = 0V		93		%
OVP Comparator Section					
Threshold Voltage		3.06	3.15	3.3	V
Hysteresis			80		mV

Note 1: PWM modulator gain = $\frac{\Delta Duty\ Cycle}{\Delta V_{ICOMP}}$

Note 2: Gain constant (K) = $\frac{IAC \bullet (VCOMP - 1.5V)}{IMO \bullet VCC \bullet \frac{VCC}{64}}$, *VCC = 12V.*

Note 3: Synchronization is accomplished with a falling edge of 2V magnitude and 100V/µsec slew rate.

PIN DESCRIPTIONS

FB: Voltage Amplifier Inverting Input, Overvoltage Comparator Input, Sync Input. This pin serves three functions. FB accepts a fraction of the power factor corrected output voltage through a voltage divider, and is nominally regulated to 3V. FB voltages 5% greater than nominal will trip the overvoltage comparator, and shut down the output stage until the output voltage drops 5%. The internal oscillator can be synchronized through FB by injecting a 2V clock signal though a capacitor. To prevent false tripping of the overvoltage comparator, the clock signal must have a fast falling edge, but a slow rising edge. See the Applications section for recommended synchronization circuits.

GND: Ground. All voltages are measured with respect to GND. The VCC bypass capacitor should be connected to ground as close to the GND pin as possible.

IAC: AC Waveform Input. This input provides voltage waveform information to the multiplier. The current loop will try to produce a current waveform with the same shape as the IAC signal. IAC is a low impedance input, nominally at 2V, which accepts a current proportional to the input voltage. Connect a resistor from the rectified input line to IAC which will conduct 500µA at maximum line voltage.

IMO: Multiplier Output and Current Sense Inverting Input. The output of the multiplier and the inverting input of the current amplifier are connected together at IMO. Avoid bringing this input below –0.5V to prevent the internal protection diode from conducting. The multiplier output is a current, making this a summing node and allowing a differential current error amplifier configuration to reject ground noise. The input resistance at this node should be 3.9k to minimize input bias current induced offset voltage. See the Applications section for the recommended circuit configuration.

OUT: Gate Driver Output. OUT provides high current gate drive for the external power MOSFET. A 15V clamp prevents excessive MOSFET gate-to-source voltage so that the UC3853 can be operated with VCC and high as 40V. A series gate resistor of at least 5 ohms should be used to minimize clamp voltage overshoot. In addition, a Schottky diode such as a 1N5818 connected between OUT and GND may be necessary to prevent parasitic substrate diode conduction.

PIN DESCRIPTIONS (cont.)

ICOMP: Current Loop Error Amplifier Output. The current loop error amplifier is a conventional operational amplifier with a 150µA current source class A output stage. Compensate the current loop by placing an impedance between ICOMP and IMO. This output can swing above the oscillator peak voltage, allowing zero duty cycle when necessary.

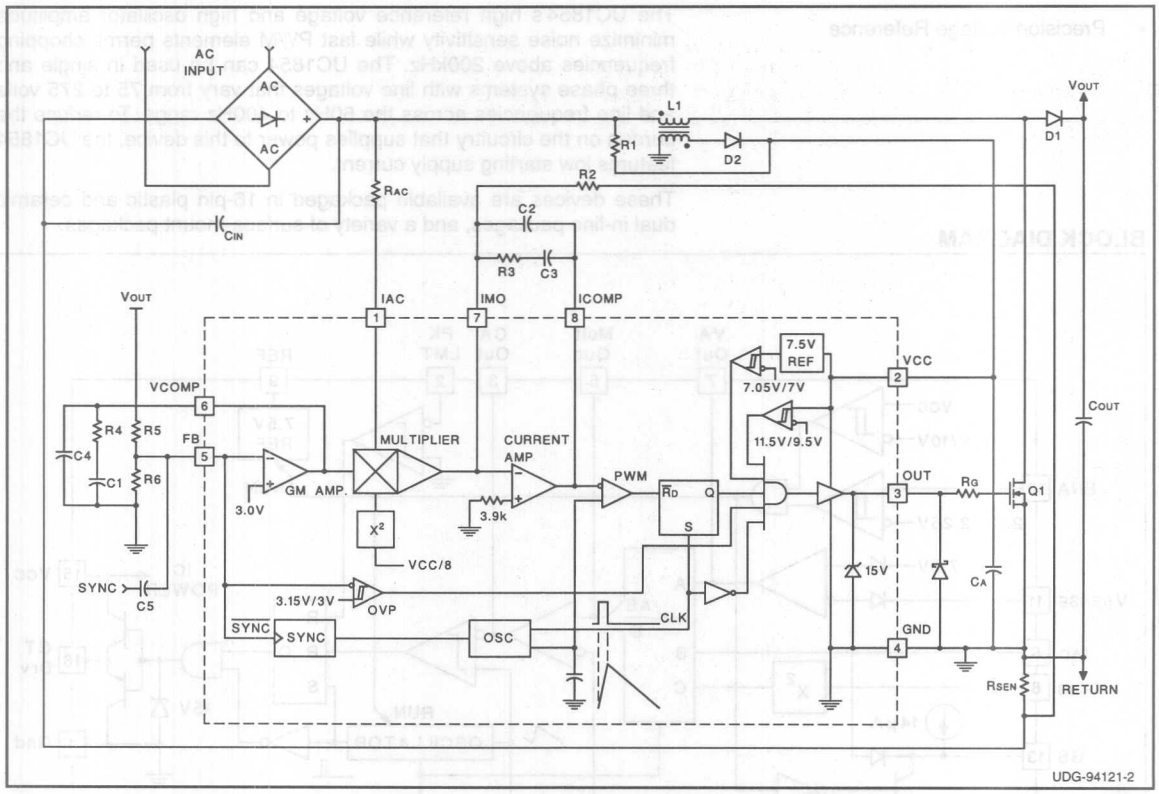
VCC: Input Supply Voltage. This pin serves two functions. It supplies power to the chip, and an input voltage level signal to the squarer circuit. When this input is connected to a DC voltage proportional to the AC input RMS voltage, the voltage loop gain is reduced by

$$\frac{64}{Vcc^2}.$$

This configuration maintains constant loop gain. The UC3853 input voltage range extends from 12V to 40V, allowing an AC supply voltage range in excess of 85VAC to 265VAC. Bypass VCC with at least a 0.1µF ceramic capacitor to ensure proper operation. See the Applications section for the recommended circuit configuration.

VCOMP: Voltage Loop Error Amplifier Output. The voltage loop error amplifier is a transconductance type operational amplifier. A feedback impedance between VCOMP and FB for loop compensation must be avoided to maintain proper operation of the overvoltage protection comparator. Instead, compensate the voltage loop with an impedance between VCOMP and GND. When VCOMP is below 1.5V, the multiplier output current is zero.

UC3853 TYPICAL APPLICATION



UDG-94121-2

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

UNITRODE

UC1854
UC2854
UC3854

High Power Factor Preregulator

FEATURES

- Control Boost PWM to 0.99 Power Factor
- Limit Line Current Distortion To <5%
- World-Wide Operation Without Switches
- Feed-Forward Line Regulation
- Average Current-Mode Control
- Low Noise Sensitivity
- Low Start-Up Supply Current
- Fixed-Frequency PWM Drive
- Low-Offset Analog Multiplier/Divider
- 1A Totem-Pole Gate Driver
- Precision Voltage Reference

DESCRIPTION

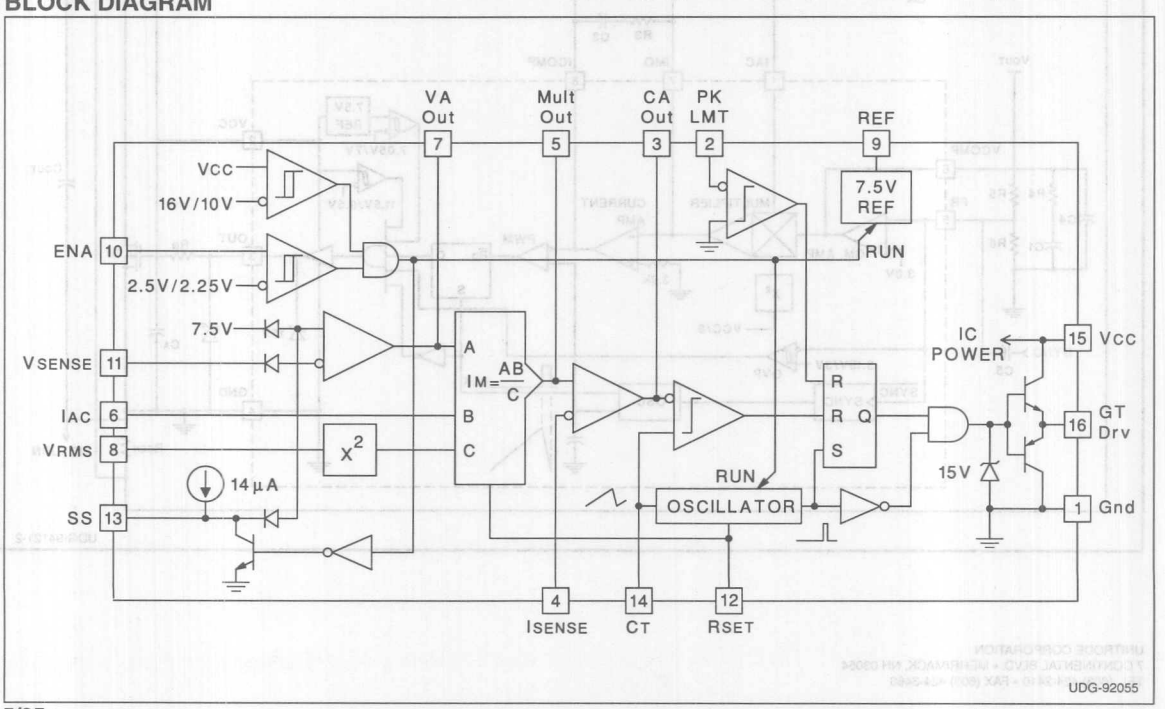
The UC1854 provides active power factor correction for power systems that otherwise would draw non-sinusoidal current from sinusoidal power lines. This device implements all the control functions necessary to build a power supply capable of optimally using available power-line current while minimizing line-current distortion. To do this, the UC1854 contains a voltage amplifier, an analog multiplier/divider, a current amplifier, and a fixed-frequency PWM. In addition, the UC1854 contains a power MOSFET compatible gate driver, 7.5V reference, line anticipator, load-enable comparator, low-supply detector, and over-current comparator.

The UC1854 uses average current-mode control to accomplish fixed-frequency current control with stability and low distortion. Unlike peak current-mode, average current control accurately maintains sinusoidal line current without slope compensation and with minimal response to noise transients.

The UC1854's high reference voltage and high oscillator amplitude minimize noise sensitivity while fast PWM elements permit chopping frequencies above 200kHz. The UC1854 can be used in single and three phase systems with line voltages that vary from 75 to 275 volts and line frequencies across the 50Hz to 400Hz range. To reduce the burden on the circuitry that supplies power to this device, the UC1854 features low starting supply current.

These devices are available packaged in 16-pin plastic and ceramic dual in-line packages, and a variety of surface-mount packages.

BLOCK DIAGRAM



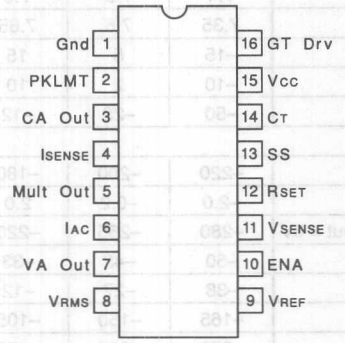
ABSOLUTE MAXIMUM RATINGS

Supply Voltage Vcc 35V
GT Drv Current, Continuous 0.5A
GT Drv Current, 50% Duty Cycle 1.5A
Input Voltage, VSENSE, VRMS 11V
Input Voltage, ISENSE, Mult Out 11V
Input Voltage, PKLMT 5V
Input Current, RSET, IAC, PKLMT, ENA 10mA
Power Dissipation 1W
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) ..... +300°C

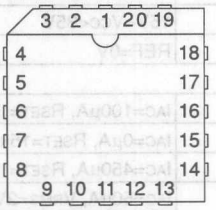
Note 1: All voltages with respect to Gnd (Pin 1).
Note 2: All currents are positive into the specified terminal.
Note 3: ENA input is internally clamped to approximately 14V.
Note 4: Consult Unitrode Integrated Circuits databook for information regarding thermal specifications and limitations of packages.

CONNECTION DIAGRAMS

DIL–16 & SOIC-16
(Top View)
J, N & DW Packages



PLCC-20 & LCC-20
(Top View)
Q & L Packages



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
Gnd	2
PKLMT	3
CA Out	4
ISENSE	5
N/C	6
Mult Out	7
IAC	8
VA Out	9
VRMS	10
N/C	11
VREF	12
ENA	13
VSENSE	14
RSET	15
N/C	16
SS	17
CT	18
VCC	19
GT Drv	20

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, VCC=18V, RSET=15k to ground, CT=1.5nF to ground, PKLMT=1V, ENA=7.5V, VRMS=1.5V, IAC=100µA, ISENSE=0V, CA Out=3.5V, VA Out=5V, VSENSE=7.5V, no load on SS, CA Out, VA Out, REF, GT Drv, –55°C<TA<125°C for the UC1854, –40°C<TA<85°C for the UC2854, and 0°C<TA<70°C for the UC3854, and TA=TJ.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
OVERALL					
Supply Current, Off	ENA=0V		1.5	2.0	mA
Supply Current, On			10	16	mA
Vcc Turn-On Threshold		14.5	16	17.5	V
Vcc Turn-Off Threshold		9	10	11	V
ENA Threshold, Rising		2.4	2.55	2.7	V
ENA Threshold Hysteresis		0.2	0.25	0.3	V
ENA Input Current	ENA=0V	–5.0	–0.2	5.0	µA
VRMS Input Current	VRMS=5V	–1.0	–.01	1.0	µA
VOLTAGE AMPLIFIER					
Voltage Amp Offset Voltage	VA Out=5V	–8		8	mV
VSENSE Bias Current		–500	–25	500	nA
Voltage Amp Gain		70	100		dB
Voltage Amp Output Swing			0.5 to 5.8		V
Voltage Amp Short Circuit Current	VA Out=0V	–36	–20	–5	mA
SS Current	SS=2.5V	–20	–14	–6	µA

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, V_{CC}=18V, R_{SET}=15k to ground, C_T=1.5nF to ground, PKLMT=1V, ENA=7.5V, V_{RMS}=1.5V, I_{AC}=100µA, I_{SENSE}=0V, CA Out=3.5V, VA Out=5V, V_{SENSE}=7.5V, no load on SS, CA Out, VA Out, REF, GT Drv, $-55^{\circ}C<T_A<125^{\circ}C$ for the UC1854, $-40^{\circ}C<T_A<85^{\circ}C$ for the UC2854, and $0^{\circ}C<T_A<70^{\circ}C$ for the UC3854, and $T_A=T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
CURRENT AMPLIFIER					
Current Amp Offset Voltage		–4		4	mV
I_{SENSE} Bias Current		–500	–120	500	nA
Input Range, I_{SENSE}, Mult Out		–0.3 to 2.5			V
Current Amp Gain		80	110		dB
Current Amp Output Swing			0.5 to 16		V
Current Amp Short Circuit Current	CA Out=0V	–36	–20	–5	mA
Current Amp Gain-BW Product	$T_A=25^{\circ}C$ (Note 6)	400	800		kHz
REFERENCE					
Reference Output Voltage	I_{REF}=0mA, $T_A=25^{\circ}C$	7.4	7.5	7.6	V
	I_{REF}=0mA, Over Temp.	7.35	7.5	7.65	V
V_{REF} Load Regulation	$-10mA<I_{REF}<0mA$	–15	5	15	mV
V_{REF} Line Regulation	$15V<V_{CC}<35V$	–10	2	10	mV
V_{REF} Short Circuit Current	REF=0V	–50	–28	–12	mA
MULTIPLIER					
Mult Out Current I_{AC} Limited	I_{AC}=100µA, R_{SET}=10k, V_{RMS}=1.25V	–220	–200	–180	µA
Mult Out Current Zero	I_{AC}=0µA, R_{SET}=15k	–2.0	–0.2	2.0	µA
Mult Out Current R_{SET} Limited	I_{AC}=450µA, R_{SET}=15k, V_{RMS}=1V, VA Out = 6V	–280	–255	–220	µA
Mult Out Current	I_{AC}=50µA, V_{RMS}=2V, VA=4V	–50	–42	–33	µA
	I_{AC}=100µA, V_{RMS}=2V, VA=2V	–38	–27	–12	µA
	I_{AC}=200µA, V_{RMS}=2V, VA=4V	–165	–150	–105	µA
	I_{AC}=300µA, V_{RMS}=1V, VA=2V	–250	–225	–150	µA
	I_{AC}=100µA, V_{RMS}=1V, VA=2V	–95	–80	–60	µA
Multiplier Gain Constant	(Note 5)		–1.0		V
OSCILLATOR					
Oscillator Frequency	R_{SET}=15k	46	55	62	kHz
	R_{SET}=8.2k	86	102	118	kHz
C_T Ramp Peak-to-Valley Amplitude		4.9	5.4	5.9	V
C_T Ramp Valley Voltage		0.8	1.1	1.3	V
GATE DRIVER					
Maximum GT Drv Output Voltage	0mA load on GT Drv, $18V<V_{CC}<35V$	13	14.5	18	V
GT Drv Output Voltage High	–200mA load on GT Drv, V_{CC}=15V	12	12.8		V
GT Drv Output Voltage Low, Off	V_{CC}=0V, 50mA load on GT Drv		0.9	1.5	V
GT Drv Output Voltage Low	200mA load on GT Drv		1.0	2.2	V
	10mA load on GT Drv		0.1	0.4	V
Peak GT Drv Current	10nF from GT Drv to Gnd		1.0		A
GT Drv Rise/Fall Time	1nF from GT Drv to Gnd		35		ns
GT Drv Maximum Duty Cycle	$V_{CA\ Out}$=7V		95		%
CURRENT LIMIT					
PKLMT Offset Voltage		–10		10	mV
PKLMT Input Current	PKLMT=–0.1V	–200	–100		µA
PKLMT to GT Drv Delay	PKLMT falling from 50mV to –50mV		175		ns

Note 5: Multiplier Gain Constant (k) is defined by: $I_{Mult\ Out} = \frac{k \times I_{AC} \times (VA\ Out - 1)}{V_{RMS}^2}$

Note 6: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS (Pin Numbers Refer to DIL Packages)

Gnd (Pin 1) (ground): All voltages are measured with respect to Gnd. Vcc and REF should be bypassed directly to Gnd with an 0.1µF or larger ceramic capacitor. The timing capacitor discharge current also returns to this pin, so the lead from the oscillator timing capacitor to Gnd should also be as short and as direct as possible.

PKLMT (Pin 2) (peak limit): The threshold for PKLMT is 0.0V. Connect this input to the negative voltage on the current sense resistor as shown in Figure 1. Use a resistor to REF to offset the negative current sense signal up to Gnd.

CA Out (Pin 3) (current amplifier output): This is the output of a wide-bandwidth op amp that senses line current and commands the pulse width modulator (PWM) to force the correct current. This output can swing close to Gnd, allowing the PWM to force zero duty cycle when necessary. The current amplifier will remain active even if the IC is disabled. The current amplifier output stage is an NPN emitter follower pull-up and an 8k resistor to ground.

ISENSE (Pin 4) (current sense minus): This is the inverting input to the current amplifier. This input and the non-inverting input Mult Out remain functional down to and below Gnd. Care should be taken to avoid taking these inputs below –0.5V, because they are protected with diodes to Gnd.

Mult Out (Pin 5) (multiplier output and current sense plus): The output of the analog multiplier and the non-inverting input of the current amplifier are connected together at Mult Out. The cautions about taking ISENSE below –0.5V also apply to Mult Out. As the multiplier output is a current, this is a high impedance input similar to ISENSE, so the current amplifier can be configured as a differential amplifier to reject Gnd noise. Figure 1 shows an example of using the current amplifier differentially.

IAC (Pin 6) (input AC current): This input to the analog multiplier is a current. The multiplier is tailored for very low distortion from this current input (IAC) to Mult Out, so this is the only multiplier input that should be used for sensing instantaneous line voltage. The nominal voltage on IAC is 6V, so in addition to a resistor from IAC to rectified 60Hz, connect a resistor from IAC to REF. If the resistor to REF is one fourth of the value of the resistor to the rectifier, then the 6V offset will be cancelled, and the line current will have minimal cross-over distortion.

VA Out (Pin 7) (voltage amplifier output): This is the output of the op amp that regulates output voltage. Like the current amplifier, the voltage amplifier will stay active even if the IC is disabled with either ENA or Vcc. This means that large feedback capacitors across the amplifier will stay charged through momentary disable cycles. Voltage amplifier output levels below 1V will inhibit multiplier output. The voltage amplifier output is internally limited to approximately 5.8V to prevent overshoot. The voltage amplifier output stage is an NPN emitter follower pull-up and an 8k resistor to ground.

VRMS (Pin 8) (RMS line voltage): The output of a boost PWM is proportional to the input voltage, so when the line voltage into a low-bandwidth boost PWM voltage regulator changes, the output will change immediately and slowly recover to the regulated level. For these devices, the VRMS input compensates for line voltage changes if it is connected to a voltage proportional to the RMS input line voltage. For best control, the VRMS voltage should stay between 1.5V and 3.5V.

REF (Pin 9) (voltage reference output): REF is the output of an accurate 7.5V voltage reference. This output is capable of delivering 10mA to peripheral circuitry and is internally short circuit current limited. REF is disabled and will remain at 0V when Vcc is low or when ENA is low. Bypass REF to Gnd with an 0.1µF or larger ceramic capacitor for best stability.

ENA (Pin 10) (enable): ENA is a logic input that will enable the PWM output, voltage reference, and oscillator. ENA also will release the soft start clamp, allowing SS to rise. When unused, connect ENA to a +5V supply or pull ENA high with a 22k resistor. The ENA pin is not intended to be used as a high speed shutdown to the PWM output.

VSENSE (Pin 11) (voltage amplifier inverting input): This is normally connected to a feedback network and to the boost converter output through a divider network.

RSET (Pin 12) (oscillator charging current and multiplier limit set): A resistor from RSET to ground will program oscillator charging current and maximum multiplier output. Multiplier output current will not exceed 3.75V divided by the resistor from RSET to ground.

SS (Pin 13) (soft start): SS will remain at Gnd as long as the IC is disabled or Vcc is too low. SS will pull up to over 8V by an internal 14µA current source when both Vcc becomes valid and the IC is enabled. SS will act as the reference input to the voltage amplifier if SS is below REF. With a large capacitor from SS to Gnd, the reference to the voltage regulating amplifier will rise slowly, and increase the PWM duty cycle slowly. In the event of a disable command or a supply dropout, SS will quickly discharge to ground and disable the PWM.

CT (Pin 14) (oscillator timing capacitor): A capacitor from CT to Gnd will set the PWM oscillator frequency according to this relationship:

$$F = \frac{1.25}{R_{SET} \times C_T}$$

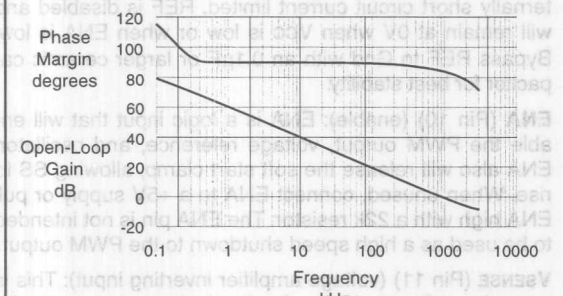
Vcc (Pin 15) (positive supply voltage): Connect Vcc to a stable source of at least 20mA above 17V for normal operation. Also bypass Vcc directly to Gnd to absorb supply current spikes required to charge external MOSFET gate capacitances. To prevent inadequate GT Drv signals, these devices will be inhibited unless Vcc exceeds the upper under-voltage lockout threshold and remains above the lower threshold.

PIN DESCRIPTIONS (cont.)

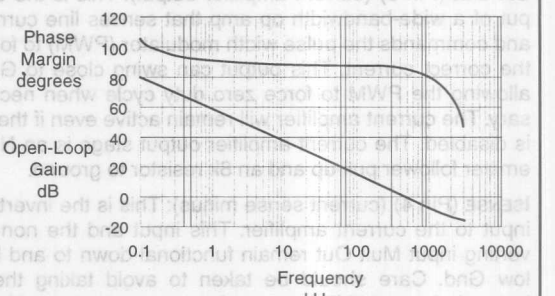
GT Drv (Pin 16) (gate drive): The output of the PWM is a totem pole MOSFET gate driver on GT Drv. This output is internally clamped to 15V so that the IC can be operated with Vcc as high as 35V. Use a series gate resistor of at least 5 ohms to prevent interaction between the gate impedance and the GT Drv output driver that might cause the GT Drv output to overshoot excessively. Some overshoot of the GT Drv output is always expected when driving a capacitive load.

TYPICAL CHARACTERISTICS at $T_A = T_J = 25°C$

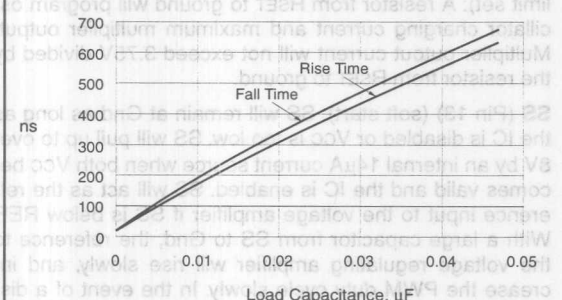
Current Amplifier Gain and Phase vs Frequency



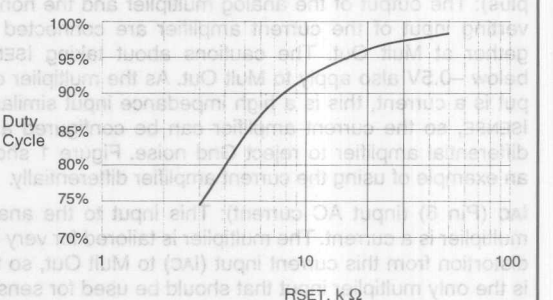
Voltage Amplifier Gain and Phase vs Frequency



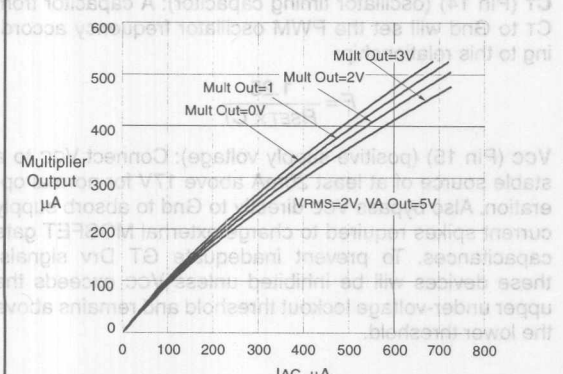
Gate Drive Rise and Fall Time



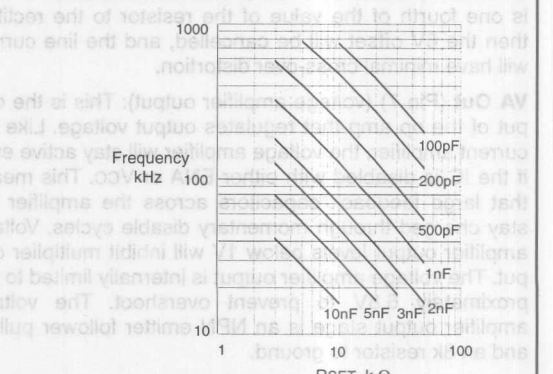
Gate Drive Maximum Duty Cycle



Multiplier Output vs Voltage on Mult

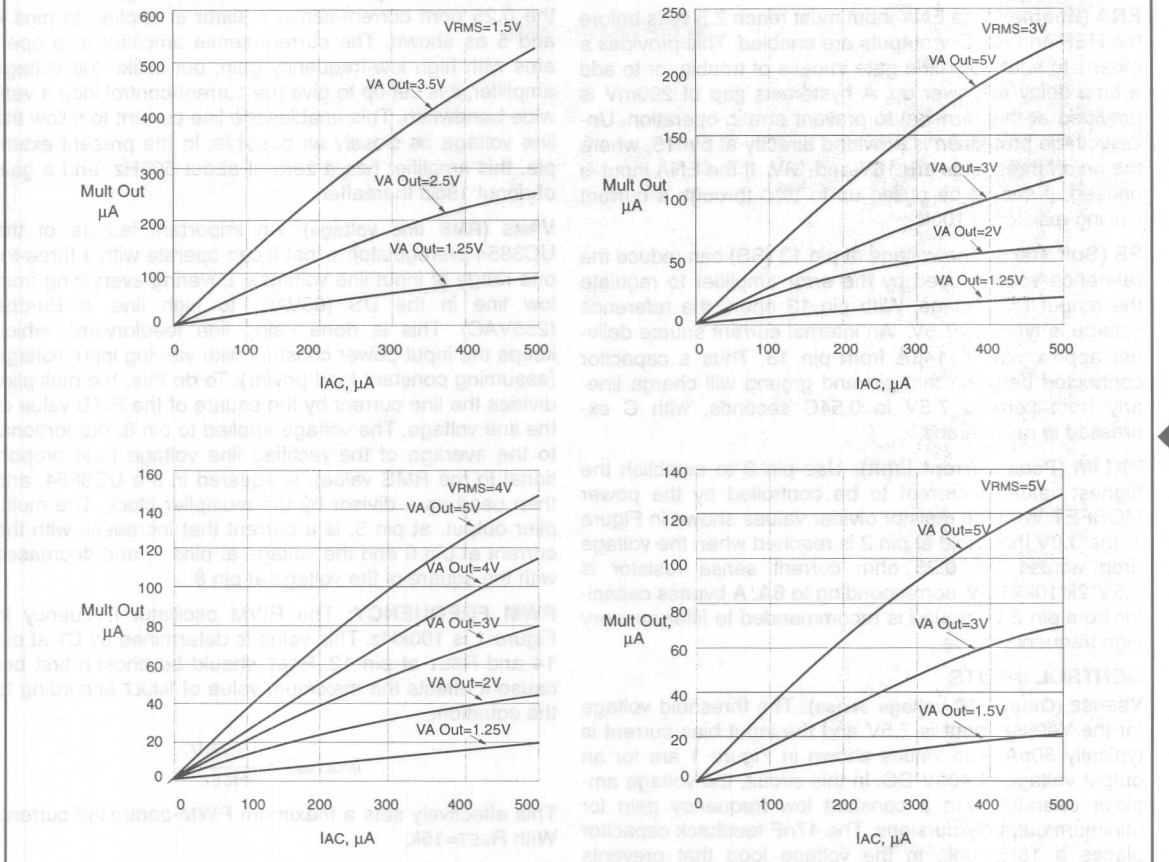


Oscillator Frequency vs RSET and CT



TYPICAL CHARACTERISTICS at $T_A = T_J = 25^oC$ (cont.)

Multiplier Output vs Multiplier Inputs with Mult Out=0V



APPLICATIONS INFORMATION

A 250W PREREGULATOR

The circuit of Figure 1 shows a typical application of the UC3854 as a preregulator with high power factor and efficiency. The assembly consists of two distinct parts, the control circuit centering on the UC3854 and the power section.

The power section is a "boost" converter, with the inductor operating in the continuous mode. In this mode, the duty cycle is dependent on the ratio between input and output voltages; also, the input current has low switching frequency ripple, which means that the line noise is low. Furthermore, the output voltage must be higher than the peak value of the highest expected AC line voltage, and all components must be rated accordingly.

In the control section, the UC3854 provides PWM pulses (GT Drv, Pin 16) to the power MOSFET gate. The duty cycle of this output is simultaneously controlled by four separate inputs to the chip:

INPUT	PIN #	FUNCTION
VSENSE	11	Output DC Voltage
IAC	6	LineVoltage Waveform
ISENSE/Mult Out	4/5	Line Current
VRMS	8	RMS Line Voltage

Additional controls of an auxiliary nature are provided. They are intended to protect the switching power MOSFETS from certain transient conditions, as follows:

INPUT	PIN #	FUNCTION
ENA	10	Start-Up Delay
SS	13	Soft Start
PKLIM	2	Maximum Current Limit

APPLICATIONS INFORMATION (cont.)

PROTECTION INPUTS

ENA (Enable): The ENA input must reach 2.5 volts before the REF and GT Drv outputs are enabled. This provides a means to shut down the gate in case of trouble, or to add a time delay at power up. A hysteresis gap of 200mV is provided at this terminal to prevent erratic operation. Undervoltage protection is provided directly at pin 15, where the on/off thresholds are 16V and 10V. If the ENA input is unused, it should be pulled up to Vcc through a current limiting resistor of 100k.

SS (Soft start): The voltage at pin 13 (SS) can reduce the reference voltage used by the error amplifier to regulate the output DC voltage. With pin 13 open, the reference voltage is typically 7.5V. An internal current source delivers approximately -14μA from pin 13. Thus a capacitor connected between that pin and ground will charge linearly from zero to 7.5V in 0.54C seconds, with C expressed in microfarads.

PKLIM (Peak current limit): Use pin 2 to establish the highest value of current to be controlled by the power MOSFET. With the resistor divider values shown in Figure 1, the 0.0V threshold at pin 2 is reached when the voltage drop across the 0.25 ohm current sense resistor is 7.5V*2k/10k=1.5V, corresponding to 6A. A bypass capacitor from pin 2 to ground is recommended to filter out very high frequency noise.

CONTROL INPUTS

VSENSE (Output DC voltage sense): The threshold voltage for the VSENSE input is 7.5V and the input bias current is typically 50nA. The values shown in Figure 1 are for an output voltage of 400V DC. In this circuit, the voltage amplifier operates with a constant low frequency gain for minimum output excursions. The 47nF feedback capacitor places a 15Hz pole in the voltage loop that prevents 120Hz ripple from propagating to the input current.

IAC (Line waveform): In order to force the line current waveshape to follow the line voltage, a sample of the power line voltage in waveform is introduced at pin 6. This signal is multiplied by the output of the voltage amplifier in the internal multiplier to generate a reference signal for the current control loop.

This input is not a voltage, but a current (hence IAC). It is set up by the 220k and 910k resistive divider (see Figure 1). The voltage at pin 6 is internally held at 6V, and the two resistors are chosen so that the current flowing into pin 6 varies from zero (at each zero crossing) to about 400μA at the peak of the waveshape. The following formulas were used to calculate these resistors:

$$R_{AC} = \frac{V_{pk}}{I_{ACpk}} = \frac{260\,VAC \times \sqrt{2}}{400\mu A} = 910k$$

$$R_{REF} = \frac{R_{AC}}{4} = 220k$$

(where Vpk is the peak line voltage)

ISENSE/Mult Out (Line current): The voltage drop across the 0.25 ohm current-sense resistor is applied to pins 4 and 5 as shown. The current-sense amplifier also operates with high low-frequency gain, but unlike the voltage amplifier, it is set up to give the current-control loop a very wide bandwidth. This enables the line current to follow the line voltage as closely as possible. In the present example, this amplifier has a zero at about 500Hz, and a gain of about 18dB thereafter.

VRMS (RMS line voltage): An important feature of the UC3854 preregulator is that it can operate with a three-to-one range of input line voltages, covering everything from low line in the US (85VAC) to high line in Europe (255VAC). This is done using line feedforward, which keeps the input power constant with varying input voltage (assuming constant load power). To do this, the multiplier divides the line current by the square of the RMS value of the line voltage. The voltage applied to pin 8, proportional to the average of the rectified line voltage (and proportional to the RMS value), is squared in the UC3854, and then used as a divisor by the multiplier block. The multiplier output, at pin 5, is a current that increases with the current at pin 6 and the voltage at pins 7, and decreases with the square of the voltage at pin 8.

PWM FREQUENCY: The PWM oscillator frequency in Figure 1 is 100kHz. This value is determined by CT at pin 14 and RSET at pin 12. RSET should be chosen first because it affects the maximum value of IMULT according to the equation:

$$I_{MULT_{MAX}} = \frac{-3.75V}{R_{SET}}$$

This effectively sets a maximum PWM-controlled current. With RSET=15k,

$$I_{MULT_{MAX}} = \frac{-3.75V}{15k} = -250\mu A$$

Also note that the multiplier output current will never exceed twice IAC.

With the 4k resistor from Mult Out to the 0.25 ohm current sense resistor, the maximum current in the current sense resistor will be

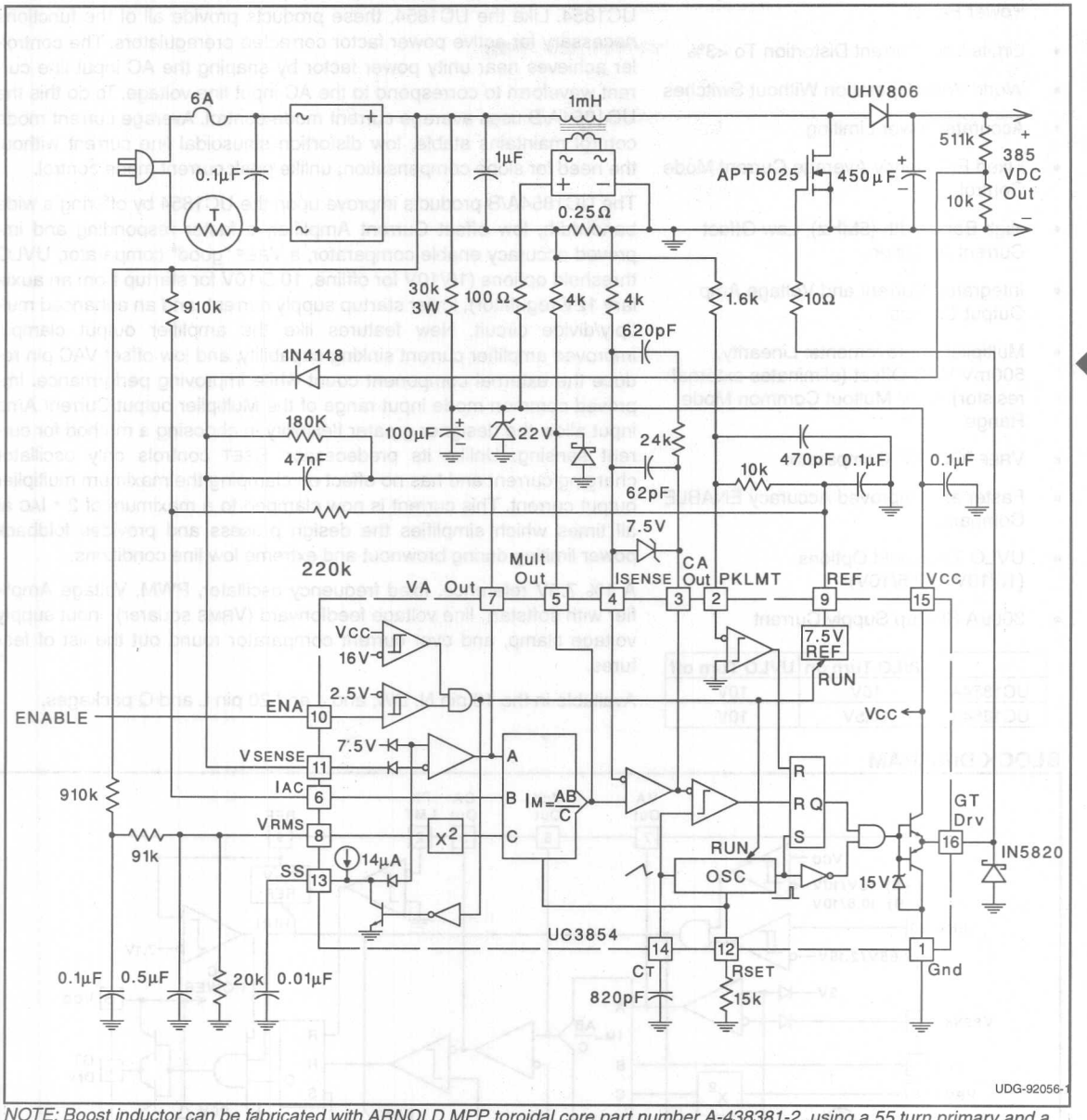
$$I_{MAX} = \frac{-I_{MULT_{MAX}} \times 4k}{0.25\Omega} = -4A$$

Having thus selected RSET, the current sense resistor, and the resistor from Mult Out to the current sense resistor, calculate CT for the desired PWM oscillator frequency from the equation

$$C_T = \frac{1.25}{F \times R_{SET}}$$

FIGURE 1 - Typical Application

This diagram depicts a complete 250 Watt Preregulator. At full load, this preregulator will exhibit a power factor of 0.99 at any power line voltage between 80 and 260 VRMS. This same circuit can be used at higher power levels with minor modifications to the power stage. See Design Note 39B and Application Note U-134 for further details.



NOTE: Boost inductor can be fabricated with ARNOLD MPP toroidal core part number A-438381-2, using a 55 turn primary and a 13 turn secondary.

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UNITRODE

Enhanced High Power Factor Preregulator

FEATURES

- Controls Boost PWM to Near Unity Power Factor
- Limits Line Current Distortion To <3%
- World-Wide Operation Without Switches
- Accurate Power Limiting
- Fixed Frequency Average Current Mode Control
- High Bandwidth (5MHz), Low Offset Current Amplifier
- Integrated Current and Voltage Amp Output Clamps
- Multiplier Improvements: Linearity, 500mV VAC Offset (eliminates external resistor), 0-5V Multout Common Mode Range
- VREF "GOOD" Comparator
- Faster and Improved Accuracy ENABLE Comparator
- UVLO Threshold Options (16/10V / 10.5/10V)
- 300µA Startup Supply Current

	UVLO Turn on	UVLO Turn off
UC1854A	16V	10V
UC1854B	10.5V	10V

DESCRIPTION

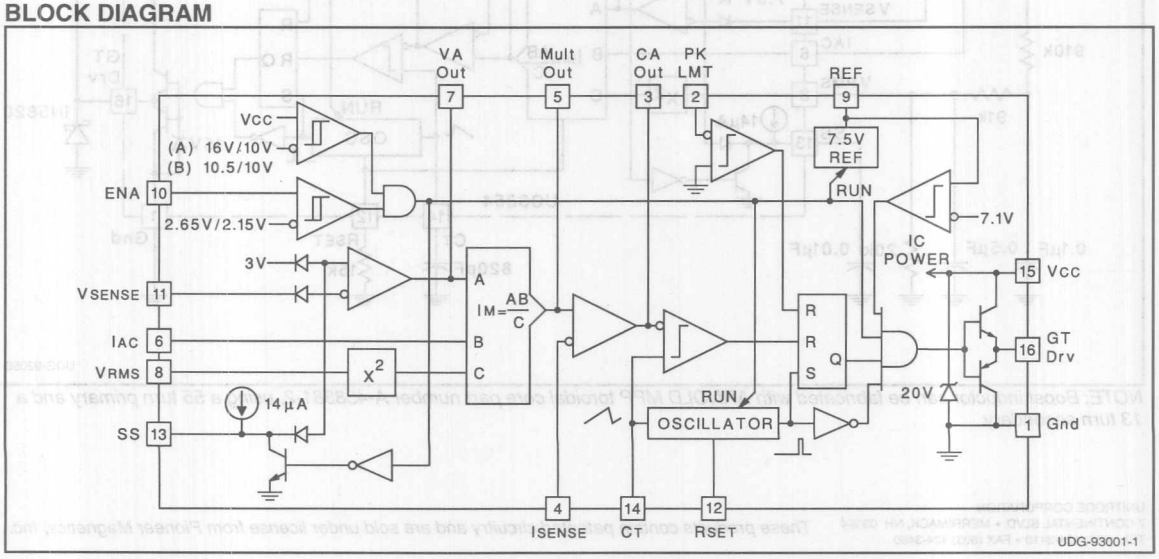
The UC1854A/B products are pin compatible enhanced versions of the UC1854. Like the UC1854, these products provide all of the functions necessary for active power factor corrected preregulators. The controller achieves near unity power factor by shaping the AC input line current waveform to correspond to the AC input line voltage. To do this the UC1854A/B uses average current mode control. Average current mode control maintains stable, low distortion sinusoidal line current without the need for slope compensation, unlike peak current mode control.

The UC1854A/B products improve upon the UC1854 by offering a wide bandwidth, low offset Current Amplifier, a faster responding and improved accuracy enable comparator, a VREF "good" comparator, UVLO threshold options (16/10V for offline, 10.5/10V for startup from an auxiliary 12V regulator), lower startup supply current, and an enhanced multiply/divide circuit. New features like the amplifier output clamps, improved amplifier current sinking capability, and low offset VAC pin reduce the external component count while improving performance. Improved common mode input range of the Multiplier output/Current Amp input allow the designer greater flexibility in choosing a method for current sensing. Unlike its predecessor, RSET controls only oscillator charging current and has no effect on clamping the maximum multiplier output current. This current is now clamped to a maximum of 2 * IAC at all times which simplifies the design process and provides foldback power limiting during brownout and extreme low line conditions.

A 1% 7.5V reference, fixed frequency oscillator, PWM, Voltage Amplifier with softstart, line voltage feedforward (VRMS squarer), input supply voltage clamp, and over current comparator round out the list of features.

Available in the 16 pin N, DW, and J and 20 pin L and Q packages.

BLOCK DIAGRAM



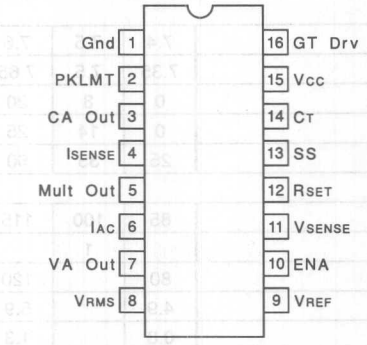
ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{CC} 22V
GT Drv Current, Continuous 0.5A
GT Drv Current, 50% Duty Cycle 1.5A
Input Voltage, V_{SENSE}, V_{RMS} 11V
Input Voltage, I_{SENSE}, Mult Out 11V
Input Voltage, PKLMT 5V
Input Current, R_{SET}, I_{AC}, PKLMT, ENA 10mA
Power Dissipation 1W
Storage Temperature . . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) . . . . . +300°C

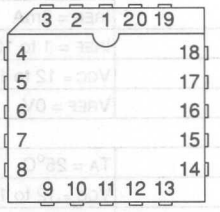
Note 1: All voltages with respect to Gnd (Pin 1).
Note 2: All currents are positive into the specified terminal.
Note 3: ENA imput is internally clamped to approximately 10V.
Note 4: Consult Unitrode Integrated Circuits databook for information regarding thermal specifications and limitations of packages.

CONNECTION DIAGRAMS

DIL–16 & SOIC-16
(Top View)
J, N & DW Packages



PLCC-20 & LCC-20
(Top View)
Q & L Packages



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
Gnd	2
PKLMT	3
CA Out	4
ISENSE	5
N/C	6
Mult Out	7
IAC	8
VA Out	9
VRMS	10
N/C	11
VREF	12
ENA	13
VSENSE	14
RSET	15
N/C	16
SS	17
CT	18
VCC	19
GT Drv	20

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, V_{CC}=18V, R_T=8.2k, C_T=1.5nF, PKLMT=1V, V_{RMS}=1.5V, I_{AC}=100µA, I_{SENSE}=0V, CA Out=3.5V, VA Out=5V, V_{SENSE}=3V, –55°C<T_A<125°C for the UC1854A/B, –40°C<T_A<85°C for the UC2854A/B, and 0°C<T_A<70°C for the UC3854A/B, and T_A=T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
OVERALL					
Supply Current, Off	CAO, VAO = 0V, V_{CC} = UVLO - 0.3V		250	400	µA
Supply Current, On			12	18	mA
V_{CC} Turn-On Threshold	UC1854A		16	17.5	V
	UC1854B		10.5	11.2	V
V_{CC} Turn-Off Threshold	UC1854A / B	9	10		V
V_{CC} Clamp	I(V_{CC}) = I_{CC}(on) + 5mA	18	20	22	V
VOLTAGE AMPLIFIER					
Input Voltage		2.9	3.0	3.1	V
V_{SENSE} Bias Current		–500	–25	500	nA
Open Loop Gain	V_{OUT} = 2 to 5V	70	100		dB
V_{OUT} High	I_{LOAD} = –500µA		6		V
V_{OUT} Low	I_{LOAD} = 500µA		0.3	0.5	V
Output Short Circuit Current	V_{OUT} = 0V		1.5	3.5	mA
Gain Bandwidth Product	Fin = 100kHz, 10mV p-p, (Note 1)		1		mHz

ELECTRICAL CHARACTERISTICS (cont.)

Unless otherwise stated, V_{CC}=18V, R_T=8.2k, C_T=1.5nF, PKLMT=1V, V_{RMS}=1.5V, I_{AC}=100µA, I_{SENSE}=0V, CA Out=3.5V, VA Out=5V, V_{SENSE}=3V, –55°C<T_A<125°C for the UC1854A/B, –40°C<T_A<85°C for the UC2854A/B, and 0°C<T_A<70°C for the UC3854A/B, and T_A=T_J.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
CURRENT AMPLIFIER						
Input Offset Voltage	V_{CM} = 0V	T_A = +25°C	–4		0	mV
		OverTemp	–5.5		0	mV
Input Bias Current(sense)	V_{CM} = 0V		–500		500	nA
Open Loop Gain	V_{CM} = 0V, V_{OUT} = 2 to 6V		80	110		dB
V_{OUT} High	I_{LOAD} = –500µA			8		V
V_{OUT} Low	ILOAD = 500µA			0.3	0.5	V
Output Short Circuit Current	V_{OUT} = 0V			1.5	3.5	mA
Common Mode Range			–0.3		5	V
Gain Bandwidth Product	Fin = 100kHz, 10mV p-p, (Note 1)		3	5		mHz
REFERENCE						
Output Voltage	I_{REF} = 0mA, T_A = 25°C		7.4	7.5	7.6	V
	I_{REF} = 0mA		7.35	7.5	7.65	V
Load Regulation	I_{REF} = 1 to 10mA		0	8	20	mV
Line Regulation	V_{CC} = 12 to 18V		0	14	25	mV
Short Circuit Current	V_{REF} = 0V		25	35	60	mA
OSCILLATOR						
Initial Accuracy	T_A = 25°C		85	100	115	kHz
Voltage Stability	V_{CC} = 12 to 18V			1		%
Total Variation	Line, Temp		80		120	kHz
Ramp Amplitude (p-p)			4.9		5.9	V
Ramp Valley Voltage			0.8		1.3	V
ENABLE / SOFTSTART / CURRENT LIMIT						
Enable Threshold			2.5	2.65	2.8	V
Enable Hysteresis	V_{FAULT} = 2.5V			500	600	mV
Enable Input Bias Current	V_{ENABLE} = 0V			–2	–5	µA
Propagation Delay to Disable	Enable Overdrive = –100mV,(Note 1)			300		ns
SS Charge Current	$V_{SOFTSTART}$ = 2.5V		10	14	24	
PKLMT Offset Voltage			–15		15	mV
PKLMT Input Current	V_{PKLMT} = –0.1V		–200	–100		µA
PKLMT Propagation Delay	(Note 1)			150		ns
MULTIPLIER						
Output Current - I_{AC} Limited	I_{AC}=100µA, V_{RMS} = 1V, R_{SET} = 10k		–220	–200	–170	µA
Output Current - Zero	I_{AC}=0µA, R_{SET} = 10k		–2.0	–0.2	2.0	µA
Output Current - Power Limited	V_{RMS} = 1.5V, Va = 6V		–230	–200	–170	µA
Output Current	V_{RMS} = 1.5V, Va = 2V			–22		µA
	V_{RMS} = 1.5V, Va = 5V			–156		µA
	V_{RMS} = 5V, Va = 2V			–2		µA
	V_{RMS} = 5V, Va = 5V			–14		µA
Gain Constant	(Note 2) V_{RMS} = 1.5V, T_J = 25°C, Va = 6V		–1.1	–1.0	–0.9	A/A

Note 1: Guaranteed by design, not 100% tested in production.

Note 2: Gain constant (K) $= \dfrac{I_{AC} \times (Va - 1.5V)}{V_{RMS}^2 \times I_{MO}}$

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, V_{CC}=18V, R_T=8.2k, C_T=1.5nF, PKLMT=1V, V_{RMS}=1.5V, I_{AC}=100µA, I_{SENSE}=0V, CA Out=3.5V, VA Out=5V, V_{SENSE}=3V, –55°C<T_A<125°C for the UC1854A/B, –40°C<T_A<85°C for the UC2854A/B, and 0°C<T_A<70°C for the UC3854A/B, and T_A=T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
GATE DRIVER					
Output High Voltage	I_{OUT} = –200mA, V_{CC} = 15V	12	12.8		V
Output Low Voltage	I_{OUT} = 200mA		1	2.2	V
	I_{OUT} = 10mA		300	500	mV
Output Low (UVLO)	I_{OUT} = 50mA, V_{CC} = 0V		0.9	1.5	V
Output Rise / Fall Time	C_{LOAD} = 1nF, (Note 1)		35		ns
Output Peak Current	C_{LOAD} = 10nF, (Note 1)		1.0		A

Note 1: Guaranteed by design, not 100% tested in production.

Note 2: Gain constant (K) $= \dfrac{I_{AC} \times (Va - 1.5V)}{V_{RMS}^2 \times I_{MO}}$

FUNCTIONAL DESCRIPTION

The UC1854A/B products were designed as pin compatible upgrades to the industry standard UC1854 active Power Factor correction circuits. The circuit enhancements allow the user to eliminate in most cases several external components currently required to successfully apply the UC1854. In addition, linearity improvements to the Multiply, Square, and Divide circuitry optimizes overall system performance. Detailed descriptions of the circuit enhancements are provided below. For in-depth design applications reference data refer to Unitrode application notes U-134 and DN-44.

MULTIPLY / SQUARE AND DIVIDE

The UC1854A/B Multiplier design maintains the same gain constant (K = –1), as the UC1854. The relationship between the inputs and output current is given as:

$$I_{MO} = I_{AC}(V_{AO} - 1.5V) / K \bullet V_{RMS}^2$$

This is nearly the same as the UC1854, but circuit differences have improved the performance and application.

The first difference is with the I_{AC} input. The UC1854A/B regulates this pin voltage to a nominal 500mV over the full operating temperature range, rather than the 6.0V used on the UC1854. This low offset voltage eliminates the need for a line zero crossing compensating resistor to V_{REF} from I_{AC} that UC1854 designs require. The maximum current at high line into I_{AC} should be limited to 250µA for best performance. Therefore, if V_{AC} (max) = 270V, then R_{AC} = 270(1.414) / 250µA = 1.53MΩ.

The V_{RMS} pin linear operating range is improved with the UC1854A/B as well. The input range for V_{RMS} extends from 0 to 5.5V. Since the UC1854A squaring circuit employs an analog multiplier, rather than a linear approximation, accuracy is improved, and discontinuities are eliminated. The external divider network connected to V_{RMS} should produce 1.5V at low line (85VAC). This will put 4.77V on V_{RMS} at high line (27VAC) which is well within its operating range.

The Voltage Amplifier output forms the third input to the Multiplier and is internally clamped to 6.0V. This eliminates an external zenerclamp often used in UC1854 designs. The offset voltage at this input to the Multiplier has been raised on the UC1854A/B to 1.5V.

The Multiplier output pin, which is also common to the Current Amplifier non-inverting input, has a –0.3V to 5.0V output range,compared to the –0.3 to 2.5V range of the UC1854. This improvement allows the UC1854A/B to be used in applications where the current sense signal amplitude is very large.

VOLTAGE AMPLIFIER

The UC1854A/B Voltage Amplifier design is essentially similar to the UC1854 with two exceptions. The first is with the internal connection. The lower voltage reduces the amount of charge on the compensation capacitor, which provides improved recovery from large signal events, such as line dropouts, or power interruption. It also minimizes the DC current flowing through the feedback. The output of the Voltage amplifier is also changed. In addition to a 6.0V temperature compensated clamp, the output short circuit current has been lowered to 2mA typical, and an active pull down has replaced the passive pulldown of the UC1854.

CURRENT AMPLIFIER

The Current Amplifier for an average current PFC controller needs a low offset voltage in order to minimize AC line current distortion. With this in mind, the UC1854A/B Current Amplifier has improved the input offset voltage from ±4mV to 0 to –3mV. The negative offset of the UC1854A/B guarantees that the PWM circuit will not drive the MOS-

FUNCTIONAL DESCRIPTION (cont.)

FET if the current command is zero (both Current amplifier inputs zero.).Previous designs required an external offset cancellation network to implement this key feature. The bandwidth of the Current Amplifier has been improved as well to 5mHz typical. While this is not generally an issue at 50 or 60Hz inputs, it is essential for 400Hz input avionics applications.

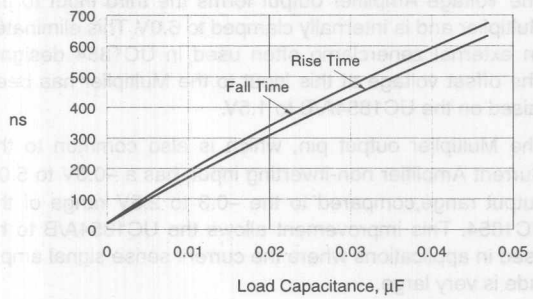
MISCELLANEOUS

Several other important enhancements have been implemented in the UC1854A/B. A Vcc supply voltage clamp at 20V allows the controller to be current fed if desired. The lower startup supply current (250µA typical), substantially reduces the power requirements of an offline startup resistor. The 10.5/10V UVLO option (UC1854B) enables the controller to be powered off of an auxiliary 12V supply.

The VREF "GOOD" comparator guarantees that the MOSFET driver output remains low if the supply or the 7.5V reference are not yet up. This improvement eliminates the need for external Schottky diodes on the PKL and CA+ pins that some UC1854 designs require. The propagation delay of the disable feature has been improved to 300ns typical. This delay was proportional to the size of the VREF capacitor on the UC1854, and is typically several orders of magnitude slower.

TYPICAL CHARACTERISTICS at TA = TJ = 25°C

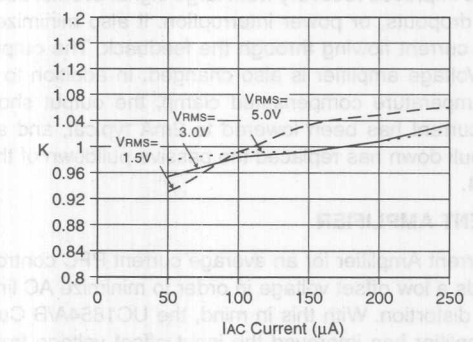
Gate Drive Rise and Fall Time



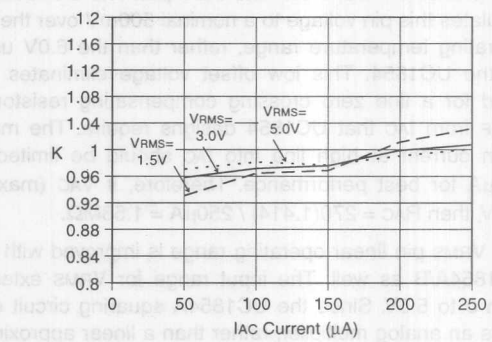
Gate Drive Maximum Duty Cycle



UC1854A/B Multiplier Linearity
VAOUT = 3.5V

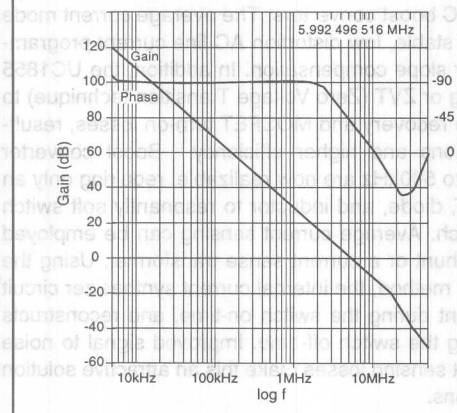


UC1854A/B Multiplier Linearity
VAOUT = 5V

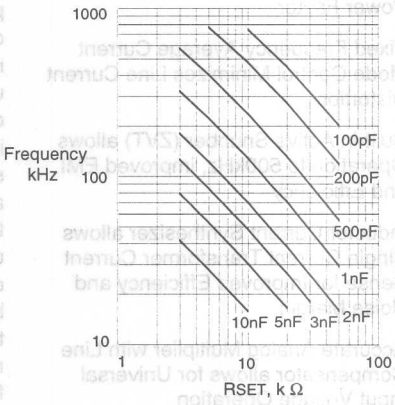


TYPICAL CHARACTERISTICS at $T_A = T_J = 25°C$ (cont.)

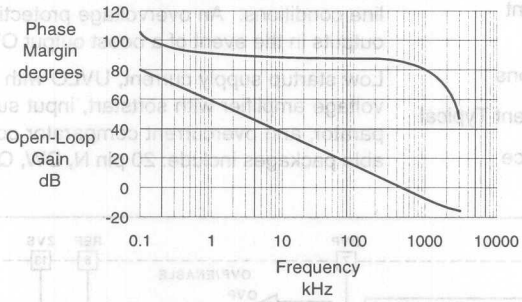
Current Amplifier Frequency Response



Oscillator Frequency vs RSET and CT



Voltage Amplifier Gain and Phase vs Frequency



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UNITRODE

UC1855A/B
UC2855A/B
UC3855A/B

High Performance Power Factor Preregulator

PRELIMINARY

FEATURES

- Controls Boost PWM to Near Unity Power Factor
- Fixed Frequency Average Current Mode Control Minimizes Line Current Distortion
- Built-in Active Snubber (ZVT) allows Operation to 500kHz, improved EMI and Efficiency
- Inductor Current Synthesizer allows Single Current Transformer Current Sense for Improved Efficiency and Noise Margin
- Accurate Analog Multiplier with Line Compensator allows for Universal Input Voltage Operation
- High Bandwidth (5MHz), Low Offset Current Amplifier
- Overvoltage and Overcurrent protection
- Two UVLO Threshold Options
- 150µA Startup Supply Current Typical
- Precision 1% 7.5V Reference

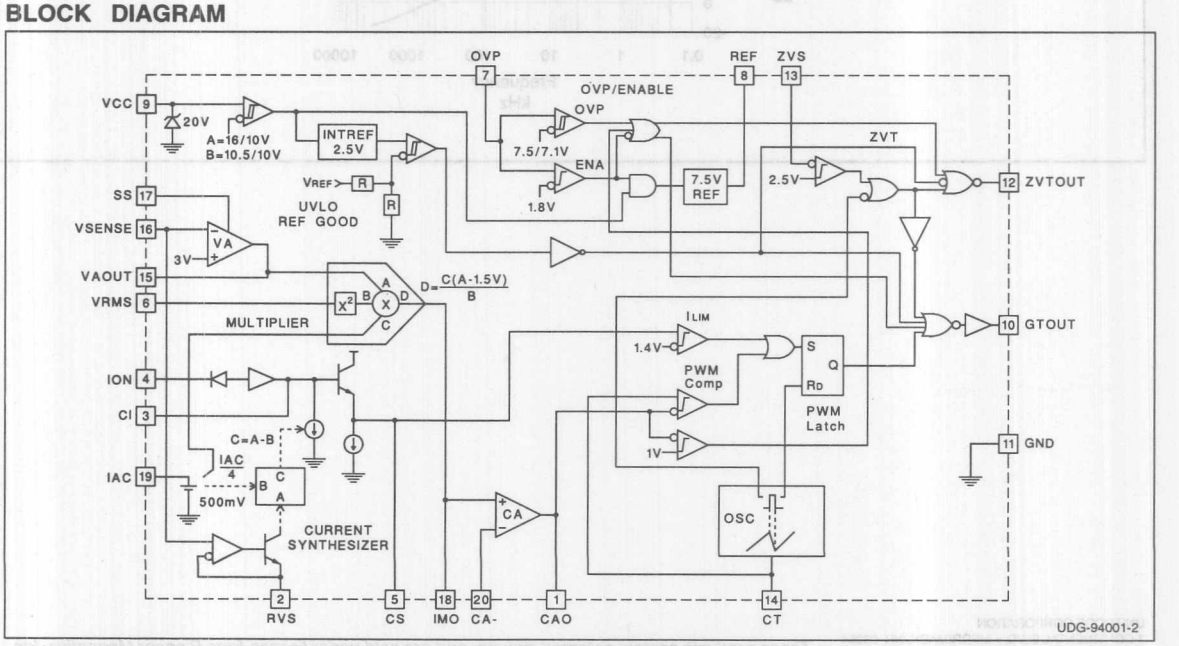
DESCRIPTION

The UC1855A/B provides all the control features necessary for high power, high frequency PFC boost converters. The average current mode control method allows for stable, low distortion AC line current programming without the need for slope compensation. In addition, the UC1855 utilizes an active snubbing or ZVT (Zero Voltage Transition technique) to dramatically reduce diode recovery and MOSFET turn-on losses, resulting in lower EMI emissions and higher efficiency. Boost converter switching frequencies up to 500kHz are now realizable, requiring only an additional small MOSFET, diode, and inductor to resonantly soft switch the boost diode and switch. Average current sensing can be employed using a simple resistive shunt or a current sense transformer. Using the current sense transformer method, the internal current synthesizer circuit buffers the inductor current during the switch on-time, and reconstructs the inductor current during the switch off-time. Improved signal to noise ratio and negligible current sensing losses make this an attractive solution for higher power applications.

The UC1855A/B also features a single quadrant multiplier, squarer, and divider circuit which provides the programming signal for the current loop. The internal multiplier current limit reduces output power during low line conditions. An overvoltage protection circuit disables both controller outputs in the event of a boost output OV condition.

Low startup supply current, UVLO with hysteresis, a 1% 7.5V reference, voltage amplifier with softstart, input supply voltage clamp, enable comparator, and overcurrent comparator complete the list of features. Available packages include: 20 pin N, DW, Q, J, and L.

BLOCK DIAGRAM



License Patent from Pioneer Magnetics. Pin numbers refer to DIL-20 J or N packages.

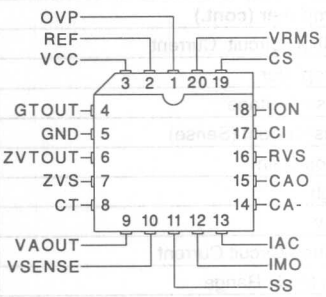
ABSOLUTE MAXIMUM RATINGS

Supply Voltage VCC ..... Internally Limited
VCC Supply Clamp Current 20mA
PFC Gate Driver Current (continuous) ..... ±0.5A
PFC Gate Driver Current (peak) ..... ±1.5A
ZVT Drive Current (continuous) ..... ±0.25A
ZVT Drive Current (peak) ..... ±0.75A
Input Current (IAC, RT, RVA) 5mA
Analog Inputs (except Peak Limit) ..... –0.3 to 10V
Peak Limit Input ..... –0.3 to 6.5V
Softstart Sinking Current 1.5mA
Storage Temperature ..... –65°C to +150°C
Junction Temperature ..... –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages. All voltages are referenced to GND.

CONNECTION DIAGRAMS

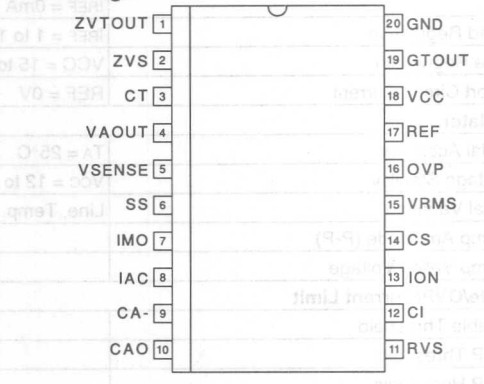
PLCC-20 & LCC-20 (Top View)
Q or L Package



DIL–20 (Top View)
J or N Package



SOIC-20 (Top View)
DW Package



ELECTRICAL CHARACTERISTICS: Unless otherwise specified: VCC = 18V, RT = 15k, RVS = 23k, CT = 470pF, CI = 150pF, VRMS = 1.5V, IAC = 100µA, ISENSE = 0V, CAOUT = 4V, VAOUT= 3.5V, VSENSE = 3V. TA = TJ. TA = –55°C to 125°C (UC1855A/B), –40°C to 85°C (UC2855A/B), 0°C to 70°C (UC3855A/B).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Overall					
Supply Current, OFF	CAO, VAOUT = 0V, VCC = UVLO –0.3V		150	500	µA
Supply Current, OPERATING			17	25	mA
VCC Turn-On Threshold	UC1855A		15.5	17.5	V
VCCTurn-Off Threshold	UC1855A,B	9	10		V
VCC Turn-On Threshold	UC1855B		10.5	10.8	V
VCC Clamp	I(VCC) = ICC(on) + 5mA	18	20	22	V
Voltage Amplifier					
Input Voltage		2.9		3.1	V
VSENSE Bias Current		–500	25	500	nA
Open Loop Gain	VOUT = 2 to 5V	65	80		dB
VOUT High	ILOAD = –300µA	5.75	6	6.25	V
VOUT Low	ILOAD = 300µA		0.3	0.5	V

ELECTRICAL CHARACTERISTICS (cont.): Unless otherwise specified: VCC = 18V, R_T = 15k, RVS = 23k, CT = 470pF, CI = 150pF, VRMS = 1.5V, IAC = 100µA, I_{SENSE} = 0V, CA_{OUT} = 4V, VAOUT= 3.5V, VSENSE = 3V. $T_A = T_J$. T_A = –55°C to 125°C (UC1855A/B), –40°C to 85°C (UC2855A/B), 0°C to 70°C (UC3855A/B).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Voltage Amplifier (cont.)					
Output Short Circuit Current	V_{OUT} = 0V		0.6	3	mA
Current Amplifier					
Input Offset Voltage	V_{CM} = – 2.5V	–4		4	mV
Input Bias Current (Sense)	V_{CM} = 2.5V	–500		500	nA
Open Loop Gain	V_{CM} = 2.5V, V_{OUT} = 2 to 6V	80	110		dB
V_{OUT} High	I_{LOAD} = –500µA		6		V
V_{OUT} Low	I_{LOAD} = 500µA		0.3	0.5	V
Output Short Circuit Current	V_{OUT} = 0V		1	3	mA
Common Mode Range		–0.3		5	V
Gain Bandwidth Product	F_{IN} = 100kHz, 10mV, P-P, T_A = 25°C	2.5	5		MHz
Reference					
Output Voltage	I_{REF} = 0mA, T_A = 25°C	7.388	7.5	7.613	V
	I_{REF} = 0mA	7.313	7.5	7.688	V
Load Regulation	I_{REF} = 1 to 10 mA	–15		15	mV
Line Regulation	VCC = 15 to 35V	–10		10	mV
Short Circuit Current	REF = 0V	20	45	65	mA
Oscillator					
Initial Accuracy	T_A = 25°C	170	200	230	kHz
Voltage Stability	V_{CC} = 12 to 18V		1		%
Total Variation	Line, Temp.	160		240	kHz
Ramp Amplitude (P-P)		4.9		5.9	V
Ramp Valley Voltage		1.1		1.6	V
Enable/OVP/Current Limit					
Enable Threshold			1.8	2.2	V
OVP Threshold			7.5	7.66	V
OVP Hysteresis		200	400	600	mV
OVP Propagation Delay			200		ns
OVP Input Bias Current	V= 7.5V		1	10	µA
PK_{LIMIT} Threshold		1.25	1.5	1.75	V
PK_{LIMIT} Input Current	$V_{PKLIMIT}$ = 1.5V		100		µA
PK_{LIMIT} Prop. Delay			100		ns
Multiplier					
Output Current - IAC Limited	IAC = 100µA, VRMS = 1V	–235	–205	–175	µA
Output Current - Zero	IAC = 0µA	–2	–0.2	2	µA
Output Current - Power Limited	VRMS = 1.5V, VAOUT = 5.5V	–250	–209	–160	µA
Output Current	VRMS = 1.5V, VAOUT = 2V		–26		µA
	VRMS = 1.5V VAOUT = 5V		–190		µA
	VRMS = 5V, VAOUT = 2V		–3		µA
	VRMS = 5V, VAOUT = 5V		–17		µA
Gain Constant	Refer to Note 1	–0.95	–0.85	–0.75	1/V
Gate Driver Output					
Output High Voltage	I_{OUT} = –200mA, VCC = 15V	12	12.8		V
Output Low Voltage	I_{OUT} = 200mA		1	2.2	V
Output Low Voltage	I_{OUT} = 10mA		300	500	mV

ELECTRICAL CHARACTERISTICS (cont.): Unless otherwise specified: VCC = 18V, RT = 15k, RVS = 23k, CT = 470pF, CI = 150pF, VRMS = 1.5V, IAC = 100µA, ISENSE = 0V, CAOUT = 4V, VAOUT= 3.5V, VSENSE = 3V. TA = TJ. TA = –55°C to 125°C (UC1855A/B), –40°C to 85°C (UC2855A/B), 0°C to 70°C (UC3855A/B).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Gate Driver Output (cont.)					
Output Low (UVLO)	IOUT = 50mA, VCC = 0V		0.9	1.5	V
Output RISE/FALL Time	CLOAD = 1nF		35		ns
Output Peak Current	CLOAD = 10nF		1.5		A
ZVT					
Reset Threshold		2.3	2.6	2.9	V
Input Bias Current	V = 2.5V, VCT = 0		6	20	µA
Propagation Delay	Measured at ZVTOUT		100		ns
Maximum Pulse Width			400		ns
Output High Voltage	IOUT = –100mA, VCC = 15V	12	12.8		V
Output Low Voltage	IOUT = 100mA		1	2.2	V
	IOUT = 10mA		300	900	mV
Output Low (UVLO)	IOUT = 50mA, VCC = 0V		0.9	1.5	V
Output RISE/FALL Time	CLOAD = 1nF		35		ns
Output Peak Current	CLOAD = 10nF		0.75		A
Current Synthesizer					
ION to CS Offset	VION = 0V		30	50	mV
CI Discharge Current	IAC = 50µA	105	118	140	µA
	IAC = 500µA		5		µA
IAC Offset Voltage		0.3	0.65	1.1	V
ION Buffer Slew Rate			10		V/µs
ION Input Bias Current	VION = 2V		2	15	µA
RVS Output Voltage	23k from RVS to GND	2.87	3	3.13	V

Note 1: Gain constant (K) $= \frac{IAC \bullet (VAOUT - 1.5V)}{(VRMS^2 \bullet IMO)}$ *at* $1.5V \leq VRMS \leq 5V$

PIN DESCRIPTIONS

CA-: This is the inverting input to the current amplifier. Connect the required compensation components between this pin and CAOUT. The common mode operating range for this input is between –0.3V and 5V.

CAO: This is the output of the wide bandwidth current amplifier and one of the inputs to the PWM duty cycle comparator. The output signal generated by this amplifier commands the PWM to force the correct input current. The output can swing from 0.1V to 7.5V.

CI: The level shifted current sense signal is impressed upon a capacitor connected between this pin and GND. The buffered current sense transformer signal charges the capacitor when the boost switch is on. When the switch is off, the current synthesizer discharges the capacitor at a rate proportional to the dI/dt of the boost inductor current. In this way, the discharge current is approximately equal to

$$\frac{3V}{R_{RVS}} - \frac{IAC}{4}.$$

Discharging the CI capacitor in this fashion, a "reconstructed" version of the inductor current is generated using only one current sense transformer.

CS: The reconstructed inductor current waveform generated on the CI pin is level shifted down a diode drop to this pin. Connect the current amplifier input resistor between CS and the inverting input of the current amplifier. The waveform on this pin is compared to the multiplier output waveform through the average current sensing current amplifier. The input to the peak current limiting comparator is also connected to this pin. A voltage level greater than 1.5 volts on this pin will trip the comparator and disable the gate driver output.

CT: A capacitor from CT to GND sets the PWM oscillator frequency according to the following equation:

$$f \approx \frac{1}{11200 \bullet CT}.$$

Use a high quality ceramic capacitor with low ESL and ESR for best results. A minimum CT value of 200pF insures good accuracy and less susceptibility to circuit lay-

PIN DESCRIPTIONS (cont.)

out parasitics. The oscillator and PWM are designed to provide practical operation to 500kHz.

GND: All voltages are measured with respect to this pin. All bypass and timing capacitors connected to GND should have leads as short and direct as possible.

GTOUT: The output of the PWM is a 1.5A peak totem pole MOSFET gate driver on GTOUT. A series resistor between GTOUT and the MOSFET gate of at least 10 ohms should be used to limit the overshoot on GTOUT. In addition, a low V_F Schottky diode should be connected between GTOUT and GND to limit undershoot and possible erratic operation.

IAC: This is a current input to the multiplier. The current into this pin should correspond to the instantaneous value of the rectified AC input line voltage. This is accomplished by connecting a resistor directly between IAC and the rectified input line voltage. The nominal 650mV level present on IAC negates the need for any additional compensating resistors to accommodate for the zero crossings of the line. A current equal to one fourth of the IAC current forms one of the inductor current synthesizer inputs.

IMO: This is the output of the multiplier, and the non-inverting input of the current amplifier. Since this output is a current, connect a resistor between this pin and ground equal in value to the input resistor of the current amplifier. The common mode operating range for this pin is –0.3V to 5V.

ION: This pin is the current sensing input. It should be connected to the secondary side output of a current sensing transformer whose primary winding is in series with the boost switch. The resultant signal applied to this input is buffered and level shifted up a diode to the CI capacitor on the CI pin. The ION buffer has a source only output. Discharge of the CI cap is enabled through the current synthesizer circuitry. The current sense transformer termination resistor should be designed to obtain a 1V input signal amplitude at peak switch current.

OVP: This pin senses the boost output voltage through a voltage divider. The enable comparator input is TTL compatible and can be used as a remote shutdown port. A voltage level below 1.8V, disables V_{REF}, oscillator, and the PWM circuitry via the enable comparator. Between 1.8V and V_{REF} (7.5V) the UC1855 is enabled. Voltage levels above 7.5V will set the PWM latch via the hysteretic OVP comparator and disable both ZVTOUT and GTOUT until the OVP level has decayed by the nominal hysteresis of 400mV. If the voltage divider is designed to initiate an OVP fault at 5% of OV, the internal hysteresis enables normal operation again when the output voltage has reached its nominal regulation level. Both the OVP and enable comparators have direct logical connections to the PWM output and exhibit typical propagation delays of 200ns.

RVS: The nominal 3V signal present on the VSENSE pin is buffered and brought out to the RVS pin. A current proportional to the output voltage is generated by connecting a resistor between this pin and GND. This current forms the second input to the current synthesizer.

VAO: This is the output of the voltage amplifier. At a given input RMS voltage, the voltage on this pin will vary directly with the output load. The output swing is limited from approximately 100mV to 6V. Voltage levels below 1.5V on this pin will inhibit the multiplier output.

VCC: Positive supply rail for the IC. Bypass this pin to GND with a 1µF low ESL, ESR ceramic capacitor. This pin is internally clamped to 20V. Current into this clamp should be limited to less than 10mA. The UC1855A has a 15.5V (nominal) turn on threshold with 6 volts of hysteresis while the UC1855B turns on at 10.5V with 500mV of hysteresis.

REF: REF is the output of the precision reference. The output is capable of supplying 25mA to peripheral circuitry and is internally short circuit current limited. REF is disabled and low whenever VCC is below the UVLO threshold, and when OVP is below 1.8V. A REF "GOOD" comparator senses REF and disables the stage until REF has attained approximately 90% of its nominal value. Bypass REF to GND with a 0.1µF or larger ceramic capacitor for best stability.

VRMS: This pin is the feedforward line voltage compensation input to the multiplier. A voltage on VRMS proportional to the AC input RMS voltage commands the multiplier to alter the current command signal by $1/VRMS^2$ to maintain a constant power balance. The input to VRMS is generally derived from a two pole low pass filter/voltage divider connected to the rectified AC input voltage. This feature allows universal input supply voltage operation and faster response to input line fluctuations for the PFC boost preregulator. For most designs, a voltage level of 1.5V on this pin should correspond to low line, and 4.7V for high line. The input range for this pin extends from 0 to 5.5V.

PIN DESCRIPTIONS (cont.)

VSENSE: This pin is the inverting input of the voltage amplifier and serves as the output voltage feedback point for the PFC boost converter. It senses the output voltage through a voltage divider which produces a nominal 3V. The voltage loop compensation is normally connected between this pin and VAO.

ZVS: This pin senses when the drain voltage of the main MOSFET switch has reached approximately zero volts, and resets the ZVT latch via the ZVT comparator. A minimum and maximum ZVTOUT pulse width are programmable from this pin. To directly sense the ≈400V drain voltage of the main switch, a blocking diode is connected between ZVS and the high voltage drain. When the drain reaches 0V, the level on ZVS is ≈0.7V which is below the 2.6V ZVT comparator threshold. The maximum ZVTOUT pulse width is approximately equal to the oscillator blanking period time.

ZVTOUT: The output of the ZVT block is a 750mA peak totem pole MOSFET gate driver on ZVTOUT. Since the ZVT MOSFET switch is typically 3X smaller than the main switch, less peak current is required from this output. Like GTOUT, a series gate resistor and Schottky diode to GND are recommended. This pin may also be used as a high current synchronization output driver.

TYPICAL APPLICATION

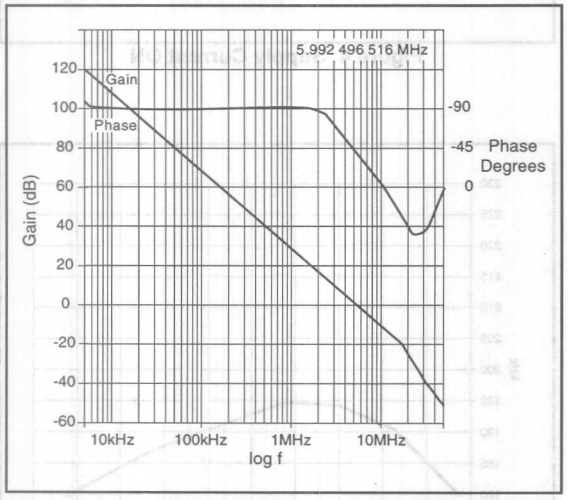


Figure 1. Current Amplifier Frequency Response

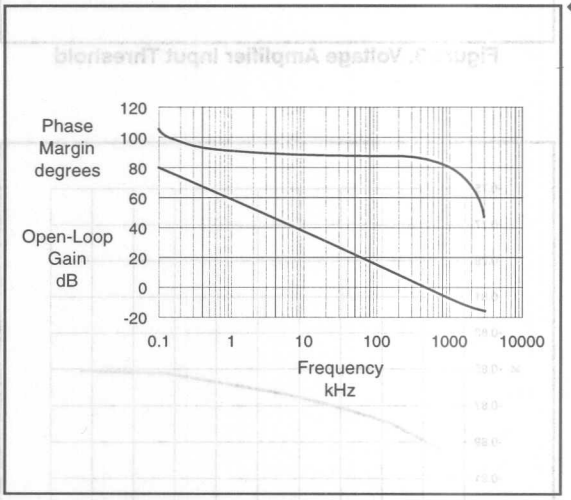


Figure 2. Voltage Amplifier Gain Phase vs Frequency

TYPICAL APPLICATION (cont.)

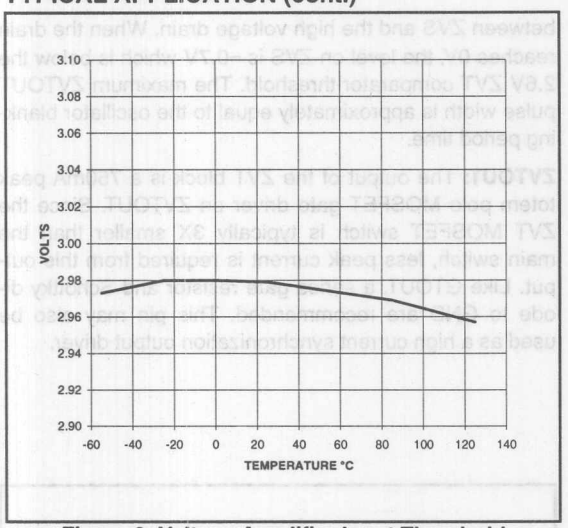


Figure 3. Voltage Amplifier Input Threshold

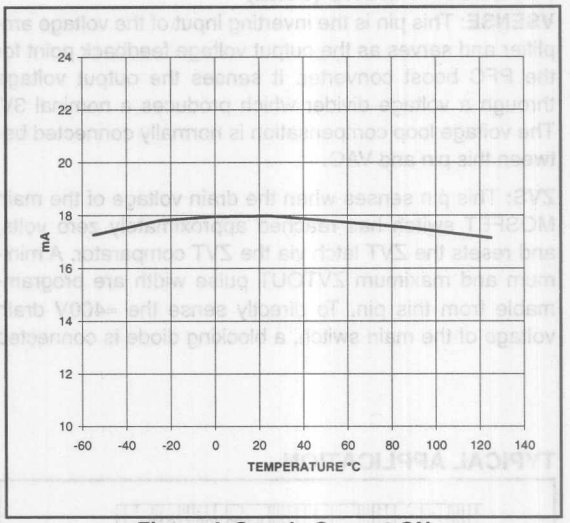


Figure 4. Supply Current ON

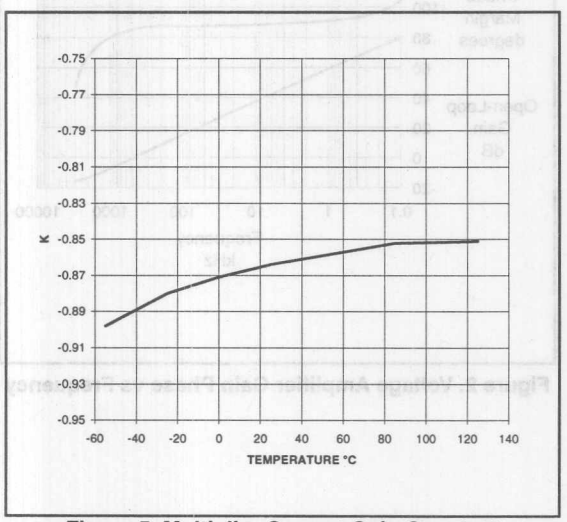


Figure 5. Multiplier Current Gain Constant

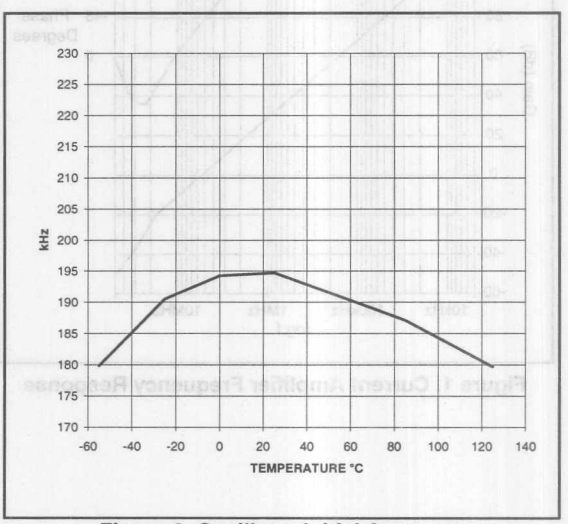


Figure 6. Oscillator Initial Accuracy

TYPICAL APPLICATION (cont.)

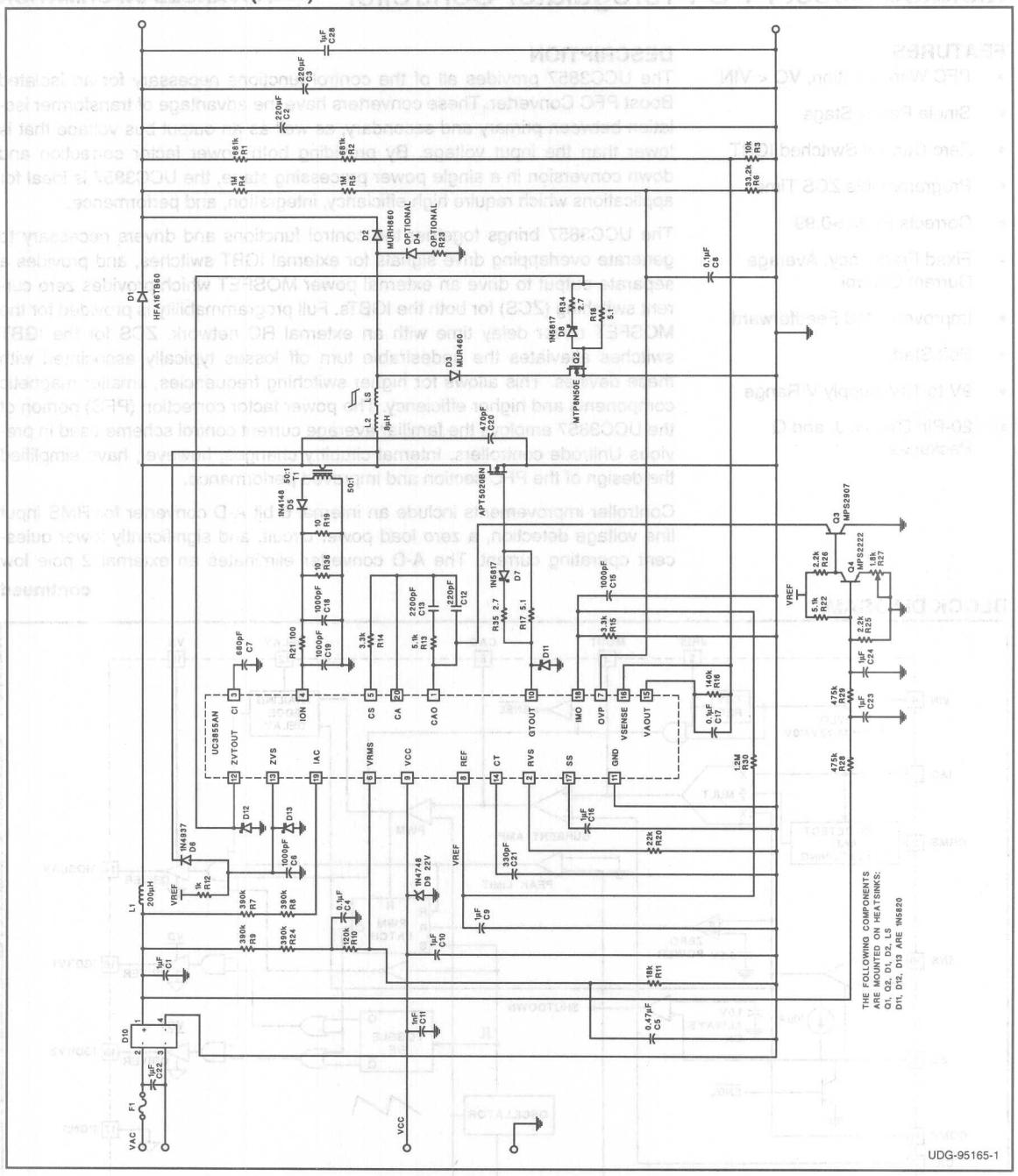


Figure 1. Typical Application

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

Isolated Boost PFC Preregulator Controller

ADVANCED INFORMATION

FEATURES

- PFC With Isolation, VO < VIN
- Single Power Stage
- Zero Current Switched IGBT
- Programmable ZCS Time
- Corrects PF to >0.99
- Fixed Frequency, Average Current Control
- Improved RMS Feedforward
- Soft Start
- 9V to 18V Supply V Range
- 20-Pin DW, N, J, and Q Packages

DESCRIPTION

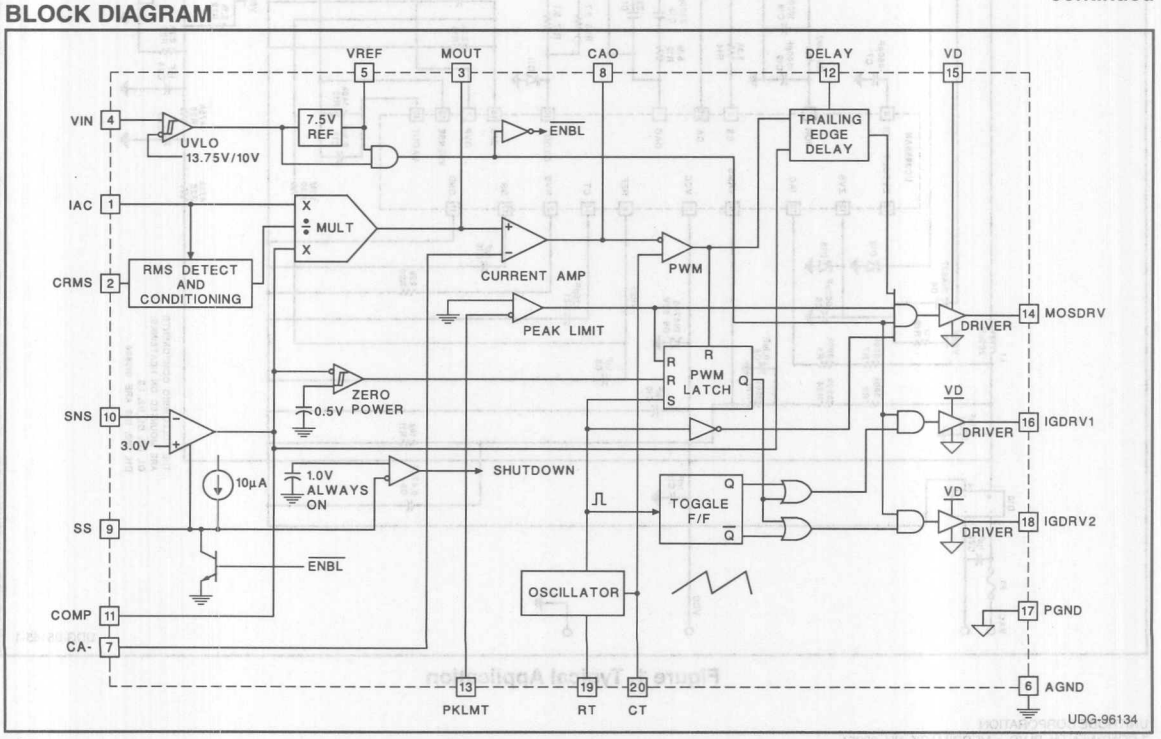
The UCC3857 provides all of the control functions necessary for an Isolated Boost PFC Converter. These converters have the advantage of transformer isolation between primary and secondary, as well as an output bus voltage that is lower than the input voltage. By providing both power factor correction and down conversion in a single power processing stage, the UCC3857 is ideal for applications which require high efficiency, integration, and performance.

The UCC3857 brings together the control functions and drivers necessary to generate overlapping drive signals for external IGBT switches, and provides a separate output to drive an external power MOSFET which provides zero current switching (ZCS) for both the IGBTs. Full programmability is provided for the MOSFET driver delay time with an external RC network. ZCS for the IGBT switches alleviates the undesirable turn off losses typically associated with these devices. This allows for higher switching frequencies, smaller magnetic components and higher efficiency. The power factor correction (PFC) portion of the UCC3857 employs the familiar average current control scheme used in previous Unitrode controllers. Internal circuitry changes, however, have simplified the design of the PFC section and improved performance.

Controller improvements include an internal 6 bit A-D converter for RMS input line voltage detection, a zero load power circuit, and significantly lower quiescent operating current. The A-D converter eliminates an external 2 pole low

continued

BLOCK DIAGRAM



7/96

DESCRIPTION (cont.)

pass filter for RMS detection. This simplifies the converter design, eliminates 2nd harmonic ripple from the feedforward component, and provides an approximate 6 times improvement in input line transient response. The zero load power comparator prevents energy transfer during open load conditions without compromising power factor at light loads. Low startup and operating currents which are achieved through the use of Unitrode's BCDMOS process simplify the auxiliary bootstrap supply design.

Additional features include: under voltage for reliable offline startup, a programmable over current shutdown, an auxiliary shutdown port, a precision 7.5V reference, a high amplitude oscillator ramp for improved noise susceptibility, softstart, and a low offset analog square, multiple and divide circuit. Like previous Unitrode PFC controllers, worldwide operation without range switches is guaranteed.

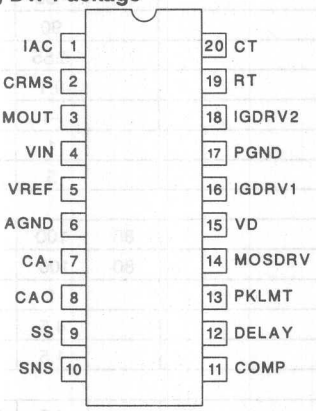
ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage (VIN, VD) 18V
General Analog/Logic Inputs
(Maximum Forced Voltage) . . . . . –0.3V to 5V
IAC (Maximum Forced Current) 200µA
Reference Output Current . . . . . Internally Limited
Output Current (MOSDRV, IGDRV1, IGDRV2)
Pulsed 1A
Continuous 200mA
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 Sec.) . . . . . +300°C

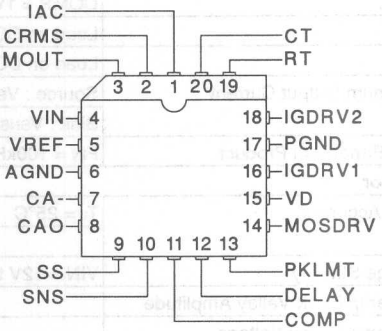
Unless otherwise indicated, voltages are reference to ground and currents are positive into, negative out of the specified terminal. Pulsed is defined as a less than 10% duty cycle with a maximum duration of 500µs. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAMS

DIL-20, SOIC- 20 (Top View)
N Package, DW Package



PLCC-20 (Top View)
Q and L Packages



ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C for the UCC3857, –40°C to +85°C for the UCC2857, and –55°C to +125°C for the UCC1857, VIN, VD = 12V, RT = 19.2K, CT = 680pF. T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply					
Supply Current, Active	No Load on Outputs, VD = VIN		3.5	TBD	mA
Supply Current, Startup	No Load on Outputs, VD = VIN		60	TBD	µA
VIN UVLO Threshold			13.75	15.5	V
UVLO Threshold Hysteresis		3	3.75	TBD	V
Reference					
Output Voltage (VREF)	T_J = 25°C, I_{REF} = 1mA	7.387	7.5	7.613	V
	Over Temperature, UCC3857	7.368	7.5	7.631	V
	Over Temperature, UCC1857, UCC2857	7.313	7.5	7.687	V

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C for the UCC3857, –40°C to +85°C for the UCC2857, and –55°C to +125°C for the UCC1857, VIN, VD = 12V, RT = 19.2K, CT = 680pF. T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Reference (cont.)					
Load Regulation	I_{REF} = 1mA to 10mA		2	TBD	mV
Line Regulation	VIN = VD = 12V to 16V		2	TBD	mV
Short Circuit Current	VREF = 0V		35		mA
Current Amplifier					
Input Offset Voltage	(Note 1)	–3	0	3	mV
Input Bias Current	(Note 1)		–50		nA
Input Offset Current	(Note 1)		25		nA
CMRR	V_{CM} = 0V to 1.5V, V_{CAO} = 3V		80		dB
AVOL	V_{CM} = 0V, V_{CAO} = 2V to 5V		90		dB
VOH	Load on CAO = 50µA, V_{MOUT} = 0V, V_{CA-} = 1V		6		V
VOL	Load on CAO = 50µA, V_{MOUT} = 0V, V_{CA-} = 1V		0.2		V
Maximum Output Current	Source : V_{CA-} = 0V, V_{MOUT} = 1V, V_{CAO} = 3V		–150		µA
	Sink : V_{CA-} = 1V, V_{MOUT} = 0V, V_{CAO} = 3V		1		mA
Gain Bandwidth Product	F_{IN} = 100kHz, 10mV p – p	3	5		MHz
Voltage Amplifier					
Input Voltage	Measured on V_{SNS}, COMP = 3V	2.9	3	3.1	V
Input Bias Current	Measured on V_{SNS}, COMP = 3V		–50		nA
AVOL	COMP = 1V to 5V		90		dB
VOH	Load on COMP = -50µA, V_{SNS} = 2.8V		5.55		V
VOL	Load on COMP = 50µA, V_{SNS} = 3.2V		0.1	0.45	V
Maximum Output Current	Source : V_{SNS} = 2.8V, COMP = 3V		–1		mA
	Sink : V_{SNS} = 3.2V, COMP = 3V		1		mA
Gain Bandwidth Product	F_{IN} = 100kHz, 10mV p – p		5		MHz
Oscillator					
Initial Accuracy	T_J = 25°C	85	100	115	kHz
		80	100	120	kHz
Voltage Stability	VIN = 12V to 18V		1		%
CT Ramp Peak-Valley Amplitude			4.5		V
CT Ramp Valley Voltage			1.5		V
Output Drivers					
Pull Up Resistance	OUTPUT = 5V		4.7	TBD	Ω
Pull Down Resistance	OUTPUT = 5V		2.5	TBD	Ω
Rise Time	C_{LOAD} = 1nF		25	TBD	ns
Fall Time	C_{LOAD} = 1nF		10	TBD	ns
Trailing Edge Delay					
Delay Time	R = 12k, C = 200pF, COMP = 4V	1.6	2	2.4	µs
Soft Start					
Charge Current			10		µA
Shutdown Comparator Threshold	Measured on SS	0		0.4	V
Multiplier					
Output Current, IAC Limited	IAC = 100µA, COMP = 5.5V, V_{CRMS} = 0V		–200		µA
Output Current, Power Limited	IAC = 100µA, COMP = 5.5V, V_{CRMS} = 1V		–200		µA
Output Current, Zero	IAC = 0	–2	0	2	µA
Gain Constant			2.5		1/V

ELECTRICAL CHARACTERISTICS (cont.): Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C for the UCC3857, –40°C to +85°C for the UCC2857, and –55°C to +125°C for the UCC1857, VIN, VD = 12V, RT = 19.2K, CT = 680pF. T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Zero Power, Peak Current					
Zero Power Comparator Threshold	Measured on COMP		0.5		V
Peak Current Limit Comparator Threshold	Measured on PKLMT		0		V

Note 1: Common mode voltages = 0V, V_{CAO} = 3V

PIN DESCRIPTIONS

AGND: Reference point of the internal reference and all thresholds, as well as the return for the remainder of the device except for the output drivers.

CA–: Inverting input of the inner current loop error amplifier.

CAO: Output of the inner current loop error amplifier. This output can swing between approximately 0.2V and 6V. It is one of the inputs to the PWM comparator.

COMP: This is the output of the voltage loop error amplifier. It is internally clamped to approximately 5.6V by the UCC3857 and can swing as low as approximately 0.1V. Voltages below 0.5V on COMP will disable the MOSDRV output and force the IGDRV1 and IGDRV2 outputs to a zero overlap condition.

CRMS: A capacitor is connected between CRMS and ground to average the AC line voltage over a half cycle. CRMS is internally connected to the RMS detection circuitry.

CT: A capacitor (low ESR, ESL) is tied between CT and ground to set the ramp generator switching frequency in conjunction with RT. The ramp generator frequency is approximately equal to:

$$\frac{0.67}{RT \bullet CT}$$

DELAY: A resistor to VREF and a capacitor to AGND are connected to DELAY to set the overlap delay time for the MOSDRV output stage. The overlap delay function can be disabled by removing the capacitor to AGND.

IAC: A resistor is connected to the rectified AC input line voltage from IAC. This provides the internal multiplier and the RMS detector with instantaneous line voltage information.

IGDRV1: Driver output for one of the two external IGBT power switches.

IGDRV2: Driver output for one of the two external IGBT power switches.

MOSDRV: Driver output for the external power MOSFET switch.

MOUT: Output of the analog multiply and divide circuit. The output current from MOUT is fed into a resistor to the return leg of the input bridge. The resultant waveform forms the sine reference for the current error amplifier.

PKLMT: Inverting input of the peak current limit comparator. The threshold for this comparator is nominally set to 0V. The peak limit comparator terminates the MOSDRV output and forces the IGDRV1 and IGDRV2 outputs to zero overlap when tripped.

PGND: Return for all high level currents, internally tied to the output driver stages of the UCC3857.

RT: A resistor is tied between RT and ground to set the charging current for the internal ramp generator. The UCC3857 provides a temperature compensated 3.0V at RT. The oscillator charging current is therefore: 3.0V/RT. Current out of RT should be limited to 250µA for best performance.

SNS: This is the feedback input for the outer voltage control loop. An external opto isolator circuit provides the output voltage regulation information to SNS across the isolation barrier.

SS: A capacitor is connected between SS and GND to provide the UCC3857 soft start feature. The voltage on COMP, is clamped to approximately the same voltage as SS. An internal 10µA (nominal) current source is provided by the UCC3857 to charge the soft start capacitor.

VD: Positive supply rail for the three output driver stages. The voltage applied to VD must be limited to less than 18VDC. VD should be bypassed to PGND with a 0.1µF to 1.0µF low ESR, ESL capacitor for best results. VD and VIN can be isolated from each other with an RC lowpass filter for better supply noise rejection.

VIN: Input voltage supply to the UCC3857. This voltage must be limited to less than 18VDC. The UCC3857 is enabled when the voltage on VIN exceeds 13.75V (nominal).

VREF: Output of the precision 7.5V reference. A 0.01µF to 0.1µF low ESR, ESL bypass capacitor is recommended between VREF and AGND for best performance.

APPLICATION INFORMATION

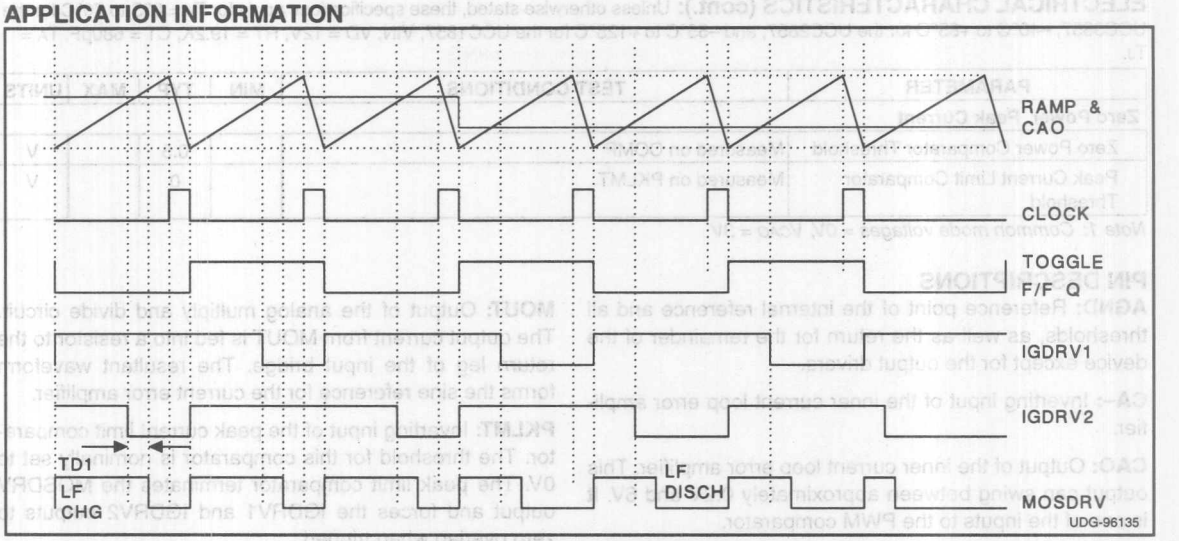


Figure 1. Typical Power Stage Waveforms

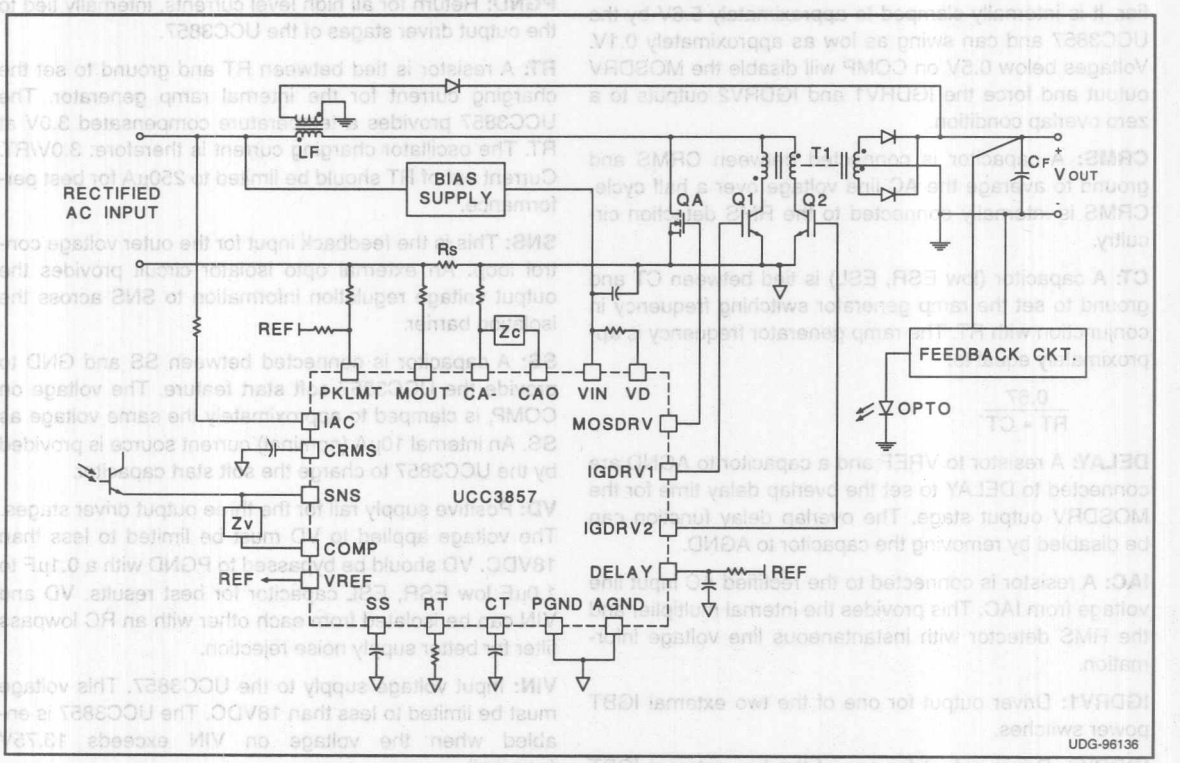


Figure 2. Typical Application Circuit

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High Efficiency, High Power Factor Preregulator

ADVANCED INFORMATION

FEATURES

- Programmable PWM Frequency Foldback for Higher Efficiency at Light Loads
- Leading Edge PWM for Reduced Output Capacitor Ripple Current
- Controls Boost PWM to Near Unity Power Factor
- World Wide Operation without Switches
- Accurate Power Limiting
- Synchronizable Oscillator
- 100µA Startup Supply Current
- Low Power BCDMOS
- 12V to 18V Operation

DESCRIPTION

The UCC3858 provides all of the functions necessary for active power factor corrected preregulators which require high efficiency at low power operation. The controller achieves near unity power factor by shaping the AC input line current waveform to correspond to the AC input line voltage using average current mode control.

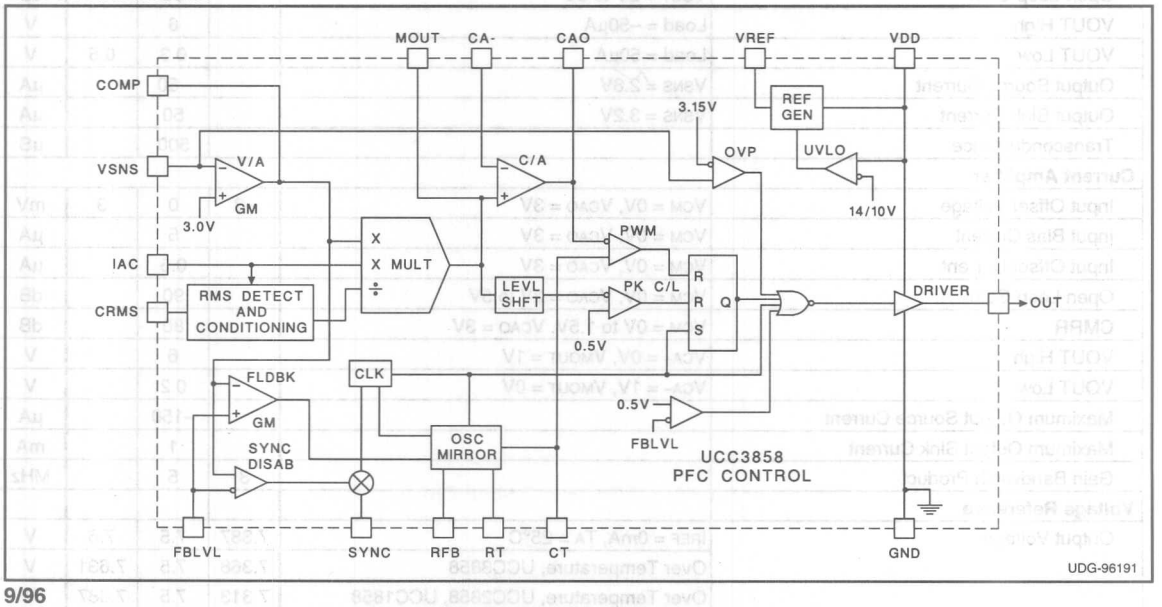
The operation of the UCC3858 closely resembles that of previously designed Unitrode PFC parts with additional features to allow higher efficiency boost converter operation at light loads. This is accomplished by linearly scaling back the PWM frequency when the output of the voltage error amplifier drops below a predetermined user programmable level indicating a light load condition. The frequency is scaled back by reducing the charging current for the CT ramp (in proportion to the output power), and increasing the dead time. There is also an instantaneous reset input to pull the IC out of foldback mode quickly when the load comes back up.

The PWM technique used in the UCC3858 is leading edge modulation. When combined with the more conventional trailing edge modulation on the downstream converter, this scheme offers the benefit of reduced ripple current on the bulk storage capacitor. The oscillator is designed for easy synchronization to the downstream converter. A simple synchronization scheme can be implemented by connecting the PWM output of the downstream converter to the SYNC pin.

Controller improvements include an onboard peak detector for the input line RMS voltage, an integrated overcurrent shutdown, overvoltage shutdown and significantly lower quiescent operating current. The peak detector eliminates an external 2-pole low pass filter for RMS detection. This simplifies the converter design as well as providing an approximate 6X improvement in input line transient response. The current signal is

continued

BLOCK DIAGRAM



DESCRIPTION (cont.)

extracted from the current error amplifier input to provide a cycle-by-cycle peak current limit. Low startup and operating currents which are achieved through the use of Unitrode's BCDMOS process simplify the bootstrap supply design as well as minimize losses in the control circuit. A transconductance voltage error amplifier allows output voltage sensing for internal overvoltage protection.

Additional features include: undervoltage lockout for reliable off-line startup, a precision 7.5V reference, and a precision RMS detection and signal conditioning circuit. Chip shutdown can be attained by bringing the VFBLVL pin below 0.5V.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{DD} 18V
Gate Drive Current
Continuous 0.2A
Pulsed 1A
Input Voltage, CA–, MOUT, VSNS 11V
Input Current IAC 200mA
Power Dissipation 1W
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 Sec.) . . . . . +300°C

Unless otherwise indicated, voltages are reference to ground and currents are positive into, negative out of the specified terminal. Pulsed is defined as a less than 10% duty cycle with a maximum duration of 500ns. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C for the UCC3858, –40°C to +85°C for the UCC2858, and –55°C to +150°C for the UCC1858, VDD = 18V, RT = 24k, CT = 330pF, RFB = 96k, IAC = 100µA, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Overall					
Supply Current, Off	CAO, COMP = 0V, VDD = UVLO – 0.3V		60		µA
Supply Current, On			3.5		mA
VDD Turn-On Threshold			13.75	15.5	V
VDD Turn-Off Threshold		9	10		V
UVLO Hysteresis			TBD		V
Voltage Amplifier					
Input Voltage	T_A = 25°C	2.95	3	3.05	V
Over Voltage Protection		3.1	3.15	3.2	V
VSNS Bias Current			1		µA
Open Loop Gain	V_{OUT} = 2V to 5V		60		dB
VOUT High	Load = –50µA		6		V
VOUT Low	Load = 50µA		0.3	0.5	V
Output Source Current	V_{SNS} = 2.8V		–50		µA
Output Sink Current	V_{SNS} = 3.2V		50		µA
Transconductance			500		µS
Current Amplifier					
Input Offset Voltage	V_{CM} = 0V, V_{CAO} = 3V	–3	0	3	mV
Input Bias Current	V_{CM} = 0V, V_{CAO} = 3V		5		µA
Input Offset Current	V_{CM} = 0V, V_{CAO} = 3V		0.5		µA
Open Loop Gain	V_{CM} = 0V, V_{CAO} = 2V to 5V		90		dB
CMRR	V_{CM} = 0V to 1.5V, V_{CAO} = 3V		80		dB
VOUT High	V_{CA-} = 0V, V_{MOUT} = 1V		6		V
VOUT Low	V_{CA-} = 1V, V_{MOUT} = 0V		0.2		V
Maximum Output Source Current			–150		µA
Maximum Output Sink Current			1		mA
Gain Bandwidth Product		3	5		MHz
Voltage Reference					
Output Voltage	I_{REF} = 0mA, T_A = 25°C	7.387	7.5	7.6	V
	Over Temperature, UCC3858	7.368	7.5	7.631	V
	Over Temperature, UCC2858, UCC1858	7.313	7.5	7.687	V

ELECTRICAL CHARACTERISTICS (cont.): Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C for the UCC3858, –40°C to +85°C for the UCC2858, and –55°C to +150°C for the UCC1858, VDD = 18V, RT = 24k, CT = 330pF, RFB = 96k, IAC = 100µA, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Voltage Reference (cont.)					
Load Regulation	I_{REF} = 1mA to 10mA		2		mV
Line Regulation	VDD = 12V to 16V		2		mV
Short Circuit Current	VREF = 0V		35		mA
Oscillator					
Initial Accuracy	T_A = 25°C	85	100	115	kHz
Voltage Stability	VDD = 12V to 18V		1		%
Total Variation	Line Temperature	80		120	kHz
Ramp Amplitude (p-p)	Oscillator Free Running, COMP = 5.5V	3.2	3.5	3.8	V
Ramp Peak Voltage		4	4.5	5	V
Peak Current Limit					
PKLMT Reference Voltage		450	500	550	mV
PKLMT Offset Voltage			100		mV
PKLMT Propagation Delay			1		µs
Multiplier					
Output Current, IAC Limited	IAC = 100µA, COMP = 5.5V, V_{CRMS} = 0V		–200		µA
Output Current, Power Limited	IAC = 100µA, COMP = 5.5V, V_{CRMS} = 1V		–200		µA
Output Current, Zero	IAC = 0µA	–2	0	2	µA
Gain Constant			2.5		1/V
PWM Frequency Foldback					
FBLVL Offset			15		mV
FBLVL Input Current			100		nA
RFB Reference			4.5		V
RFB Foldback Override			1.5		V
Gate Driver					
Pull Up Resistance	OUT = 5V		4.7		Ω
Pull Down Resistance	OUT = 5V		2.5		Ω
Output Rise Time	C_{LOAD} = 1nF		25		ns
Output Fall Time	C_{LOAD} = 1nF		10		ns

Note 1: Guaranteed by design, not 100% tested in production.

PIN DESCRIPTIONS

CA-: Inverting input to the current amplifier. This input and the non-inverting input MOUT remain functional down to and below GND.

CAO: Output of a wide bandwidth amplifier that senses line current and commands the pulse width modulator (PWM) to force the correct current. This output can swing close to GND, allowing the PWM to force zero duty cycle when necessary.

CRMS: A capacitor connected between CRMS and GND enables averaging of the AC line voltage over a half cycle. IAC current is internally mirrored to provide charging current for CRMS.

CT: (Oscillator Timing Capacitor) A capacitor from CT to GND will set the free-running PWM oscillator frequency according to:

$$f = \frac{0.814}{RT \bullet CT}$$

COMP: Output of the transconductance amplifier that regulates output voltage. The voltage amplifier output is internally limited to approximately 6V to prevent overshoot. It is also used to determine the frequency foldback mode.

FBLVL: (Frequency Foldback Level Select) Selects the level of the voltage error amplifier output at which frequency foldback begins. A chip shutdown can be attained by bringing the foldback level pin to below 0.5V.

GND: (Ground) All voltages measured with respect to ground. VDD and REF should be bypassed directly to

PIN DESCRIPTIONS (cont.)

GND with a 0.1µF or larger ceramic capacitor. The timing capacitor discharge current also returns to this pin, so the lead from the oscillator timing to GND should be as short and direct as possible.

IAC: (Input AC Current) This input to the analog multiplier is a current. The multiplier is tailored for very low distortion from this current input (IAC) to MOUT.

MOUT: (Multiplier Output and Current Sense Plus) The output of the analog multiplier and the non-inverting input of the current amplifier are connected together at MOUT. As the multiplier output is a current, this is a high impedance input so the amplifier can be configured as a differential amplifier to reject ground noise. The voltage at this pin is also used to implement peak current limiting.

OUT: (Gate Drive) The output of the PWM is a totem pole MOSFET gate driver on gate drive. A series gate resistor of at least 5Ω is recommended to prevent interaction between the gate impedance and the output driver that might cause the gate drive to overshoot excessively.

RFB: (Minimum Frequency Reference) A resistor between this pin and VREF is used to set the minimum frequency during foldback mode. Once the value of RT and CT are determined, use

$$RFB = \frac{1}{C_T \bullet f_{MIN}} - R_T$$

find the value of RFB which will set the minimum foldback frequency to f_{MIN}. This pin also incorporates a foldback override which enables the part to return quickly to normal operating mode when the load comes back up. To override foldback mode, force this pin below 1.5V with an open collector.

RT: A resistor from RT to GND is used to program oscillator charging current.

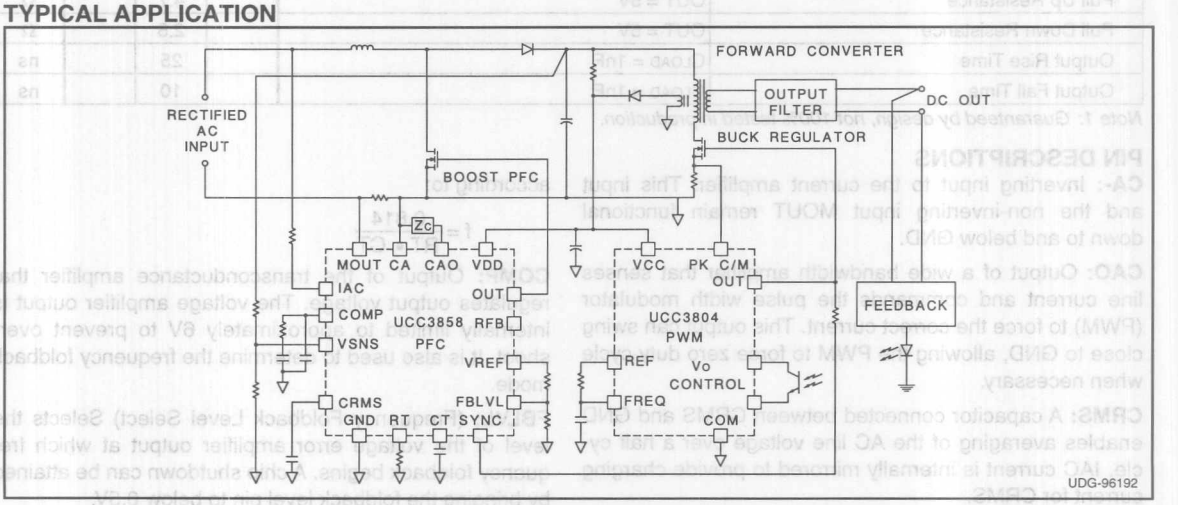
SYNC: Oscillator synchronization input. Allows for SYNC interface to trailing edge modulators in the DC-DC stage. Alternately, a synchronization pulse can be generated from the positive output edge of the downstream regulator. The internal clock is reset (charged up) on the rising edge of the SYNC input.

VDD: Positive supply voltage. Connect to a stable source of at least 20mA between 13V and 17V for normal operation. Bypass VDD directly to GND to absorb supply current spikes required to charge external MOSFET gate capacitance. To prevent inadequate gate drive signals, the output devices will be inhibited unless VDD exceeds the upper undervoltage lockout voltage threshold and remains above the lower threshold.

VREF: VREF is the output of an accurate 7.5V voltage reference. This output is capable of delivering 10mA to peripheral circuitry and is internally short circuit current limited. VREF is disabled and will remain at 0V when VDD is low. Bypass VREF to GND with a 0.1µF or larger ceramic capacitor for best stability.

VSNS: Voltage amplifier inverting input. This is normally connected to a feedback network and to the boost converter output through a divider network. It also is an input to the overvoltage comparator and the output is terminated if this pin exceeds 3.15V.

TYPICAL APPLICATION

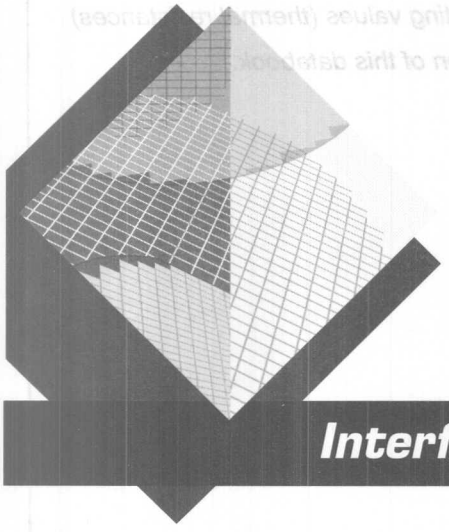


Typical Application Circuit

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Consult Applications Handbook for available applications/design notes.

Datasheets in this section are organized in numeric order using the commercial part number.



Interface/SCSI Circuits

6

Packaging Note:

- *Values listed for recommended lead soldering time and temperature apply to ceramic thru-hole components only. Please consult the Packaging Section of this databook for recommendations on plastic SMD board attach processing.*

- *Unless otherwise noted, thermal resistance values listed on individual data sheets are for the device as it operates in a plastic thru-hole package. Results for other packaging options can be inferred by scaling the package rating values (thermal resistances) presented in the Packaging Section of this databook.*

SCSI Active Terminators

SCSI Active Terminators	UNITRODE PART NUMBER				
	UC5601	UC5602	UC5603	UC5604	UC5605
Channels	18	18	9	9	9
Channel Capacitance	10	11	6	9	4
Termination Impedance	110	110	110	110	110
Disconnect High or Low	H	H	H	H	L
Termpwr Voltage Range	4 - 5.25	4 - 5.25	4 - 5.25	4 - 5.25	4 - 5.25
Supports Active Negation	N	N	Y	N	Y
SCSI Hot Plug Current (nA)	< 10	< 10	< 10	< 10	< 10
Type SE, LVD or SE/LVD	SE	SE	SE	SE	SE

SCSI Active Terminators (cont'd)	UNITRODE PART NUMBER				
	UCC5606	UC5607	UC5608	UC5609	UCC5610
Channels	9	18	18	18	18
Channel Capacitance	1.8	8	6	6	3
Termination Impedance	110 & 2500	110	110	110	110 & 2500
Disconnect High or Low	L	2L	H	L	H
Termpwr Voltage Range	2.7 - 5.25	4 - 5.25	4 - 5.25	4 - 5.25	2.7 - 5.25
Supports Active Negation	Y	Y	Y	Y	Y
SCSI Hot Plug Current (nA)	< 10	< 10	< 10	< 10	< 10
Type SE, LVD or SE/LVD	SE	SE	SE	SE	SE

SCSI Active Terminators (cont'd)	UNITRODE PART NUMBER				
	UCC5611	UC5612	UC5613	UCC5614	UCC5615✚
Channels	18	9	9	9	9
Channel Capacitance	3	4	3	1.8	1.8
Termination Impedance	110 & 2500	110	110	110 & 2500	110
Disconnect High or Low	L	H	H	H	L
Termpwr Voltage Range	2.7 - 5.25	4 - 5.25	4 - 5.25	2.7 - 5.25	4 - 5.25
Supports Active Negation	Y	Y	Y	Y	Y
SCSI Hot Plug Current (nA)	< 10	< 10	< 10	< 10	< 10
Type SE, LVD or SE/LVD	SE	SE	SE	SE	SE

✚ New Product

SCSI Active Terminators & Interface Drivers, Receivers & Transceivers

SCSI Active Terminators (cont'd)	UNITRODE PART NUMBER				
	UCC5616+	UCC5617+	UCC5618+	UCC5619+	UCC5620+
Channels	9	18	18	27	27
Channel Capacitance	1.8	2.5	2.5	3	3
Termination Impedance	110	110	110	110	110
Disconnect High or Low	H	L	H	L	H
Termpwr Voltage Range	4 - 5.25	4 - 5.25	4 - 5.25	4 - 5.25	4 - 5.25
Supports Active Negation	Y	Y	Y	Y	Y
SCSI Hot Plug Current (nA)	< 10	< 10	< 10	< 10	< 10
Type SE, LVD or SE/LVD	SE	SE	SE	SE	SE

SCSI Active Terminators (cont'd)	UNITRODE PART NUMBER				
	UCC5621+	UCC5622+	UCC5630+	UCC5632+	UCC5640+
Channels	27	27	9	9	9
Channel Capacitance	3	3	4	4	3
Termination Impedance	110	110	Single 110, Differential 105, Common Mode150	Single 110, Differential 105, Common Mode150	Differential 105, Common Mode150
Disconnect High or Low	2L	2H	H	H	H
Termpwr Voltage Range	4 - 5.25	4 - 5.25	2.7 - 5.25	2.7 - 5.25	2.7 - 5.25
Supports Active Negation	Y	Y	Y	Y	NA
SCSI Hot Plug Current (nA)	< 10	< 10	< 10	< 10	< 10
Type SE, LVD or SE/LVD	SE	SE	LVD/SE	LVD/SE	LVD

Interface Drivers, Receivers, Transceivers	UNITRODE PART NUMBER					
	UC5170C	UC5171	UC5172	UC5180C	UC5181C	UC5350+
Drivers	8	8	8			1
Receivers				8	8	1
Power	±10V	±10V	±10V	+5V	+5V	+5V
EIA232/V.28	Y	Y	Y	Y	Y	ISO 11898, CAN, Devicenet, & SDS
EIA423/V.10	Y	Y	Y	Y	Y	
EIA422/V.11	N	N	N	Y	Y	
V.35	N	N	N	Y	Y	
Appletalk	N	N	N	N	Y	

+ New Product

IrDA Products & Special Function Circuits

IrDA Products	UNITRODE PART NUMBER				
	UCC5340 ★	UCC5341 ✚ ★	UCC5342 ✚ ★	UCC5343 ✚ ★	UCC5344 ✚ ★
Device Type	Receiver	Receiver	Transceiver	Transceiver	Transceiver
Supply Voltage	3.3V or 5V	3.3V or 5V	3.3V or 5V	3.3V or 5V	3.3V or 5V
Data Rate	2.4kBPS to 115.2kBPS	2.4kBPS to 115.2kBPS	2.4kBPS to 115.2kBPS	2.4kBPS to 115.2kBPS	9.6kBPS to 4mBPS
Dynamic Range	150nA to 100mA	100nA to 100mA	100nA to 100mA	100nA to 100mA	100nA to 100mA
Quiescent Current	90µA	250µA	250µA	250µA	900µA
Encoder/Decoder	N	N	N	Y	N
IrDA Compliant	Y	Y	Y	Y	Y
LED Driver	NA	NA	500mA	500mA	500mA

Special Function Circuits	UNITRODE PART NUMBER			
	UC37131/2 ✚ ✖	UC560	UC5661	UCC5950
Part Name	Smart Power Switch	SCSI Single Ended Source/ Sink Regulator	Ethernet Coaxial Impedance Monitor	Digital to Analog Converter
Description	65V Universal High or Low Side Driver with Current Limiting	18 and 27 Line SCSI Termination Applications	Contains all the Functions Required to Monitor Ethernet Coaxial Systems and is Compatible with IEEE 802.3, 10Base5, 10Base2, and 10BaseT	10-Bit BiCMOS Digital to Analog Converter for Servo and Instrumentation Systems

✚ New Product
★ Refer to Portable Products Section for Product Data Sheet
✖ Refer to Power Drivers Section for Product Data Sheet

IrDA Products	Unitrode Part Number			
Device Type	Receiver	Receiver	Transceiver	Transceiver
Supply Voltage	3.3V or 5V	3.3V or 5V	3.3V or 5V	3.3V or 5V
Data Rate	2.4kBPS to 115.2kBPS	2.4kBPS to 115.2kBPS	2.4kBPS to 115.2kBPS	9.6kBPS to 4mBPS
Dynamic Range	100nA to 100mA	100nA to 100mA	100nA to 100mA	100nA to 100mA
Quiescent Current	90µA	250µA	250µA	900µA
Encoder/Decoder	N	N	N	Y
IrDA Compliant	Y	Y	Y	Y
LED Driver	NA	NA	500mA	500mA

Special Function Chips	Unitrode Part Number			
Part Name	Smart Power Switch	SCSI Single Ended Source/ Sink Regulator	Ethernet Coaxial Impedance Monitor	Digital to Analog Converter
Description	55V Universal Low Side Driver Current Limiting	Applications	Contains all the Functions Required to Monitor Ethernet Coaxial Systems and is Compatible with IEEE 802.3, 10Base5, 10Base2, and 10BaseT	10-Bit EDCMOS Digital to Analog Converter for Servo and Instrumentation Systems

✦ New Product
★ Refer to Portable Products Section for Product Data Sheet
✖ Refer to Power Drivers Section for Product Data Sheet

UNITRODE

Octal Line Driver

FEATURES

- Eight Single Ended Line Drivers in One Package
- Meets EIA Standards EIA232E/V.28, EIA423A and CCITT V.10/X.26
- Single External Resistor Controls Slew Rate
- Wide Supply Voltage Range
- Tri-State Outputs
- Output Short-Circuit Protection

DESCRIPTION

The UC5170C is a single-ended octal line driver designed to meet both standard modem control applications (EIA232E/V.28), and long line drive applications (EIA423A/V.10/X.26). The slew rate for all eight drivers is controlled by a single external resistor. The slew rate and output levels in Low Mode are independent of the power variations.

Mode selection is easily accomplished by taking the select pins (Ms+ and Ms-) to ground for low output mode (EIA232E/V.28 and EIA423A/V.10) or to their respective supplies for high mode (EIA232E/V.28). High mode should only by used to drive adapters that take power from the control lines, or applications using high threshold receivers.

ABSOLUTE MAXIMUM RATINGS (Note 1)

V+ (Pin 20) 15V
V- (Pin 11) . . . . . –15V
PLCC Power Dissipation, T_A = 25°C (Note 2) . . . . . 1000 mW
DIP Power Dissipation, T_A = 25°C (Note 2) . . . . . 1250 mW
Input Voltage . . . . . –1.5V to +7V
Output Voltage . . . . . –12V to +12V
Slew Rate Resistor . . . . . 2k to 10kΩ
Storage Temperature . . . . . –65°C to +150°C

Note 1: All voltages are with respect to ground, pin 18.
Note 2: Consult Packaging Section of Databook for thermal limitations and considerations of packages.

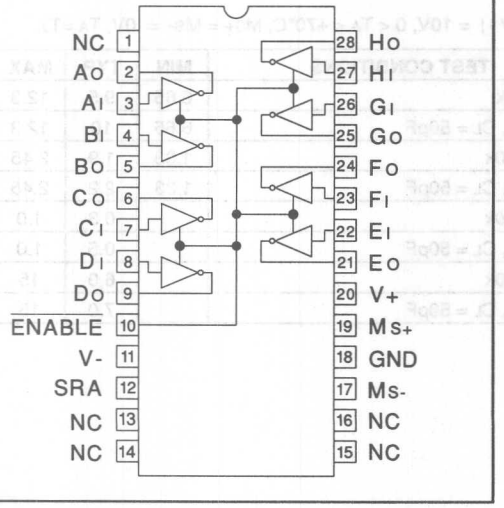
FUNCTIONAL TABLE

INPUTS		OUTPUTS	
		HIGH	LOW
$\overline{EN}$	DATA	EIA-232E[2]	EIA423A+EIA232E
0	0	(V+)-3V	5V to 6V
0	1	(V-)-3V	–5V to -6V
1	X	High Z	High Z

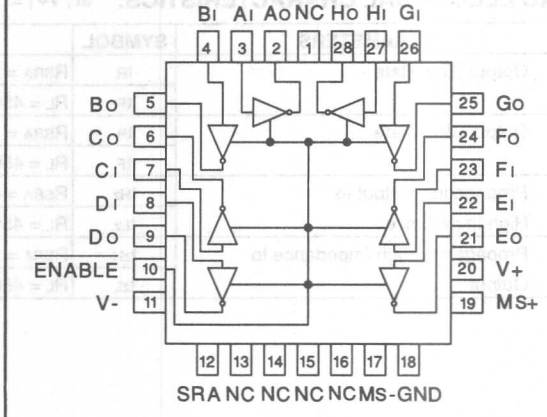
Note 2: Minimum output swings.

CONNECTION DIAGRAMS

N PACKAGE (TOP VIEW)



Q PACKAGE (TOP VIEW)



DC ELECTRICAL CHARACTERISTICS:

Unless otherwise stated these specifications hold for $|V+| = |V-| = 10V$, $0 < T_A < +70°C$, $M_{S+} = M_{S-} = 0V$, $R_{SRA} = +10k$, $T_A = T_J$.

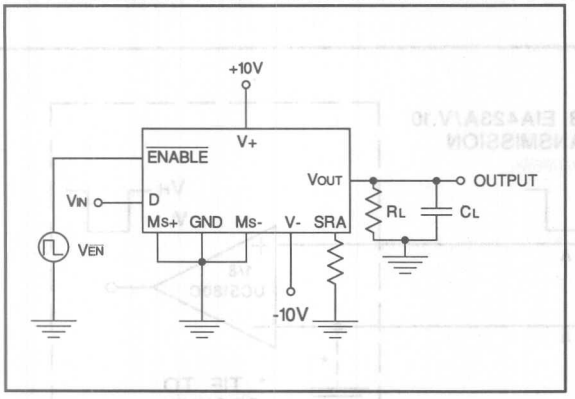
PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY REQUIREMENTS						
V+ Range			9		15	V
V- Range			-9		-15	V
V+ Supply Current	$I+$	R_L = Infinite $\overline{En}$ = 0V		25	42	mA
V- Supply Current	$I-$	R_L = Infinite $\overline{En}$ = 0V		-23	-42	mA
INPUTS						
High Level Input Voltage	V_{IH}		2.0			V
Low Level Input Voltage	V_{IL}				0.8	V
Input Clamp Voltage	V_{IK}	I_I = -15 mA		-1.1	-1.8	V
High Level Input Current	I_{IH}	V_{IH} = 2.4V		0.25	40	µA
Low Level Input Current	I_{IL}	V_{IL} = 0.4V	-200	-8.0		µA
OUTPUTS						
High Level (Low Mode) Output Voltage (EIA423A/V.10, EIA232E/V.28)	V_{OH}	V_{IN} = 0.8V R_L = Inf.	5.0	5.3	6.0	V
		$\overline{En}$ = 0.8V R_L = 3k	5.0	5.3	6.0	V
		R_L = 450	4.5	5.2	6.0	V
Low Level (Low Mode) Output Voltage (EIA423A/V.10,EIA232E/V.28)	V_{OL}	V_{IN} = 2.0V R_L = Inf.	-5.0	-5.3	-6.0	V
		$\overline{En}$ = 0.8V R_L = 3k	-5.0	-5.3	-6.0	V
		R_L = 450	-4.5	-5.2	-6.0	V
Output Balance (EIA423A/V.10)	V_{BAL}	R_L = 450 $V_{OH} - V_{OL} = V_{BAL}$		0.2	0.4	V
High Level (High Mode) Output Voltage (EIA232E/V.28)	V_{OH}	V_{IN} = 0.8V R_L = Inf., M_{S+} = V+, M_{S-} = V-	7.0	7.6	10	V
		$\overline{En}$ = 0.8V R_L = 3k, M_{S+} = V+, M_{S-} = V-	7.0	7.6	10	V
Low Level (High Mode) Output Voltage (EIA232E, V.28)	V_{OL}	V_{IN} = 2.0V R_L = Inf., M_{S+} = V+, M_{S-} =V-	-7.0	-7.7	-10	V
		En = 0.8V R_L = 3k, M_{S+} = V+, M_{S-} = V-	-7.0	-7.7	-10	V
Off-State Output Current	I_{OZ}	$\overline{En}$ = 2.0V, V_O = ±6V, V+ = 15V, V- = -15V	-100		100	µA
Short-Circuit Current	I_{OS}	V_{IN} = 0V, $\overline{En}$ = 0V	25	50		mA
		V_{IN} = 5V, $\overline{En}$ = 0V	25	40		mA

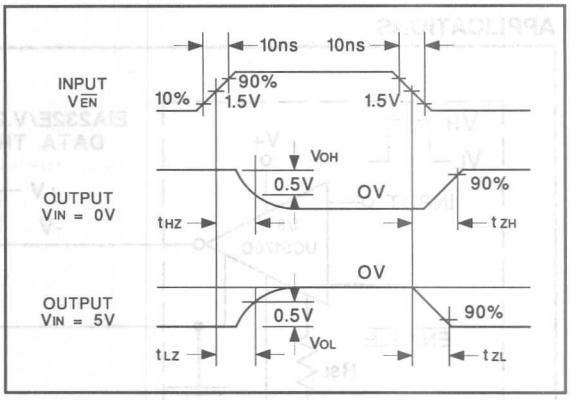
AC ELECTRICAL CHARACTERISTICS:

at $|V+| = |V-| = 10V$, $0 < T_A < +70°C$, $M_{S+} = M_{S-} = 0V$, $T_A = T_J$.

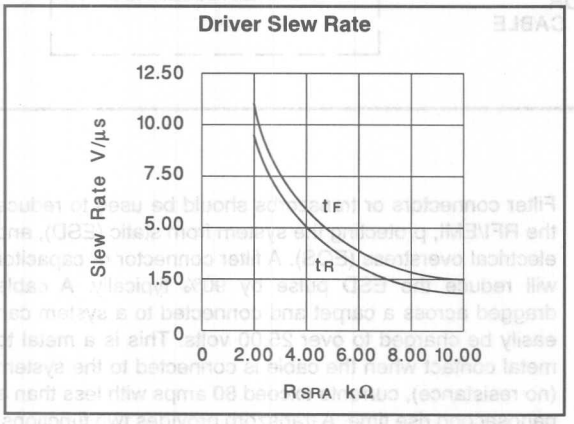
PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Slew Rate	t_R	R_{SRA} = 2k	6.65	9.5	12.3	V/µs
	t_F	R_L = 450, C_L = 50pF	6.65	10	12.3	V/µs
Output Slew Rate	t_R	R_{SRA} = 10k	1.33	1.9	2.45	V/µs
	t_F	R_L = 450, C_L = 50pF	1.33	2.2	2.45	V/µs
Propagation Output to High Impedance	t_{HZ}	R_{SRA} = 10k		0.3	1.0	µs
	t_{LZ}	R_L = 450, C_L = 50pF		0.5	1.0	µs
Propagation High Impedance to Output	t_{ZH}	R_{SRA} = 10k		6.0	15	µs
	t_{ZL}	R_L = 450, C_L = 50pF		7.0	15	µs

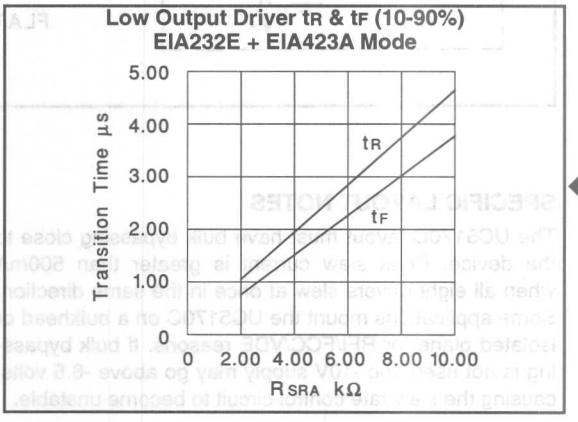
AC PARAMETER TEST CIRCUIT AND WAVEFORMS





AC CHARACTERISTICS





APPLICATION INFORMATION

Slew Rate Programming

Slew rate for the UC5170C is set up by a single external resistor connected between the SRA pin and ground. Slew rate adjustments can be approximated by using the following formula:

$$V/\mu s = \frac{20}{R_{SRA}} \; (R_{SRA} \text{ in k } \Omega)$$

The slew rate resistor can vary between 2k and 10k which allows slew rates between 10 to 2.2V/µs, respectively. The relationship between slew rate and RSRA is shown in the typical characteristics.

Waveshaping of the output lets the user control the level of interference (near-end crosstalk) that may be coupled to adjacent circuits in an interconnection. The recommended output characteristics for cable length and data rates can be found in EIA standard EIA423A +V.10. Approximations of these standards are given by the following equations:

Max. Data Rate = 300/t (For data rates 1k to 100k bit/s)

Max. Cable Length (feet) = 100 x t (Max. length 4000 *feet)*

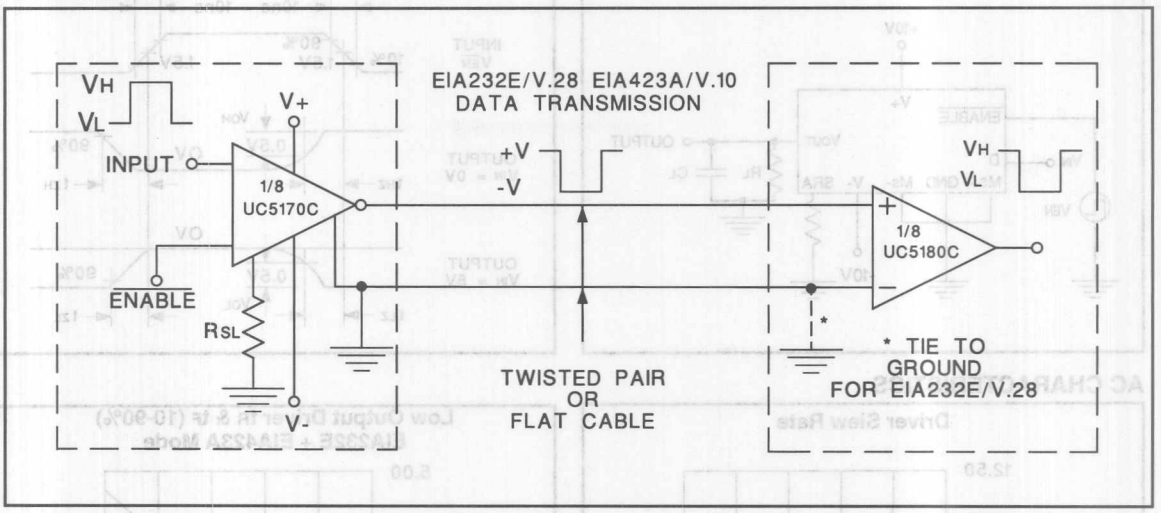
where t is the transition time from 10% to 90% of the output swing in microseconds. For data rates below 1k bit/s t may be up to 300 microseconds.

Output Voltage Programming

The UC5170C has two programmable output modes, either a low voltage mode which meets EIA423A, EIA232E/V.28/V.10 specifications, or the high output mode which meets the EIA232E, V.28 specifications.

The high output mode provides greater output swings, minimum of 3V below and supply rails for driving higher, attenuated lines. This mode is selected by connecting the mode select pins to their respected supplies, MS+ to V+ and MS- to V-.

APPLICATIONS



SPECIFIC LAYOUT NOTES

The UC5170C layout must have bulk bypassing close to the device. Peak slew current is greater than 500mA when all eight drivers slew at once in the same direction. Some applications mount the UC5170C on a bulkhead or isolated plane for RFI/FCC/VDE reasons. If bulk bypassing is not used, the -10V supply may go above -8.5 volts, causing the slew rate control circuit to become unstable.

The UC5170C can have output oscillation at 100kHz if the +10V supply is applied before the -10V supply. This has been a problem in some terminal designs where the +10V was developed from the flyback, which can result in a 500ms difference in the application of the supplies at power up.

GENERAL LAYOUT NOTES

The drivers and receivers should be mounted close to the system common ground point, with the ground reference tied to the common point to reduce RFI/EMI.

Filter connectors or transzorbs should be used to reduce the RFI/EMI, protecting the system from static (ESD), and electrical overstress (EOS). A filter connector or capacitor will reduce the ESD pulse by 90% typically. A cable dragged across a carpet and connected to a system can easily be charged to over 25,00 volts. This is a metal to metal contact when the cable is connected to the system (no resistance), currents exceed 80 amps with less than a nanosecond rise time. A transzorb provides two functions, the device capacitance inherently acts as a filter capacitor, and the device clamps the ESD and EOS pulses which would pass through the capacitor and destroy the devices. The recommended transzorb for the UC5170C is P6KEIOCA.

*Transzorb is a trademark of General Semiconductor Industries.

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UNITRODE

Octal Line Driver

FEATURES

- Eight Single-Ended Line Drivers in One Package
- Digital Selection of High Mode EIA232E/CCITT V.28 only, and Low Mode EIA232E/V.28 & EIA423A/CCITT V.10/X.26
- Single External Resistor Controls Slew Rate
- Wide Supply Voltage Range
- Tri-State Outputs
- Output Short-Circuit Protection
- Low Power Consumption
- 2kV ESD Protection on all Pins

DESCRIPTION

The UC5171 is a single-ended octal line driver designed to meet both standard modem control applications (EIA232E/V.28), and long line drive applications (EIA423A/V.10/X.26). The slew rate for all 8 drivers is controlled by a single external resistor. The slew rate and output levels in Low Mode are independent of the power variations.

Mode selection is accomplished by the select pin Ms logic "low" for low output mode (EIA232E/V.28 & EIA423A/V.10) or pin Ms logic "high" for high mode (EIA232E/V.28). High mode should only be used to drive adapters that take power from the control lines, or applications using high threshold receivers.

ABSOLUTE MAXIMUM RATINGS (Note 1)

V+ (Pin 20) 15V
V- (Pin 11) . . . . . -15V
PLCC Power Dissipation, T_A = 25°C (Note 2) . . . . . 1000 mW
DIP Power Dissipation, T_A = 25°C (Note 2) . . . . . 1250 mW
Input Voltage . . . . . -1.5V to +7V
Output Voltage . . . . . -12V to +12V
Slew Rate Resistor . . . . . 2k to 10kΩ
Storage Temperature . . . . . -65°C to +150°C

Note 1: All voltages are with respect to ground, pin 18.
Note 2: Consult Packaging section of Databook for thermal limitations and considerations of package.

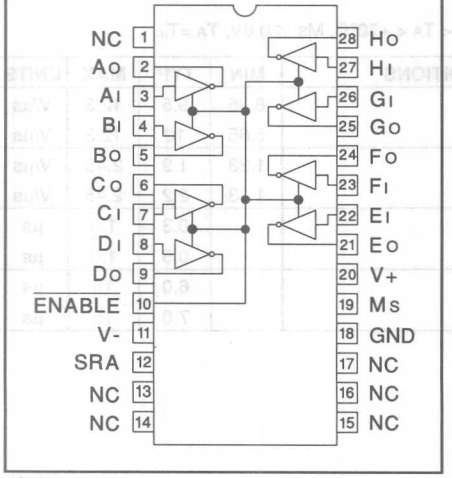
FUNCTIONAL TABLE

INPUTS		OUTPUTS	
$\overline{EN}$	DATA	EIA-232E(3)	EIA-232E/EIA-423A
0	0	(V+)-3V	5V to 6V
0	1	(V-)+3V	-5V to -6V
1	X	High Z	High Z

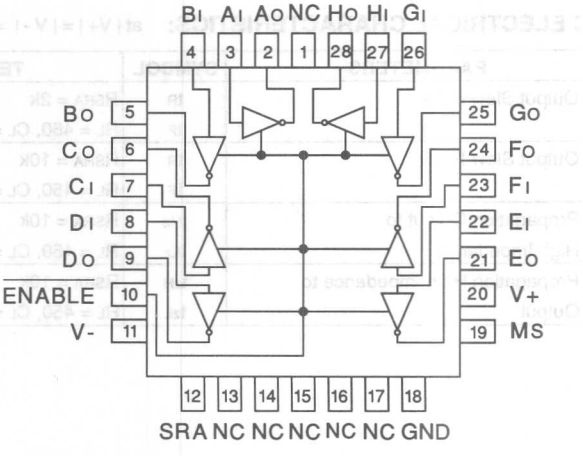
Note 3: Minimum output swings.

CONNECTION DIAGRAMS

N PACKAGE (TOP VIEW)



Q PACKAGE (TOP VIEW)



7/95

DC ELECTRICAL CHARACTERISTICS:

Unless otherwise stated these specifications hold for $|V+| = |V-| = +10V$, $0 < T_A < +70°C$, $M_S \leq 0.8V$, $R_{SRA} = +10k$, $T_A = T_J$.

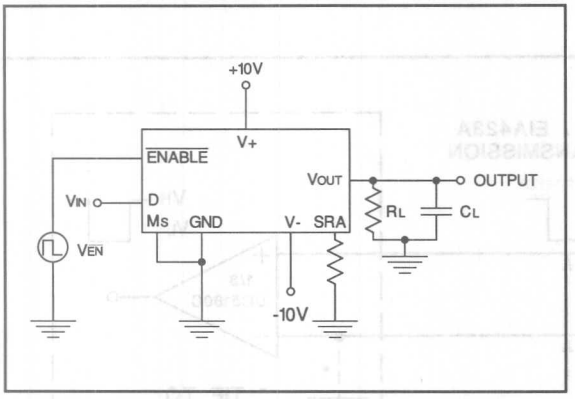
PARAMETERS	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLY REQUIREMENTS							
V+ Range				9		15	V
V- Range				-15		-9	V
V+ Supply Current	$I+$	R_L = Infinite $\overline{En}$ = 0V			25	42	mA
V- Supply Current	$I-$	R_L = Infinite $\overline{En}$ = 0V		-42	-23		mA
INPUTS							
High Level Input Voltage	V_{IH}			2.0			V
Low Level Input Voltage	V_{IL}					0.8	V
Input Clamp Voltage	V_{IK}	I_I = -15 mA		-1.8	-1.1		V
High Level Input Current	I_{IH}	V_{IH} = 2.4V			0.25	40	µA
Low Level Input Current	I_{IL}	V_{IL} = 0.4V		-200	-8.0		µA
OUTPUTS							
High Level	V_{OH}	V_{IN} = 0.8V	R_L = Inf.	5.0	5.3	6.0	V
Output Voltage EIA232E		$\overline{En}$ = 0.8V	R_L = 3k	5.0	5.3	6.0	V
(EIA423A)			R_L = 450	4.5	5.2	6.0	V
Low Level	V_{OL}	V_{IN} = 2.0V	R_L = Inf.	-6.0	-5.3	-5.0	V
Output Voltage EIA232E		$\overline{En}$ = 0.8V	R_L = 3k	-6.0	-5.3	-5.0	V
(EIA423A)			R_L = 450	-6.0	-5.2	-4.5	V
Output Balance (EIA423A)	V_{BAL}	R_L = 450	$V_{OH} + V_{OL} = V_{BAL}$		0.2	0.4	V
High Level	V_{OH}	V_{IN} = 0.8V, M_S = 2.0V	R_L = Inf.	7.0	7.6	10	V
Output Voltage (EIA232E)		$\overline{En}$ = 0.8V	R_L = 3k	7.0	7.6	10	V
Low Level Output Voltage	V_{OL}	V_{IN} = 2.0V, M_S = 2.0V	R_L = Inf.	-10	-7.7	-7.0	V
(EIA232E)		En = 0.8V	R_L = 3k	-10	-7.7	-7.0	V
Off-State Output Current	I_{OZ}	$\overline{En}$ = 2.0V, V_O = ±6V, M_S = 2.0V		-100		100	µA
Short-Circuit Current	I_{OS}	$\overline{En}$ = 0V	V_{IN} = 0V	25	50		mA
			V_{IN} = 5V	25	40		mA

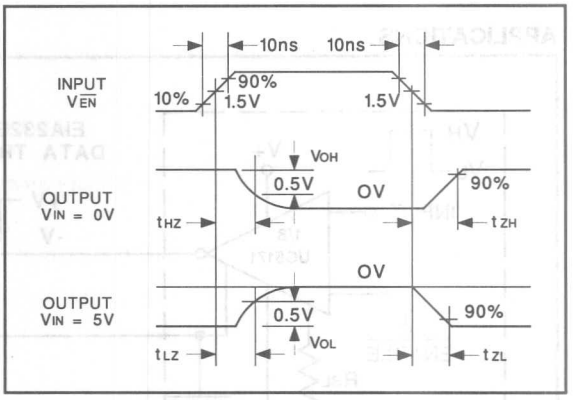
AC ELECTRICAL CHARACTERISTICS:

at $|V+| = |V-| = +10V$, $0 < T_A < +70°C$, $M_S \leq 0.8V$, $T_A = T_J$.

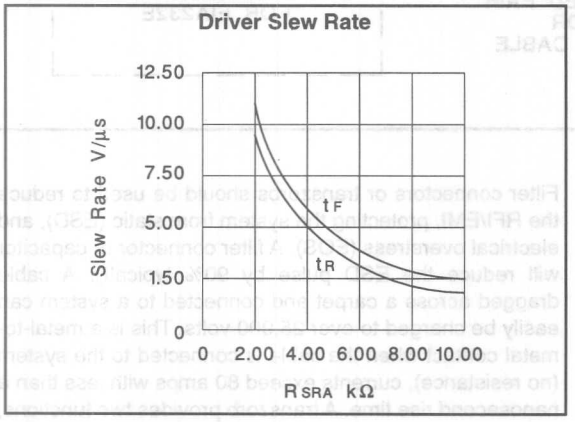
PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Slew Rate	t_R	R_{SRA} = 2k	6.65	9.5	12.3	V/µs
	t_F	R_L = 450, C_L = 50pF	6.65	10	12.3	V/µs
Output Slew Rate	t_R	R_{SRA} = 10k	1.33	1.9	2.45	V/µs
	t_F	R_L = 450, C_L = 50pF	1.33	2.2	2.45	V/µs
Propagation Output to	t_{HZ}	R_{SRA} = 10k		0.3	1.0	µs
High Impedance	t_{LZ}	R_L = 450, C_L = 50pF		0.5	1.0	µs
Propagation High Impedance to	t_{ZH}	R_{SRA} = 10k		6.0	15	µs
Output	t_{ZL}	R_L = 450, C_L = 50pF		7.0	15	µs

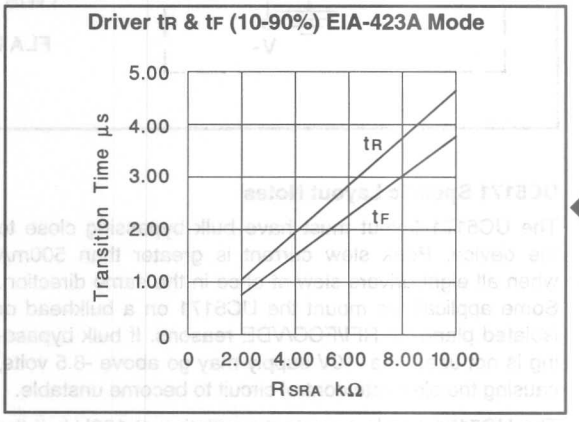
AC PARAMETER TEST CIRCUIT AND WAVEFORMS





AC CHARACTERISTICS





APPLICATIONS INFORMATION

Slew Rate Programming

Slew rate for the UC5171 is set up by a single external resistor connected between the SRA pin and ground. Slew rate adjustments can be approximated by using the following formula:

$$V/\mu s = \frac{20}{R_{SRA}} \; (R_{SRA} \text{ in } k\Omega)$$

The slew rate resistor can vary between 2k and 10kΩ which allows slew rates between 10 to 2.2V/µs, respectively. The relationship between slew rate and RSRA is shown in the typical characteristics.

Waveshaping of the output lets the user control the level of interference (near-end crosstalk) that may be coupled to adjacent circuits in an interconnection. The recommended output characteristics for cable length and data rates can be found in EIA standard EIA-423A. Approximations of these standards are given by the following equations:

Max. Data Rate=300/t (For data rates 1k to 100k bit/s)

Max. Cable Length (feet)=100 x t (Max. length 4000 feet)

where t is the transition time from 10% to 90% of the output swing in microseconds. For data rates below 1k bit/s, t may be up to 300 microseconds.

Output Voltage Programming

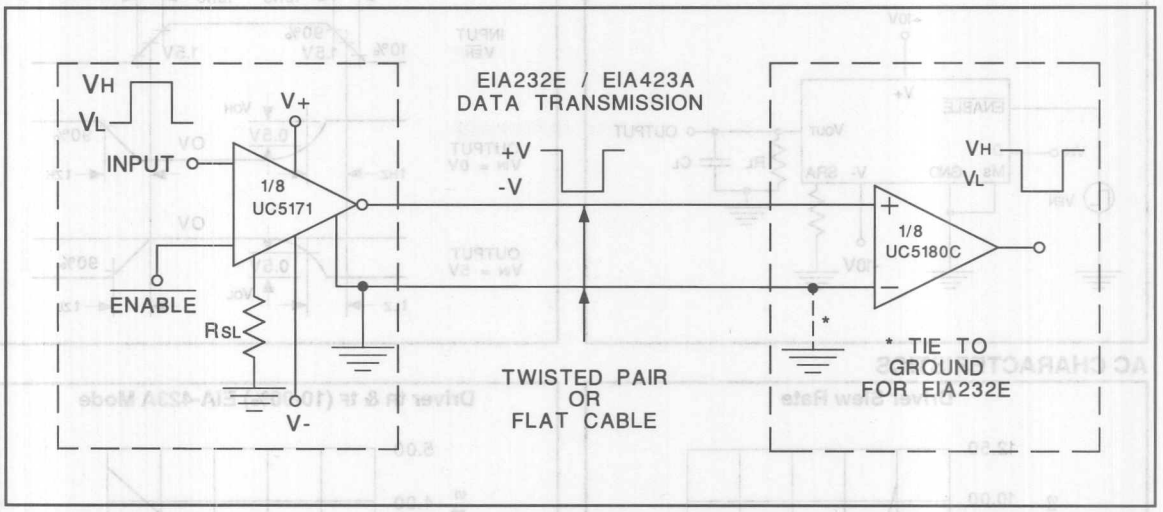
The UC5171 has two programmable output modes, either a low voltage mode which meets EIA-423A operational specifications, or the high output voltage mode which meets the EIA-232E specifications.

The high output mode provides greater output swings, minimum of 3V below the supply rails, for driving higher, attenuated lines. This mode is selected by connecting the modes select pin, (MS), to a TTL "high" level. The low output mode provides a controlled output swing and is accomplished by connecting the mode select pin, (Ms), to a TTL "low level."

EIA Standards

The UC5171 meets or exceeds the EIA Standards for EIA-232E and EIA-423A modes of operation except under power down conditions. When powered down with the output attached to an active buss, the UC5171 has the potential to load the bus under transient conditions.

APPLICATIONS



UC5171 Specific Layout Notes

The UC5171 layout must have bulk bypassing close to the device. Peak slew current is greater than 500mA when all eight drivers slew at once in the same direction. Some applications mount the UC5171 on a bulkhead or isolated plane for RFI/FCC/VDE reasons. If bulk bypassing is not used, the -10V supply may go above -8.5 volts, causing the slew rate control circuit to become unstable.

The UC5171 can have output oscillation at 100kHz if the +10V supply is applied before the -10V supply. This has been a problem in some terminal designs where the +10V was developed from the flyback, which can result in a 500ms difference in the application of the supplies at power up.

General Layout Notes

The drivers and receivers should be mounted close to the system common ground point, with the ground reference tied to the common point to reduce RFI/EMI.

Filter connectors or transzorbs should be used to reduce the RFI/EMI, protecting the system from static (ESD), and electrical overstress (EOS). A filter connector or capacitor will reduce the ESD pulse by 90% typically. A cable dragged across a carpet and connected to a system can easily be charged to over 25,000 volts. This is a metal-to-metal contact when the cable is connected to the system (no resistance), currents exceed 80 amps with less than a nanosecond rise time. A transzorb provides two functions, the device capacitance inherently acts as a filter capacitor, and the device clamps the ESD and EOS pulses which would pass through the capacitor and destroy the devices. The recommended transzorb for the UC5171 is P6KEIOCA

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UNITRODE

Octal Line Driver

FEATURES

- Eight Single-Ended Line Drivers in One Package
- Meets Standards EIA232E/CCITT V.28, and EIA423A/CCITT V.10/X.26
- Single External Resistor Controls Slew Rate
- Wide Supply Voltage Range
- Tri-State Outputs
- Output Short-Circuit Protection
- Low Power Consumption
- 2kV ESD Protection on all Pins
- EOS on all Output Pins 35V under all Output Conditions
- High Current Output for Long Line Drive, Exceeds Standards

DESCRIPTION

The UC5172 is a single-ended octal line driver designed to meet both standard modem control applications (EIA232E/V.28), and long line drive applications (EIA423A/V.10/X.26). The slew rate for all 8 drivers is controlled by a single external resistor. The slew rate and output levels are independent of the power variations.

The UC5172 has high output current, and current balance for long line drive applications. EOS - Output parasitic SCRs powered on and off are 35V, well above signal levels, allowing protection devices to work.

Inputs are compatible TTL+MOS logic families and are diode protected against negative transients.

FUNCTIONAL TABLE

INPUTS		OUTPUT
$\overline{EN}$	DATA	EIA232E/EIA423A
0	0	5V to 6V
0	1	-5V to -6V
1	X	High Z

Note 2: Minimum output swings.

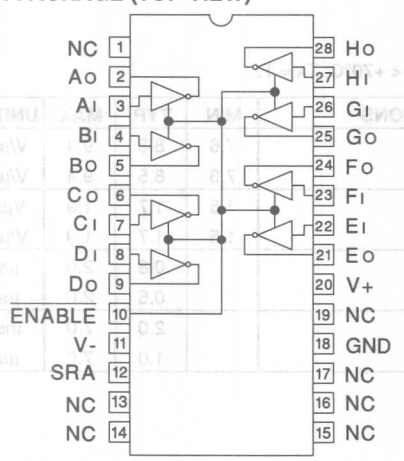
ABSOLUTE MAXIMUM RATINGS (Note 1)

V+ (Pin 20) 15V
V- (Pin 11) . . . . . -15V
PLCC Power Dissipation, T_A=25°C (Note 3) . . . . . 1000 mW
DIP Power Dissipation, T_A=25°C (Note 3) . . . . . 1250 mW
Input Voltage . . . . . -1.5V to +7V
Output Voltage . . . . . -6V to +6V
Slew Rate Resistor . . . . . 2k to 10kΩ
Storage Temperature . . . . . -65°C to +150°C

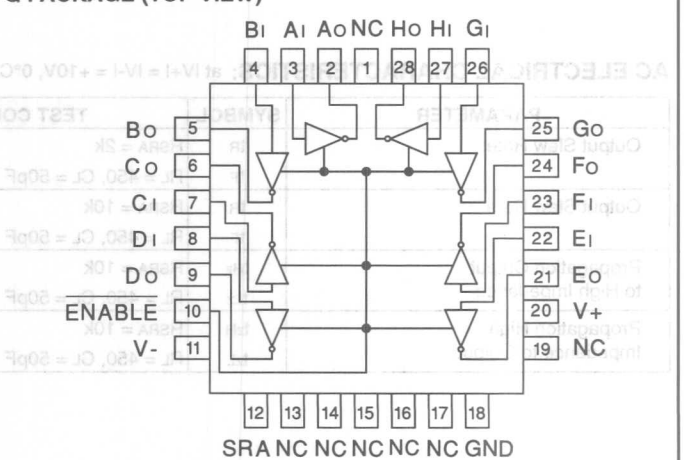
Note 1: All voltages are with respect to ground, pin 18.
Note 3: Consult Packaging section of Databook for thermal limitations and considerations of package.

CONNECTION DIAGRAMS

N PACKAGE (TOP VIEW)



Q PACKAGE (TOP VIEW)



9/96

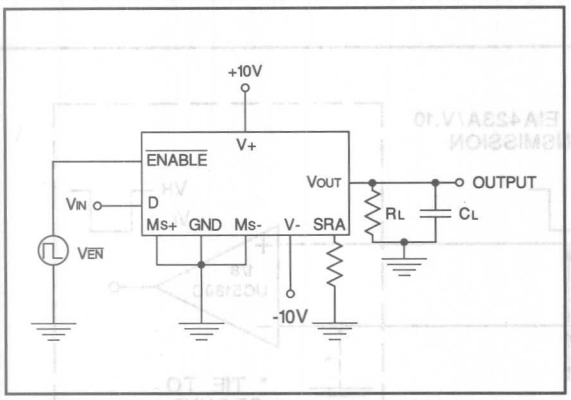
DC ELECTRICAL CHARACTERISTICS: Unless otherwise stated these specifications hold for $|V+| = |V-| = 10V$, $0°C < T_A < +70°C$, $R_{SRA} = +10k$, $T_A = T_J$.

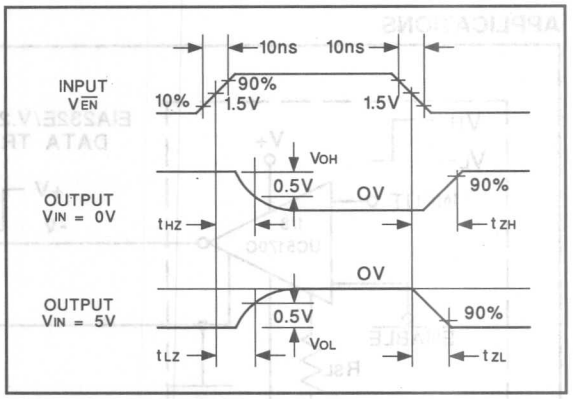
PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLY REQUIREMENTS							
V+ Range				9		15	V
V- Range				-9		-15	V
V+ Supply Current	I+	R_L = Infinite $\overline{En}$ = 0V			15	25	mA
V- Supply Current	I-	R_L = Infinite $\overline{En}$ = 0V			-17	-25	mA
INPUTS							
High-Level Input Voltage	V_{IH}			2.0			V
Low-Level Input Voltage	V_{IL}					0.8	V
Input Clamp Voltage	V_{IK}	I_I = -15 mA			-1.1	-18	V
High Level Input Current	I_{IH}	V_{IH} = 2.4V		-2	0.25	40	µA
Low Level Input Current	I_{IL}	V_{IL} = 0.4V		-200	-8.0		µA
OUTPUTS							
High Level Output Voltage	V_{OH}	V_{IN} = 0.8V	R_L = Inf.	5.0	5.3	6.0	V
EIA232E		$\overline{En}$ = 0.8V	R_L = 3k	5.0	5.3	6.0	V
(EIA-423A)			R_L = 450	4.5	5.2	6.0	V
Low Level Output Voltage	V_{OL}	V_{IN} = 2.0V	R_L = Inf.	-5.0	-5.3	-6.0	V
EIA232E		$\overline{En}$ = 0.8V	R_L = 3k	-5.0	-5.6	-6.0	V
(EIA-423A)			R_L = 450	-4.5	-5.4	-6.0	V
Output Balance (EIA-423A)	V_{BAL}	R_L = 450, $V_{OH} - V_{OL} = V_{BAL}$			0.2	0.4	V
Off-State Output Current	I_{OZ}	$\overline{En}$ = 2.0V, V_O = ±6V, V+ = 15V, V– = -15V		-100		100	µA
Short-Circuit Current	I_{OS}	$\overline{En}$ = 0V	V_{IN} = 0V	25	65		mA
			V_{IN} = 5V	25	70		mA
Power Off Output Current	I_{PO}	V_O = ±6V, V+ = V– = 0V		-100		100	mA

AC ELECTRICAL CHARACTERISTICS: at $|V+| = |V-| = +10V$, $0°C < T_A < +70°C$, $T_A = T_J$.

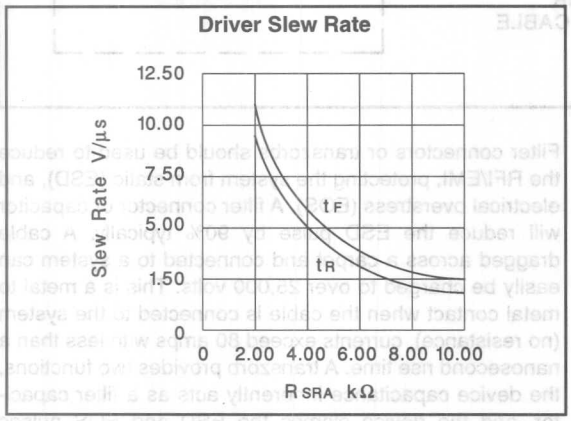
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Slew Rate	t_R	R_{SRA} = 2k	7.6	8.5	9.4	V/µs
	t_F	R_L = 450, C_L = 50pF	7.6	8.5	9.4	V/µs
Output Slew Rate	t_R	R_{SRA} = 10k	1.5	1.7	1.9	Vµs
	t_F	R_L = 450, C_L = 50pF	1.5	1.7	1.9	V/µs
Propagation Output to High Impedance	t_{HZ}	R_{SRA} = 10k		0.8	2.0	µs
	t_{LZ}	R_L = 450, C_L = 50pF		0.5	2.0	µs
Propagation High Impedance to Output	t_{ZH}	R_{SRA} = 10k		2.0	7.0	ms
	t_{ZL}	R_L = 450, C_L = 50pF		1.0	7.0	µs

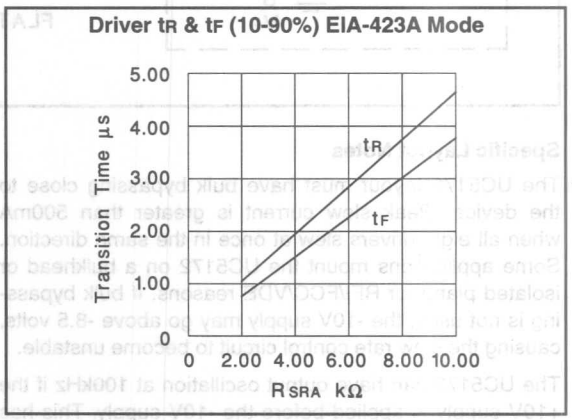
AC PARAMETER TEST CIRCUIT AND WAVEFORMS





AC CHARACTERISTICS





APPLICATIONS

Slew Rate Programming

Slew rate for the UC5172 is set up by a single external resistor connected between the SRA pin and ground. Slew rate adjustments can be approximated by using the following formula:

$$V/\mu s = \frac{20}{R_{SRA}} \text{ (RSRA in k}\Omega\text{)}$$

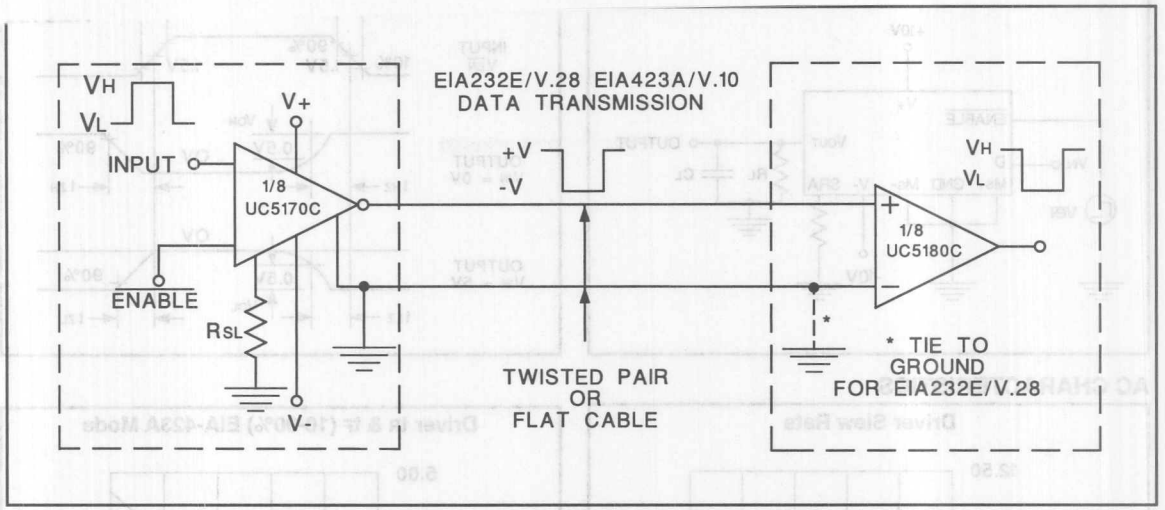
The slew rate resistor can vary between 2k and 10kΩ which allows slew rates between 10 to 2.2V/µs, respectively. The relationship between slew rate and RSRA is shown in the typical characteristics.

Waveshaping of the output lets the user control the level of interference (near-end crosstalk) that may be coupled to adjacent circuits in an interconnection. The recommended output characteristics for cable length and data rates can be found in EIA standard EIA-423A. Approximations of these standards are given by the following equations:

Max. Data Rate = 300/t (For data rates 1k to 100k bit/s)
Max. Cable Length (feet) = 100 x t (Max. length 4000 feet)

where t is the transition time from 10% to 90% of the output swing in microseconds. For data rates below 1k bit/s, t may be up to 300 microseconds.

The UC5172 has been used in applications up to 460KBPS.



Specific Layout Notes

The UC5172 layout must have bulk bypassing close to the device. Peak slew current is greater than 500mA when all eight drivers slew at once in the same direction. Some applications mount the UC5172 on a bulkhead or isolated plane for RFI/FCC/VDE reasons. If bulk bypassing is not used, the -10V supply may go above -8.5 volts, causing the slew rate control circuit to become unstable.

The UC5172 can have output oscillation at 100kHz if the +10V supply is applied before the -10V supply. This has been a problem in some terminal designs where the +10V was developed from the flyback, which can result in a 500ms difference in the application of the supplies at power up.

General Layout Notes

The drivers and receivers should be mounted close to the system common ground point, with the ground reference tied to the common point to reduce RFI/EMI.

Filter connectors or transzorbs should be used to reduce the RFI/EMI, protecting the system from static (ESD), and electrical overstress (EOS). A filter connector or capacitor will reduce the ESD pulse by 90% typically. A cable dragged across a carpet and connected to a system can easily be charged to over 25,000 volts. This is a metal to metal contact when the cable is connected to the system (no resistance), currents exceed 80 amps with less than a nanosecond rise time. A transzorb provides two functions, the device capacitance inherently acts as a filter capacitor, and the device clamps the ESD and EOS pulses which would pass through the capacitor and destroy the devices. The recommended transzorb for the UC5172 is P6KEIOCA.

*Transzorb is a trademark of General Semiconductor Industries.

UNITRODE CORPORATION
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TEL. (603) 424-2410 • FAX (603) 424-3460

UNITRODE

Octal Line Receiver

FEATURES

- Meets EIA 232E/423A/422A and CCITT V.10,V.11, V.28, X.26, X.27
- Single +5V Supply--TTL Compatible Outputs
- Differential Inputs Withstand ± 25V
- Low Open Circuit Voltage for Improved Failsafe Characteristic
- Reduced Supply Current--35 mA Max
- Input Noise Filter
- Internal Hysteresis

DESCRIPTION

The UC5180C is an octal line receiver designed to meet a wide range of digital communications requirements as outlined in EIA standards EIA232E, EIA423A, EIA422A, and CCITT V.10, V.11, V.28, X.26, and X.27. The UC5180C includes an input noise filter and is intended for applications employing data rates up to 200 KBPS. A failsafe function allows these devices to "fail" to a known state under a wide variety of fault conditions at the inputs.

ABSOLUTE MAXIMUM RATINGS (Note 1)

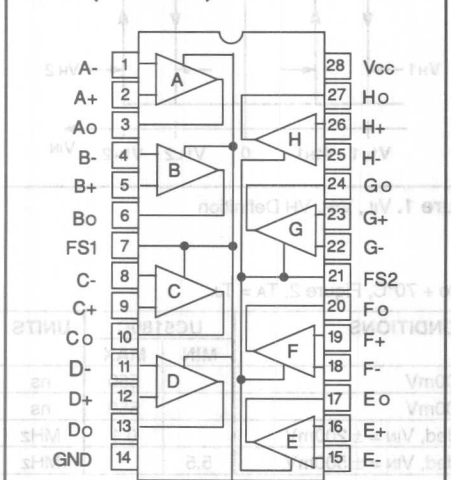
Supply Voltage, Vcc	7V
Output Sink Current	50 mA
Output Short Circuit Time	1 Sec
Common Mode Input Range	15V
Differential Input Range	25V
Failsafe Voltage	-0.3 to Vcc
PLCC Power Dissipation, T_A = 25°C (Note 2)	1000 mW
DIP Power Dissipation, T_A = 25°C (Note 2)	1200 mW
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 Seconds)	-300°C

Note 1: All voltages are with respect to ground, pin 14. Currents are positive into, negative out of the specified terminal

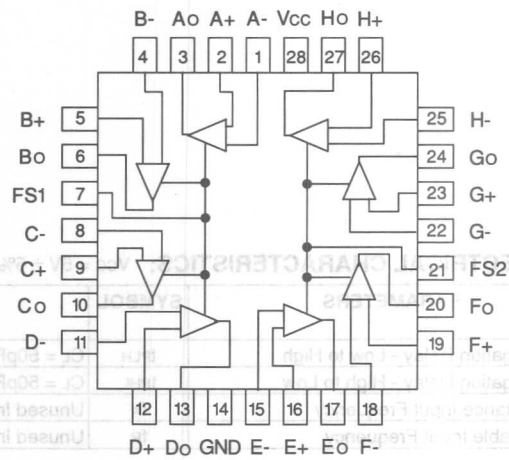
Note 2: Consult Packaging Section of Databook for thermal limitations and considerations of package.

CONNECTION DIAGRAMS

DIL-28 (TOP VIEW)



PLCC-28 (TOP VIEW)



DC ELECTRICAL CHARACTERISTICS: Unless otherwise stated these specifications apply for T_A = 0°C to +70°C, V_{CC} = 5V ± 5%, Input Common Mode Range ± 7V, T_A = T_J

PARAMETERS	SYMBOL	TEST CONDITIONS		UC5180C MIN	UC5180C MAX	UNITS
DC Input Resistance	R_{IN}	3V ≤ | V_{IN} | ≤ 25V		3	7	kΩ
Failsafe Output Voltage	V_{OFS}	Inputs Open or Shorted Together, or One Input Open and One Grounded	0 ≤ I_{OUT} ≤ 8mA, $V_{FAILSAFE}$ = 0V		0.45	V
			0 ≥ I_{OUT} ≥ - 400 µA, $V_{FAILSAFE}$ = V_{CC}	2.7		
Differential Input High Threshold	V_{TH}	V_{OUT} = 2.7V, I_{OUT} = 440 µA (See Figure 1)	R_S = 0 (Note 2)	50	200	mV
			R_S = 500 (Note 2)		400	
Differential Input Low Threshold	V_{TL}	V_{OUT} = 0.45V, I_{OUT} = 440 mA (See Figure 1)	R_S = 0 (Note 2)	-200	-50	mV
			R_S = 500 (Note 2)	-400		
Hysteresis	V_H	F_S = 0V or V_{CC} (See Figure 1)		50	140	mV
Open Circuit Input Voltage	V_{ICC}				75	mV
Input Capacitance	C_I				20	pF
High Level Output Voltage	V_{CH}	V_{ID} = 1V, I_{OUT} = - 440µA		2.7		V
Low Level Output Voltage	V_{OL}	V_{ID} = -1V (Note 3)	I_{OUT} = 4 mA		0.4	V
			I_{OUT} = 8 mA		0.45	
Short Circuit Output Current	I_{OS}	Note 4		20	100	mA
Supply Current	I_{CC}	4.75V ≤ V_{CC} ≤ 5.25V			35	mA
Input Current	I_{IN}	Other Inputs Grounded	V_{IN} = +10V		3.25	mA
			V_{IN} = -10V	-3.25		

Note 2: Rs is a resistor in series with each input.
Note 3: Measured after 100ms warm up (at 0°C)
Note 4: Only 1 output may be shorted at one time and then only for a maximum of 1 sec.

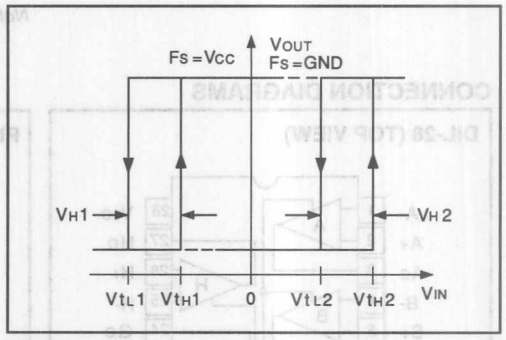


Figure 1. VtL, VtH, VH Definition

AC ELECTRICAL CHARACTERISTICS: V_{CC} = 5V ± 5%, T_A = 0°C to + 70°C, Figure 2, T_A = T_J.

PARAMETERS	SYMBOL	TEST CONDITIONS	UC5180C MIN	UC5180C MAX	UNITS
Propagation Delay - Low to High	t_{PLH}	C_L = 50pF, V_{IN} = ± 500mV		550	ns
Propagation Delay - High to Low	t_{PHL}	C_L = 50pF, V_{IN} = ± 500mV		550	ns
Acceptance Input Frequency	f_A	Unused Input Grounded, V_{IN} = ± 200mV		0.1	MHz
Rejectable Input Frequency	f_R	Unused Input Grounded, V_{IN} = ± 500mV	5.5		MHz

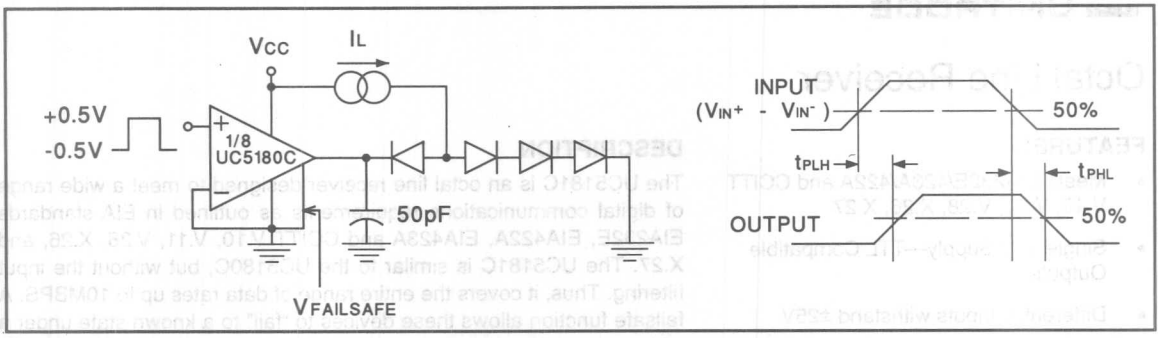


Figure 2. AC Test Circuit

APPLICATIONS INFORMATION

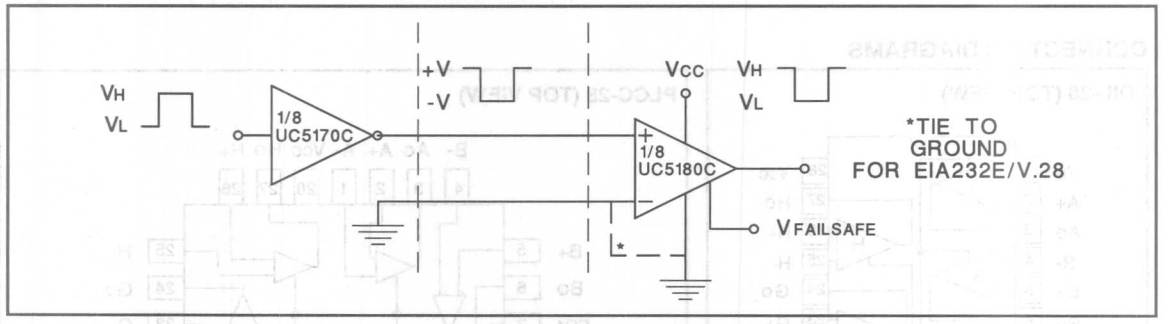
Failsafe Operation

These devices provide a failsafe operating mode to guard against input fault conditions as defined in EIA422A and EIA423A standards. These fault conditions are (1) drive in power-off condition, (2) receiver not interconnected with driver, (3) open-circuited interconnecting cable, and (4) short-circuited interconnecting cable. If one of these four fault conditions occurs at the inputs of a receiver, then the output of that receiver is driven to a known logic level. The receiver is programmed by connecting the failsafe input to Vcc or ground. A connection to Vcc provides a logic "1" output under fault conditions, while a connection to ground provides a logic "0". There are two failsafe pins (FS1 and FS2) on the UC5180C where each provides common failsafe control for four receivers.

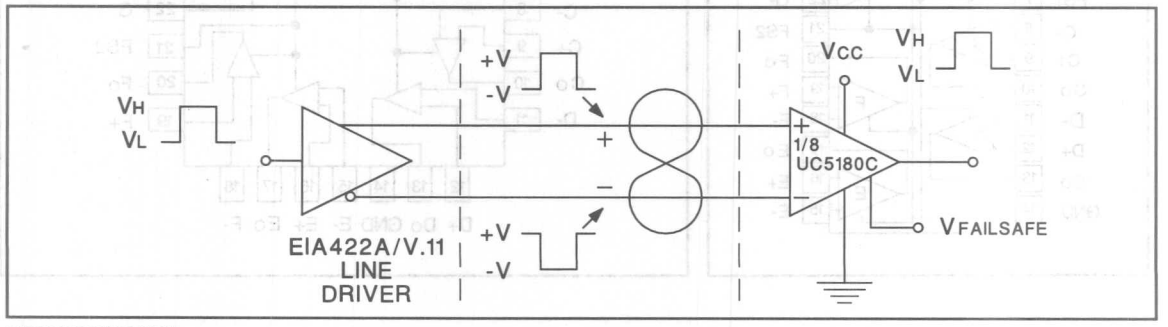
Input Filtering (UC5180C)

The UC5180C has input filtering for additional noise rejection. This filtering is a function of both signal level and frequency. For the specified input (5.5 MHz at ±500 mV) the input stage filter attenuates the signal such that the output stage threshold levels are not exceeded and no change of state occurs at the output.

EIA232E/V.28 / EIA423A/V.10 DATA TRANSMISSION



EIA422A/V.11 DATA TRANSMISSION



UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

FEATURES

- Meets EIA232E/423A/422A and CCITT V.10, V.11, V.28, X.26, X.27
- Single +5V Supply—TTL Compatible Outputs
- Differential Inputs withstand ±25V
- Low Open Circuit Voltage for Improved Failsafe Characteristic
- Reduced Supply Current—35mA Max
- Internal Hysteresis

DESCRIPTION

The UC5181C is an octal line receiver designed to meet a wide range of digital communications requirements as outlined in EIA standards EIA232E, EIA422A, EIA423A and CCITT V.10, V.11, V.28, X.26, and X.27. The UC5181C is similar to the UC5180C, but without the input filtering. Thus, it covers the entire range of data rates up to 10MBPS. A failsafe function allows these devices to "fail" to a known state under a wide variety of fault conditions at the inputs.

ABSOLUTE MAXIMUM RATINGS (Note 1)

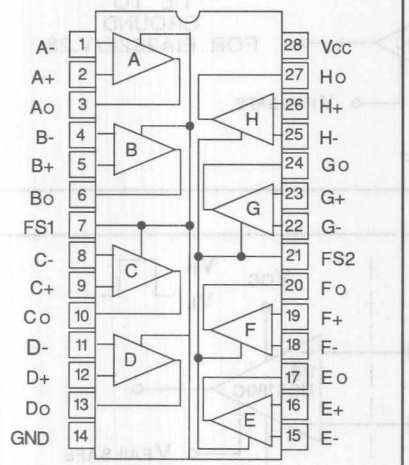
Supply Voltage, Vcc 7V
Output Sink Current 50mA
Output Short Circuit Time . . . . . 1 Sec
Common Mode Input Range 15V
Differential Input Range 25V
Failsafe Voltage . . . . . -0.3 to Vcc
PLCC Power Dissipation, TA=25° C (Note 2) . . . . . 1000 mW
DIP Power Dissipation, TA=25° C (Note 2) . . . . . 1200 mW
Storage Temperature Range . . . . . -65° C to +150° C
Lead Temperature (Soldering, 10 seconds) . . . . . -300° C

Note 1: All voltages are with respect to ground, pin 14. Currents are positive in, negative out of the specified terminal.

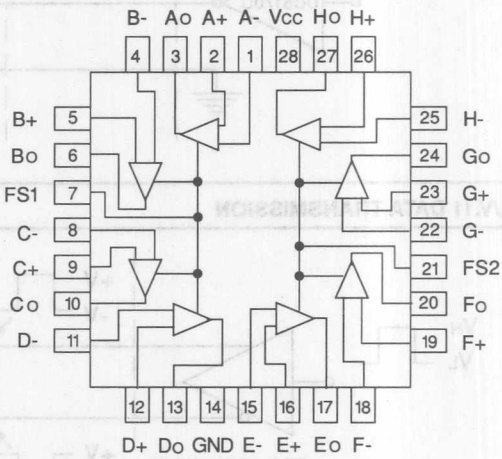
Note 2: Consult packaging section of Databook for thermal limitations and considerations of package.

CONNECTION DIAGRAMS

DIL-28 (TOP VIEW)



PLCC-28 (TOP VIEW)



DC ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, these specifications apply for T_A = 0°C to +70°C; V_{CC} = 5V ±5%, Input Common Mode Range ±7V, T_A=T_J.

PARAMETER	SYMBOL	TEST CONDITIONS		UC5181C MIN	UC5181C MAX	UNITS
DC Input Resistance	R_{IN}	3V ≤ |V_{IN}|≤25V		3	7	kΩ
Failsafe Output Voltage	V_{OFS}	Inputs Open or Shorted Together, or One Input Open and One Grounded	0≥I_{OUT}≥8mA $V_{FAILSAFE}$=0V		0.45	V
			0≥I_{OUT}≥-400µA, $V_{FAILSAFE}$=V_{CC}	2.7		
Differential Input High Threshold	V_{TL}	V_{OUT}= 0.45V, I_{OUT} = -440µA (See Figure 1)	R_S = 0 (Note3)	50	200	mV
			R_S = 500 (Note 3)		400	
Differential Input Low Threshold	V_{TL}	V_{OUT} = 0.45V, I_{OUT} = 8 mA (See Figure 1)	R_S = 0 (Note 3)	-200	-50	mV
			R_S = 500 (Note 3)	-400		
Hysteresis	V_H	F_S=0V or V_{CC} (See Figure 1)		45	140	mV
Open Circuit Input Voltage	V_{IOC}				75	mV
Input Capacitance	C_I				20	pF
High Level Output Voltage	V_{OH}	V_{ID} = 1V, I_{OUT} = -440 µA		2.7		V
Low Level Output Voltage	V_{OL}	V_{ID} = -1V (Note 4)	I_{OUT} = 4 mA		0.4	V
			I_{OUT} = 8 mA		0.45	
Short Circuit Output Current	I_{OS}	Note 5		20	100	mA
Supply current	I_{CC}	4.75V ≤V_{CC}≤5.25V			35	mA
Input Current	I_{IN}	Other Inputs Grounded	V_{IN} = +10V		3.25	mA
			V_{IH} = -10V	-3.25		

Note 3: R_S is a resistor in series with each input.
Note 4: Measure after 100 ms warm up (at 0°C).
Note 5: Only 1 output may be shorted at a time and then only for a maximum of 1 sec.
Note 6: The delays, either t_{PLH} or t_{PHL}, shall not vary from receiver to receiver by more than 35ns.

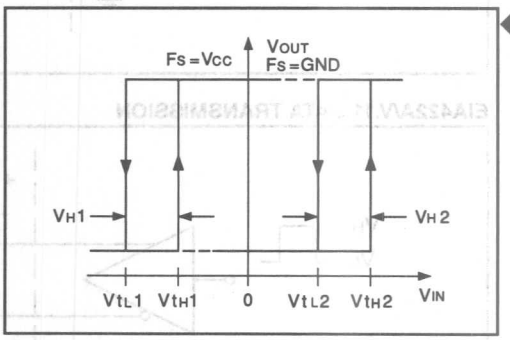


Figure 1. V_{TL}, V_{TH},V_H Definition

AC ELECTRICAL CHARACTERISTICS:

V_{CC}=5V ±5%. T_A=0°C to +70°C, Figure 2 T_A=T_J.

PARAMETER	SYMBOL	TEST CONDITIONS	UC5181C MIN	UC5181C MAX	UNITS
Propagation Delay–Low to High	t_{PLH}	C_L=50pF, V_{IN}= ±500 mV (Note 6)		120	ns
Propagation Delay–High to Low	t_{PHL}	C_L=50pF, V_{IN}= ±500 mV (Note 6)		120	ns
Acceptable Input frequency	f_A	Unused Input Grounded, V_{IN}= ±200 mV		5.0	MHz

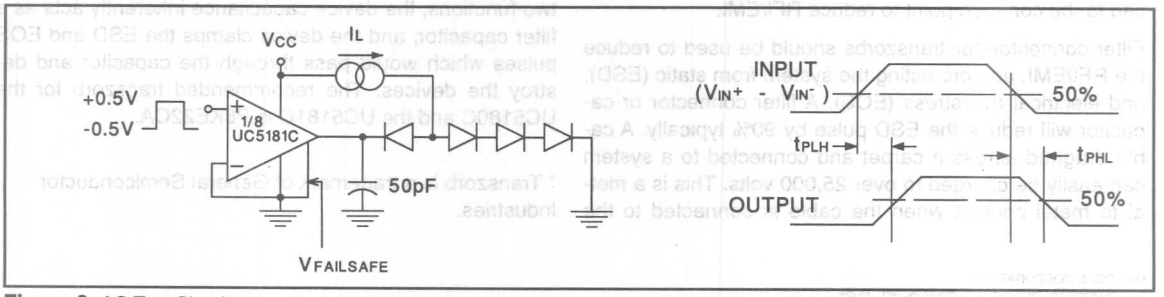


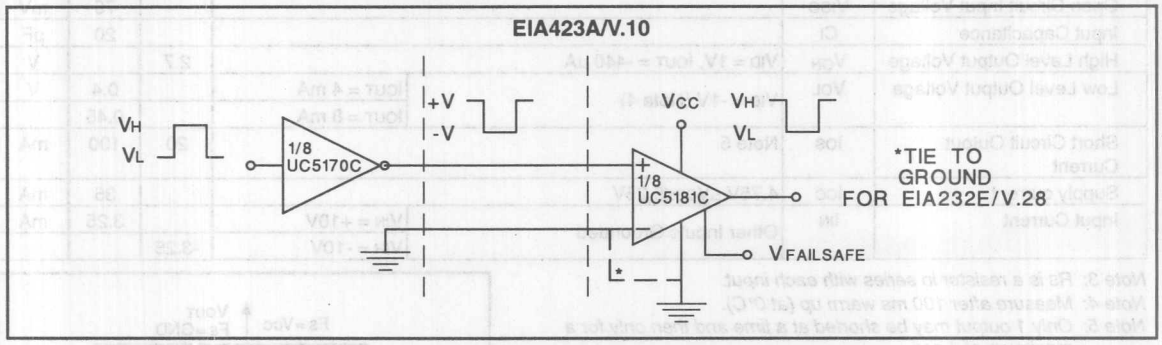
Figure 2. AC Test Circuit

APPLICATIONS INFORMATION

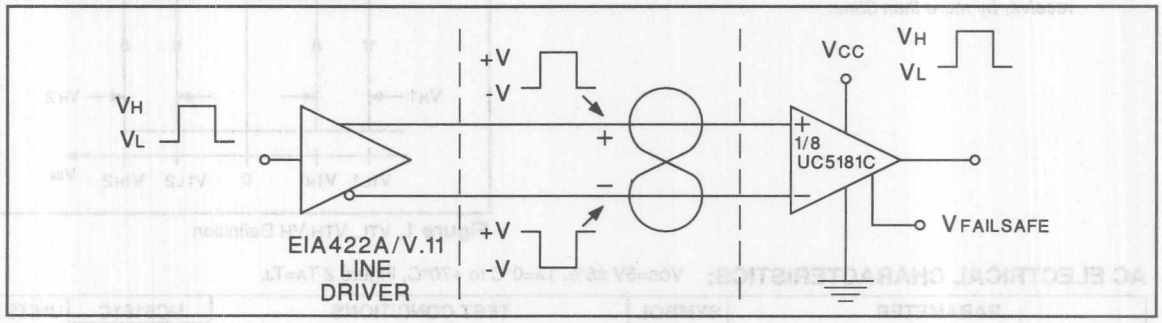
Failsafe Operation

These devices provide a failsafe operating mode to guard against input fault conditions as defined in EIA422A and EIA423A standards. These fault conditions are (1) driver in power-off condition, (2) receiver not interconnected with driver, (3) open-circuited interconnecting cable, and (4) short-circuited interconnecting cable. If one of these four fault conditions occurs at the inputs of a receiver, then the output of that receiver is driven to a known logic level. The receiver is programmed by connecting the failsafe input to Vcc or ground. A connection to Vcc provides a logic "1" output under fault conditions, while a connection to ground provides a logic "0". There are two failsafe pins (F_{S1} and F_{S2}) on the UC5181C where each provides common failsafe control for four receivers.

EIA232E/V.28 / EIA423A/V.10 DATA TRANSMISSION



EIA422A/V.11 DATA TRANSMISSION



GENERAL LAYOUT NOTES

The drivers and receivers should be mounted close to the system common ground point, with the ground reference tied to the common point to reduce RFI/EMI.

Filter connectors or transzorbs should be used to reduce the RFI/EMI, and protecting the system from static (ESD), and electrical overstress (EOS). A filter connector or capacitor will reduce the ESD pulse by 90% typically. A cable dragged across a carpet and connected to a system can easily be charged to over 25,000 volts. This is a metal to metal contact when the cable is connected to the system (no resistance), currents exceed 80 amps with less than a nanosecond rise time. A transzorb provides two functions, the device capacitance inherently acts as a filter capacitor, and the device clamps the ESD and EOS pulses which would pass through the capacitor and destroy the devices. The recommended transzorb for the UC5180C and the UC5181C is P6KE22CA.

* Transzorb is a trademark of General Semiconductor Industries.

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UNITRODE

CAN Transceiver

PRELIMINARY

FEATURES

- Pin Compatible with PCA82C250 and DeviceNet, SDS, ISO898 Compatible
- High Speed, up to 1Mbps
- Differential Transmit to the Bus and Receive from the Bus to the CAN Controller
- –25V to +18V Common Mode Protection on the Transmit Output
- 100V Transient Protection on the Transmit Output
- 24V Supply Cross Wire Protection on CANH and CANL
- No Bus Loading When Powered Down
- Operates over –40°C to +125°C
- Unitrode DeviceNet ID#107

DESCRIPTION

The UC5350 Control Area Network (CAN) Transceiver is designed for industrial applications employing the CAN serial communications physical layer per the ISO 11898 standard. The device is a high speed transceiver designed for use up to 1Mbps. Especially designed for hostile environments, this device features cross-wire and over voltage protection, thermal shutdown, a wide common mode range, and loss of ground protection.

The UC5350 CAN Transceiver interfaces the single ended CAN Controller with the differential CAN Bus found in industrial and automotive applications. It operates over the –7V to +12V common mode range of the bus and will withstand common mode transients of –25V to +18V as well as Schaffner tests.

The VREF output provides half the VCC voltage for the controller reference.

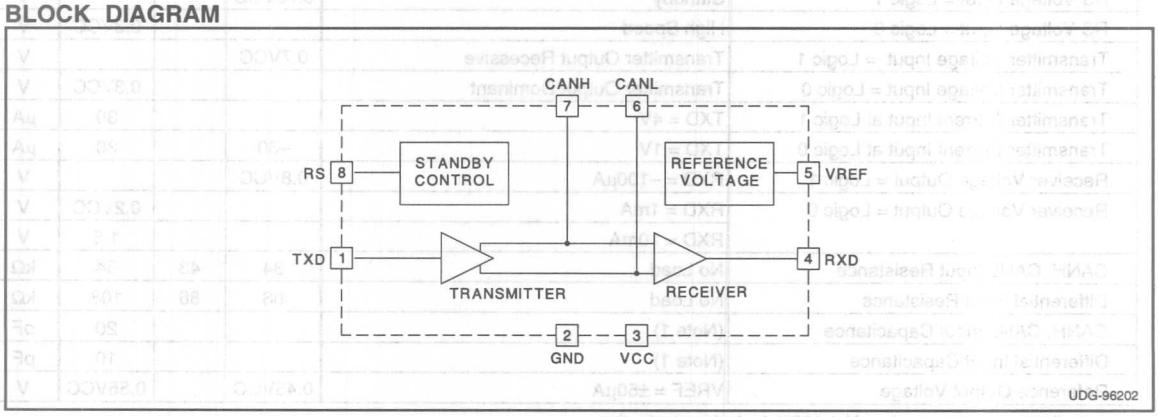
Performance features that improve bus bandwidth and length, while reducing reflection and distortion include high input impedance, a symmetrical differential signal driver, and low propagation delay. Reduced reflection and distortion results in increases of effective bus length and bandwidth.

The transceiver operates over a wide temperature range, –40°C to +125°C and is available in 8-pin SOIC and Dual-in-Line packages.

FUNCTIONAL TABLE (VCC = 4.5V to 5.5V)

Inputs		System Mode	Output Mode	Outputs	
TXD	RS			$V_{CANH} - V_{CANL}$	RXD
0	0	High Speed	Dominant	1.5V to 3V	0
1	0	High Speed	Recessive	–120mV to +12mV	1
High Z	0	High Speed	Recessive	–120mV to +12mV	1
X	1	Standby		High Z	0 at Bus = Dominant 1 at Bus = Recessive

BLOCK DIAGRAM



1/97

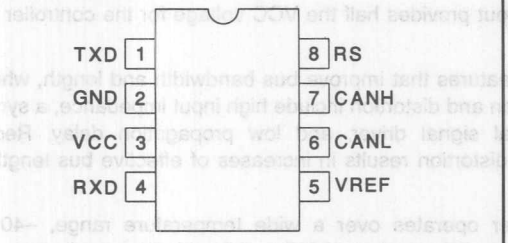
ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... –0.3V to 9V
TXD, RXD, VREF, RS ..... –0.3V to VCC + 0.3V
CANL, CANH
0V < VCC < 5.5V ..... –8V to +36V
Non-Destructive, Non-Operative ..... –8V to +32V
Transient, Schaffner Test (Fig. 1) ..... –150 to +100V
Operating Temperature ..... –40°C to +125°C
Storage Temperature ..... –65°C to +150°C
Junction Temperature ..... –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

Currents are positive into, negative out of the specified terminal. Consult Packaging Section of the Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

DIL-8, SOIC-8 (Top View)
N, D Package



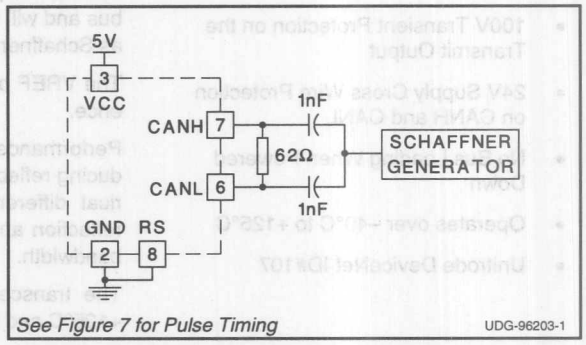


Figure 1. Schaffner Test

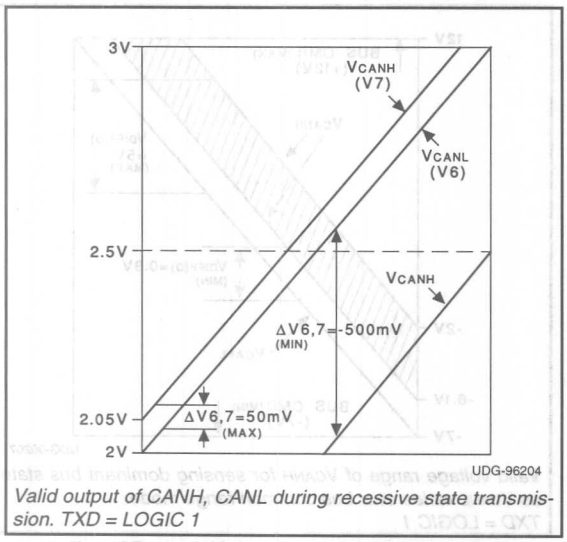
ELECTRICAL CHARACTERISTICS (Total Device): Unless otherwise stated, the device is disconnected from the bus line; VCC = 4.5V to 5.5V; 60Ω in parallel with 100pF load between CANH and CANL; T_A = –40°C to +125°C, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage		4.5		5.5	V
Supply Current	Dominant, TXD = 1V			70	mA
	Recessive, TXD = 4V		9	12	mA
	Standby, RS = 4V		1	1.5	mA
RS Input Current		–5		5	µA
RS Voltage Input = Logic 1	Standby	0.75VCC			V
RS Voltage Input = Logic 0	High Speed			0.3VCC	V
Transmitter Voltage Input = Logic 1	Transmitter Output Recessive	0.7VCC			V
Transmitter Voltage Input = Logic 0	Transmitter Output Dominant			0.3VCC	V
Transmitter Current Input at Logic 1	TXD = 4V			30	µA
Transmitter Current Input at Logic 0	TXD = 1V	–30		30	µA
Receiver Voltage Output = Logic 1	RXD = –100µA	0.8VCC			V
Receiver Voltage Output = Logic 0	RXD = 1mA			0.2VCC	V
	RXD = 10mA			1.5	V
CANH, CANL Input Resistance	No Load	34	43	54	kΩ
Differential Input Resistance	No Load	68	86	108	kΩ
CANH, CANL Input Capacitance	(Note 1)			20	pF
Differential Input Capacitance	(Note 1)			10	pF
Reference Output Voltage	VREF = ±50µA	0.45VCC		0.55VCC	V

Note 1: Guaranteed by design. Not 100% tested in production.

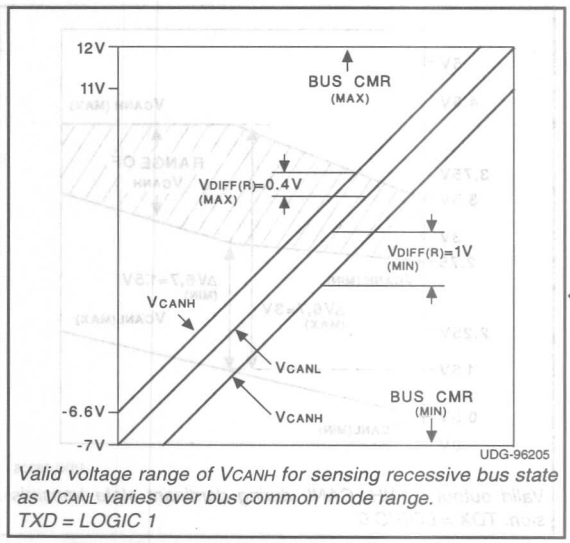
ELECTRICAL CHARACTERISTICS (DC Parameters For Recessive State): Unless otherwise stated, the device is disconnected from the bus line; 60Ω in parallel with 100pF load between CANH and CANL.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{CANH}, V_{CANL}	No Load, TXD = 4V (Figure 2)	2	2.5	3	V
Differential Output Transmitter (V_{CANH} – V_{CANL})	No Load, TXD = 4V (Figure 2)	–500	0	50	mV
Differential Input Receiver	Common Mode Range = –7V to +12V, TXD = 4V, CANH, CANL Externally Driven (Figure 3)	–1		0.40	V
Differential Input Resistance	No Load	68		108	kΩ



Valid output of CANH, CANL during recessive state transmission. TXD = LOGIC 1

Figure 2. Recessive State Voltage Diagram

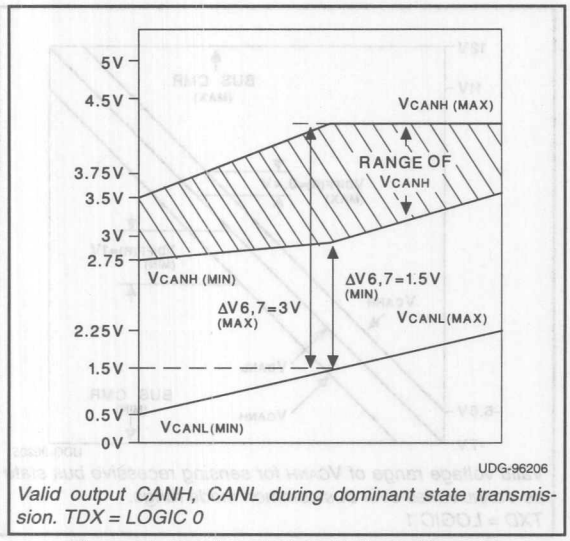


Valid voltage range of V_{CANH} for sensing recessive bus state as V_{CANL} varies over bus common mode range. TXD = LOGIC 1

Figure 3. Recessive State Voltage Diagram

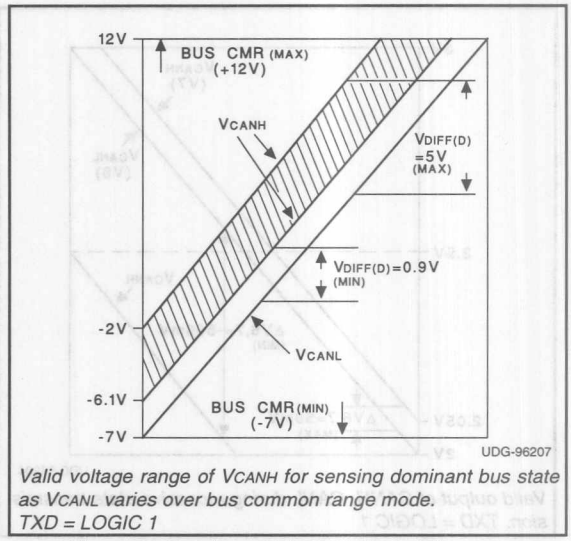
ELECTRICAL CHARACTERISTICS (DC Parameters For Dominant State): Unless otherwise stated, the device is disconnected from the bus line; 60Ω in parallel with 100pF load between CANH and CANL.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
CANH Output Voltage (V_{CANH})	TXD = 1V (Figure 4)	2.75	3.5	4.5	V
CANL Output Voltage (V_{CANL})	TXD = 1V (Figure 4)	0.50	1.5	2.25	V
Differential Output Transmitter (V_{CANH} - V_{CANL})	TXD = 1V (Figure 4)	1.5	2	3	V
Differential Input Receiver ($V_{DIFF(D)}$)	Common Mode Range = –7 to +12V, TXD = 4V, CANH, CANL Externally Driven (Figure 5)	0.9		5	V



Valid output CANH, CANL during dominant state transmission. TDX = LOGIC 0

Figure 4. Dominant State Voltage Diagram



Valid voltage range of V_{CANH} for sensing dominant bus state as V_{CANL} varies over bus common range mode. TXD = LOGIC 1

Figure 5. Dominant State Voltage Diagram

TRANSMITTER CHARACTERISTICS: Unless otherwise stated, the device is disconnected from the bus line; 60Ω in parallel with 100pF load between CANH and CANL.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Differential Output Transmitter (V_{CANH} - V_{CANL})	Dominant Mode	1.5	2	3	V
	Recessive Mode	–500		50	mV
Delay From TXD to Bus Active T_{ON} (TXD)	(Figure 6)			50	ns
Delay From TXD to Bus Inactive T_{OFF} (TXD)	60Ω Across CANH and CANL (Figure 6)			50	ns

RECEIVER CHARACTERISTICS: Unless otherwise stated, the device is disconnected from the bus line; 60Ω in parallel with 100pF load between CANH and CANL.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Differential Input Receiver (V_{CANH} - V_{CANL})	Dominant Mode, TXD = 4V	0.9			V
	Recessive Mode, TXD = 4V			0.4	V
Differential Input Hysteresis	TXD = 4V		150		mV
Delay From Bus to RXD (T_{ON})	Inactive to Active Bus (Figure 6)			50	ns
Delay From Bus to RXD (T_{OFF})	Active to Inactive Bus, 60Ω Across CANH and CANL (Figure 6)			50	ns

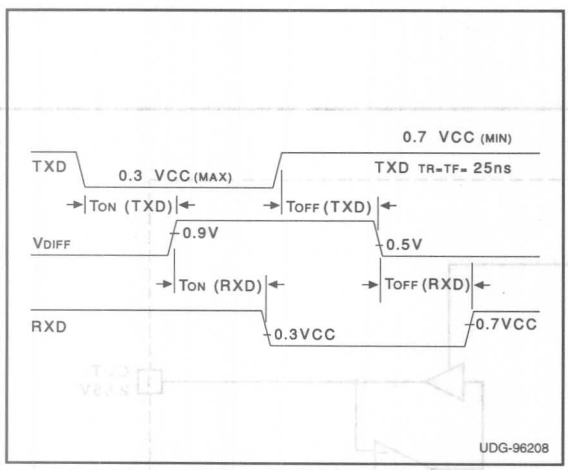


Figure 6. Transceiver AC Response

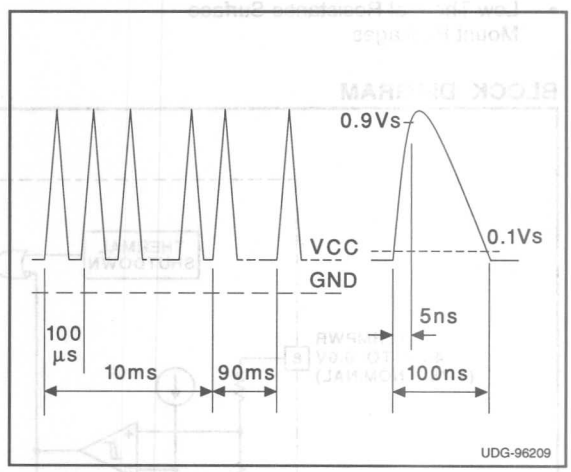


Figure 7. Timing Diagram for Schaffner Tests

Magnitude Specifications for Vs

ISO	DIN 40839-1	Schaffner
DP7637/1	(Draft)	NSG500C/506C
up to 150V	up to 150V	40V to 200V

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27-Line SCSI Source/Sink Regulator

FEATURES

- Complies with SCSI, SCSI-2, SCSI-3 SPI and Ultra SCSI (Fast-20)
- 2.85V Regulated Output Voltage With 1.4% Tolerance
- Provides Current for up to 27 Lines of Active Termination for SCSI Buses
- –750mA Sourcing Current for Termination
- +300mA Sinking Current for Active Negation Drivers
- 0.9V Dropout Voltage Regulator at 750mA and 2.75V Output
- 100µA Supply Current in Disconnect Mode
- Current Limit and Thermal Shutdown Protection
- Low Thermal Resistance Surface Mount Packages

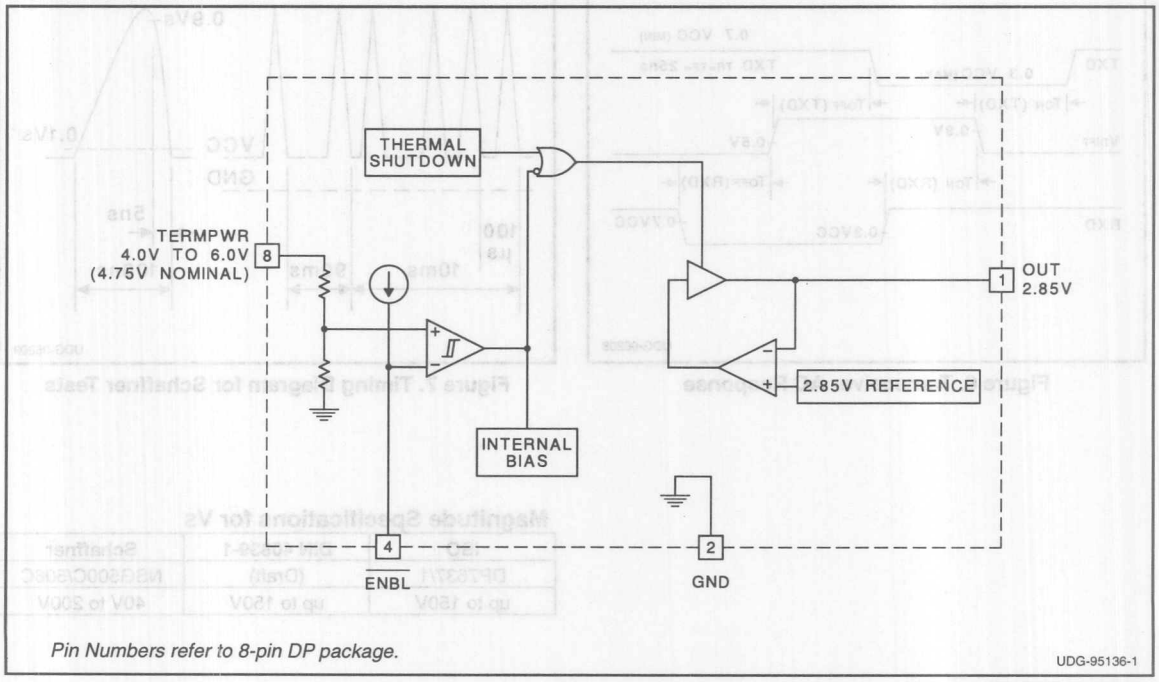
DESCRIPTION

The UC560 provides current for up to 27 lines of active termination for a SCSI (Small Computers Systems Interface) parallel bus. The SCSI standard requires active termination at both ends of the cable. The UC560 is based on the UC5603 and UC5613 SCSI Active Terminators. It uses the voltage regulator and internal logic circuits of those parts, but has no termination circuits. The UC560 provides greater source current drive capability compared to the UC5603 and UC5613.

The UC560 sink current maintains regulation with all active-negation drivers negated. It provides a disconnect feature which disables the regulator to greatly reduce standby power. Internal circuit trimming is utilized for a 1.4% tolerance output voltage. Other features include thermal shutdown and current limit for short circuit conditions.

The UC560 is available in low thermal resistance versions of the industry standard 8-pin power SOIC, 5-pin TO-220 and 5-pin TO-263.

BLOCK DIAGRAM



Pin Numbers refer to 8-pin DP package.

UDG-95136-1

ABSOLUTE MAXIMUM RATINGS

TERMPWR Voltage 7V
ENBL Voltage ..... –0.3V to TERMPWR + 0.3V
Regulator Output Current 1.4A
Power Dissipation 2.5W
Storage Temperature ..... –65°C to +150°C
Junction Temperature ..... –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

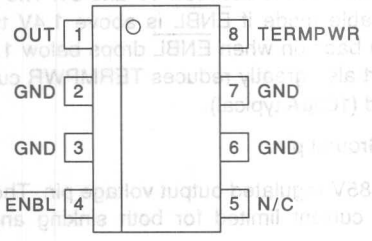
Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

RECOMMENDED OPERATING CONDITIONS

TERMPWR Voltage ..... 4.0V to 6.0V
ENBL Voltage ..... 0V to TERMPWR

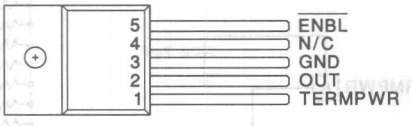
CONNECTION DIAGRAMS

SOIC-8 (Top View)
DP Package



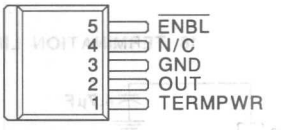
Note: Pins 2,3,6, and 7 are heat sinking pins. Pin 2 is the connect point for electrical ground.

5-Pin TO-220 (Top View)
T Package



Note: TAB is ground.

5-Pin TO-263 (Top View)
TD Package



Note: TAB is ground.

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, T_A = 0°C to 70°C, TERMPWR = 4.75V, $\overline{ENBL}$ = 0V, C_{OUT} = 4.7µF, $C_{TERMPWR}$ = 4.7µF, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current Section					
TERMPWR Supply Current	No Load		16	22	mA
	I_{OUT} = –700mA		710	750	mA
Power Down Mode	$\overline{ENBL}$ = 2.0V		100	140	µA
Regulator Section					
Regulator Output Voltage	25°C, No Load	2.81	2.85	2.89	V
Load Regulation	I_{OUT} = 300mA to –750mA (Note 2)		25	30	mV
Line Regulation	TERMPWR = 4.0V to 6.0V, No Load (Note 2)		10	20	mV
Dropout Voltage	I_{OUT} = –750mA, V_{OUT} = 2.75V		0.9	1.2	V
Short Circuit Current	V_{OUT} = 0.0V	–0.85	–1.3		A
Sinking Current	V_{OUT} = 3.5V		500	600	mA
	$\overline{ENBL}$ = 2.0V, V_{OUT} = 3.0V		1	2	mA
Thermal Shutdown	(Note 1)		170		°C
Thermal Shutdown Hysteresis	(Note 1)		10		°C
Shutdown Section					
$\overline{ENBL}$ Threshold		1.1	1.4	1.7	V
Threshold Hysteresis			100		mV
$\overline{ENBL}$ Output Current			–10	–15	µA

Note 1: Guaranteed by design. Not 100% tested in production.
Note 2: Tested at a constant junction temperature by low duty cycle pulse testing.

PIN DESCRIPTIONS

ENBL: Enable Bar pin. The $\overline{\text{ENBL}}$ function is active low, and the pin will source 10µA typically when at ground and TERMPWR is between 4V and 6V. The part will go into disable mode if $\overline{\text{ENBL}}$ is above 1.4V typical, and will turn back on when $\overline{\text{ENBL}}$ drops below 1.3V typical. The part also greatly reduces TERMPWR current when disabled (100µA typical).

GND: Ground pin.

OUT: 2.85V regulated output voltage pin. The part is internally current limited for both sinking and sourcing current to prevent damage. When the part is in disabled mode ($\overline{\text{ENBL}} \geq$ 1.4V typical), the output goes to 0V with no external supply source on OUT. The part will sink current, though, if there is an external supply voltage applied to OUT when in disabled mode. For best perfomance, a 4.7µF low ESR capacitor is recommended.

TERMPWR: Supply voltage pin. The pin should be decoupled with at least a 2.2µF low ESR output capacitor. For best perfomance, a 4.7µF low ESR capacitor is recommended. Lead lengths should be kept at a minimum.

APPLICATIONS INFORMATION

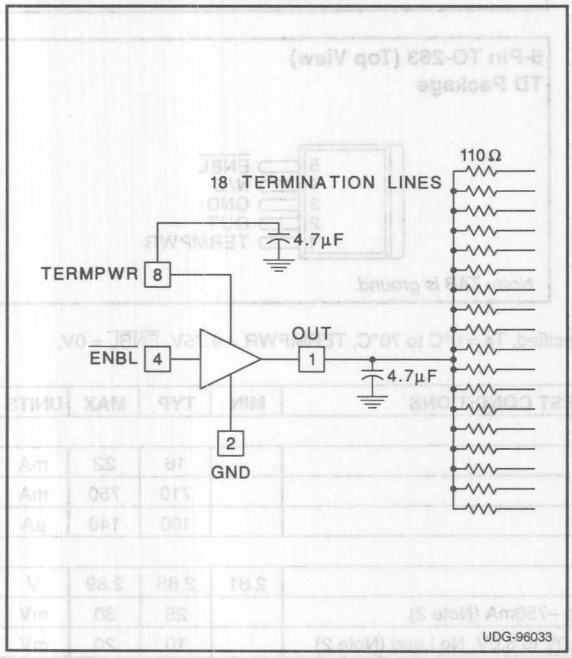


Figure 1. Typical SCSI Bus Configuration Utilizing UC560 Device

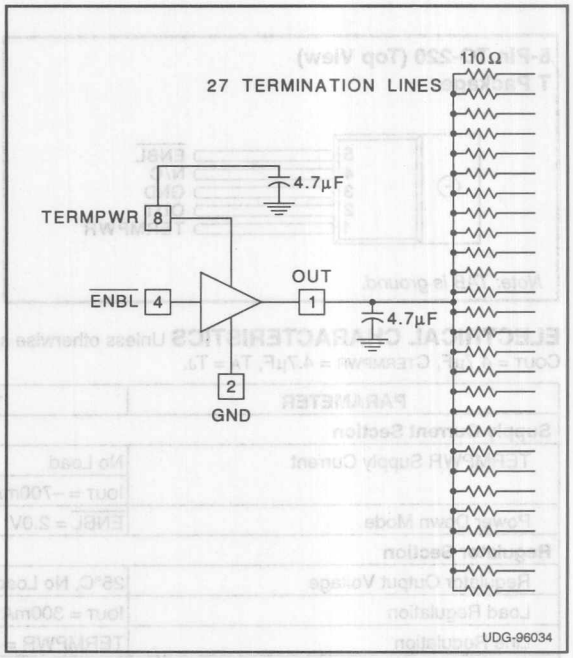
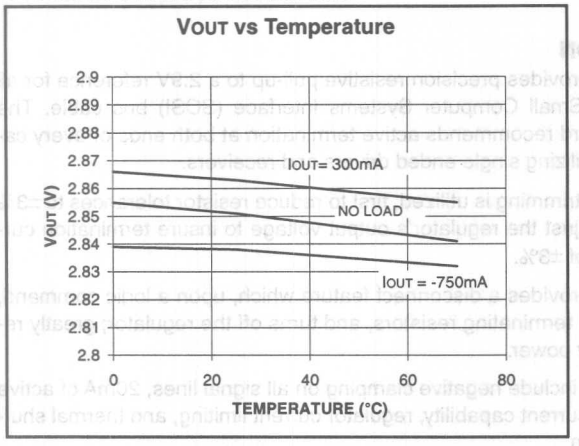
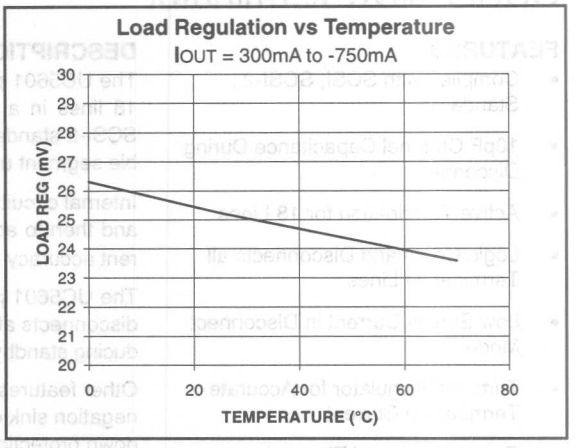
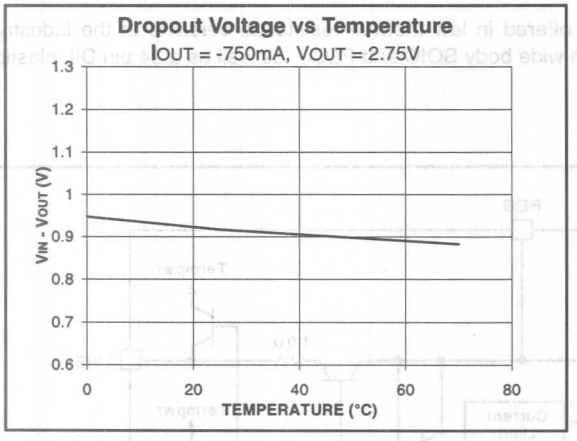


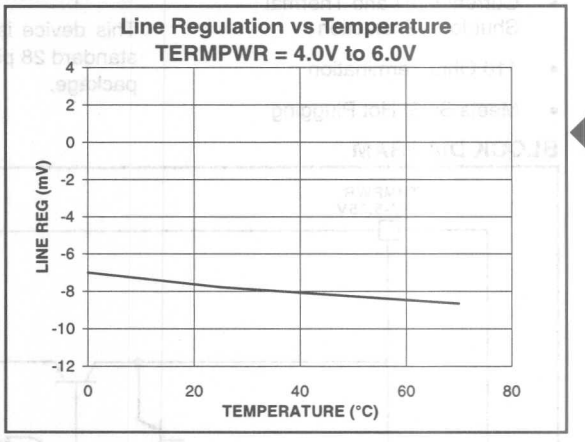
Figure 2. Typical Wide SCSI Bus Configuration Utilizing UC560 Device

TYPICAL CHARACTERISTICS









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UNITRODE

SCSI Active Terminator

FEATURES

- Complies with SCSI, SCSI-2 Standards
- 10pF Channel Capacitance During Disconnect
- Active Termination for 18 Lines
- Logic Command Disconnects all Termination Lines
- Low Supply Current in Disconnect Mode
- Trimmed Regulator for Accurate Termination Current
- Current Limit and Thermal Shutdown Protection
- 110 Ohm Termination
- Meets SCSI Hot Plugging

DESCRIPTION

The UC5601 provides precision resistive pull-up to a 2.9V reference for all 18 lines in a Small Computer Systems Interface (SCSI) bus cable. The SCSI-2 standard recommends active termination at both ends of every cable segment utilizing single ended drivers and receivers.

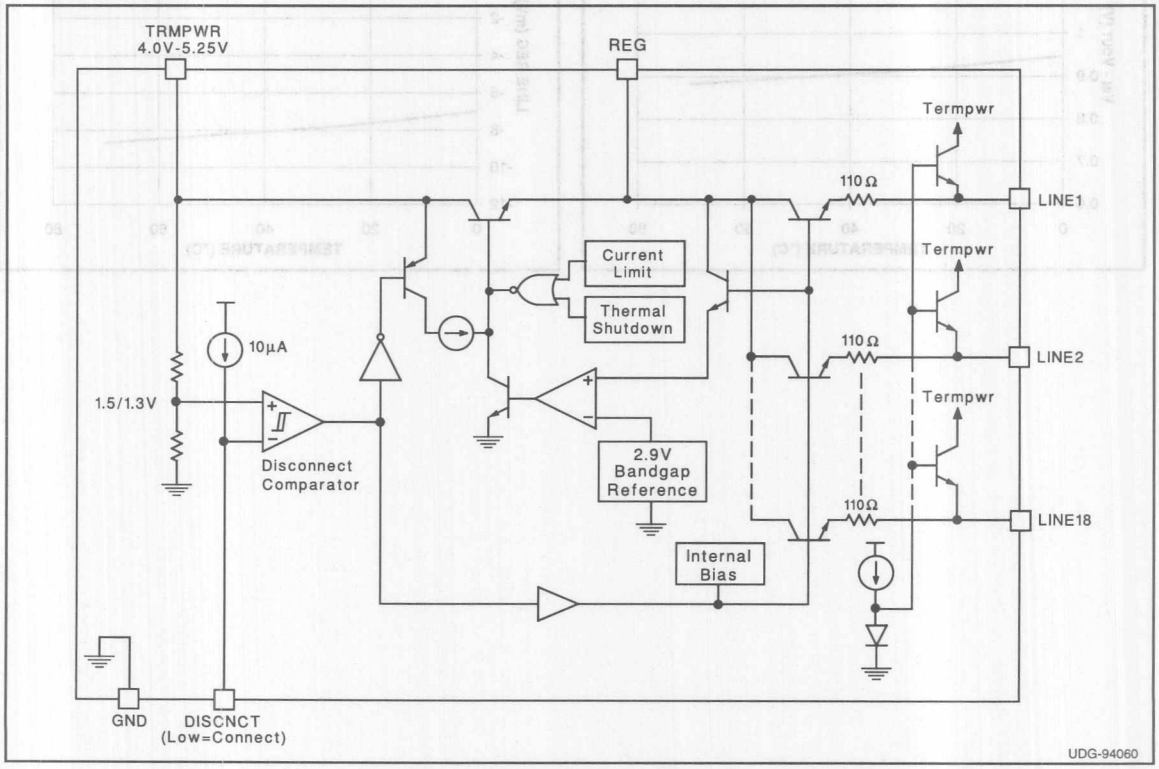
Internal circuit trimming is utilized, first to reduce resistor tolerances to ±3% and then to adjust the regulator's output voltage to insure termination current accuracy of ±3%.

The UC5601 provides a disconnect feature which, upon a logic command, disconnects all terminating resistors, and turns off the regulator; greatly reducing standby power.

Other features include negative clamping on all signal lines, 20mA of active negation sink current capability, regulator current limiting, and thermal shutdown protection.

This device is offered in low thermal resistance versions of the industry standard 28 pin wide body SOIC and PLCC, as well as a 24 pin DIL plastic package.

BLOCK DIAGRAM



Circuit Design Patented

10/94

ABSOLUTE MAXIMUM RATINGS

Termpwr Voltage ..... +7V
Signal Line Voltage ..... 0V to +7V
Regulator Output Current 1A
Storage Temperature ..... –65°C to +150°C
Operating Temperature ..... –55°C to +150°C
Lead Temperature (Soldering, 10 Sec.) ..... +300°C

Unless otherwise specified all voltages are with respect to Ground. Currents are positive into, negative out of the specified terminal.

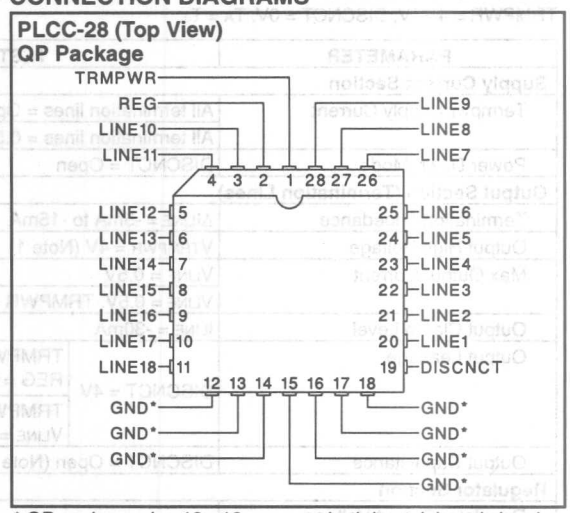
Consult Packaging Section of Unitrode Integrated Circuits databook for thermal limitations and considerations of packages.

RECOMMENDED OPERATING CONDITIONS

Termpwr Voltage ..... 4.0V to 5.25V
Signal Line Voltage ..... 0V to +3V
Disconnect Input Voltage ..... 0V to Termpwr

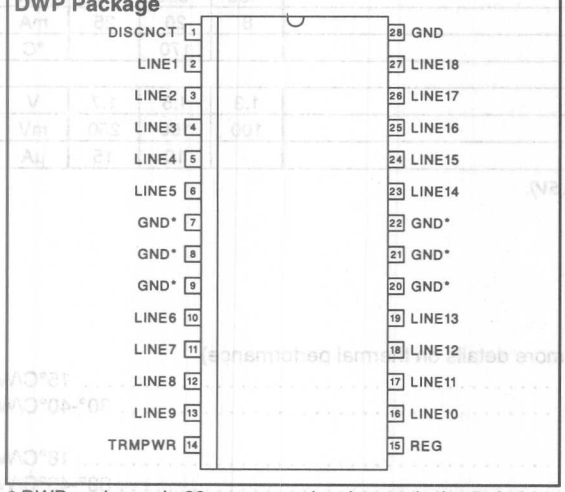
CONNECTION DIAGRAMS

PLCC-28 (Top View)
QP Package



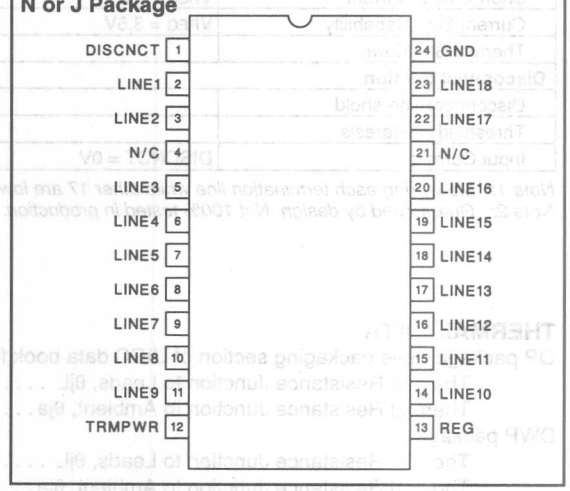
** QP package pins 12 - 18 serve as both heatsink and signal ground.*

SOIC-28 (Top View)
DWP Package



** DWP package pin 28 serves as signal ground; pins 7, 8, 9, 20, 21, 22 serve as heatsink/ground.*

DIL-24 (Top View)
N or J Package



Note: Drawings are not to scale.

ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C. TRMPWR = 4.75V, DISCNCT = 0V. T_A = T_J.

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNITS
Supply Current Section							
Termpwr Supply Current	All termination lines = Open				17	25	mA
	All termination lines = 0.5V				400	430	mA
Power Down Mode	DISCNCT = Open				100	150	µA
Output Section (Termination Lines)							
Termination Impedance	ΔI_{LINE} = -5mA to -15mA			107	110	113	Ω
Output High Voltage	V_{TRMPWR} = 4V (Note 1)			2.65	2.9		V
Max Output Current	V_{LINE} = 0.5V			-21.1	-21.7	-22.4	mA
	V_{LINE} = 0.5V, TRMPWR = 4V (Note 1)			-19.8	-21.7	-22.4	mA
Output Clamp Level	I_{LINE} = -30mA			-0.2	-0.05	0.1	V
Output Leakage	DISCNCT = 4V	TRMPWR = 0V to 5.25V REG = 0V	V_{LINE} = 0 to 4V		10	400	nA
			V_{LINE} = 5.25V			100	µA
		TRMPWR = 0V to 5.25V, REG = Open V_{LINE} = 0V to 5.25V			10	400	nA
Output Capacitance	DISCNCT = Open (Note 2)				10	12	pF
Regulator Section							
Regulator Output Voltage				2.8	2.9	3.0	V
Line Regulation	TRMPWR = 4V to 6V				10	20	mV
Load Regulation	I_{REG} = 0 to -400mA				20	50	mV
Drop Out Voltage	All Termination Lines = 0.5V				1.0	1.2	V
Short Circuit Current	V_{REG} = 0V			-450	-650	-850	mA
Current Sink Capability	V_{REG} = 3.5V			8	20	25	mA
Thermal Shutdown					170		°C
Disconnect Section							
Disconnect Threshold				1.3	1.5	1.7	V
Threshold Hysteresis				100	160	250	mV
Input Current	DISCNCT = 0V				10	15	µA

Note 1: Measuring each termination line while other 17 are low (0.5V).
Note 2: Guaranteed by design. Not 100% tested in production.

THERMAL DATA

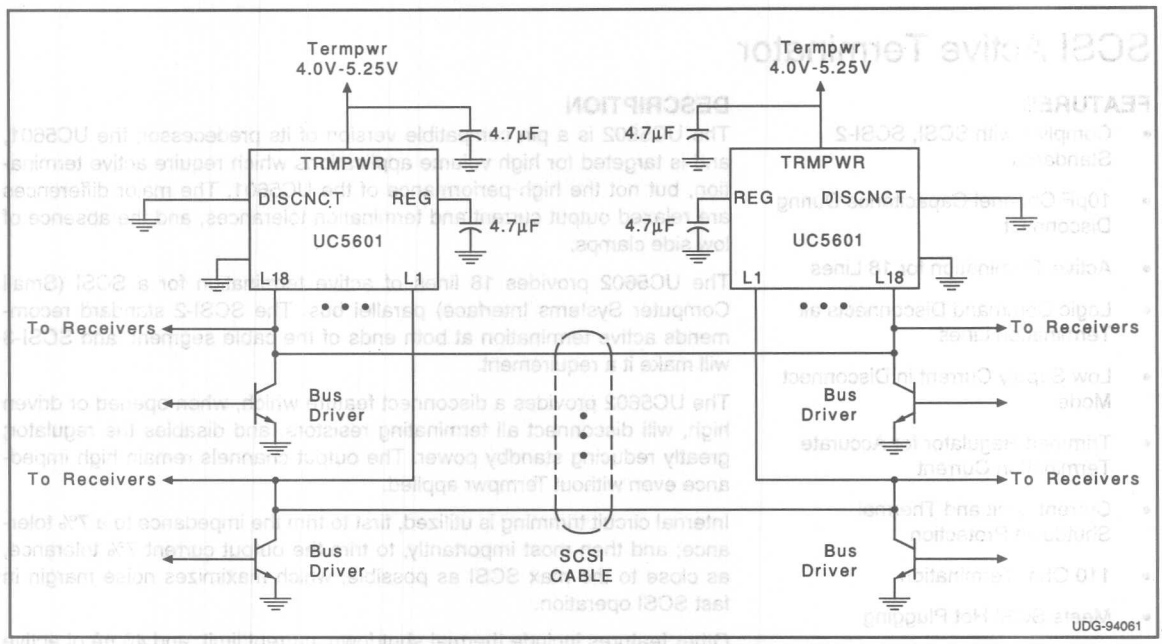
QP package: (see packaging section of UICC data book for more details on thermal performance)
- Thermal Resistance Junction to Leads, θjL . . . . . 15°C/W
- Thermal Resistance Junction to Ambient, θja . . . . . 30°-40°C/W

DWP package:
- Thermal Resistance Junction to Leads, θjL . . . . . 18°C/W
- Thermal Resistance Junction to Ambient, θja . . . . . 33°-43°C/W

J package:
- Thermal Resistance Junction to Leads, θjL . . . . . 40°C/W
- Thermal Resistance Junction to Ambient, θja . . . . . 75°-85°C/W

N package:
- Thermal Resistance Junction to Leads, θjL . . . . . 50°C/W
- Thermal Resistance Junction to Ambient, θja . . . . . 95°-105°C/W

Note: The above numbers for θjL are maximums for the limiting thermal resistance of the package in a standard mounting configuration. The θja numbers are meant to be guidelines for the thermal performance of the device/pc-board system. All of the above numbers assume no ambient airflow.



Typical SCSI Bus Configuration Using the UC5601

A Look at the Response of a SCSI-2 Cable

Figure 1 shows a single line of a SCSI cable. The driver is an open colletor type which when asserted pulls low, and when negated the termination resistance serves as the pull-up.

Figure 2 shows a worst case scenario of mid cable de-assertion with a close proximity receiver. The voltage V_{STEP} is defined as:

$$V_{STEP} = V_{OL} + I_O Z_0$$

V_{OL} = Driver Output Low Voltage
I_O = Current from Receiving Terminator
Z_0 = Cable Characteristic Impedance

$$I_O = \frac{V_{REG} - V_{OL}}{110}$$

In the pursuit of higher data rates, sampling culd occur during this step portion, therefore it is important to ensure that the step is as high as possible to get the most noise margin. For this reason the UC5601 is trimmed so that the output current (I_O) is as close as possible to the SCSI max current spec of 22.4mA. The Termination impedance is initially trimmed on the IC to 110 ohms typical, then the regulator voltage is trimmed for the highest output current to within 22.4mA.

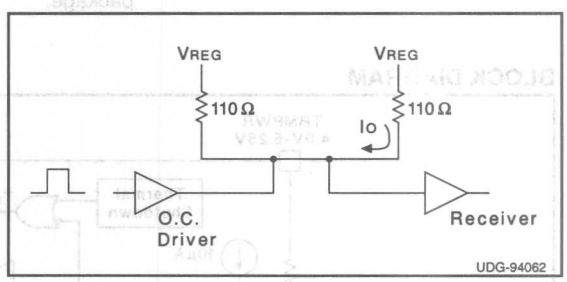


Figure 1. A Single Line of a SCSI Cable

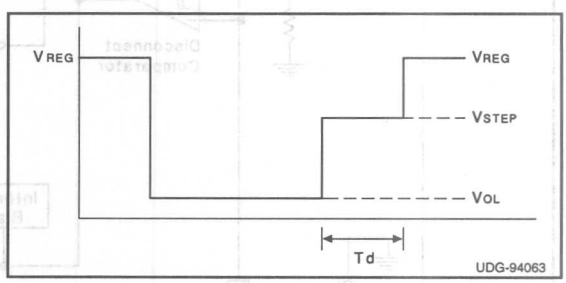


Figure 2. A Typical Response of a SCSI Cable

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UNITRODE

SCSI Active Terminator

FEATURES

- Complies with SCSI, SCSI-2 Standards
- 10pF Channel Capacitance During Disconnect
- Active Termination for 18 Lines
- Logic Command Disconnects all Termination Lines
- Low Supply Current in Disconnect Mode
- Trimmed Regulator for Accurate Termination Current
- Current Limit and Thermal Shutdown Protection
- 110 Ohm Termination
- Meets SCSI Hot Plugging

DESCRIPTION

The UC5602 is a pin compatible version of its predecessor, the UC5601, and is targeted for high volume applications which require active termination, but not the high performance of the UC5601. The major differences are relaxed output current and termination tolerances, and the absence of low side clamps.

The UC5602 provides 18 lines of active termination for a SCSI (Small Computer Systems Interface) parallel bus. The SCSI-2 standard recommends active termination at both ends of the cable segment, and SCSI-3 will make it a requirement.

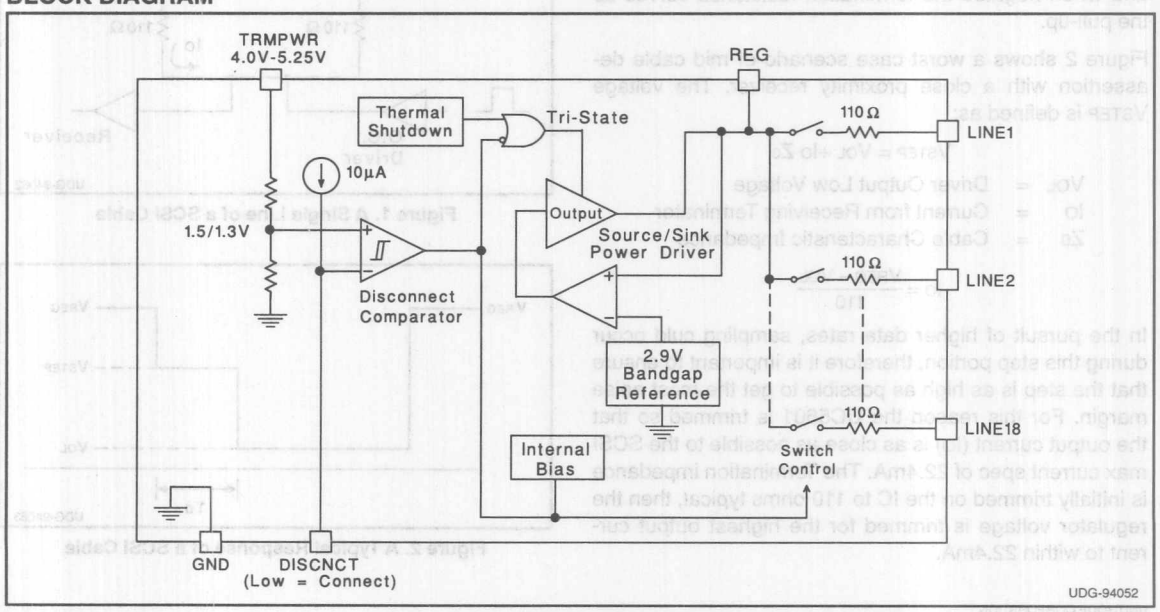
The UC5602 provides a disconnect feature which, when opened or driven high, will disconnect all terminating resistors, and disables the regulator; greatly reducing standby power. The output channels remain high impedance even without Termpwr applied.

Internal circuit trimming is utilized, first to trim the impedance to a 7% tolerance; and then most importantly, to trim the output current 7% tolerance, as close to the max SCSI as possible, which maximizes noise margin in fast SCSI operation.

Other features include thermal shutdown, current limit, and 40mA of active negation sink current capability.

This device is offered in low thermal resistance versions of the industry standard 28 pin wide body SOIC and PLCC, as well as a 24 pin DIL plastic package.

BLOCK DIAGRAM



Circuit Design Patented

ABSOLUTE MAXIMUM RATINGS

Termpwr Voltage . . . . . +7V
Signal Line Voltage. . . . . 0V to +7V
Regulator Output Current 0.5A
Storage Temperature . . . . . –65°C to +150°C
Operating Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 Sec.) . . . . . +300°C

Unless otherwise specified all voltages are with respect to Ground. Currents are positive into, negative out of the specified terminal.

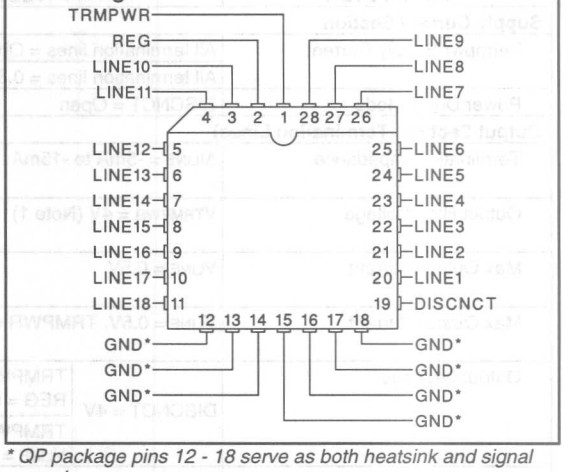
Consult Packaging Section of Unitrode Integrated Circuits databook for thermal limitations and considerations of packages.

RECOMMENDED OPERATING CONDITIONS

Termpwr Voltage . . . . . 4.0V to 5.25V
Signal Line Voltage. . . . . 0V to +3V
Disconnect Input Voltage . . . . . 0V to Termpwr

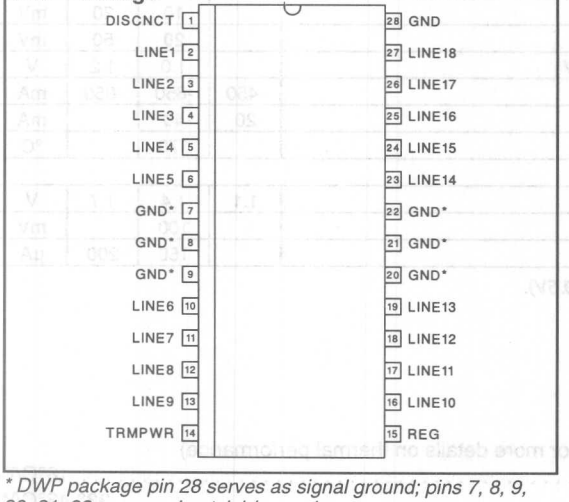
CONNECTION DIAGRAMS

PLCC-28 (Top View)
QP Package



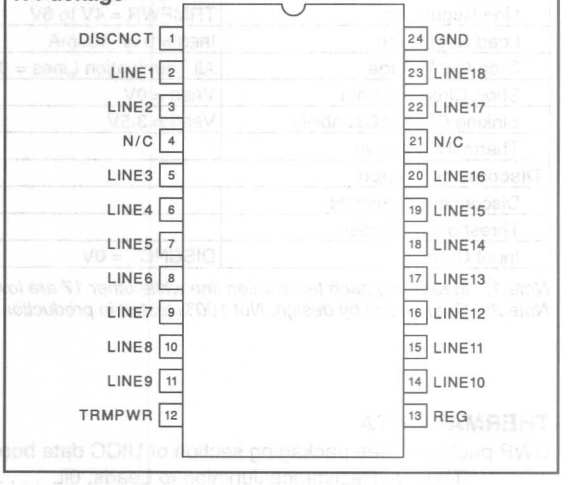
** QP package pins 12 - 18 serve as both heatsink and signal ground.*

SOIC-28 (Top View)
DWP Package



** DWP package pin 28 serves as signal ground; pins 7, 8, 9, 20, 21, 22 serve as heatsink/ground.*

DIL-24 (Top View)
N Package



Note: Drawings are not to scale.

ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C. TRMPWR = 4.75V, DISCNCT = 0V. T_A = T_J.

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNITS
Supply Current Section							
Termpwr Supply Current	All termination lines = Open				20	29	mA
	All termination lines = 0.5V				400	435	mA
Power Down Mode	DISCNCT = Open				100	150	µA
Output Section (Termination Lines)							
Termination Impedance	ΔI_{LINE} = -5mA to -15mA		T_J = 25°C	102	110	118	Ω
			0°C < T_J < 70°C	97		129	Ω
Output High Voltage	V_{TRMPWR} = 4V (Note 1)		T_J = 25°C	2.6	2.9	3.1	V
			0°C < T_J < 70°C	2.55		3.2	V
Max Output Current	V_{LINE} = 0.5V		T_J = 25°C	-19.5	-21.4	-22.4	mA
			0°C < T_J < 70°C	-18.5		-22.4	mA
Max Output Current	V_{LINE} = 0.5V, TRMPWR = 4V (Note 1)		T_J = 25°C	-18.0	-21.5	-22.4	mA
			0°C < T_J < 70°C	-17.0		-22.4	mA
Output Leakage	DISCNCT = 4V	TRMPWR = 0V to 5.25V REG = 0V	V_{LINE} = 0 to 4V		10	400	nA
			V_{LINE} = 5.25V			100	µA
		TRMPWR = 0V to 5.25V, REG = Open V_{LINE} = 0V to 5.25V			10	400	nA
Output Capacitance	DISCNCT = Open (Note 2)				10	13	pF
Regulator Section							
Regulator Output Voltage			T_J = 25°C	2.7	2.9	3.1	V
			0°C < T_J < 70°C	2.55		3.2	V
Line Regulation	TRMPWR = 4V to 6V				10	20	mV
Load Regulation	I_{REG} = 0 to -400mA				20	50	mV
Drop Out Voltage	All Termination Lines = 0.5V				1.0	1.2	V
Short Circuit Current	V_{REG} = 0V			-450	-650	-850	mA
Sinking Current Capability	V_{REG} = 3.5V			20	40		mA
Thermal Shutdown					170		°C
Disconnect Section							
Disconnect Threshold				1.1	1.4	1.7	V
Threshold Hysteresis					100		mV
Input Current	DISCNCT = 0V				150	200	µA

Note 1: Measuring each termination line while other 17 are low (0.5V).
Note 2: Guaranteed by design. Not 100% tested in production.

THERMAL DATA

DWP package: (see packaging section of UICC data book for more details on thermal performance)

Thermal Resistance Junction to Leads, θjL ..... 18°C/W
Thermal Resistance Junction to Ambient, θja ..... 33°-43°C/W

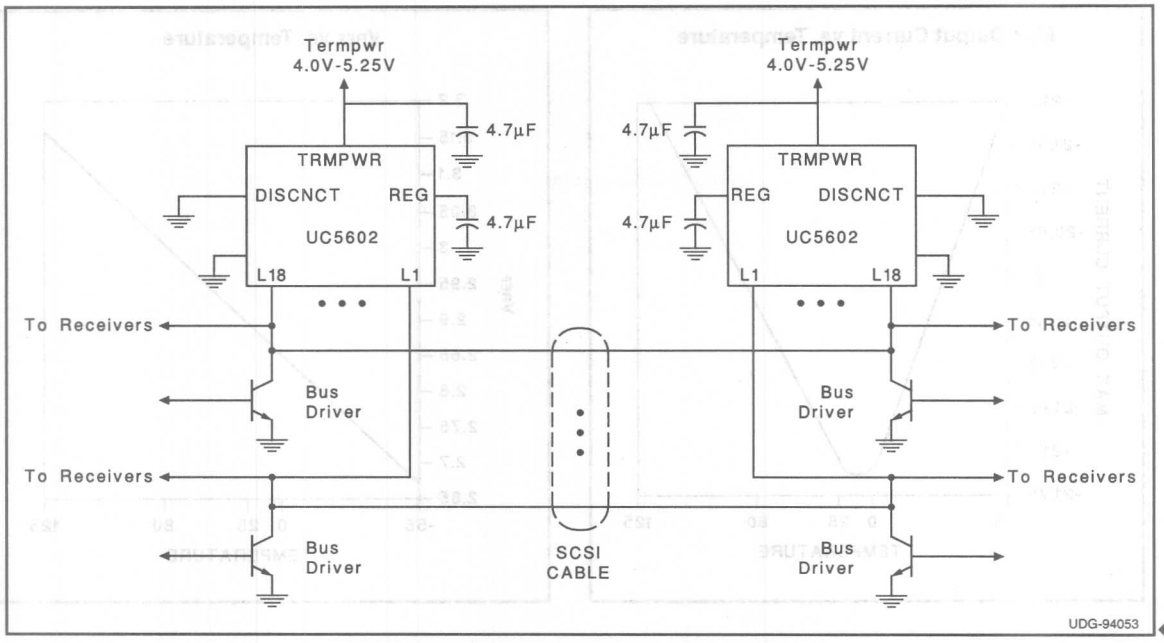
N package:

Thermal Resistance Junction to Leads, θjL ..... 50°C/W
Thermal Resistance Junction to Ambient, θja ..... 95°-105°C/W

QP package:

Thermal Resistance Junction to Leads, θjL ..... 15°C/W
Thermal Resistance Junction to Ambient, θja ..... 30°-40°C/W

Note: The above numbers for θjL are maximums for the limiting thermal resistance of the package in a standard mounting configuration. The θja numbers are meant to be guidelines for the thermal performance of the device/pc-board system. All of the above numbers assume no ambient airflow.



Typical SCSI Bus Configuration Using the UC5602

A Look at the Response of a SCSI-2 Cable

Figure 1 shows a single line of a SCSI cable. The driver is an open colletor type which when asserted pulls low, and when negated the termination resistance serves as the pull-up.

Figure 2 shows a worst case scenario of mid cable de-assertion with a close proximity receiver. The voltage V_{STEP} is defined as:

$$V_{STEP} = V_{OL} + I_O Z_0$$

V_{OL} = Driver Output Low Voltage
I_O = Current from Receiving Terminator
Z_0 = Cable Characteristic Impedance

$$I_O = \frac{V_{REG} - V_{OL}}{110}$$

In the pursuit of higher data rates, sampling could occur during this step portion, therefore it is important to ensure that the step is as high as possible to get the most noise margin. For this reason the UC5602 is trimmed so that the output current (I_O) is as close as possible to the SCSI max current spec of 22.4mA. The Termination impedance is initially trimmed on the IC to 110 ohms typical, then the regulator voltage is trimmed for the highest output current to within 22.4mA.

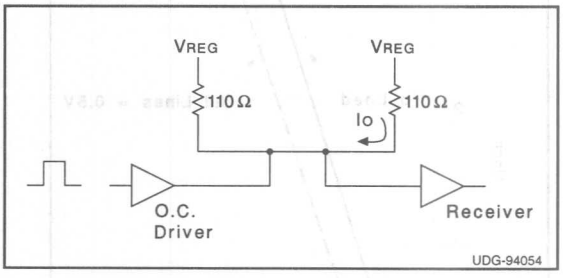


Figure 1. A Single Line of a SCSI Cable

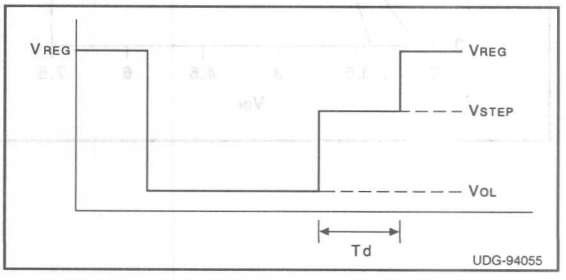
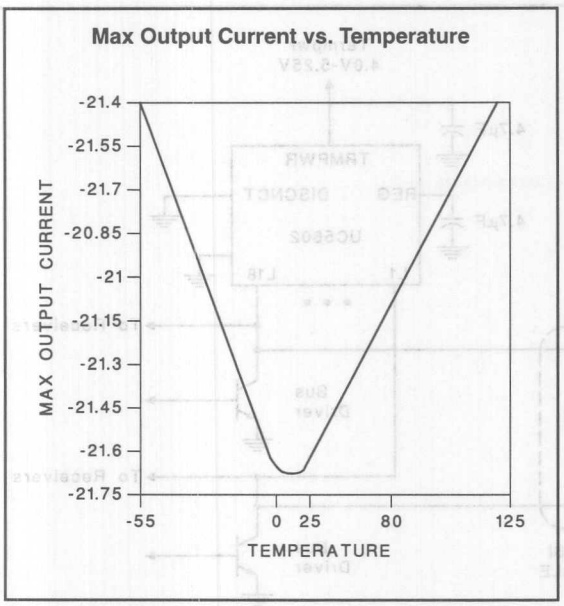
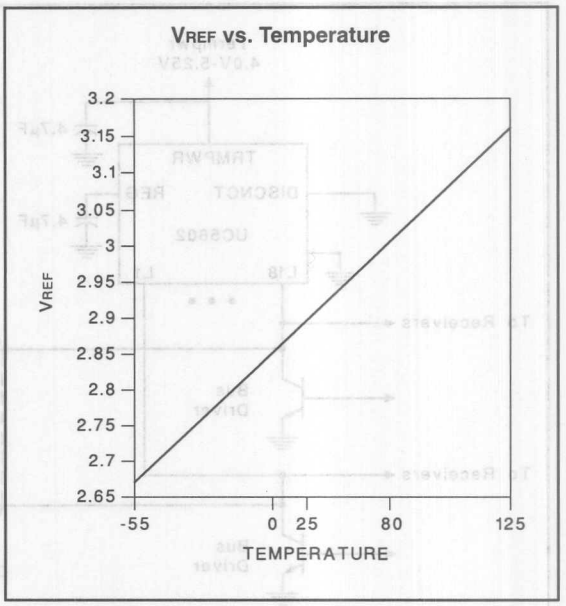
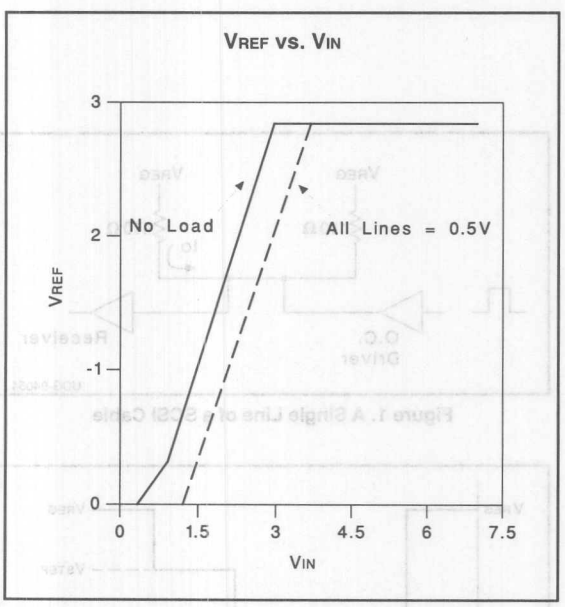
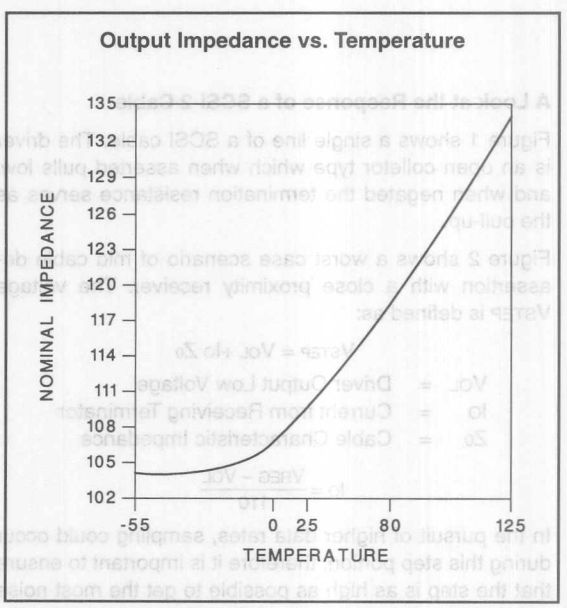


Figure 2. A Typical Response of a SCSI Cable









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UNITRODE

9-Line SCSI Active Terminator

FEATURES

- Complies with SCSI, SCSI-2 and SPI-2 Standards
- 6pF Channel Capacitance during Disconnect
- 100µA Supply Current in Disconnect Mode
- Meets SCSI Hot Plugging
- -400mA Sourcing Current for Termination
- +400mA Sinking Current for Active Negation Drivers
- Logic Command Disconnects all Termination Lines
- Trimmed Termination Current to 3%
- Trimmed Impedance to 3%
- Negative Clamping on all Signal Lines
- Current Limit and Thermal Shutdown Protection

DESCRIPTION

The UC5603 provides 9 lines of active termination for a SCSI (Small Computers Systems Interface) parallel bus. The SCSI standard recommends active termination at both ends of the cable segment.

The UC5603 provides a disconnect feature which, when opened or driven high, will disconnect all terminating resistors, and disables the regulator; greatly reducing standby power. The output channels remain high impedance even without Termpwr applied. A low channel capacitance of 6pF allows units at interim points of the bus to have little to no effect on the signal integrity.

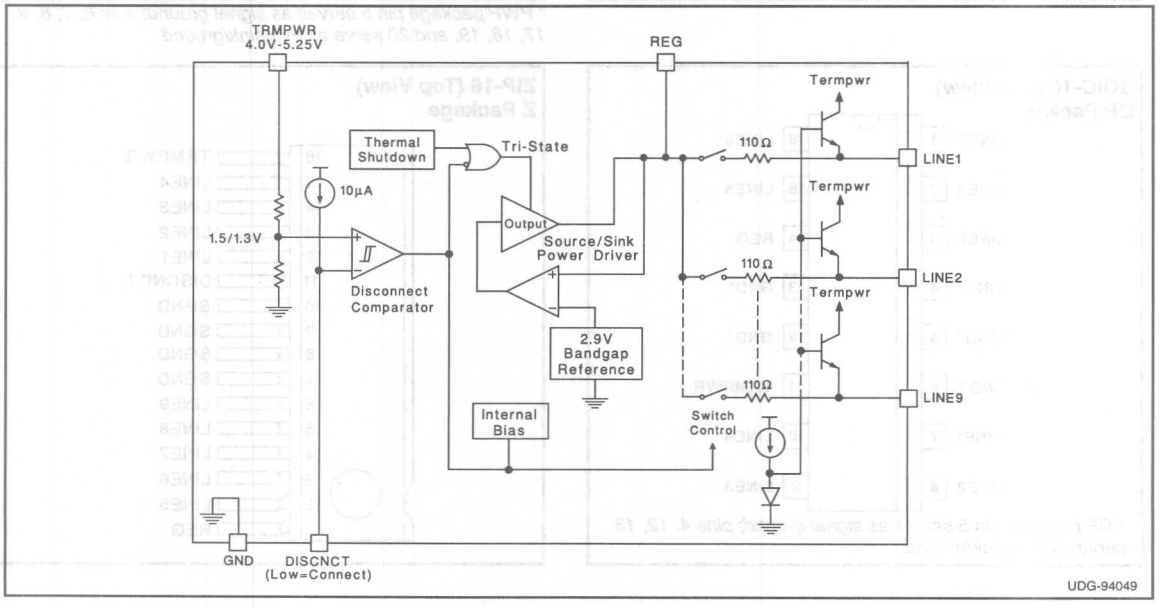
Functionally the UC5603 is similar to its predecessor, the UC5601 - 18 line Active Terminator. Several electrical enhancements were incorporated in the UC5603, such as a sink/source regulator output stage to accommodate all signal lines at +5V, while the regulator remains at its nominal value, reduced channel capacitance to 6pF typical, and as with the UC5601, custom power packages are utilized to allow normal operation at full power conditions (1.2 watts).

Internal circuit trimming is utilized, first to trim the impedance to a 3% tolerance, and then most importantly, to trim the output current to a 3% tolerance, as close to the max SCSI spec as possible, which maximizes noise margin in fast SCSI operation.

Other features include negative clamping on all signal lines to protect external circuitry from latch-up, thermal shutdown and current limit.

This device is offered in low thermal resistance versions of the industry standard 16 pin narrow body SOIC, 16 pin ZIP (zig-zag in line package) and 24 pin TSSOP.

BLOCK DIAGRAM



Circuit Design Patented

ABSOLUTE MAXIMUM RATINGS

Termpwr Voltage ..... +7V
Signal Line Voltage..... 0V to +7V
Regulator Output Current 0.5A
Storage Temperature ..... –65°C to +150°C
Operating Temperature ..... –55°C to +150°C
Lead Temperature (Soldering, 10 Sec.)..... +300°C

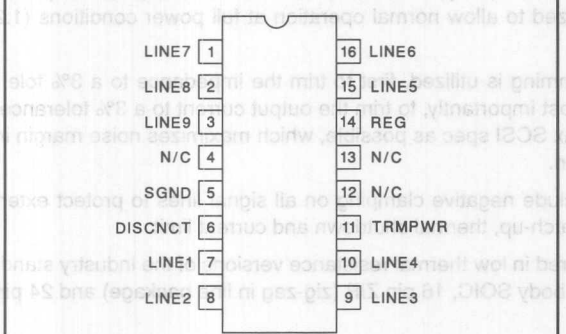
Unless otherwise specified all voltages are with respect to Ground. Currents are positive into, negative out of the specified terminal.
Consult Packaging Section of Unitrode Integrated Circuits databook for thermal limitations and considerations of packages.

RECOMMENDED OPERATING CONDITIONS

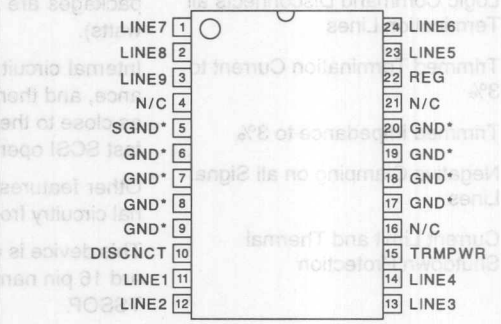
Termpwr Voltage ..... 3.8V to 5.25V
Signal Line Voltage..... 0V to +5V
Disconnect Input Voltage ..... 0V to Termpwr

CONNECTION DIAGRAMS

DIL-16 (Top View)
N or J Package

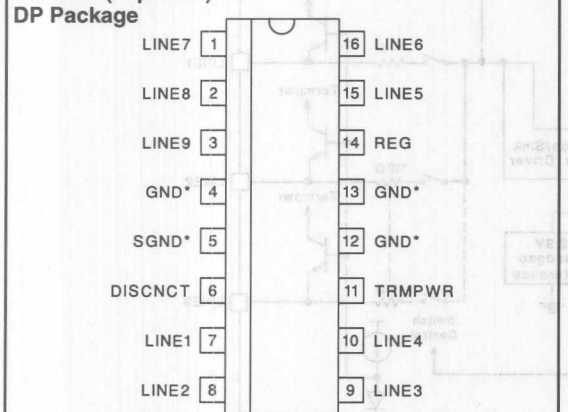


TSSOP-24 (Top View)
PWP Package



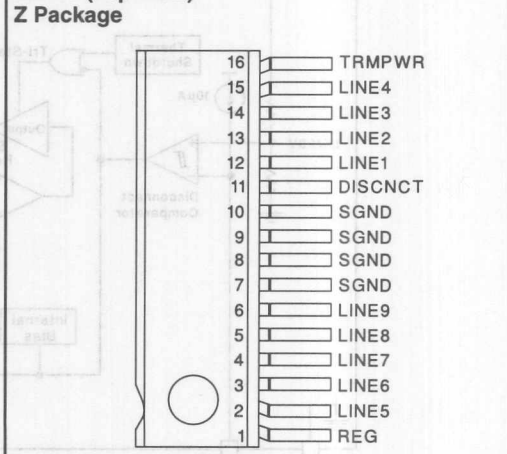
** PWP package pin 5 serves as signal ground; pins 6, 7, 8, 9, 17, 18, 19, and 20 serve as heatsink/ground.*

SOIC-16 (Top View)
DP Package



** DP package pin 5 serves as signal ground; pins 4, 12, 13 serve as heatsink/ground.*

ZIP-16 (Top View)
Z Package



Note: Drawings are not to scale.

ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for T_A= 0°C to 70°C. TRMPWR = 4.75V DISCNCT = 0V. T_A = T_J.

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNITS
Supply Current Section							
Termpwr Supply Current	All termination lines = Open				12	18	mA
	All termination lines = 0.5V				200	220	mA
Power Down Mode	DISCNCT = Open				100	150	µA
Output Section (Terminator Lines)							
Terminator Impedance	ΔI_{LINE} = -5mA to -15mA			107	110	113	Ohms
Output High Voltage	V_{TRMPWR} = 4V (Note 1)			2.7	2.9		V
Max Output Current	V_{LINE} = 0.5V		T_J = 25°C	-21.1	-21.9	-22.4	mA
			0°C < T_J < 70°C	-20.5	-21.9	-22.4	mA
Max Output Current	V_{LINE} = 0.5V, TRMPWR = 4V (Note 1)		T_J = 25°C	-20.3	-21.9	-22.4	mA
			0°C < T_J < 70°C	-19.8	-21.9	-22.4	mA
	V_{LINE} = 0.2V, TRMPWR = 4.0V to 5.25V		0°C < T_J < 70°C	–22.0	–24.0	–25.4	mA
Output Clamp Level	I_{LINE} = -30mA			-0.2	-0.05	0.1	V
Output Leakage	DISCNCT = 4V	TRMPWR = 0V to 5.25V REG = 0V	V_{LINE} = 0 to 4V		10	400	nA
			V_{LINE} = 5.25V			100	µA
		TRMPWR = 0V to 5.25V, REG = Open V_{LINE} = 0V to 5.25V			10	400	nA
Output Capacitance	DISCNCT = Open (Note 2) (DP Package)				6	8	pF
Regulator Section							
Regulator Output Voltage				2.8	2.9	3	V
Regulator Output Voltage	All Termination Lines = 5V			2.8	2.9	3	V
Line Regulation	TRMPWR = 4V to 6V				10	20	mV
Load Regulation	I_{REG} = +100mA to -100mA				20	50	mV
Drop Out Voltage	All Termination Lines = 0.5V				0.7	1	V
Short Circuit Current	V_{REG} = 0V			-200	-400	-600	mA
Sinking Current Capability	V_{REG} = 3.5V			200	400	600	mA
Thermal Shutdown					170		°C
Thermal Shutdown Hysteresis					10		°C
Disconnect Section							
Disconnect Threshold				1.3	1.5	1.7	V
Threshold Hysteresis				100	160	250	mV

Note 1: Measuring each termination line while other 8 are low (0.5V).
Note 2: Guaranteed by design. Not 100% tested in production.

APPLICATION INFORMATION

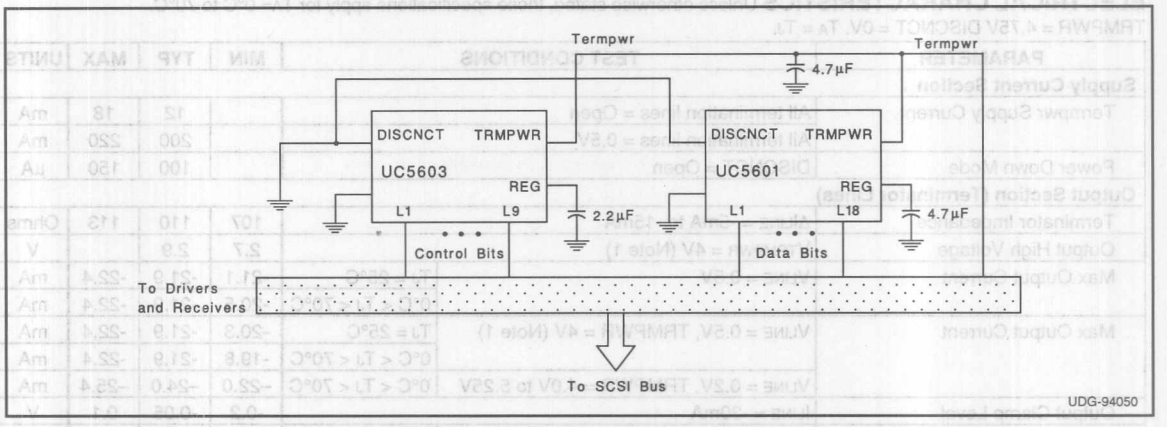


Figure 1: Typical Wide SCSI Bus Configurations Utilizing 1 UC5601 and 1 UC5603 Device

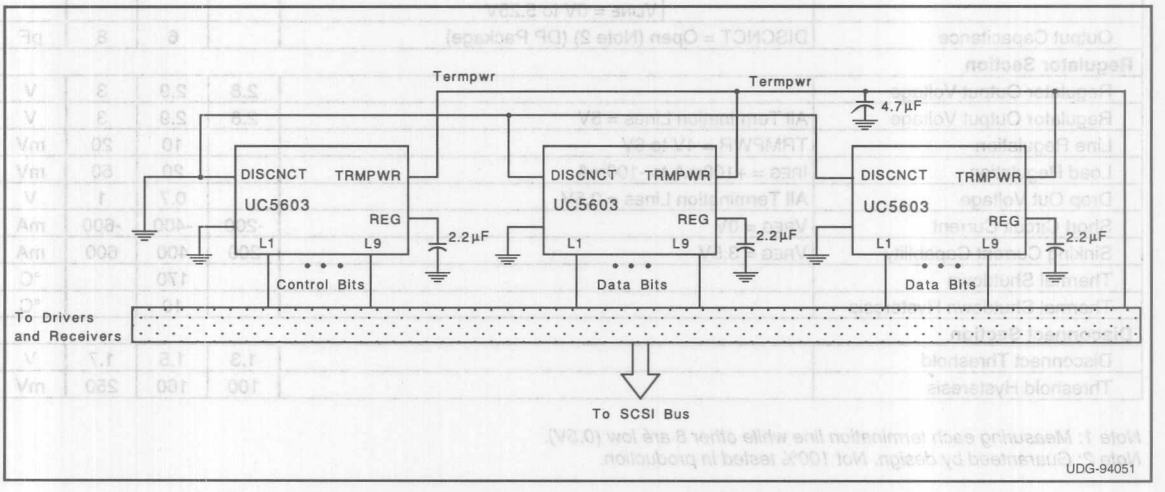


Figure 2: Typical Wide SCSI Bus Configurations Utilizing 3 UC5603 Devices.

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

UNITRODE

9-Line Low Capacitance SCSI Active Terminator

FEATURES

- Complies with SCSI, SCSI-2 Standards
- 9pF Channel Capacitance during Disconnect
- 100µA Supply Current in Disconnect Mode
- Meets SCSI Hot Plugging Capability
- –300mA Sourcing Current for Termination
- +40mA Sinking Current for Active Negation
- Logic Command Disconnects all Termination Lines
- Trimmed Termination Current to 7%
- Trimmed Impedance to 7%
- Current Limit and Thermal Shutdown Protection

DESCRIPTION

The UC5604 provides 9 lines of active termination for a SCSI (Small Computer Systems Interface) parallel bus. The SCSI standard recommends active termination at both ends of the cable segment.

The UC5604 provides a disconnect feature which, when opened or driven high, will disconnect all terminating resistors and disable the regulator, greatly reducing standby power. The output channels remain high impedance even without Termpwr applied.

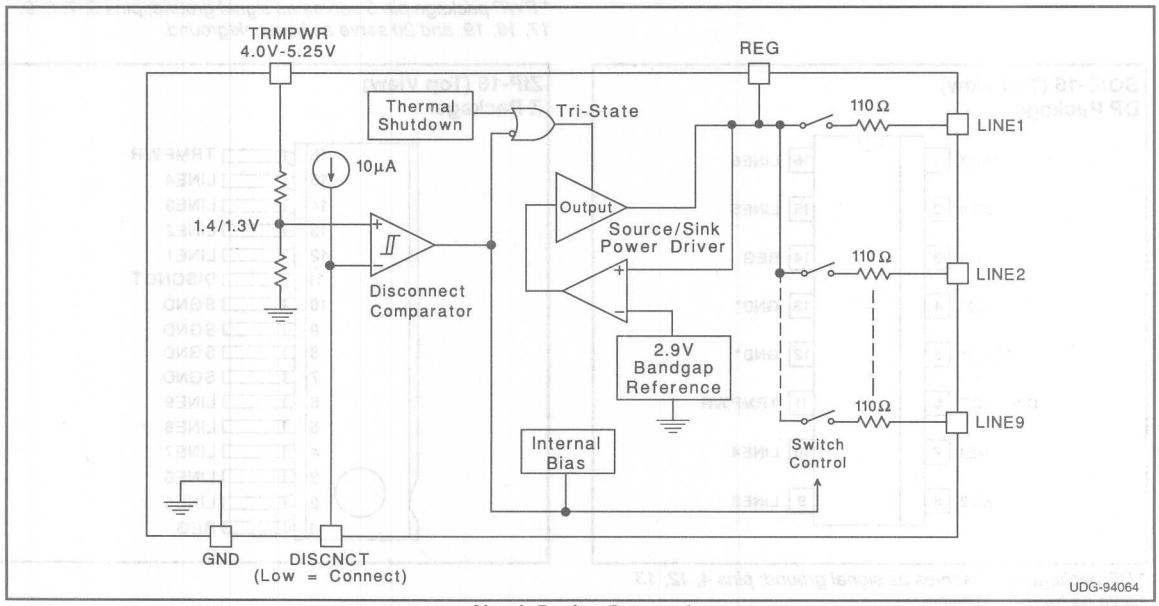
The UC5604 is pin-for-pin compatible with its predecessor, the UC5603 - 9 line Active Terminator. The only functional difference between the UC5604 and UC5603 is the absence of the negative clamps. Parametrically, the UC5604 has a 7% tolerance on impedance and current compared to a 3% tolerance on the UC5603 and the sink current is reduced from 300mA to 40mA. Custom power packages are utilized to allow normal operation at full power conditions (1.2 watts).

Internal circuit trimming is utilized, first to trim the impedance to a 7% tolerance, and then most importantly, to trim the output current to a 7% tolerance, as close to the max SCSI spec as possible, which maximizes noise margin in fast SCSI operation.

Other features include thermal shutdown and current limit.

This device is offered in low thermal resistance versions of the industry standard 16 pin narrow body SOIC, 16 pin ZIP (zig-zag in line package) and 24 pin TSSOP.

BLOCK DIAGRAM



Circuit Design Patented

ABSOLUTE MAXIMUM RATINGS

Termpwr Voltage ..... +7V
Signal Line Voltage..... 0V to +7V
Regulator Output Current 0.5A
Storage Temperature ..... –65°C to +150°C
Operating Temperature ..... –55°C to +150°C
Lead Temperature (Soldering, 10 Sec.)..... +300°C

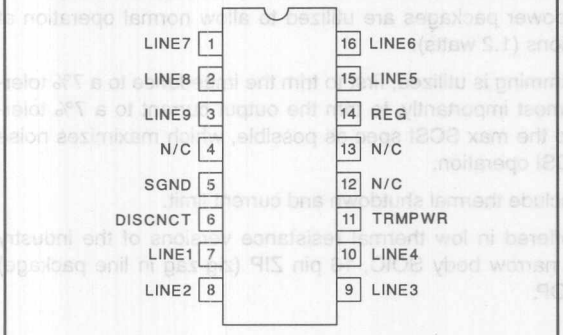
Unless otherwise specified all voltages are with respect to Ground. Currents are positive into, negative out of the specified terminal.
Consult Packaging Section of Unitrode Integrated Circuits databook for thermal limitations and considerations of packages.

RECOMMENDED OPERATING CONDITIONS

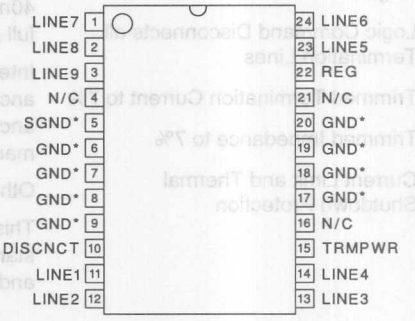
Termpwr Voltage ..... 3.8V to 5.25V
Signal Line Voltage..... 0V to +5V
Disconnect Input Voltage ..... 0V to Termpwr

CONNECTION DIAGRAMS

DIL-16 (Top View)
N or J Package

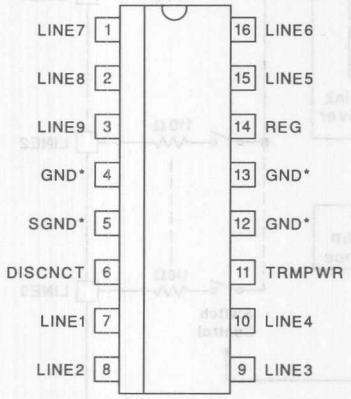


TSSOP-24 (Top View)
PWP Package

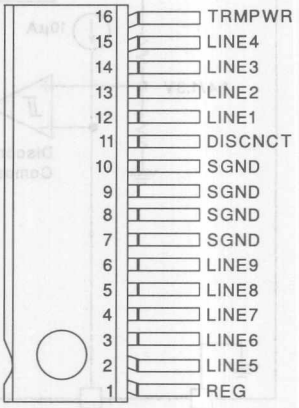


** PWP package pin 5 serves as signal ground; pins 6, 7, 8, 9, 17, 18, 19, and 20 serve as heatsink/ground.*

SOIC-16 (Top View)
DP Package



ZIP-16 (Top View)
Z Package



** DP package pin 5 serves as signal ground; pins 4, 12, 13 serve as heatsink/ground.*

Note: Drawings are not to scale.

ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C. TRMPWR = 4.75V, DISCNCT = 0V. T_A = T_J.

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNITS
Supply Current Section							
Termpwr Supply Current	All termination lines = Open				14	20	mA
	All termination lines = 0.5V				200	220	mA
Power Down Mode	DISCNCT = Open				100	150	µA
Output Section (Terminator Lines)							
Terminator Impedance	ΔI_{LINE} = -5mA to -15mA			97	110	129	Ohms
Output High Voltage	TRMPWR = 4V (Note 1)		0°C < T_J < 70°C	2.55		3.2	V
			T_J = 25°C	2.6	2.9	3.1	V
Max Output Current	V_{LINE} = 0.5V		T_J = 25°C	-19.5	-21.9	-22.4	mA
			0°C < T_J < 70°C	-18.5	-21.9	-22.4	mA
Max Output Current	V_{LINE} = 0.5V, TRMPWR = 4V (Note 1)		T_J = 25°C	-18.0	-21.9	-22.4	mA
			0°C < T_J < 70°C	-17.0	-21.9	-22.4	mA
Output Clamp Level	I_{LINE} = -30mA			-0.2	-0.05	0.1	V
Output Leakage	DISCNCT = 4V	TRMPWR = 0V to 5.25V REG = 0V	V_{LINE} = 0 to 4V		10	400	nA
			V_{LINE} = 5.25V			100	µA
		TRMPWR = 0V to 5.25V, REG = Open V_{LINE} = 0V to 5.25V			10	400	nA
Output Capacitance	DISCNCT = Open (Note 2)				9	12	pF
Regulator Section							
Regulator Output Voltage				2.5	2.9	3.2	V
Regulator Output Voltage	All Termination Lines = 5V			2.55	2.9	3.1	V
Line Regulation	TRMPWR = 4V to 6V				10	20	mV
Load Regulation	I_{REG} = +100mA to -100mA				20	50	mV
Drop Out Voltage	All Termination Lines = 0.5V				1.0	1.2	V
Short Circuit Current	V_{REG} = 0V			-200	-400	-600	mA
Sinking Current Capability	V_{REG} = 3.5V			20	40		mA
Thermal Shutdown					170		°C
Thermal Shutdown Hysteresis					10		°C
Disconnect Section							
Disconnect Threshold				1.1	1.4	1.7	V
Threshold Hysteresis					100		mV
Input Current	DISCNCT = 0V				150	200	µA

Note 1: Measuring each termination line while other 8 are low (0.5V).
Note 2: Guaranteed by design. Not 100% tested in production.

APPLICATION INFORMATION

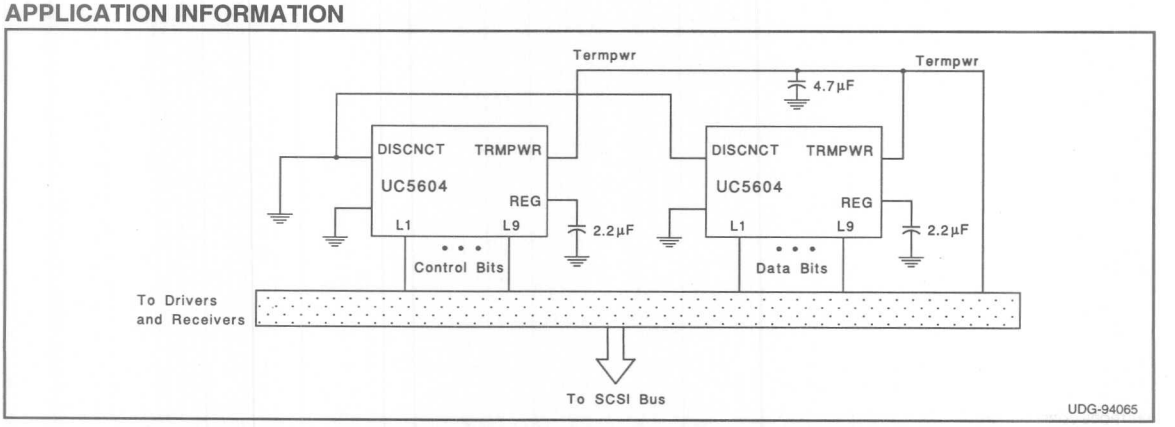


Figure 1: Typical SCSI Bus Configurations Utilizing 2 UC5604 Devices

APPLICATION INFORMATION (cont.)

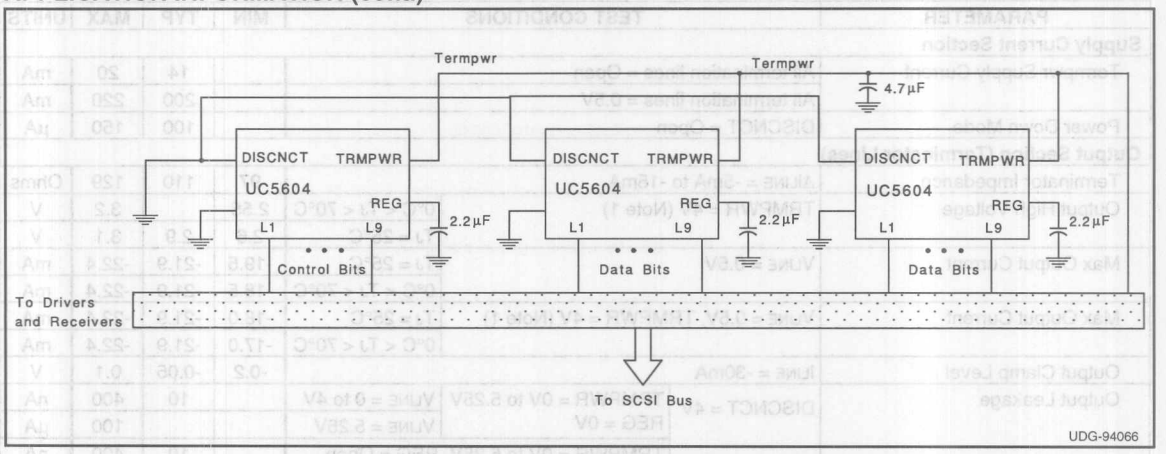


Figure 2: Typical Wide SCSI Bus Configurations Utilizing 3 UC5604 Devices.

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

UNITRODE

9-Line Low Capacitance SCSI Active Terminator

FEATURES

- Reverse Disconnect
- Complies with SCSI, SCSI-2 and SPI-2 Standards
- 5pF Channel Capacitance during Disconnect
- Hot Plugging Capability
- –400mA Sourcing Current for Termination
- +100mA Sinking Current for Active Negation
- 1V Dropout Voltage Regulator
- 100µA Supply Current in Disconnect Mode
- Trimmed Termination Current to 5%
- Trimmed Impedance to 5%
- Low Thermal Resistance Surface Mount Packages

DESCRIPTION

The UC5605 provides 9 lines of active termination for a SCSI (Small Computer Systems Interface) parallel bus. The SCSI standard recommends active termination at both ends of the cable segment.

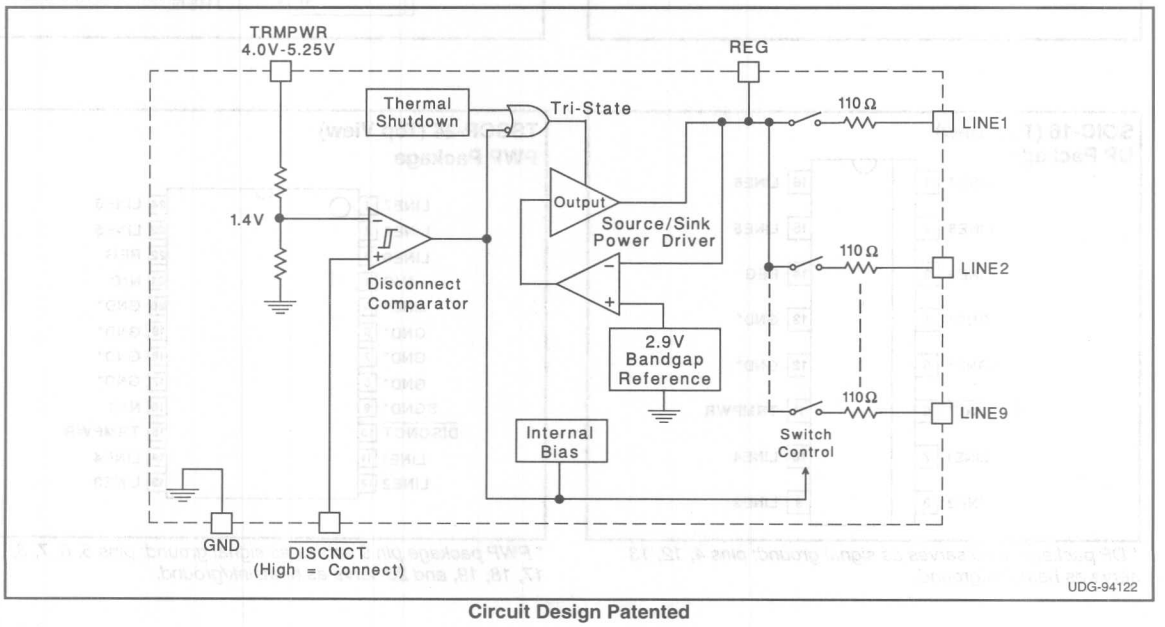
The only functional differences between the UC5603 and UC5605 is the absence of the negative clamps on the output lines and the disconnect input must be at a logic-low for the terminating resistors to be disconnected. Parametrically, the UC5605 has a 5% tolerance on impedance and current compared to a 3% tolerance on the UC5603. Custom power packages are utilized to allow normal operation at full power (2 Watts).

The UC5605 provides a disconnect feature which, when driven low, disconnects all terminating resistors, disables the regulator and greatly reduces standby power consumption. The output channels remain high impedance even without Termpwr applied. A low channel capacitance of 5pF allows interim points of the bus to have little to no effect on the signal integrity.

Internal circuit trimming is utilized, first to trim the impedance to a 5% tolerance, and then most importantly, to trim the output current to a 5% tolerance, as close to the maximum SCSI specification as possible. This maximizes the noise margin in fast SCSI operation. Other features include thermal shutdown and current limit.

This device is offered in low thermal resistance versions of the industry standard 16 pin narrow body SOIC, 16 pin ZIP (zig-zag in line package) and 24 pin TSSOP.

BLOCK DIAGRAM



Circuit Design Patented

3/97

ABSOLUTE MAXIMUM RATINGS

Termpwr Voltage . . . . . +7V
Signal Line Voltage . . . . . 0V to +7V
Regulator Output Current 0.6A
Storage Temperature . . . . . –65°C to +150°C
Operating Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 Sec.) . . . . . +300°C

Unless otherwise specified all voltages are with respect to Ground. Currents are positive into, negative out of the specified terminal.

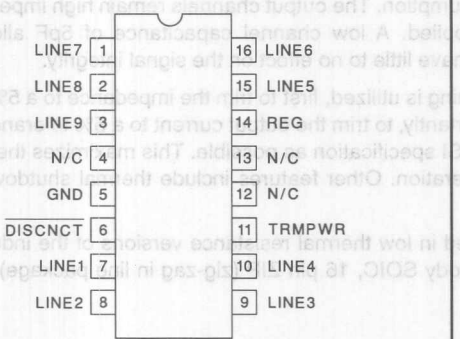
Consult Packaging Section of Unitrode Integrated Circuits databook for thermal limitations and considerations of packages.

RECOMMENDED OPERATING CONDITIONS

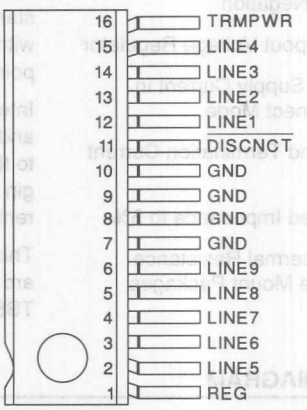
Termpwr Voltage . . . . . 3.8V to 5.25V
Signal Line Voltage . . . . . 0V to +5V
Disconnect Input Voltage . . . . . 0V to Termpwr

CONNECTION DIAGRAMS

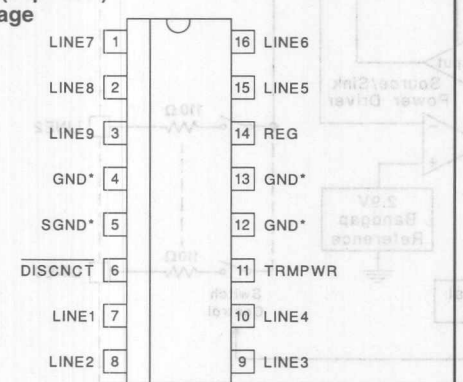
DIL-16 (Top View)
N or J Package



ZIP-16 (Top View)
Z Package

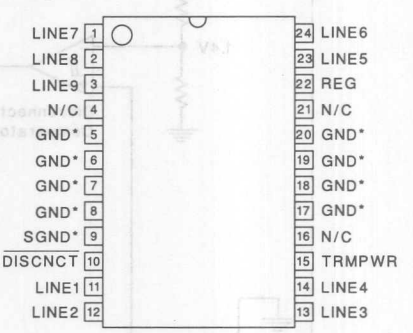


SOIC-16 (Top View)
DP Package



** DP package pin 5 serves as signal ground; pins 4, 12, 13 serve as heatsink/ground.*

TSSOP-24 (Top View)
PWP Package



** PWP package pin 9 serves as signal ground; pins 5, 6, 7, 8, 17, 18, 19, and 20 serve as heatsink/ground.*

Note: Drawings are not to scale.

ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C. TRMPWR = 4.75V, $\overline{\text{DISCNCT}}$ = 2.4V, $T_A = T_J$.

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNITS
Supply Current Section							
Termpwr Supply Current	All termination lines = Open				17	23	mA
	All termination lines = 0.5V				200	225	mA
Power Down Mode	$\overline{\text{DISCNCT}}$ = 0V				100	150	µA
Output Section (Termination Lines)							
Terminator Impedance	ΔI_{LINE} = -5mA to -15mA			104.5	110	115.5	Ohms
Output High Voltage	TRMPWR = 4V			2.65	2.9	3.1	V
Max Output Current	V_{LINE} = 0.5V		T_J = 25°C	-20.3	-21.5	-22.4	mA
			0°C < T_J < 70°C	-19.8	-21.5	-22.4	mA
Max Output Current	V_{LINE} = 0.5V, TRMPWR = 4V (Note 1)		T_J = 25°C	-19.5	-21.5	-22.4	mA
			0°C < T_J < 70°C	-19.0	-21.5	-22.4	mA
	V_{LINE} = 0.2V, TRMPWR = 4.0V to 5.25V		0°C < T_J < 70°C	–21.6	–24.0	–25.4	mA
Output Leakage	$\overline{\text{DISCNCT}}$ = 0V, TRMPWR = 0V to 5.25V	REG = 0V	V_{LINE} = 0 to 4V		10	400	nA
			V_{LINE} = 5.25V			100	µA
		REG = Open	V_{LINE} = 0V to 5.25V		10	400	nA
Output Capacitance	$\overline{\text{DISCNCT}}$ = 0V (Note 2) (DP Package)				5	6	pF
Regulator Section							
Regulator Output Voltage				2.7	2.9	3.1	V
	All Termination Lines = 4V			2.7	2.9	3.1	V
Line Regulation	TRMPWR = 4V to 6V				10	20	mV
Drop Out Voltage	All Termination Lines = 0.5V				1.0	1.2	V
Short Circuit Current	REG = 0V			-200	-400	-600	mA
Sinking Current Capability	REG = 3.5V			75	100	400	mA
Thermal Shutdown					170		°C
Thermal Shutdown Hysteresis					10		°C
Disconnect Section							
Disconnect Threshold				1.1	1.4	1.7	V

Note 1: Measuring each termination line while other 8 are low.
Note 2: Guaranteed by design. Not 100% tested in production.

APPLICATION INFORMATION

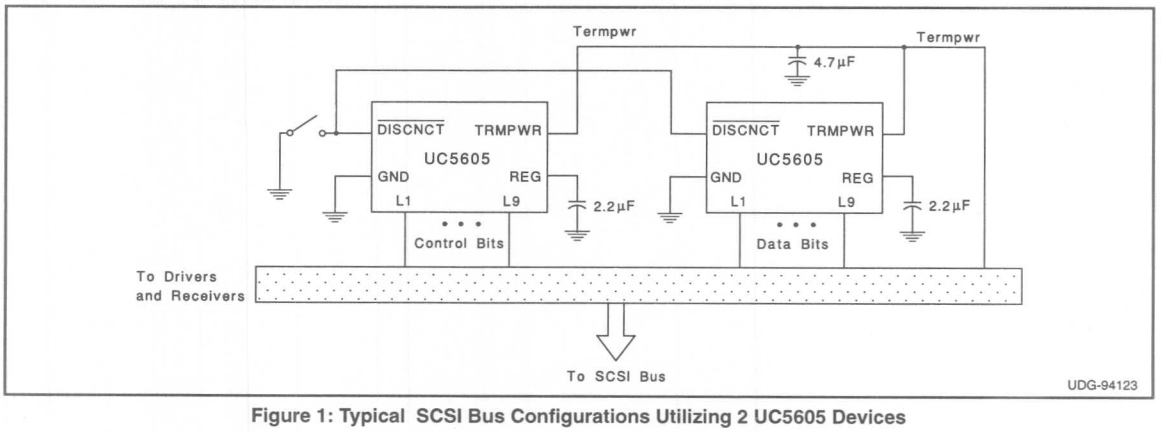


Figure 1: Typical SCSI Bus Configurations Utilizing 2 UC5605 Devices

APPLICATION INFORMATION (cont.)

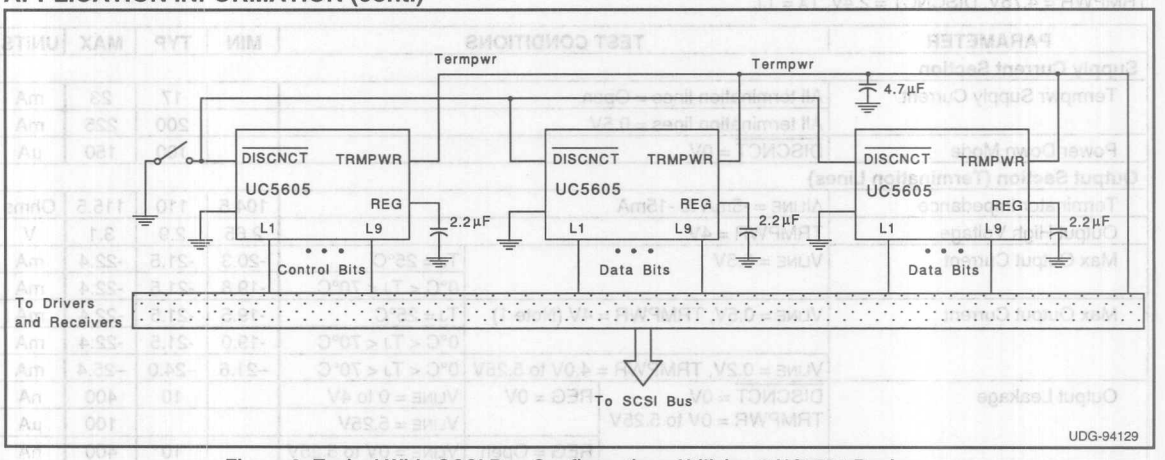


Figure 2: Typical Wide SCSI Bus Configurations Utilizing 3 UC5605 Devices.

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

UNITRODE

9-Line 3-5 Volt SCSI Active Terminator, Reverse Disconnect

FEATURES

- Complies with SCSI, SCSI-2 and SCSI-3 Standards
- 2.7V to 7V Operation
- 1.8pF Channel Capacitance during Disconnect
- 1µA Supply Current in Disconnect Mode
- 110 Ohm/2.5k Programmable Termination
- Completely Meets SCSI Hot Plugging
- -400mA Sourcing Current for Termination
- +400mA Sinking Current for Active Negation Drivers
- Trimmed Termination Current to 4%
- Trimmed Impedance to 7%
- Current Limit and Thermal Shutdown Protection

DESCRIPTION

The UCC5606 provides 9 lines of active termination for a SCSI (Small Computer Systems Interface) parallel bus. The SCSI standard recommends active termination at both ends of the cable segment.

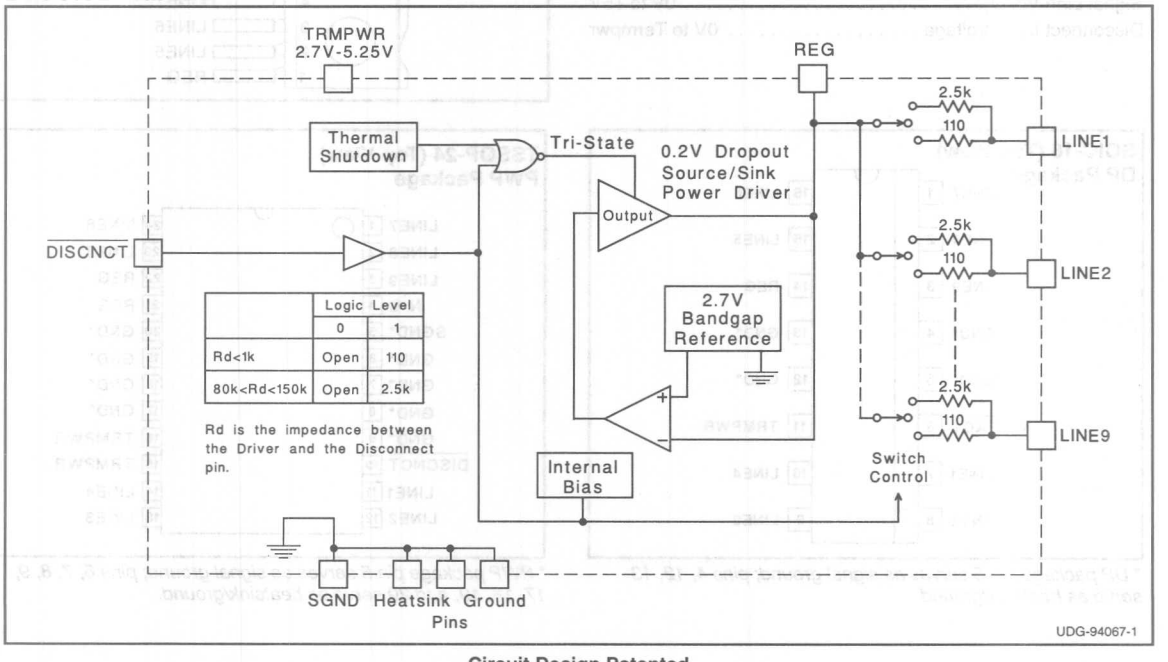
The UCC5606 is ideal for high performance 3.3V SCSI systems. The key features contributing to such low operating voltage are the 0.1V drop out regulator and the 2.7V reference. The reduced reference voltage was necessary to accommodate the lower termination current dictated in the SCSI-3 specification. During disconnect the supply current is typically only 1µA, which makes the IC attractive for battery powered systems.

The UCC5606 is designed with an ultra low channel capacitance of 1.8pF, which eliminates effects on signal integrity from disconnected terminators at interim points on the bus.

The UCC5606 can be programmed for either a 110 ohm or 2.5k ohm termination. The 110 ohm termination is used for standard SCSI bus lengths and the 2.5k ohm termination is typically used in short bus applications. When driving the TTL compatible $\overline{\text{DISCNCT}}$ pin directly, the 110 ohm termination is connected when the $\overline{\text{DISCNCT}}$ pin is driven high, and disconnected when low. When the $\overline{\text{DISCNCT}}$ pin is driven through an impedance between 80k and 150k, the 2.5k ohm termination is connected when the $\overline{\text{DISCNCT}}$ pin is driven high, and disconnected when driven low.

continued

BLOCK DIAGRAM



	Logic Level	
	0	1
Rd<1k	Open	110
80k<Rd<150k	Open	2.5k

Rd is the impedance between the Driver and the Disconnect pin.

Circuit Design Patented

Description Continued

The power amplifier output stage allows the UCC5606 to source full termination current and sink active negation current when all termination lines are actively negated.

The UCC5606 is pin for pin compatible with Unitrode's other 9 line SCSI terminators, except that $\overline{\text{DISCNCT}}$ is now active low, allowing lower capacitance and lower voltage upgrades to existing systems. The UCC5606, as with all Unitrode terminators, is completely hot pluggable and appears as high impedance at the terminating channels with V_{TRMPWR} = 0V or open.

Internal circuit trimming is utilized, first to trim the 110 ohm termination impedance to a 7% tolerance, and then most importantly, to trim the output current to a 4% tolerance, as close to the max SCSI-3 spec as possible, which maximizes noise margin in fast SCSI operation.

Other features include thermal shutdown and current limit.

This device is offered in low thermal resistance versions of the industry standard 16 pin narrow body SOIC, 16 pin ZIP (Zig-Zag In Line package), 24 pin TSSOP and 28 pin PLCC.

ABSOLUTE MAXIMUM RATINGS

Termpwr Voltage	+7V
Signal Line Voltage	0V to +7V
Regulator Output Current	0.6A
Storage Temperature	–65°C to +150°C
Operating Temperature	–55°C to +150°C
Lead Temperature (Soldering, 10 Sec.)	+300°C

Unless otherwise specified all voltages are with respect to Ground. Currents are positive into, negative out of the specified terminal.

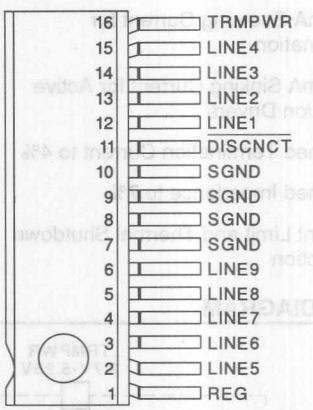
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RECOMMENDED OPERATING CONDITIONS

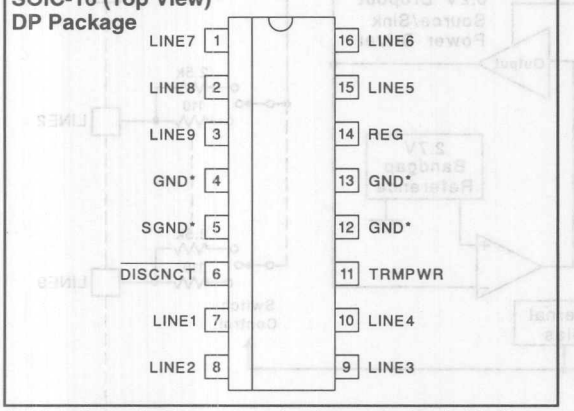
Termpwr Voltage	2.7V to 5.25V
Signal Line Voltage	0V to +5V
Disconnect Input Voltage	0V to Termpwr

CONNECTION DIAGRAMS

ZIP-16 (Top View)
Z Package

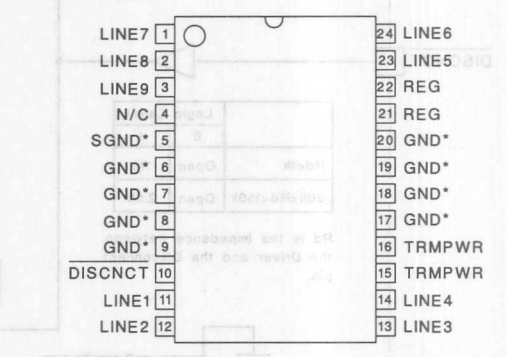


SOIC-16 (Top View)
DP Package



** DP package pin 5 serves as signal ground; pins 4, 12, 13 serve as heatsink/ground.*

TSSOP-24 (Top View)
PWP Package

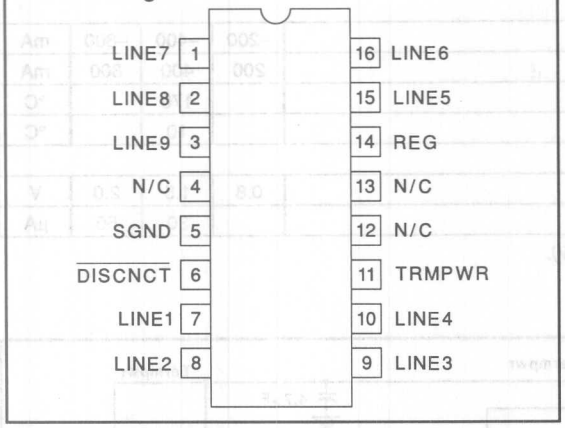


** PWP package pin 5 serves as signal ground; pins 6, 7, 8, 9, 17, 18, 19, and 20 serve as heatsink/ground.*

Note: Drawings are not to scale.

CONNECTION DIAGRAMS (cont.)

DIL-16 (Top View)
N or J Package



Note: Drawings are not to scale.

ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C. TRMPWR = 3.3V, $\overline{\text{DISCNCT}}$ = 3.3V, $R_{DISCNCT}$ = 0 ohms. $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current Section					
Termpwr Supply Current	All termination lines = Open		1	2	mA
	All termination lines = 0.2V		210	218	mA
Power Down Mode	$\overline{\text{DISCNCT}}$ = 0V		0.5	5	µA
Output Section (110 ohms - Terminator Lines)					
Terminator Impedance		102.3	110	117.7	Ohms
Output High Voltage	TRMPWR = 3V (Note 1)	2.5	2.7	3.0	V
Max Output Current	V_{LINE} = 0.2V, T_J = 25°C	–22.1	–23	–24	mA
	V_{LINE} = 0.2V	–21	–23	–24	mA
	V_{LINE} = 0.2V, TRMPWR = 3V, T_J = 25°C (Note 1)	–20.2	–23	–24	mA
	V_{LINE} = 0.2V, TRMPWR = 3V (Note 1)	–19	–23	–24	mA
	V_{LINE} = 0.5V			–22.4	mA
Output Leakage	$\overline{\text{DISCNCT}}$ = 0V, TRMPWR = 0V to 5.25V		10	400	nA
Output Capacitance	$\overline{\text{DISCNCT}}$ = 0V, DP Package (Note 2)		1.8	2.5	pF
Output Section (2.5k ohms - Terminator Lines) ($R_{DISCNCT}$ = 80k ohms)					
Terminator Impedance		2	2.5	3	kΩ
Output High Voltage	TRMPWR = 3V (Note 1)	2.5	2.7	3.0	V
Max Output Current	V_{LINE} = 0.2V	–0.7	–1	–1.4	mA
	V_{LINE} = 0.2V, TRMPWR = 3V (Note 1)	–0.6	–1	–1.5	mA
Output Leakage	$\overline{\text{DISCNCT}}$ = 0V, TRMPWR = 0 to 5.25V		10	400	nA
Output Capacitance	$\overline{\text{DISCNCT}}$ = 0V, DP Package (Note 2)		1.8	2.5	pF
Regulator Section					
Regulator Output Voltage	5.25V > TRMPWR > 3V	2.5	2.7	3.0	V
Drop Out Voltage	All Termination Lines = 0.2V		0.1	0.2	V

ELECTRICAL CHARACTERISTICS (cont.) Unless otherwise stated, these specifications apply for T_A=0°C to 70°C. TRMPWR = 3.3V, $\overline{DISCNCT}$ = 3.3V, $R_{DISCNCT}$ = 0 ohms. $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Regulator Section (cont.)					
Short Circuit Current	V_{REG} = 0V	–200	–400	–800	mA
Sinking Current Capability	V_{REG} = 3V	200	400	800	mA
Thermal Shutdown	(Note 2)		170		°C
Thermal Shutdown Hysteresis	(Note 2)		10		°C
Disconnect Section					
Disconnect Threshold	$R_{DISCNCT}$ = 0 & 80k	0.8	1.5	2.0	V
Input Current	$\overline{DISCNCT}$ = 3.3V		30	50	µA

Note 1: Measuring each termination line while other 8 are low (0.2V).
Note 2: Guaranteed by design. Not 100% tested in production.

APPLICATION INFORMATION

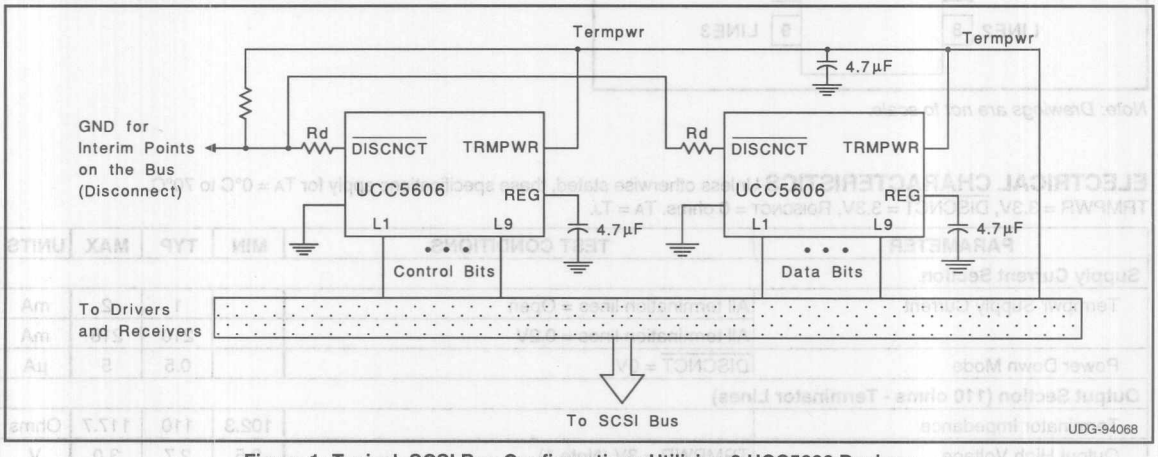


Figure 1: Typical SCSI Bus Configurations Utilizing 2 UCC5606 Devices

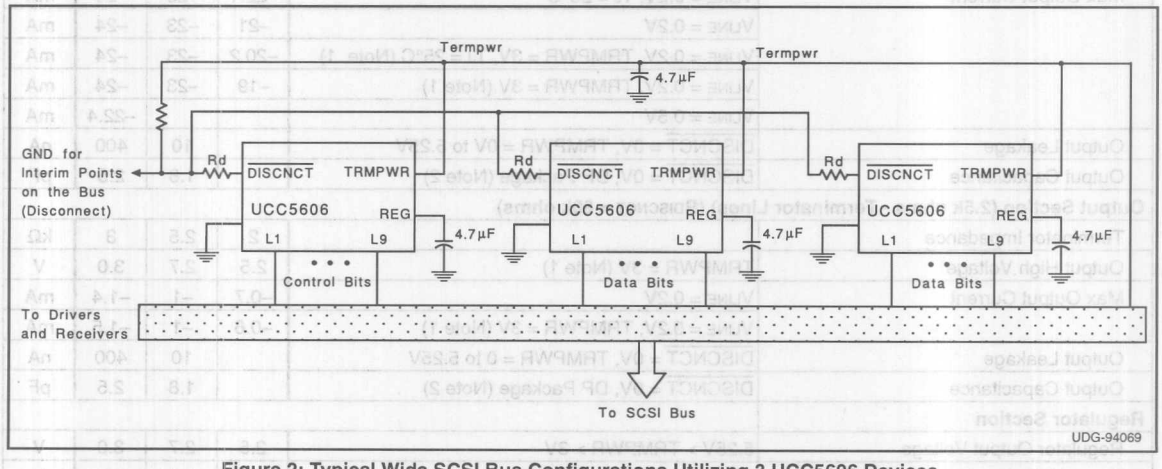


Figure 2: Typical Wide SCSI Bus Configurations Utilizing 3 UCC5606 Devices.

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

Plug and Play, 18-Line SCSI Active Terminator

FEATURES

- Complies with SCSI and SCSI-2 Standards
- 8pF Channel Capacitance during Disconnect
- SCSI Plug and Play, Dual Low Disconnect, Logic Low Command Disconnects All Termination Lines
- Meets SCSI Hot Plugging Capability
- –650mA Sourcing Current for Termination
- +200mA Sinking Current for Active Negation
- 200µA Supply Current in Disconnect Mode
- Trimmed Termination Current to 7%
- Trimmed Impedance to 7%
- Provides Active Termination for 18 Lines
- Current Limit and Thermal Shutdown Protection
- Low Thermal Resistance Surface Mount Packages

DESCRIPTION

The UC5607 provides 18 lines of active termination for a SCSI (Small Computer Systems Interface) parallel bus. The SCSI standard recommends active termination at both ends of the cable segment.

The UC5607 provides a low disconnect feature which will disconnect all terminating resistors, and will disable the regulator, greatly reducing standby power. The output channels remain high impedance even without Termpwr applied.

The UC5607 terminator is specially designed with two disconnect pins for full SCSI Plug and Play (PnP) applications.

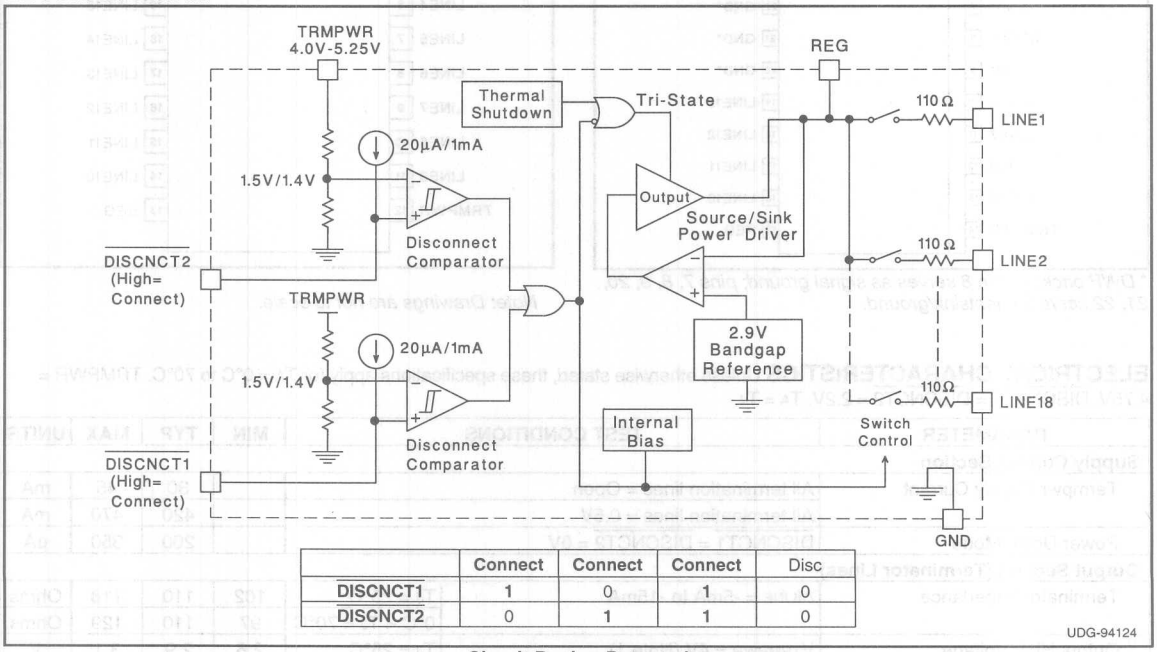
Custom power packages are utilized to allow normal operation at full power conditions (2 Watts).

Internal circuit trimming is utilized, first to trim the impedance to a 7% tolerance, and then most importantly, to trim the output current to a 7% tolerance, as close to the max SCSI spec as possible, which maximizes noise margin in fast SCSI operation.

Other features include thermal shutdown and current limit.

This device is offered in low thermal resistance versions of the industry standard 28 pin wide body SOIC, and 28 pin PLCC, as well as 24 pin DIP.

BLOCK DIAGRAM



	Connect	Connect	Connect	Disc
$\overline{\text{DISCNCT1}}$	1	0	1	0
$\overline{\text{DISCNCT2}}$	0	1	1	0

UDG-94124

Circuit Design Patented

12/94

ABSOLUTE MAXIMUM RATINGS

Termpwr Voltage ..... +7V
Signal Line Voltage..... 0V to +7V
Regulator Output Current..... 1A
Storage Temperature ..... –65°C to +150°C
Operating Temperature ..... –55°C to +150°C
Lead Temperature (Soldering, 10 Sec.)..... +300°C

Unless otherwise specified all voltages are with respect to Ground. Currents are positive into, negative out of the specified terminal.

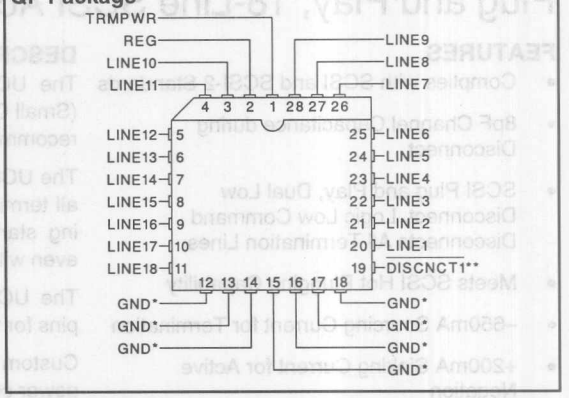
Consult Packaging Section of Unitrode Integrated Circuits databook for thermal limitations and considerations of packages.

RECOMMENDED OPERATING CONDITIONS

Termpwr Voltage ..... 3.8V to 5.25V
Signal Line Voltage..... 0V to +5V
Disconnect Input Voltage ..... 0V to Termpwr

CONNECTION DIAGRAMS

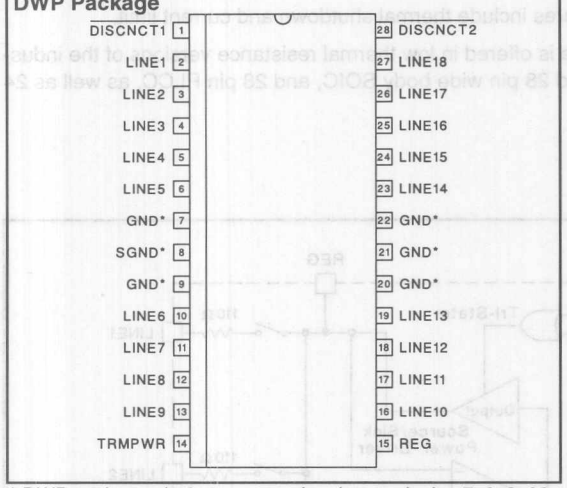
PLCC-28 (Top View)
QP Package



** QP package pins 12 - 18 serve as both heatsink and signal ground.*

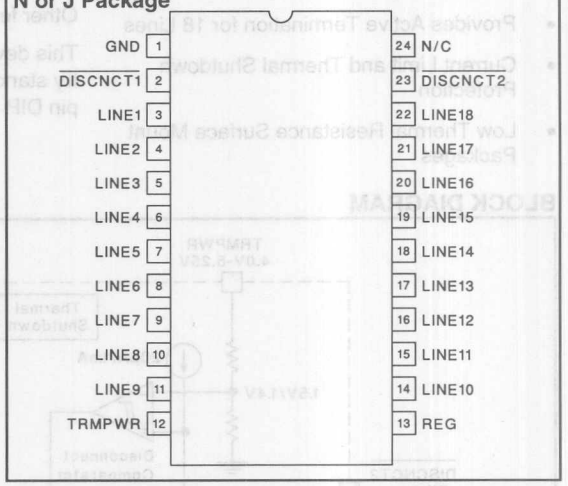
*** $\overline{\text{DISCNCT2}}$ is internally tied to ground.*

SOIC-28 (Top View)
DWP Package



** DWP package pin 8 serves as signal ground; pins 7, 8, 9, 20, 21, 22 serve as heatsink/ground.*

DIL-24 (Top View)
N or J Package



Note: Drawings are not to scale.

ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C. TRMPWR = 4.75V, $\overline{\text{DISCNCT1}}$ = $\overline{\text{DISCNCT2}}$ = 2.2V. T_A = T_J.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Supply Current Section						
Termpwr Supply Current	All termination lines = Open			30	45	mA
	All termination lines = 0.5V			420	470	mA
Power Down Mode	$\overline{\text{DISCNCT1}}$ = $\overline{\text{DISCNCT2}}$ = 0V			200	350	µA
Output Section (Terminator Lines)						
Terminator Impedance	ΔI_{LINE} = -5mA to -15mA	T_J = 25°C	102	110	118	Ohms
		0°C < T_J < 70°C	97	110	129	Ohms
Output High Voltage	V_{TRMPWR} = 4V (Note 1)	T_J = 25°C	2.6	2.9	3.1	V
		0°C < T_J < 70°C	2.55	2.9	3.2	V

ELECTRICAL CHARACTERISTICS (cont.) Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C. TRMPWR = 4.75V, $\overline{DISCNCT1}$ = $\overline{DISCNCT2}$ = 2.2V. T_A = T_J.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Output Section (Terminator Lines) cont.						
Max Output Current	V_{LINE} = 0.5V	T_J = 25°C	-19.5	-21.9	-22.4	mA
		0°C < T_J < 70°C	-18.5	-21.9	-22.4	mA
Max Output Current	V_{LINE} = 0.5V, TRMPWR = 4V (Note 1)	T_J = 25°C	-18.0	-21.9	-22.4	mA
		0°C < T_J < 70°C	-17.0	-21.9	-22.4	mA
Output Leakage	$\overline{DISCNCT1}$ = $\overline{DISCNCT2}$ = 0V, TRMPWR = 0V to 5.25V			10	400	nA
Output Capacitance	$\overline{DISCNCT1}$ = $\overline{DISCNCT2}$ = 0V (Note 2)			8	10	pF
Regulator Section						
Regulator Output Voltage	All Termination Lines = 5V	T_J = 25°C	2.7	2.9	3.1	V
		0°C < T_J < 70°C	2.55	2.9	3.2	V
Line Regulation	TRMPWR = 4V to 6V			10	20	mV
Load Regulation	I_{REG} = +100mA to -100mA			20	50	mV
Drop Out Voltage	All Termination Lines = 0.5V			1.0	1.2	V
Short Circuit Current	REG = 0V		-450	-650	-850	mA
Sinking Current Capability	REG = 3.5V		100	200	500	mA
Thermal Shutdown				170		°C
Thermal Shutdown Hysteresis				10		°C
Disconnect Section						
Disconnect Threshold			0.8	1.4	2.0	V
Threshold Hysteresis				100		mV
Input Current	$\overline{DISCNCT1}$ = $\overline{DISCNCT2}$ = 0V			-20	-50	µA
	$\overline{DISCNCT1}$ = $\overline{DISCNCT2}$ = 2.4V			-1		mA

Note 1: Measuring each termination line while other 17 are low (0.5V).
Note 2: Guaranteed by design. Not 100% tested in production.

APPLICATION INFORMATION

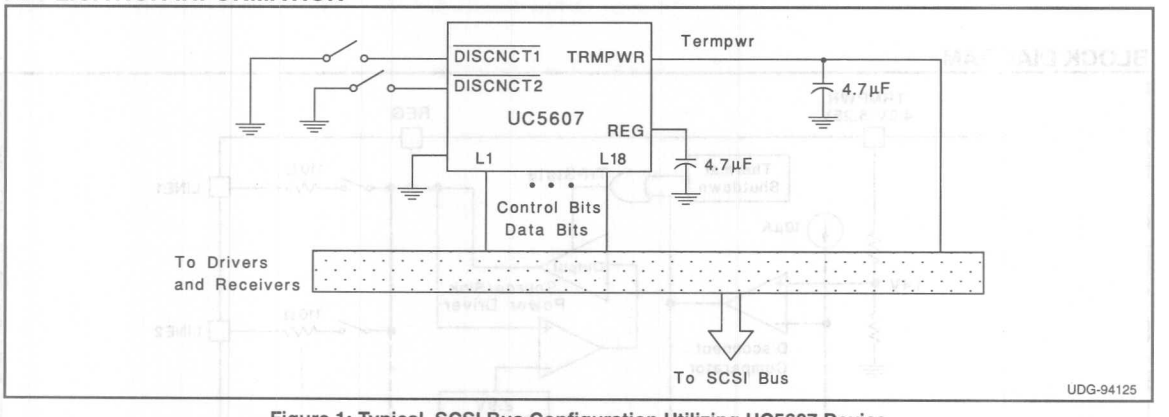


Figure 1: Typical SCSI Bus Configuration Utilizing UC5607 Device

UNITRODE CORPORATION
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TEL. (603) 424-2410 • FAX (603) 424-3460

UNITRODE

18-Line Low Capacitance SCSI Active Terminator

FEATURES

- Complies with SCSI, SCSI-2 and SPI-2 Standards
- 6pF Channel Capacitance during Disconnect
- 100µA Supply Current in Disconnect Mode
- Meets SCSI Hot Plugging Capability
- –650mA Sourcing Current for Termination
- +200mA Sinking Current for Active Negation
- Provides Active Termination for 18 Lines
- Logic Command Disconnects all Termination Lines
- Trimmed Termination Current to 5%
- Trimmed Impedance to 5%
- Current Limit and Thermal Shutdown Protection

DESCRIPTION

The UC5608 provides 18 lines of active termination for a SCSI (Small Computer Systems Interface) parallel bus. The SCSI standard recommends active termination at both ends of the bus cable.

The UC5608 is pin-for-pin compatible with its predecessors, the UC5601 and UC5602 - 18 Line Active Terminator. Parametrically the UC5608 has a 5% tolerance on impedance and current compared to a 3% tolerance on the UC5601 and the sink current is increased from 20 to 200mA. The low side clamps have been removed. Custom power packages are utilized to allow normal operation at full power conditions (2 Watts).

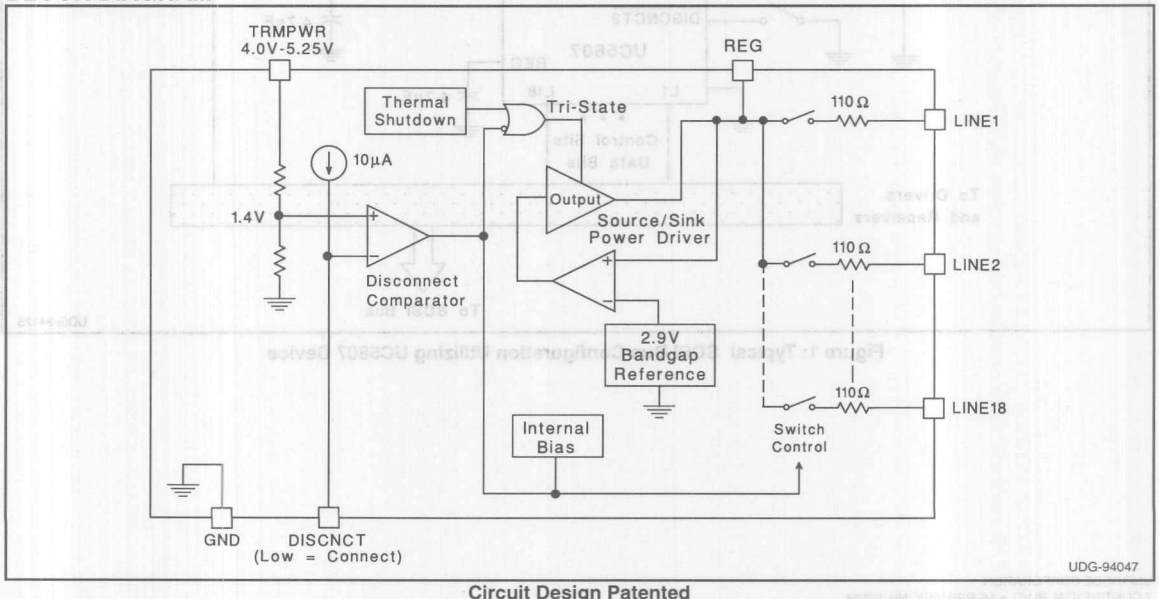
When in disconnect mode the terminator will disconnect all terminating resistors and disable the regulator, greatly reducing standby power. The output channels remain high impedance even without Termpwr applied.

Internal circuit trimming is utilized to trim the impedance to a 5% tolerance and, most importantly, to trim the output current to a 5% tolerance, as close to the max SCSI spec as possible, which maximizes noise margin in fast SCSI operation.

Other features include 4.0 to 5.25V Termpwr, thermal shutdown and current limit.

This device is offered in low thermal resistance versions of the industry standard 28 pin wide body SOIC, 28 pin wide body TSSOP, and 28 pin PLCC, as well as 24 pin DIP.

BLOCK DIAGRAM



Circuit Design Patented

3/97

ABSOLUTE MAXIMUM RATINGS

Termpwr Voltage ..... +7V
Signal Line Voltage ..... 0V to +7V
Regulator Output Current 1A
Storage Temperature ..... –65°C to +150°C
Operating Temperature ..... –55°C to +150°C
Lead Temperature (Soldering, 10 Sec.) ..... +300°C

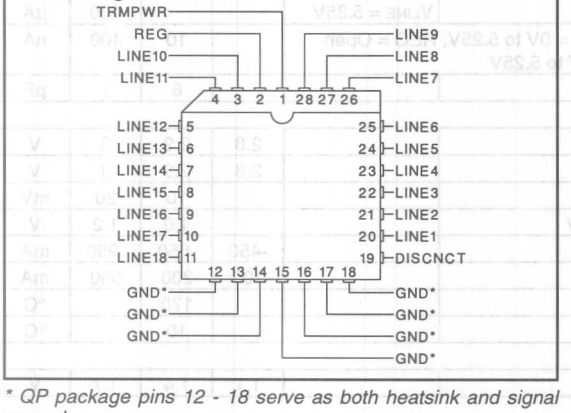
Unless otherwise specified all voltages are with respect to Ground. Currents are positive into, negative out of the specified terminal.
Consult Packaging Section of Unitrode Integrated Circuits databook for thermal limitations and considerations of packages.

RECOMMENDED OPERATING CONDITIONS

Termpwr Voltage ..... 3.8V to 5.25V
Signal Line Voltage ..... 0V to +5V
Disconnect Input Voltage ..... 0V to Termpwr

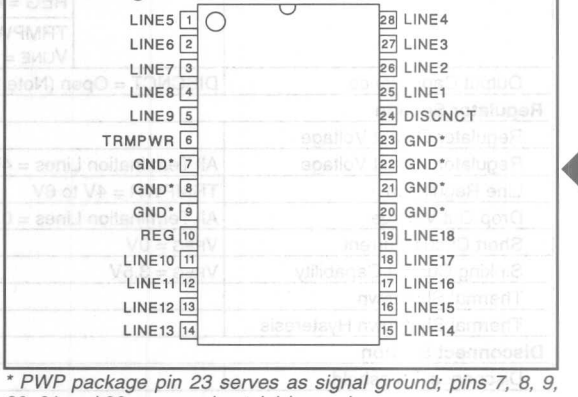
CONNECTION DIAGRAMS

PLCC-28 (Top View)
QP Package



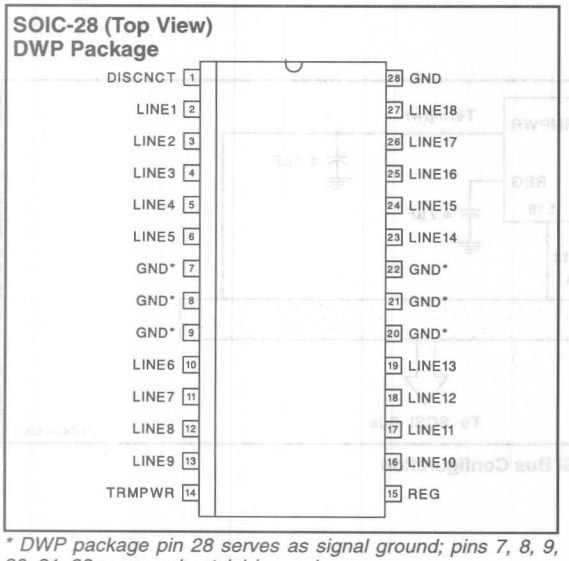
** QP package pins 12 - 18 serve as both heatsink and signal ground.*

TSSOP-28 (Top View)
PWP Package



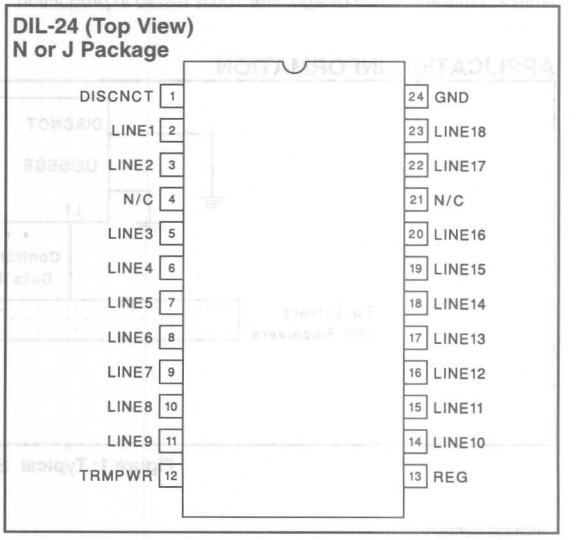
** PWP package pin 23 serves as signal ground; pins 7, 8, 9, 20, 21 and 22 serve as heatsink/ground.*

SOIC-28 (Top View)
DWP Package



** DWP package pin 28 serves as signal ground; pins 7, 8, 9, 20, 21, 22 serve as heatsink/ground.*

DIL-24 (Top View)
N or J Package



Note: Drawings are not to scale.

ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C. TRMPWR = 4.75V, DISCNCT = Ground. $T_A = T_J$.

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNITS
Supply Current Section							
Termpwr Supply Current	All termination lines = Open				17	25	mA
	All termination lines = 0.5V				400	430	mA
Power Down Mode	DISCNCT = Open				100	150	µA
Output Section (Terminator Lines)							
Terminator Impedance	ΔI_{LINE} = -5mA to -15mA			104.5	110	115.5	Ohms
Output High Voltage	V_{TRMPWR} = 4V (Note 1)			2.65	2.9	3.0	V
Max Output Current	V_{LINE} = 0.5V		T_J = 25°C	-20.3	-21.5	-22.4	mA
			0°C < T_J < 70°C	-19.8	-21.5	-22.4	mA
Max Output Current	V_{LINE} = 0.5V, TRMPWR = 4V (Note 1)		T_J = 25°C	-19.5	-21.5	-22.4	mA
			0°C < T_J < 70°C	-19.0	-21.5	-22.4	mA
	V_{LINE} = 0.2V, TRMPWR = 4V to 5.25V		0°C < T_J < 70°C	-21.6	-24.0	-25.4	mA
Output Leakage	DISCNCT = 4V	TRMPWR = 0V to 5.25V REG = 0V	V_{LINE} = 0 to 4V		10	400	nA
			V_{LINE} = 5.25V			100	µA
		TRMPWR = 0V to 5.25V, REG = Open V_{LINE} = 0V to 5.25V			10	400	nA
Output Capacitance	DISCNCT = Open (Note 2)				6	7	pF
Regulator Section							
Regulator Output Voltage				2.8	2.9	3	V
Regulator Output Voltage	All Termination Lines = 4V			2.8	2.9	3	V
Line Regulation	TRMPWR = 4V to 6V				10	20	mV
Drop Out Voltage	All Termination Lines = 0.5V				1.0	1.2	V
Short Circuit Current	V_{REG} = 0V			-450	-650	-950	mA
Sinking Current Capability	V_{REG} = 3.5V			100	200	500	mA
Thermal Shutdown					170		°C
Thermal Shutdown Hysteresis					10		°C
Disconnect Section							
Disconnect Threshold				1.1	1.4	1.7	V

Note 1: Measuring each termination line while other 17 are low (0.5V).
Note 2: Guaranteed by design. Not 100% tested in production.

APPLICATION INFORMATION

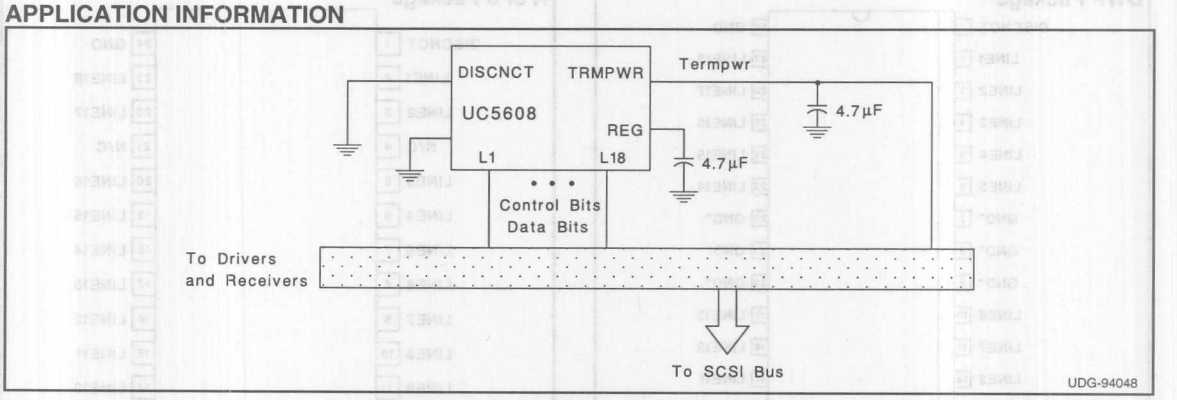


Figure 1: Typical SCSI Bus Configuration

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UNITRODE

18-Line Low Capacitance SCSI Active Terminator

FEATURES

- Reverse Disconnect
- Complies with SCSI, SCSI-2 and SPI-2 Standards
- 6pF Channel Capacitance during Disconnect
- 100µA Supply Current in Disconnect Mode
- Meets SCSI Hot Plugging Capability
- –650mA Sourcing Current for Termination
- +200mA Sinking Current for Active Negation
- Provides Active Termination for 18 Lines
- Logic Command Disconnects all Termination Lines
- Trimmed Termination Current to 5%
- Trimmed Impedance to 5%
- Current Limit and Thermal Shutdown Protection

DESCRIPTION

The UC5609 provides 18 lines of active termination for a SCSI (Small Computer Systems Interface) parallel bus. The SCSI standard recommends active termination at both ends of the bus cable.

The UC5609 is pin-for-pin compatible with its predecessors, the UC5601, UC5602 and UC5608 - 18 Line Active Terminators, except for the reverse disconnect sense. Parametrically the UC5609 has a 5% tolerance on impedance and current compared to a 3% tolerance on the UC5601 and the sink current is increased from 20 to 200mA. The low side clamps have been removed. Custom power packages are utilized to allow normal operation at full power conditions (2 Watts).

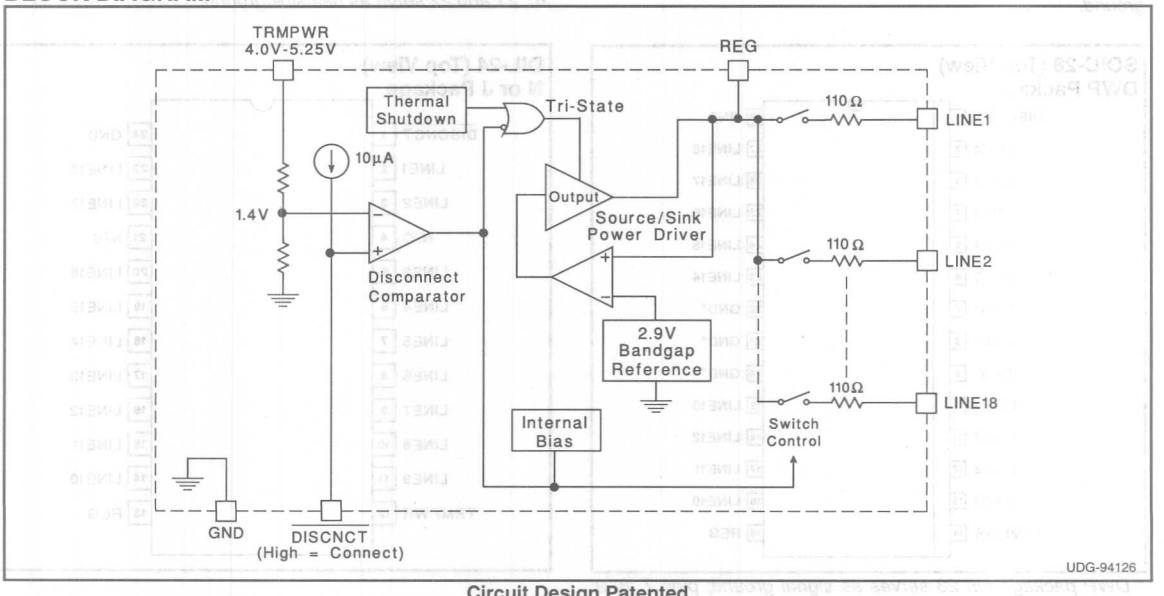
When in disconnect mode the terminator will disconnect all terminating resistors and disable the regulator, greatly reducing standby power. The output channels remain high impedance even without Termpwr applied.

Internal circuit trimming is utilized to trim the impedance to a 5% tolerance and, most importantly, to trim the output current to a 5% tolerance, as close to the max SCSI spec as possible, which maximizes noise margin in fast SCSI operation.

Other features include 4.0 to 5.25V Termpwr, thermal shutdown and current limit.

This device is offered in low thermal resistance versions of the industry standard 28 pin wide body SOIC, 28 pin wide body TSSOP, and 28 pin PLCC, as well as 24 pin DIP.

BLOCK DIAGRAM



Circuit Design Patented

4/97

ABSOLUTE MAXIMUM RATINGS

Termpwr Voltage ..... +7V
Signal Line Voltage..... 0V to +7V
Regulator Output Current 1A
Storage Temperature ..... –65°C to +150°C
Operating Temperature ..... –55°C to +150°C
Lead Temperature (Soldering, 10 Sec.)..... +300°C

Unless otherwise specified all voltages are with respect to Ground. Currents are positive into, negative out of the specified terminal.

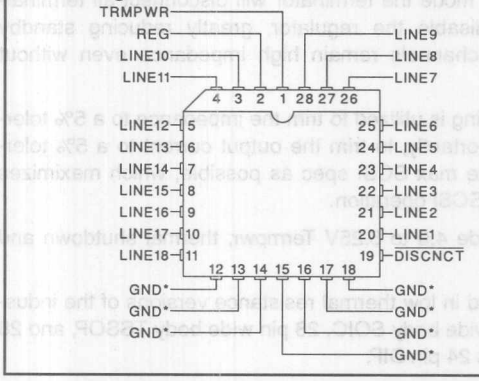
Consult Packaging Section of Unitrode Integrated Circuits databook for thermal limitations and considerations of packages.

RECOMMENDED OPERATING CONDITIONS

Termpwr Voltage ..... 3.8V to 5.25V
Signal Line Voltage..... 0V to +5V
Disconnect Input Voltage ..... 0V to Termpwr

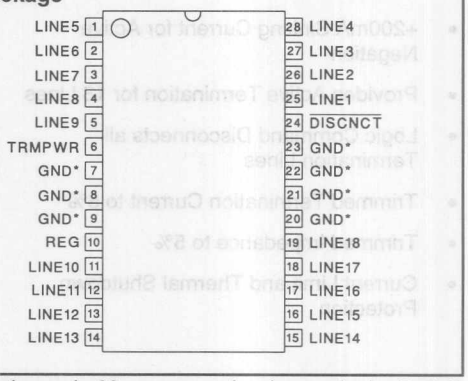
CONNECTION DIAGRAMS

PLCC-28 (Top View)
QP Package



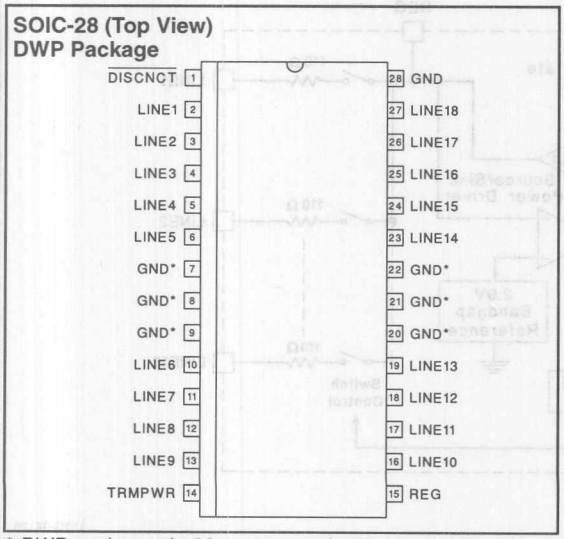
** QP package pins 12 - 18 serve as both heatsink and signal ground.*

TSSOP-28 (Top View)
PWP Package



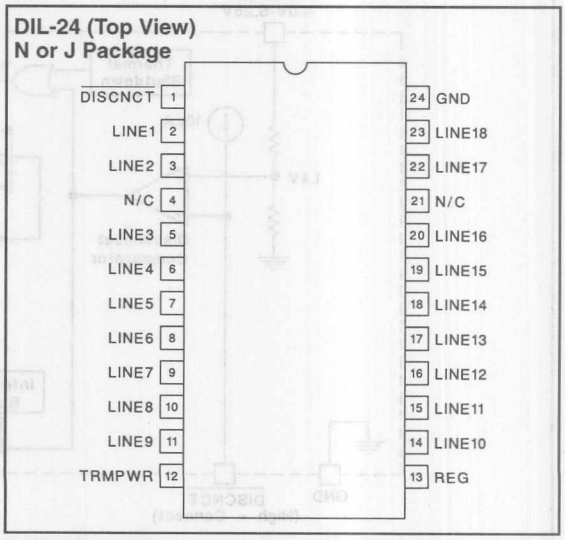
** PWP package pin 23 serves as signal ground; pins 7, 8, 9, 20, 21 and 22 serve as heatsink/ground.*

SOIC-28 (Top View)
DWP Package



** DWP package pin 28 serves as signal ground; pins 7, 8, 9, 20, 21, 22 serve as heatsink/ground.*

DIL-24 (Top View)
N or J Package



Note: Drawings are not to scale.

ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C. TRMPWR = 4.75V, $\overline{\text{DISCNCT}}$ = 2.4V. $T_A = T_J$.

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNITS
Supply Current Section							
Termpwr Supply Current	All termination lines = Open				17	25	mA
	All termination lines = 0.5V				400	430	mA
Power Down Mode	DISCNCT = GND				100	150	µA
Output Section (Terminator Lines)							
Terminator Impedance	ΔI_{LINE} = -5mA to -15mA			104.5	110	115.5	Ω
Output High Voltage	V_{TRMPWR} = 4V (Note 1)			2.65	2.9	3.0	V
Max Output Current	V_{LINE} = 0.5V		T_J = 25°C	-20.3	-21.5	-22.4	mA
			0°C < T_J < 70°C	-19.8	-21.5	-22.4	mA
Max Output Current	V_{LINE} = 0.5V, TRMPWR = 4V (Note 1)		T_J = 25°C	-19.5	-21.5	-22.4	mA
			0°C < T_J < 70°C	-19.0	-21.5	-22.4	mA
	V_{LINE} = 0.2V, TRMPWR = 4V to 5.25V		0°C < T_J < 70°C	-21.6	-24.0	-25.4	mA
Output Leakage	$\overline{\text{DISCNCT}}$ = GND	TRMPWR = 0V to 5.25V REG = 0V	V_{LINE} = 0 to 4V		10	400	nA
			V_{LINE} = 5.25V			100	µA
		TRMPWR = 0V to 5.25V, REG = Open V_{LINE} = 0V to 5.25V			10	400	nA
Output Capacitance	$\overline{\text{DISCNCT}}$ = GND (Note 2)				6	7	pF
Regulator Section							
Regulator Output Voltage				2.8	2.9	3	V
Regulator Output Voltage	All Termination Lines = 4V			2.8	2.9	3	V
Line Regulation	TRMPWR = 4V to 6V				10	20	mV
Drop Out Voltage	All Termination Lines = 0.5V				1.0	1.2	V
Short Circuit Current	V_{REG} = 0V			-450	-650	-950	mA
Sinking Current Capability	V_{REG} = 3.5V			100	200	500	mA
Thermal Shutdown					170		°C
Thermal Shutdown Hysteresis					10		°C
Disconnect Section							
Disconnect Threshold				1.1	1.4	1.7	V

Note 1: Measuring each termination line while other 17 are low (0.5V).
Note 2: Guaranteed by design. Not 100% tested in production.

APPLICATION INFORMATION

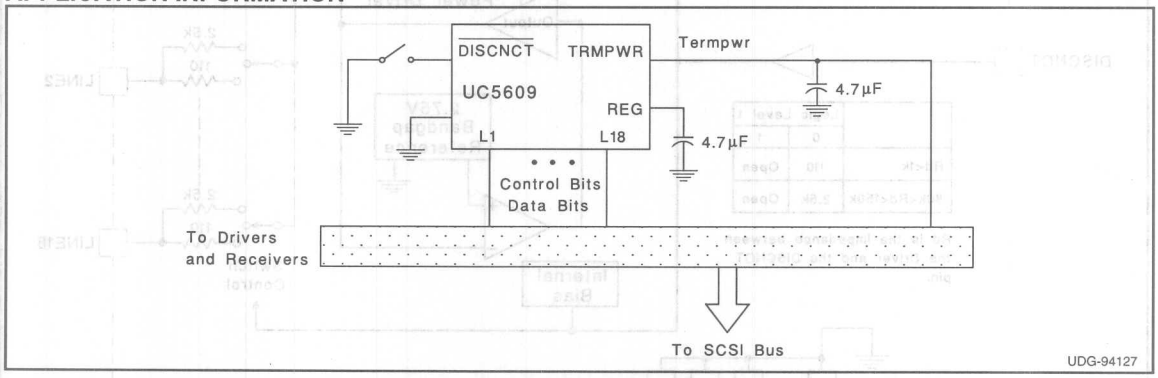


Figure 1: Typical SCSI Bus Configuration

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

UNITRODE

18-Line 3-5 Volt Low Capacitance SCSI Active Terminator

FEATURES

- Complies with SCSI, SCSI-2, SCSI-3 and FAST-20 (Ultra) Standards
- 2.75V to 7V Operation
- 1.8pF Channel Capacitance during Disconnect
- 0.5µA Supply Current in Disconnect Mode
- 110 Ohm/2.5k Programmable Termination
- Completely Meets SCSI Hot Plugging
- -650mA Sourcing Current for Termination
- +400mA Sinking Current for Active Negation Drivers
- Trimmed Termination Current to 4%
- Trimmed Impedance to 7%
- Current Limit and Thermal Shutdown Protection

DESCRIPTION

The UCC5610 provides 18 lines of active termination for a SCSI (Small Computer Systems Interface) parallel bus. The SCSI standard recommends active termination at both ends of the cable.

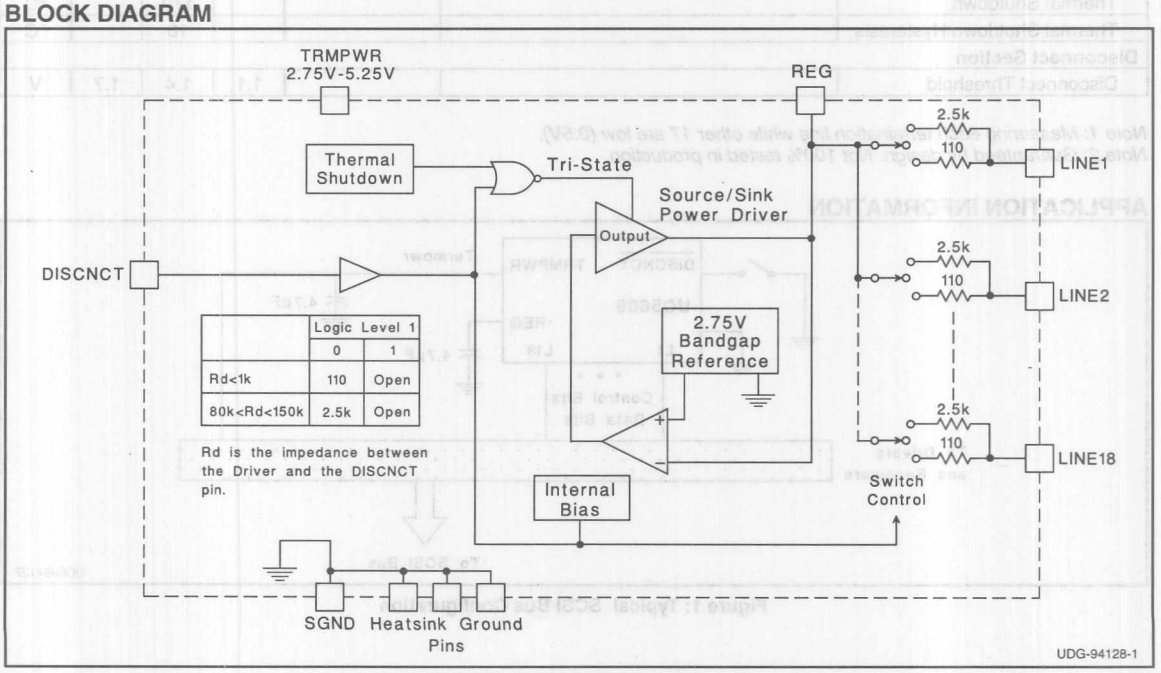
The UCC5610 is ideal for high performance 3.3V SCSI systems. The key features contributing to such low operating voltage are the 0.1V drop out regulator and the 2.75V reference. The reduced reference voltage was necessary to accommodate the lower termination current dictated in the SCSI-3 specification. During disconnect the supply current is typically only 0.5µA, which makes the IC attractive for battery powered systems.

The UCC5610 is designed with an ultra low channel capacitance of 1.8pF, which eliminates effects on signal integrity from disconnected terminators at interim points on the bus.

The UCC5610 can be programmed for either a 110 ohm or 2.5k ohm termination. The 110 ohm termination is used for standard SCSI bus lengths and the 2.5k ohm termination is typically used in short bus applications. When driving the TTL compatible DISCNCT pin directly, the 110 ohm termination is connected when the DISCNCT pin is driven low, and disconnected when driven high. When the DISCNCT pin is driven through an impedance between 80k and 150k, the 2.5k ohm termination is connected when the DISCNCT pin is driven low, and disconnected when driven high.

continued

BLOCK DIAGRAM



Circuit Design Patented

Description Continued

The power amplifier output stage allows the UCC5610 to source full termination current and sink active negation current when all termination lines are actively negated.

The UCC5610 is pin for pin compatible with Unitrode's other 18 line SCSI terminators, allowing lower capacitance and lower voltage upgrades to existing systems. The UCC5610, as with all Unitrode terminators, is completely hot pluggable and appears as high impedance at the terminating channels with V_{TRMPWR} = 0V or open.

Internal circuit trimming is utilized, first to trim the 110 ohm termination impedance to a 7% tolerance, and then most importantly, to trim the output current to a 4% tolerance, as close to the max SCSI-3 spec as possible, which maximizes noise margin in FAST-20 SCSI operation.

Other features include thermal shutdown and current limit.

This device is offered in low thermal resistance versions of the industry standard 28 pin wide body SOIC, 24 pin wide body DIP and 28 pin PLCC.

ABSOLUTE MAXIMUM RATINGS

Termpwr Voltage ..... +7V
Signal Line Voltage ..... 0V to +7V
Regulator Output Current ..... Self-regulating
Storage Temperature ..... –65°C to +150°C
Operating Temperature ..... –55°C to +150°C
Lead Temperature (Soldering, 10 Sec.) ..... +300°C

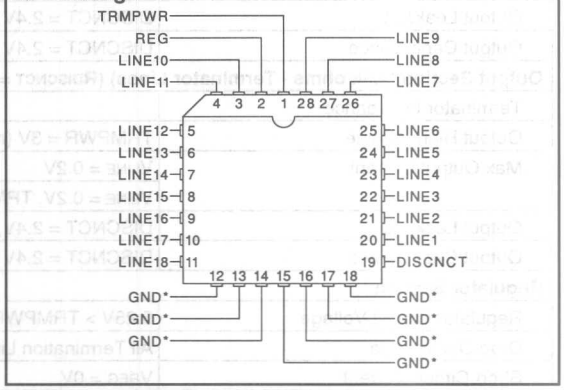
Unless otherwise specified all voltages are with respect to Ground. Currents are positive into, negative out of the specified terminal.
Consult Packaging Section of Unitrode Integrated Circuits databook for thermal limitations and considerations of packages.

RECOMMENDED OPERATING CONDITIONS

Termpwr Voltage ..... 2.75V to 5.25V
Signal Line Voltage ..... 0V to +5V
Disconnect Input Voltage ..... 0V to Termpwr

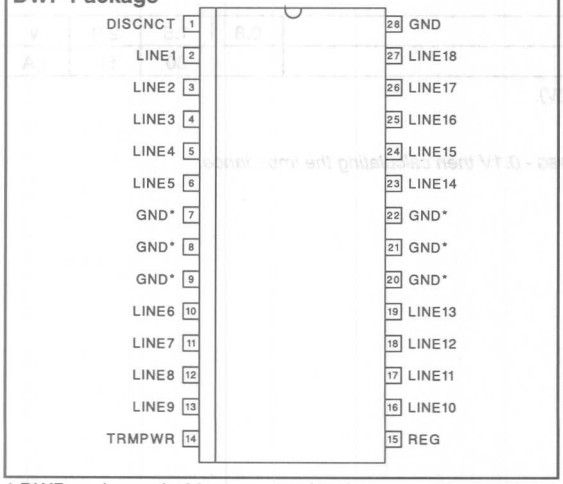
CONNECTION DIAGRAMS

PLCC-28 (Top View)
QP Package



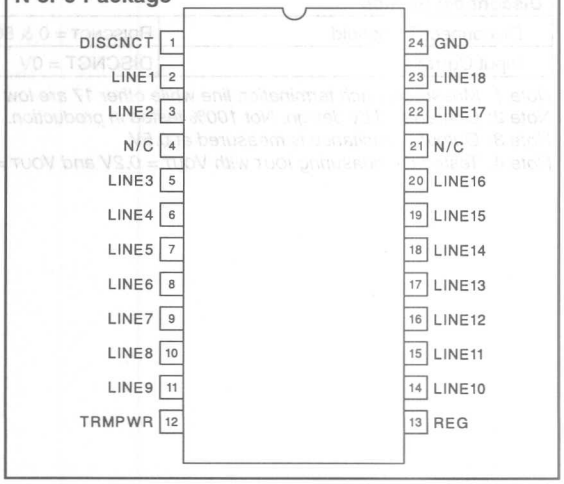
** QP package pins 12 - 18 serve as both heatsink and signal ground.*

SOIC-28 (Top View)
DWP Package



** DWP package pin 28 serves as signal ground; pins 7, 8, 9, 20, 21, 22 serve as heatsink/ground.*

DIL-24 (Top View)
N or J Package



Note: Drawings are not to scale.

ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C. TRMPWR = 3.3V, DISCNCT = 0V, $R_{DISCNCT}$= 0 ohms. T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current Section					
Termpwr Supply Current	All termination lines = Open		1	2	mA
	All termination lines = 0.2V		415	455	mA
Power Down Mode	DISCNCT = Termpwr		0.5	5	µA
Output Section (110 ohms - Terminator Lines)					
Terminator Impedance	(Note 4)	102.3	110	117.7	Ohms
Output High Voltage	(Note 1)	2.5	2.7	3.0	V
Max Output Current	V_{LINE} = 0.2V, T_J = 25°C	–22.1	–23	–24	mA
	V_{LINE} = 0.2V	–21	–23	–24	mA
	V_{LINE} = 0.2V, TRMPWR = 3V, T_J = 25°C (Note 1)	–20.2	–23	–24	mA
	V_{LINE} = 0.2V, TRMPWR = 3V (Note 1)	–19	–23	–24	mA
	V_{LINE} = 0.5V			–22.4	mA
Output Leakage	DISCNCT = 2.4V, TRMPWR = 0V to 5.25V		10	400	nA
Output Capacitance	DISCNCT = 2.4V (Note 2, 3) (DWP Package)		1.8	2.5	pF
Output Section (2.5k ohms - Terminator Lines) ($R_{DISCNCT}$ = 80k ohms)					
Terminator Impedance		2	2.5	3	kΩ
Output High Voltage	TRMPWR = 3V (Note 1)	2.5	2.7	3.0	V
Max Output Current	V_{LINE} = 0.2V	–0.7	–1	–1.4	mA
	V_{LINE} = 0.2V, TRMPWR = 3V (Note 1)	–0.6	–1	–1.5	mA
Output Leakage	DISCNCT = 2.4V, TRMPWR = 0 to 5.25V		10	400	nA
Output Capacitance	DISCNCT = 2.4V (Note 2, 3) (DWP Package)		1.8	2.5	pF
Regulator Section					
Regulator Output Voltage	5.25V > TRMPWR > 3V	2.5	2.7	3.0	V
Drop Out Voltage	All Termination Lines = 0.2V		0.1	0.2	V
Short Circuit Current	V_{REG} = 0V	–450	–650	–800	mA
Sinking Current Capability	V_{REG} = 3V	200	400	800	mA
Thermal Shutdown	(Note 2)		170		°C
Thermal Shutdown Hysteresis	(Note 2)		10		°C
Disconnect Section					
Disconnect Threshold	$R_{DISCNCT}$ = 0 & 80k	0.8	1.5	2.0	V
Input Current	DISCNCT = 0V		30	50	µA

Note 1: Measuring each termination line while other 17 are low (0.2V).
Note 2: Guaranteed by design. Not 100% tested in production.
Note 3: Output capacitance is measured at 0.5V.
Note 4: Tested by measuring I_{OUT} with V_{OUT} = 0.2V and V_{OUT} = V_{REG} - 0.1V then calculating the impedance.

APPLICATION INFORMATION

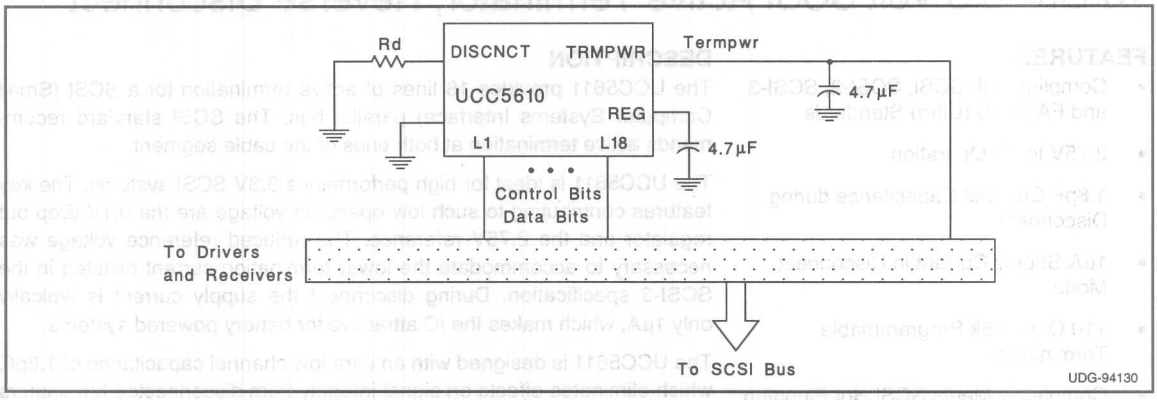


Figure 1: Typical SCSI Bus Configurations Utilizing A UCC5610 Device

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

UNITRODE

18-Line 3-5 Volt SCSI Active Terminator, Reverse Disconnect

FEATURES

- Complies with SCSI, SCSI-2, SCSI-3 and FAST-20 (Ultra) Standards
- 2.75V to 7V Operation
- 1.8pF Channel Capacitance during Disconnect
- 1µA Supply Current in Disconnect Mode
- 110 Ohm/2.5k Programmable Termination
- Completely Meets SCSI Hot Plugging
- –650mA Sourcing Current for Termination
- +400mA Sinking Current for Active Negation Drivers
- Trimmed Termination Current to 4%
- Trimmed Impedance to 7%
- Current Limit and Thermal Shutdown Protection

DESCRIPTION

The UCC5611 provides 18 lines of active termination for a SCSI (Small Computer Systems Interface) parallel bus. The SCSI standard recommends active termination at both ends of the cable segment.

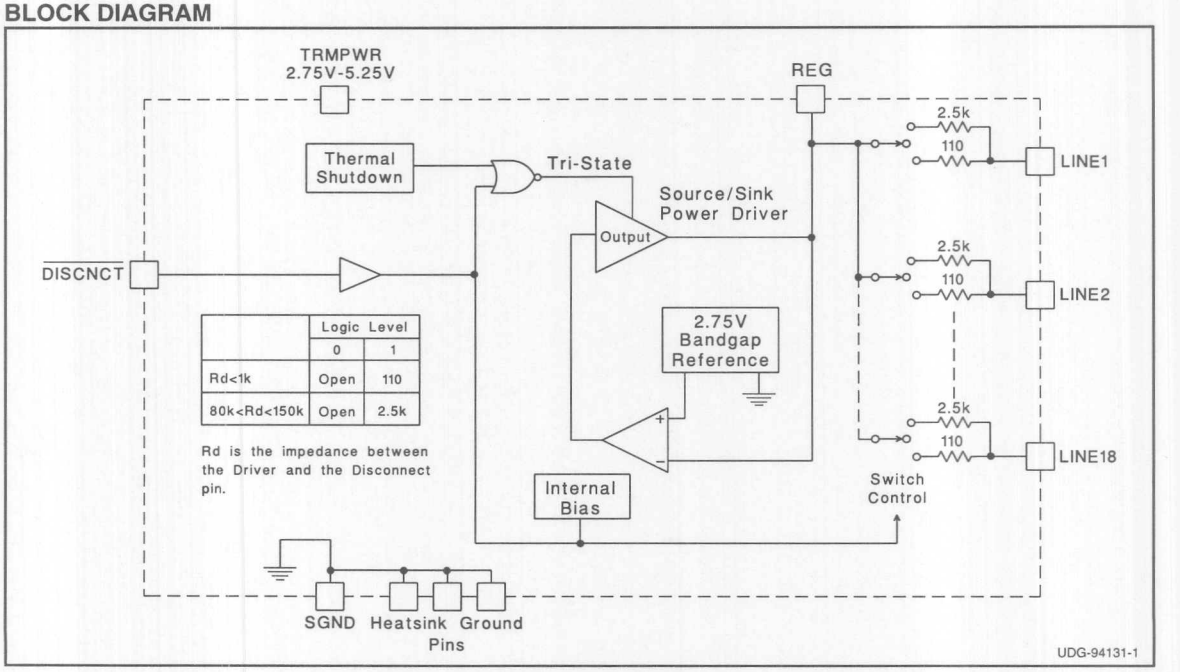
The UCC5611 is ideal for high performance 3.3V SCSI systems. The key features contributing to such low operating voltage are the 0.1V drop out regulator and the 2.75V reference. The reduced reference voltage was necessary to accommodate the lower termination current dictated in the SCSI-3 specification. During disconnect the supply current is typically only 1µA, which makes the IC attractive for battery powered systems.

The UCC5611 is designed with an ultra low channel capacitance of 1.8pF, which eliminates effects on signal integrity from disconnected terminators at interim points on the bus.

The UCC5611 can be programmed for either a 110 ohm or 2.5k ohm termination. The 110 ohm termination is used for standard SCSI bus lengths and the 2.5k ohm termination is typically used in short bus applications. When driving the TTL compatible $\overline{\text{DISCNCT}}$ pin directly, the 110 ohm termination is connected when the $\overline{\text{DISCNCT}}$ pin is driven high, and disconnected when low. When the $\overline{\text{DISCNCT}}$ pin is driven through an impedance between 80k and 150k, the 2.5k ohm termination is connected when the $\overline{\text{DISCNCT}}$ pin is driven high, and disconnected when driven low.

continued

BLOCK DIAGRAM



	Logic Level	
	0	1
Rd<1k	Open	110
80k<Rd<150k	Open	2.5k

Rd is the impedance between the Driver and the Disconnect pin.

Circuit Design Patented

Description Continued

The power amplifier output stage allows the UCC5611 to source full termination current and sink active negation current when all termination lines are actively negated.

The UCC5611 is pin for pin compatible with Unitrode's other 18 line SCSI terminators, except that $\overline{\text{DISCNCT}}$ is now active low, allowing lower capacitance and lower voltage upgrades to existing systems. The UCC5611, as with all Unitrode terminators, is completely hot pluggable and appears as high impedance at the terminating channels with V_{TRMPWR} = 0V or open.

Internal circuit trimming is utilized, first to trim the 110 ohm termination impedance to a 7% tolerance, and then most importantly, to trim the output current to a 4% tolerance, as close to the max SCSI-3 spec as possible, which maximizes noise margin in FAST-20 SCSI operation.

Other features include thermal shutdown and current limit.

This device is offered in low thermal resistance versions of the industry standard 28 pin wide body SOIC, 24 pin wide body DIP and 28 pin PLCC.

ABSOLUTE MAXIMUM RATINGS

Termpwr Voltage ..... +7V
Signal Line Voltage ..... 0V to +7V
Regulator Output Current ..... Self-regulating
Storage Temperature ..... –65°C to +150°C
Operating Temperature ..... –55°C to +150°C
Lead Temperature (Soldering, 10 Sec.) ..... +300°C

Unless otherwise specified all voltages are with respect to Ground. Currents are positive into, negative out of the specified terminal.

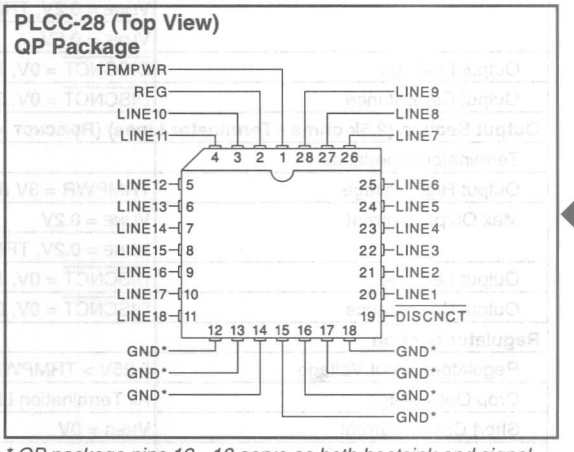
Consult Packaging Section of Unitrode Integrated Circuits databook for thermal limitations and considerations of packages.

RECOMMENDED OPERATING CONDITIONS

Termpwr Voltage ..... 2.75V to 5.25V
Signal Line Voltage ..... 0V to +5V
Disconnect Input Voltage ..... 0V to Termpwr

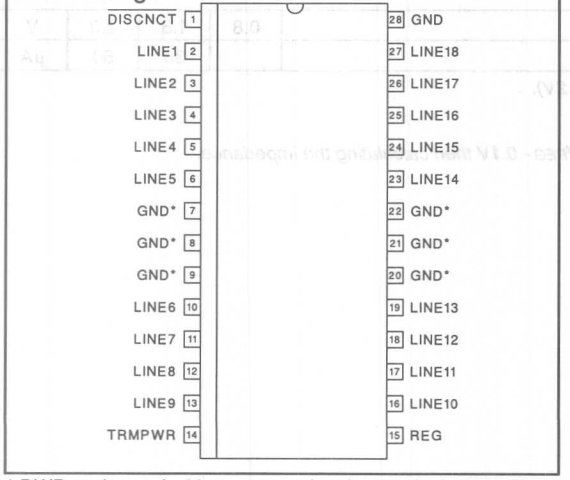
CONNECTION DIAGRAMS

PLCC-28 (Top View)
QP Package



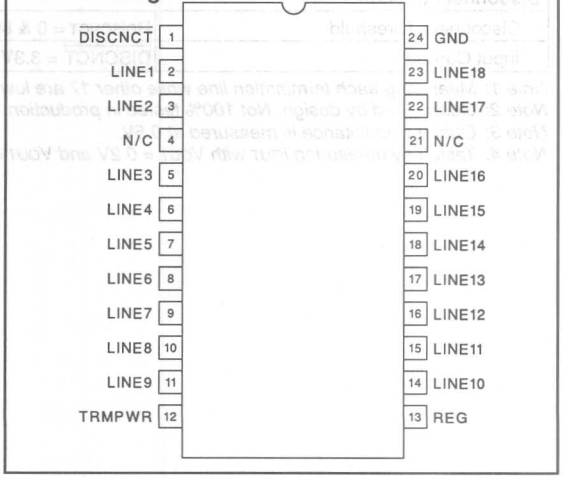
** QP package pins 12 - 18 serve as both heatsink and signal ground.*

SOIC-28 (Top View)
DWP Package



** DWP package pin 28 serves as signal ground; pins 7, 8, 9, 20, 21, 22 serve as heatsink/ground.*

DIL-24 (Top View)
N or J Package



Note: Drawings are not to scale.

ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C. TRMPWR = 3.3V, $\overline{DISCNCT}$ = 3.3V, $R_{DISCNCT}$ = 0 ohms. T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current Section					
Termpwr Supply Current	All termination lines = Open		1	2	mA
	All termination lines = 0.2V		415	435	mA
Power Down Mode	$\overline{DISCNCT}$ = 0V		0.5	5	µA
Output Section (110 ohms - Terminator Lines)					
Terminator Impedance	(Note 4)	102.3	110	117.7	Ohms
Output High Voltage	TRMPWR = 3V (Note 1)	2.5	2.7	3.0	V
Max Output Current	V_{LINE} = 0.2V, T_J = 25°C	–22.1	–23	–24	mA
	V_{LINE} = 0.2V	–21	–23	–24	mA
	V_{LINE} = 0.2V, TRMPWR = 3V, T_J = 25°C (Note 1)	–20.2	–23	–24	mA
	V_{LINE} = 0.2V, TRMPWR = 3V (Note 1)	–19	–23	–24	mA
	V_{LINE} = 0.5V			–22.4	mA
Output Leakage	$\overline{DISCNCT}$ = 0V, TRMPWR = 0V to 5.25V		10	400	nA
Output Capacitance	$\overline{DISCNCT}$ = 0V, DWP Package (Note 2, 3)		1.8	2.5	pF
Output Section (2.5k ohms - Terminator Lines) ($R_{DISCNCT}$ = 80k ohms)					
Terminator Impedance		2	2.5	3	kΩ
Output High Voltage	TRMPWR = 3V (Note 1)	2.5	2.7	3.0	V
Max Output Current	V_{LINE} = 0.2V	–0.7	–1	–1.4	mA
	V_{LINE} = 0.2V, TRMPWR = 3V (Note 1)	–0.6	–1	–1.5	mA
Output Leakage	$\overline{DISCNCT}$ = 0V, TRMPWR = 0 to 5.25V		10	400	nA
Output Capacitance	$\overline{DISCNCT}$ = 0V, DWP Package (Note 2, 3)		1.8	2.5	pF
Regulator Section					
Regulator Output Voltage	5.25V > TRMPWR > 3V	2.5	2.7	3.0	V
Drop Out Voltage	All Termination Lines = 0.2V		0.1	0.2	V
Short Circuit Current	V_{REG} = 0V	–450	–650	–800	mA
Sinking Current Capability	V_{REG} = 3V	200	400	800	mA
Thermal Shutdown	(Note 2)		170		°C
Thermal Shutdown Hysteresis	(Note 2)		10		°C
Disconnect Section					
Disconnect Threshold	$R_{DISCNCT}$ = 0 & 80k	0.8	1.5	2.0	V
Input Current	$\overline{DISCNCT}$ = 3.3V		30	50	µA

Note 1: Measuring each termination line while other 17 are low (0.2V).
Note 2: Guaranteed by design. Not 100% tested in production.
Note 3: Output Capacitance is measured at 0.5V.
Note 4: Tested by measuring I_{OUT} with V_{OUT} = 0.2V and V_{OUT} = V_{REG} - 0.1V then calculating the impedance.

APPLICATION INFORMATION

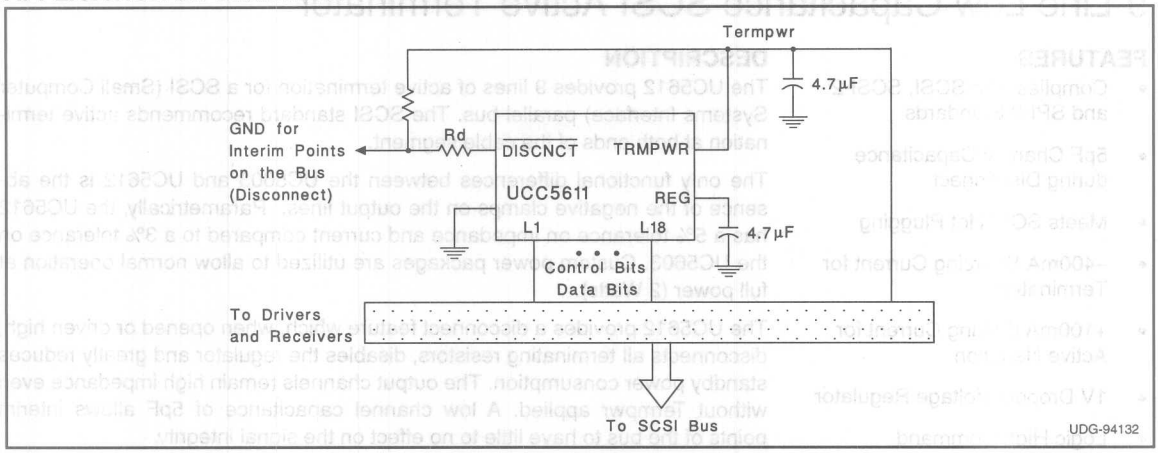


Figure 1: Typical SCSI Bus Configurations Utilizing A UCC5611 Device

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

UNITRODE

9-Line Low Capacitance SCSI Active Terminator

FEATURES

- Complies with SCSI, SCSI-2 and SPI-2 Standards
- 5pF Channel Capacitance during Disconnect
- Meets SCSI Hot Plugging
- –400mA Sourcing Current for Termination
- +100mA Sinking Current for Active Negation
- 1V Dropout Voltage Regulator
- Logic High Command Disconnects all Termination Lines
- 100µA Supply Current in Disconnect Mode
- Trimmed Termination Current to 5%
- Trimmed Impedance to 5%
- Low Thermal Resistance Surface Mount Packages

DESCRIPTION

The UC5612 provides 9 lines of active termination for a SCSI (Small Computer Systems Interface) parallel bus. The SCSI standard recommends active termination at both ends of the cable segment.

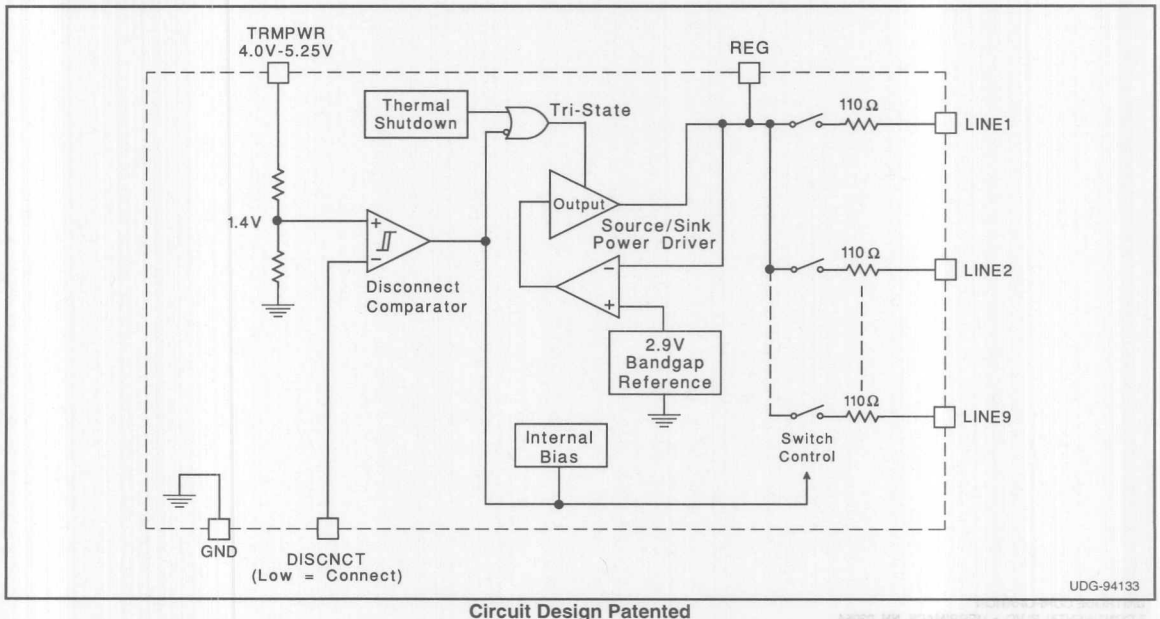
The only functional differences between the UC5603 and UC5612 is the absence of the negative clamps on the output lines. Parametrically, the UC5612 has a 5% tolerance on impedance and current compared to a 3% tolerance on the UC5603. Custom power packages are utilized to allow normal operation at full power (2 Watts).

The UC5612 provides a disconnect feature which, when opened or driven high, disconnects all terminating resistors, disables the regulator and greatly reduces standby power consumption. The output channels remain high impedance even without Termpwr applied. A low channel capacitance of 5pF allows interim points of the bus to have little to no effect on the signal integrity.

Internal circuit trimming is utilized, first to trim the impedance to a 5% tolerance, and then most importantly, to trim the output current to a 5% tolerance, as close to the maximum SCSI specification as possible. This maximizes the noise margin in fast SCSI operation. Other features include thermal shutdown and current limit.

This device is offered in low thermal resistance versions of the industry standard 16 pin narrow body SOIC, 16 pin ZIP (zig-zag in line package) and 24 pin TSSOP.

BLOCK DIAGRAM



Circuit Design Patented

3/97

ABSOLUTE MAXIMUM RATINGS

Termpwr Voltage ..... +7V
Signal Line Voltage..... 0V to +7V
Regulator Output Current..... 0.6A
Storage Temperature ..... –65°C to +150°C
Operating Temperature ..... –55°C to +150°C
Lead Temperature (Soldering, 10 Sec.)..... +300°C

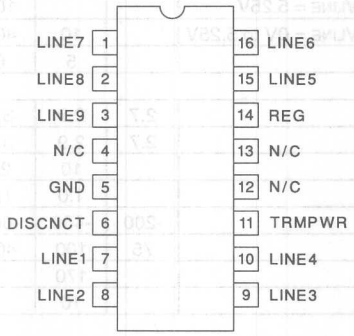
Unless otherwise specified all voltages are with respect to Ground. Currents are positive into, negative out of the specified terminal.
Consult Packaging Section of Unitrode Integrated Circuits databook for thermal limitations and considerations of packages.

RECOMMENDED OPERATING CONDITIONS

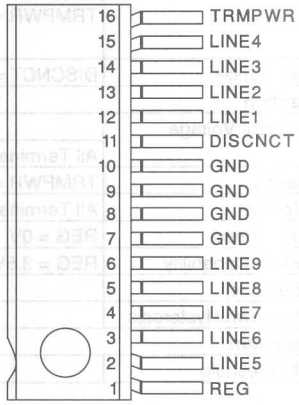
Termpwr Voltage ..... 3.8V to 5.25V
Signal Line Voltage..... 0V to +5V
Disconnect Input Voltage ..... 0V to Termpwr

CONNECTION DIAGRAMS

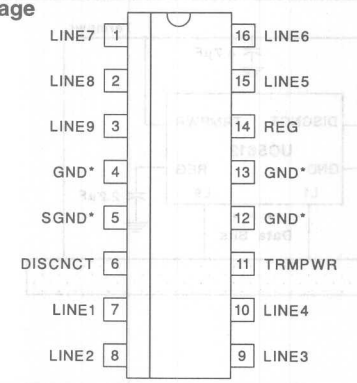
DIL-16 (Top View)
N or J Package



ZIP-16 (Top View)
Z Package

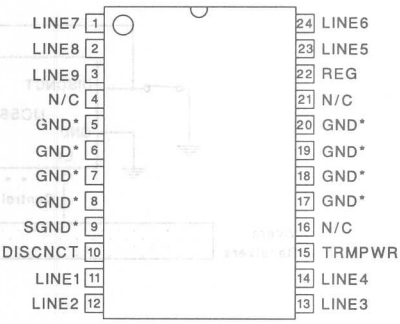


SOIC-16 (Top View)
DP Package



** DP package pin 5 serves as signal ground; pins 4, 12, 13 serve as heatsink/ground.*

TSSOP-24 (Top View)
PWP Package



** PWP package pin 9 serves as signal ground; pins 5, 6, 7, 8, 17, 18, 19, and 20 serve as heatsink/ground.*

Note: Drawings are not to scale.

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C. TRMPWR = 4.75V, DISCNCT = 0V, T_A = T_J.

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNITS
Supply Current Section							
Termpwr Supply Current	All termination lines = Open				17	23	mA
	All termination lines = 0.5V				200	225	mA
Power Down Mode	DISCNCT = Open				100	150	µA
Output Section (Termination Lines)							
Terminator Impedance	ΔI_{LINE} = -5mA to -15mA			104.5	110	115.5	Ohms
Output High Voltage				2.65	2.9	3.1	V
Max Output Current	V_{LINE} = 0.5V		T_J = 25°C	-20.3	-21.5	-22.4	mA
			0°C < T_J < 70°C	-19.8	-21.5	-22.4	mA
Max Output Current	V_{LINE} = 0.5V, TRMPWR = 4V (Note 1)		T_J = 25°C	-19.5	-21.5	-22.4	mA
			0°C < T_J < 70°C	-19.0	-21.5	-22.4	mA
	V_{LINE} = 0.2V, TRMPWR = 4V to 5.25V		0°C < T_J < 70°C	-21.6	-24.0	-25.4	mA
Output Leakage	DISCNCT = 4V TRMPWR = 0V to 5.25V	REG = 0V	V_{LINE} = 0 to 4V		10	400	nA
			V_{LINE} = 5.25V			100	µA
		REG = Open	V_{LINE} = 0V to 5.25V		10	400	nA
Output Capacitance	DISCNCT = Open (Note 2) (DP Package)				5	6	pF
Regulator Section							
Regulator Output Voltage				2.7	2.9	3.1	V
	All Termination Lines = 4V			2.7	2.9	3.1	V
Line Regulation	TRMPWR = 4V to 6V				10	20	mV
Drop Out Voltage	All Termination Lines = 0.5V				1.0	1.2	V
Short Circuit Current	REG = 0V			-200	-400	-600	mA
Sinking Current Capability	REG = 3.5V			75	100	400	mA
Thermal Shutdown					170		°C
Thermal Shutdown Hysteresis					10		°C
Disconnect Section							
Disconnect Threshold				1.1	1.4	1.7	V

Note 1: Measuring each termination line while other 8 are low.
Note 2: Guaranteed by design. Not 100% tested in production.

APPLICATION INFORMATION

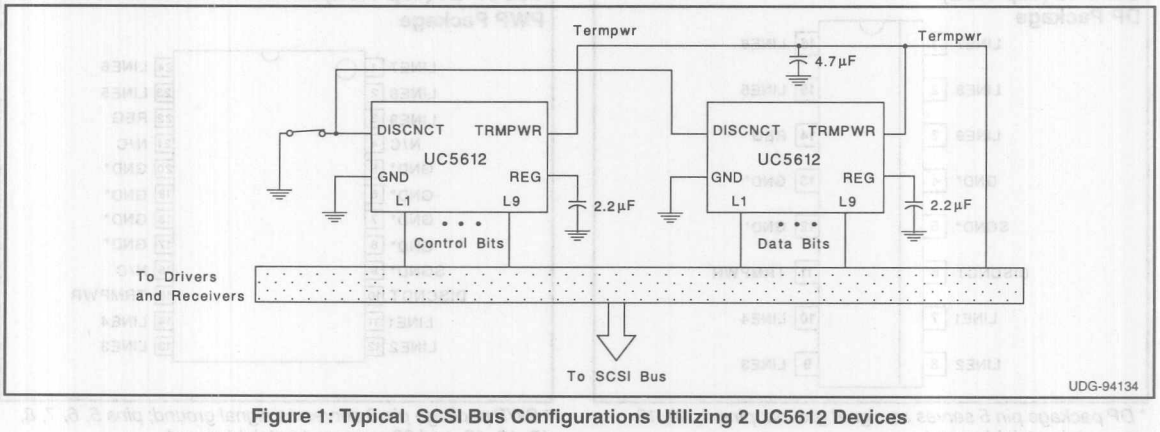


Figure 1: Typical SCSI Bus Configurations Utilizing 2 UC5612 Devices

APPLICATION INFORMATION (cont.)

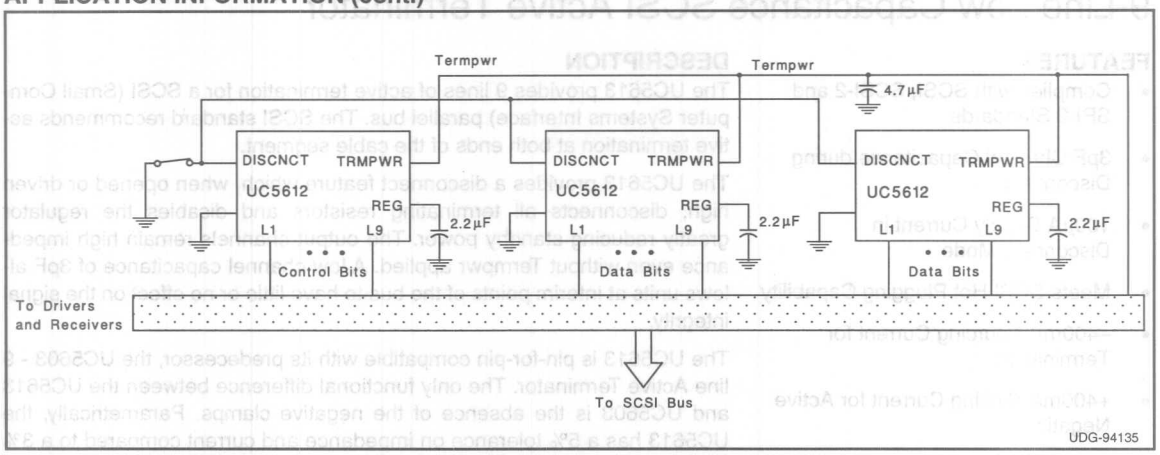
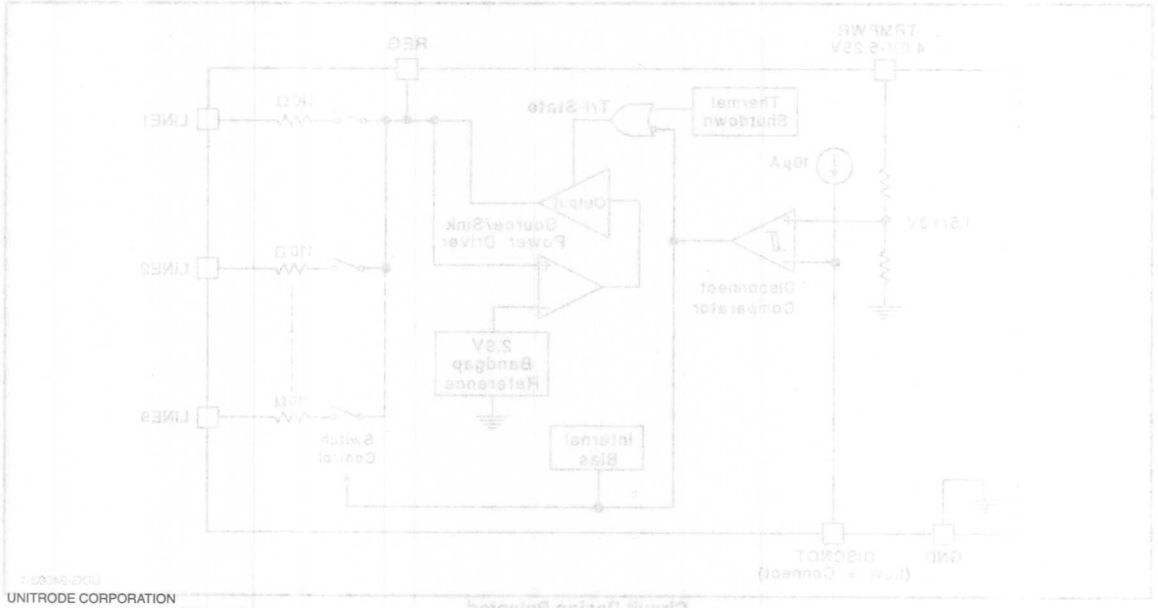


Figure 2: Typical Wide SCSI Bus Configurations Utilizing 3 UC5612 Devices.



UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

UNITRODE

9-Line Low Capacitance SCSI Active Terminator

FEATURES

- Complies with SCSI, SCSI-2 and SPI-2 Standards
- 3pF Channel Capacitance during Disconnect
- 100µA Supply Current in Disconnect Mode
- Meets SCSI Hot Plugging Capability
- –400mA Sourcing Current for Termination
- +400mA Sinking Current for Active Negation
- Logic Command Disconnects all Termination Lines
- Trimmed Termination Current to 5%
- Trimmed Impedance to 5%
- Current Limit and Thermal Shutdown Protection

DESCRIPTION

The UC5613 provides 9 lines of active termination for a SCSI (Small Computer Systems Interface) parallel bus. The SCSI standard recommends active termination at both ends of the cable segment.

The UC5613 provides a disconnect feature which, when opened or driven high, disconnects all terminating resistors and disables the regulator greatly reducing standby power. The output channels remain high impedance even without Termpwr applied. A low channel capacitance of 3pF allows units at interim points of the bus to have little or no effect on the signal integrity.

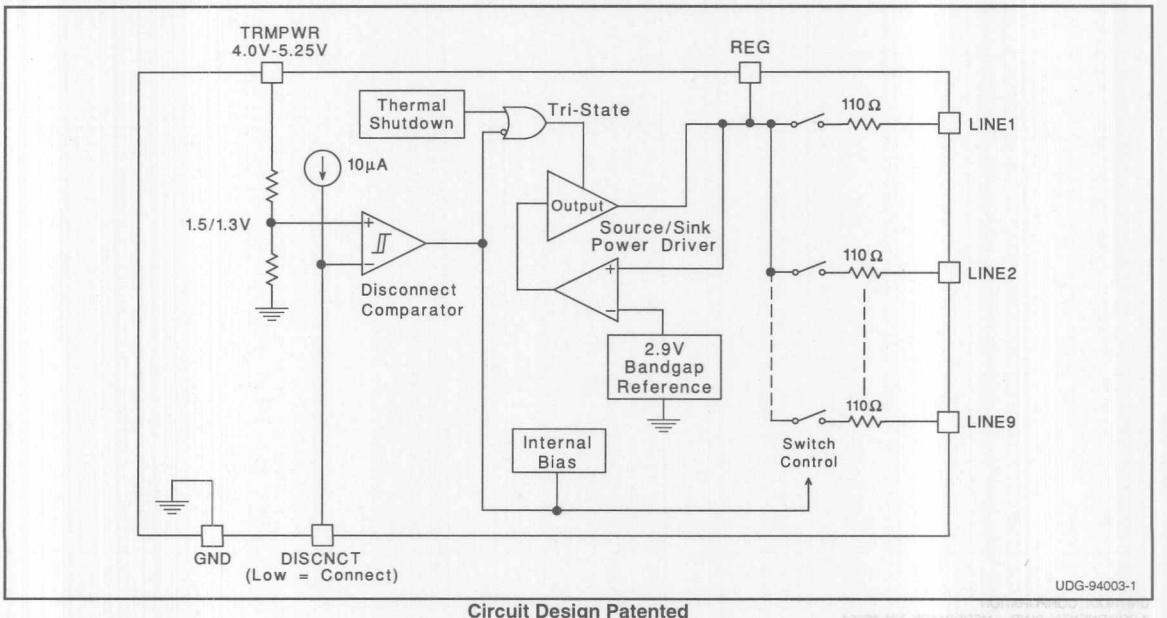
The UC5613 is pin-for-pin compatible with its predecessor, the UC5603 - 9 line Active Terminator. The only functional difference between the UC5613 and UC5603 is the absence of the negative clamps. Parametrically, the UC5613 has a 5% tolerance on impedance and current compared to a 3% tolerance on the UC5603. Custom power packages are utilized to allow normal operation at full power (1.2 watts).

Internal circuit trimming is utilized, first to trim the impedance to a 5% tolerance; then, the output current is trimmed to a 5% tolerance. The output current trim is set as close as possible to the maximum value of the SCSI specification which maximizes the noise margin for fast SCSI operation.

Other features include thermal shutdown and current limit.

This device is offered in low thermal resistance versions of the industry standard 16 pin narrow body SOIC, 16 pin ZIP (zig-zag in line package), and 24 pin TSSOP.

BLOCK DIAGRAM



Circuit Design Patented

ABSOLUTE MAXIMUM RATINGS

Termpwr Voltage ..... +7V
Signal Line Voltage..... 0V to +7V
Regulator Output Current 0.5A
Storage Temperature ..... –65°C to +150°C
Operating Temperature ..... –55°C to +150°C
Lead Temperature (Soldering, 10 Sec.)..... +300°C

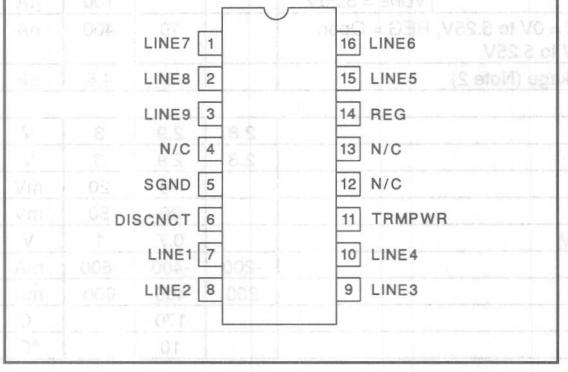
Unless otherwise specified all voltages are with respect to Ground. Currents are positive into, negative out of the specified terminal.
Consult Packaging Section of Unitrode Integrated Circuits databook for thermal limitations and considerations of packages.

RECOMMENDED OPERATING CONDITIONS

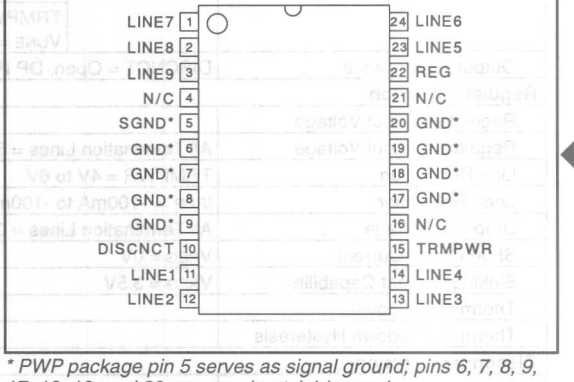
Termpwr Voltage ..... 3.8V to 5.25V
Signal Line Voltage..... 0V to +5V
Disconnect Input Voltage ..... 0V to Termpwr

CONNECTION DIAGRAMS

DIL-16 (Top View)
N or J Package

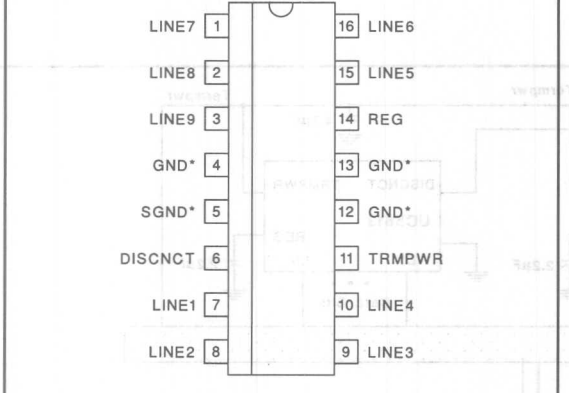


TSSOP-24 (Top View)
PWP Package

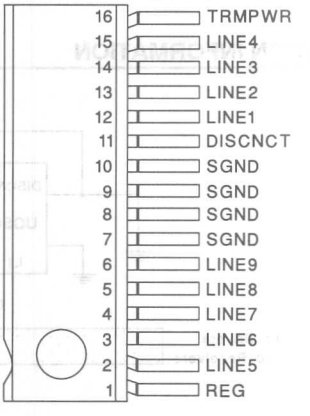


** PWP package pin 5 serves as signal ground; pins 6, 7, 8, 9, 17, 18, 19, and 20 serve as heatsink/ground.*

SOIC-16 (Top View)
DP Package



ZIP-16 (Top View)
Z Package



** DP package pin 5 serves as signal ground; pins 4, 12, 13 serve as heatsink/ground.*

Note: Drawings are not to scale.

ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C. TRMPWR = 4.75V, DISCNCT = 0V. T_A = T_J.

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNITS
Supply Current Section							
Termpwr Supply Current	All termination lines = Open				17	23	mA
	All termination lines = 0.5V				200	225	mA
Power Down Mode	DISCNCT = Open				100	150	µA
Output Section (Terminator Lines)							
Terminator Impedance	ΔI_{LINE} = -5mA to -15mA			104.5	110	115.5	Ohms
Output High Voltage	TRMPWR = 4V (Note 1)			2.7	2.9		V
Max Output Current	V_{LINE} = 0.5V		T_J = 25°C	-20.3	-21.5	-22.4	mA
			0°C < T_J < 70°C	-19.8	-21.5	-22.4	mA
Max Output Current	V_{LINE} = 0.5V, TRMPWR = 4V (Note 1)		T_J = 25°C	-19.5	-21.5	-22.4	mA
			0°C < T_J < 70°C	-19.0	-21.5	-22.4	mA
	V_{LINE} = 0.2V, TRMPWR = 4V to 5.25V		0°C < T_J < 70°C	-21.6	-24.0	-25.4	mA
Output Leakage	DISCNCT = 4V	TRMPWR = 0V to 5.25V REG = 0V	V_{LINE} = 0 to 4V		10	400	nA
			V_{LINE} = 5.25V			100	µA
		TRMPWR = 0V to 5.25V, REG = Open V_{LINE} = 0V to 5.25V			10	400	nA
Output Capacitance	DISCNCT = Open, DP Package (Note 2)				3	4.5	pF
Regulator Section							
Regulator Output Voltage				2.8	2.9	3	V
Regulator Output Voltage	All Termination Lines = 5V			2.8	2.9	3	V
Line Regulation	TRMPWR = 4V to 6V				10	20	mV
Load Regulation	I_{REG} = +100mA to -100mA				20	50	mV
Drop Out Voltage	All Termination Lines = 0.5V				0.7	1	V
Short Circuit Current	V_{REG} = 0V			-200	-400	-600	mA
Sinking Current Capability	V_{REG} = 3.5V			200	400	600	mA
Thermal Shutdown					170		°C
Thermal Shutdown Hysteresis					10		°C
Disconnect Section							
Disconnect Threshold				1.3	1.5	1.7	V
Threshold Hysteresis				100	160	250	mV

Note 1: Measuring each termination line while other 8 are low (0.5V).
Note 2: Guaranteed by design. Not 100% tested in production.

APPLICATION INFORMATION

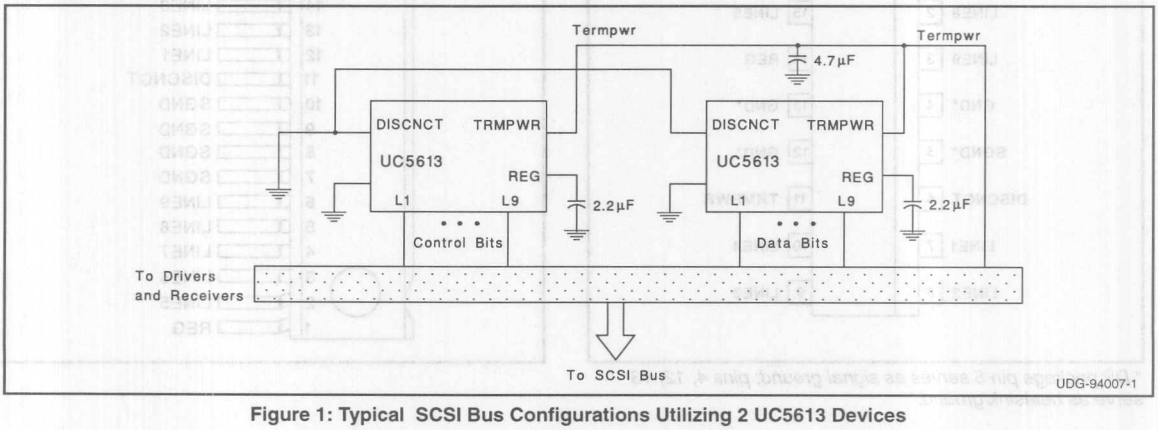


Figure 1: Typical SCSI Bus Configurations Utilizing 2 UC5613 Devices

APPLICATION INFORMATION (cont.)

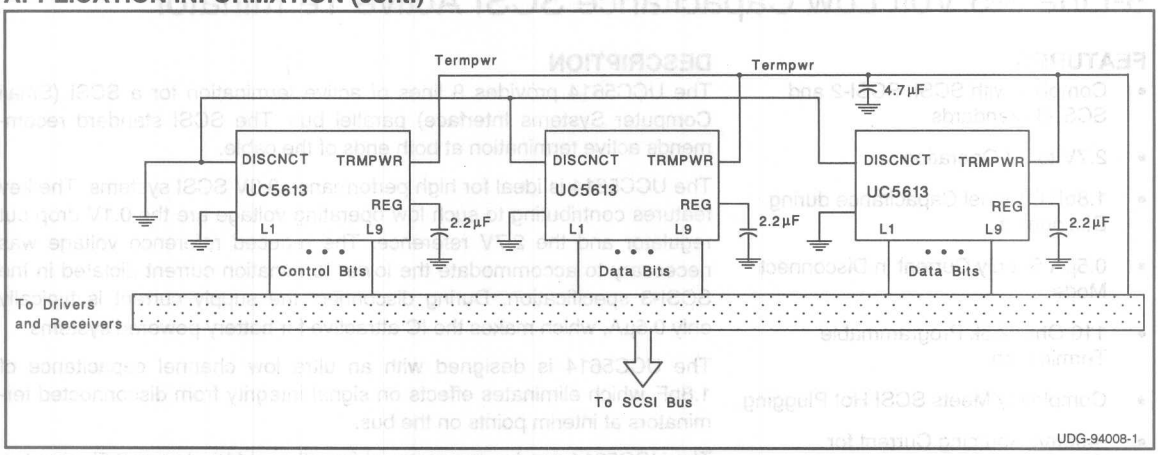


Figure 2: Typical Wide SCSI Bus Configurations Utilizing 3 UC5613 Devices.

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

UNITRODE

9-Line 3-5 Volt Low Capacitance SCSI Active Terminator

FEATURES

- Complies with SCSI, SCSI-2 and SCSI-3 Standards
- 2.7V to 7V Operation
- 1.8pF Channel Capacitance during Disconnect
- 0.5µA Supply Current in Disconnect Mode
- 110 Ohm/2.5k Programmable Termination
- Completely Meets SCSI Hot Plugging
- -400mA Sourcing Current for Termination
- +400mA Sinking Current for Active Negation Drivers
- Trimmed Termination Current to 4%
- Trimmed Impedance to 7%
- Current Limit and Thermal Shutdown Protection

DESCRIPTION

The UCC5614 provides 9 lines of active termination for a SCSI (Small Computer Systems Interface) parallel bus. The SCSI standard recommends active termination at both ends of the cable.

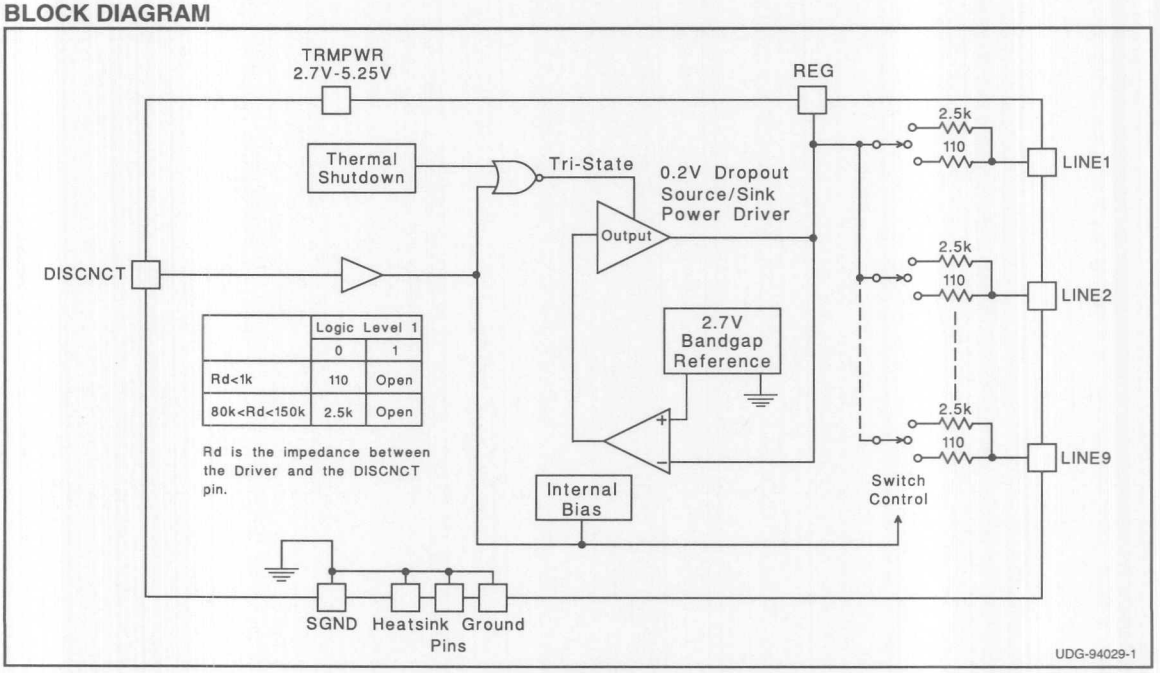
The UCC5614 is ideal for high performance 3.3V SCSI systems. The key features contributing to such low operating voltage are the 0.1V drop out regulator and the 2.7V reference. The reduced reference voltage was necessary to accommodate the lower termination current dictated in the SCSI-3 specification. During disconnect the supply current is typically only 0.5µA, which makes the IC attractive for battery powered systems.

The UCC5614 is designed with an ultra low channel capacitance of 1.8pF, which eliminates effects on signal integrity from disconnected terminators at interim points on the bus.

The UCC5614 can be programmed for either a 110 ohm or 2.5k ohm termination. The 110 ohm termination is used for standard SCSI bus lengths and the 2.5k ohm termination is typically used in short bus applications. When driving the TTL compatible DISCNCT pin directly, the 110 ohm termination is connected when the DISCNCT pin is driven low, and disconnected when driven high. When the DISCNCT pin is driven through an impedance between 80k and 150k, the 2.5k ohm termination is connected when the DISCNCT pin is driven low, and disconnected when driven high.

continued

BLOCK DIAGRAM



	Logic Level 1	
	0	1
Rd<1k	110	Open
80k<Rd<150k	2.5k	Open

Rd is the impedance between the Driver and the DISCNCT pin.

Circuit Design Patented

Description Continued

The power amplifier output stage allows the UCC5614 to source full termination current and sink active negation current when all termination lines are actively negated.

The UCC5614 is pin for pin compatible with Unitrode's other 9 line SCSI terminators, allowing lower capacitance and lower voltage upgrades to existing systems. The UCC5614, as with all Unitrode terminators, is completely hot pluggable and appears as high impedance at the terminating channels with V_{TRMPWR} = 0V or open.

Internal circuit trimming is utilized, first to trim the 110 ohm termination impedance to a 7% tolerance, and then most importantly, to trim the output current to a 4% tolerance, as close to the max SCSI-3 spec as possible, which maximizes noise margin in fast SCSI operation.

Other features include thermal shutdown and current limit.

This device is offered in low thermal resistance versions of the industry standard 16 pin narrow body SOIC, 16 pin ZIP (Zig-Zag In Line package), 24 pin TSSOP and 28 pin PLCC.

ABSOLUTE MAXIMUM RATINGS

Termpwr Voltage . . . . . +7V
Signal Line Voltage. . . . . 0V to +7V
Regulator Output Current 0.6A
Storage Temperature . . . . . –65°C to +150°C
Operating Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 Sec.) . . . . . +300°C

Unless otherwise specified all voltages are with respect to Ground. Currents are positive into, negative out of the specified terminal.

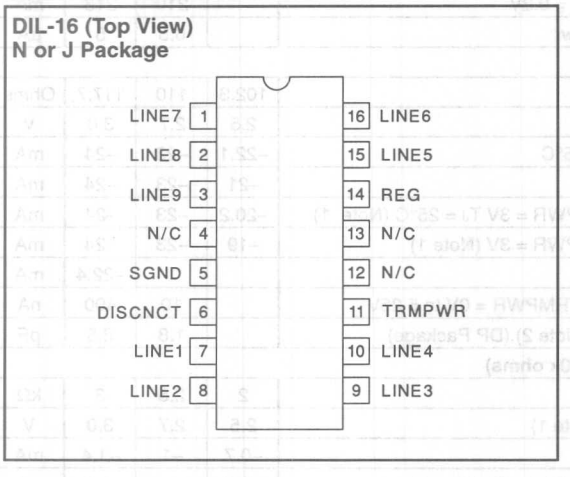
Consult Packaging Section of Unitrode Integrated Circuits databook for thermal limitations and considerations of packages.

RECOMMENDED OPERATING CONDITIONS

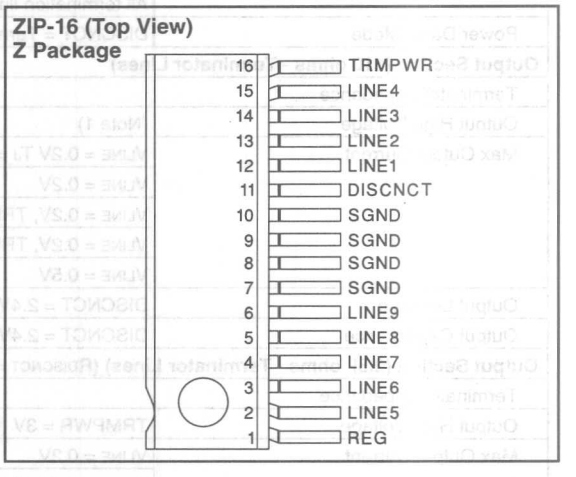
Termpwr Voltage . . . . . 2.7V to 5.25V
Signal Line Voltage. . . . . 0V to +5V
Disconnect Input Voltage . . . . . 0V to Termpwr

CONNECTION DIAGRAMS

DIL-16 (Top View)
N or J Package



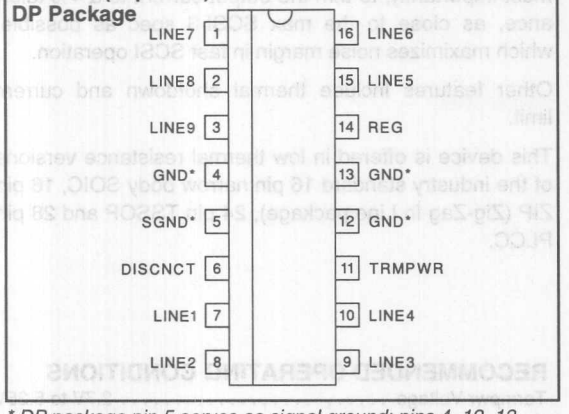
ZIP-16 (Top View)
Z Package



Note: Drawings are not to scale.

CONNECTION DIAGRAMS (cont.)

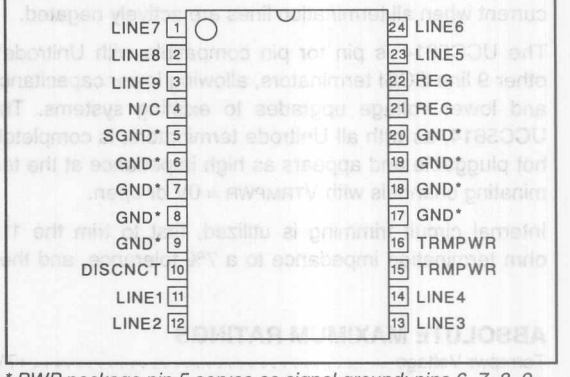
SOIC-16 (Top View)
DP Package



** DP package pin 5 serves as signal ground; pins 4, 12, 13 serve as heatsink/ground.*

Note: Drawings are not to scale.

TSSOP-24 (Top View)
PWP Package



** PWP package pin 5 serves as signal ground; pins 6, 7, 8, 9, 17, 18, 19, and 20 serve as heatsink/ground.*

ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C. TRMPWR = 3.3V, DISCNCT = 0V, $R_{DISCNCT}$= 0 ohms. $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current Section					
Termpwr Supply Current	All termination lines = Open		1	2	mA
	All termination lines = 0.2V		210	218	mA
Power Down Mode	DISCNCT = Termpwr		0.5	5	µA
Output Section (110 ohms - Terminator Lines)					
Terminator Impedance		102.3	110	117.7	Ohms
Output High Voltage	(Note 1)	2.5	2.7	3.0	V
Max Output Current	V_{LINE} = 0.2V T_J = 25°C	–22.1	–23	–24	mA
	V_{LINE} = 0.2V	–21	–23	–24	mA
	V_{LINE} = 0.2V, TRMPWR = 3V T_J = 25°C (Note 1)	–20.2	–23	–24	mA
	V_{LINE} = 0.2V, TRMPWR = 3V (Note 1)	–19	–23	–24	mA
	V_{LINE} = 0.5V			–22.4	mA
Output Leakage	DISCNCT = 2.4V, TRMPWR = 0V to 5.25V		10	400	nA
Output Capacitance	DISCNCT = 2.4V (Note 2) (DP Package)		1.8	2.5	pF
Output Section (2.5k ohms - Terminator Lines) ($R_{DISCNCT}$ = 80k ohms)					
Terminator Impedance		2	2.5	3	kΩ
Output High Voltage	TRMPWR = 3V (Note 1)	2.5	2.7	3.0	V
Max Output Current	V_{LINE} = 0.2V	–0.7	–1	–1.4	mA
	V_{LINE} = 0.2V, TRMPWR = 3V (Note 1)	–0.6	–1	–1.5	mA
Output Leakage	DISCNCT = 2.4V, TRMPWR = 0 to 5.25V		10	400	nA
Output Capacitance	DISCNCT = 2.4V (Note 2) (DP Package)		1.8	2.5	pF
Regulator Section					
Regulator Output Voltage	5.25V > TRMPWR > 3V	2.5	2.7	3.0	V
Drop Out Voltage	All Termination Lines = 0.2V		0.1	0.2	V
Short Circuit Current	V_{REG} = 0V	–200	–400	–800	mA

ELECTRICAL CHARACTERISTICS (cont.) Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C. TRMPWR = 3.3V, DISCNCT = 0V, $R_{DISCNCT}$= 0 ohms. T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Regulator Section (cont.)					
Sinking Current Capability	V_{REG} = 3V	200	400	800	mA
Thermal Shutdown	(Note 2)		170		°C
Thermal Shutdown Hysteresis	(Note 2)		10		°C
Disconnect Section					
Disconnect Threshold	$R_{DISCNCT}$ = 0 & 80k	0.8	1.5	2.0	V
Input Current	DISCNCT = 0V		30	50	µA

Note 1: Measuring each termination line while other 8 are low (0.2V).
Note 2: Guaranteed by design. Not 100% tested in production.

APPLICATION INFORMATION

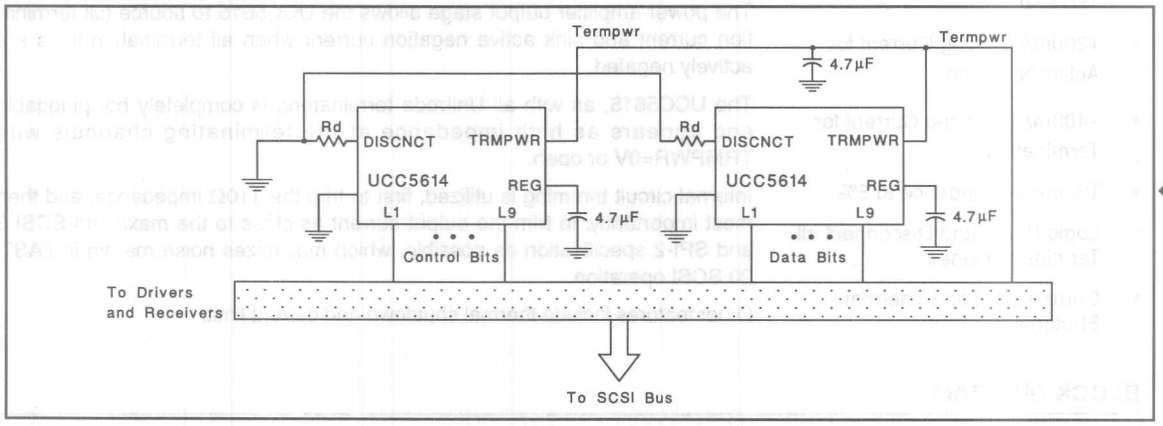


Figure 1: Typical SCSI Bus Configurations Utilizing 2 UCC5614 Devices

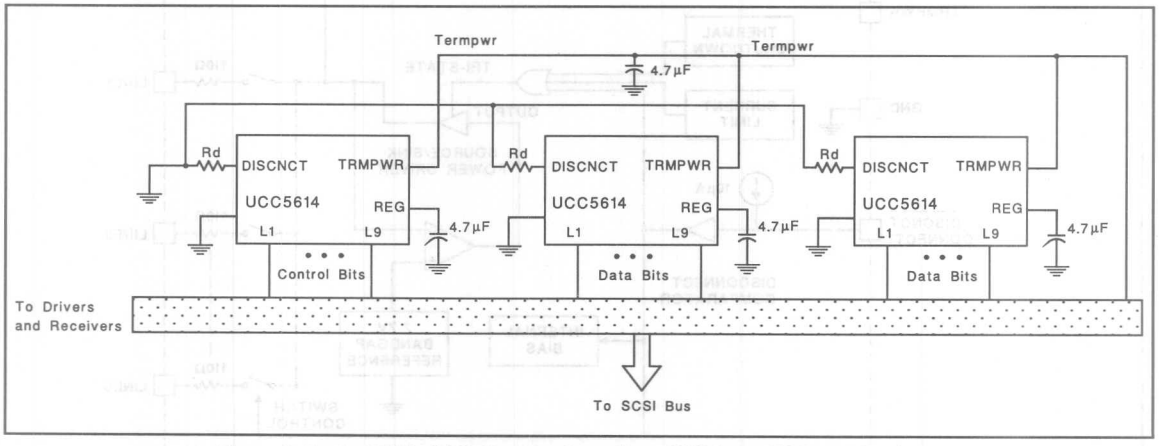


Figure 2: Typical Wide SCSI Bus Configurations Utilizing 3 UCC5614 Devices.

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

9-Line SCSI Terminator (Reverse Disconnect)

FEATURES

- Complies with SCSI, SCSI-2, SCSI-3, SPI, and FAST-20 Standards
- 1.8pF Channel Capacitance During Disconnect
- 1000µA Supply Current in Disconnect Mode
- 110Ω Termination
- SCSI Hot Plugging Compliant, 10nA Typical
- +200mA Sinking Current for Active Negation
- –400mA Sourcing Current for Termination
- Trimmed Impedance to 5%
- Logic Command Disconnect all Termination Lines
- Current Limit and Thermal Shutdown

DESCRIPTION

The UCC5615 provides 9 lines of active termination for a SCSI (Small Computers Systems Interface) parallel bus. The SCSI standard recommends and Fast-20 (Ultra) requires active termination at both ends of the cable.

Pin for pin compatible with the UC5605 and UCC5606, the UCC5615 is ideal for high performance 5V SCSI systems, Termpwr 4V to 7V. During disconnect the supply current is only 100µA typical, which makes the IC attractive for lower powered systems.

The UCC5615 is designed with a low channel capacitance of 1.8pF, which eliminates effects on signal integrity from disconnected terminators at interim points on the bus.

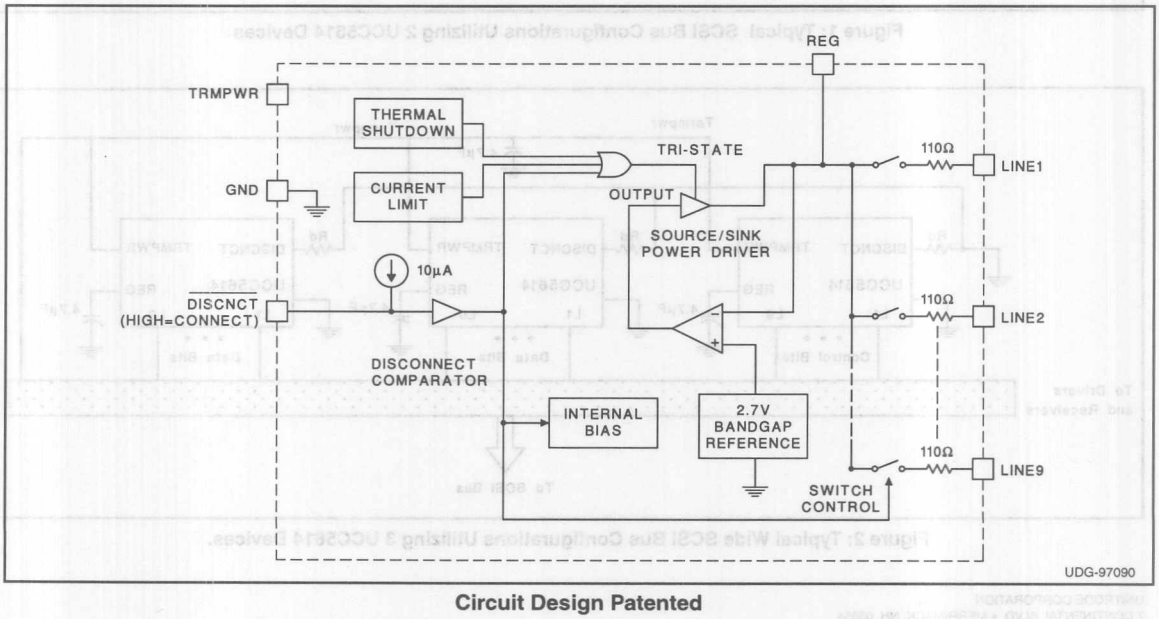
The power amplifier output stage allows the UCC5615 to source full termination current and sink active negation current when all termination lines are actively negated.

The UCC5615, as with all Unitrode terminators, is completely hot pluggable and appears as high impedance at the terminating channels with TRMPWR=0V or open.

Internal circuit trimming is utilized, first to trim the 110Ω impedance, and then most importantly, to trim the output current as close to the maximum SCSI-3 and SPI-2 specification as possible, which maximizes noise margin in FAST-20 SCSI operation.

Other features include thermal shutdown and current limit.

BLOCK DIAGRAM



Circuit Design Patented

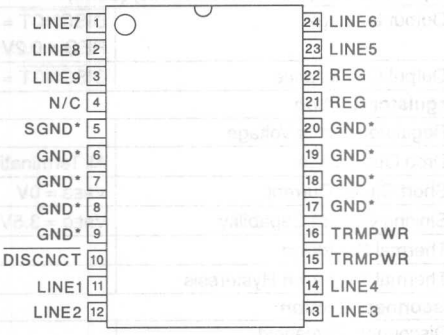
ABSOLUTE MAXIMUM RATINGS

Tempwr . . . . . +7V
Signal Line Voltage . . . . . .0V to +7V
Regulator Output Current 0.5A
Storage Temperature . . . . . .–65°C to +150°C
Operating Junction Temperature . . . . . .–55°C to +150°C
Lead Temperature (Soldering, 10 Seconds) . . . . . .300°C

All currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

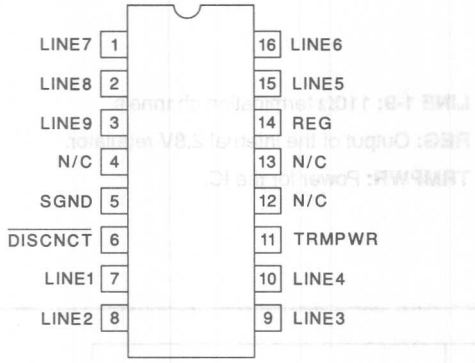
CONNECTION DIAGRAMS

TSSOP-24 (Top View)
PWP Package



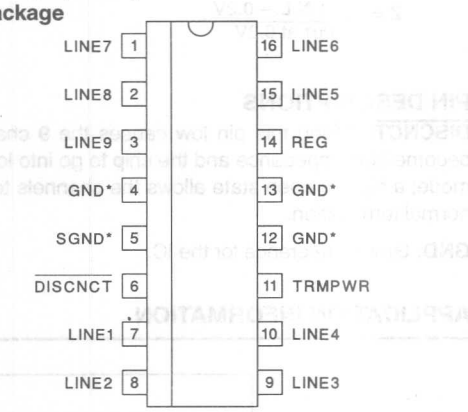
** PWP package pin 5 serves as signal ground; pins 6, 7, 8, 9, 17, 18, 19, and 20 serve as heatsink ground.*

DIL-16 (Top View)
N or J Package



Note: Drawings are not to scale.

SOIC-16 (Top View)
DP Package



** DP package pin 5 serves as signal ground; pins 4, 12, and 13 serve as heatsink/ground.*

ELECTRICAL CHARACTERISTICS

Unless otherwise stated these specifications apply for T_A = 0°C to 70°C, TRMPWR = 4.75V, $\overline{\text{DISCNCT}}$ = 4.75V, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current Section					
Termpwr Supply Current	All termination lines = Open		1	2	mA
	All termination lines = 0.2V		210	230	mA
Power Down Mode	$\overline{\text{DISCNCT}}$ = 0V		100	150	µA
Output Section (Termination Lines)					
Termination Impedance	(Note 3)	104.5	110	115.5	Ω
Output High Voltage	V_{TRMPWR} = 4V (Note 1)	2.6	2.8	3	V
Maximum Output Current	V_{LINE} = 0.2V, T_J = 25°C	–22.1	–23.3	–24	mA
	V_{LINE} = 0.2V	–20.7	–23.3	–24	mA
	V_{LINE} = 0.2V, TRMPWR = 4V, T_J = 25°C (Note 1)	–21	–23	–24	mA
	V_{LINE} = 0.2V, TRMPWR = 4V (Note 1)	–20	–23	–24	mA
	V_{LINE} = 0.5V			–22.4	mA

ELECTRICAL CHARACTERISTICS (cont.) Unless otherwise stated these specifications apply for T_A = 0°C to 70°C, TRMPWR = 4.75V, $\overline{DISCNCT}$ = 4.75V, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Section (Termination Lines) (cont.)					
Output Leakage	$\overline{DISCNCT}$ = 0V, TRMPWR = 0V to 5.25V, REG = 0.2V		10	400	nA
Output Capacitance	$\overline{DISCNCT}$ = 2.4V (Note 2)		1.8	2.5	pF
Regulator Section					
Regulator Output Voltage		2.6	2.8	3	V
Drop Out Voltage	All Termination Lines = 0.2V		0.4	0.8	V
Short Circuit Current	V_{REG} = 0V	–225	–400	–600	mA
Sinking Current Capability	V_{REG} = 3.5V	100	200	400	mA
Thermal Shutdown			170		°C
Thermal Shutdown Hysteresis			10		°C
Disconnect Section					
Disconnect Threshold		0.8	1.5	2	V
Input Current	$\overline{DISCNCT}$ = 0V		–10	–30	µA

Note 1: Measuring each termination line while other 8 are low (0.2V).
Note 2: Guaranteed by design. Not 100% tested in production.
Note 3: Tested by measuring I_{OUT} with V_{OUT} = 0.2V and V_{OUT} with no load, then calculating:

$$Z = \frac{V_{OUT}\ \text{N.L.} - 0.2V}{I_{OUT}\ \text{at}\ 0.2V}.$$

PIN DESCRIPTIONS

$\overline{DISCNCT}$: Taking this pin low causes the 9 channels to become high impedance and the chip to go into low-power mode; a high or open state allows the channels to provide normal termination.

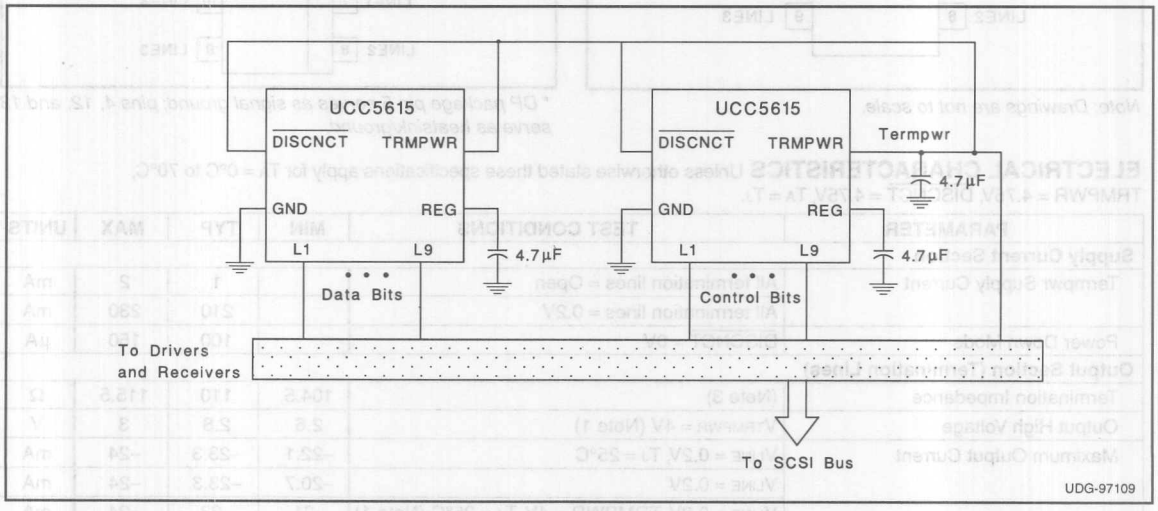
GND: Ground reference for the IC.

LINE 1-9: 110Ω termination channels.

REG: Output of the internal 2.8V regulator.

TRMPWR: Power for the IC.

APPLICATION INFORMATION



UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

9-Line SCSI Terminator

FEATURES

- Complies with SCSI, SCSI-2, SCSI-3, SPI, FAST-20, and SPI-2 Standards
- 1.8pF Channel Capacitance During Disconnect
- 100µA Supply Current in Disconnect Mode
- 110 Ohm Termination
- SCSI Hot Plugging Compliant, 10nA Typical
- +200mA Sinking Current for Active Negation
- –400mA Sourcing Current for Termination
- Trimmed Impedance to 5%
- Logic Command Disconnect all Termination Lines
- Current Limit and Thermal Shutdown

DESCRIPTION

The UCC5616 provides 9 lines of active termination for a SCSI (Small Computers Systems Interface) parallel bus. The SCSI standard recommends and Fast-20 (Ultra) requires active termination at both ends of the cable.

Pin for pin compatible with the UC5603, UC5612, UC5613, and UCC5614 the UCC5616 is ideal for high performance 5V SCSI systems, Termpwr 4V to 7V. During disconnect the supply current is only 50µA typical, which makes the IC attractive for lower powered systems.

The UCC5616 is designed with a low channel capacitance of 1.8pF, which eliminates effects on signal integrity from disconnected terminators at interim points on the bus.

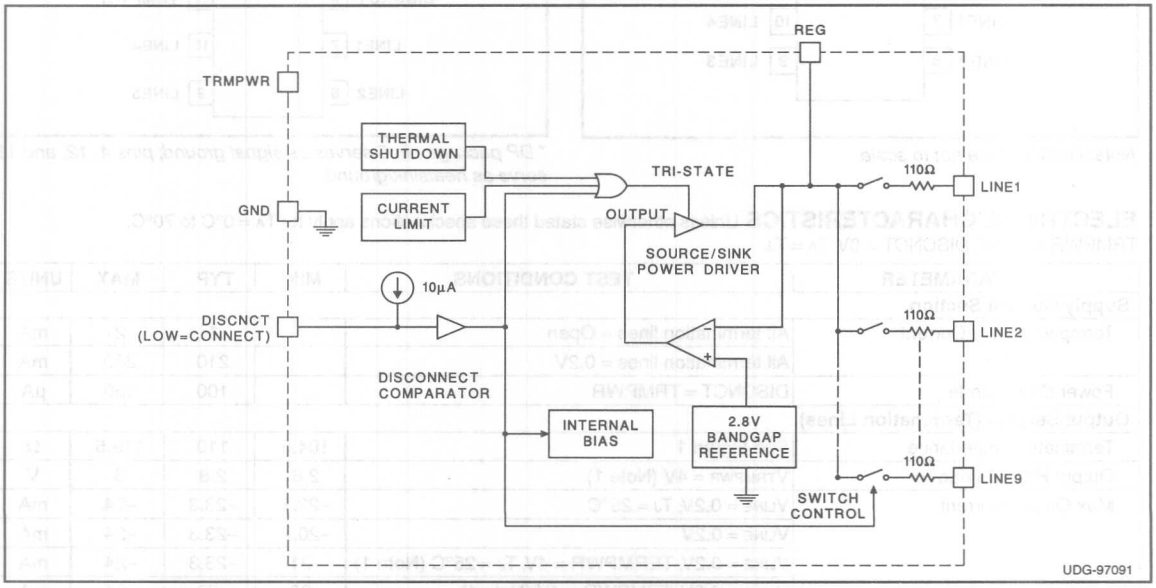
The power amplifier output stage allows the UCC5616 to source full termination current and sink active negation current when all termination lines are actively negated.

The UCC5616, as with all Unitrode terminators, is completely hot pluggable and appears as high impedance at the terminating channels with TRMPWR=0V or open.

Internal circuit trimming is utilized, first to trim the 110 ohm impedance, and then most importantly, to trim the output current as close to the max SCSI-3 and SPI spec as possible, which maximizes noise margin in FAST-20 SCSI operation.

Other features include thermal shutdown and current limit.

BLOCK DIAGRAM



Circuit Design Patented

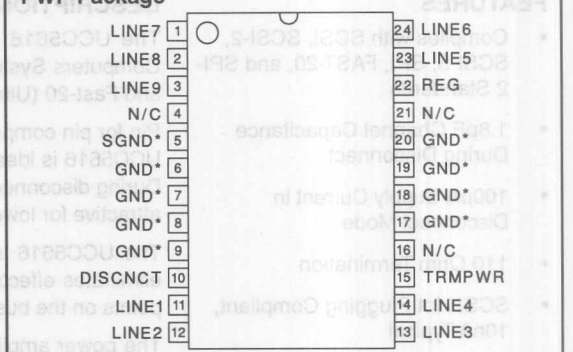
ABSOLUTE MAXIMUM RATINGS

Tempwr . . . . . +7V
Signal Line Voltage . . . . . .0V to +7V
Regulator Output Current 0.5A
Storage Temperature . . . . . .–65°C to +150°C
Operating Junction Temperature . . . . . .–55°C to +150°C
Lead Temperature (Soldering, 10 Seconds) . . . . . .300°C

All currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

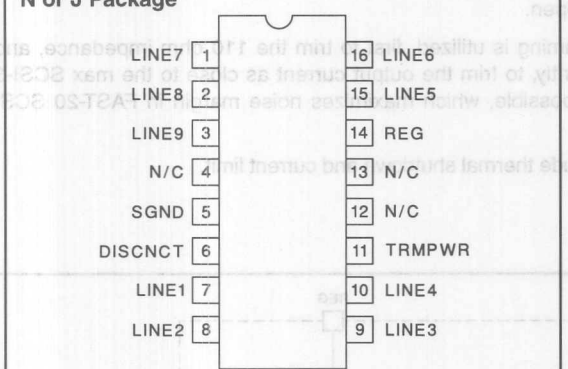
CONNECTION DIAGRAMS

TSSOP-24 (Top View)
PWP Package



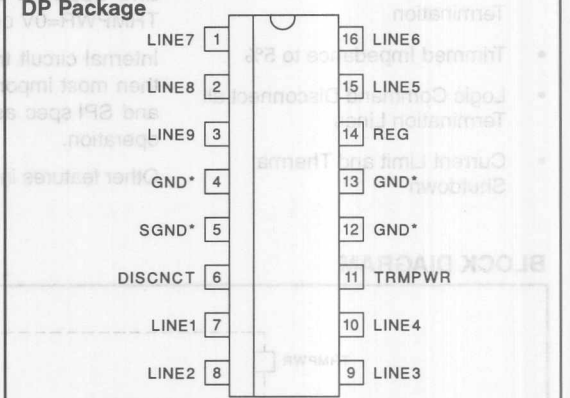
** PWP package pin 5 serves as signal ground; pins 6, 7, 8, 9, 17, 18, 19, and 20 serve as heatsink ground.*

DIL-16 (Top View)
N or J Package



Note: Drawings are not to scale.

SOIC-16 (Top View)
DP Package



** DP package pin 5 serves as signal ground; pins 4, 12, and 13 serve as heatsink/ground.*

ELECTRICAL CHARACTERISTICS

Unless otherwise stated these specifications apply for T_A = 0°C to 70°C, TRMPWR = 4.75V, DISCNCT = 0V, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current Section					
Termpwr Supply Current	All termination lines = Open		1	2	mA
	All termination lines = 0.2V		210	230	mA
Power Down Mode	DISCNCT = TRMPWR		100	150	µA
Output Section (Termination Lines)					
Termination Impedance	See Figure 1	104.5	110	115.5	Ω
Output High Voltage	V_{TRMPWR} = 4V (Note 1)	2.6	2.8	3	V
Max Output Current	V_{LINE} = 0.2V, T_J = 25°C	–22.1	–23.3	–24	mA
	V_{LINE} = 0.2V	–20.7	–23.3	–24	mA
	V_{LINE} = 0.2V, TERMPWR = 4V, T_J = 25°C (Note 1)	–21	–23.3	–24	mA
	V_{LINE} = 0.2V, TRMPWR = 4V (Note 1)	–20	–23	–24	mA
	V_{LINE} = 0.5V			–22.4	mA

ELECTRICAL CHARACTERISTICS (cont.) Unless otherwise stated these specifications apply for T_A = 0°C to 70°C, TRMPWR = 4.75V, DISCNCT = 0V, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Section (Termination Lines) (cont.)					
Output Leakage	DISCNCT = 2.4V, TRMPWR = 0V to 5.25V, REG = 0.2V		10	400	nA
Output Capacitance	DISCNCT = 2.4V (Note 2)		1.8	2.5	pF
Regulator Section					
Regulator Output Voltage		2.6	2.8	3	V
Drop Out Voltage	All Termination Lines = 0.2V		0.4	0.8	V
Short Circuit Current	V_{REG} = 0V	–225	–400	–600	mA
Sinking Current Capability	V_{REG} = 3.5V	100	200	400	mA
Thermal Shutdown			170		°C
Thermal Shutdown Hysteresis			10		°C
Disconnect Section					
Disconnect Threshold		0.8	1.5	2	V
Input Current	DISCNCT = 0V		–10	–30	µA

Note 1: Measuring each termination line while other 8 are low (0.2V).
Note 2: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

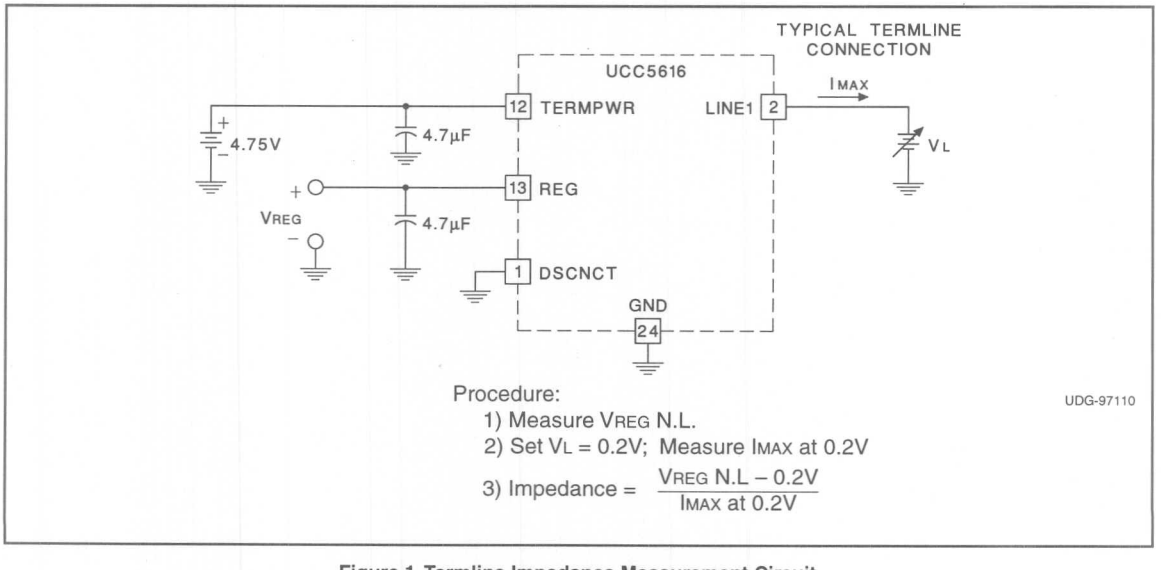
DISCNCT: Taking this pin high or leaving it open causes the 9 channels to become high impedance and the chip to go into low-power mode; a low state allows the channels to provide normal termination.

GND: Ground reference for the IC.

LINE1-9: 110 ohm termination channels.

REG: Output of the internal 2.8V regulator.

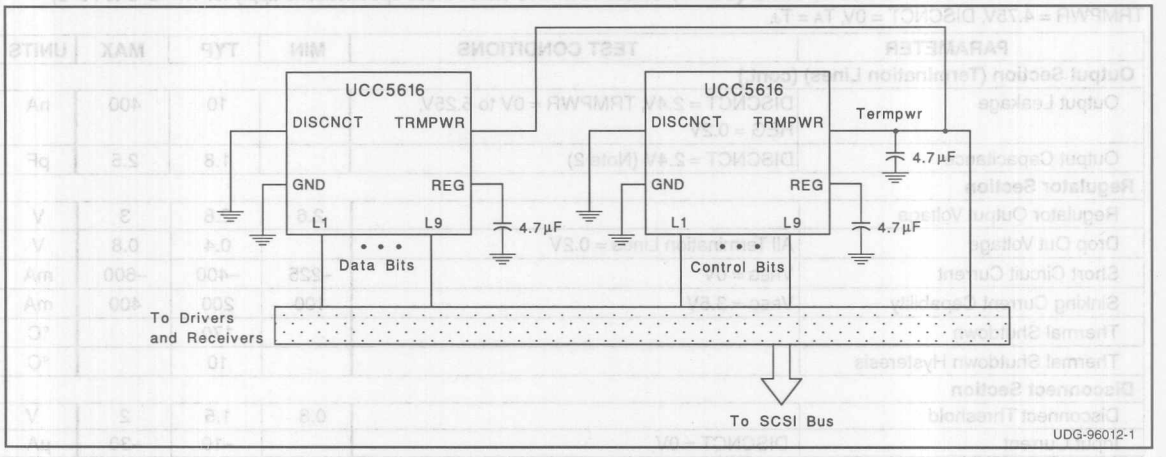
TRMPWR: Power for the IC.



Procedure:
1) Measure V_{REG} N.L.
2) Set V_L = 0.2V; Measure I_{MAX} at 0.2V
3) Impedance = $\frac{V_{REG}\ N.L. - 0.2V}{I_{MAX}\ at\ 0.2V}$

Figure 1. Termline Impedance Measurement Circuit

APPLICATION INFORMATION



UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

UNITRODE

18-Line SCSI Terminator (Reverse Disconnect)

FEATURES

- Complies with SCSI, SCSI-2, SCSI-3 and FAST-20 Standards
- 2pF Channel Capacitance During Disconnect
- 50µA Supply Current in Disconnect Mode
- 110Ω Termination
- SCSI Hot Plugging Compliant, 10nA Typical
- +400mA Sinking Current for Active Negation
- –650mA Sourcing Current for Termination
- Trimmed Impedance to 5%

DESCRIPTION

The UCC5617 provides 18 lines of active termination for a SCSI (Small Computers Systems Interface) parallel bus. The SCSI standard recommends and Fast-20 (Ultra) requires active termination at both ends of the cable.

Pin for pin compatible with the UC5609, the UCC5617 is ideal for high performance 5V SCSI systems, Termpwr 4.0V to 5.25V. During disconnect the supply current is only 50µA typical, which makes the IC attractive for lower powered systems.

The UCC5617 is designed with a low channel capacitance of 2pF, which eliminates effects on signal integrity from disconnected terminators at interim points on the bus.

The power amplifier output stage allows the UCC5617 to source full termination current and sink active negation current when all termination lines are actively negated.

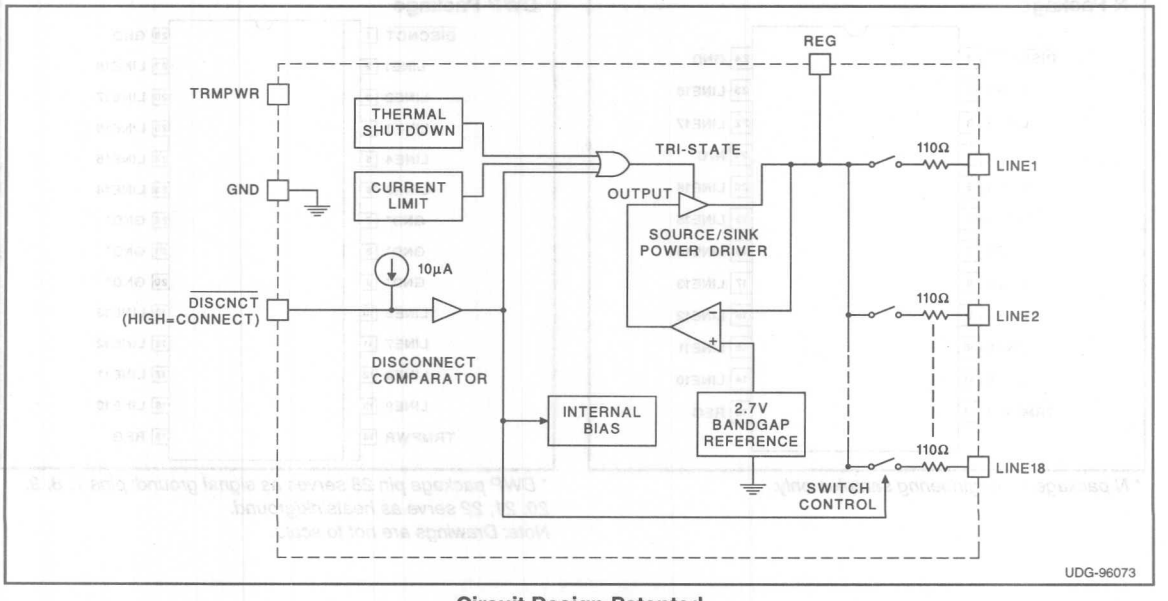
The UCC5617, as with all Unitrode terminators, is completely hot pluggable and appears as high impedance at the terminating channels with TRMPWR=0V or open.

Internal circuit trimming is utilized, first to trim the 110Ω impedance, and then most importantly, to trim the output current as close to the maximum SCSI-3 specification as possible, which maximizes noise margin in fast SCSI operation.

Other features include thermal shutdown and current limit.

This device is offered in low thermal resistance versions of the industry standard 28 pin wide body SOIC, TSSOP and PLCC.

BLOCK DIAGRAM



Circuit Design Patented

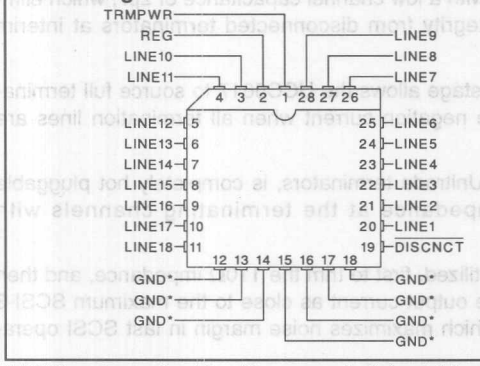
ABSOLUTE MAXIMUM RATINGS

Tempwr . . . . . +7V
Signal Line Voltage . . . . . .0V to +7V
Regulator Output Current 1A
Storage Temperature . . . . . –65°C to +150°C
Operating Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 Seconds) . . . . . 300°C

All currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

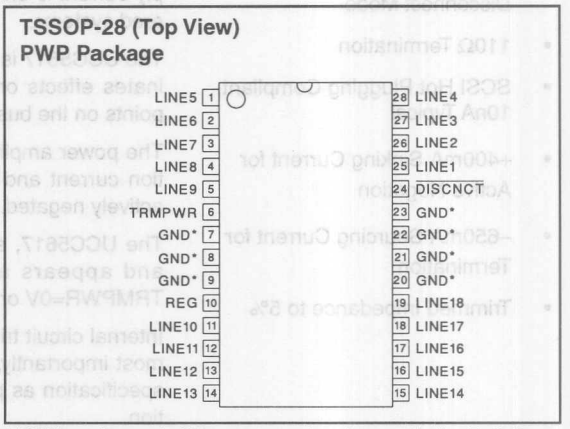
CONNECTION DIAGRAMS

PLCC-28 (Top View)
QP Package



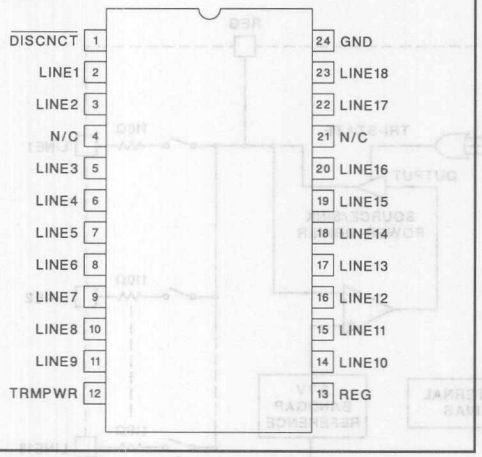
** DWP package pins 12 - 18 serve as both heatsink and signal ground.*

TSSOP-28 (Top View)
PWP Package



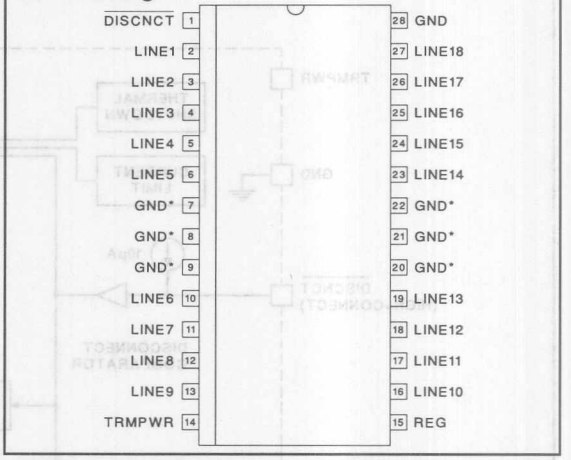
** PWP package pin 23 serves as signal ground; pins 7, 8, 9, 20, 21, and 22 serve as heatsink ground.*

DIL-24 (Top View)
N Package



** N package for engineering samples only.*

SOIC-28 (Top View)
DWP Package



** DWP package pin 28 serves as signal ground; pins 7, 8, 9, 20, 21, 22 serve as heatsink/ground.*
Note: Drawings are not to scale.

ELECTRICAL CHARACTERISTICS Unless otherwise stated these specifications apply for T_A = 0°C to 70°C, TRMPWR = 4.75V, $\overline{DISCNCT}$ = 4.75V, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current Section					
Termpwr Supply Current	All termination lines = Open		1	2	mA
	All termination lines = 0.2V		420	450	mA
Power Down Mode	$\overline{DISCNCT}$ = 0V		50	100	µA
Output Section (Termination Lines)					
Termination Impedance	(Note 3)	104.5	110	115.5	Ω
Output High Voltage	V_{TRMPWR} = 4V (Note 1)	2.6	2.8	3	V
Maximum Output Current	V_{LINE} = 0.2V, T_J = 25°C	–22.1	–23.3	–24	mA
	V_{LINE} = 0.2V	–20.7	–23.3	–24	mA
	V_{LINE} = 0.2V, TRMPWR = 4V, T_J = 25°C (Note 1)	–21	–23	–24	mA
	V_{LINE} = 0.2V, TRMPWR = 4V (Note 1)	–20	–23	–24	mA
	V_{LINE} = 0.5V			–22.4	mA
Output Leakage	$\overline{DISCNCT}$ = 0V, TRMPWR = 0V to 5.25V, REG = 0.2V, V_{LINE} = 5.25V		10	400	nA
Output Capacitance	$\overline{DISCNCT}$ = 2.4V (Note 2)		2	3.5	pF
Regulator Section					
Regulator Output Voltage		2.6	2.8	3	V
Drop Out Voltage	All Termination Lines = 0.2V		0.4	0.8	V
Short Circuit Current	V_{REG} = 0V	–475	–650	–850	mA
Sinking Current Capability	V_{REG} = 3.5V	200	400	800	mA
Thermal Shutdown			170		°C
Thermal Shutdown Hysteresis			10		°C
Disconnect Section					
Disconnect Threshold		0.8	1.5	2	V
Input Current	$\overline{DISCNCT}$ = 0V		–10	–30	µA

Note 1: Measuring each termination line while other 17 are low (0.2V).
Note 2: Guaranteed by design. Not 100% tested in production.
Note 3: Tested by measuring I_{OUT} with V_{OUT} = 0.2V and V_{OUT} with no load, then calculating:

$$Z = \frac{V_{OUT}\ N.L. - 0.2V}{I_{OUT}\ at\ 0.2V}.$$

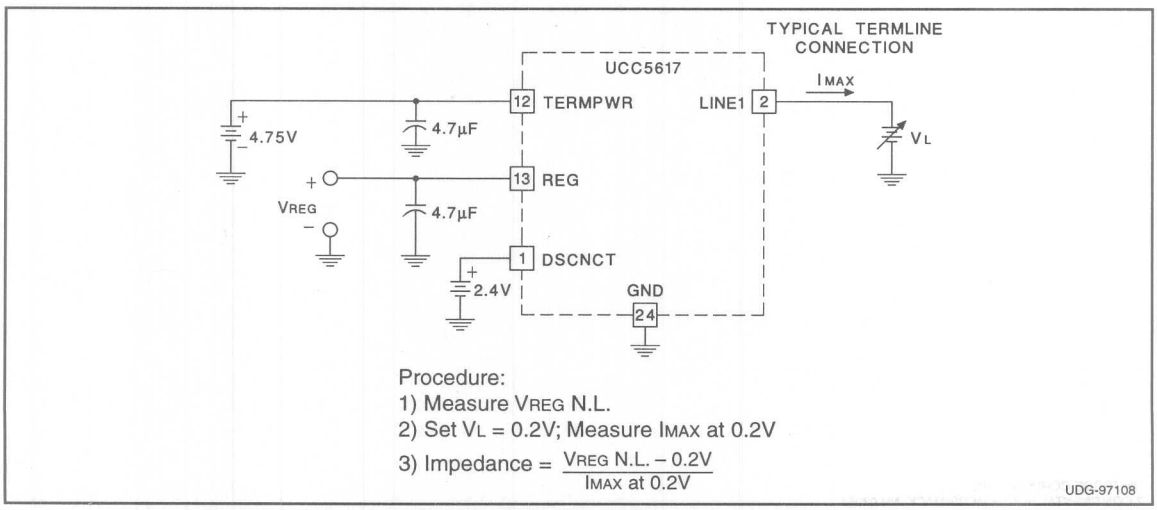


Figure 1. Termline Impedance Measurement Circuit

DISCNCT: Taking this pin low causes the 18 channels to become high impedance and the chip to go into low-power mode; a high or open state allows the channels to provide normal termination.

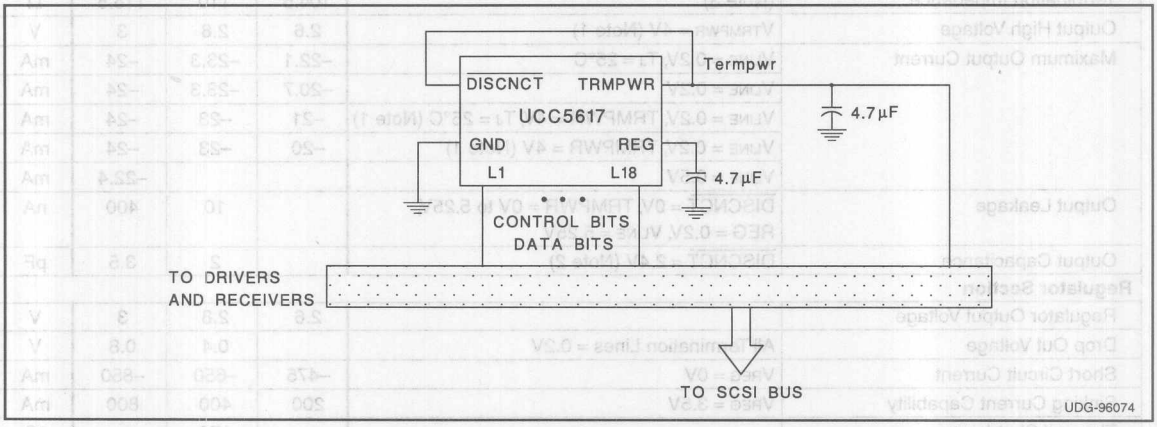
GND: Ground reference for the IC.

LINE 1-18: 110Ω termination channels.

REG: Output of the internal 2.8V regulator.

TRMPWR: Power for the IC.

APPLICATION INFORMATION



UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

UNITRODE

18-Line SCSI Terminator

FEATURES

- Complies with SCSI, SCSI-2, SCSI-3 and FAST-20 Standards
- 2pF Channel Capacitance During Disconnect
- 50µA Supply Current in Disconnect Mode
- 110 Ohm Termination
- SCSI Hot Plugging Compliant, 10nA Typical
- +400mA Sinking Current for Active Negation
- –650mA Sourcing Current for Termination
- Trimmed Impedance to 5%

DESCRIPTION

The UCC5618 provides 18 lines of active termination for a SCSI (Small Computers Systems Interface) parallel bus. The SCSI standard recommends and Fast-20 (Ultra) requires active termination at both ends of the cable.

Pin for pin compatible with the UC5601 and UC5608, the UCC5618 is ideal for high performance 5V SCSI systems, Termpwr 4.0-5.25V. During disconnect the supply current is only 50µA typical, which makes the IC attractive for lower powered systems.

The UCC5618 is designed with a low channel capacitance of 2pF, which eliminates effects on signal integrity from disconnected terminators at interim points on the bus.

The power amplifier output stage allows the UCC5618 to source full termination current and sink active negation current when all termination lines are actively negated.

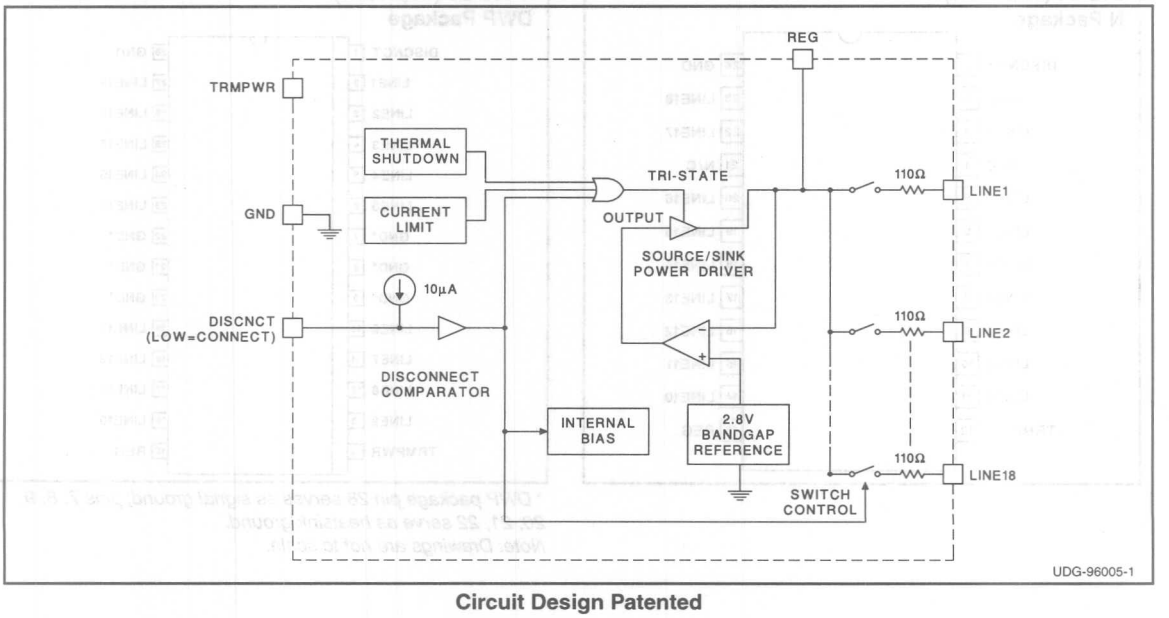
The UCC5618, as with all Unitrode terminators, is completely hot pluggable and appears as high impedance at the terminating channels with TRMPWR=0V or open.

Internal circuit trimming is utilized, first to trim the 110 ohm impedance, and then most importantly, to trim the output current as close to the max SCSI-3 spec as possible, which maximizes noise margin in fast SCSI operation.

Other features include thermal shutdown and current limit.

This device is offered in low thermal resistance versions of the industry standard 28 pin wide body SOIC, TSSOP and PLCC.

BLOCK DIAGRAM



Circuit Design Patented

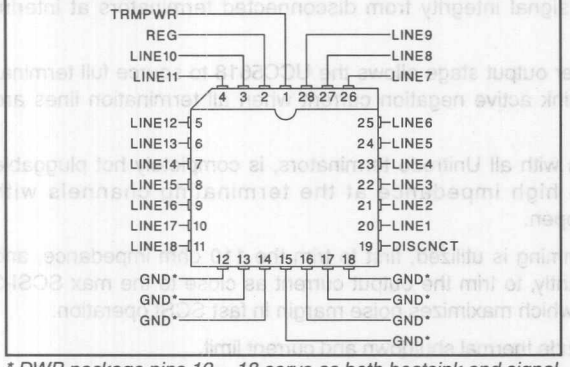
ABSOLUTE MAXIMUM RATINGS

Tempwr . . . . . +7V
Signal Line Voltage . . . . . .0V to +7V
Regulator Output Current 1A
Storage Temperature . . . . . –65°C to +150°C
Operating Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 Seconds) . . . . . .300°C

All currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

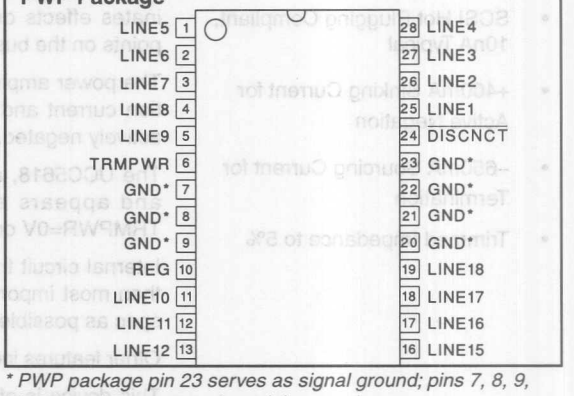
CONNECTION DIAGRAMS

PLCC-28 (Top View)
QP Package



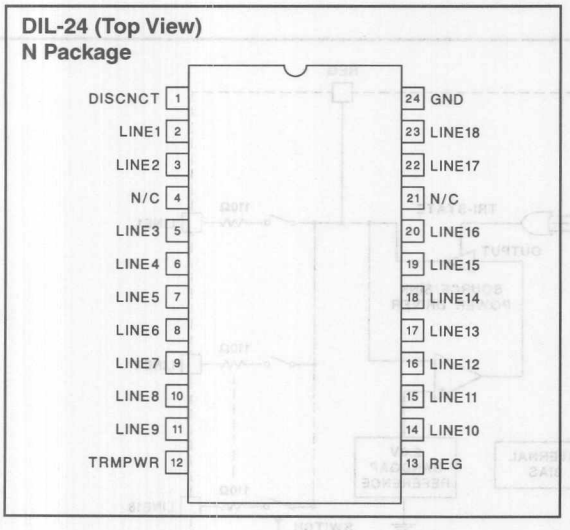
** DWP package pins 12 - 18 serve as both heatsink and signal ground.*

TSSOP-28 (Top View)
PWP Package

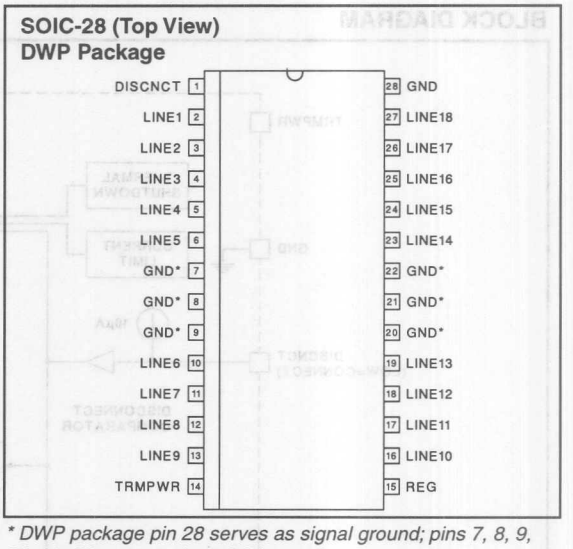


** PWP package pin 23 serves as signal ground; pins 7, 8, 9, 20, 21, and 22 serve as heatsink ground.*

DIL-24 (Top View)
N Package



SOIC-28 (Top View)
DWP Package



** DWP package pin 28 serves as signal ground; pins 7, 8, 9, 20, 21, 22 serve as heatsink/ground.*
Note: Drawings are not to scale.

ELECTRICAL CHARACTERISTICS Unless otherwise stated these specifications apply for T_A = 0°C to 70°C, TRMPWR = 4.75V, DISCNCT = 0V, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current Section					
Termpwr Supply Current	All termination lines = Open		1	2	mA
	All termination lines = 0.2V		420	440	mA
Power Down Mode	DISCNCT = TRMPWR		50	100	µA
Output Section (Termination Lines)					
Termination Impedance	See Figure 1	104.5	110	115.5	Ω
Output High Voltage	V_{TRMPWR} = 4V (Note 1)	2.6	2.8	3	V
Max Output Current	V_{LINE} = 0.2V, T_J = 25°C	–22.1	–23.3	–24	mA
	V_{LINE} = 0.2V	–20.7	–23.3	–24	mA
	V_{LINE} = 0.2V, TERMPWR = 4V, T_J = 25°C (Note 1)	–21	–23.3	–24	mA
	V_{LINE} = 0.2V, TRMPWR = 4V (Note 1)	–20	–23	–24	mA
	V_{LINE} = 0.5V			–22.4	mA
Output Leakage	DISCNCT = 2.4V, TRMPWR = 0V to 5.25V, REG = 0.2V, V_{LINE} = 5.25V		10	400	nA
Output Capacitance	DISCNCT = 2.4V (Note 2)		2	3.5	pF
Regulator Section					
Regulator Output Voltage		2.6	2.8	3	V
Drop Out Voltage	All Termination Lines = 0.2V		0.4	0.8	V
Short Circuit Current	V_{REG} = 0V	–475	–650	–850	mA
Sinking Current Capability	V_{REG} = 3.5V	200	400	800	mA
Thermal Shutdown			170		°C
Thermal Shutdown Hysteresis			10		°C
Disconnect Section					
Disconnect Threshold		0.8	1.5	2	V
Input Current	DISCNCT = 0V		–10	–30	µA

Note 1: Measuring each termination line while other 17 are low (0.2V).
Note 2: Guaranteed by design. Not 100% tested in production.

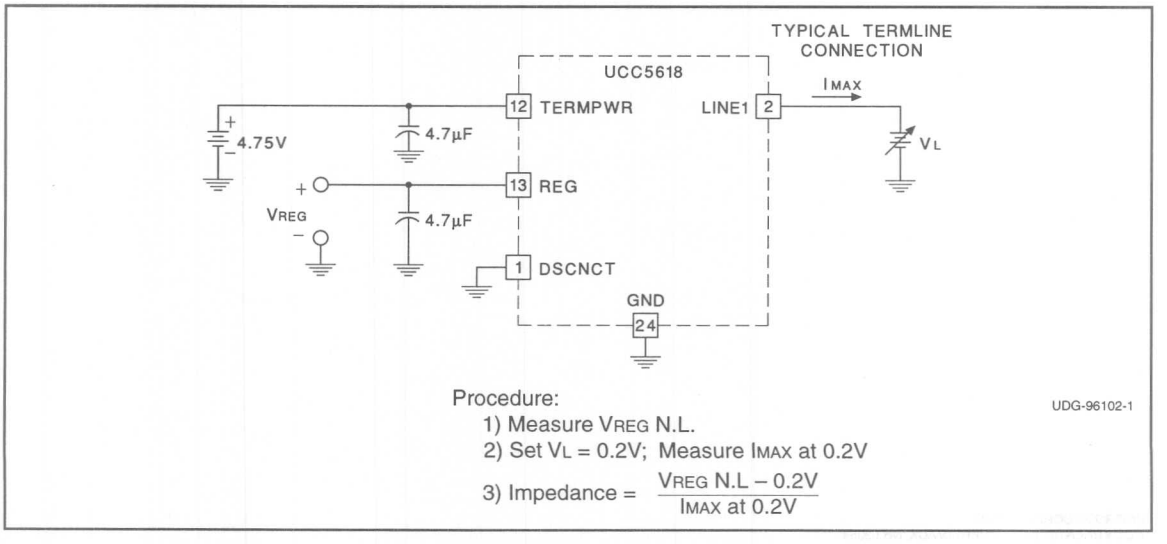


Figure 1. Termline Impedance Measurement Circuit

PIN DESCRIPTIONS

DISCNCT: Taking this pin high or leaving it open causes the 18 channels to become high impedance and the chip to go into low-power mode; a low state allows the channels to provide normal termination.

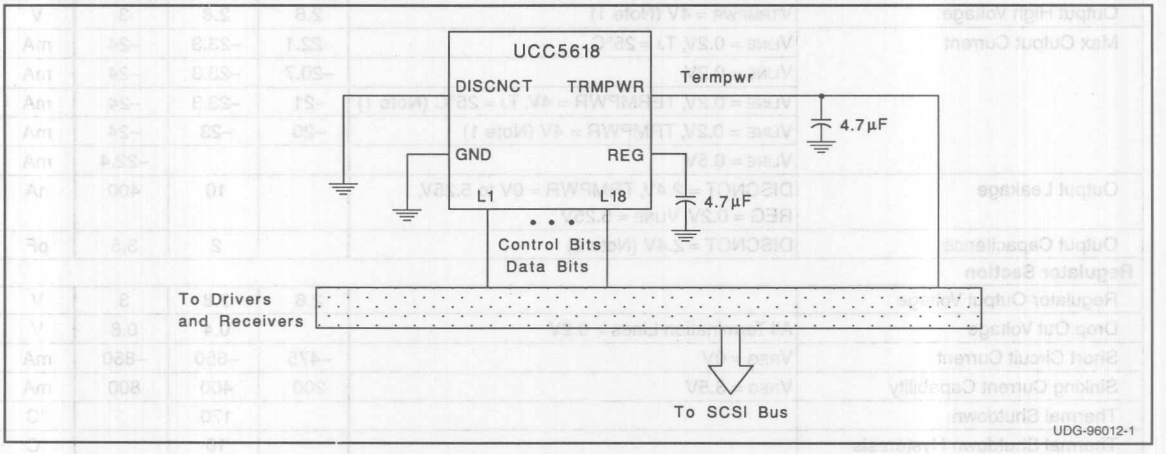
GND: Ground reference for the IC.

LINE1-18: 110 ohm termination channels.

REG: Output of the internal 2.8V regulator.

TRMPWR: Power for the IC.

APPLICATION INFORMATION



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27-Line SCSI Terminator With Reverse Disconnect

FEATURES

- Complies with SCSI, SCSI-2, SCSI-3 and FAST-20 (Ultra) Standards
- 2.5pF Channel Capacitance during Disconnect
- 100µA Supply Current in Disconnect Mode
- 4V To 7V Operation
- 110 Ohm Termination
- Completely Meets SCSI Hot Plugging
- –900mA Sourcing Current for Termination
- +500mA Sinking Current for Active Negation
- Logic Command Disconnects all Termination Lines
- Trimmed Impedance to 5%
- Current Limit and Thermal Shutdown Protection

DESCRIPTION

UCC5619 provides 27 lines of active termination for a SCSI (Small Computer Systems Interface) parallel bus. The SCSI standard recommends active termination at both ends of the cable.

The UCC5619 is ideal for high performance 5V SCSI systems. During disconnect the supply current is typically only 100µA, which makes the IC attractive for lower powered systems.

The UCC5619 is designed with a low channel capacitance of 2.5pF, which eliminates effects on signal integrity from disconnected terminators at interim points on the bus.

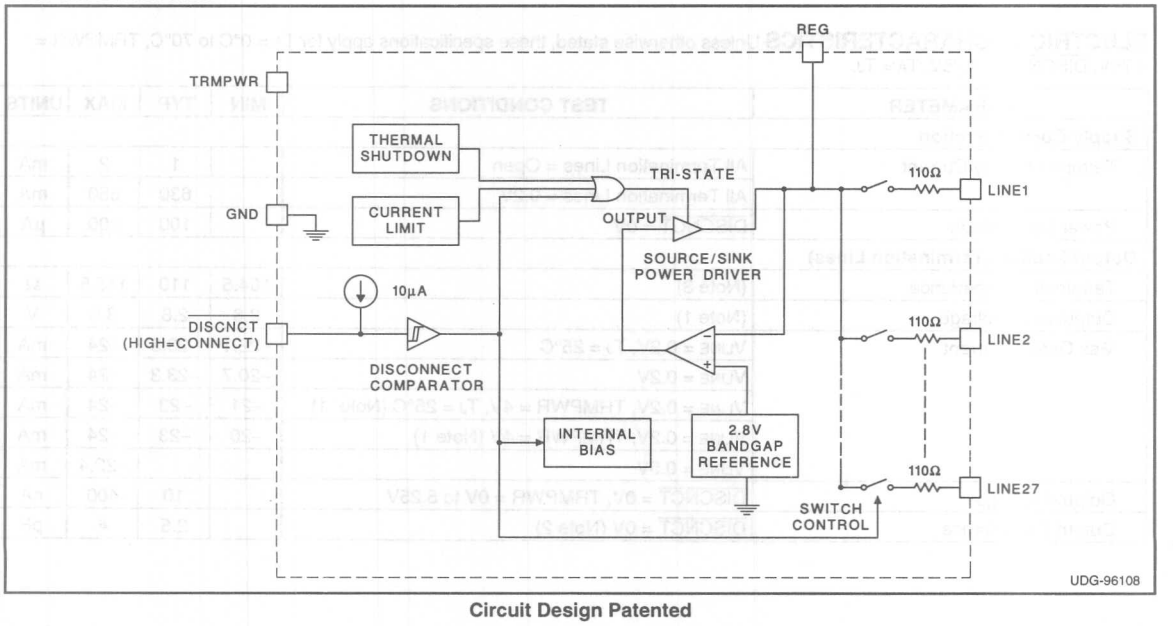
The power amplifier output stage allows the UCC5619 to source full termination current and sink active negation current when all termination lines are actively negated.

The UCC5619, as with all Unitrode terminators, is completely hot pluggable and appears as high impedance at the teminating channels with V_{TRMPWR} = 0V or open.

Internal circuit trimming is utilized, first to trim the 110Ω impedance, and then most importantly, to trim the output current as close to the maximum SCSI-3 specification as possible, which maximizes noise margin in fast SCSI operation.

Consult SSOP-36 Packaging Diagram for exact dimensions.

BLOCK DIAGRAM



Circuit Design Patented

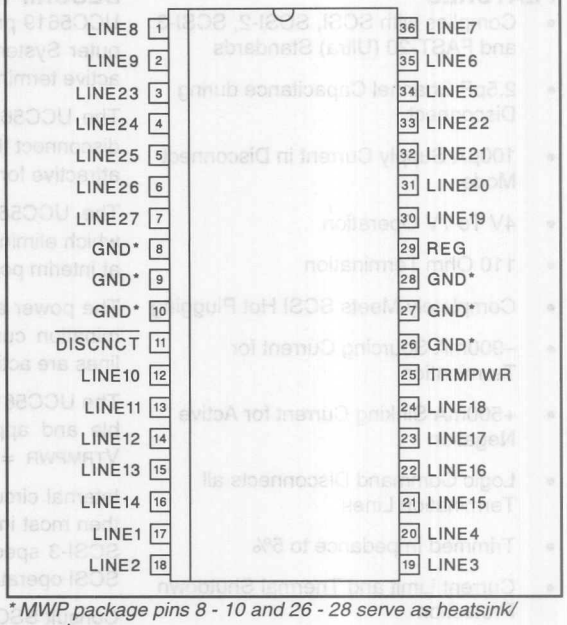
ABSOLUTE MAXIMUM RATINGS

Termpwr Voltage ..... +7V
Signal Line Voltage..... 0V to +7V
Regulator Output Current 1.5A
Storage Temperature ..... –65°C to +150°C
Junction Temperature..... –55°C to +150°C
Lead Temperature (Soldering, 10 Sec.)..... +300°C

Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

SSOP-36 (Top View)
MWP Package



** MWP package pins 8 - 10 and 26 - 28 serve as heatsink/ground.*

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C, TRMPWR = 4.75V, $\overline{\text{DISCNCT}}$ = 4.75V, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current Section					
Termpwr Supply Current	All Termination Lines = Open		1	2	mA
	All Termination Lines = 0.2V		630	650	mA
Power Down Mode	$\overline{\text{DISCNCT}}$ = 0V		100	200	µA
Output Section (Termination Lines)					
Termination Impedance	(Note 3)	104.5	110	115.5	Ω
Output High Voltage	(Note 1)	2.6	2.8	3.0	V
Max Output Current	V_{LINE} = 0.2V, T_J = 25°C	–22.1	–23.3	–24	mA
	V_{LINE} = 0.2V	–20.7	–23.3	–24	mA
	V_{LINE} = 0.2V, TRMPWR = 4V, T_J = 25°C (Note 1)	–21	–23	–24	mA
	V_{LINE} = 0.2V, TRMPWR = 4V (Note 1)	–20	–23	–24	mA
	V_{LINE} = 0.5V			–22.4	mA
Output Leakage	$\overline{\text{DISCNCT}}$ = 0V, TRMPWR = 0V to 5.25V		10	400	nA
Output Capacitance	$\overline{\text{DISCNCT}}$ = 0V (Note 2)		2.5	4	pF

ELECTRICAL CHARACTERISTICS (cont.) Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C, TRMPWR = 4.75V, DISCNCT = 4.75V, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Regulator Section					
Regulator Output Voltage		2.6	2.8	3.0	V
Drop Out Voltage	All Termination Lines = 0.2V		0.4	0.8	V
Short Circuit Current	V_{REG} = 0V	–650	–900	–1300	mA
Sinking Current Capability	V_{REG} = 3.5V	300	500	900	mA
Thermal Shutdown			170		°C
Thermal Shutdown Hysteresis			10		°C
Disconnect Section					
Disconnect Threshold		0.8	1.5	2.0	V
Input Current	$\overline{DISCNCT}$ = 0V		–20	–60	µA

Note 1: Measuring each termination line while other 26 are low (0.2V).
Note 2: Guaranteed by design. Not 100% tested in production.
Note 3: Tested by measuring I_{OUT} with V_{OUT} = 0.2V and V_{OUT} with no load, then calculate :

$$Z = \frac{V_{OUT}\ \text{N.L.} - 0.2V}{I_{OUT}\ \text{at}\ 0.2V}$$

PIN DESCRIPTIONS

DISCNCT: Taking this pin low causes all channels to become high impedance, and the chip to go into low-power mode; a high state or leaving it open allows the channels to provide normal termination.

GND: Ground reference for the IC.

LINE1 - 27: 110Ω termination channels.

REG: Output of the internal 2.7V regulator.

TRMPWR: Power for the IC.

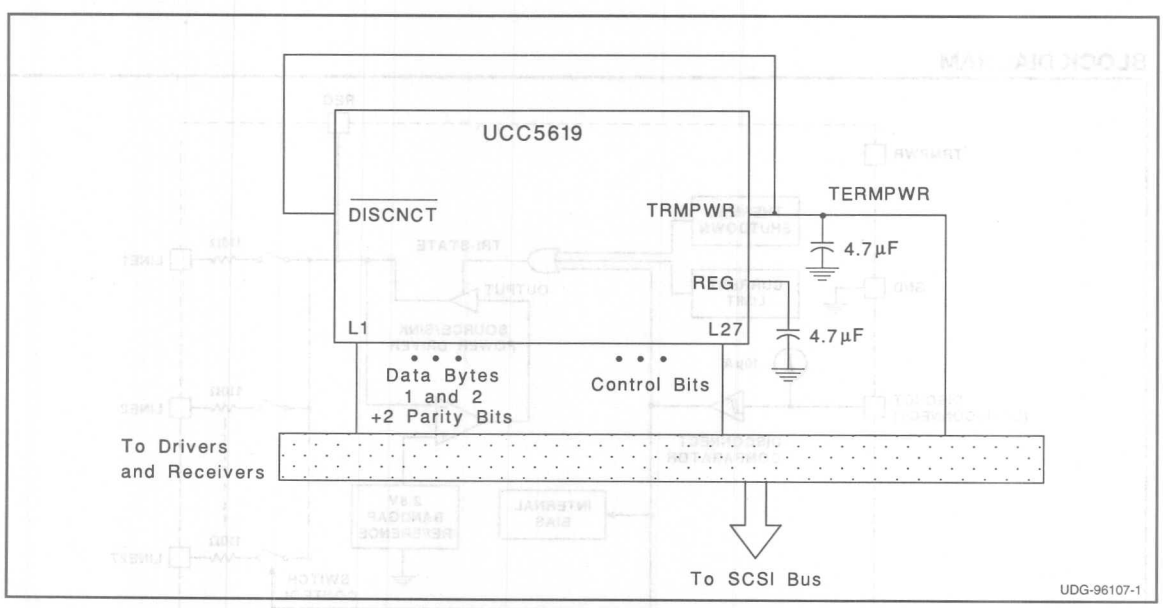


Figure 1. Typical Wide SCSI Bus Configuration Using the UCC5619

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27-Line SCSI Terminator

FEATURES

- Complies with SCSI, SCSI-2, SCSI-3 and FAST-20 (Ultra) Standards
- 2.5pF Channel Capacitance during Disconnect
- 100µA Supply Current in Disconnect Mode
- 4V To 7V Operation
- 110 Ohm Termination
- Completely Meets SCSI Hot Plugging
- –900mA Sourcing Current for Termination
- +500mA Sinking Current for Active Negation
- Logic Command Disconnects all Termination Lines
- Trimmed Impedance to 5%
- Current Limit and Thermal Shutdown Protection

DESCRIPTION

UCC5620 provides 27 lines of active termination for a SCSI (Small Computer Systems Interface) parallel bus. The SCSI standard recommends active termination at both ends of the cable.

The UCC5620 is ideal for high performance 5V SCSI systems. During disconnect the supply current is typically only 100µA, which makes the IC attractive for lower powered systems.

The UCC5620 is designed with a low channel capacitance of 2.5pF, which eliminates effects on signal integrity from disconnected terminators at interim points on the bus.

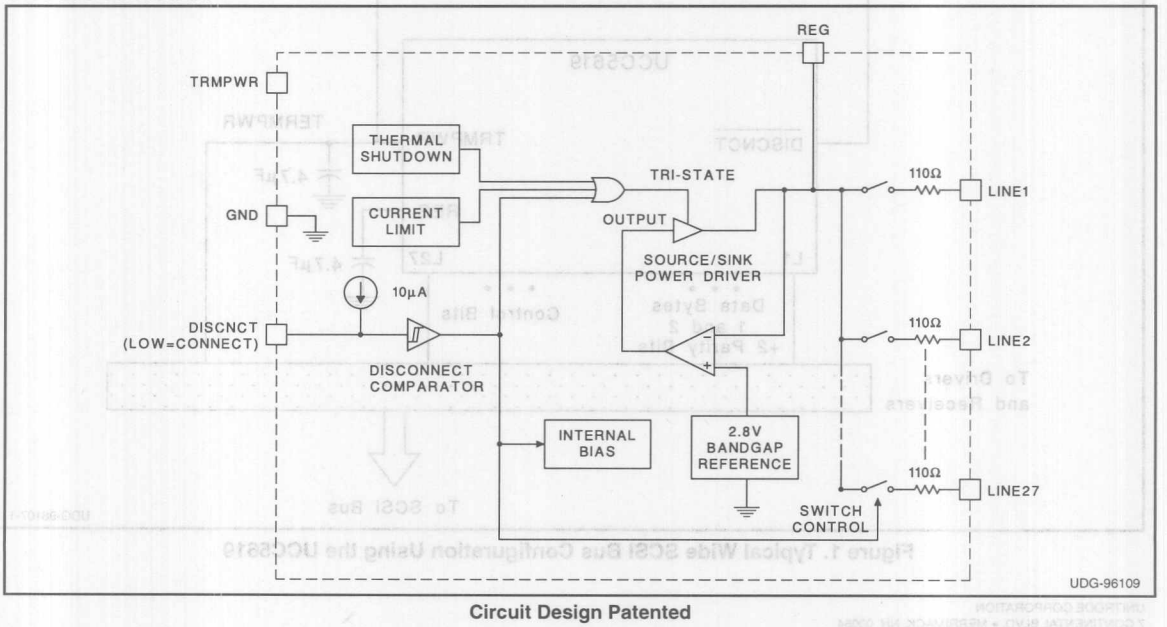
The power amplifier output stage allows the UCC5620 to source full termination current and sink active negation current when all termination lines are actively negated.

The UCC5620, as with all Unitrode terminators, is completely hot pluggable and appears as high impedance at the teminating channels with V_{TRMPWR} = 0V or open.

Internal circuit trimming is utilized, first to trim the 110Ω impedance, and then most importantly, to trim the output current as close to the maximum SCSI-3 specification as possible, which maximizes noise margin in fast SCSI operation.

Consult SSOP-36 Packaging Diagram for exact dimensions.

BLOCK DIAGRAM



Circuit Design Patented

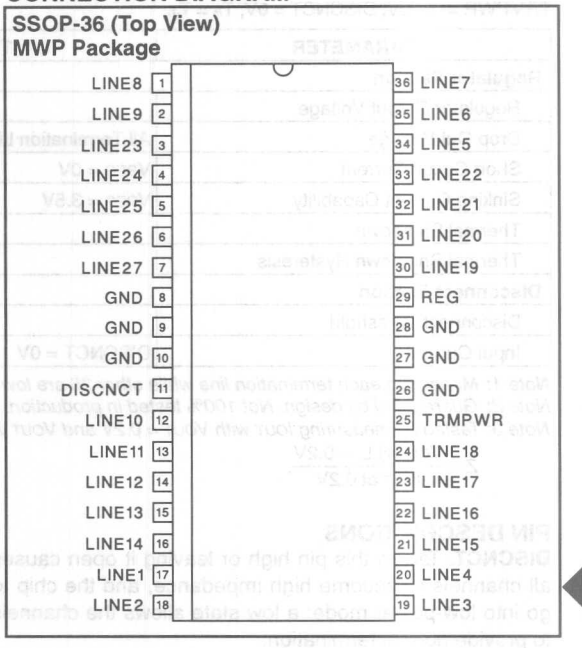
ABSOLUTE MAXIMUM RATINGS

Termpwr Voltage ..... +7V
Signal Line Voltage..... 0V to +7V
Regulator Output Current 1.5A
Storage Temperature ..... –65°C to +150°C
Junction Temperature..... –55°C to +150°C
Lead Temperature (Soldering, 10 Sec.)..... +300°C

Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

SSOP-36 (Top View)
MWP Package



ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C, TRMPWR = 4.75V, DISCNCT = 0V, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current Section					
Termpwr Supply Current	All Termination Lines = Open		1	2	mA
	All Termination Lines = 0.2V		630	650	mA
Power Down Mode	DISCNCT = Termpwr		100	200	µA
Output Section (Termination Lines)					
Termination Impedance	(Note 3)	104.5	110	115.5	Ω
Output High Voltage	(Note 1)	2.6	2.8	3.0	V
Max Output Current	V_{LINE} = 0.2V, T_J = 25°C	–22.1	–23.3	–24	mA
	V_{LINE} = 0.2V	–20.7	–23.3	–24	mA
	V_{LINE} = 0.2V, TRMPWR = 4V, T_J = 25°C (Note 1)	–21	–23	–24	mA
	V_{LINE} = 0.2V, TRMPWR = 4V (Note 1)	–20	–23	–24	mA

ELECTRICAL CHARACTERISTICS (cont.) Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C, TRMPWR = 4.75V, DISCNCT = 0V, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Regulator Section					
Regulator Output Voltage		2.6	2.8	3.0	V
Drop Out Voltage	All Termination Lines = 0.2V		0.4	0.8	V
Short Circuit Current	V_{REG} = 0V	–650	–900	–1300	mA
Sinking Current Capability	V_{REG} = 3.5V	300	500	900	mA
Thermal Shutdown			170		°C
Thermal Shutdown Hysteresis			10		°C
Disconnect Section					
Disconnect Threshold		0.8	1.5	2.0	V
Input Current	DISCNCT = 0V		–20	–60	µA

Note 1: Measuring each termination line while other 26 are low (0.2V).
Note 2: Guaranteed by design. Not 100% tested in production.
Note 3: Tested by measuring I_{OUT} with V_{OUT} = 0.2V and V_{OUT} with no load, then calculate:

$$Z = \frac{V_{OUT}\ \text{N.L.} - 0.2V}{I_{OUT}\ \text{at}\ 0.2V}.$$

PIN DESCRIPTIONS

DISCNCT: Taking this pin high or leaving it open causes all channels to become high impedance, and the chip to go into low-power mode; a low state allows the channels to provide normal termination.

GND: Ground reference for the IC.

LINE1 - 27: 110Ω termination channels.

REG: Output of the internal 2.7V regulator.

TRMPWR: Power for the IC.

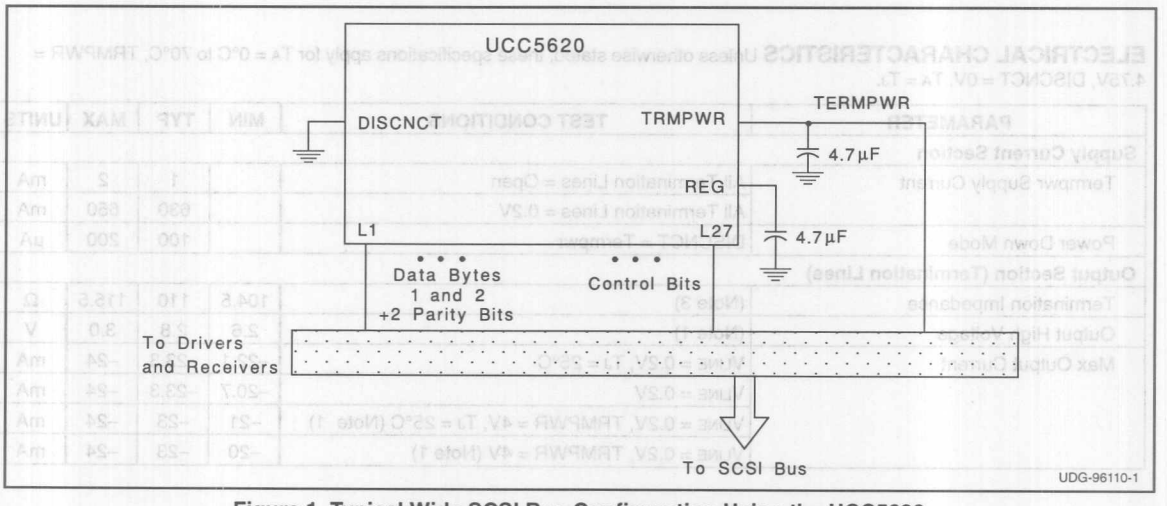


Figure 1. Typical Wide SCSI Bus Configuration Using the UCC5620

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27 - Line SCSI Terminator With Split Reverse Disconnect

FEATURES

- Complies with SCSI, SCSI-2, SCSI-3 and FAST-20 (Ultra) Standards
- 2.5pF Channel Capacitance During Disconnect
- 100µA Supply Current in Disconnect Mode
- 4V To 7V Operation
- 110Ω Termination
- Completely Meets SCSI Hot Plugging
- –900mA Sourcing Current for Termination
- +500mA Sinking Current for Active Negation
- Logic Command Disconnects all Termination Lines
- Split Reverse Controls Lines 1 to 9 and 10 to 27 Separately
- Trimmed Impedance to 5%
- Current Limit and Thermal Shutdown Protection

DESCRIPTION

UCC5621 provides 27 lines of active termination for a SCSI (Small Computer Systems Interface) parallel bus. The SCSI standard recommends active termination at both ends of the cable.

The UCC5621 is ideal for high performance 5V SCSI systems. During disconnect the supply current is typically only 100µA, which makes the IC attractive for lower powered systems.

The UCC5621 features a split reverse disconnect allowing the user to control termination lines 10 to 27 with disconnect one, $\overline{\text{DISCNCT1}}$, and control terminiation lines 1 to 9 with disconnect two, $\overline{\text{DISCNCT2}}$.

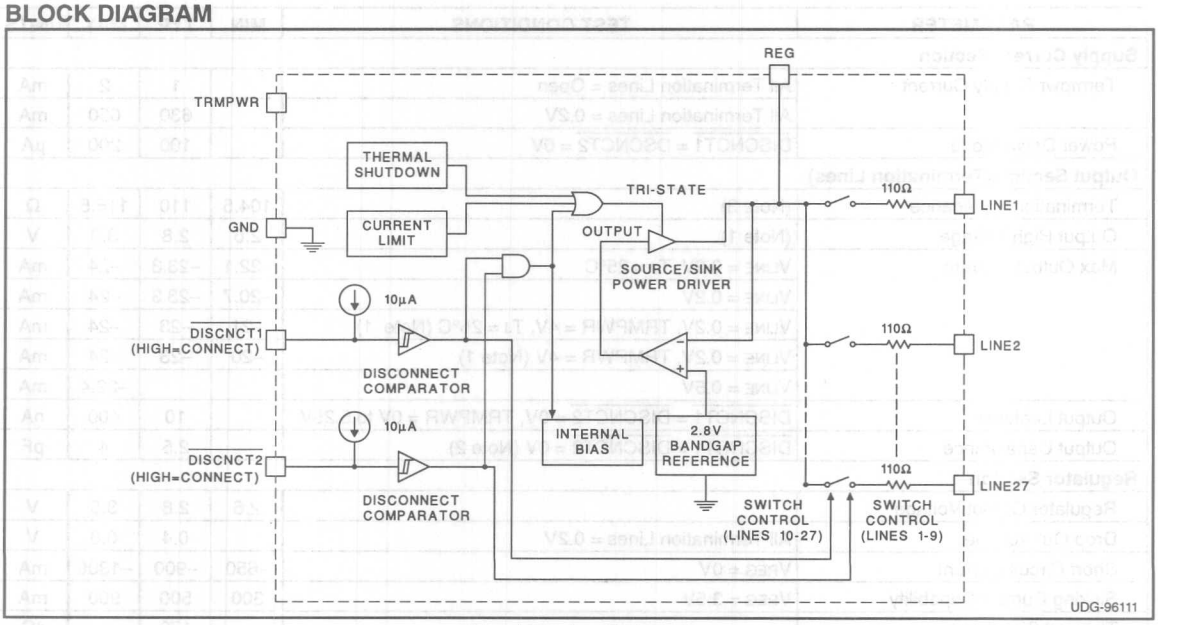
The UCC5621 is designed with a low channel capacitance of 2.5pF, which eliminates effects on signal integrity from disconnected terminators at interim points on the bus.

The power amplifier output stage allows the UCC5621 to source full termination current and sink active negation current when all termination lines are actively negated.

The UCC5621, as with all Unitrode terminators, is completely hot pluggable and appears as high impedance at the teminating channels with V_{TRMPWR} = 0V or open.

continued

BLOCK DIAGRAM



Circuit Design Patented

12/96

DESCRIPTION (cont.)

Internal circuit trimming is utilized, first to trim the 110Ω impedance, and then most importantly, to trim the output current as close to the maximum SCSI-3 specification as possible, which maximizes noise margin in FAST-20 SCSI operation.

Other features include thermal shutdown and current limit. This device is offered in low thermal resistance versions of the industry standard 44 pin wide body SSOP (MWP). Consult SSOP-44 Packaging Diagram for exact dimensions.

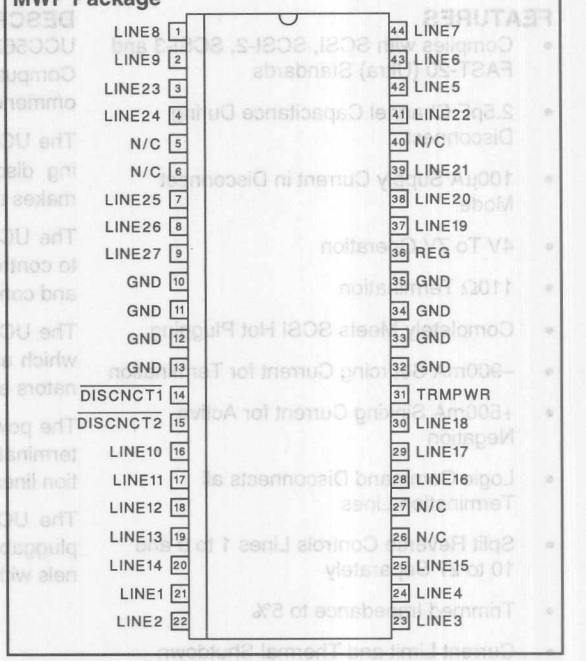
ABSOLUTE MAXIMUM RATINGS

Termpwr Voltage . . . . . +7V
Signal Line Voltage . . . . . 0V to +7V
Regulator Output Current 1.5A
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 Sec.) . . . . . +300°C

Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

SSOP-44 (Top View)
MWP Package



ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C, TRMPWR = 4.75V, $\overline{\text{DISCNCT1}}$ = $\overline{\text{DSCNCT2}}$ = 4.75V, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current Section					
Termpwr Supply Current	All Termination Lines = Open		1	2	mA
	All Termination Lines = 0.2V		630	650	mA
Power Down Mode	$\overline{\text{DISCNCT1}}$ = $\overline{\text{DSCNCT2}}$ = 0V		100	200	µA
Output Section (Termination Lines)					
Termination Impedance	(Note 3)	104.5	110	115.5	Ω
Output High Voltage	(Note 1)	2.6	2.8	3.0	V
Max Output Current	V_{LINE} = 0.2V, T_J = 25°C	–22.1	–23.3	–24	mA
	V_{LINE} = 0.2V	–20.7	–23.3	–24	mA
	V_{LINE} = 0.2V, TRMPWR = 4V, T_J = 25°C (Note 1)	–21	–23	–24	mA
	V_{LINE} = 0.2V, TRMPWR = 4V (Note 1)	–20	–23	–24	mA
	V_{LINE} = 0.5V			–22.4	mA
Output Leakage	$\overline{\text{DISCNCT1}}$ = $\overline{\text{DISCNCT2}}$ = 0V, TRMPWR = 0V to 5.25V		10	400	nA
Output Capacitance	$\overline{\text{DISCNCT1}}$ = $\overline{\text{DISCNCT2}}$ = 0V (Note 2)		2.5	4	pF
Regulator Section					
Regulator Output Voltage		2.6	2.8	3.0	V
Drop Out Voltage	All Termination Lines = 0.2V		0.4	0.8	V
Short Circuit Current	V_{REG} = 0V	–650	–900	–1300	mA
Sinking Current Capability	V_{REG} = 3.5V	300	500	900	mA
Thermal Shutdown			170		°C
Thermal Shutdown Hysteresis			10		°C

ELECTRICAL CHARACTERISTICS (cont.) Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C, TRMPWR = 4.75V, $\overline{DISCNCT1}$ = $\overline{DISCNCT2}$ = 4.7V, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Disconnect Section					
Disconnect Threshold $\overline{DISCNCT1}$	Controls Lines 10 to 27	0.8	1.5	2.0	V
Input Current $\overline{DISCNCT1}$	$\overline{DISCNCT1}$ = 0V		–10	–30	µA
Disconnect Threshold $\overline{DISCNCT2}$	Controls Lines 1 to 9	0.8	1.5	2	V
Input Current $\overline{DISCNCT2}$	$\overline{DISCNCT2}$ = 0V		–10	–30	µA

Note 1: Measuring each termination line while other 26 are low (0.2V).
Note 2: Guaranteed by design. Not 100% tested in production.
Note 3: Tested by measuring I_{OUT} with V_{OUT} = 0.2V and V_{OUT} with no load, then calculate:

$$Z = \frac{V_{OUT}\ N.L. - 0.2V}{I_{OUT}\ at\ 0.2V}.$$

PIN DESCRIPTIONS

$\overline{DISCNCT1}$: Disconnect one controls termination lines 10 – 27. Taking this pin low causes termination lines 10 – 27 to become high impedence, taking this pin high or leaving it open allows the channels to provide normal termination.

$\overline{DISCNCT2}$: Disconnect two controls termination lines 1 – 9. Taking this pin low causes termination lines 1 – 9 to become high impedence. Taking this pin high or leaving it open allows the channels to provide normal terminiation. Taking both disconnect pins low will put the chip in to sleep mode where it will be in low-power mode.

GND: Ground reference for the IC.

LINE1 - 27: 110Ω termination channels.

REG: Output of the internal 2.7V regulator.

TRMPWR: Power for the IC.

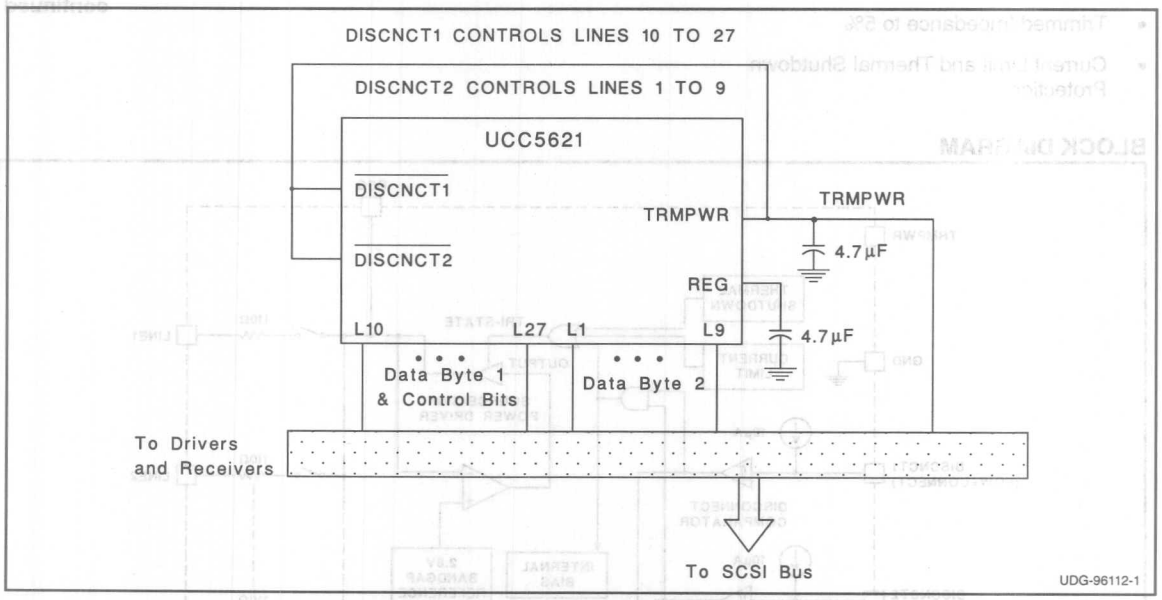


Figure 1. Typical Wide SCSI Bus Configuration Using the UCC5621

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

27 - Line SCSI Terminator With Split Disconnect

FEATURES

- Complies with SCSI, SCSI-2, SCSI-3 and FAST-20 (Ultra) Standards
- 2.5pF Channel Capacitance During Disconnect
- 100µA Supply Current in Disconnect Mode
- 4V To 7V Operation
- 110Ω Termination
- Completely Meets SCSI Hot Plugging
- –900mA Sourcing Current for Termination
- +500mA Sinking Current for Active Negation
- Logic Command Disconnects all Termination Lines
- Split Disconnect Controls Lines 1 to 9 and 10 to 27 Separately
- Trimmed Impedance to 5%
- Current Limit and Thermal Shutdown Protection

DESCRIPTION

The UCC5622 provides 27 lines of active termination for a SCSI (Small Computer Systems Interface) parallel bus. The SCSI standard recommends active termination at both ends of the cable.

The UCC5622 is ideal for high performance 5V SCSI systems. During disconnect the supply current is typically only 100µA, which makes the IC attractive for lower powered systems.

The UCC5622 features a split disconnect allowing the user to control termination lines 10 to 27 with disconnect one, DISCNCT1, and control terminiation lines 1 to 9 with disconnect two, DISCNCT2.

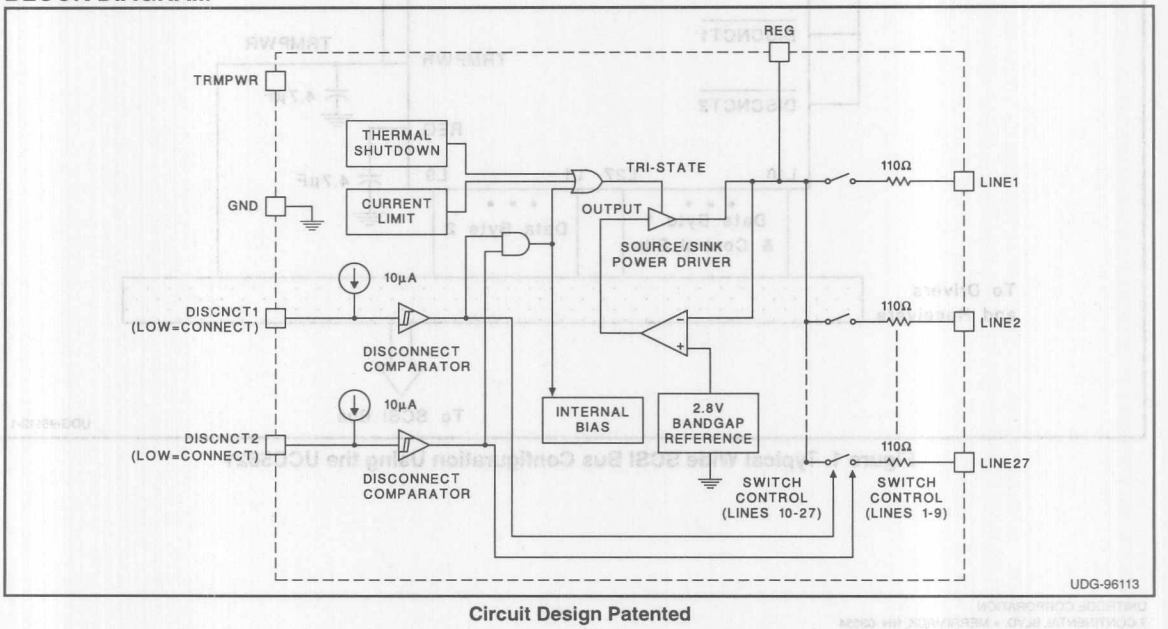
The UCC5622 is designed with a low channel capacitance of 2.5pF, which eliminates effects on signal integrity from disconnected terminators at interim points on the bus.

The power amplifier output stage allows the UCC5622 to source full termination current and sink active negation current when all termination lines are actively negated.

The UCC5622, as with all Unitrode terminators, is completely hot pluggable and appears as high impedance at the teminating channels with V_{TRMPWR} = 0V or open.

continued

BLOCK DIAGRAM



Circuit Design Patented

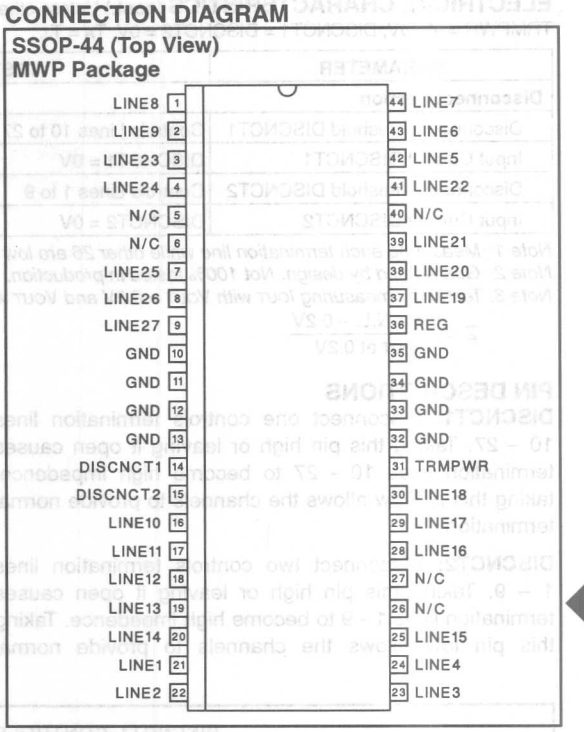
DESCRIPTION (cont.)

Internal circuit trimming is utilized, first to trim the 110Ω impedance, and then most importantly, to trim the output current as close to the maximum SCSI-3 specification as possible, which maximizes noise margin in FAST-20 SCSI operation.

Other features include thermal shutdown and current limit. This device is offered in low thermal resistance versions of the industry standard 44 pin wide body SSOP (MWP). Consult SSOP-44 Packaging Diagram for exact dimensions.

CONNECTION DIAGRAM

SSOP-44 (Top View)
MWP Package



ABSOLUTE MAXIMUM RATINGS

Termpwr Voltage . . . . . +7V
Signal Line Voltage. . . . . 0V to +7V
Regulator Output Current 1.5A
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature. . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 Sec.) . . . . . +300°C

Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C, TRMPWR = 4.75V, DISCNCT1 = DSCNCT2 = 0V, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current Section					
Termpwr Supply Current	All Termination Lines = Open		1	2	mA
	All Termination Lines = 0.2V		630	650	mA
Power Down Mode	DISCNCT1 = DSCNCT2 = TRMPWR		100	200	µA
Output Section (Termination Lines)					
Termination Impedance	(Note 3)	104.5	110	115.5	Ω
Output High Voltage	(Note 1)	2.6	2.8	3.0	V
Max Output Current	V_{LINE} = 0.2V, T_J = 25°C	–22.1	–23.3	–24	mA
	V_{LINE} = 0.2V	–20.7	–23.3	–24	mA
	V_{LINE} = 0.2V, TRMPWR = 4V, T_J = 25°C (Note 1)	–21	–23	–24	mA
	V_{LINE} = 0.2V, TRMPWR = 4V (Note 1)	–20	–23	–24	mA
	V_{LINE} = 0.5V			–22.4	mA
Output Leakage	DISCNCT1 = DISCNCT2 = 2.4V, TRMPWR = 0V to 5.25V		10	400	nA
Output Capacitance	DISCNCT1 = DISCNCT2 = 2.4V (Note 2)		2.5	4	pF
Regulator Section					
Regulator Output Voltage		2.6	2.8	3.0	V
Drop Out Voltage	All Termination Lines = 0.2V		0.4	0.8	V
Short Circuit Current	V_{REG} = 0V	–650	–900	–1300	mA
Sinking Current Capability	V_{REG} = 3.5V	300	500	900	mA
Thermal Shutdown			170		°C
Thermal Shutdown Hysteresis			10		°C

ELECTRICAL CHARACTERISTICS (cont.) Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C, TRMPWR = 4.75V, DISCNCT1 = DISCNCT2 = 0V, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Disconnect Section					
Disconnect Threshold DISCNCT1	Controls Lines 10 to 27	0.8	1.5	2.0	V
Input Current DISCNCT1	DISCNCT1 = 0V		–10	–30	µA
Disconnect Threshold DISCNCT2	Controls Lines 1 to 9	0.8	1.5	2	V
Input Current DISCNCT2	DISCNCT2 = 0V		–10	–30	µA

Note 1: Measuring each termination line while other 26 are low (0.2V).
Note 2: Guaranteed by design. Not 100% tested in production.
Note 3: Tested by measuring I_{OUT} with V_{OUT} = 0.2V and V_{OUT} with no load, then calculate:

$$Z = \frac{V_{OUT}\ \text{N.L.} - 0.2V}{I_{OUT}\ \text{at}\ 0.2V}.$$

PIN DESCRIPTIONS

DISCNCT1: Disconnect one controls termination lines 10 – 27. Taking this pin high or leaving it open causes termination lines 10 - 27 to become high impedence, taking this pin low allows the channels to provide normal termination.

DISCNCT2: Disconnect two controls termination lines 1 – 9. Taking this pin high or leaving it open causes termination lines 1 - 9 to become high impedence. Taking this pin low allows the channels to provide normal terminiation. Taking both disconnect pins high or leaving them open will put the chip in to sleep mode where it will be in low-power mode.

GND: Ground reference for the IC.

LINE1 - 27: 110Ω termination channels.

REG: Output of the internal 2.7V regulator.

TRMPWR: Power for the IC.

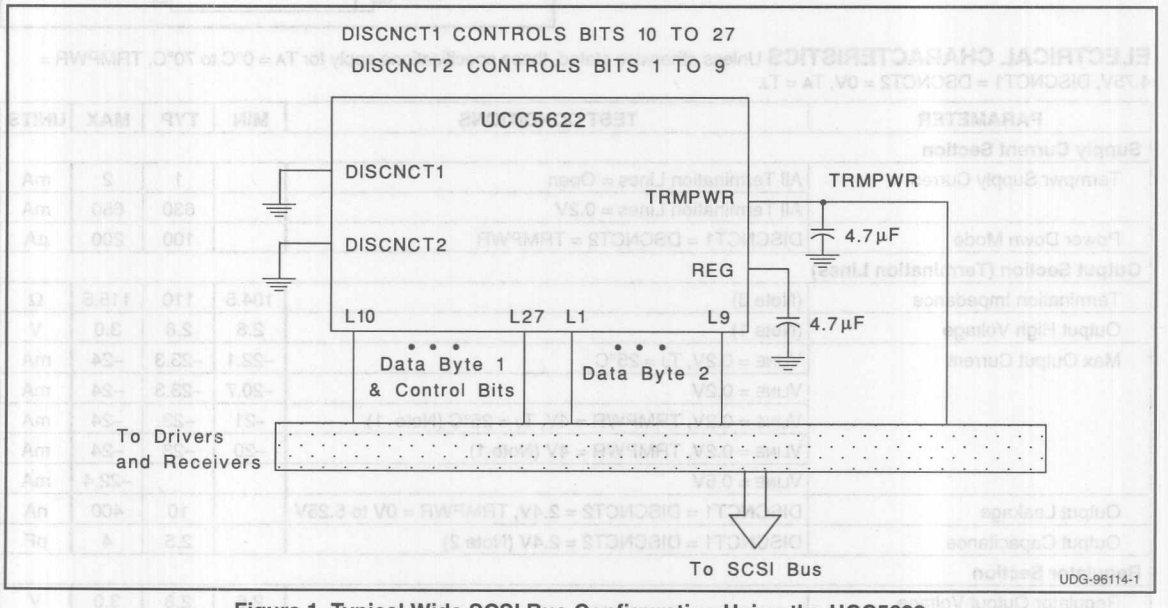


Figure 1. Typical Wide SCSI Bus Configuration Using the UCC5622

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL: (603) 424-2410 • FAX (603) 424-3460

Low Voltage Differential (LVD/SE) SCSI 9 Line Terminator

FEATURES

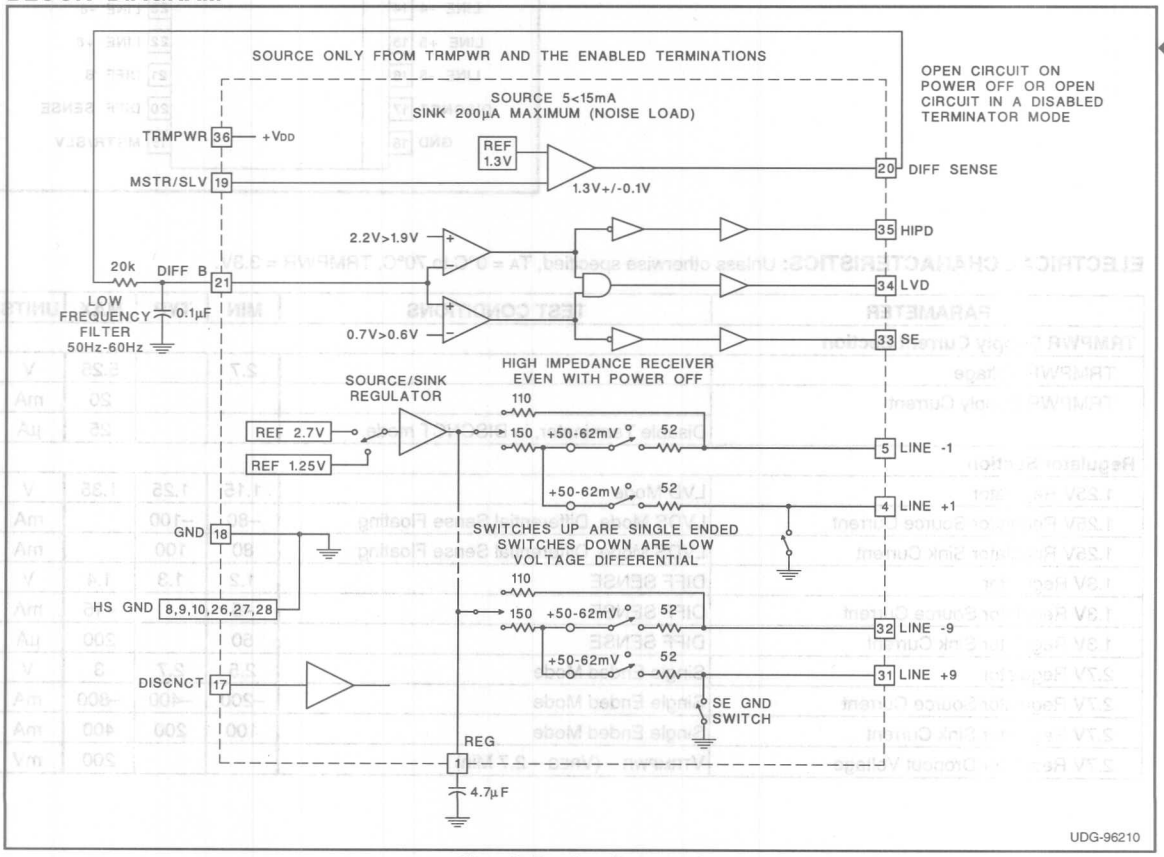
- Auto Selection Multi-Mode Single Ended or Low Voltage Differential Termination
- 2.7V to 5.25V Operation
- Differential Failsafe Bias
- Thermal Packaging for Low Junction Temperature and Better MTBF
- Master/Slave Inputs
- Supports Active Negation
- Standby (Disable Mode) 5µA
- 3pF Channel Capacitance

DESCRIPTION

The UCC5630 Multi-Mode Low Voltage Differential and Single Ended Terminator is both a single ended terminator and a low voltage differential terminator for the transition to the next generation SCSI Parallel Interface (SPI-2). The low voltage differential is a requirement for the higher speeds at a reasonable cost and is the only way to have adequate skew budgets. The transceivers can be incorporated into the controller, unlike SCSI high power differential (EIA485) which requires external transceivers. Low Voltage differential is specified for FAST-40 and FAST-80, but has the potential of speeds up to FAST-320. The UCC5630 is SPI-2 compliant and SPI and FAST-20 compatible. Consult SSOP-36 Package Diagram for exact dimensions.

The UCC5630 can not be used with SCSI high voltage differential (HVD) EIA485. It will shut down when it sees high power differential to protect the bus. The pinning for high power differential is not the same as LVD or single ended and the bias voltage, current and power are also different for EIA485 differential.

BLOCK DIAGRAM



Circuit Design Patented

ABSOLUTE MAXIMUM RATINGS

TRMPWR Voltage 6V
Signal Line Voltage..... 0V to TRMPWR
Package Power Dissipation 2W
Storage Temperature ..... –65°C to +150°C
Junction Temperature ..... –55°C to +150°C
Lead Temperature (Soldering, 10sec.) ..... +300°C

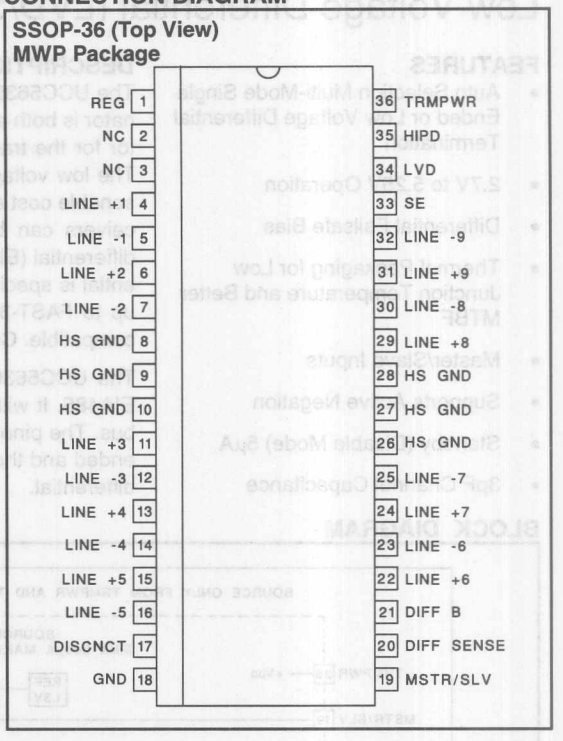
All voltages are with respect to respect to pin 1. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of the Databook for thermal limitations and considerations of packages.

RECOMMENDED OPERATING CONDITIONS

TRMPWR Voltage ..... 2.7V TO 5.25V

CONNECTION DIAGRAM

SSOP-36 (Top View)
MWP Package



ELECTRICAL CHARACTERISTICS: Unless otherwise specified, T_A = 0°C to 70°C, TRMPWR = 3.3V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
TRMPWR Supply Current Section					
TRMPWR Voltage		2.7		5.25	V
TRMPWR Supply Current				20	mA
	Disable Terminator, in DISCNCT mode.			25	µA
Regulator Section					
1.25V Regulator	LVD Mode	1.15	1.25	1.35	V
1.25V Regulator Source Current	LVDS Mode, Differential Sense Floating	–80	–100		mA
1.25V Regulator Sink Current	LVDS Mode, Differential Sense Floating	80	100		mA
1.3V Regulator	DIFF SENSE	1.2	1.3	1.4	V
1.3V Regulator Source Current	DIFF SENSE	–5		–15	mA
1.3V Regulator Sink Current	DIFF SENSE	50		200	µA
2.7V Regulator	Single Ended Mode	2.5	2.7	3	V
2.7V Regulator Source Current	Single Ended Mode	–200	–400	–800	mA
2.7V Regulator Sink Current	Single Ended Mode	100	200	400	mA
2.7V Regulator Dropout Voltage	V_{TRMPWR} – (V_{REG} – 2.7 Min)			200	mV

ELECTRICAL CHARACTERISTICS (cont.): Unless otherwise specified, T_A = 0°C to 70°C, TRMPWR = 3.3V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Differential Termination Section					
Differential Impedance		100	105	110	Ω
Common Mode Impedance		105	122	140	Ω
Differential Bias Voltage	Drivers Tri-stated	100		125	mV
Common Mode Bias			1.25		V
Output Capacitance	Single Ended Measurement to Ground (Note 1)			3	pF
Single Ended Termination Section					
Impedance		102.3	110	117.7	Ω
Termination Current	Signal Level 0.2V	–21	–23	–25.4	mA
	Signal Level 0.5V			–22.4	mA
Output Leakage	Disabled, TRMPWR = 0V to 5.25V			400	nA
Output Capacitance	Single Ended Measurement to Ground (Note 1)			3	pF
Single Ended GND SW Impedance				60	Ω
Disconnect (DISCNCT) Input Section					
DISCNCT Threshold		0.8		2.0	V
DISCNCT Input Current	$V_{DISCNCT}$ = 0V and 3.3V	–30		30	µA
Differential Sense (DIFF B) Input Sections					
DIFF B Single Ended Threshold		0.6		0.7	V
DIFF B Sense LVDS Threshold		1.9		2.2	V
DIFF B Input Current	$V_{DIFF\ B}$ = 0V and 3.3V	–30		30	µA
Master/Slave (MSTR/SLV) Input Section					
MSTR/SLV Threshold		0.8		2	V
MSTR/SLV Input Current		–30		30	µA
Status Bits (SE, LVD, HIPD) Output Section					
I_{SOURCE}	V_{LOAD} = 2.4V	–4	–8.7		mA
I_{SINK}	V_{LOAD} = 0.5V	3	6		mA
	V_{LOAD} = 0.4V	2	5		mA

Note 1: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

DIFF B: DIFF SENSE filter pin should be connected to a 0.1µF capacitor to GND and 20k resistor to SCSI/Bus DIFF SENSE Line.

DIFF SENSE: The SCSI bus DIFF SENSE line is driven to 1.3V to detect what type of devices are connected to the SCSI bus.

DISCNCT: Disconnect shuts down the terminator when it is not at the ended of the bus. The disconnect pin low enables the terminator.

HIPD: TTL compatible status bit indicating high voltage differential has been detected on DIFF B. The terminator is in shutdown.

HS GND: Heat Sink GND. Connect to large area PC board traces to increase power dissipation capability.

GND: Power Supply Return.

LINE -1 thru -9: Signal line/active line for single ended or negative line in differential applications for the SCSI bus.

LINE +1 thru +9: Ground line for single ended or positive line for differential applications for the SCSI bus.

LVD: TTL compatible status bit indicating low voltage differential level on DIFF B. The terminator is in LVD mode.

MSTR/SLV: Mode select for the non-controlling terminator. MSTR enables the 1.3V regulator.

REG: Regulator bypass, must be connected to a 4.7µF capacitor.

SE: TTL compatible status bit indicating single ended device has been detected on DIFF B. The terminator is in single ended mode.

TRMPWR: V_{IN} 2.7V to 5.25V supply.

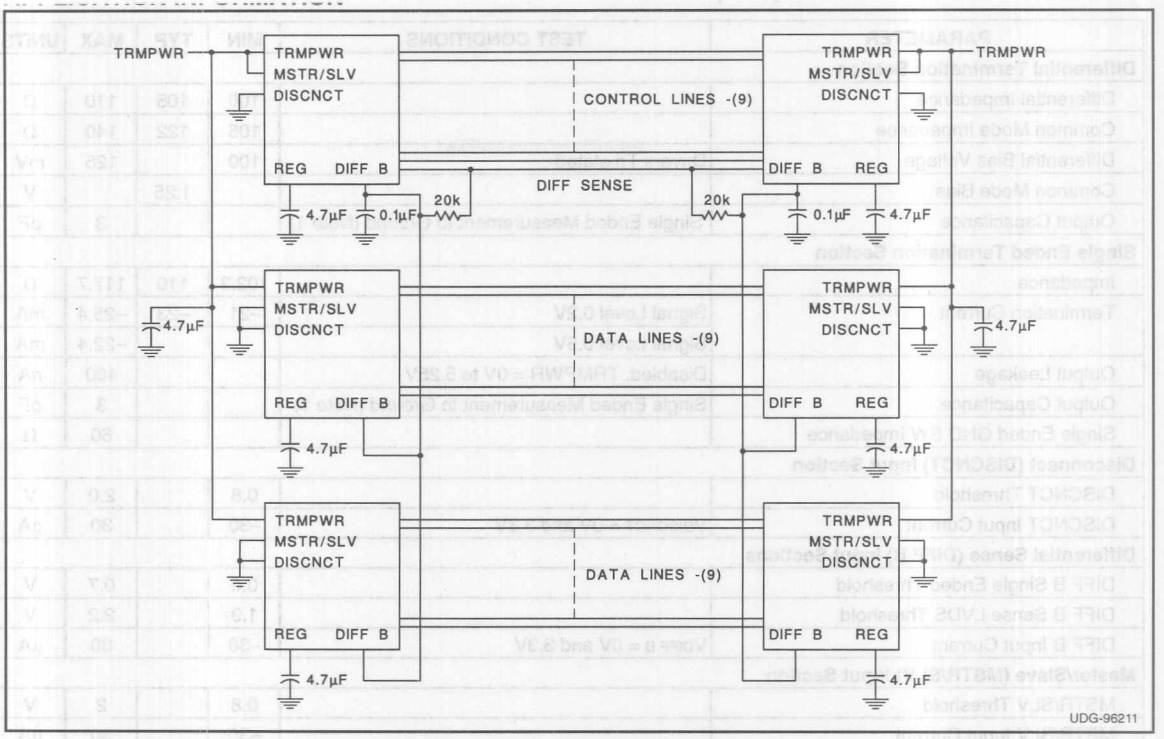


Figure 1. Application Drawing

The master is selected by placing TRMPWR on MSTR/SLV and the terminator enabled by grounding DISCNCT, enabling the 1.3V regulator. The master is the only terminator connected directly to DIFF SENSE bus line, all the other terminators receive the mode signal by connecting the DIFF B pins together.

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

Multi-mode (LVD/SE) SCSI 9 Line Terminator w/ 2.85V Regulator

FEATURES

- Auto Selection Single Ended (SE) or Low Voltage Differential (LVD) Termination
- Meets SCSI-1, SCSI-2, SCSI-3 SPI, Ultra Fast-20, Ultra-2 (SPI-2 LVD) and Ultra 3 Standards
- 2.7V to 5.25V Termpwr Operation
- Differential Failsafe Bias
- Thermal Packaging for Low Junction Temperature and Better MTBF

DESCRIPTION

The UCC5632 Multi-mode SCSI Terminator, both Low Voltage Differential and Single Ended Terminator is both a single ended terminator and a low voltage differential terminator for the transition to the next generation SCSI Parallel Interface (SPI-2). The low voltage differential is a requirement for the higher speeds at a reasonable cost and is the only way to have adequate skew budgets. The transceivers can be incorporated into the controller, unlike SCSI high power differential (EIA485) which requires external transceivers. Low Voltage differential is specified for Ultra-2 (Fast-40) and Ultra-3 (Fast-80), but has the potential of speeds up to Fast-320.

The UCC5630 cannot be used with SCSI differential EIA485, it will shutdown when it sees high power differential to protect the bus. The pinning for high power differential is not the same as LVD SCSI or single ended and the bias voltage, current and power are also different for EIA485 differential.

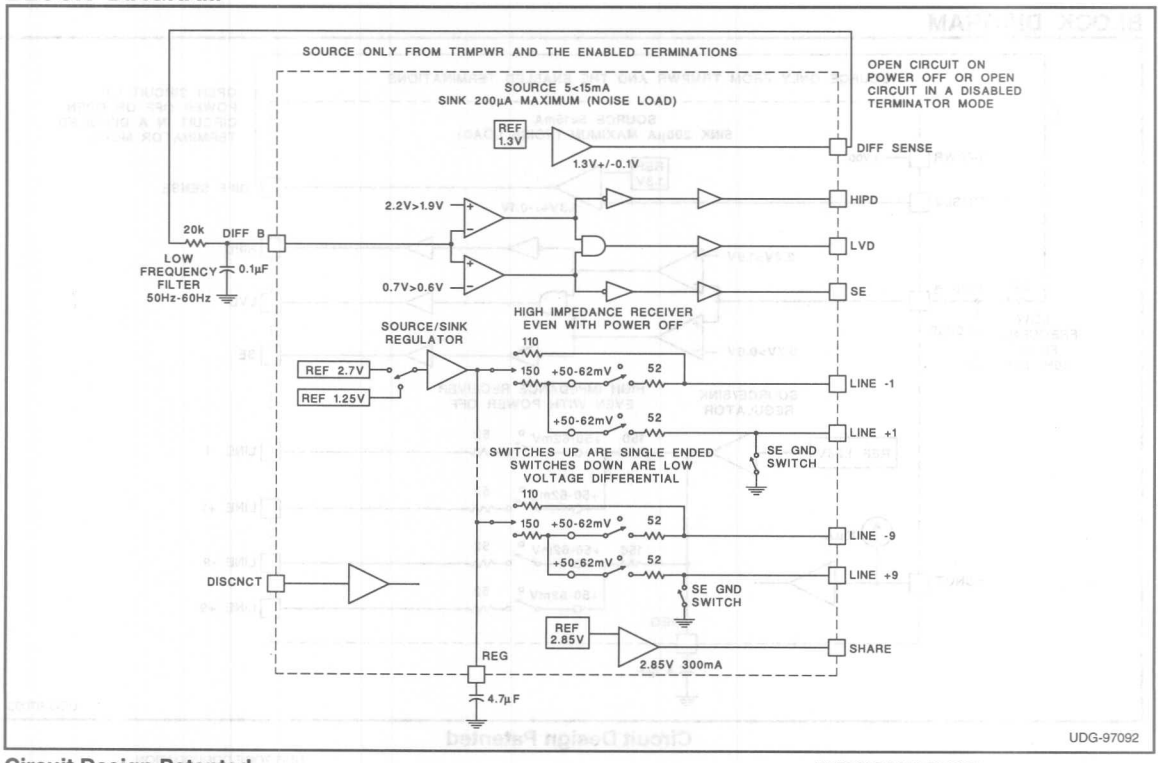
ABSOLUTE MAXIMUM RATINGS

TERMPWR Voltage . . . . . +6V
Signal Line Voltage. . . . . 0V to TERMPWR
Package Power Dissipation 2W
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

RECOMMENDED OPERATING CONDITIONS

TERMPWR Voltage 2.7Vto 5.25V

BLOCK DIAGRAM



Circuit Design Patented

3/97

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

Low Voltage Differential (LVD) SCSI 9 Line Terminator

FEATURES

- SCSI SPI-2 LVD SCSI 9 Line Low Voltage Differential Termination
- Meets SCSI SPI-2 Ultra-2 (Fast-40) and Ultra-3 (Fast-80) Standby
- 2.7V to 5.25V Operation
- Differential Failsafe Bias

DESCRIPTION

The UCC5640 Low Voltage Differential Terminator is a low voltage differential terminator only for SCSI Parallel Interface (SPI-2). The low voltage differential is a requirement for the higher speeds at a reasonable cost and is the only way to have adequate skew budgets. The transceivers can be incorporated into the controller, unlike SCSI high power differential (EIA485) which requires external transceivers. Low Voltage differential is specified for Ultra-2 (Fast-40) and Ultra-3 (Fast-80), but has the potential of speeds up to Fast-320.

The UCC5640 cannot be used with SCSI differential EIA485, it will shutdown when it sees high power differential to protect the bus. The pinning for high power differential is not the same as LVD SCSI or single ended and the bias voltage, current and power are also different for EIA485 differential.

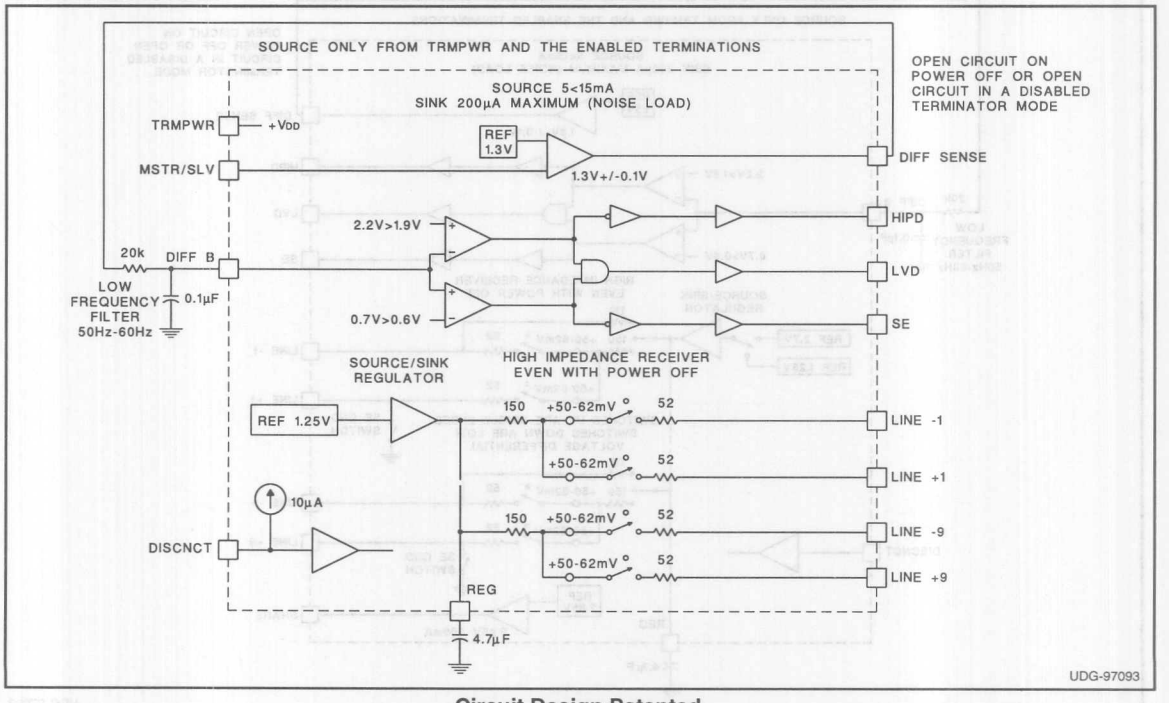
ABSOLUTE MAXIMUM RATINGS

TERMPWR Voltage . . . . . +6
Signal Line Voltage. . . . . 0V to TERMPWR
Package Dissipation. 1W
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

RECOMMENDED OPERATING CONDITIONS

TERMPWR Voltage . . . . . 2.7V to 5.25V

BLOCK DIAGRAM



Circuit Design Patented

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

UNITRODE

Ethernet Coaxial Impedance Monitor

FEATURES

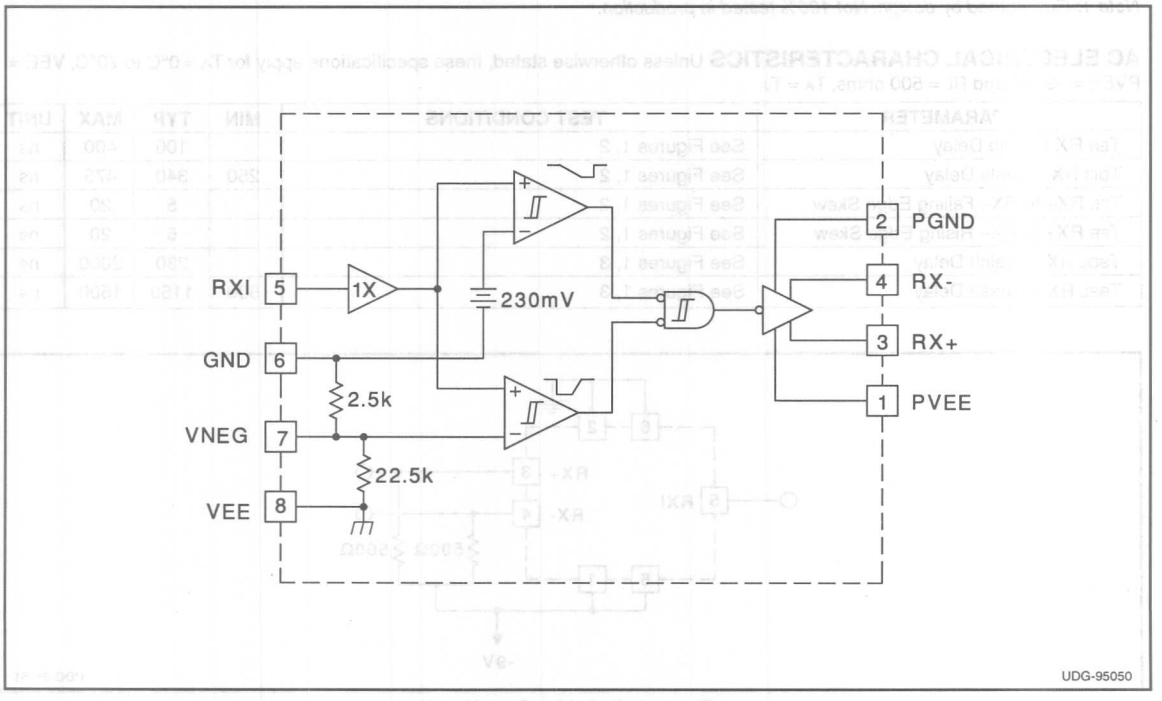
- Compatible with IEEE 802.3 10Base5, 10Base2, and 10BaseT
- Preset and Adjustable Data Thresholds
- Protects DTE from Spurious Data
- Prevents Erroneous Transmission Through Repeaters
- Detects Cable Termination Errors
- Detects Cable Impedance Errors

DESCRIPTION

The UC5661 is a monolithic integrated circuit which functions as an Ethernet Coaxial Impedance Monitor (CIM). This IC is intended to augment the receive (RX) function of IEEE 802.3 Coaxial Transceiver Interface (CTI) circuits. The UC5661 implements a hardware algorithm to detect reflections on the Ethernet coaxial cable or twisted pair which are caused by improper network termination or physical medium damage. If a physical problem is detected, the UC5661, whose receiver outputs operate in parallel with the CTI, immediately squelches the receive data, preventing the propagation of invalid network packets. During ordinary operation, the CIM RX outputs enable at the beginning of the data packet preamble, making it transparent to normal CTI functions. The valid data threshold, although preset for thick and thin-wire Ethernets, may be adjusted with the addition of one or two external resistors to meet 10BaseT requirements.

A secondary system design feature is provided by the UC5661. At the completion of a normal data transmission, the CIM Squelch activates much faster than typical transceiver ICs. The receiver outputs of the UC5661 have been designed to properly terminate the data packet, even with RX data transformers as small as 16µH, possibly allowing for smaller and less expensive system implementations. In these cases, end-of-packet squelch overshoot will be held to less than 100mV.

BLOCK DIAGRAM



5/95

ABSOLUTE MAXIMUM RATINGS

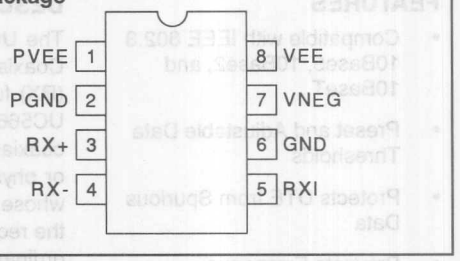
Supply Voltage (PVEE,VEE) . . . . . –15V
Input Voltage (RXI) . . . . . +2V to –10V
Operating Temperature Range . . . . . 0°C to +70°C
Junction Temperature (Note 1) . . . . . +125°C
Storage Temperature Range . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

All currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

Note 1: The devices are guaranteed by design to be functional up to the absolute maximum junction temperature.

CONNECTION DIAGRAMS

DIL-8 (Top View)
J or N Package



DC ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C, VEE = PVEE = –9.0V, and R_L = 500 ohms, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Current	Outputs Locked or Unlocked, Unloaded		10	20	mA
Input Bias Current	RXI = 0V		2	5	µA
Input Shunt Resistance	RXI = - 2V to 0V	0.200	45		MΩ
Input Shunt Capacitance	(Note 1)		3	4	pF
VNEG (Valid Data Reference)	VNEG = open	–980	–900	–830	mV
RX Output Voltage High (Squelch)		–1.2	–0.9	0	V
RX Output Voltage Low (Enable)		–6	–3.7	–3.2	V
Output Short Circuit	RX+ = RX– = 9V	–150			mA
Valid Data Threshold		–980	–900	–830	mV
Data Reflection Threshold		200	230	300	mV

Note 1: Guaranteed by design. Not 100% tested in production.

AC ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C, VEE = PVEE = –9.0V, and R_L = 500 ohms, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{EN} RX Enable Delay	See Figures 1, 2		100	400	ns
T_{DIS} RX Disable Delay	See Figures 1, 2	250	340	475	ns
T_{FS} RX+ to RX– Falling Edge Skew	See Figures 1, 2		5	20	ns
T_{FR} RX+ to RX– Rising Edge Skew	See Figures 1, 2		5	20	ns
T_{SQL} RX Squelch Delay	See Figures 1, 3		230	2000	ns
T_{REL} RX Release Delay	See Figures 1, 3	500	1150	1500	ns

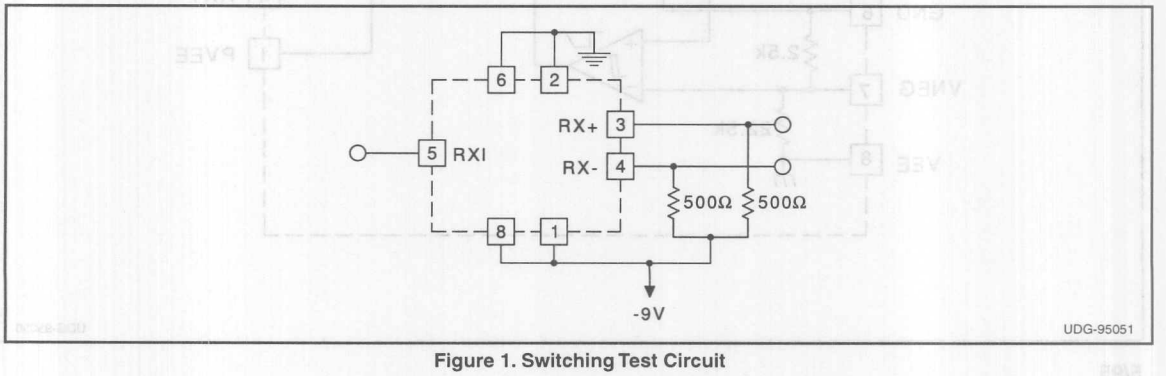


Figure 1. Switching Test Circuit

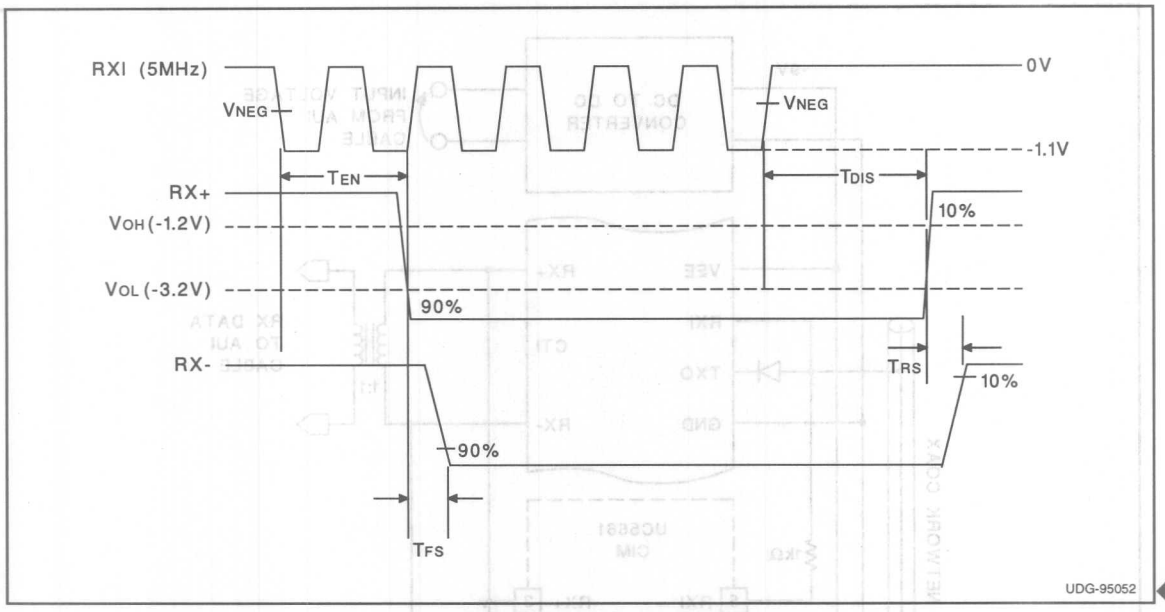


Figure 2. Input/Output Timing Diagram

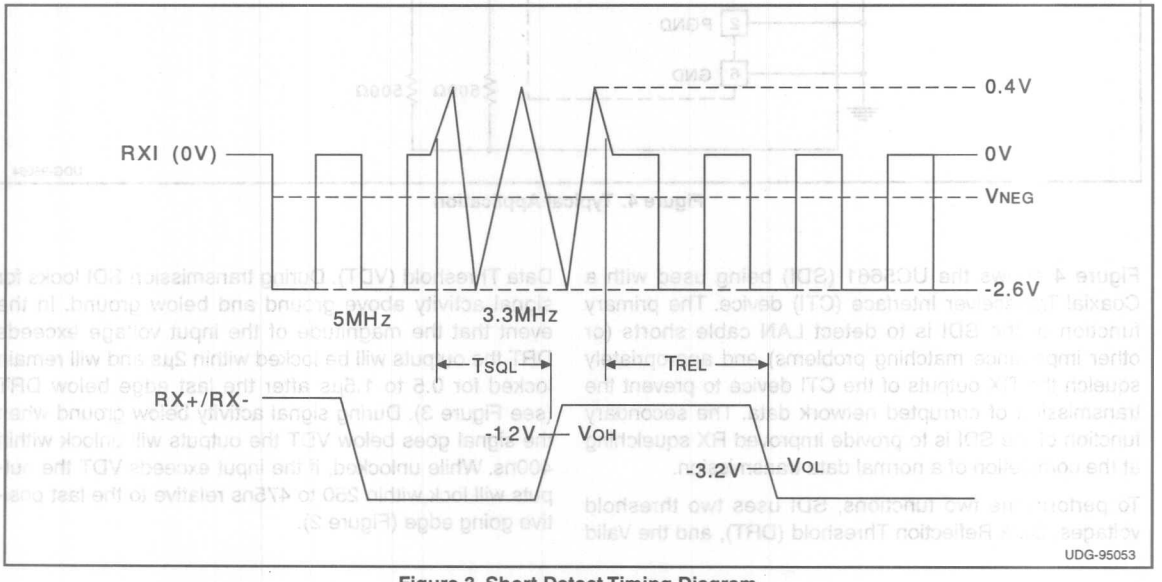


Figure 3. Short Detect Timing Diagram

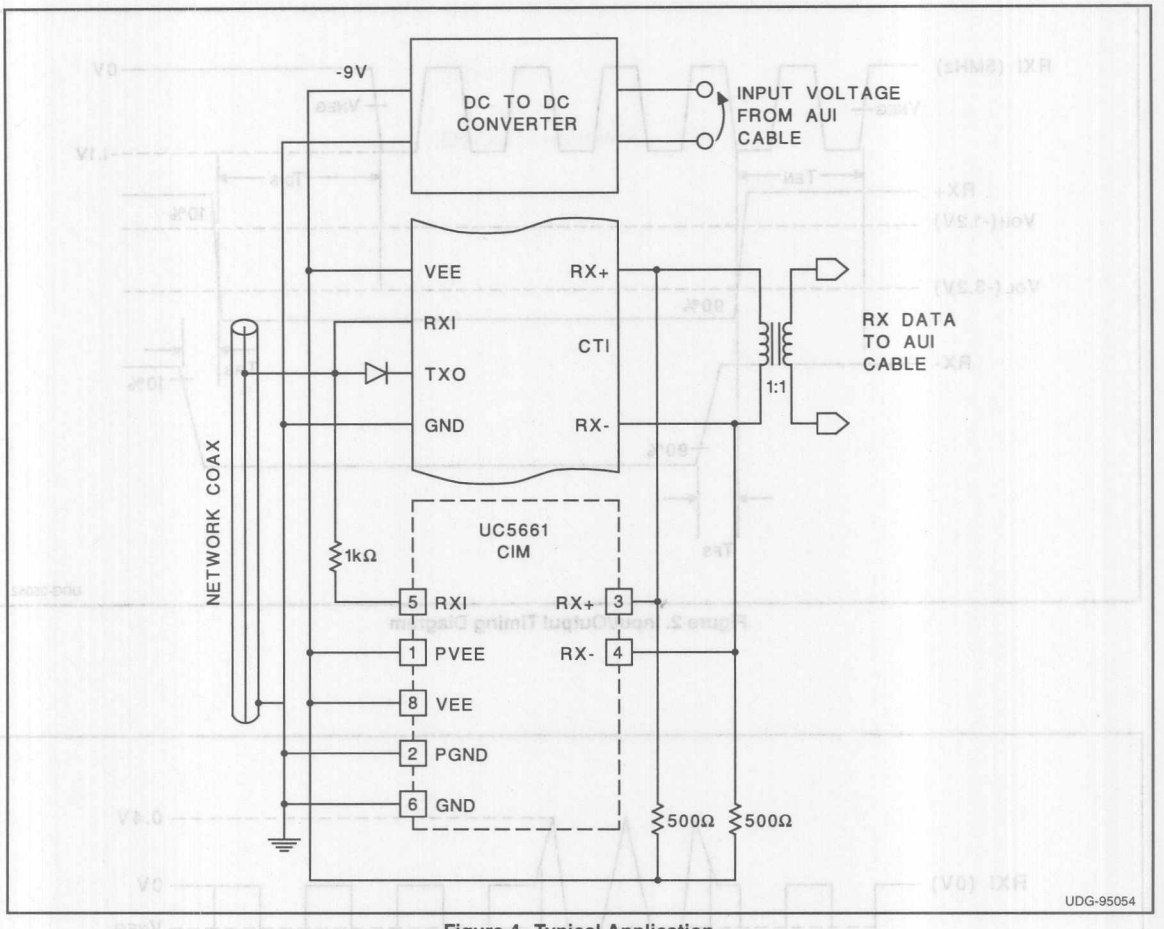


Figure 4. Typical Application

Figure 4 shows the UC5661 (SDI) being used with a Coaxial Transceiver Interface (CTI) device. The primary function of the SDI is to detect LAN cable shorts (or other impedance matching problems) and appropriately squelch the RX outputs of the CTI device to prevent the transmission of corrupted network data. The secondary function of the SDI is to provide improved RX squelching at the completion of a normal data transmission.

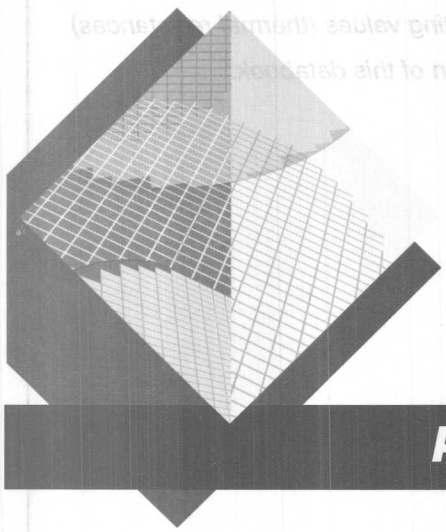
To perform the two functions, SDI uses two threshold voltages, Data Reflection Threshold (DRT), and the Valid Data Threshold (VDT). During transmission SDI looks for signal activity above ground and below ground. In the event that the magnitude of the input voltage exceeds DRT the outputs will be locked within 2µs and will remain locked for 0.5 to 1.5µs after the last edge below DRT (see Figure 3). During signal activity below ground when the signal goes below VDT the outputs will unlock within 400ns. While unlocked, if the input exceeds VDT the outputs will lock within 250 to 475ns relative to the last positive going edge (Figure 2).

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Consult Applications Handbook for available applications/design notes.

Datasheets in this section are organized in numeric order using the commercial part number.



Power Drivers

7

Packaging Note:

- *Values listed for recommended lead soldering time and temperature apply to ceramic thru-hole components only. Please consult the Packaging Section of this databook for recommendations on plastic SMD board attach processing.*

- *Unless otherwise noted, thermal resistance values listed on individual data sheets are for the device as it operates in a plastic thru-hole package. Results for other packaging options can be inferred by scaling the package rating values (thermal resistances) presented in the Packaging Section of this databook.*

Power and FET Drivers

Power and FET Drivers	UNITRODE PART NUMBER				
	L293/D ★	UC2950	UC3702✚	UC3705	UC3706
Power Driver	Quad	Single		Single	Dual
FET Driver					
Isolated Driver Pairs					
Relay Drivers			Quad		
Input Configuration	Non▼	Sink◆	Non▼	Comp■	Comp■
Enable					
Inhibit	Y		Y		Y
Analog Stop					Y
Output Rise Time (ns)	250			60	60
Maximum Voltage	36	35	42.5	40	40
Peak Output Current (A)	2.0/1.2	4.0	50mA per Relay	1.5	1.5
Application/Design Note				U-118, U-137	U-118, U-137

Power and FET Drivers (cont'd)	UNITRODE PART NUMBER				
	UC3707	UC3708	UC3709	UC3710	UC3711
Power Driver	Dual	Dual Non-Inv.			
FET Driver			Single	Single	Dual
Isolated Driver Pairs					
Input Configuration	Comp■	Inv.	Non▼	Comp■	Non▼
Enable		Y			
Inhibit	Y				
Analog Stop	Y				
Output Rise Time (ns)	50	75	40	40	20
Maximum Voltage	40	35	40	20	40
Peak Output Current (A)	1.5	3.0	1.5	6.0/1.0/2.0 AUX 0.5/1.0	1.5/1.0/2.0 AUX 0.5/1.0
Application/Design Note	U-118, U-137	DN-35, U-137	U-118, U-137		

✚ New Product
▼ Non-Inverting
◆ Sink/Source TTL
■ Complementary
★ Refer to Intelligent Motion Section for Product Data Sheet

Power and FET Drivers (cont'd)	UNITRODE PART NUMBER				
	UC3714	UC3715	UC3724/25	UC3726/27	UCC3776
Power Driver				Single	
FET Driver	Dual	Dual	Single		Quad
Isolated Driver Pairs			FET Drv	IGBT Drv	
Input Configuration	Non▼	Non▼	Non▼	Non▼	Non▼
Enable	Y	Y			Y
Inhibit					
Analog Stop					
Output Rise Time (ns)	100/50	100/50	30	75	
Maximum Voltage	20	20	40	40	18
Peak Output Current (A)	1.0/2.0	1.0/2.0	2.0	4.0	1.5/2.0
Application/Design Note			DN-35, U-127	DN-57, DN-60, U-143C	

Power Supply Support Products	UNITRODE PART NUMBER		
	UC3610 ★	UC3611 ★	UC3612 ★
Description	Dual Schottky Diode Bridge	Quad Schottky Diode Array	Dual Schottky Diode
Application	Eight-diode Array for High Current, Low Duty Cycle Flyback Voltage Clamping for Inductive Loads	Four-diode Array for High Current Bridges and Voltage Clamps	Two-diode Array for High Current, Low Duty Cycle Flyback Voltage Clamping for Inductive Loads
Key Features	• Monolithic Eight-diode Array • High Peak Current • Low Forward Voltage • Fast Recovery Time	• Matched, Four-diode Monolithic Array • High Peak Current • Low Forward Voltage • Parallelable for Higher Current or Lower Voltage Drop	• Monolithic Two-diode Array • High Peak Current • Low Forward Voltage • Fast Recovery Time

Special Function Circuits	UNITRODE PART NUMBER	
	UC3704	UC37131/2 ✚
Part Name	Bridge Transducer Switch	Smart Power Switch
Description	Contains a Complete Signal Conditioning System to Interface Low-level Variable Impedance Transducers to a Digital System	65V Universal High or Low Side Driver with Current Limiting

✚ New Product
▼ Non-Inverting
★ Refer to General Power Supply Circuits Section for Product Data Sheet

UNITRODE

Half-Bridge Bipolar Switch

FEATURES

- Source or Sink 4.0A
- Supply Voltage to 35V
- High-Current Output Diodes
- Tri-State Operation
- TTL and CMOS Input Compatibility
- Thermal Shutdown Protection
- 300kHz Operation
- Low-Cost TO-220 Package

DESCRIPTION

This device is a monolithic integrated circuit designed to provide high-current switching with low saturation voltages when activated by low-level logic signals. Source and sink switches may be independently activated without regard to timing as a built-in interlock will keep the sink off if the source is on.

This driver has the high current capability to drive large capacitive loads with fast rise and fall times; but with high-speed internal flyback diodes, it is also ideal for inductive loads. Two UC2950s can be used together to form a full bridge, bipolar motor driver compatible with high frequency chopper current control.

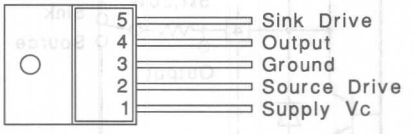
ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage Range, Vc	8V to 35V
Output Voltage Range, Vo	-3.0V to Vc+3V
Input Voltage Range, VIN	-0.3V to +7.0V
Peak Output Current (100 ms, 10% DC)	±4.0A
Continuous Output Current	±2.0A
Power Dissipation with Heat Sink	15W
Power Dissipation in Free Air	2W
Operating Temperature Range, TA	-20°C to +100°C
Storage Temperature Range, Ts	-55°C to +125°C

Note 1: Consult Packaging section of databook for thermal limitations and considerations of package.

CONNECTION DIAGRAM

5-PIN TO-220 (TOP VIEW)
T Package

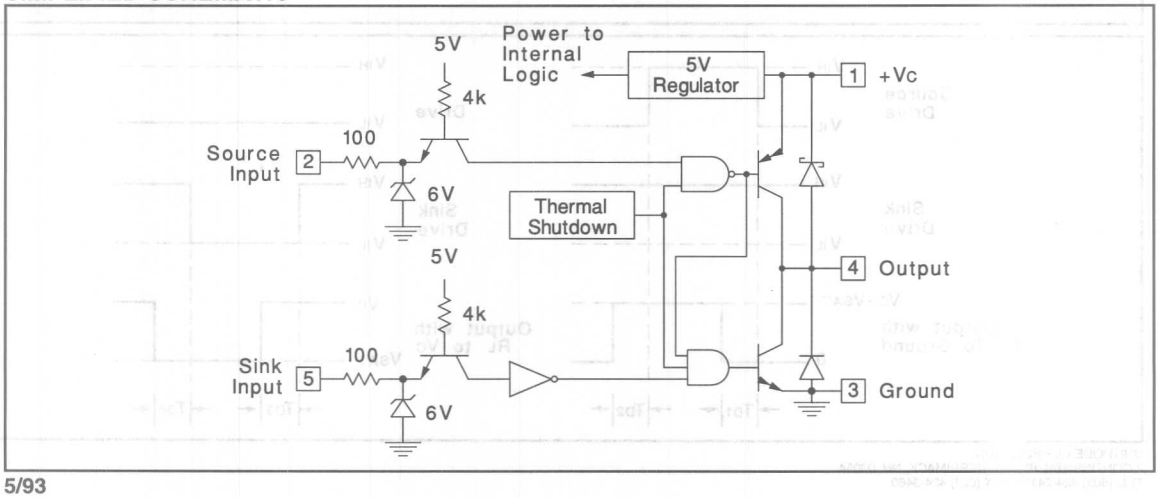


TRUTH TABLE

Source Drive Pin 2	Sink Drive Pin 5	Output Pin 4
Low	Low	Low
Low	High	Off
High	Low	High
High	High	High

Note: With no load, output voltage will be HIGH in the OFF state.

SIMPLIFIED SCHEMATIC



5/93

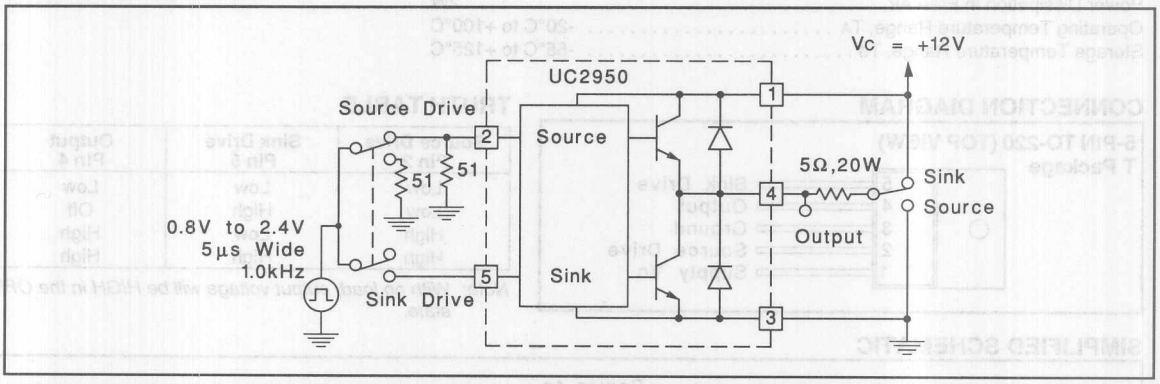
ELECTRICAL CHARACTERISTICS: Unless otherwise stated, V_C = 35V, T_A = -20°C to +100°C, V_{IL} = 0.8V, V_{IH} = 2.4V for either input, $T_A = T_J$.

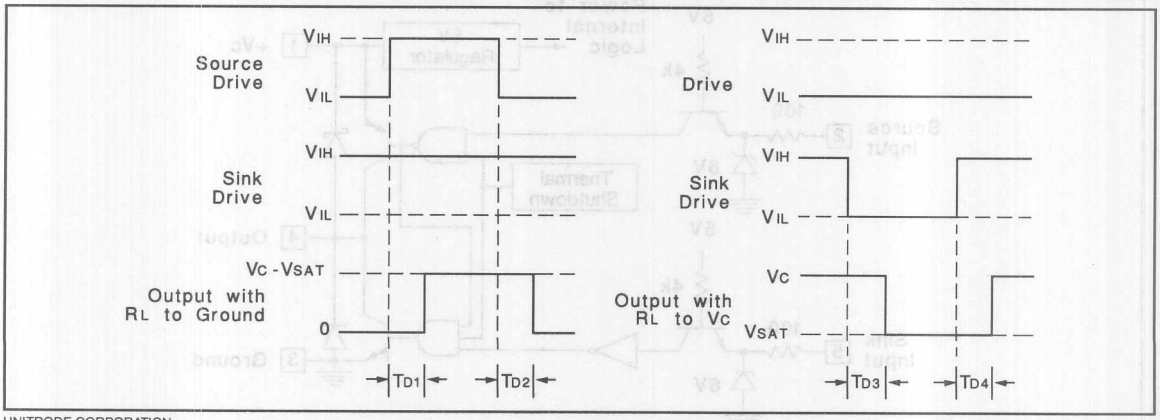
PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Leakage to V_C	Output Off		20	500	µA
Output Leakage to Ground	Output Off		-200	-500	µA
Output Sink Saturation	V_{OL}, I_L = 2.0A		1.2	2.0	V
Output Source Saturation	(V_C-V_{OL}), I_L = -2.0A		1.2	2.0	V
Sink Diode Forward Voltage	I_D = -2.0A		1.4	2.0	V
Source Diode Forward Voltage	I_D = 2.0A		1.4	2.0	V
Input Current	Either Input, V_I = 5V		20	100	µA
	Either Input, V_I = 0V		-1.0	-1.6	mA
Supply Current	Output High		20	30	mA
	Output Low		10	20	mA

SWITCHING CHARACTERISTICS: See Test Circuit. V_C = 12V, R_L = 5Ω, T_A = 25°C. Guaranteed by design, not 100% tested in production.

PARAMETERS	MIN	TYP	MAX	UNITS
Source Turn-On Delay, t_{D1}		300	500	ns
Source Turn-Off Delay, t_{D2}		1.0	2.0	µs
Sink Turn-On Delay, t_{D3}		200	400	ns
Sink Turn-Off Delay, t_{D4}		100	300	ns
Cross-Conduction Current Spike When Source and Sink are Activated Together		0.6	1.0	µs

SWITCHING TEST CIRCUIT





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Quad PWM Relay Driver

FEATURES

- Maintains Constant Average Relay Voltage With Varying Supply Voltages
- VBUS Voltages up to 42.5V
- Up to 50mA per Relay
- Integrated Schottky Flyback Diodes
- Individual Relay Control Inputs
- Short Circuit Protection
- User Selectable Operating Center Frequency and Relay Voltage
- Global Reset

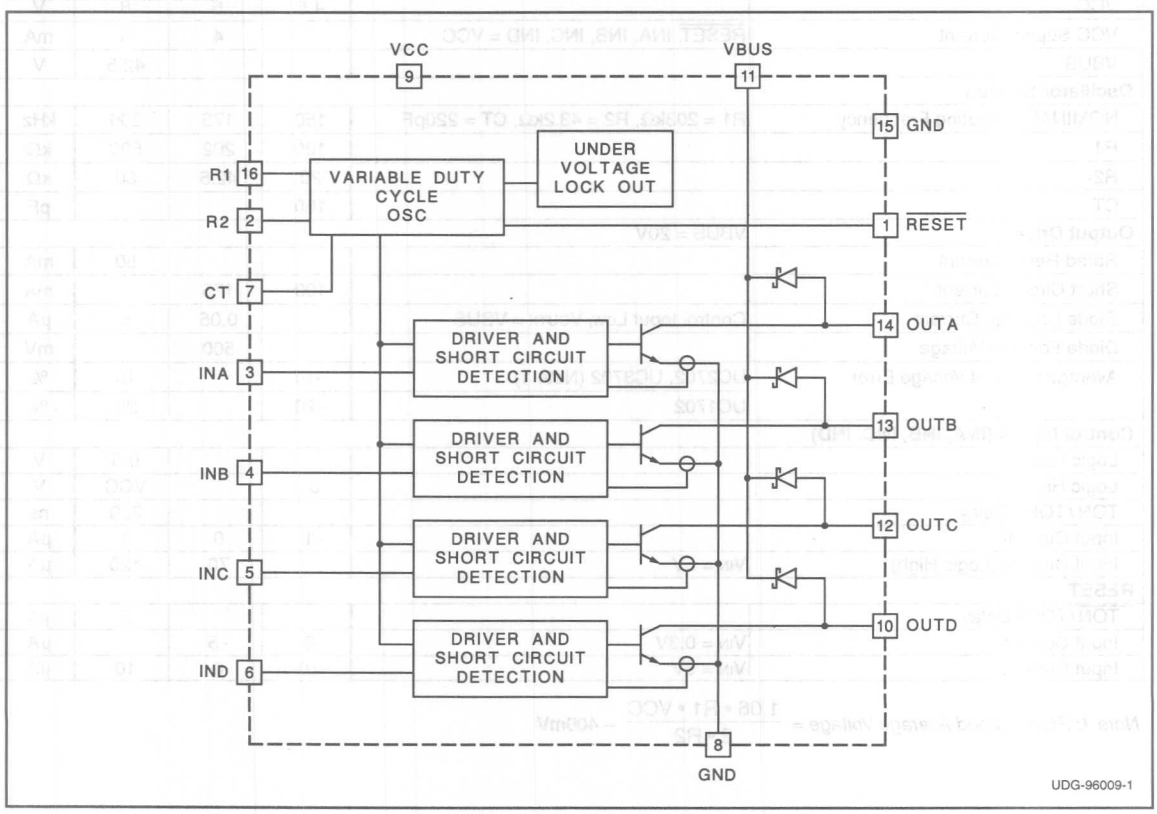
DESCRIPTION

The UC3702 Quad Relay Driver is intended to drive up to four relays from logic inputs using an unregulated relay voltage supply. The relays are driven from the Bus supply in a power efficient PWM converter fashion. The relay coil is used as the inductive element. (See the application's section concerning the relay selection.) VBUS must be higher then the rated relay voltage. Short circuit protection is provided on chip with periodic retry.

The UC3702 requires a +5V logic supply as a reference. Two external resistors program the effective relay voltage and a capacitor sets the nominal operating frequency. Internal Schottky diodes eliminate the need for any external power components.

In typical applications, the UC3702 grants the user the flexibility to choose the most cost effective relay without the added burden of generating a separate relay supply voltage. The UC3702 will even function with a poorly regulated supply VBUS, containing significant 100Hz or 120Hz ripple.

BLOCK DIAGRAM



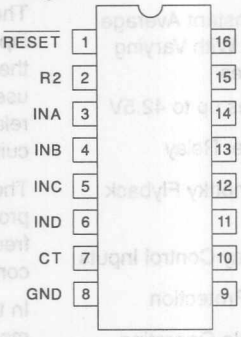
ABSOLUTE MAXIMUM RATINGS

VBUS . . . . . +50V
VCC . . . . . +9V
Input Voltage . . . . . –0.3V to VCC + 0.3V
Average Current per Relay 50mA
Total Output Capacitance. 25pF
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

Currents are positive into, negative out of the specified terminal.
Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAMS

DIL-16, SOIC-16 (Top View)
J or N, D Package



ELECTRICAL CHARACTERISTICS

Unless otherwise stated these specifications apply for T_A = –55°C to +125°C for UC1702; –25°C to +85°C for UC2702; 0°C to +70°C for UC3702; VBUS = 34V, VCC = 5V, $\overline{\text{RESET}}$ = VCC, R2 = 43.2kΩ; R1 = 203kΩ; CT = 220pF, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Section					
VCC		4.5	5	8	V
VCC Supply Current	$\overline{\text{RESET}}$, INA, INB, INC, IND = VCC		4	6	mA
VBUS				42.5	V
Oscillator Section					
NOMINAL Operating Frequency	R1 = 203kΩ, R2 = 43.2kΩ, CT = 220pF	150	175	200	kHz
R1		100	202	500	kΩ
R2		20	42.5	80	kΩ
CT		100			pF
Output Driver	VBUS = 20V				
Rated Relay Current				50	mA
Short Circuit Current		100	175		mA
Diode Leakage Current	Control Input Low, V_{OUTX} = VBUS		0.05	5	µA
Diode Forward Voltage			500		mV
Averaged Output Voltage Error	UC2702, UC3702 (Note 1)	–10		10	%
	UC1702	–20		20	%
Control Inputs (INA, INB, INC, IND)					
Logic Low				0.5	V
Logic High		3		VCC	V
TON / TOFF Delay				250	ns
Input Current		–1	0	1	µA
Input Current (Logic High)	V_{IN} = 5V		70	120	µA
$\overline{\text{RESET}}$					
TON/TOFF Delay				2	µs
Input Current	V_{IN} = 0.3V	–8	–5		µA
Input Current	V_{IN} = 5V	–10	0	10	µA

Note 1: Programmed Average Voltage $= \dfrac{1.06 \bullet R1 \bullet VCC}{2 \bullet R2} - 400mV$

PIN DESCRIPTIONS

CT: A capacitor from the CT pin to ground sets the oscillator center frequency. Note that the oscillator period must be least an order of magnitude less than the relaxation time constant (L/R) of the relay coil. However, a needlessly high operating frequency only increases power dissipation. For best accuracy, CT should be 220pF or greater.

GND: Both ground pins must be connected to a low noise system ground.

INA, INB, INC, IND: Separate digital control inputs for each of the four relay drivers. An active high input (a logic high) turns on the respective relay. Active low disables the common-emitter drive transistor.

OUTA, OUTB, OUTC, OUTD: Each of these output pins can be connected to the low side of one relay coil. The rated relay coil voltage of all relays to be driven by a single UC3702 must be the same. (It is permissible to use coils with different rated series resistances with a single UC3702, so long as the rated coil voltages are the same and care is taken with respect to the relaxation times of the different relay coils). Output transients are slew rate limited to decrease electro-magnetic radiation.

R1: User selected external resistor must be placed from the R1 pin to the VBUS voltage supply. Sensing the VBUS amplitude, the oscillator varies its ON duty cycle such that the average voltage across the driver coil is constant.

R2: User selected external resistor must placed from R2 pin to GND. This resistor, in conjunction with the external timing capacitor, CT, sets the OFF cycle time of the oscillator. For best accuracy, use 42.3kΩ for R2.

$\overline{\text{RESET}}$: Digital reset pin is active low. When $\overline{\text{RESET}}$ is low, the oscillator stops running and all drivers are open collector.

VCC: Nominally 5V. In addition to supplying the voltage for the driver logic and oscillator circuit, the VCC supply is used as reference for the generating the average relay voltage. It is recommended that the VCC be regulated to ±5% of its nominal value or better to insure good regulation. Good decoupling with a minimum of 1µF is necessary.

VBUS: This pin should be tied to a low impedance voltage source at some voltage higher than the rated voltage of the relay coil to be driven. VBUS may even be a poorly filtered rectified sin wave, as the UC3702 will regulate the correct duty cycle. Good decoupling with a minimum of 1µF is necessary.

APPLICATION INFORMATION

The UC3702 must be programmed for a specific relay voltage. The table given below has some suggested values of R1, R2, and CT. The VCC supply voltage is assumed to be 5V.

Rated Relay Voltage	R1	R2	CT
9V	153kΩ	43.2kΩ	220pF
12V	203kΩ	43.2kΩ	220pF
24V	398kΩ	43.2kΩ	220pF

More generally, the following equation can be used to determine the equivalent average relay voltage:

$$V_{RELAY} = \frac{1.06 \bullet VCC \bullet R1}{2 \bullet R2} - 400mV$$

Industrial Relays

The UC3702 takes advantage of the inductance of the relay coil to regulate a constant coil current in a manner very similar to a switch-mode power supply. To use the UC3702 correctly, the coil characteristics must be known. The rated relay voltage is what the relay manufacturers specify as voltage to drive the relay coil with if the coil were driven from a dc source. Most manufacturers also specify the series resistance of the coil. This is the resistance of the copper wire and determines the steady state coil ON current. For example, a 12V relay with a 320Ω series coil resistance with a draw of 37.5mA of constant current. The relay inductance is not typically specified in the manufacturer's short-form datasheet, so the engineer will need an LCR bridge to measure it or request the information from the relay manufacturer.

APPLICATION INFORMATION (cont.)

Although the inductance may not be specified in the relay datasheet, it is very repeatable since it is determined by the number of turns and geometry of the relay.

The relay's coil inductance divided by its series resistance is the relay coil's relaxation time constant. It is important that the relaxation time constant be at least an order of magnitude longer than the nominal switching period of the UC3702 to obtain a constant current through the relay coil. This means that some relays may be ill-suited for use with the UC3702.

For example, a common 12V industrial relay has a series resistance of 500Ω and a coil inductance of 500mH. Its relaxation time constant is 1ms, an order of magnitude less than the period of a 10kHz oscillator.

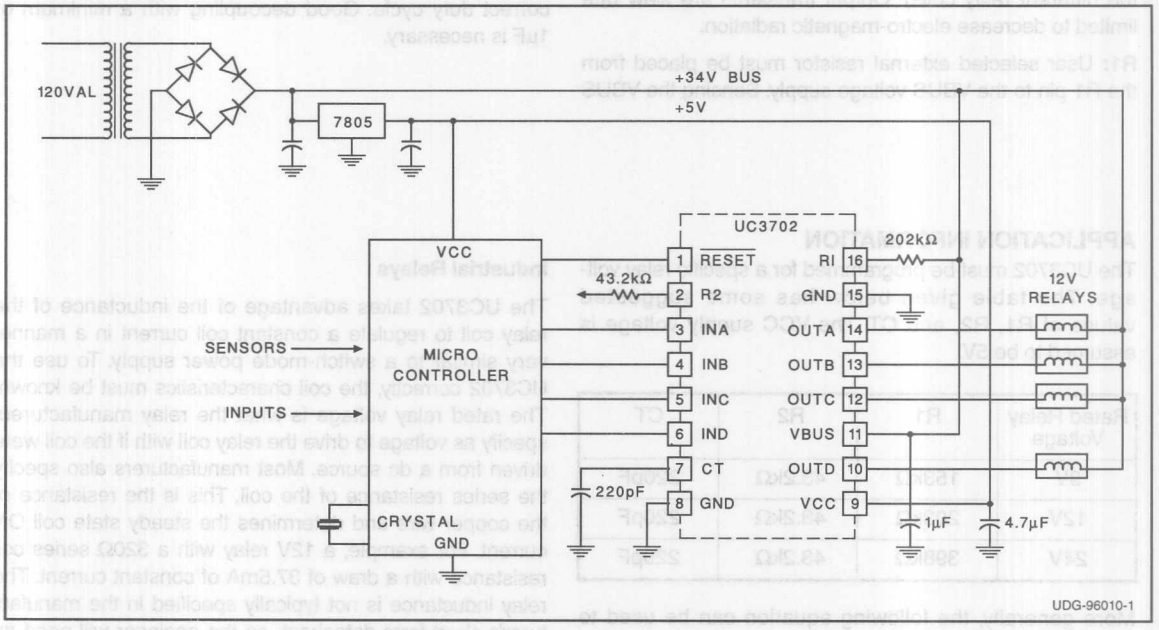
When performing an engineering evaluation of the UC3702 in a system, it is useful to have a current probe. Alternately, a 1Ω resistor can be placed in series with the relay coil in the prototype and differential voltage probes can be used to observe the coil current. (Do not use a large series resistor, as this will impact observed relaxation time constant.)

Layout Considerations

The layout of the printed circuit board and good decoupling of the power supplies is critical to proper operation of the UC3702. For best results, high quality 4.7µF tantalum capacitors should be placed as close as possible to the VCC and the VBUS pins.

In addition to decoupling considerations, the R1 and R2 pins are sensitive to capacitive coupling from any of the driver outputs (OUTA - D) which can slew at speeds of 300V/µs. The external resistors R1 and R2 should be placed as close as possible to their respective pins. Avoid routing the outputs directly past these pins without a low impedance trace (such as GND, VCC, or VBUS) in between to act as a capacitive shield.

Typical Microcontroller Application Driving 12V Industrial Relays



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UNITRODE

Bridge Transducer Switch

FEATURES

- Dual Matched Current Sources
- High-gain Differential Sensing Circuit
- Wide Common-mode Input Capability
- Complementary Digital Open-collector Outputs
- Externally Programmable Time Delay
- Optional Output Latch with Reset
- Built-in Diagnostic Activation
- Wide Supply Voltage Range
- High Current Heater Power Source Driver

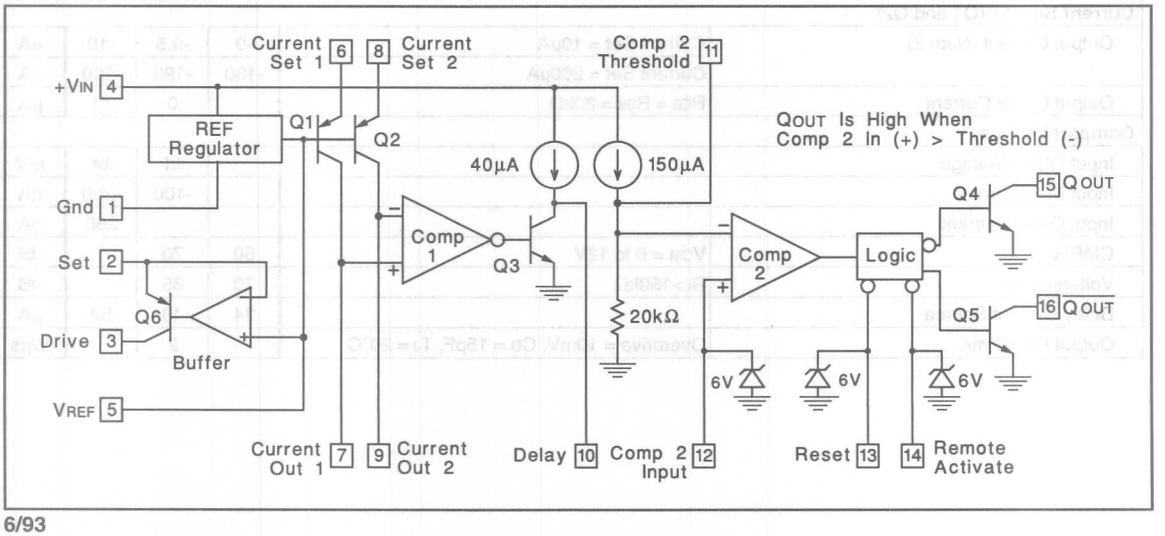
DESCRIPTION

This integrated circuit contains a complete signal conditioning system to interface low-level variable impedance transducers to a digital system. A pair of matched, temperature-compensated current sources are provided for balanced transducer excitation followed by a precision, high-gain comparator. The output of this comparator can be delayed by a user-selectable duration, after which a second comparator will switch complementary outputs separately activated for diagnostic operation and has an optional latch with external reset capability. An added feature is a high current power source useful as a heater driver in differential temperature sensing applications. The UC3704 is designed for 0°C to +70°C environments.

UC3704 COMPATIBLE SENSORS

SENSOR TYPE	ACTIVATION SOURCE						
	Temperature	Pressure	Force	Position	Displacement	Velocity	Shock
Thermistor	X					X	
Sensistor	X					X	
Thermocouple	X						
Semiconductor	X	X	X				
Photo Voltaic				X	X	X	
Photo Resistive				X	X	X	
Strain Gage		X	X	X	X	X	X
Piezoelectric		X	X		X	X	X
Magneto Resistive				X	X		
Inductive				X	X	X	X
Hall Effect				X	X		
Capacitive							X

BLOCK DIAGRAM



6/93

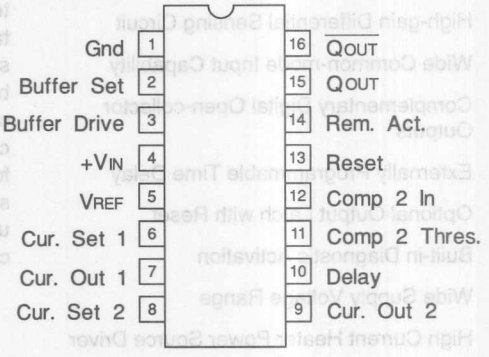
ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($+V_{IN}$) 40V
Output Current (each output) . . . . . 50 mA
Buffer Power Source Current 200mA
Comparator 1 Inputs . . . . . -0.5V to V_{REF}
Comparator 2 Inputs . . . . . 0 to 5.5V
Remote Activation and Reset Inputs . . . . . 0 to 5.5V
Power Dissipation at T_A = 25°C 1000mW
Operating Junction Temperature . . . . . -55°C to +150°C
Storage Temperature Range . . . . . -65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) . . . . . +300°C

Note: Unless otherwise specified, all voltages are with respect to ground (Pin 1).
Currents are positive into, negative out of the specified terminal.
Consult Packaging section of Databook for thermal limitations and considerations of package.

CONNECTION DIAGRAM

DIL-16 (TOP VIEW)
J or N Package



ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, these specifications apply for T_A = 0°C to +70°C for the UC3704: V_{IH} = 15V, T_A = T_J.

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Power Inputs					
Supply Voltage Range		4.2		36	V
Supply Current	V_{IN} = 36V		5	10	mA
Reference Section (with respect to V_{IN})					
V_{REF} Value $\lvert V_{IN} - V_{REF} \rvert$	T_J = 25°C	2.1	2.2	2.3	V
V_{REF} Temperature Coefficient	Note 1	-1	-2	-3	mV/°C
Line Regulation	ΔV_{IN} = 4.2 to 25V		2	10	mV
Load Regulation	ΔI_O = 0 to 4mA		2	10	mV
Short Circuit Current	V_{IN} = 36V, V_{REF} = V_{IN} or Ground			±25	mA
Current Source (Q1 and Q2)					
Output Current (Note 2)	Current Set = 10µA	-9	-9.5	-10	µA
	Current Set = 200µA	-180	-195	-200	µA
Output Offset Current	R_{E6} = R_{E8} = 20kΩ		0	±1	µA
Comparator One					
Input Offset Voltage			±1	±4	mV
Input Bias Current			-100	-300	nA
Input Offset Current				±60	nA
CMRR	V_{CM} = 0 to 12V	60	70		dB
Voltage gain	R_L>150kΩ	70	85		dB
Delay Current Source		34	40	52	µA
Output Rise Time	Overdrive = 10mV, C_D = 15pF, T_J = 20°C		2		V/µs

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = 0°C to +70°C for the UC3704: V_{IH} = 15V, T_A = T_J.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Comparator Two (Q_{OUT} and $\overline{Q_{OUT}}$)						
Threshold Voltage			2.2	3.0	3.8	V
Threshold Resistance	To Ground		14	20	24	kΩ
Input Bias Current	V_{IN} (Pin 12) = 5V			1	3	µA
Remote Activate Current	Pin 14 = 0V			0.2	0.5	mA
Reset Current	Pin 13 = 0V			0.2	0.5	mA
Remote Activate Threshold	T_A = 25°C		0.8	1.2		V
Reset Threshold	T_A = 25°C		0.8	1.2		V
Output Saturation	I_{OUT} = 16mA			0.2	0.5	V
	I_{OUT} = 50mA			0.7	2.0	V
Output Leakage	V_{OUT} = 40V			0.2	10	µA
Output Response	Comp. Overdrive = 1V, R_L = 5k to V_{IN}	Turn-on		0.4		µs
		Turn-off		1.0		µs
Buffer						
Set Voltage (V_{IN} -Vs)	T_J = 25°C, Is = 100mA		1.9	2.1	2.3	V
Drive Current	T_J = 25°C, R_S = 200Ω, V_D = 0V		90	100	120	mA

Note 1: Parameter guaranteed by design, not tested in production.

Note 2: Collector output current $= \frac{V_{IN} - V_{REF} - V_{BE}}{R_E} \approx \frac{1.5V}{R_E}$

APPLICATIONS INFORMATION

Sensor Section

The input portion of the UC3704 provides both excitation and sensing for a low-level, variable impedance transducer. This circuitry consists of a pair of highly matched PNP transistors biased for operation as constant current sources followed by a high gain precision comparator.

The reference voltage at the bases of the PNP transistors has a TC to offset the base-emitter voltage variation of these transistors resulting in a constant voltage across the external emitter resistors and correspondingly constant collector currents for balancing, offsetting, or to provide unique temperature characteristic.

With the PNP transistor's optimum current ranging from 10 to 200µA, and the common-mode input voltage of the comparator usable from ground to (V_{IN} - 3V), a wide range of transducer impedance levels is possible.

The sensor comparator has a current source pull-up at the output so that an external capacitor from this point to ground can be used to provide a programmable delay before reaching the second comparator's threshold. The low-impedance on-state of Comp 1's output provides quick reset of this capacitor. This programmable delay function is useful for providing transient protection by requiring that Comp 1 remain activated for a finite period of time before Comp 2 triggers. Another application is in counting repetitive pulses where a missing pulse will allow Comp 1's output to rise to Comp 2's threshold. This time delay function is:

$$Delay = \frac{Comp\ 2\ Threshold}{Delay\ Current} X\ C_D \approx 175ms/\mu F$$

If hysteresis is desired for Comparator 1, it may be accommodated by applying positive feedback from the delay terminal to the non-inverting input on Pin 7. This will aid in providing oscillation-free transitions for very slowly changing inputs.

APPLICATIONS INFORMATION (cont.)

Output Section

The output portion of the UC3704 is basically a second comparator with complimentary, open-collector outputs. This comparator has a built-in, ground-referenced threshold implemented with a high-impedance current source and resistor so that it may be easily overridden with an external voltage source if desired. Comp 2's input transistors are NPN types which require at least 1V of common-mode voltage for accurate operation and should not see a differential input voltage greater than 6V.

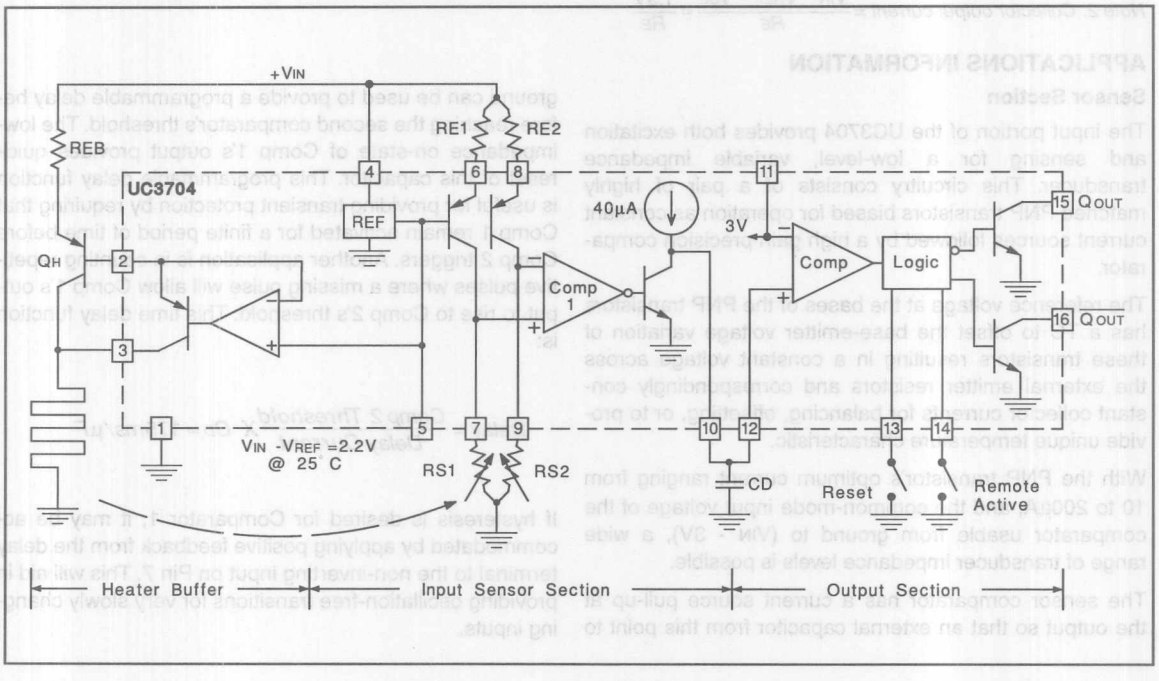
For diagnostic or latching purposes, the output logic is equipped with a Remote Activate and Reset function. These pins have internal pull-ups and are only active when pulled low below a threshold of approximately 1V. A low signal at the Remote Activate Pin causes the outputs to change state in exactly the same manner as if Comp 2's input is raised above the threshold on Pin 11. If Pin 16 is connected to Pin 14, positive feedback results and the outputs will latch once triggered by Comp 2's input. Pulling the Reset terminal low overrides the Remote Activate Pin releasing the latch.

Reference Buffer

This circuit is designed to provide up to 100mA to drive a high current external PNP transistor useful for powering a heater for differential temperature measurements. Care must be taken that power dissipation in Q6 does not cause excessive thermal gradients which will degrade the accuracy of the sensing circuitry.

Using a heating element attached to a temperature sensitive resistor, RS1, in one leg of the input bridge implements a flow sensor for either gasses or liquids. As long as there is flow, heat from the element is carried away and the sensor voltage remains below threshold. Using an identical sensor, RS2, without a heater to establish this threshold compensates for the ambient temperature of the flow.

TYPICAL APPLICATION FOR MONITORING LIQUID OR GAS FLOW



UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

High Speed Power Driver

FEATURES

- 1.5A Source/Sink Drive
- 100 nsec Delay
- 40 nsec Rise and Fall into 1000pF
- Inverting and Non-Inverting Inputs
- Low Cross-Conduction Current Spike
- Low Quiescent Current
- 5V to 40V Operation
- Thermal Shutdown Protection
- MINIDIP and Power Packages

DESCRIPTION

The UC1705 family of power drivers is made with a high speed Schottky process to interface between low-level control functions and high-power switching devices - particularly power MOSFETs. These devices are also an optimum choice for capacitive line drivers where up to 1.5 amps may be switched in either direction. With both Inverting and Non-Inverting inputs available, logic signals of either polarity may be accepted, or one input can be used to gate or strobe the other.

Supply voltages for both Vs and Vc can independently range from 5V to 40V. For additional application details, see the UC1707/3707 data sheet.

The UC1705 is packaged in an 8-pin hermetically sealed CERDIP for -55°C to +125°C operation. The UC3705 is specified for a temperature range of 0°C to +70°C and is available in either a plastic minidip or a 5-pin, power TO-220 package.

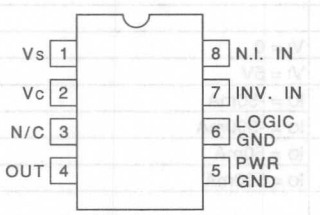
TRUTH TABLE

INV	N.I	OUT
H	H	L
L	H	H
H	L	L
L	L	L

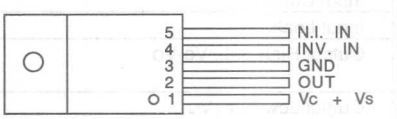
$\overline{OUT}$ = $\overline{INV}$ and N.I.
$\overline{OUT}$ = INV or $\overline{N.I.}$

CONNECTION DIAGRAMS

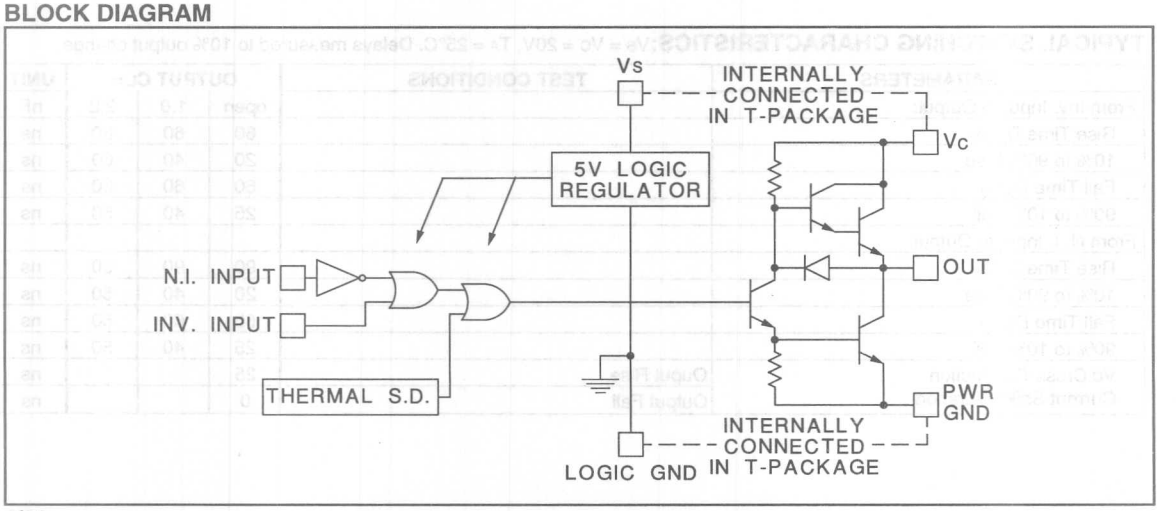
DIL-8 MINIDIP, SOIC-8
(TOP VIEW)
N or J Package, D Package



5-PIN TO-220
(TOP VIEW)
T Package



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

	N-Pkg	J-Pkg	T-Pkg
Supply Voltage, V_{IN}	40V	40V	40V
Collector Supply Voltage, Vc	40V	40V	40V
Output Current (Source or Sink)			
Steady-State	±500mA	±500mA	±1.0A
Peak Transient	±1.5A	±1.0A	±2.0A
Capacitive Discharge Energy	20µJ	15µJ	50µJ
Digital Inputs (See Note)	5.5V	5.5V	5.5V
Power Dissipation at T_A = 25°C (See Note)	1W	1W	3W
Power Dissipation at T_A (Leads/Case) = 25°C (See Note)	3W	2W	25W
Operating Temperature Range	0°C to +70°C	-55°C to +125°C	0°C to +70°C
Storage Temperature Range	-65°C to +150°C	-65°C to +150°C	-65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C	300°C	300°C

Note: All currents are positive into, negative out of the specified terminal.
Digital Drive can exceed 5.5V if input current is limited to 10mA
Consult Packaging Section of Databook for thermal limitations and considerations of package.

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1705, -25°C to +85°C for the UC2705, and 0°C to +70°C for the UC3705; V_S = Vc = 20V, T_A = T_J.

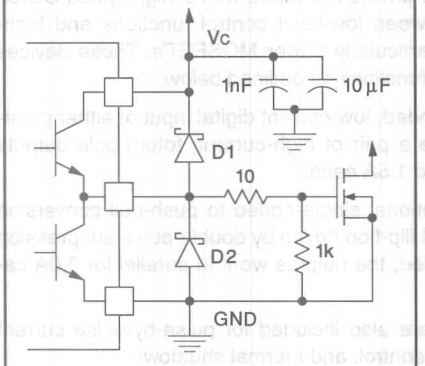
PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_S Supply Current	V_S = 40V, (Outputs High, T Pkg)		6	8	mA
	V_S = 40V, (Outputs Low, T Pkg)		8	12	mA
Vc Supply Current (N, J Only)	Vc = 40V, Outputs Low		2	4	mA
Vc Leakage Current (N, J Only)	V_S = 0, Vc = 30V		.05	0.1	mA
Digital Input Low Level				0.8	V
Digital Input High Level		2.2			V
Input Current	V_I = 0		-0.6	-1.0	mA
Input Leakage	V_I = 5V		0.5	0.1	mA
Output High Sat., Vc-Vo	I_O = -50mA			2.0	V
	I_O = -500mA			2.5	V
Output Low Sat., Vo	I_O = 50mA			0.4	V
	I_O = 500mA			2.5	V
Thermal Shutdown			155		°C

TYPICAL SWITCHING CHARACTERISTICS: V_S = Vc = 20V, T_A = 25°C. Delays measured to 10% output change.

PARAMETERS	TEST CONDITIONS	OUTPUT C_L =			UNIT
From Inv. Input to Output:		open	1.0	2.2	nF
Rise Time Delay		60	60	60	ns
10% to 90% Rise		20	40	60	ns
Fall Time Delay		60	60	60	ns
90% to 10% Fall		25	40	50	ns
From N. I. Input to Output:					
Rise Time Delay		90	90	90	ns
10% to 90% Rise		20	40	60	ns
Fall Time Delay		60	60	60	ns
90% to 10% Fall		25	40	50	ns
Vc Cross-Conduction Current Spike Duration	Ouput Rise	25			ns
	Output Fall	0			ns

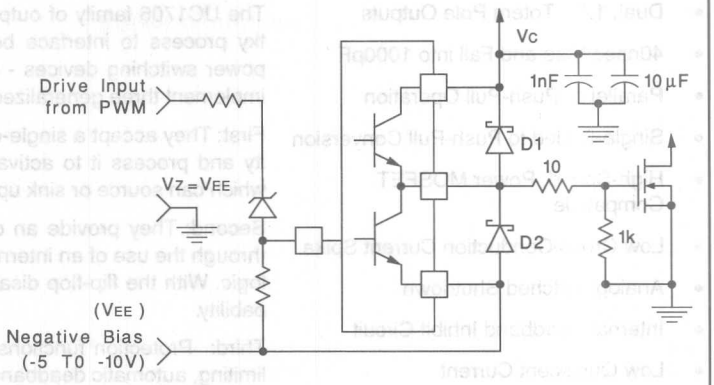
APPLICATIONS

Power MOSFET Drive Circuit



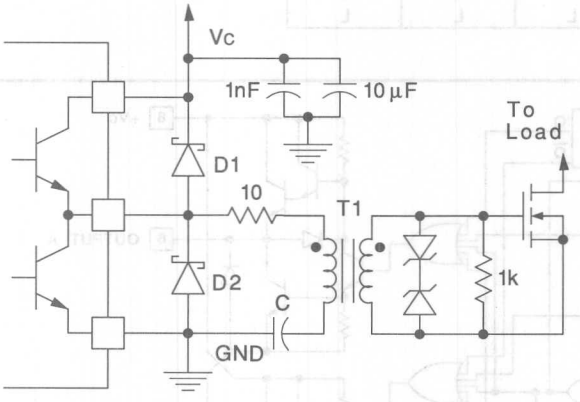
D1, D2: UC3611 Schottky Diodes

Power MOSFET Drive Circuit using Negative Bias Voltage and Level Shifting to Ground Referenced PWMs.



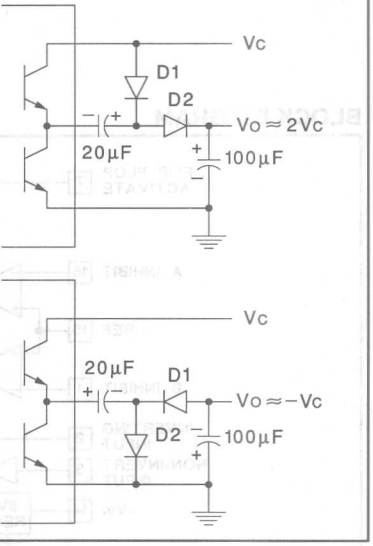
D1, D2: UC3611 Schottky Diodes

Transformer Coupled MOSFET Drive Circuit



D1, D2: UC3611 Schottky Diodes

Charge Pump Circuits



UNITRODE CORPORATION
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UNITRODE

UC1706
UC2706
UC3706

Dual Output Driver

FEATURES

- Dual, 1.5A Totem Pole Outputs
- 40nsec Rise and Fall into 1000pF
- Parallel or Push-Pull Operation
- Single-Ended to Push-Pull Conversion
- High-Speed, Power MOSFET Compatible
- Low Cross-Conduction Current Spike
- Analog, Latched Shutdown
- Internal Deadband Inhibit Circuit
- Low Quiescent Current
- 5 to 40V Operation
- Thermal Shutdown Protection
- 16-Pin Dual-In-Line Package
- 20-Pin Surface Mount Package

DESCRIPTION

The UC1706 family of output drivers are made with a high-speed Schottky process to interface between low-level control functions and high-power switching devices - particularly power MOSFET's. These devices implement three generalized functions as outlined below.

First: They accept a single-ended, low-current digital input of either polarity and process it to activate a pair of high-current, totem pole outputs which can source or sink up to 1.5A each.

Second: They provide an optional single-ended to push-pull conversion through the use of an internal flip-flop driven by double-pulse-suppression logic. With the flip-flop disabled, the outputs work in parallel for 3.0A capability.

Third: Protection functions are also included for pulse-by-pulse current limiting, automatic deadband control, and thermal shutdown.

These devices are available in a two-watt plastic "bat-wing" DIP for operation over a 0°C to 70°C temperature range and, with reduced power, in a hermetically sealed cerdip for -55°C to +125°C operation. Also available in surface mount Q and L packages.

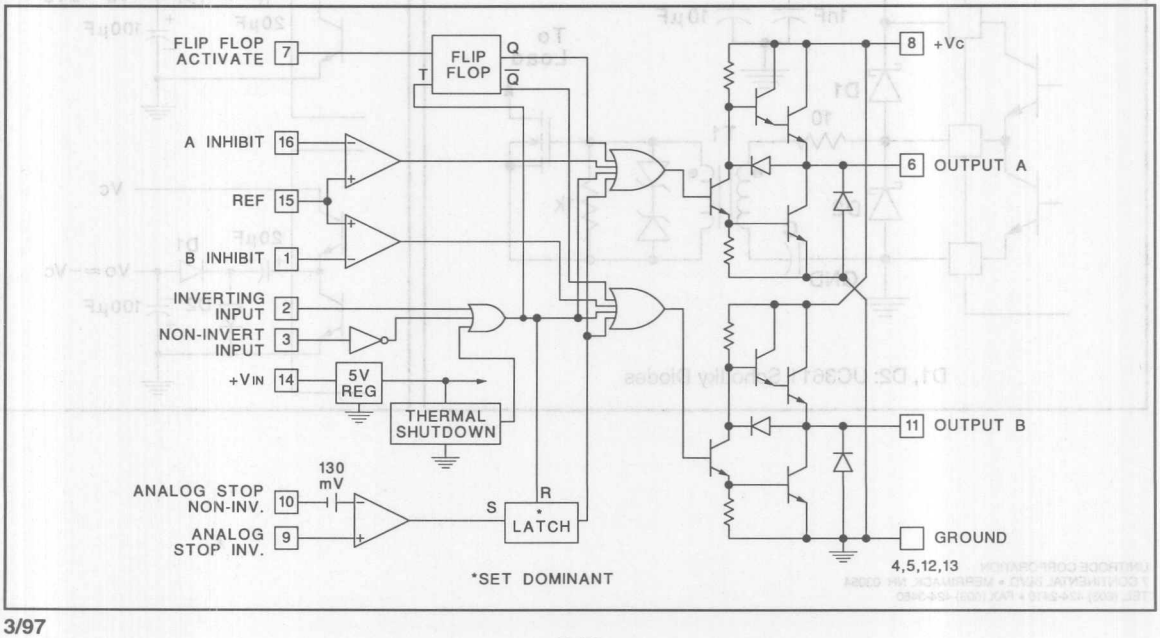
TRUTH TABLE

INV	N.I	OUT
H	H	L
L	H	H
H	L	L
L	L	L

$\overline{OUT} = \overline{INV}$ and N.I.

$\overline{OUT}$ = INV or $\overline{N.I.}$

BLOCK DIAGRAM



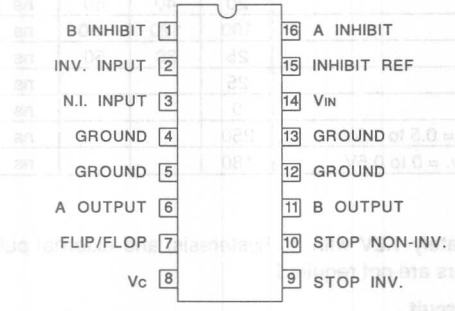
ABSOLUTE MAXIMUM RATINGS

	N-Pkg	J-Pkg
Supply Voltage, V_{IN}	40V	40V
Collector Supply Voltage, Vc	40V	40V
Output Current (Each Output, Source or Sink)		
Steady-State	±500mA	±500mA
Peak Transient	±1.5A	±1.0A
Capacitive Discharge Energy	20µJ	15µJ
Digital Inputs	5.5V	5.5V
Analog Stop Inputs	V_{IN}	V_{IN}
Power Dissipation at T_A = 25°C (See Note)	2W	1W
Power Dissipation at T (Leads/Case) = 25°C (See Note)	5W	2W
Operating Temperature Range	-55°C to +125°C	
Storage Temperature Range	-65°C to +150°C	
Lead Temperature (Soldering, 10 Seconds)	300°C	

Note: All voltages are with respect to the four ground pins which must be connected together. All currents are positive into, negative out of the specified terminal. Consult Packaging section of Databook for thermal limitations and considerations of package.

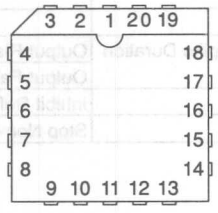
CONNECTION DIAGRAMS

DIL-16, SOIC-16
(TOP VIEW)
J or N Package, DW Package



Note: All four ground pins must be connected to a common ground.

PLCC-20, LCC-20
(TOP VIEW)
Q, L Packages



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
B INHIBIT	2
INV INPUT	3
N.I. INPUT	4
GROUND	5
N/C	6
GROUND	7
A OUTPUT	8
FLIP/FLOP	9
Vc	10
N/C	11
STOP NON-INV.	12
STOP INV.	13
B OUTPUT	14
GROUND	15
N/C	16
GROUND	17
V_{IN}	18
INHIBIT REF	19
A INHIBIT	20

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1706, -25°C to +85°C for the UC2706 and 0°C to +70°C for the UC3706; V_{IN} = Vc = 20V. T_A = T_J.

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{IN} Supply Current	V_{IN} = 40V		8	10	mA
Vc Supply Current	Vc = 40V, Outputs Low		4	5	mA
Vc Leakage Current	V_{IN} = 0, Vc = 30V, No Load		.05	0.1	mA
Digital Input Low Level				0.8	V
Digital Input High Level		2.2			V
Input Current	V_I = 0		-0.6	-1.0	mA
Input Leakage	V_I = 5V		.05	0.1	mA
Output High Sat., Vc-Vo	Io = -50mA			2.0	V
	Io = -500mA			2.5	V

ELECTRICAL CHARACTERISTICS (cont.): Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1706, -25°C to +85°C for the UC2706 and 0°C to +70°C for the UC3706; V_{IN} = V_C = 20V. T_A = T_J.

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Low Sat., V_O	I_O = 50mA			0.4	V
	I_O = 500mA			2.5	V
Inhibit Threshold	V_{REF} = 0.5V	0.4		0.6	V
	V_{REF} = 3.5V	3.3		3.7	V
Inhibit Input Current	V_{REF} = 0		-10	-20	µA
Analog Threshold	V_{CM} = 0 to 15V	100	130	150	mV
Input Bias Current	V_{CM} = 0		-10	-20	µA
Thermal Shutdown			155		°C

TYPICAL SWITCHING CHARACTERISTICS: V_{IN} = V_C = 20V, T_A = 25°C. Delays measured to 10% output change.

PARAMETERS	TEST CONDITIONS	OUTPUT C_L =			UNIT
From Inv. Input to Output:		open	1.0	2.2	nF
Rise Time Delay		110	130	140	ns
10% to 90% Rise		20	40	60	ns
Fall Time Delay		80	90	110	ns
90% to 10% Fall		25	30	50	ns
From N. I. Input to Output:					
Rise Time Delay		120	130	140	ns
10% to 90% Rise		20	40	60	ns
Fall Time Delay		100	120	130	ns
90% to 10% Fall		25	30	50	ns
V_C Cross-Conduction Current Spike Duration	Output Rise	25			ns
	Output Fall	0			ns
Inhibit Delay	Inhibit Ref. = 1V, Inhibit Inv. = 0.5 to 1.5V	250			ns
Analog Shutdown Delay	Stop Non-Inv. = 0V, Stop Inv. = 0 to 0.5V	180			ns

CIRCUIT DESCRIPTION

Outputs

The totem-pole outputs have been designed to minimize cross-conduction current spikes while maximizing fast, high-current rise and fall times. Current limiting can be done externally either at the outputs or at the common Vc pin. The output diodes included have slow recovery and should be shunted with high-speed external diodes when driving high-frequency inductive loads.

Flip/Flop

Grounding pin 7 activates the internal flip-flop to alternate the two outputs. With pin 7 open, the two outputs operate simultaneously and can be paralleled for higher current operation. Since the flip-flop is triggered by the digital input, an off-time of at last 200nsec must be provided to allow the flip/flop to change states. Note that the circuit logic is configured such that the "OFF" state is defined as the outputs low.

Digital Inputs

With both an inverting and non-inverting input available, either active-high or active-low signals may be accepted. These are true TTL compatible inputs--the threshold is approximately 1.2V with no hysteresis; and external pull-up resistors are not required.

Inhibit Circuit

Although it may have other uses, this circuit is included to eliminate the need for deadband control when driving relatively slow bipolar power transistors. A diode from each inhibit input to the opposite power switch collector will keep one output from turning-on until the other has turned-off. The threshold is determined by the voltage on pin 15 which can be set from 0.5 to 3.5V. When this circuit is not used, ground pin 15 and leave 1 and 16 open.

Analog Shutdown

This circuit is included to get a latched shutdown as close to the outputs as possible, from a time standpoint. With an internal 130mV threshold, this comparator has a common-mode range from ground to (V_{IN} - 3V). When not used, both inputs should be grounded. The time required for this circuit to latch is inversely proportional to the amount of overdrive but reaches a minimum of 180nsec. As with the flip-flop, an input off-time of at least 200nsec is required to reset the latch between pulses.

CIRCUIT DESCRIPTION (cont.)

Supply Voltage

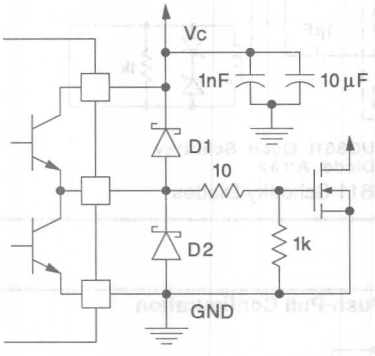
With an internal 5V regulator, this circuit is optimized for use with a 7 to 40V supply; however, with some slight response time degradation, it can also be driven from 5V. When VIN is low, the entire circuit is disabled and no current is drawn from VC. When combined with a UC1840 PWM, the Driver Bias switch can be used to supply VIN to the UC1706. VIN switching should be fast as if VC is high, undefined operation of the outputs may occur with VIN less than 5V.

Thermal Considerations

Should the chip temperature reach approximately 155°C, a parallel, non-inverting input is activated driving both outputs to the low state.

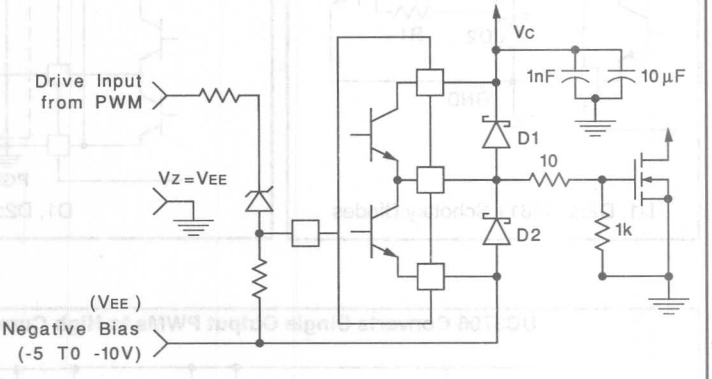
APPLICATIONS

Power MOSFET Drive Circuit



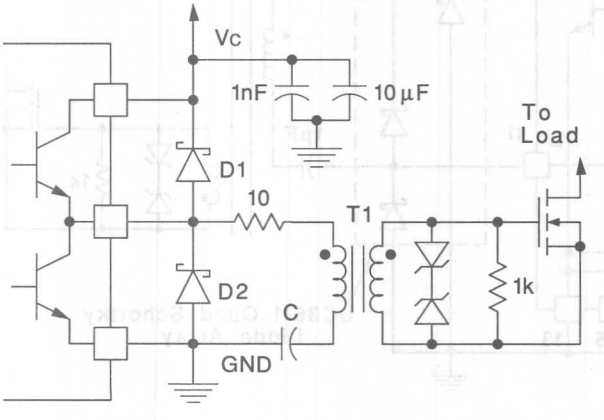
D1, D2: UC3611 Schottky Diodes

Power MOSFET Drive Circuit Using Negative Bias Voltage and Level Shifting to Ground Referenced PWMs.



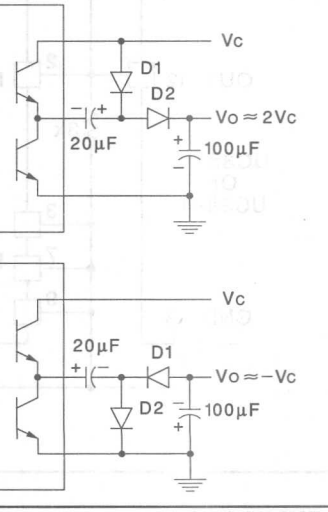
D1, D2: UC3611 Schottky Diodes

Transformer Coupled MOSFET Drive Circuit



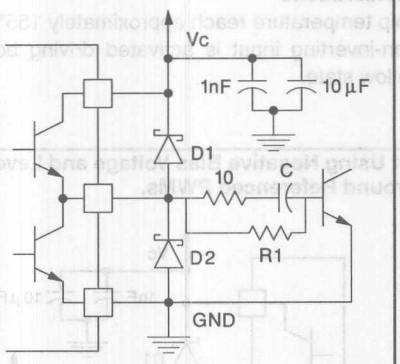
D1, D2: UC3611 Schottky Diodes

Charge Pump Circuits



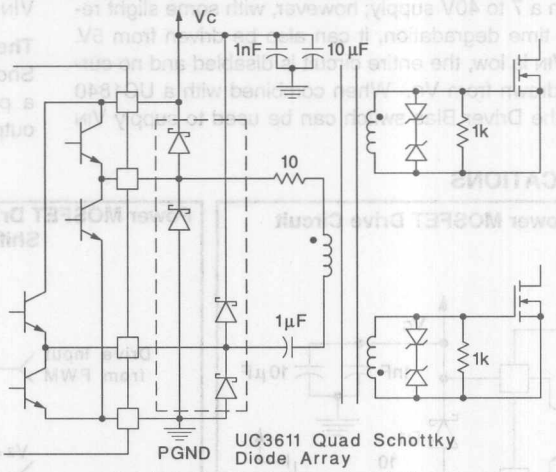
APPLICATIONS (cont'd)

Power Bipolar Drive Circuit



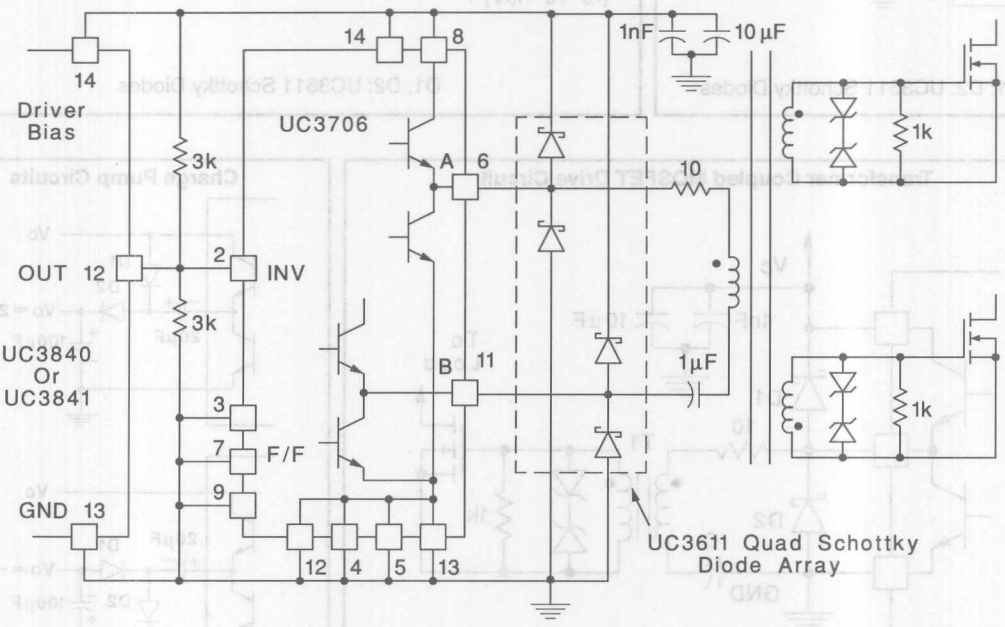
D1, D2: UC3611 Schottky Diodes

Transformer Coupled Push-Pull MOSFET Drive Circuit



D1, D2: UC3611 Schottky Diodes

UC3706 Converts Single Output PWMs to High Current Push-Pull Configuration



UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
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UNITRODE

Dual Channel Power Driver

UC1707
UC2707
UC3707

FEATURES

- Two Independent Drivers
- 1.5A Totem Pole Outputs
- Inverting and Non-Inverting Inputs
- 40ns Rise and Fall into 1000pF
- High-Speed, Power MOSFET Compatible
- Low Cross-Conduction Current Spike
- Analog Shutdown with Optional Latch
- Low Quiescent Current
- 5V to 40V Operation
- Thermal Shutdown Protection
- 16-Pin Dual-In-Line Package
- 20-Pin PLCC and CLCC Package

DESCRIPTION

The UC1707 family of power drivers is made with a high-speed Schottky process to interface between low-level control functions and high-power switching devices - particularly power MOSFETs. These devices contain two independent channels, each of which can be activated by either a high or low input logic level signal. Each output can source or sink up to 1.5A as long as power dissipation limits are not exceeded.

Although each output can be activated independently with its own inputs, it can be forced low in common through the action either of a digital high signal at the Shutdown terminal or a differential low-level analog signal. The Shutdown command from either source can either be latching or not, depending on the status of the Latch Disable pin.

Supply voltage for both V_{IN} and V_C can independently range from 5V to 40V.

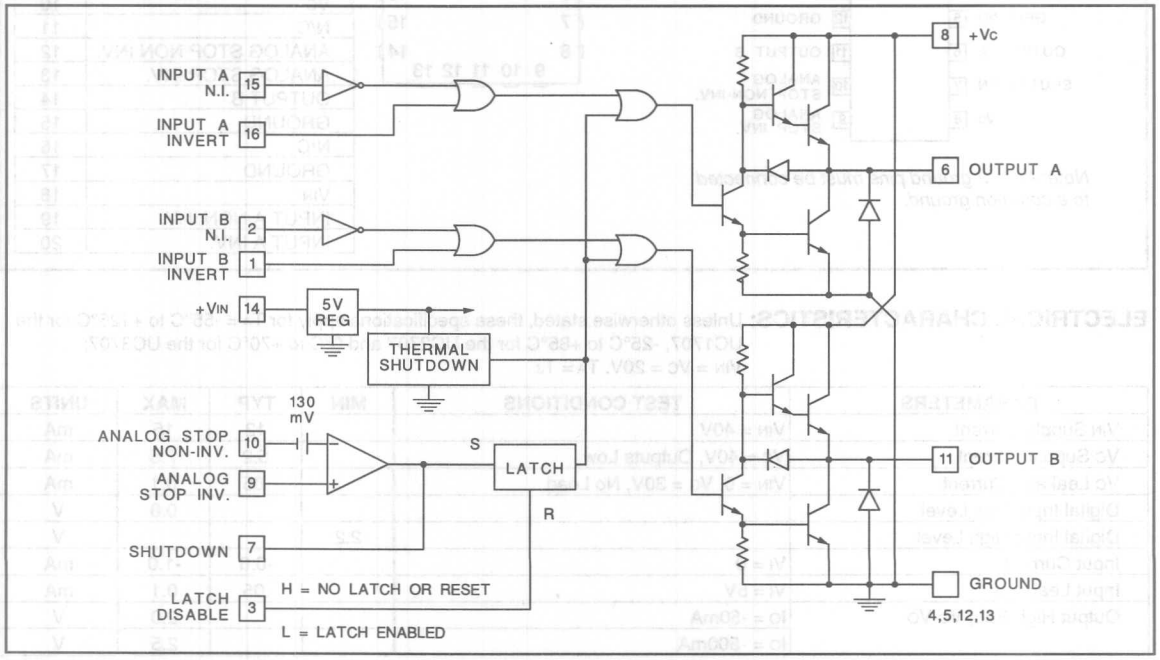
These devices are available in two-watt plastic "bat-wing" DIP for operation over a 0°C to 70°C temperature range and, with reduced power, in a hermetically sealed cerdip for -55°C to +125°C operation. Also available in surface mount DW, Q, L packages.

TRUTH TABLE (Each Channel)

INV.	N.I	OUT
H	H	L
L	H	H
H	L	L
L	L	L

$\overline{OUT} = \overline{INV}$ and N.I.
$\overline{OUT}$ = INV or N.I.

BLOCK DIAGRAM



3/97

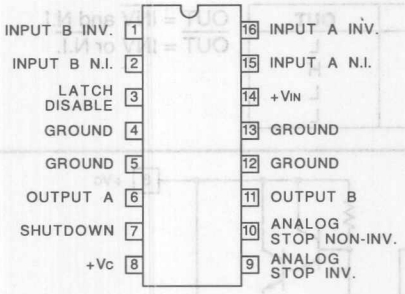
ABSOLUTE MAXIMUM RATINGS

	N-Pkg	J-Pkg
Supply Voltage, V_{IN}	40V	40V
Collector Supply Voltage, V_C	40V	40V
Output Current (Each Output, Source or Sink)		
Steady-State	±500mA	±500mA
Peak Transient	±1.5A	±1.0A
Capacitive Discharge Energy	20µJ	15µJ
Digital Inputs (See Note)	5.5V	5.5V
Analog Stop Inputs	V_{IN}	V_{IN}
Power Dissipation at T_A = 25°C (See Note)	2W	1W
Power Dissipation at T (Leads/Case) = 25°C (See Note)	5W	2W
Operating Temperature Range	-55°C to +125°C	
Storage Temperature Range	-65°C to +150°C	
Lead Temperature (Soldering, 10 Seconds)	300°C	

Note: All voltages are with respect to the four ground pins which must be connected together. All currents are positive into, negative out of the specified terminal.
Digital Drive can exceed 5.5V if input current is limited to 10mA.
Consult Packaging section of Databook for thermal limitations and considerations of package.

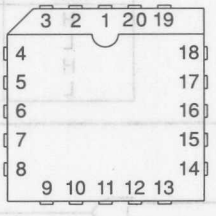
CONNECTION DIAGRAMS

DIL-16, SOIC-16
(TOP VIEW)
J or N Package, DW Package



Note: All four ground pins must be connected to a common ground.

PLCC-20, LCC-20
(TOP VIEW)
Q, L Packages



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
INPUT B INV.	2
INPUT B N.I.	3
LATCH DISABLE	4
GROUND	5
N/C	6
GROUND	7
OUTPUT A	8
SHUTDOWN	9
V_C	10
N/C	11
ANALOG STOP NON INV.	12
ANALOG STOP INV.	13
OUTPUT B	14
GROUND	15
N/C	16
GROUND	17
V_{IN}	18
INPUT A NON INV.	19
INPUT A INV.	20

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1707, -25°C to +85°C for the UC2707 and 0°C to +70°C for the UC3707; V_{IN} = V_C = 20V. T_A = T_J.

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{IN} Supply Current	V_{IN} = 40V		12	15	mA
V_C Supply Current	V_C = 40V, Outputs Low		5.2	7.5	mA
V_C Leakage Current	V_{IN} = 0, V_C = 30V, No Load		.05	0.1	mA
Digital Input Low Level				0.8	V
Digital Input High Level		2.2			V
Input Current	V_I = 0		-0.6	-1.0	mA
Input Leakage	V_I = 5V		.05	0.1	mA
Output High Sat., V_C-V_O	I_O = -50mA			2.0	V
	I_O = -500mA			2.5	V

ELECTRICAL CHARACTERISTICS (cont.):

Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1707, -25°C to +85°C for the UC2707 and 0°C to +70°C for the UC3707; V_{IN} = V_C = 20V. T_A = T_J.

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Low Sat., V_O	I_O = 50mA			0.4	V
	I_O = 500mA			2.5	V
Analog Threshold	V_{CM} = 0 to 15V	100	130	150	mV
Input Bias Current	V_{CM} = 0		-10	-20	µA
Thermal Shutdown			155		°C
Shutdown Threshold	Pin 7 Input	0.4	1.0	2.2	V
Latch Disable Threshold	Pin 3 Input	0.8	1.2	2.2	V

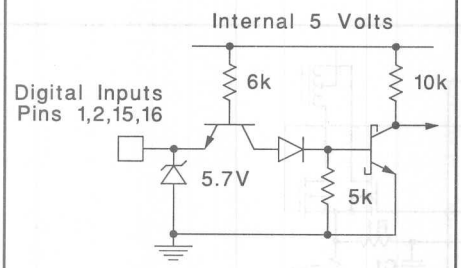
TYPICAL SWITCHING CHARACTERISTICS:

V_{IN} = V_C = 20V, T_A = 25°C. Delays measured to 10% output change.

PARAMETERS	TEST CONDITIONS	OUTPUT C_L =			UNIT
From Inv. Input to Output:		open	1.0	2.2	nF
Rise Time Delay		40	50	60	ns
10% to 90% Rise		25	40	50	ns
Fall Time Delay		30	40	50	ns
90% to 10% Fall		25	40	50	ns
From N. I. Input to Output:					
Rise Time Delay		30	40	50	ns
10% to 90% Rise		25	40	50	ns
Fall Time Delay		45	55	65	ns
90% to 10% Fall		25	40	50	ns
V_C Cross-Conduction Current Spike Duration	Ouput Rise	25			ns
	Output Fall	0			ns
Analog Shutdown Delay	Stop Non-Inv. = 0V Stop Inv. = 0 to 0.5V	180			ns
Digital Shutdown Delay	2V Input on Pin 7	50			ns

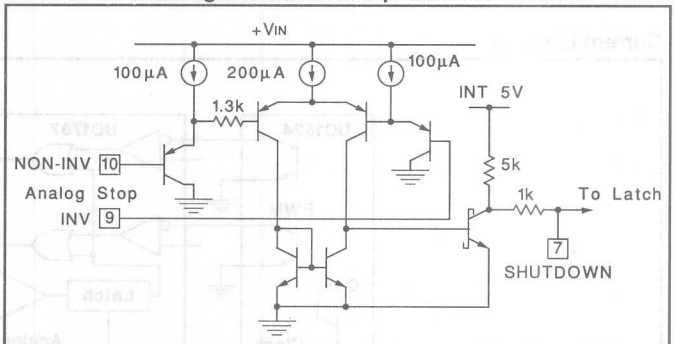
SIMPLIFIED INTERNAL CIRCUITRY

Typical Digital Input Gate



The input zener may be used to clamp input signal voltages higher than 5V as long as the zener current is limited to 10mA max. External pull-up resistors are not required.

Analog Shutdown Comparator Circuit

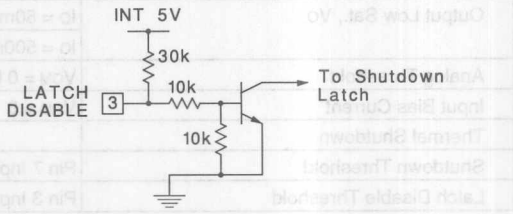


The input common-mode voltage range is from ground to (V_{IN}-3V). When not used both inputs should be grounded. Activate time is a function of overdrive with a typical value of 180ns. Pin 7 serves both as a comparator output and as a common digital shutdown input. A high signal here will accomplish the fastest turn off of both outputs. Note that "OFF" is defined as the outputs low. Pulling shutdown low defeats the latch operation regardless of its status.

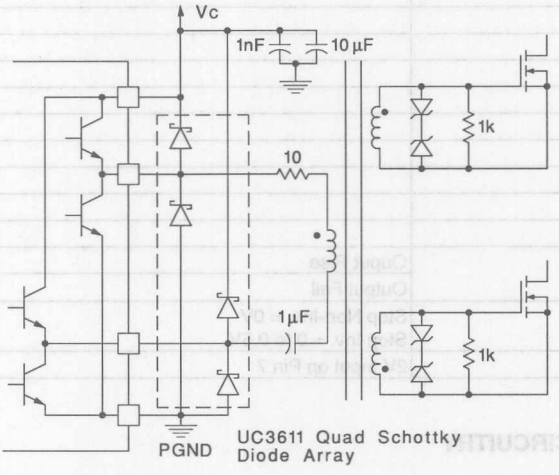
SIMPLIFIED INTERNAL CIRCUITRY (continued)

Latch Disable

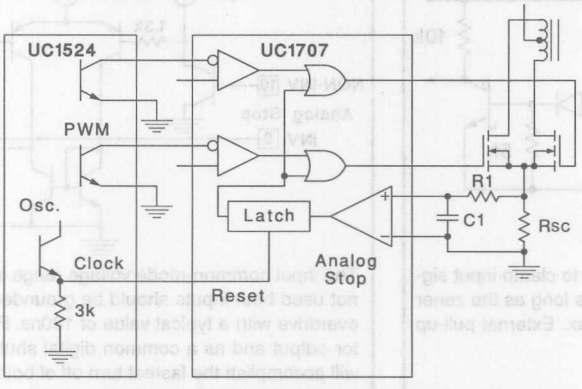
The Shutdown latch is disabled when pin 3 is open. An impedance of 4k or less from pin 3 to ground will allow a shutdown signal to set the latch which can then be reset by either recycling the V_{IN} supply or by momentarily (>200ns) raising pin 3 high.



Transformer Coupled Push-pull MOSFET Drive Circuit



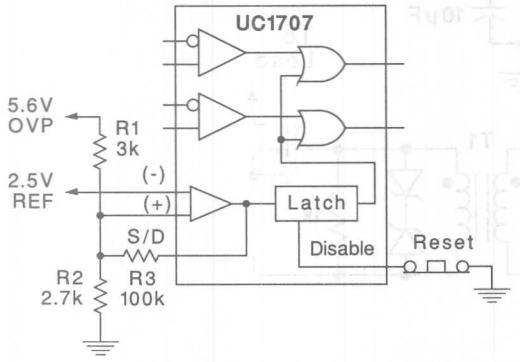
Current Limiting



The Analog shutdown can give pulse-by-pulse current limiting with a reset pulse from the clock output of the UC1524. R1C1 is used to filter leading edge spikes.

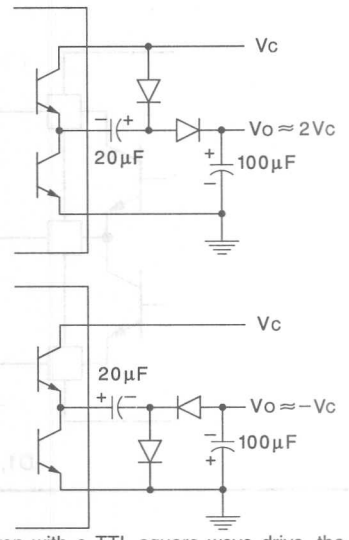
APPLICATIONS (continued)

Over-Voltage Protection



With an external reference, the shutdown comparator can be used for over-voltage protection. R1 and R2 set the shutdown level while R3 adds positive feedback for hysteresis.

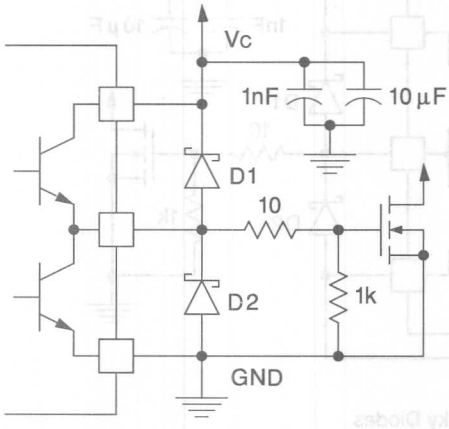
Charge Pump Circuits



When driven with a TTL square wave drive, the low output impedance of the UC1707 allows ready implementation of charge pump voltage converters.

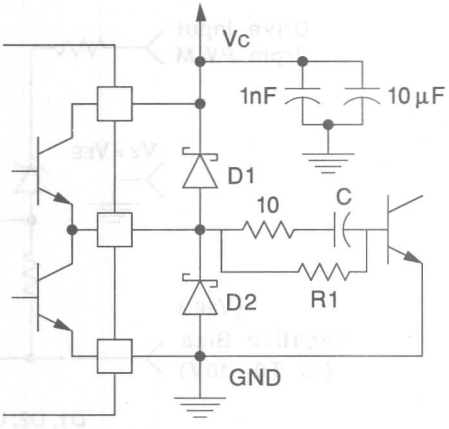
OUTPUT STAGE COUPLING

Power MOSFET Drive Circuit



D1, D2: UC3611 Schottky Diodes

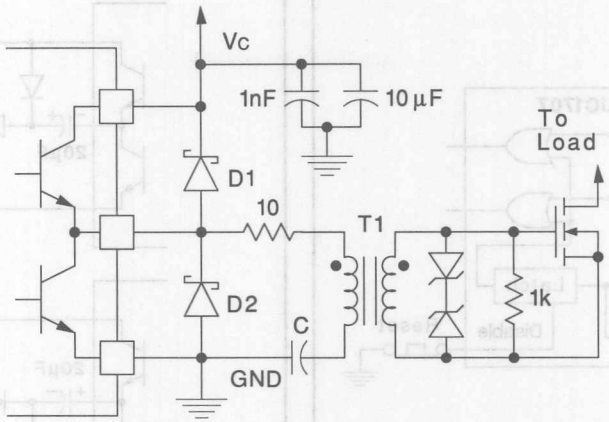
Power Bipolar Drive Circuit



D1, D2: UC3611 Schottky Diodes

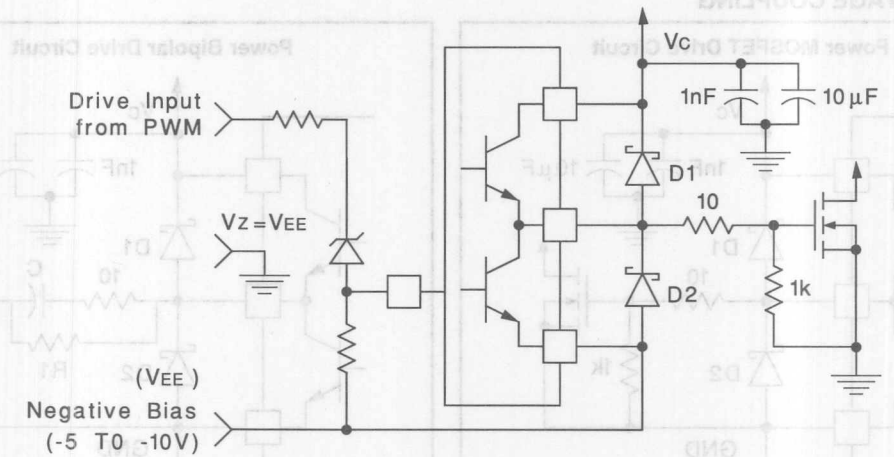
TRANSFORMER COUPLING

Transformer Coupled MOSFET Drive Circuit



D1, D2: UC3611 Schottly Diodes

Power MOSFET Drive Circuit Using Negative Bias Voltage and Level Shifting To Ground Reference PWM



D1, D2: UC3611 Schottky Diodes

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

Dual Non-Inverting Power Driver

FEATURES

- 3.0A Peak Current Totem Pole Output
- 5 to 35V Operation
- 25ns Rise and Fall Times
- 25ns Propagation Delays
- Thermal Shutdown and Under-Voltage Protection
- High-Speed, Power MOSFET Compatible
- Efficient High Frequency Operation
- Low Cross-Conduction Current Spike
- Enable and Shutdown Functions
- Wide Input Voltage Range
- ESD Protection to 2kV

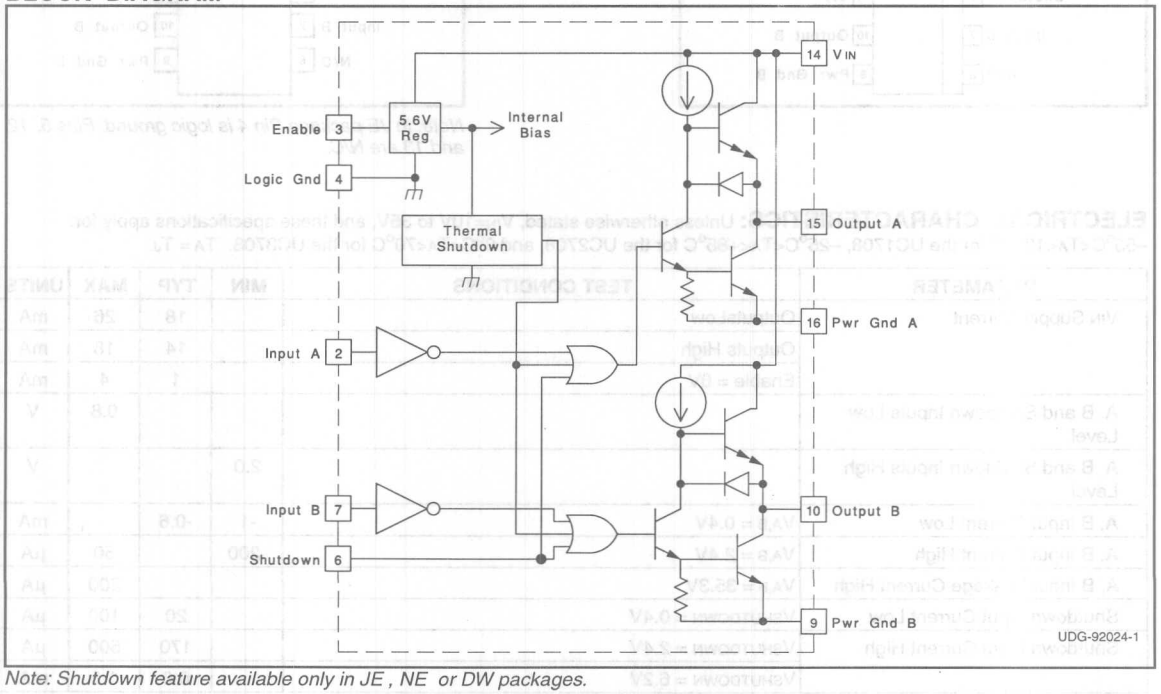
DESCRIPTION

The UC1708 family of power drivers is made with a high-speed, high-voltage, Schottky process to interface control functions and high-power switching devices – particularly power MOSFETs. Operating over a 5 to 35 volt supply range, these devices contain two independent channels. The A and B inputs are compatible with TTL and CMOS logic families, but can withstand input voltages as high as VIN. Each output can source or sink up to 3A as long as power dissipation limits are not exceeded.

Although each output can be activated independently with its own inputs, they can be forced low in common through the action of either a digital high signal at the Shutdown terminal or by forcing the Enable terminal low. The Shutdown terminal will only force the outputs low, it will not effect the behavior of the rest of the device. The Enable terminal effectively places the device in under-voltage lockout, reducing power consumption by as much as 90%. During under-voltage and disable (Enable terminal forced low) conditions, the outputs are held in a self-biasing, low-voltage, state.

The UC3708 and UC2708 are available in plastic 8-pin MINIDIP and 16-pin "bat-wing" DIP packages for commercial operation over a 0°C to +70°C temperature range and industrial temperature range of -25°C to +85°C respectively. For operation over a -55°C to +125°C temperature range, the UC1708 is available in hermetically sealed 8-pin MINIDIP and 16 pin DIP packages. Surface mount devices are also available.

BLOCK DIAGRAM



Note: Shutdown feature available only in JE , NE or DW packages.

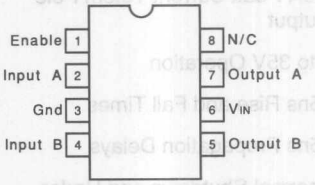
ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage V_{IN} 35V
Output Current (Each Output, Source or Sink)
  Steady-State 0.5A
  Peak Transient 3A
Ouput Voltage . . . . . -0.3 to (V_{IN} + 0.3)V
Enable and Shutdown Inputs . . . . . -0.3 to 6.2V
A and B Inputs . . . . . -0.3 to (V_{IN} + 0.3)V
Operating Junction Temperature (Note 2) . . . . . 150°C
Storage Temperature Range . . . . . -65° to 150°C
Lead Temperature (Soldering, 10 Seconds) . . . . . 300°C

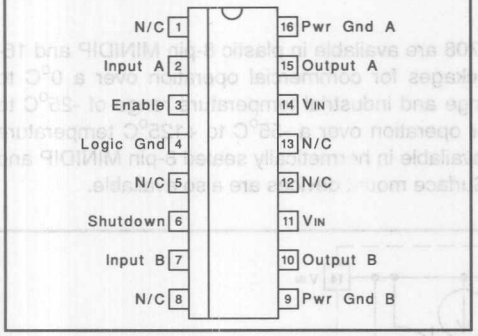
NOTE 1: All voltages are with respect to Logic Gnd pin. All currents are positive into, negative out of, device terminals.
NOTE 2: Consult Unitrode Integrated Circuits databook for information regarding thermal specifications and limitations of packages.

CONNECTION DIAGRAMS

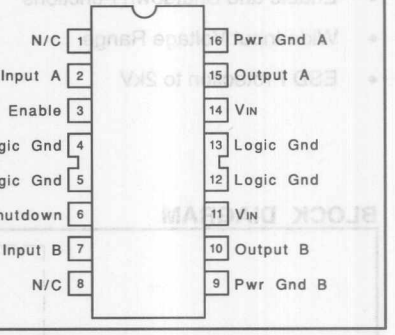
DIL-8 (Top View)
J Or N Package



SOIC-16 (Top View)
DW Package



DIL-16 (Top View)
JE or NE Package



Note: In JE package Pin 4 is logic ground. Pins 5, 12, and 13 are N/C.

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, V_{IN}=10V to 35V, and these specifications apply for: –55°C<T_A<125°C for the UC1708, –25°C<T_A<+85°C for the UC2708, and 0°C<T_A<70°C for the UC3708. T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{IN} Supply Current	OutputsLow		18	26	mA
	Outputs High		14	18	mA
	Enable = 0V		1	4	mA
A, B and Shutdown Inputs Low Level				0.8	V
A, B and Shutdown Inputs High Level		2.0			V
A, B Input Current Low	$V_{A,B}$ = 0.4V	-1	-0.6		mA
A, B Input Current High	$V_{A,B}$ = 2.4V	-200		50	µA
A, B Input Leakage Current High	$V_{A,B}$ = 35.3V			200	µA
Shutdown Input Current Low	$V_{SHUTDOWN}$ = 0.4V		20	100	µA
Shutdown Input Current High	$V_{SHUTDOWN}$ = 2.4V		170	500	µA
	$V_{SHUTDOWN}$ = 6.2V		0.6	1.5	mA

ELECTRICAL CHARACTERISTICS (cont.): Unless otherwise stated, V_{IN} = 10V to 35V, and these specifications apply for: –55°C<T_A<125°C for the UC1708, –25°C<T_A<+85°C for the UC2708, and 0°C<T_A<70°C for the UC3708. T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Enable Input Current Low	V_{ENABLE} = 0V	-600	-460	200	µA
Enable Input Current High	V_{ENABLE} = 6.2V			200	µA
Enable Threshold Rising			2.8	3.6	V
Enable Threshold Falling		1.0	2.4	3.4	V
Output High Sat., V_{IN} - V_{OUT}	I_{OUT} = -50mA			2.0	V
	I_{OUT} = -500mA			2.5	V
Output Low Sat., V_{OUT}	I_{OUT} = 50mA			0.5	V
	I_{OUT} = 500mA			2.5	V
Thermal Shutdown			155		°C

SWITCHING CHARACTERISTICS (Figure 1) (V_{IN} = 20V, delays measured to 10% output change.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
From A,B Input to Output:					
Rise Time Delay (TPLH)	CL = 0pF		25	40	ns
	CL = 1000pF (Note 3)		25	40	ns
	CL = 2200pF		30	45	ns
10% to 90% Rise (TTLH)	CL = 0pF		55	75	ns
	CL = 1000pF (Note 3)		25	50	ns
	CL = 2200pF		40	55	ns
Fall Time Delay (TPHL)	CL = 0pF		25	40	ns
	CL = 1000pF (Note 3)		25	45	ns
	CL = 2200pF		35	50	ns
90% to 10% Fall (TTHL)	CL = 0pF		15	20	ns
	CL = 1000pF (Note 3)		25	45	ns
	CL = 2200pF		40	55	ns
From Shutdown Input to Output					
Rise Time Delay (TPLH)	CL = 0pF		25	75	ns
	CL = 1000pF (Note 3)		30	75	ns
	CL = 2200pF		35	75	ns
10% to 90% Rise (TTLH)	CL = 0pf		50	75	ns
	CL = 1000pF (Note 3)		25	50	ns
	CL = 2200pF		40	55	ns
Fall Time Delay (TPHL)	CL = 0pF		25	45	ns
	CL = 1000pF (Note 3)		30	50	ns
	CL = 2200pF		35	55	ns
90% to 10% Fall (TTHL)	CL = 0pF		25	20	ns
	CL = 1000pF (Note 3)		25	45	ns
	CL = 2200pF		40	55	ns
Total Supply Current	F = 200kHz, 50% duty cycle, both channels; CL = 0pF		23	25	mA
	F = 200kHz, 50% duty cycle, both channels; CL = 2200pF		38	45	mA

NOTE 3: These parameters, specified at 1000pF, although guaranteed over recommended operating conditions, are not tested in production.

Figure 1: AC Test Circuit and Switching Time Waveforms

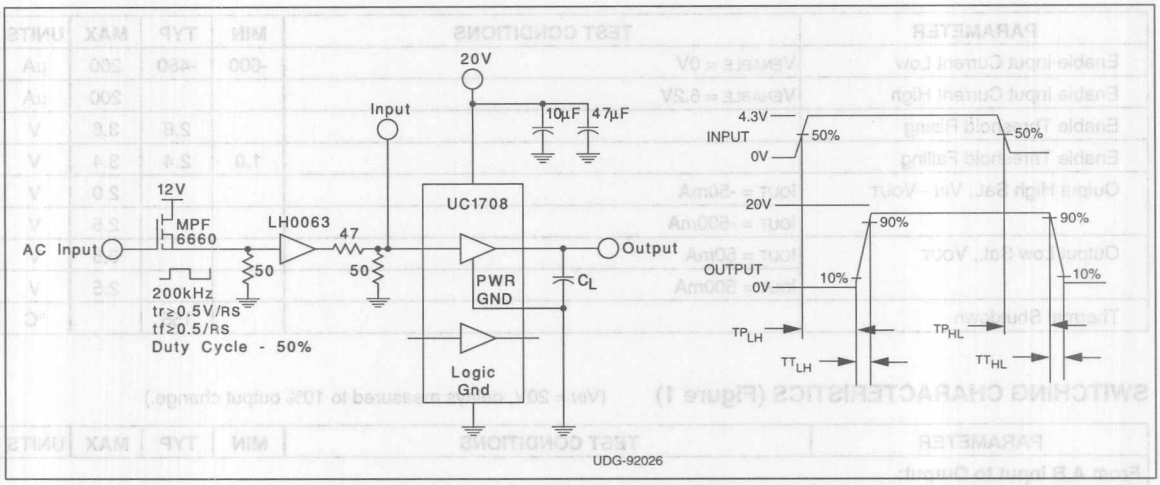
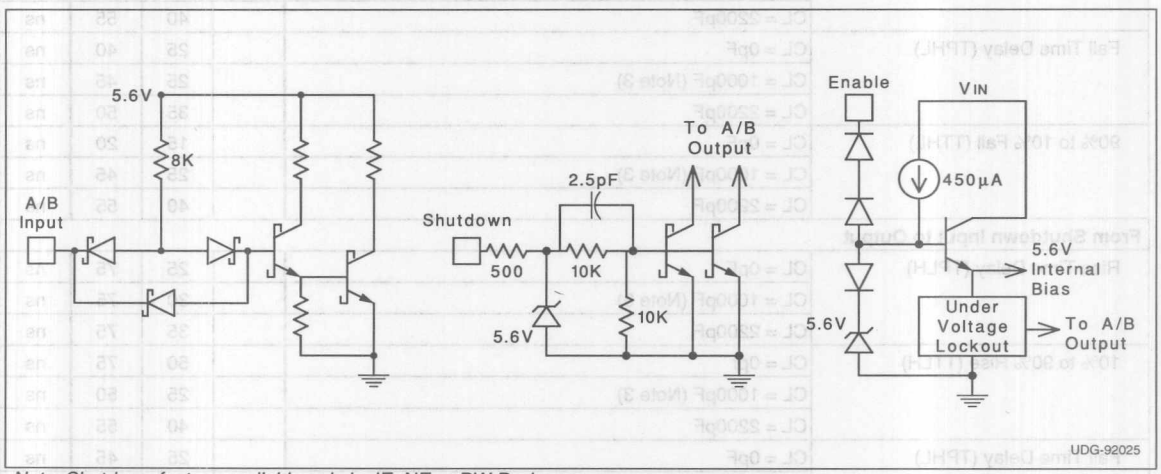


Figure 2: Equivalent Input Circuits



Note: Shutdown feature available only in JE, NE or DW Packages.

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UNITRODE

UC1709
UC2709
UC3709

Dual High-Speed FET Driver

FEATURES

- 1.5 Amp Source/Sink Drive
- Pin Compatible with 0026 Products
- 40 ns Rise and Fall into 1000 pF
- Low Quiescent Current
- 5V to 40V Operation
- Thermal Protection

DESCRIPTION

The UC3709 family of power drivers is an effective low-cost solution to the problem of providing fast turn-on and off for the capacitive gates of power MOSFETs. Made with a high-speed Schottky process, these devices will provide up to 1.5 amps of either source or sink current from a totem-pole output stage configured for minimal cross-conduction current spike.

The UC3709 is pin compatible with the MMH0026 or DS0026, and while the delay times are longer, the supply current is much less than these older devices.

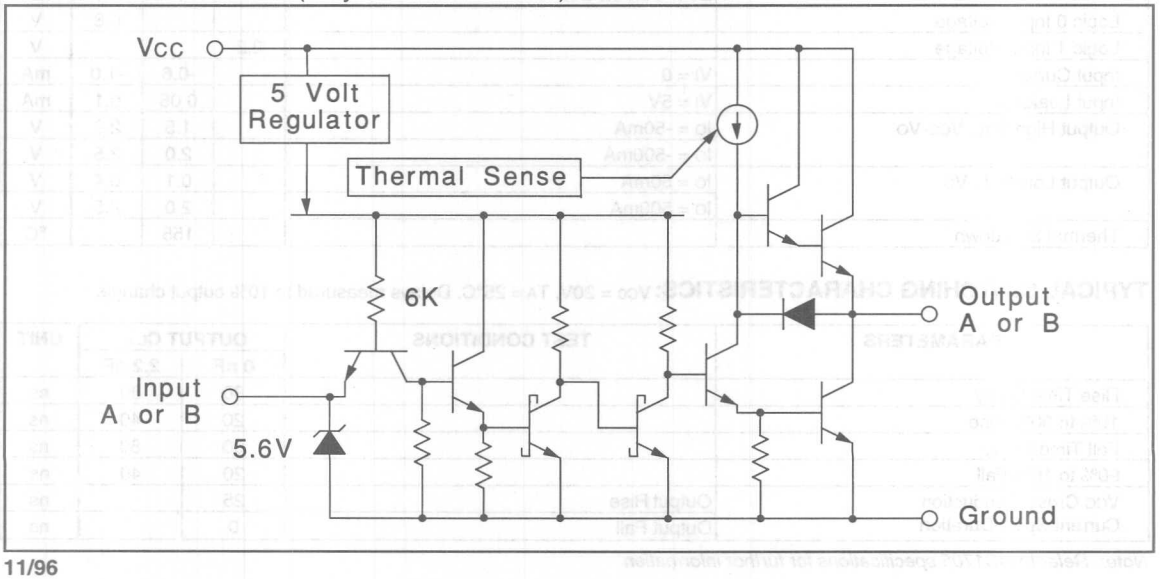
With inverting logic, these units feature complete TTL compatibility at the inputs with an output stage that can swing over 30V. This design also includes thermal shutdown protection.

ABSOLUTE MAXIMUM RATINGS

	N-Pkg	J-Pkg
Supply Voltage, V_{CC}	40V	40V
Output Current (Source or Sink)		
Steady-State	±500	±500 mA
Peak Transient	±1.5A	±1.0A
Capacitive Discharge Energy	20 µJ	15 µJ
Digital Inputs (See Note)	5.5V	5.5V
Power Dissipation at T_A = 25°C	1W	1W
Power Dissipation at T_C = 25°C	3W	2W
Operating Temperature Range	-55°C to +125°C	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C	-65°C to +150°C
Lead Temperature (Soldering, 10 Seconds)	300°C	300 °C

Note: All currents are positive into, negative out of the specified terminals. Digital drive can exceed 5.5V if input current is limited to 10mA. Consult Packaging section of Databook for thermal limitations and considerations of package.

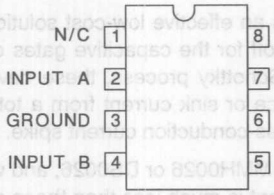
SIMPLIFIED SCHEMATIC (Only One Driver Shown)



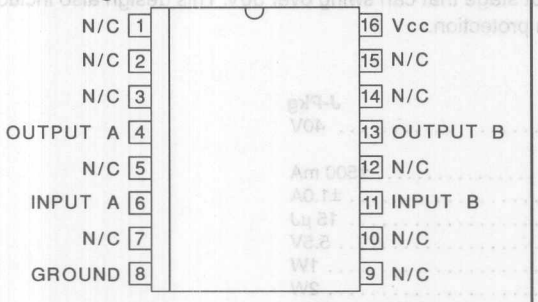
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CONNECTION DIAGRAMS

8 PIN DIL (TOP VIEW)
N or J Package



SOIC-16 (TOP VIEW)
DW Package



PLCC-20, LCC-20 (TOP VIEW)
Q, L Packages



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
N/C	2
INPUT A	3
N/C	4
N/C	5
GROUND	6
N/C	7
N/C	8
INPUT B	9
N/C	10
N/C	11
OUTPUT B	12
N/C	13
N/C	14
N/C	15
Vcc	16
N/C	17
N/C	18
N/C	19
OUTPUT A	20

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1709, -40°C to +85°C for the UC2709, and 0°C to +70°C for the UC3709; V_{CC} = 20V, $T_A = T_J$.

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	Both Outputs High		10	12	mA
	Both Outputs Low		7	10	mA
Logic 0 Input Voltage				0.8	V
Logic 1 Input Voltage		2.2			V
Input Current	V_I = 0		-0.6	-1.0	mA
Input Leakage	V_I = 5V		0.05	0.1	mA
Output High Sat., V_{CC}-V_O	I_O = -50mA		1.5	2.0	V
	I_O = -500mA		2.0	2.5	V
Output Low Sat., V_O	I_O = 50mA		0.1	0.4	V
	I_O = 500mA		2.0	2.5	V
Thermal Shutdown			155		°C

TYPICAL SWITCHING CHARACTERISTICS:

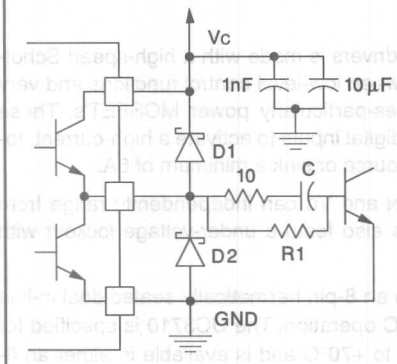
V_{CC} = 20V, T_A = 25°C. Delays measured to 10% output change.

PARAMETERS	TEST CONDITIONS	OUTPUT C_L =		UNIT
		0 nF	2.2 nF	
Rise Time Delay		80	80	ns
10% to 90% Rise		20	40	ns
Fall Time Delay		60	80	ns
90% to 10% Fall		20	40	ns
V_{CC} Cross-Conduction Current Spike Duration	Output Rise	25		ns
	Output Fall	0		ns

Note: Refer to UC1705 specifications for further information

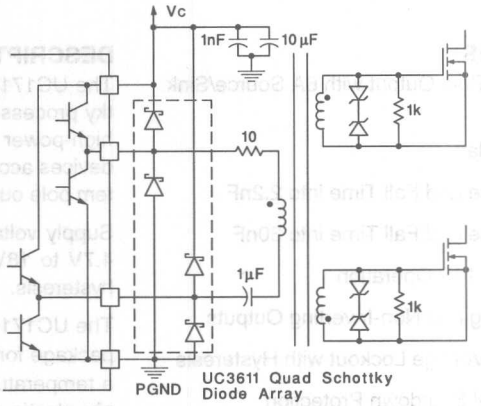
APPLICATIONS

Power Bipolar Drive Circuit



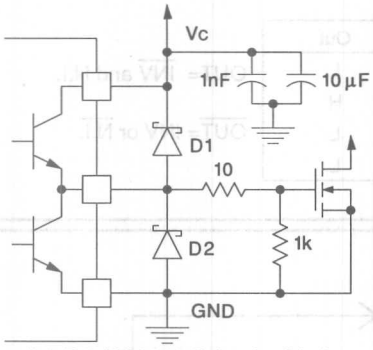
D1, D2: UC3611 Schottky Diodes

Transformer Coupled Push-Pull MOSFET Drive Circuit



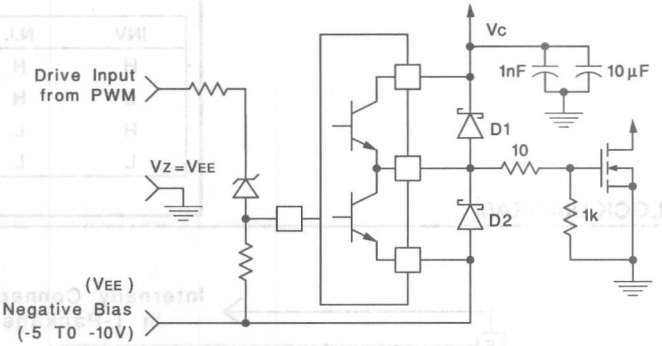
D1, D2: UC3611 Schottky Diodes

Power MOSFET Drive Circuit



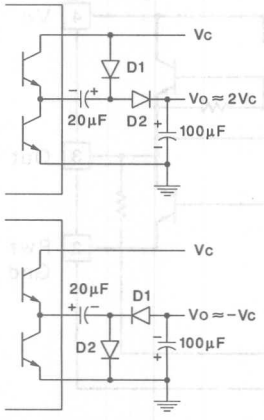
D1, D2: UC3611 Schottky Diodes

Power MOSFET Drive Circuit Using Negative Bias Voltage and Level Shifting To Ground Referenced PWMS

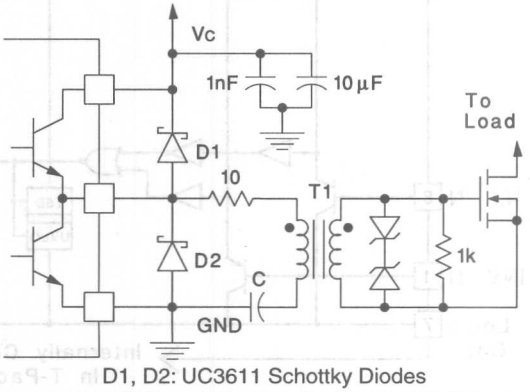


D1, D2: UC3611 Schottky Diodes

Charge Pump Circuits



Transformer Coupled MOSFET Drive Circuit



D1, D2: UC3611 Schottky Diodes

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High Current FET Driver

FEATURES

- Totem Pole Output with 6A Source/Sink Drive
- 5ns Delay
- 5ns Rise and Fall Time into 2.2nF
- 5ns Rise and Fall Time into 30nF
- 4.7V to 18V Operation
- Inverting and Non-Inverting Outputs
- Under-Voltage Lockout with Hysteresis
- Thermal Shutdown Protection
- MINIDIP and Power Packages

DESCRIPTION

The UC1710 family of FET drivers is made with a high-speed Schottky process to interface between low-level control functions and very high-power switching devices-particularly power MOSFET's. These devices accept low-current digital inputs to activate a high-current, totem pole output which can source or sink a minimum of 6A.

Supply voltages for both V_{IN} and V_C can independently range from 4.7V to 18V. These devices also feature under-voltage lockout with hysteresis.

The UC1710 is packaged in an 8-pin hermetically sealed dual in-line package for -55°C to +125°C operation. The UC3710 is specified for a temperature range of 0°C to +70°C and is available in either an 8-pin plastic dual in-line or a 5-pin, TO-220 package. Surface mount devices are also available.

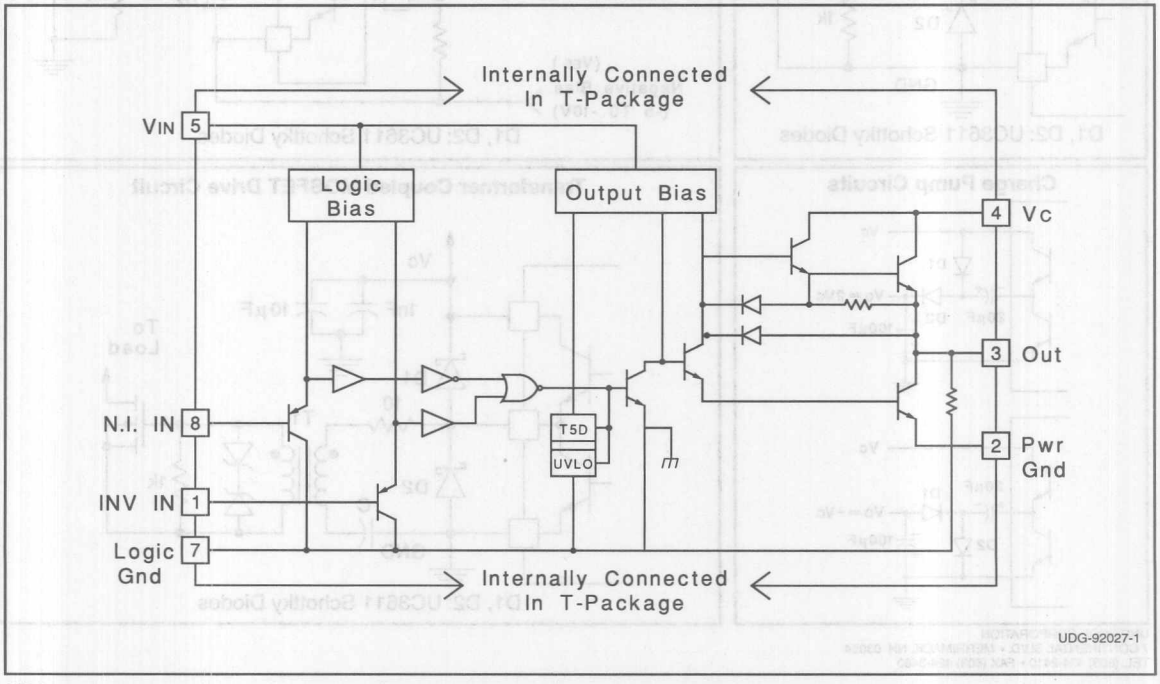
TRUTH TABLE

INV	N.I.	Out
H	H	L
L	H	H
H	L	L
L	L	L

$OUT = \overline{INV}$ and N.I.

$\overline{OUT}$ = INV or $\overline{N.I.}$

BLOCK DIAGRAM



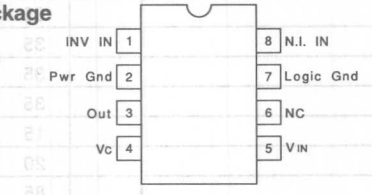
ABSOLUTE MAXIMUM RATINGS

	N-Pkg	J-Pkg	T-Pkg
Supply Voltage, Vin	20V	20V	20V
Collector Supply Voltage, Vc	20V	20V	20V
Operating Voltage	18V	18V	18V
Output Current (Source or Sink)			
Steady-State	±500mA	±500mA	±1A
Digital Inputs	-0.3V-VIN	-0.3V-VIN	-0.3V-VIN
Power Dissipation at Ta=25°C	1W	1W	3W
Power Dissipation at T (Case) = 25°C	2W	2W	25W
Operating Junction Temperature	-55°C-+150°C	-55°C-+150°C	-55°C-+150°C
Storage Temperature	-65°C-+150°C	-65°C-+150°C	-65°C-+150°C
Lead Temperature (Soldering, 10 seconds)	300°C	300°C	300°C

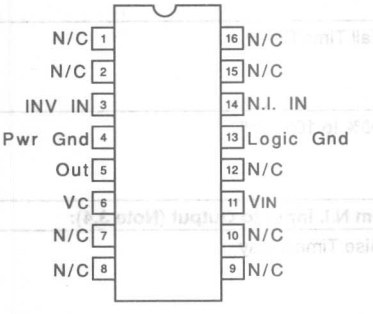
Note 1: All currents are positive into, negative out of the specified terminal.
Note 2: Consult Unitrode Integrated Circuits databook for information regarding thermal specifications and limitations of packages.

CONNECTION DIAGRAMS

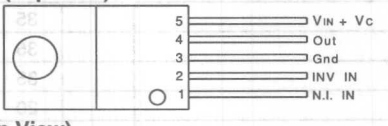
DIL-8 MINIDIP (Top View)
J or N Package



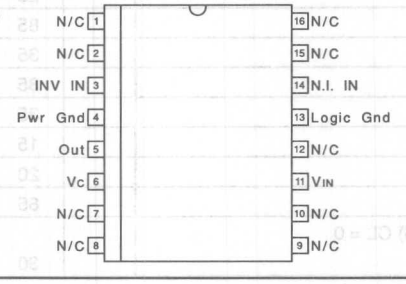
DIL-16 (Top View)
SP Package



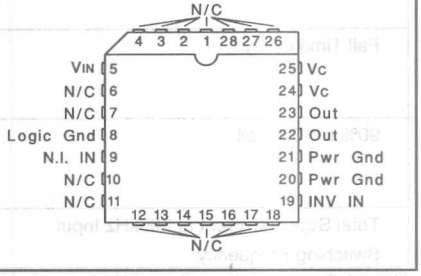
5-Pin TO-220 (Top View)
T Package



SOIC-16 (Top View)
DW Package



PLCC-28 (Top View)
QP Package



ELECTRICAL CHARACTERISTICS:

(Unless otherwise stated, these specifications apply for TA =- 55°C to +125°C for the UC1710 and TA = 0 °C to +70°C for the UC3710; VIN = Vc = 15V, No load TA = TJ..)

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VIN Supply Current	VIN=18V, Vc=18V, Output Low		26	35	mA
	VIN=18V, Vc=18V, Output High		21	30	mA
Vc Supply Current	VIN=18V, Vc=18V, Output Low		1.5	5.0	mA
	VIN=18V, Vc=18V,Output High		5.0	8	mA
UVLO Threshold	VIN High to Low	3.8	4.1	4.4	V
	VIN Low to High	4.1	4.4	4.8	V
UVLO Threshold Hysteresis		0.1	0.3	0.5	V
Digital Input Low Level				0.8	V
Digital Input High Level		2.0			V
Digital Input Current	Digital Input=0.0V	-70	-4.0		µA

ELECTRICAL CHARACTERISTICS (cont.)

(Unless otherwise stated, these specifications apply for T_A =- 55°C to +125°C for the UC1710 and T_A = 0 °C to +70°C for the UC3710; V_{IN} = V_C = 15V, No load. T_A = T_J.)

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output High Sat., Vc-Vo	Io=-100mA		1.35	2.2	V
	Io=-6A		3.2	4.5	V
Output Low Sat., Vo	Io = 100mA		0.25	0.6	V
	Io = 6A		3.4	4.5	V
Thermal Shutdown			165		°C
From Inv.,Input to Output (Note 3, 4):					
Rise Time Delay	CL = 0		35	70	ns
	CL = 2.2nF		35	70	ns
	CL = 30nF		35	70	ns
10% to 90% Rise	CL = 0		20	40	ns
	CL = 2.2nF		25	40	ns
	CL = 30nF		85	150	ns
Fall Time Delay	CL = 0		35	70	ns
	CL = 2.2nF		35	70	ns
	CL = 30nF		35	80	ns
90% to 10% Fall	CL = 0		15	40	ns
	CL = 2.2nF		20	40	ns
	CL = 30nF		85	150	ns
From N.I. Input to Output (Note 3,4):					
Rise Time Delay	CL = 0		35	70	ns
	CL = 2.2nF		35	70	ns
	CL = 30nF		35	70	ns
10% to 90% Rise	CL = 0		20	40	ns
	CL = 2.2nF		25	40	ns
	CL = 30nF		85	150	ns
Fall Time Delay	CL = 0		35	70	ns
	CL = 2.2nF		35	70	ns
	CL = 30nF		35	80	ns
90% to 10% Fall	CL = 0		15	40	ns
	CL = 2.2nF		20	50	ns
	CL = 30nF		85	150	ns
Total Supply Current at 200kHz Input Switching Frequency	T_A = 25°C (Note 5) CL = 0		30	40	mA

Note: 3. Delay measured from 50% input change to 10% output change.
Note: 4. Those parameters with CL = 30nF are not tested in production.
Note: 5. Inv. Input pulsed at 50% duty cycle with N.I. Input = 3V. or N.I. Input pulsed at 50% duty cycle with Inv. Input = 0V.

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Dual Ultra High-Speed FET Driver

FEATURES

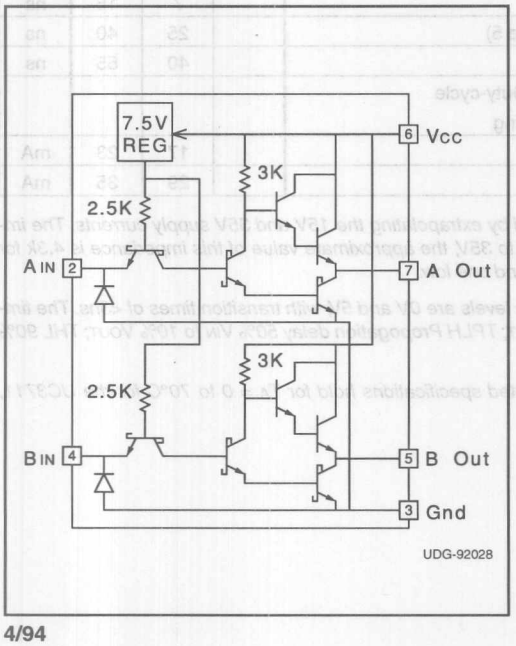
- 25ns Rise and Fall into 1000pF
- 15ns Propagation Delay
- 1.5A Source or Sink Output Drive
- Operation with 5V to 35V Supply
- High-Speed Schottky NPN Process
- 8-PIN MINIDIP Package

ABSOLUTE MAXIMUM RATINGS (note 1)

Input Supply Voltage, Vcc 40V
Output Current (Source or Sink)
  Steady State ..... +/-500mA
  Peak Transient ..... +/-1.5A
Inputs
Maximum Forced Voltage..... -0.3V to 7V
Maximum Forced Current..... +/- 10mA
Power Dissipation 1W
Operating Junction Temperature ..... -55°C to +150°C

Note 1: Unless otherwise indicated, voltages are reference to ground and currents are positive into, negative out of, the specified terminals. All reliability information for this device has been gathered at an ambient air temperature of 125°C, and a supply voltage of 25V.
Note 2: Consult Unitrode Integrated Circuits databook for information regarding thermal specifications and limitations of packages.

BLOCK DIAGRAM



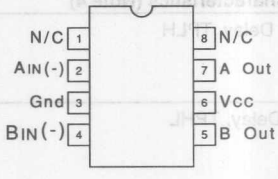
DESCRIPTION

The UC1711 family of FET drivers are made with an all-NPN Schottky process in order to optimize switching speed, temperature stability, and radiation resistance. The cost for these benefits is a quiescent supply current which varies with both output state and supply voltage. For lower power requirements, refer to the the UC1709 family which is both pin compatible with, and functionally equivalent to the UC1711.

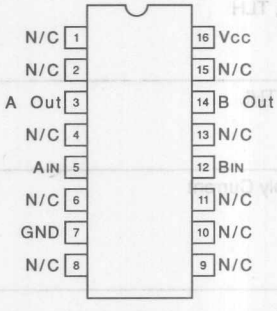
These devices implement inverting logic with TTL compatible inputs, and output stages which will either source, or sink in excess of 1.5A of load current with minimal cross-conduction charge. Due to their monolithic construction, the channels are well matched and can be paralleled for doubled output current capability.

CONNECTION DIAGRAMS

DIL-8 (Top View)
J or N Package



DIL-16 (Top View)
JE or NE Package



PLCC-20 (Top View)
QP Package



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
AIN	2
N/C	3 - 5
GND	6
N/C	7 - 9
BIN	10
N/C	11 - 13
B Out	14
N/C	15
Vcc	16
N/C	17
A Out	18
N/C	19
N/C	20

ELECTRICAL CHARACTERISTICS: Unless otherwise stated specifications hold for T_A = 0 to 70°C for the UC3711, and T_A = -55 to 125°C for the UC1711, Vcc = 15V. T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply					
Supply Current (Note 3)	Both inputs = 0V; Vcc = 15V		11	15	mA
	Both inputs = 5V; Vcc = 15V		20	27	mA
	Both inputs = 0V; Vcc = 35V		15	20	mA
	Both inputs = 5V; Vcc = 35V		41	56	mA
Logic Inputs					
Logic 0 Input Voltage				0.8	V
Logic 1 Input Voltage		2.2			V
Input Current	V_{IN} = 0V	-5.0	-2.7		mA
	V_{IN} = 5V		0.5	2.0	mA
Output Stages					
Output High Level	I_{SOURCE} = 20mA, below Vcc		1.5	2.0	V
	I_{SOURCE} = 200mA, below Vcc		2.0	3.0	V
Output Low Level	I_{SINK} = 20mA		.25	0.4	V
	I_{SINK} = 200mA		0.4	1.0	V
Switching Characteristics (Note 4)					
Rise Time Delay, TPLH	C_{LOAD} = 0		10	40	ns
	C_{LOAD} = 1000pF, (Note 5)		15	50	ns
	C_{LOAD} = 2200pF		20	55	ns
Fall Time Delay, TPHL	C_{LOAD} = 0		3	20	ns
	C_{LOAD} = 1000pf, (Note 5)		5	20	ns
	C_{LOAD} = 2200pF		5	20	ns
Rise Time, TLH	C_{LOAD} = 0, (Note 5)		12	25	ns
	C_{LOAD} = 1000pF, (Note 5)		25	40	ns
	C_{LOAD} = 2200pF		40	55	ns
Fall Time, THL	C_{LOAD} = 0, (Note 5)		7	15	ns
	C_{LOAD} = 1000pF, (Note 5)		25	40	ns
	C_{LOAD} = 2200pF		40	55	ns
Total Supply Current	Freq = 200kHz, 50% Duty-cycle Both Channels Switching				
	C_{LOAD} = 0		17	23	mA
	C_{LOAD} = 2200pF		29	35	mA

Note 3: Supply currents at other input supply votages can be calculated by extrapolating the 15V and 35V supply currents. The impedance of the chip at the Vcc pin is linear for supply voltages from 8V to 35V, the approximate value of this impedance is 4.3k for both inputs low, 0.94k for both inputs high, and 1.54k for one input high and one low.

Note 4: Switching test conditions are, Vcc = 15V, Input voltage waveform levels are 0V and 5V, with transition times of <3ns. The timing terms are defined as : TPHL Propagation delay 50% V_{IN} to 90% V_{OUT}; TPLH Propogation delay 50% V_{IN} to 10% V_{OUT}; THL 90% V_{OUT} to 10% V_{OUT}; TLH 10% V_{OUT} to 90% V_{OUT}.

Note 5: This specification not tested in production.Unless otherwise stated specifications hold for T_A = 0 to 70°C for the UC3711, and T_A = -55 to 125°C for the UC1711, Vcc = 15V. T_A = T_J.

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Smart Power Switch

FEATURES

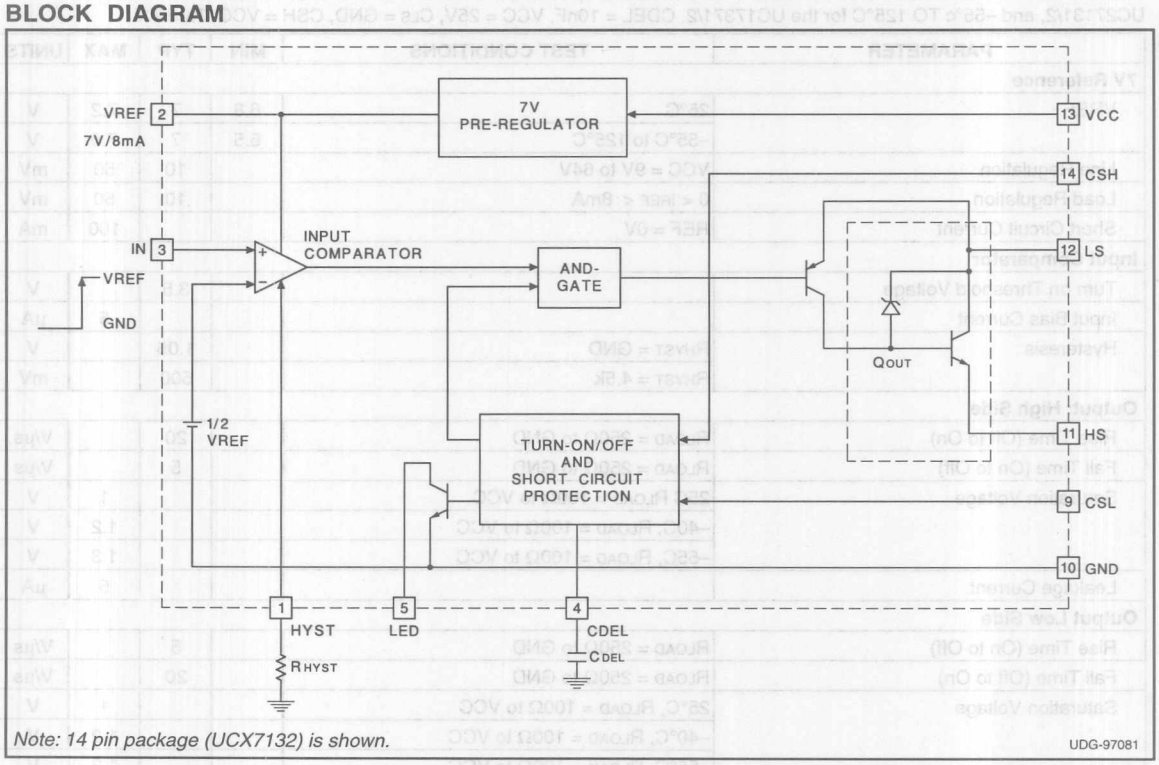
- 250mA Continuous Output Current
- Low Side or High Side Switch Configuration
- 9V to 65V Operation
- Overload and Short Circuit Protection
- Power Interruption Protection
- +7V Regulated Voltage
- 1V Saturation Voltages
- 2mA Quiescent Current
- Programmable Overcurrent and Power Interruption Protection (on UC37132)
- 1% to 30% Programmable Input Comparator Hysteresis (on UC37132)

DESCRIPTION

The UC37131 and UC37132 are a family of smart power switches which can drive resistive or inductive loads from the high side or low side. The input to the switch is driven by a low voltage signal, typically 5V, and features adjustable hysteresis. The output of the UC37131/2 can switch a load between 9V and 65V. Output current capability is 250mA continuous or 600mA peak.

The UC37131/2 can be configured low side (load to VDD) or high side (load to ground). Both configurations provide high current switching with low saturation voltages which can drive resistive or inductive loads. The chip has inherent smart features that allow for programmable turn on delay in enabling the output following startup. The same capacitor that specifies the turn on delay is also used to program a VCC power interruption time. If VCC drops below a threshold for a time specified by this capacitor, the output is turned off and a new turn on delay will be re-triggered. Similarly, if high current persists longer than the response delay, the output driver will be switched off for n-times the response delay.

BLOCK DIAGRAM



Note: 14 pin package (UCX7132) is shown.

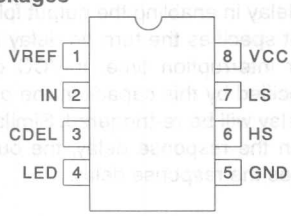
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3/97

ABSOLUTE MAXIMUM RATINGS

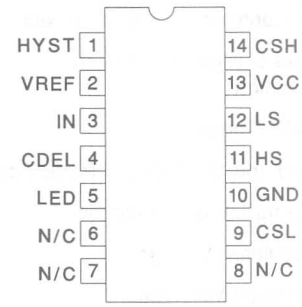
VCC, LS, HS. 65V
CSH (UCX7131)) 65V
Output Current
  Continuous 250mA
  Peak. 600mA
Remaining Pin Voltages . . . . . –0.3V to 9V
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C
Currents are positive into, negative out of the specified terminal.
Consult Packaging Section of Databook for thermal limitations and considerations of packages.

DIL-8, SOIC-8 (Top View) (for UCX7131)
J or N, D Packages



CONNECTION DIAGRAM

DIL-14, SOIC-14 (Top View) (for UCX7132)
J or N, D Packages



ELECTRICAL CHARACTERISTICS

Unless otherwise specified, 0°C to 70°C for the UC37131/2, –40°C to 85°C for the UC27131/2, and –55°c TO 125°C for the UC17371/2. CDEL = 10nF, VCC = 25V, C_{LS} = GND, CSH = VCC. T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
7V Reference					
VREF	25°C	6.8	7	7.2	V
	–55°C to 125°C	6.5	7	7.5	V
Line Regulation	VCC = 9V to 64V		10	50	mV
Load Regulation	0 < I_{REF} < 8mA		10	50	mV
Short Circuit Current	REF = 0V			100	mA
Input Comparator					
Turn on Threshold Voltage			3.5		V
Input Bias Current				5	µA
Hysteresis	R_{HYST} = GND		1.05		V
	R_{HYST} = 4.5k		500		mV
Output: High Side					
Rise Time (Off to On)	R_{LOAD} = 250Ω to GND		20		V/µs
Fall Time (On to Off)	R_{LOAD} = 250Ω to GND		5		V/µs
Saturation Voltage	25C R_{LOAD} = 100Ω to VCC			1	V
	–40C, R_{LOAD} = 100Ω to VCC			1.2	V
	–55C, R_{LOAD} = 100Ω to VCC			1.3	V
Leakage Current				5	µA
Output Low Side					
Rise Time (On to Off)	R_{LOAD} = 250Ω to GND		5		V/µs
Fall Time (Off to On)	R_{LOAD} = 250Ω to GND		20		V/µs
Saturation Voltage	25°C, R_{LOAD} = 100Ω to VCC			1	V
	–40°C, R_{LOAD} = 100Ω to VCC			1.2	V
	–55°C, R_{LOAD} = 100Ω to VCC			1.3	V

ELECTRICAL CHARACTERISTICS Unless otherwise specified, 0°C to 70°C for the UC37131/2, –40°C to 85°C for the UC27131/2, and –55°c TO 125°C for the UC17371/2. CDEL = 10nF, VCC = 25V, C_{LS} = GND, CSH = VCC. $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Outside: Low Side (cont.)					
Leakage Current				5	µA
VCC Fault Section					
Output Turn On Delay	Step VCC from 0V to 9V (See Figure 3a)		12.8		ms
Output Turn Off Delay	Pulse VCC = 25V to 0V (See Figure 3b)		500		µs
VCC Turn Off Threshold	Pulse VCC Low		7		V
Overcurrent Fault Section					
Overload Ignore Time	Step I_{LOAD}: VCC – CSH = 200mV and CSL – GND = 200mV		75		µs
Time Output Stays Off	Overload Time = 100µs		500		µs
High Side Current Threshold	VCC – CSH		150		mV
Low Side Current Threshold	CSL – GND		150		mV
LED Output					
I Sink, Overload Ignore Time	VCC – CSH = 0.6 or CSL – GND = 0.6		3		mA
Overall					
Delay to Output			2		µs
ICC	Output Off			2	mA
	I_L = 1mA (High and Low Side)			3	mA
	I_L = 250mA (High and Low Side)			7	mA

PIN DESCRIPTION

CDEL: The capacitor used to program both VCC pulse interruption time and power turn-on delay. The capacitor discharge time corresponds to VCC interruption and the charge time to VCC turn-on delay. The ratio between turn-on delay and turn-off delay will be fixed based on a fixed internal charge and discharge currents and voltage thresholds. The same fault circuitry and capacitor is used for short circuit and overload protection. If an overcurrent or short circuit is detected, the capacitor starts charging and turns off the output if it persists at the end of its charge time. The output will stay off for approximately 100 times longer than the programmed charge time. After short circuit recovery, the output will be reactivated in order to check if the short circuit was removed or not. If the overcurrent persists the chip will work in this pulsing mode.

CSH: The pin used to program the current limit for high side applications by connecting a resistor between VCC and CSH. An over load current is detected when the voltage drop between VCC and CSH exceeds 150mV (on the UCX7132).

CSL: The pin used to program the current limit for low side applications by connecting a resistor between CSL and GND. An over load current is detected when the voltage drop between CSL and GND exceeds 150mV (on UCX7321).

GND: The reference point for the internal reference, all thresholds, and the return for the remainder of the device.

HS: The output of the switching transistor in the high side configuration. The emitter of the output transistor is the HS pin which is connected to the load.

HYST: The pin used to program the input comparator hysteresis by connecting a resistor to ground. The hysteresis defaults to 30% with HYST grounded.

IN: The input to the comparator that detects when the output transistor should be turned on. The input threshold is 3.5V (1/2 REF).

LED: Open collector output intended to drive an LED during overcurrent detection.

LS: The output of the switching transistor in the low side configuration. The collector of the output transistor is the LS pin which is connected to the load.

VREF: The 7V regulated reference capable of supplying up to 8mA. The maximum bypass capacitor is 33nF.

VCC: The supply voltage for the chip. Bypass this pin with a good quality ceramic capacitor to ground.

APPLICATION INFORMATION

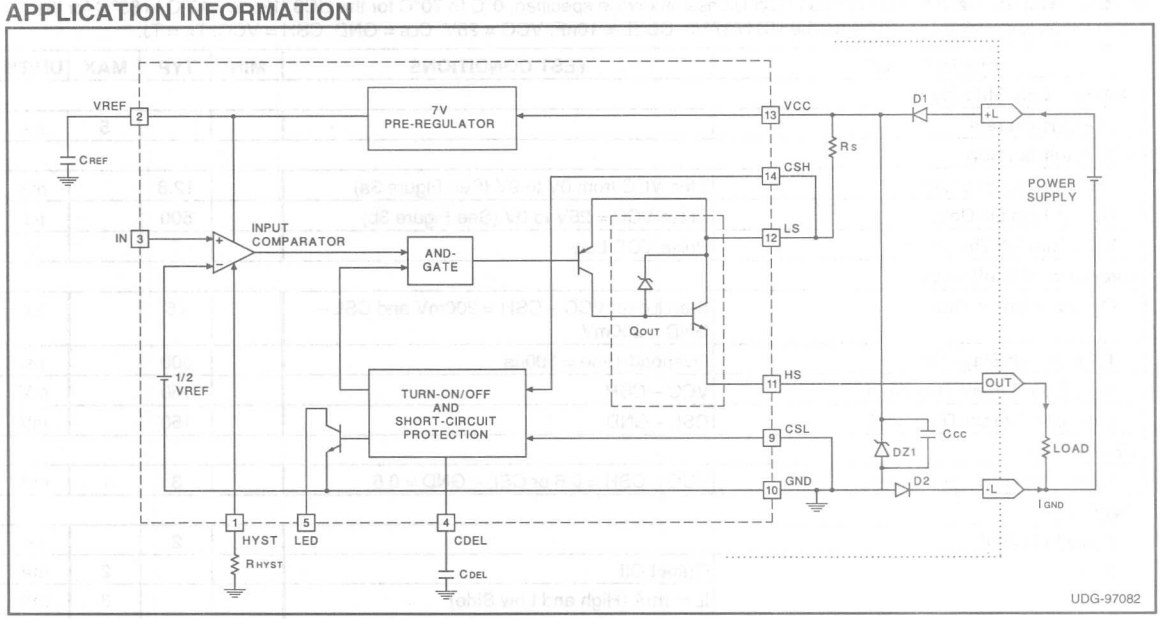


Figure 2a. High Side Application

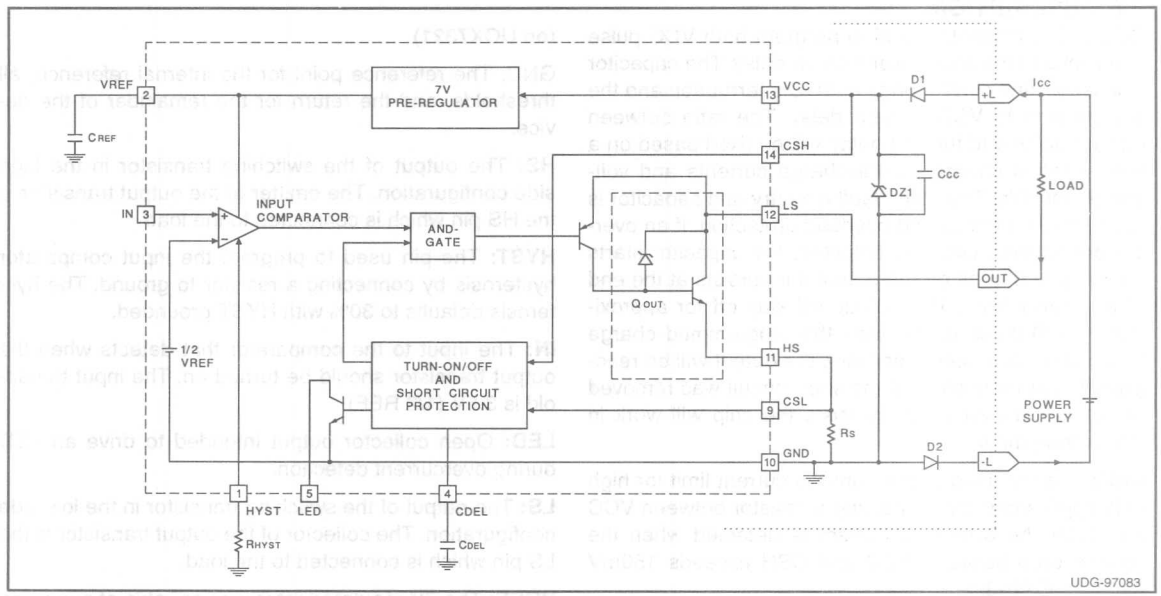


Figure 2b. Low Side Application

APPLICATION INFORMATION (cont.)

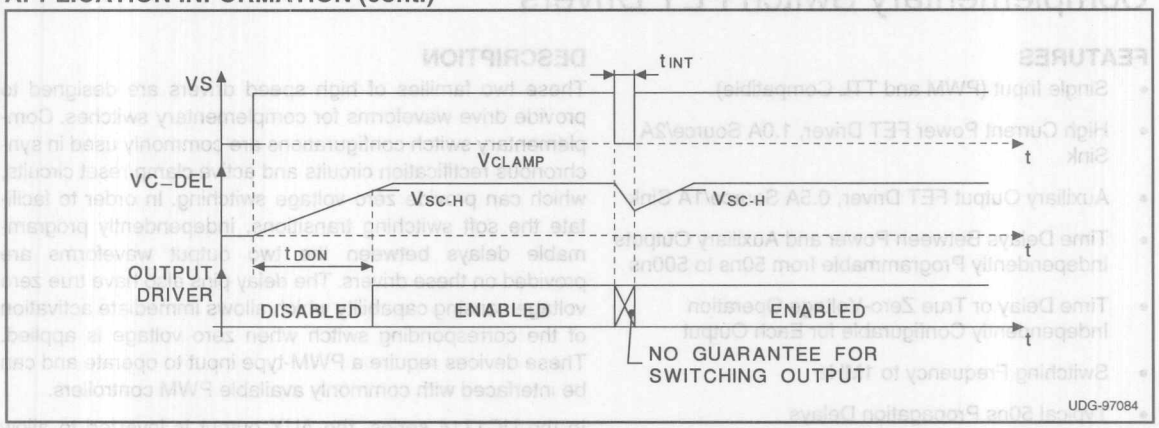


Figure 3a.

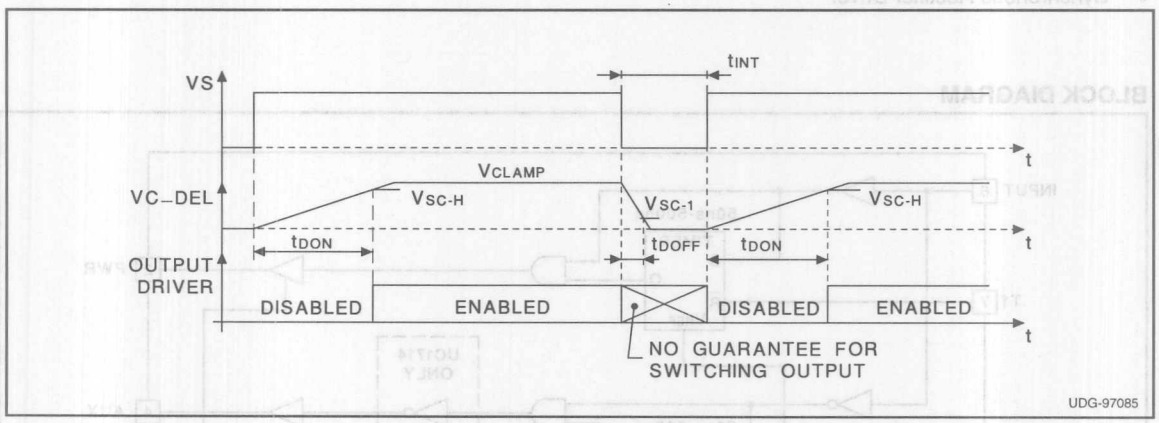


Figure 3b.

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Complementary Switch FET Drivers

FEATURES

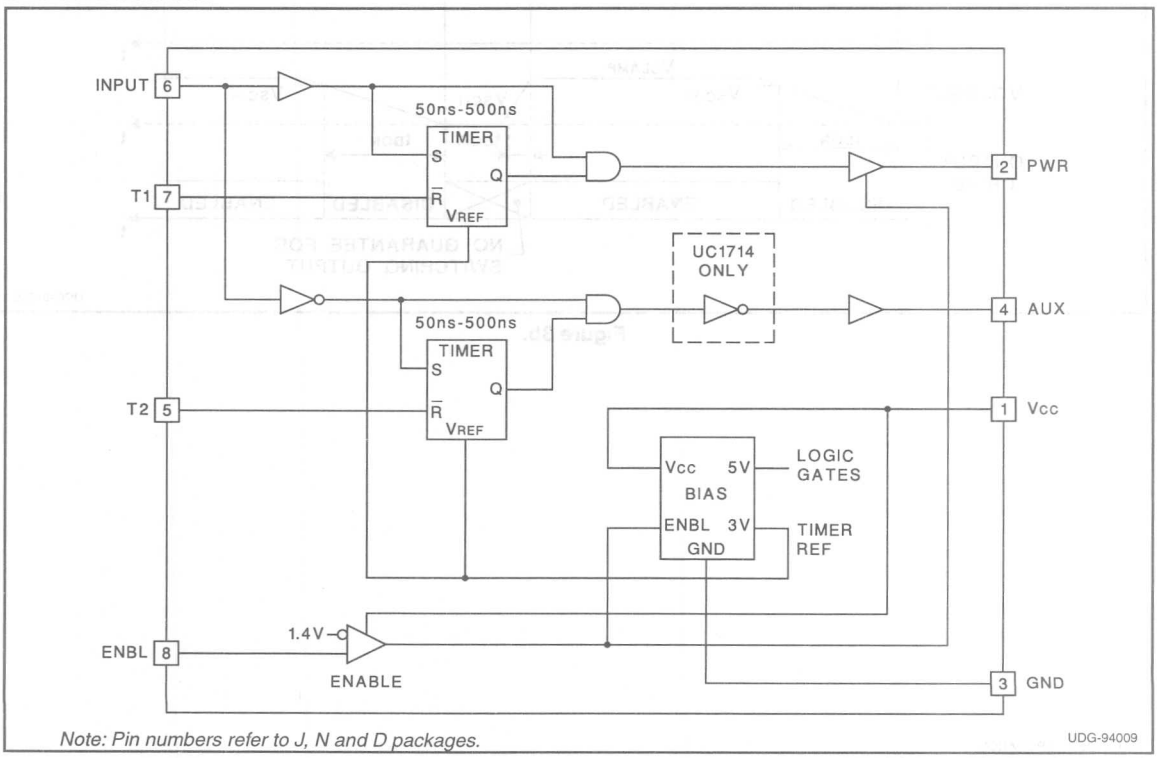
- Single Input (PWM and TTL Compatible)
- High Current Power FET Driver, 1.0A Source/2A Sink
- Auxiliary Output FET Driver, 0.5A Source/1A Sink
- Time Delays Between Power and Auxiliary Outputs Independently Programmable from 50ns to 500ns
- Time Delay or True Zero-Voltage Operation Independently Configurable for Each Output
- Switching Frequency to 1MHz
- Typical 50ns Propagation Delays
- ENBL Pin Activates 220µA Sleep Mode
- Power Output is Active Low in Sleep Mode
- Synchronous Rectifier Driver

DESCRIPTION

These two families of high speed drivers are designed to provide drive waveforms for complementary switches. Complementary switch configurations are commonly used in synchronous rectification circuits and active clamp/reset circuits, which can provide zero voltage switching. In order to facilitate the soft switching transitions, independently programmable delays between the two output waveforms are provided on these drivers. The delay pins also have true zero voltage sensing capability which allows immediate activation of the corresponding switch when zero voltage is applied. These devices require a PWM-type input to operate and can be interfaced with commonly available PWM controllers.

In the UC1714 series, the AUX output is inverted to allow driving a p-channel MOSFET. In the UC1715 series, the two outputs are configured in a true complementary fashion.

BLOCK DIAGRAM



Note: Pin numbers refer to J, N and D packages.

UDG-94009

9/96

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Vcc 20V
Power Driver IOH
  continuous ..... –200mA
  peak ..... –1A
Power Driver IOL
  continuous 400mA
  peak 2A
Auxiliary Driver IOH
  continuous ..... –100mA
  peak ..... –500mA
Auxiliary Driver IOL
  continuous 200mA
  peak 1A

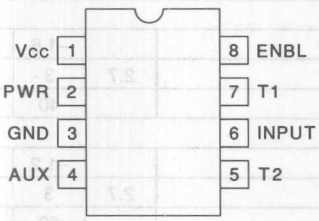
Input Voltage Range (INPUT, ENBL) ..... –0.3V to 20V
Storage Temperature Range. ..... –65°C to 150°C
Operating Junction Temperature (Note 1) ..... 150°C
Lead Temperature (Soldering 10 seconds) ..... 300°C

Note 1: Unless otherwise indicated, voltages are referenced to ground and currents are positive into, negative out of, the specified terminals.

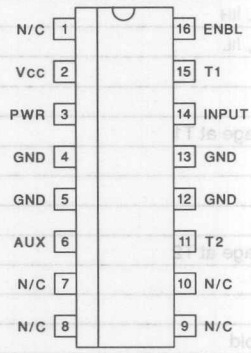
Note 2: Consult Packaging Section of databook for thermal limitations and specifications of packages.

CONNECTION DIAGRAMS

DIL-8, SOIC-8 (Top View)
J or N, D Packages



SOIC-16 (Top View)
DP Package



ELECTRICAL CHARACTERISTICS: Unless otherwise stated, V_{CC} = 15V, ENBL ≥ 2V, R_{T1} = 100kΩ from T1 to GND, R_{T2} = 100kΩ from T2 to GND, and –55°C < T_A < 125°C for the UC1714/5, –40°C < T_A < 85°C for the UC2714/5, and 0°C < T_A < 70°C for the UC3714/5, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Overall					
Vcc		7		20	V
Icc, nominal	ENBL = 2.0V		18	24	mA
Icc, sleep mode	ENBL = 0.8V		200	300	µA
Power Driver (PWR)					
Pre Turn-on PWR Output, Low	Vcc = 0V, Iout = 10mA, ENBL ≤ 0.8V		0.3	1.6	V
PWR Output Low, Sat. (VPWR)	INPUT = 0.8V, Iout = 40mA		0.3	0.8	V
	INPUT = 0.8V, Iout = 400mA		2.1	2.8	V
PWR Output High, Sat. (Vcc – VPWR)	INPUT = 2.0V, Iout = –20mA		2.1	3	V
	INPUT = 2.0V, Iout = –200mA		2.3	3	V
Rise Time	C_L = 2200pF		30	60	ns
Fall Time	C_L = 2200pF		25	60	ns
T1 Delay, AUX to PWR	INPUT rising edge, R_{T1} = 10kΩ (Note 4)	20	35	80	ns
T1 Delay, AUX to PWR	INPUT rising edge, R_{T1} = 100kΩ (Note 4)	350	500	700	ns
PWR Prop Delay	INPUT falling edge, 50% (Note 3)		35	100	ns
Auxiliary Driver (AUX)					
AUX Output Low, Sat (VAUX)	VIN = 2.0V, Iout = 20mA		0.3	0.8	V
	VIN = 2.0V, Iout = 200mA		1.8	2.6	V

ELECTRICAL CHARACTERISTICS (cont.): Unless otherwise stated, V_{CC} = 15V, ENBL ≥ 2V, R_{T1} = 100kΩ from T1 to GND, R_{T2} = 100kΩ from T2 to GND, and –55°C < T_A < 125°C for the UC1714/5, –40°C < T_A < 85°C for the UC2714/5, and 0°C < T_A < 70°C for the UC3714/5, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Auxiliary Driver (AUX) (cont.)					
AUX Output High, Sat (V_{CC} - V_{AUX})	V_{IN} = 0.8V, I_{OUT} = -10mA		2.1	3.0	V
	V_{IN} = 0.8V, I_{OUT} = -100mA		2.3	3.0	V
Rise Time	C_L = 1000pF		45	60	ns
Fall Time	C_L = 1000pF		30	60	ns
T2 Delay, PWR to AUX	INPUT falling edge, R_{T2} = 10kΩ (Note 4)	20	50	80	ns
T2 Delay, PWR to AUX	INPUT falling edge, R_{T2} = 100kΩ (Note 4)	250	350	550	ns
AUX Prop Delay	INPUT rising edge, 50% (Note 3)		35	80	ns
Enable (ENBL)					
Input Threshold		0.8	1.2	2.0	V
Input Current, I_{IH}	ENBL = 15V		1	10	µA
Input Current, I_{IL}	ENBL = 0V		–1	–10	µA
T1					
Current Limit	T1 = 0V		–1.6	–2	mA
Nominal Voltage at T1		2.7	3	3.3	V
ZVS Delay	T1 = 2.5V, (Note 5)		40	70	ns
T2					
Current Limit	T2 = 0V		–1.2	–2	mA
Nominal Voltage at T2		2.7	3	3.3	V
ZVS Delay	T2 = 2.5V, (Note 5)		50	100	ns
Input (INPUT)					
Input Threshold		0.8	1.4	2.0	V
Input Current, I_{IH}	INPUT = 15V		1	10	µA
Input Current, I_{IL}	INPUT = 0V		–5	–20	µA

Note 3: Propagation delay times are measured from the 50% point of the input signal to the 10% point of the output signal's transition with no load on outputs.

Note 4: T1 (T2) Delay is defined as the time between the 10% transition point of AUX (PWR) and the 10% transition point of PWR (AUX) with no capacitive load on either output.

Note 5: ZVS Delay is defined as : for the PWR output, the 10% transition point of its rising edge measured from the 50% point of the rising edge of INPUT and for the AUX, the 10% transition point of its rising edge on the UC1715 or the 90% transition point of its falling edge on the UC1714 measured from the 50% point of the falling edge of INPUT.

PIN DESCRIPTIONS

AUX: The AUX switches immediately at INPUT's rising edge but waits through the T2 delay after INPUT's falling edge before switching. AUX is capable of sourcing 0.5A and sinking 1.0A of drive current. See the Time Relationships diagram below for the difference between the UC1714 and UC1715 for INPUT, MAIN, and AUX. During sleep mode, AUX is inactive with a high impedance.

ENBL: The ENBL input switches at TTL logic levels (approximately 1.2V), and its input range is from 0V to 20V. The ENBL input will place the device into sleep mode when it is a logical low. The current into Vcc during the sleep mode is typically 220µA.

GND: This is the reference pin for all input voltages and the return point for all device currents. It carries the full peak sinking current from the outputs. Any tendency for the outputs to ring below GND voltage must be damped or clamped such that GND remains the most negative potential.

INPUT: The input switches at TTL logic levels (approximately 1.4V) but the allowable range is from 0 to 20V, allowing direct connection to most common IC PWM controller outputs. The rising edge immediately switches the AUX output, and initiates a timing delay, T1, before switching on the PWR output. Similarly, the INPUT falling edge immediately turns off the PWR output and initiates a timing delay, T2, before switching the AUX output.

It should be noted that if the input signal comes from a controller with FET drive capability, this signal provides

PIN DESCRIPTIONS (cont.)

another option. INPUT and PWR provide a delay only at the leading edge while INPUT and AUX provide the delay at the trailing edge.

PWR: The PWR output waits for the T1 delay after the INPUT's rising edge before switching on, but switches off immediately at INPUT's falling edge (neglecting propagation delays). This output is capable of sourcing 1A and sinking 2A of peak gate drive current. PWR output includes a passive, self-biased circuit which holds this pin active low, when ENBL ≤ 0.8V regardless of VCC's voltage.

T1: A resistor to ground programs the time delay between AUX switch turn-off and PWR turn-on.

T2: This pin functions in the same way as T1 but controls the time delay between PWR turn-off and activation of the AUX switch.

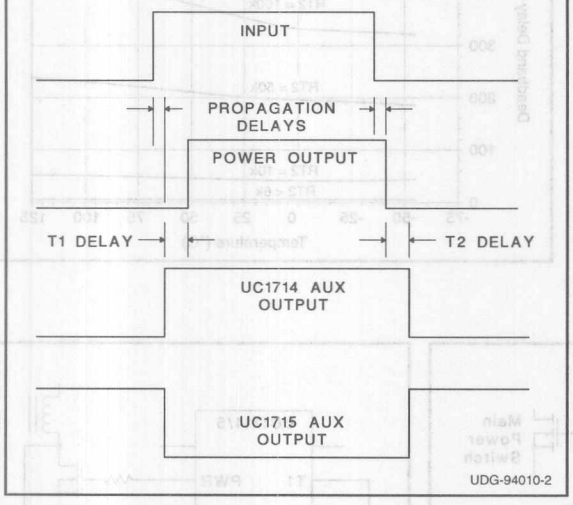
T1, T2: The resistor on each of these pins sets the charging current on internal timing capacitors to provide independent time control. The nominal voltage level at each pin is 3V and the current is internally limited to 1mA. The total delay from INPUT to each output includes a propagation delay in addition to the programmable timer but since the propagation delays are approximately equal, the relative time delay between the two outputs can be assumed to be solely a function of the programmed delays. The relationship of the time delay vs. RT is shown in the Typical Characteristics curves.

Either or both pins can alternatively be used for voltage sensing in lieu of delay programming. This is done by pulling the timer pins below their nominal voltage level which immediately activates the timer output.

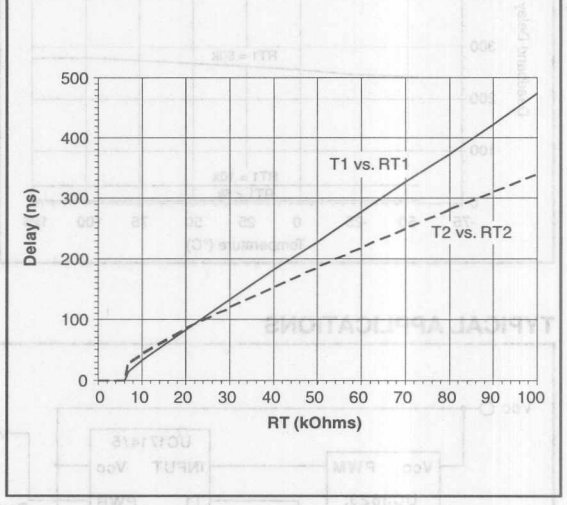
Vcc: The Vcc input range is from 7V to 20V. This pin should be bypassed with a capacitor to GND consistent with peak load current demands.

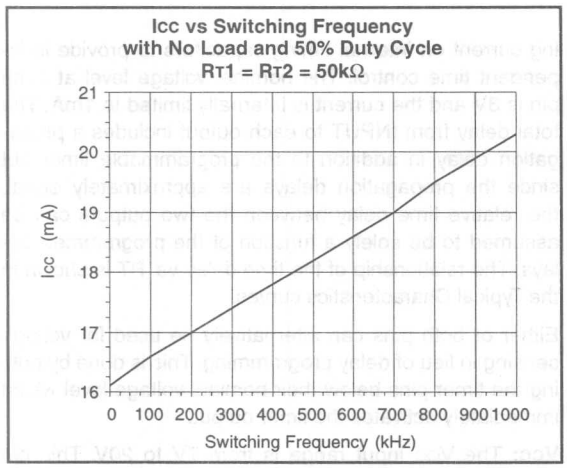
TYPICAL CHARACTERISTICS

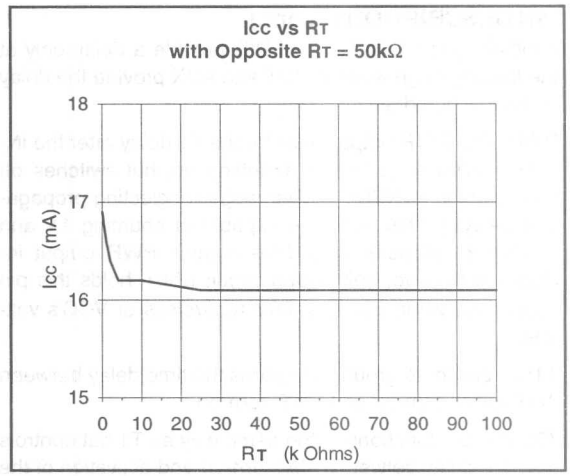
Time Relationships (Notes 3, 4)

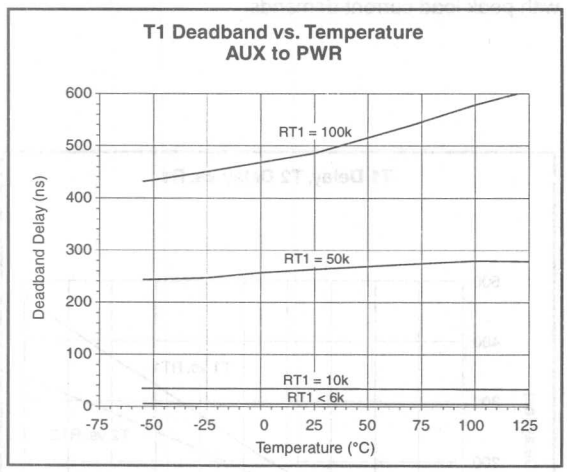


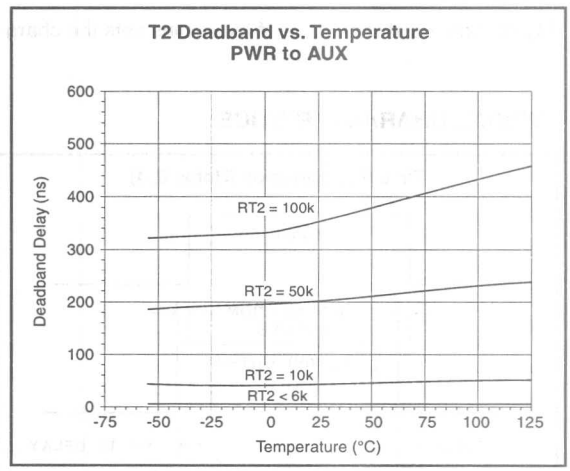
T1 Delay, T2 Delay vs. RT











TYPICAL APPLICATIONS

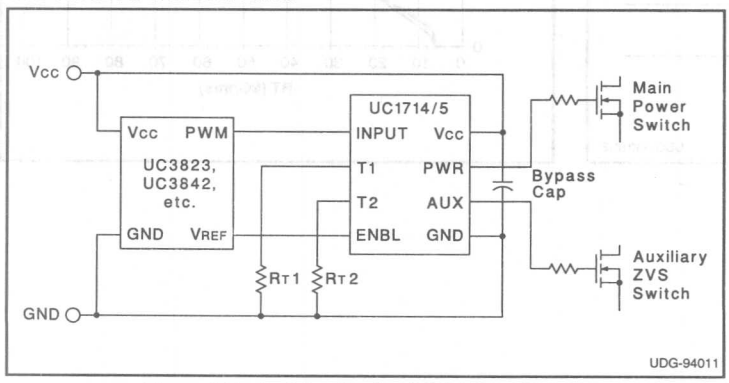


Figure 1. Typical Application With Timed Delays

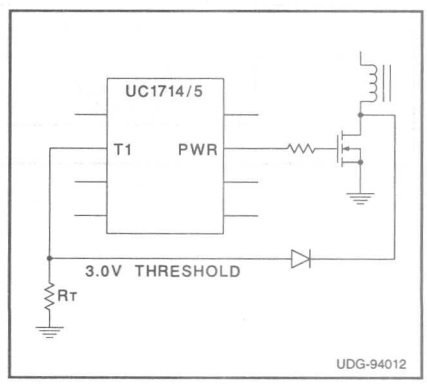


Figure 2. Using the Timer Input for Zero-Voltage Sensing

TYPICAL APPLICATIONS (cont.)

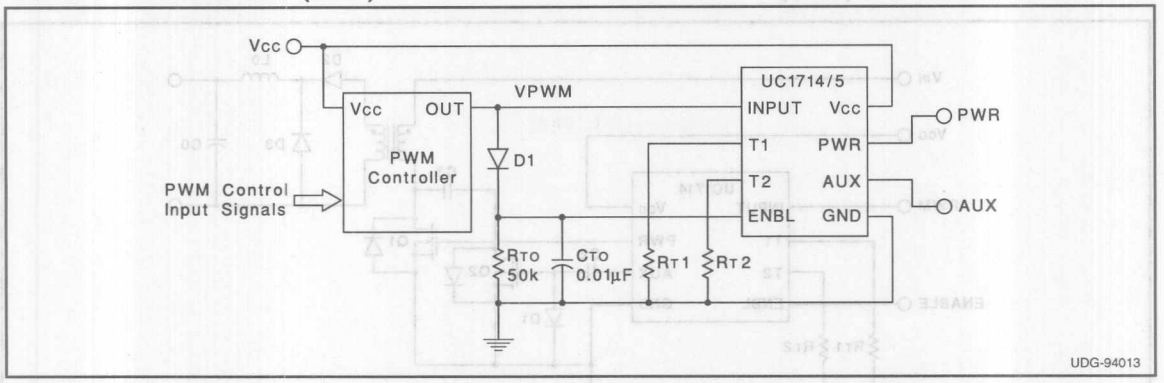


Figure 3. Self-actuated Sleep Mode with the Absence of an Input PWM Signal. Wake Up Occurs with the First Pulse while Turn-off is Determined by the RTO • CTO Time Constant

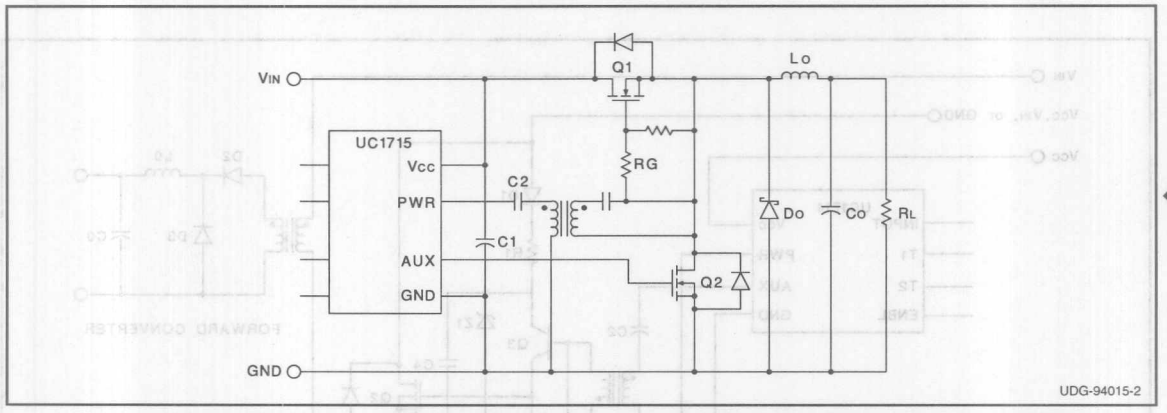


Figure 4. Using the UC1715 as a Complementary Synchronous Rectifier Switch Driver with N-Channel FETs

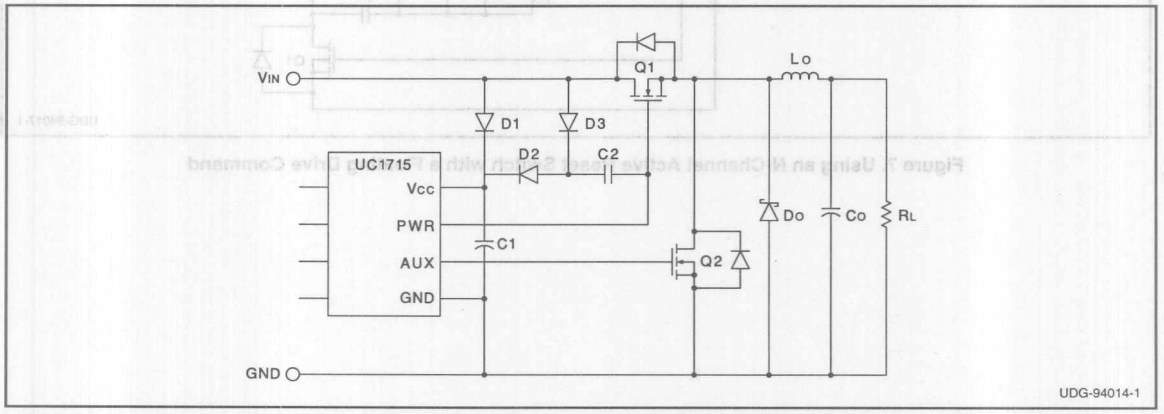


Figure 5. Synchronous Rectifier Application with a Charge Pump to Drive the High-Side N-Channel Buck Switch. VIN is Limited to 10V as Vcc will Rise to Approximately 2VIN.

TYPICAL APPLICATIONS (cont.)

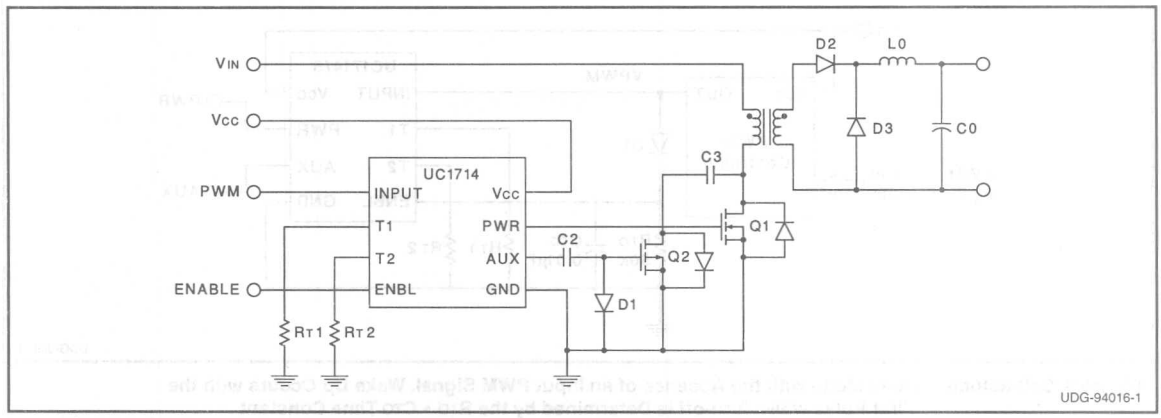


Figure 6. Typical Forward Converter Topology with Active Reset Provided by the UC1714 Driving an N-Channel Switch (Q1) and a P-Channel Auxilliary Switch (Q2)

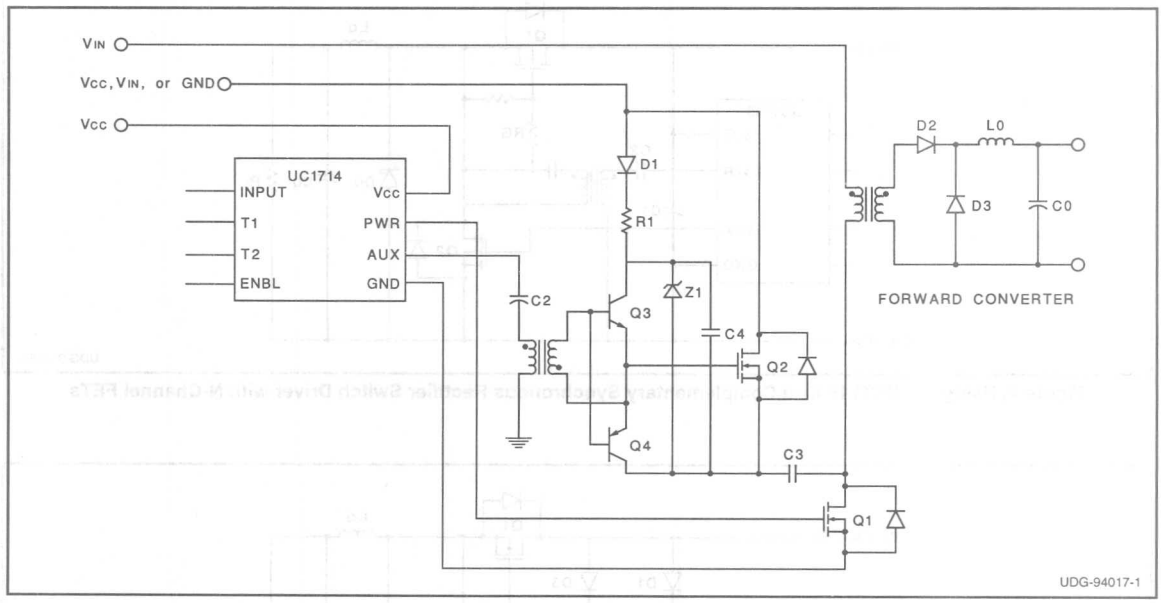


Figure 7. Using an N-Channel Active Reset Switch with a Floating Drive Command

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Isolated Drive Transmitter

FEATURES

- 500mA Output Drive, Source or Sink
- 8 to 35V Operation
- Transmits Logic Signal Instantly
- Programmable Operating Frequency
- Under-Voltage Lockout
- Able To Pass DC Information Across Transformer
- Up To 600kHz Operation

DESCRIPTION

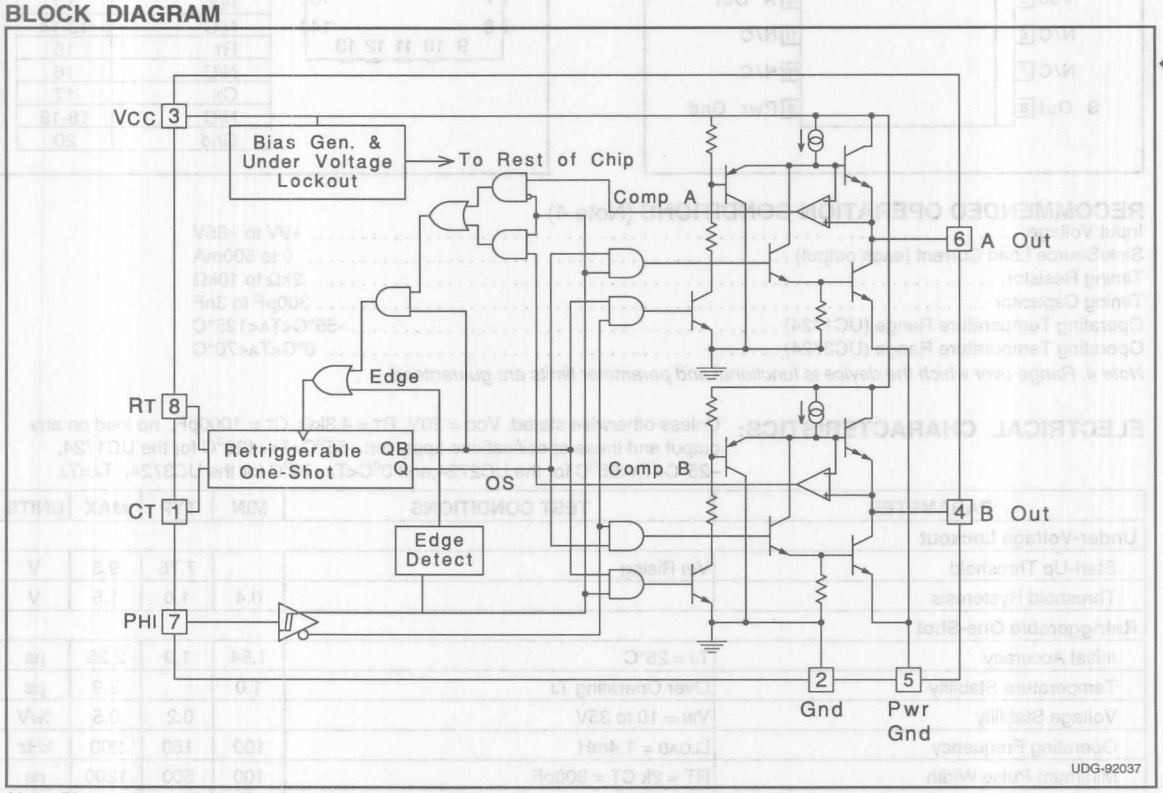
The UC1724 family of Isolated Drive Transmitters, along with the UC1725 Isolated Drivers, provide a unique solution to driving isolated power MOSFET gates. They are particularly suited to drive the high-side devices on a high-voltage H-bridge. The UC1724 devices transmit drive logic, and drive power, to the isolated gate circuit using a low cost pulse transformer.

This drive system utilizes a duty-cycle modulation technique that gives instantaneous response to the drive control transistions, and reliably passes steady-state, or DC, conditions. High frequency operation, up to 600kHz, allows the cost and size of the coupling transformer to be minimized.

These devices will operate over an 8 to 35 Volt supply range. The dual high current totem pole outputs are disabled by an uder-voltage lockout circuit to prevent spurious responses during startup or low voltage conditions.

These devices are available in 8-pin plastic or ceramic dual-inline packages, as well as surface mount packages.

BLOCK DIAGRAM



Note: Pin numbers refer to DIL-8 packages.

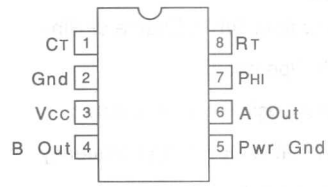
ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{IN} 40V
Source/Sink Current (Pulsed) 1A
Source/Sink Current (Continuous) 0.5A
Ouput Voltage (Pins 4, 6) . . . . . -0.3 to (V_{IN} +0.3)V
P_{HI}, R_T, and C_T inputs (Pins 1, 7, and 8) . . . . . -0.3 to 6V
Operating Junction Temperature (Note 2) . . . . . 150°C
Storage Temperature Range . . . . . -65°C to 150°C
Lead Temperature (Soldering, 10 Seconds) . . . . . 300°C

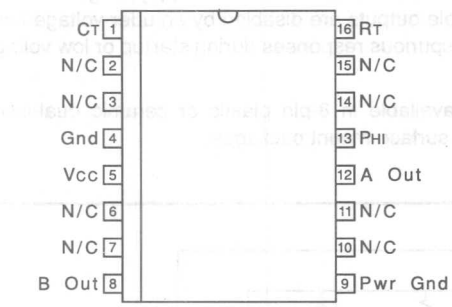
Note 1: All voltages are with respect to GND (Pin 2); all currents are positive into, negative out of part.
Note 2: Consult Unitrode Integrated Circuit Databook for thermal limitations and considerations of package.
Note 3: Pin numbers refer to DIL-8 packages.

CONNECTION DIAGRAMS

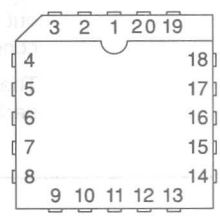
DIL-8 (Top View)
J Or N Package



SOIC-16 (Top View)
DW Package



PLCC-20 (Top View)
Q Package



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
Vcc	2
N/C	3-4
B Out	5
N/C	6
Pwr Gnd	7
N/C	8-9
A Out	10
N/C	11
PHI	12
N/C	13-14
RT	15
N/C	16
CT	17
N/C	18-19
Gnd	20

RECOMMENDED OPERATION CONDITIONS (Note 4)

Input Voltage . . . . . +9V to +35V
Sink/Source Load Current (each output) . . . . . 0 to 500mA
Timing Resistor . . . . . 2kΩ to 10kΩ
Timing Capacitor . . . . . 300pF to 3nF
Operating Temperature Range (UC1724) . . . . . -55°C<T_A<125°C
Operating Temperature Range (UC3724) . . . . . 0°C<T_A<70°C

Note 4: Range over which the device is functional and parameter limits are guaranteed.

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, V_{CC} = 20V, R_T = 4.3kΩ, C_T = 1000pF, no load on any output and these specifications apply for: –55°C<T_A<125°C for the UC1724, –25°C<T_A<85°C for the UC2724,and 0°C<T_A<70°C for the UC3724. T_A=T_J.

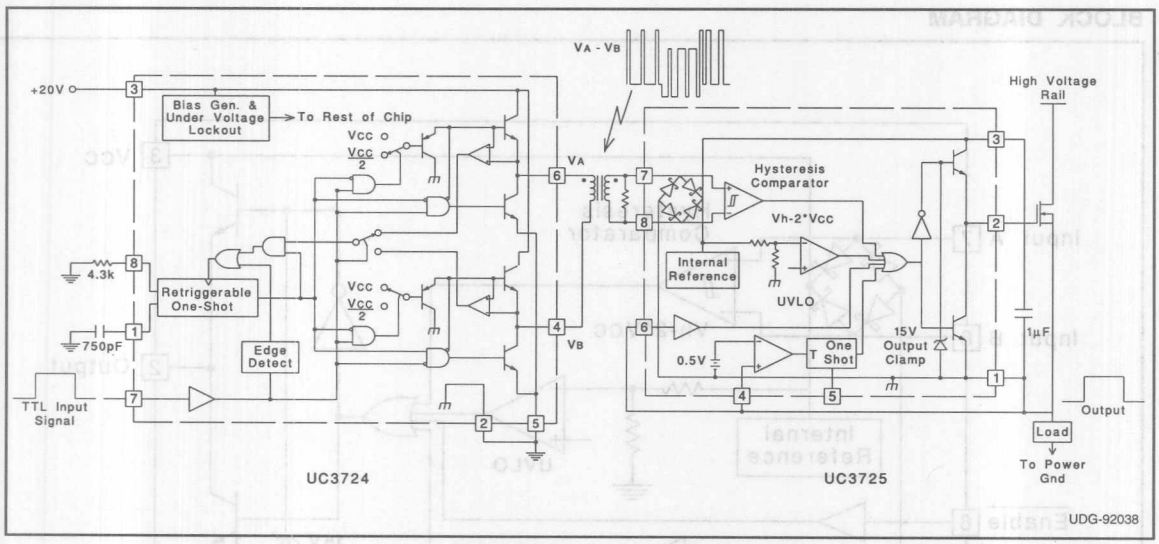
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Under-Voltage Lockout					
Start-Up Threshold	V_{IN} Rising		7.75	9.5	V
Threshold Hysteresis		0.4	1.0	1.5	V
Retriggerable One-Shot					
Initial Accuracy	T_J = 25°C	1.54	1.9	2.25	µs
Temperature Stability	Over Operating T_J	1.0		2.9	µs
Voltage Stability	V_{IN} = 10 to 35V		0.2	0.5	%/V
Operating Frequency	L_{LOAD} = 1.4mH	100	150	200	kHz
Minimum Pulse Width	RT = 2k CT = 300pF	100	500	1200	ns
Operating Frequency	RT = 2k C_T = 300pF L_{LOAD} = 1.4mH	500	750	1100	kHz

ELECTRICAL CHARACTERISTICS (cont.)

Unless otherwise stated, V_{CC} = 20V, R_T = 4.3kΩ, C_T = 1000pF, no load on any output and these specifications apply for: –55°C<T_A<125°C for the UC1724, –25°C<T_A<85°C for the UC2724,and 0°C<T_A<70°C for the UC3724. T_A=T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Phi Input (Control Input)					
HIGH Input Voltage		2.0			V
LOW Input Voltage				0.8	V
HIGH Input Current	V_{IH} = +2.4V	-220	-130		mA
LOW Input Current	V_{IL} = +0.4V	-600	-300		µA
Delay to One-Shot				350	ns
Delay to Output				250	ns
Output Drivers					
Output Low Level	I_{SINK} = 50mA		0.3	0.4	V
	I_{SINK} = 250mA		0.5	2.1	V
Output High Level (Volts Below V_{CC})	I_{SOURCE} = 50 mA		1.5	2.1	V
	I_{SOURCE} = 250 mA		1.7	2.5	V
Rise/Fall Time	No load		30	90	ns
Total Supply Current					
Supply Current	C_T = 1.4V		15	30	mA

Typical Application



UNITRODE CORPORATION
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TEL. (603) 424-2410 • FAX (603) 424-3460

UNITRODE

UC1725
UC2725
UC3725

Isolated High Side FET Driver

FEATURES

- Receives Both Power and Signal Across the Isolation Boundary
- 9 to 15 Volt High Level Gate Drive
- Under-voltage Lockout
- Programmable Over-current Shutdown and Restart
- Output Enable Function

DESCRIPTION

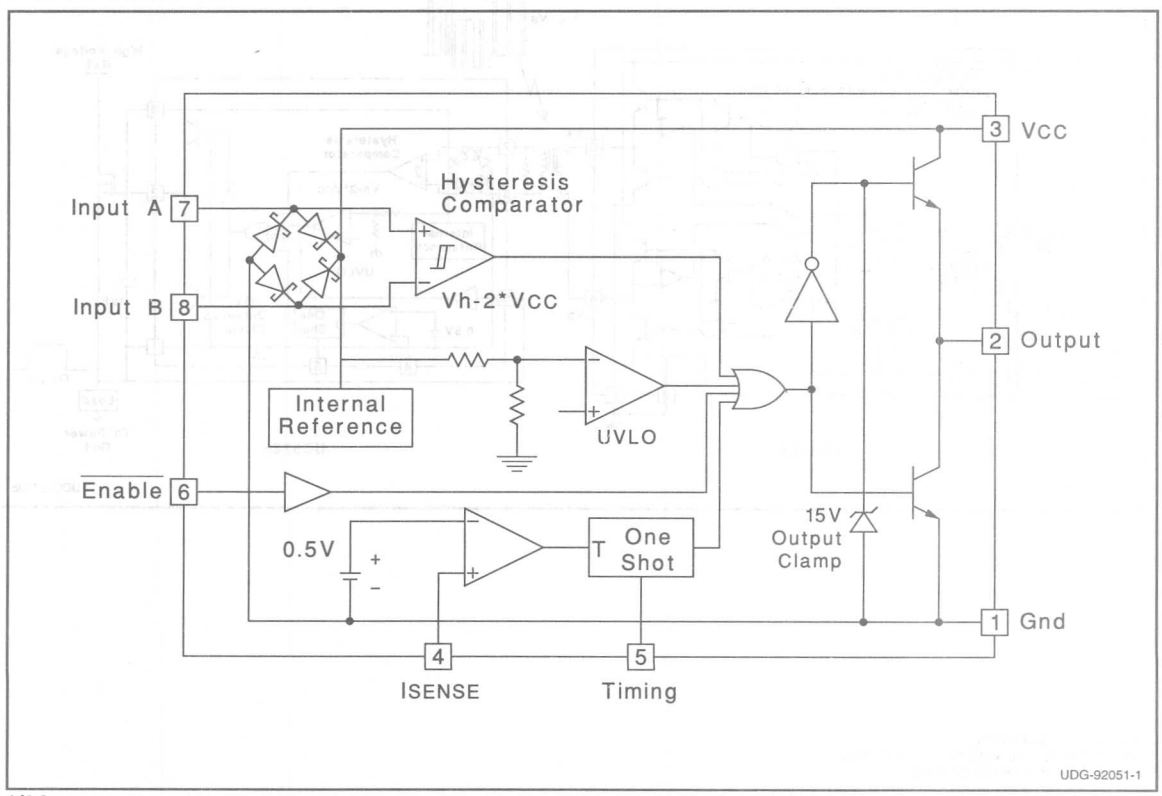
The UC1725 and its companion chip, the UC1724, provide all the necessary features to drive an isolated MOSFET transistor from a TTL input signal. A unique modulation scheme is used to transmit both power and signals across an isolation boundary with a minimum of external components.

Protection circuitry, including under-voltage lockout, over-current shutdown, and gate voltage clamping provide fault protection for the MOSFET. High level gate drive is guaranteed to be greater than 9 volts and less than 15 volts under all conditions.

Uses include isolated off-line full bridge and half bridge drives for driving motors, switches, and any other load requiring full electrical isolation.

The UC1725 is characterized for operation over the full military temperature range of -55°C to +125°C while the UC2725 and UC3725 are characterized for -25°C to +85°C and 0°C to +70°C respectively.

BLOCK DIAGRAM



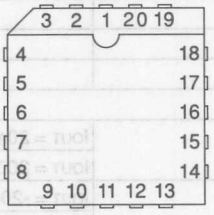
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (pin 3) 30V
Power inputs (pins 7 & 8) 30V
Output current, source or sink (pin 2)
DC. 0.5A
Pulse (0.5 us) 2.0A
Enable and Current limit inputs (pins 4 & 6). . . . . -0.3 to 6V
Power Dissipation at $T_A \leq 25°C$ (DIL-8) 1W
Power Dissipation at $T_A \leq 25°C$ (SO-14) 725mW
Lead Temperature (Soldering, 10 Seconds) . . . . . 300°C

Note 1: Unless otherwise indicated, voltages are referenced to ground and currents are positive into, negative out of, the specified terminals (pin numbers refer to DIL-8 package).
Note 2: See Unitrode Integrated Circuits databook for information regarding thermal specifications and limitations of packages.

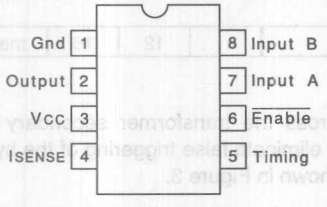
CONNECTION DIAGRAMS

PLCC-20 (Top View)
Q Package

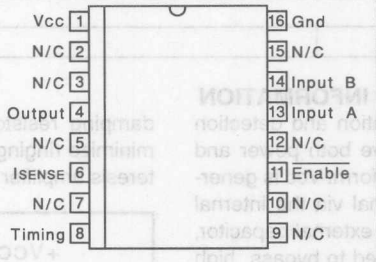


PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
ISENSE	2
N/C	3-5
Timing	6
$\overline{\text{Enable}}$	7
N/C	8-9
Input A	11
N/C	12-14
Input B	15
Gnd	16
Vcc	17
N/C	18-19
Output	20

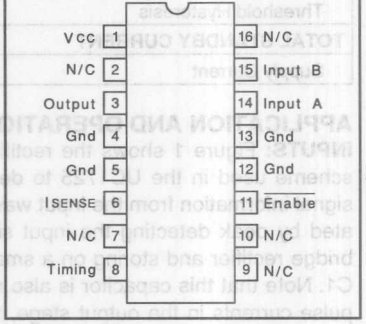
DIL-8 (Top View)
J Or N Package



SOIC-16 (Top View)
DW Package



DIL-16 (Top View)
JE Or NE Package



ELECTRICAL CHARACTERISTICS:

(Unless otherwise stated, these specifications apply for $-55°C \leq T_A \leq +125°C$ for UC1725; $-25°C \leq T_A \leq +85°C$ for UC2725; $0°C \leq T_A \leq +70°C$ for UC3725; V_{CC} (pin 3) = 0 to 15V, R_T=10k, C_T=2.2nf, $T_A = T_J$, pin numbers refer to DIL-8 package.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
POWER INPUT SECTION (PINS 7 & 8)					
Forward Diode Drop, Schottky Rectifier	I_F = 50ma		.55	.7	V
	I_F = 500ma		1.1	1.5	V
CURRENT LIMIT SECTION (PIN 4)					
Input bias current	V_{PIN4} = OV		-1	-10	µA
Threshold voltage		0.4	0.5	0.6	V
Delay to outputs	V_{PIN4} = 0 to 1V		100	250	ns
TIMING SECTION (PIN 5)					
Output Off Time		27	30	33	µs
Upper Mono Threshold		6.3	7.0	7.7	V
Lower Mono Threshold		1.9	2.0	2.3	V
HYSTERESIS AMPLIFIER (PINS 7 & 8)					
Input Open Circuit Voltage	Inputs (pins 7 & 8), Open Circuited, T_A= 25°C	7.0	Vcc/2	8.0	V
Input Impedance	T_A = 25°C	23	28	33	kΩ
Hysteresis		26.5	2•Vcc	30.5	V
Delay to Outputs	$V_{PIN7} - V_{PIN8} = V_{CC} + 1V$		100	300	ns

ELECTRICAL CHARACTERISTICS (cont.)

(Unless otherwise stated, these specifications apply for -55°C≤TA≤+125°C for UC1725; -25°C≤TA≤+85°C for UC2725; 0°C≤TA≤+70°C for UC3725; VCC (pin 3) = 0 to 15V, Rt=10k, CT=2.2nf, TA =TJ, pin numbers refer to DIL-8 package.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ENABLE SECTION (PIN 6)					
High Level Input Voltage		2.1	1.4		V
Low Level Input Voltage			1.4	.8	V
Input Bias Current			-250	-500	µA
OUTPUT SECTION					
Output Low Level	IOUT = 20mA		0.35	0.5	V
	IOUT = 200mA		0.6	2.5	V
Output High Level	IOUT = -20mA	13	13.5		V
	IOUT = -200mA	12	13.4		V
	VCC = 30V, Iout = -20mA		14	15	V
Rise/Fall Time	CT = 1nf		30	60	ns
UNDER VOLTAGE LOCKOUT					
UVLO Low Saturation	20mA, VCC = 8V		0.8	1.5	V
Start-up Threshold		11.2	12	12.6	V
Threshold Hysteresis		.75	1.0	1.12	V
TOTAL STANDBY CURRENT					
Supply Current			12	16	ma

APPLICATION AND OPERATION INFORMATION

INPUTS: Figure 1 shows the rectification and detection scheme used in the UC1725 to derive both power and signal information from the input waveform. Vcc is generated by peak detecting the input signal via the internal bridge rectifier and storing on a small external capacitor, C1. Note that this capacitor is also used to bypass high pulse currents in the output stage, and therefore should be placed direclty between pins 1 and 3 using minimal lead lengths.

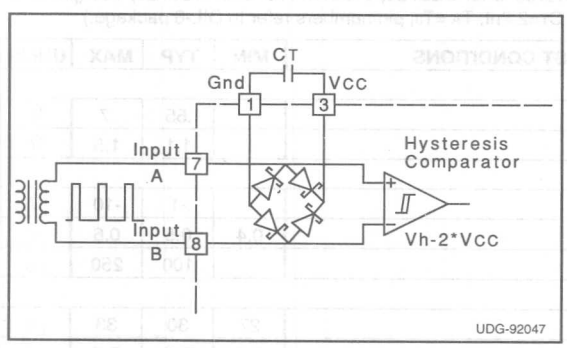


FIGURE 1 - Input Stage

Signal detection is performed by the internal hysteresis comparator which senses the polarity of the input signal as shown in Figure 2. This is accomplished by setting (re-setting) the comparator only if the input signal exceeds Vcc (-Vcc). In some cases it may be necessary to add a damping resistor across the transformer secondary to minimize ringing and eliminate false triggering of the hysteresis amplifier as shown in Figure 3.

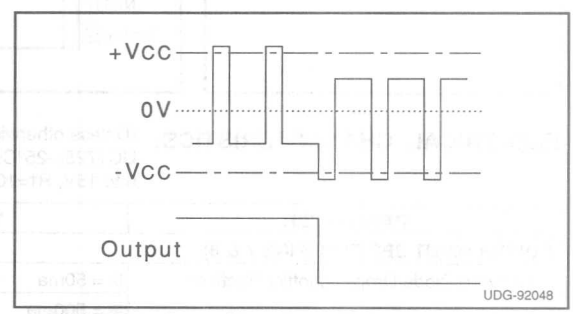


FIGURE 2 - Input Waveform (DIL-8 Pin 7 - Pin 8)

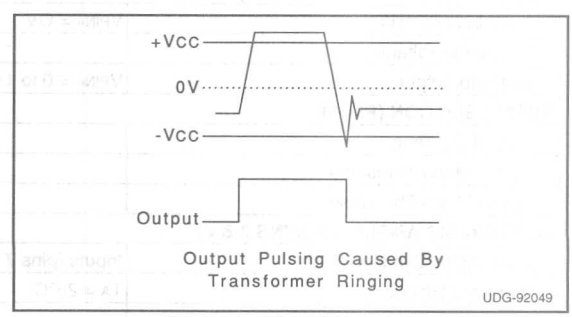


FIGURE 3 - Signal Detection

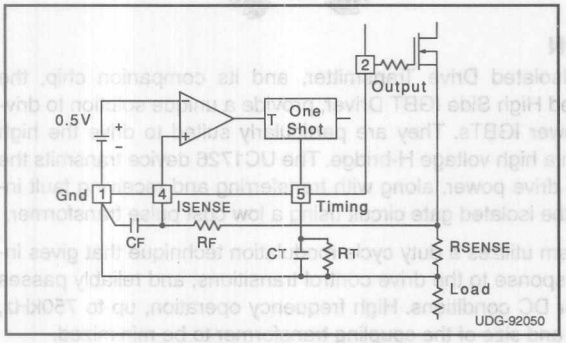


FIGURE 4 - Current Limit

CURRENT LIMIT AND TIMING: Current sensing and shutdown can be implemented directly at the output using the scheme shown in Figure 4. Alternatively, a current transformer can be used in place of RSENSE. A small RC filter in series with the input (pin 4) is generally needed to eliminate the leading edge current spike caused by parasitic circuit capacitances being charged during turn on. Due to the speed of the current sense circuit, it is very important to ground CF directly to Gnd as shown to eliminate false triggering of the one shot caused by ground drops.

One shot timing is easily programmed using an external capacitor and resistor as shown in Figure 4. This, in turn, controls the output off time according to the formula:

$$T_{OFF} = 1.28 \bullet RC.$$

If current limit feature is not required, simply ground pin 4 and leave pin 5 open.

OUTPUT: Gate drive to the power FET is provided by a totem pole output stage capable of sourcing and sinking currents in excess of 1 amp. The undervoltage lockout circuit guarantees that the high level output will never be less than 9 volts. In addition, during undervoltage lockout, the output stage will actively sink current to eliminate the need for an external gate to source resistor. High level output is also clamped to 15 volts. Under high capacitive loading however, the output may overshoot 2 to 3 volts, due to the drivers' inabitlity to switch from full to zero output current instantaneously. In a practical circuit this is not normally a concern. A few ohms of series gate resistance is normally required to prevent parasitic oscillations, and will also eliminate overshoot at the gate.

ENABLE: An enable pin is provided as a fast, digital input that can be used in a number of applications to directly switch the output. Figure 6 shows a simple means of providing a fast, high voltage translation by using a small signal, high voltage transistor in a cascode configuration. Note that the UC1725 is still used to provide power, drive and protection circuitry for the power FET.

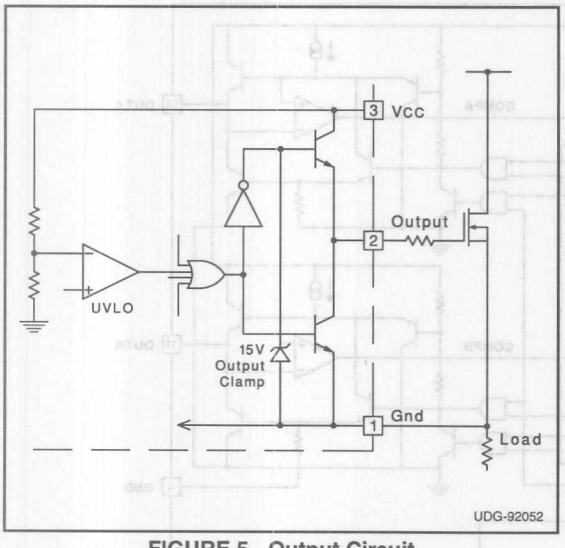


FIGURE 5 - Output Circuit

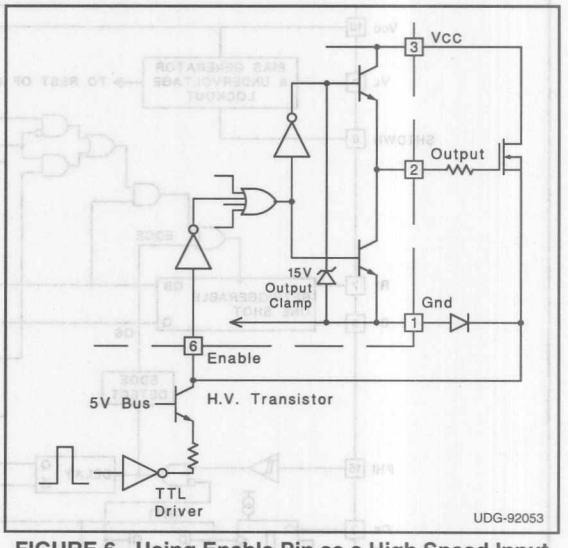


FIGURE 6 - Using Enable Pin as a High Speed Input Path

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Isolated Drive Transmitter

FEATURES

- 750mA Output Drive, Source or Sink
- 8 to 35V Operation
- Transmits Drive Logic and Power through Low Cost Transformer
- Programmable Operating Frequency
- Up to 750kHz Operation
- Improved Output Control Algorithm Minimizes Output Jitter
- Fault Logic Monitors Isolated High Side IGBT Driver UC1727 for Faults
- User Programmable Fault Timing Screens False Fault Signals
- Shutdown Mode Disables On Chip Logic Reference for Low Standby Power
- Optional External Biasing of Logic Circuitry can Reduce Overall Power Dissipation

DESCRIPTION

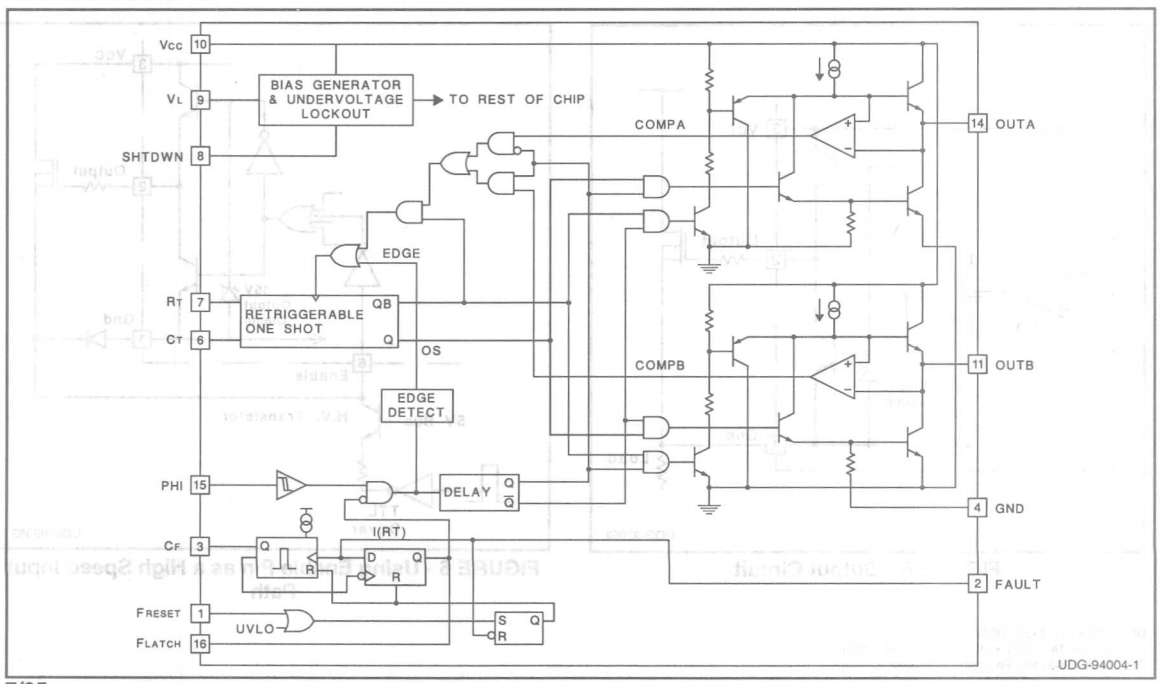
The UC1726 Isolated Drive Transmitter, and its companion chip, the UC1727 Isolated High Side IGBT Driver, provide a unique solution to driving isolated power IGBTs. They are particularly suited to drive the high side devices on a high voltage H-bridge. The UC1726 device transmits the drive logic and drive power, along with transferring and receiving fault information with the isolated gate circuit using a low cost pulse transformer.

This drive system utilizes a duty cycle modulation technique that gives instantaneous response to the drive control transitions, and reliably passes steady state, or DC conditions. High frequency operation, up to 750kHz, allows the cost and size of the coupling transformer to be minimized.

The UC1726 can be powered from a single V_{CC} supply which internally generates a voltage reference for the logic circuitry. It can also be placed into a low power shutdown mode that disables the internal reference. The IC's logic circuitry can be powered from an external supply, V_L, to minimize overall power dissipation. Fault logic monitors the Isolated High Side IGBT Driver UC1727 for faults. Based on user defined timing, the UC1726 distinguishes valid faults, which it responds to by setting the fault latch pin. This also disables the gate drive information until the fault reset pin is toggled to a logic one.

The UC1726 operates over an 8 to 35 volt supply range. The typical V_{CC} voltage will be greater than 28 volts to be compatible with the UC1727. The undervoltage lockout circuitry of the Isolated High Side IGBT Driver UC1727 locks out the drive information during its undervoltage lockout.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply Voltage Vcc 40V
Source/Sink Current (Pulsed) 1.5A
Source/Sink Current (Continuous) 1.0A
Output Voltage (pins 12, 14) ..... –0.3 to (Vcc + 0.3)V
CF, FRESET, FAULT, SHTDWN,
FLATCH, VL, PHI, RT ..... –0.3 to 6.0V
CT ..... 1.0 to 6.0V
Operating Junction Temperature (Note 2) ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 seconds) ..... 300°C

Note 1: All voltages are with respect to GND (Pin 2); all currents are positive into, negative out of part.

RECOMMENDED OPERATING CONDITIONS (Note 3)

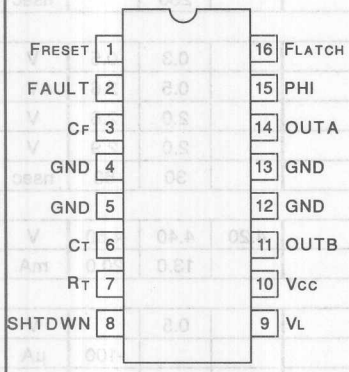
Input Voltage ..... +9 to +35.0V
Sink/Source Current (each output) ..... 0 to 750mA
Timing Resistor ..... 2.4k to 200kΩ
Timing Capacitor (CT) ..... 75pF to 2.0nF
Timing Capacitor (CF) ..... 75pF to 3.0nF

Note 2: See Unitrode Integrated Circuits databook for information regarding thermal specifications and limitations of packages.

Note 3: Range over which the device is functional and parameter limits are guaranteed.

CONNECTION DIAGRAMS

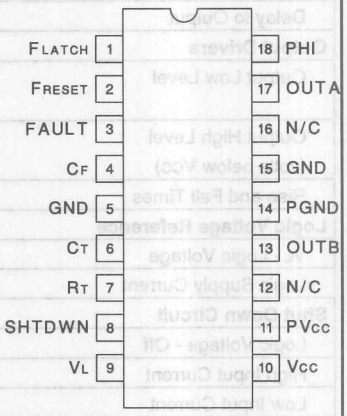
DIL-16 (Top View)
N Package



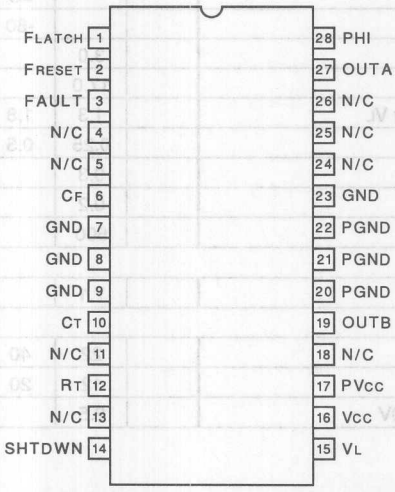
DIL-16 (Top View)
SP Package



DIL-18 (Top View)
J Package



SOIC-28 (Top View)
DWP Package



PLCC-28 (Top View)
QP Package



PACKAGE PIN FUNCTION	
FUNCTION	PIN
GND	1
CT	2
N/C	3-4
RT	5
SHTDWN	6
VL	7
VCC	8
N/C	9
PVCC	10
OUTB	11
PGND	12-18
GND	19
OUTA	20
PHI	21
FLATCH	22
FRESET	23
FAULT	24
N/C	25
CF	26
N/C	27
N/C	28

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, V_{CC} = 20V, R_T = 4.32kΩ, C_T = 330pF and C_F = 2.2nF, no load on any output, and –55°C < T_A < 125°C for the UC1726, –40°C < T_A < 85°C for the UC2726, and 0°C < T_A < 70°C for the UC3726, T_A = T_J.

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Retriggerable one shot					
Initial Accuracy	T_J = 25°C	1.400	1.600	1.800	µsec
Temperature Stability	Over operating T_J	1.000		2.200	µsec
Voltage Stability	V_{CC} = 10 to 35V		0.2		%/V
Operating Frequency	L_{LOAD} = 1.5mH		170		kHz
PHI Input (Control Input)					
HIGH Input Voltage		2.0			V
LOW Input Voltage				0.8	V
HIGH Input Current			10		µA
LOW Input Current			-300	–600	µA
Delay to one shot			100	250	nsec
Delay to Output	C_T = 1.4V		250		nsec
Output Drivers					
Output Low Level	I_{SINK} = 20mA		0.3	0.5	V
	I_{SINK} = 400mA		0.5	2.6	V
Output High Level	I_{SOURCE} = –20mA		2.0	2.6	V
(volts below V_{CC})	I_{SOURCE} = –400mA		2.0	2.9	V
Rise and Fall Times	No load		30	60	nsec
Logic Voltage Reference					
V_L - Logic Voltage	Internal Voltage	4.20	4.40	4.60	V
Logic Supply Current	V_L = 4.75V to 5.25V, C_T = 1.4V		13.0	20.0	mA
Shut Down Circuit					
Logic Voltage - Off			0.5		V
High Input Current	V_{IH} = 2.4			-100	µA
Low Input Current	V_{IL} = 0.4			-20	µA
Fault Logic					
Fault Reset High Input Current	V_{IH} = 2.4			±5	µA
Fault Reset Low Input Current	V_{IL} = 0.4			-10	µA
Fault High Input Current	V_{IH} = 2.4			±5	µA
Fault Low Input Current	V_{IL} = 0.4			-60	µA
Fault Pulse Width	C_F = 330pF		3.0		µs
	C_F = 2.2nF		17.0		µs
Fault Latch, V_{OH}	I_{LOAD} = –1mA, Volts below V_L		1.3	1.8	V
Fault Latch, V_{OL}	I_{LOAD} = 1mA		0.25	0.5	V
Fault Latch, V_{OH}	I_{LOAD} = 0, Volts below V_L		0.3		V
Fault Latch, V_{OL}	I_{LOAD} = 0		0.2		V
Fault Reset Pulse Width			500		ns
UVLO					
Turn On Threshold			7.1		V
Total Supply Current					
Supply Current	C_T = 1.4V		22	40	mA
	C_T = 1.4V, V_L = 5.0V		12	20	mA
	C_T = 1.4V, Shutdown = 5.0V		2.5		mA

Refer to Typical Application on Page 5 and Application Note U-143C "New Chip Pair Provides Isolated Drive for High Voltage IGBTs"

PIN DESCRIPTIONS

CF: The timing input to the fault logic. A capacitor is placed across the input of CF and ground. The timing window is approximately t = 2.1CFRT.

CT: The connection to the timing capacitor that controls the operating frequency. A capacitor to ground is repetitively charged during the one shot pulse width. It is discharged when a comparator senses zero current in the primary side of the transformer. The one shot pulse width is consequently determined by the time it takes to charge the capacitor from a threshold voltage of VL/4 to VL/2. This pin must be tied to a capacitor. See Recommended Operating Conditions.

FAULT: This input to the fault logic initiates the user programmable timer. This time interval, specified by the capacitor on CF, determines the validity of the fault. The pin is tied to a low cost optocoupler, and is high until the UC1727 sends drive information from the PHI pin through the transformer while the FAULT pin stays low. Once this pin goes high, it must stay high during the entire fault window to be accepted as a valid fault. A valid fault sets the FLATCH pin high and prevents the transmitting of gate drive information until the FRESET is toggled high. If fault logic is not used, the FAULT pin must be grounded.

FLATCH: A valid fault sets this pin to a logic one and prevents the transmitting of gate drive information. The FLATCH pin can only be reset by connecting the FRESET to a logic 0.

FRESET: The input to the fault logic that resets the fault logic latch (FLATCH) and enables drive transmit data. This input must be low when powered up and stay low until after the fault latch has been set.

GND: The signal and power ground for the device. The power ground of the output transistor is isolated on the chip from the substrate ground which biases the remainder of the device.

OUTA: One output of the two totem pole outputs connected across the transformer primary winding. When PHI is high, the output toggles between 0.3V during the one shot charge time and approximately VCC + 0.4V during the remainder of the period. When PHI is low the output toggles between VCC - 2V during the one shot charge time and approximately 0.6VCC during the remainder of the period.

OUTB: One output of the two totem pole outputs connected across the transformer primary winding. When PHI is high, the output toggles between VCC - 2V during the one shot charge time and approximately 0.6VCC during the remainder of the period. When PHI is low the output toggles between 0.3V during the one shot charge time and approximately VCC + 0.4V during the remainder of the period.

PGND: This is the ground for the output transistors bonded in the 28 pin packages. On the sixteen pin packages it is bonded separately to the GND pin.

PHI: A logic control input to the isolated gate drive that changes the outputs as described above. This changes the duty cycle of the voltage wave form applied across the transformer. The Isolated High Side IGBT Driver UC1727 senses the different duty cycles as different drive commands.

PVCC: This is the input voltage for the output transistors on the 28 pin package. On the sixteen pin packages it is bonded separately to the VCC pin.

RT: The input that sets the CT and CF capacitor currents with a resistor to ground. The voltage on RT is approximately 0.3VL. The resulting charge currents are: ICT = ICF = VL / 4RT.

SHTDWN: This input shuts down the internal reference. A TTL logic one puts the UC1726 into a low standby current mode. This input has a pull down resistor on the chip to guarantee proper operation when left open. If an external logic voltage is applied to VL, this shutdown feature cannot be used without bringing the external voltage source to zero volts.

VCC: The input voltage that biases the outputs and the internal reference. It can vary between 8V to 35V. This supply pin will typically be greater than 28V to be compatible with the UC1727. In order to minimize power dissipation use an external logic supply, VCC approximately 15V, and a step up transformer (N = 2).

VL: The logic supply pin that biases all circuits except for the totem pole outputs. A bypass capacitor is recommended on this pin when left unconnected. The internal reference is approximately 4.4V. A 5.0V supply can be applied to this pin to assure minimum power dissipation. When an external supply higher than the VL voltage is applied to this pin, the internal reference turns off.

OPERATING FREQUENCY:

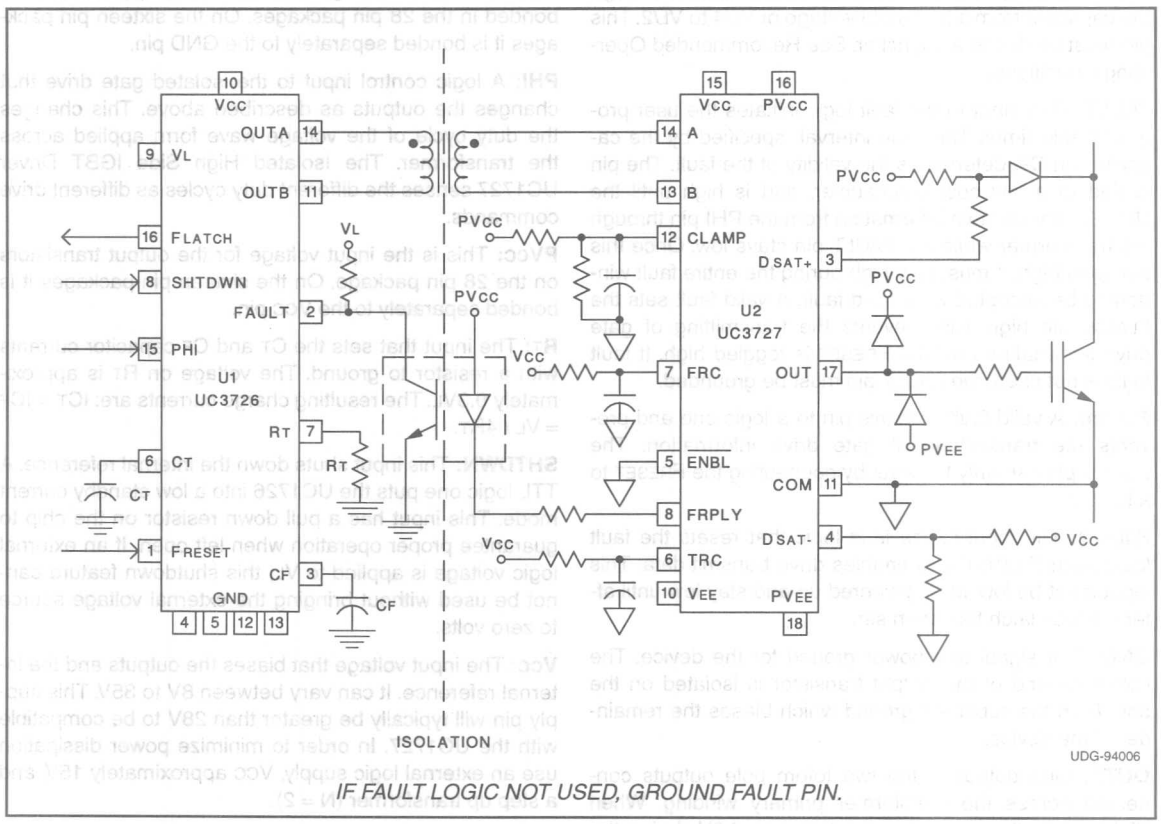
The chip operating frequency is determined by the values of components connected to the RT and CT pins. A resistor connected between RT and ground sets the charge current to ICT = VL / 4RT. The operating frequency varies slightly depending on the VCC and VL voltages. The following equations approximate the one shot pulse width at operating frequency when VCC = 20V.

$$T_{PW} = 1.1R_T(C_T + 50pF)$$

$$Fo = \frac{1}{3.3R_T(C_T + 50pF)}$$

The 50pF additional capacity represents internal chip capacitance at the CT input.

TYPICAL APPLICATION



IF FAULT LOGIC NOT USED, GROUND FAULT PIN.

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

Isolated High Side IGBT Driver

FEATURES

- Receives Power and Signal from Single Isolation Transformer
- Generates Split Rail for 4A Peak Bipolar Gate Drive
- 16V High Level Gate Drive
- Low Level Gate Drive more Negative than -5V
- Undervoltage Lockout
- Desaturation Detection and Fault Processing
- Separate Output Enable Input
- Programmable Stepped Gate Drive for Soft Turn On
- Programmable Stepped Gate Drive for Soft Fault

DESCRIPTION

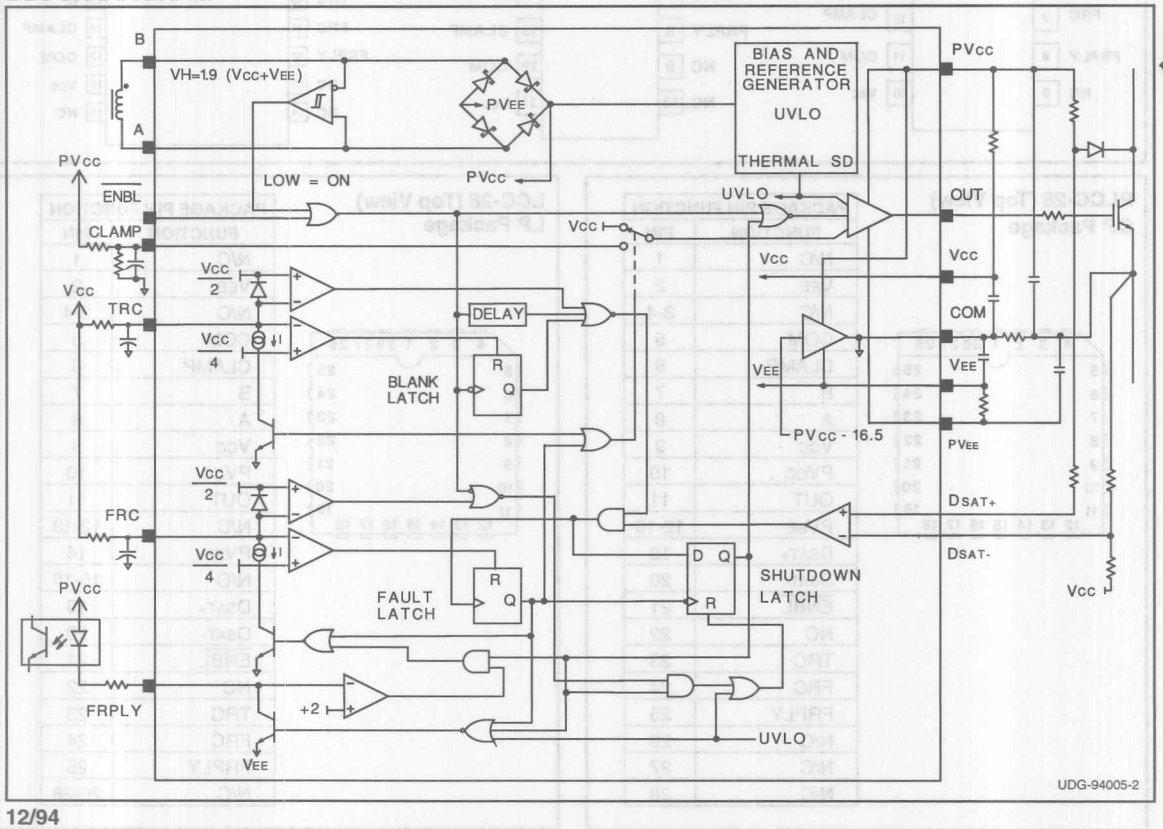
The UC1727 and its companion chip, the UC1726, provide all the necessary features to drive an isolated IGBT transistor from a TTL input signal. A unique modulation scheme is used to transmit both power and signal across an isolation boundary with a minimum of external components.

Protection features include under voltage lockout and desaturation detection. High level gate drive signals are typically 16V. Intermediate high drive levels can be programmed for various periods of time to limit surge current at turn on and in the event of desaturation due to a short circuit.

The chip generates a bipolar supply so that the gate can be driven to a negative voltage insuring the IGBT remains off in the presence of high common mode slew rates.

Uses include isolated off-line full bridge and half bridge drives for motors, switches, and any other load requiring full electrical isolation.

BLOCK DIAGRAM



12/94

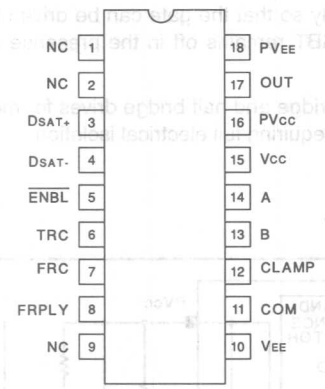
ABSOLUTE MAXIMUM RATINGS

Supply voltage (V_{CC} - V_{EE}) 40V
Power Inputs (IA - BI) 45V
Analog Input Voltage ($\overline{ENBL}$, CLAMP) ..... -0.3 To Vcc+0.3
Analog Input Voltage (D_{SAT+}, D_{SAT-}) ..... V_{EE}-0.3 to V_{CC}+0.3
Analog Input Current (D_{SAT+}, D_{SAT-}) ..... -10 to 10mA
Output Current, |(OUT)|
DC 0.8A
Pulse (0.5µs) 4A
FRPLY Output Current 30mA

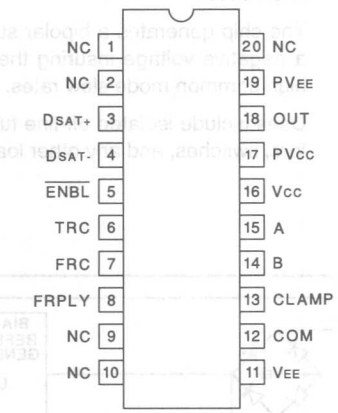
Note: All voltages are with respect to COM. Currents are positive into the specified terminal.

CONNECTION DIAGRAMS

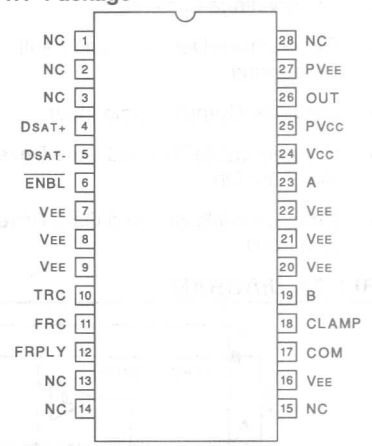
DIL-18 (Top View)
J Package



DIL-20 (Top View)
N Package



SOIC-28 (Top View)
DWP Package

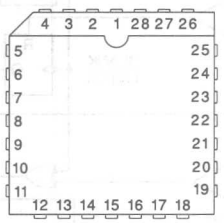


PLCC-28 (Top View)
QP Package



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
V_{EE}	2
N/C	3-4
COM	5
CLAMP	6
B	7
A	8
V_{CC}	9
PV_{CC}	10
OUT	11
PV_{EE}	12-18
D_{SAT+}	19
D_{SAT-}	20
$\overline{ENBL}$	21
NC	22
TRC	23
FRC	24
FRPLY	25
N/C	26
N/C	27
N/C	28

LCC-28 (Top View)
LP Package



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
V_{EE}	2
N/C	3-4
COM	5
CLAMP	6
B	7
A	8
V_{CC}	9
PV_{CC}	10
OUT	11
N/C	12-13
PV_{EE}	14
N/C	15-18
D_{SAT+}	19
D_{SAT-}	20
$\overline{ENBL}$	21
NC	22
TRC	23
FRC	24
FRPLY	25
N/C	26-28

See Application Note U-143A "New Chip Pair Provides Isolated Drive for High Voltage IGBTs"

PIN DESCRIPTIONS

A, B: Signal and power input pins. Connect these pins to the secondary of the transformer driven by UC1726.

CLAMP: Analog programming pin for intermediate drive level to be used at turn on or in response to a desaturation event. Requires a bypass capacitor to COM.

COM: Self generated common for bipolar supply. This pin will be 16.5V below PVCC.

DSAT+, DSAT-: Inputs to the desaturation comparator. Desaturation is detected when DSAT+ is greater than DSAT-.

$\overline{\text{ENBL}}$: Negative true enable input. Tie to VCC to disable the chip. Connect to COM to enable the chip. If the $\overline{\text{ENBL}}$ pin is used as the primary input to the chip, connect B to VCC and A to VEE.

FRC: Fault Resistor and Capacitor. Programs the duration that OUT will be held at CLAMP potential during a desaturation event before it is driven fully low. Also sets the period of time that OUT will be held low before allowing it to be driven high again.

FRPLY: Fault Reply pin. Open collector output. Normally connected to VEE. When desaturation is detected, the pin opens.

OUT: Gate drive output. Connect to gate of IGBT with a series damping resistor greater than 3 ohms.

TRC: Timing Resistor and Capacitor. Programs the duration that OUT will be held at CLAMP potential and the period of time the desaturation comparator will be ignored during the rising edge.

VCC: Positive supply voltage. Bypass to COM with a low ESL/ESR 1µF capacitor.

VEE: Negative supply voltage. Bypass to COM with a low ESL/ESR 1µF capacitor.

PVEE: Output driver negative supply. Connect to VEE with a 3.3 ohm resistor and bypass to COM with a low ESL/ESR 1µF capacitor.

PVCC: Output driver positive supply. Connect to VCC with a 3.3 ohm resistor and bypass to COM with a low ESL/ESR 1µF capacitor.

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = –55°C to 125°C for the UC1727, T_A = –40°C to 85°C for the UC2727, T_A = 0°C to 70°C for the UC3727, R(TRC) = 54.9k, C(TRC) = 180pF, R(FRC) = 309K, C(FRC) = 200pF, VCC - VEE = 25V, CLAMP = 9V, T_A = T_J, and all voltages are measured with respect to COM.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Power Input Receivers					
Forward Diode Drop	I_F = 50mA		0.5	0.65	V
	I_F = 500mA		1.2	2	V
VCC Regulator					
VCC	25 ≤ (VCC - VEE) ≤ 36V, |I(COM)| ≤ 15mA	15.5	16.5	17.5	V
Hysteresis Comparator					
Input Open Circuit Voltage	(Measured with respect to VEE)		12		V
Input Impedance			100		kΩ
Hysteresis		44	47	50	V
Enable Input					
High Level Input Voltage		12			V
Low Level Input Voltage				5	V
Input Bias Current	$\overline{\text{ENBL}}$ = COM		–460	–900	µA
Output Driver					
Saturation to VCC	I(OUT) = -20mA		1.7	2.3	V
Saturation to VCC	I(OUT) = -500mA		2	2.5	V
Saturation to VEE	I(OUT) = 20mA		2	3	V
Saturation to VEE	I(OUT) = 500mA		2.4	3.6	V

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = –55°C to 125°C for the UC1727, T_A = –40°C to 85°C for the UC2727, T_A = 0°C to 70°C for the UC3727, R(TRC) = 54.9k, C(TRC) = 180pF, R(FRC) = 309K, C(FRC) = 200pF, V_{CC} - V_{EE} = 25V, CLAMP = 9V, T_A = T_J, and all voltages are measured with respect to COM.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Driver (cont.)					
Turn on Clamp Voltage	I(OUT) = -100mA	7	9	11	V
Fault Clamp Voltage	II(OUT)I = 100mA	8	10	12.5	V
UVLO Saturation to V_{EE}	I(OUT) = 20mA,V_{CC} no connection		2	3	V
Rise and Fall Times	CI = 1n, CLAMP = V_{CC}, R_{OUT} = 3Ω (Note 1)		75	150	ns
Turn On Sequence Timer					
Clamped Driver Time	(Note 1)	0.4	1	1.7	µs
Blanking Time	(Note 1)	3	5	7	µs
Fault Manager					
Clamped Driver Time	(Note 1)	0.4	1	1.7	µs
Fault Lock Off Time	(Note 1)	15	25	35	µs
FRPLY Saturation	I(FRPLY) = 10mA		1.8	3	V
FRPLY Leakage	FRPLY = V_{CC}		0	10	µA
Desaturation Detection Comparator					
Input Offset Voltage (Iviol)	V_{CM} = V_{EE}+2, V_{CM} = V_{CC}-2		0	20	mV
Input Bias Current			–1.5	10	µA
Delay to Output	C(FRC) = 0 (Note 1)		150		ns
Undervoltage Lock Out					
V_{CC} Threshold		14	15.5	17	V
V_{CC} Hysteresis			0.35		V
V_{EE} Threshold		–4.5	–5.5	–6.5	V
V_{EE} Hysteresis		0.5	1	1.5	V
Thermal Shutdown					
Threshold	Not tested		175		°C
Hysteresis	Not tested		45		°C
Total Standby Current					
I(V_{CC})			24	30	mA

Note 1: Guaranteed by design, but not 100% tested in production.

APPLICATION INFORMATION

Figure 1 shows the rectification and detection scheme used in the UC1727 to derive both power and signal information from the input waveform. V_{CC}-V_{EE} is generated by peak detecting the input signal via the internal bridge rectifier and storing it on external capacitors. COM is generated by an internal amplifier that maintains PVcc-COM = 16.5V.

Signal detection is performed by the internal hysteresis comparator which senses the polarity of the input signal as shown in Figure 2. This is accomplished by setting (or resetting) the comparator only if the input signal exceeds 0.95 | V_{CC}-V_{EE} |. In some cases it may be necessary to add a damping resistor across the transformer secondary to minimize ringing and eliminate false triggering of the hysteresis comparator as shown in Figure 3.

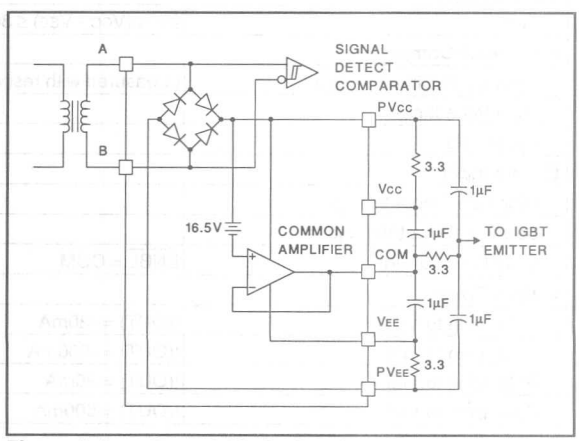


Figure 1. Input Stage & Bipolar Supply

APPLICATION INFORMATION (cont.)

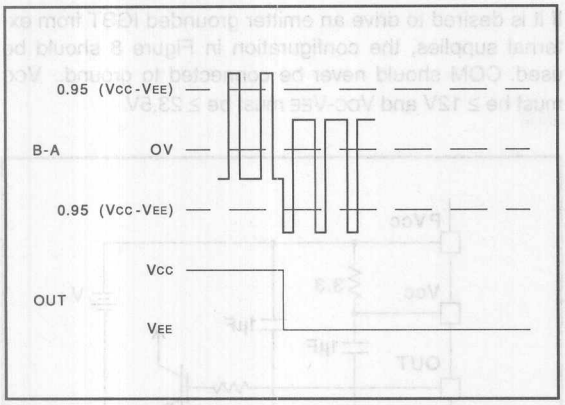


Figure 2. Input Waveform

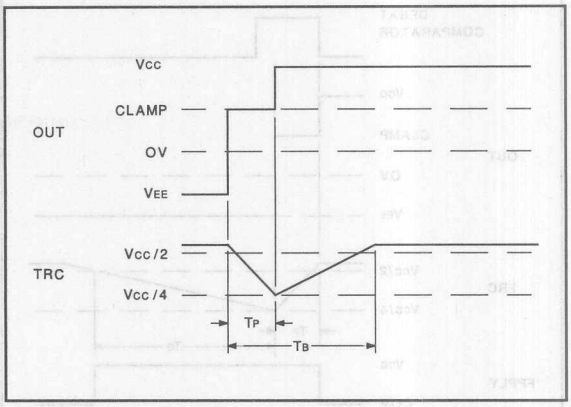


Figure 4. Rising Edge Waveform

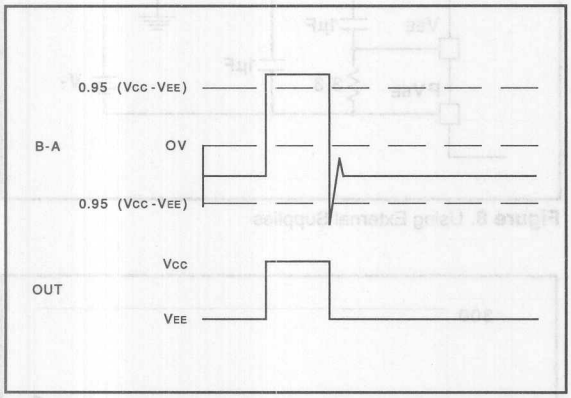


Figure 3. Output Pulsing Caused By Transformer Ringing

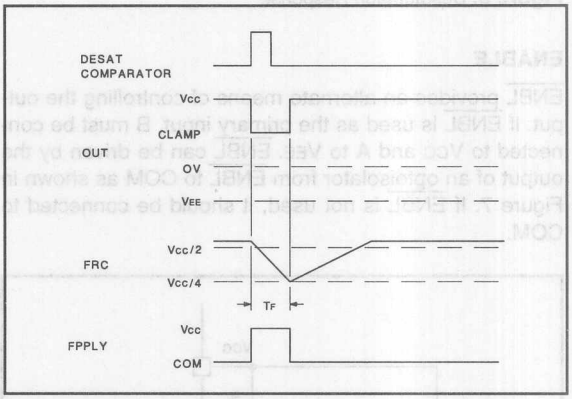


Figure 5. Transient Desaturation Response

GATE DRIVE WAVEFORM

The rising edge of OUT can be programmed for a two step sequence as shown in Figure 4. The plateau voltage is programmed by a resistive divider from Vcc to COM applied at CLAMP. CLAMP must be bypassed to COM. The plateau voltage is approximately OUT = CLAMP. The plateau time is set by a resistor from TRC to Vcc and a capacitor to COM as:

$$Tp = RC \ln\left(\frac{R-7.6k}{R-12.4k}\right).$$

TRC also programs a blanking time during which the chip ignores the desaturation comparator. The blanking time is:

$$Tb = Tp + 0.4RC.$$

In the event that desaturation is detected outside the blanking interval, OUT will be driven back to the CLAMP plateau for a fault time set by a resistor from FRC to Vcc and a capacitor to COM as:

$$Tf = RC \ln\left(\frac{R-7.6k}{R-12.4k}\right).$$

If the event is transient, OUT will return high at the end of Tf as shown in Figure 5. During Tf, FRPLY is open. After Tf, FRPLY is connected to COM.

Desaturation shown in Figure 6 that persists longer than Tf will cause OUT to be driven low. The chip will not accept a command to drive OUT high for a delay period of

$$Td = 0.4RC$$

FRPLY will be open during this entire period.

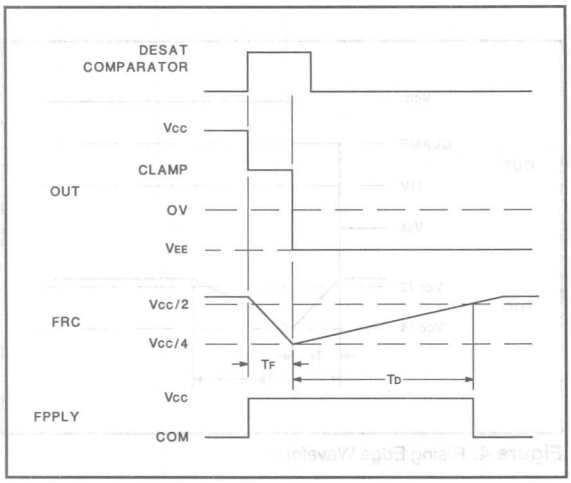


Figure 6. Desaturation Response

ENABLE

$\overline{\text{ENBL}}$ provides an alternate means of controlling the output. If $\overline{\text{ENBL}}$ is used as the primary input, B must be connected to Vcc and A to VEE. $\overline{\text{ENBL}}$ can be driven by the output of an optoisolator from $\overline{\text{ENBL}}$ to COM as shown in Figure 7. If $\overline{\text{ENBL}}$ is not used, it should be connected to COM.

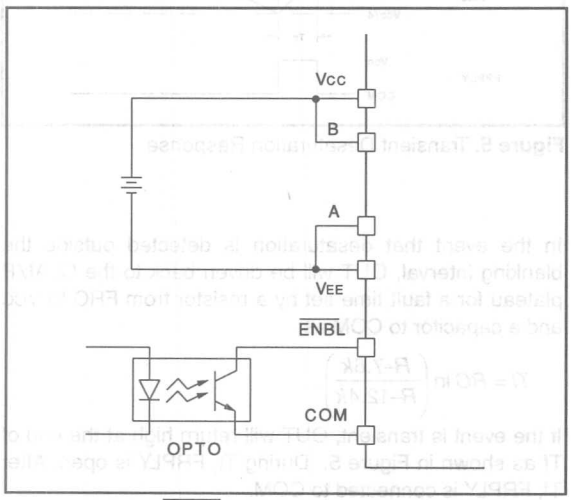


Figure 7. Using $\overline{\text{ENBL}}$ as Primary Input

EXTERNAL BIPOLAR SUPPLIES

If it is desired to drive an emitter grounded IGBT from external supplies, the configuration in Figure 8 should be used. COM should never be connected to ground. Vcc must be ≥ 12V and Vcc-VEE must be ≥ 23.5V.

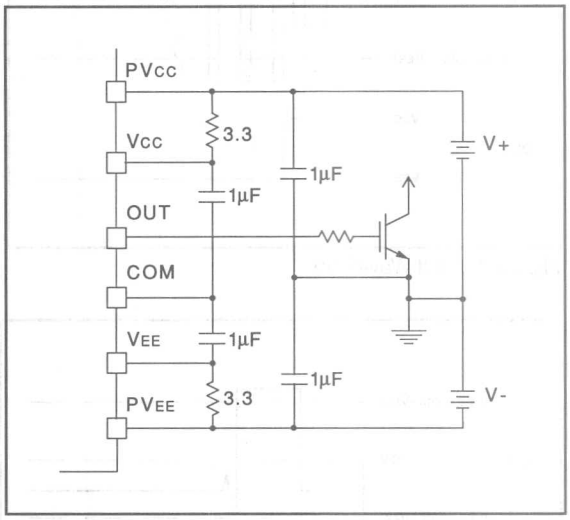


Figure 8. Using External Supplies

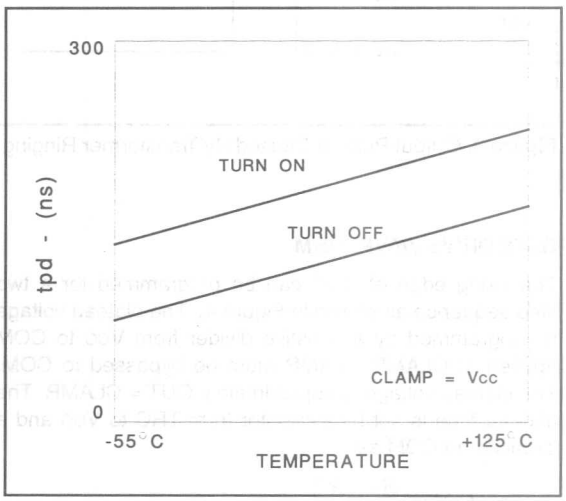


Figure 9. Input to Output Delay

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7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

UNITRODE

UCC1776
UCC2776
UCC3776
PRELIMINARY

Quad FET Driver

FEATURES

- High Peak Output Current Each Output – 1.5A Source, 2.0A Sink
- Wide Operating Voltage Range 4.5V to 18V
- Thermal Shutdown
- CMOS Compatible Inputs
- Outputs Are Active Low for Undervoltage Lockout Condition

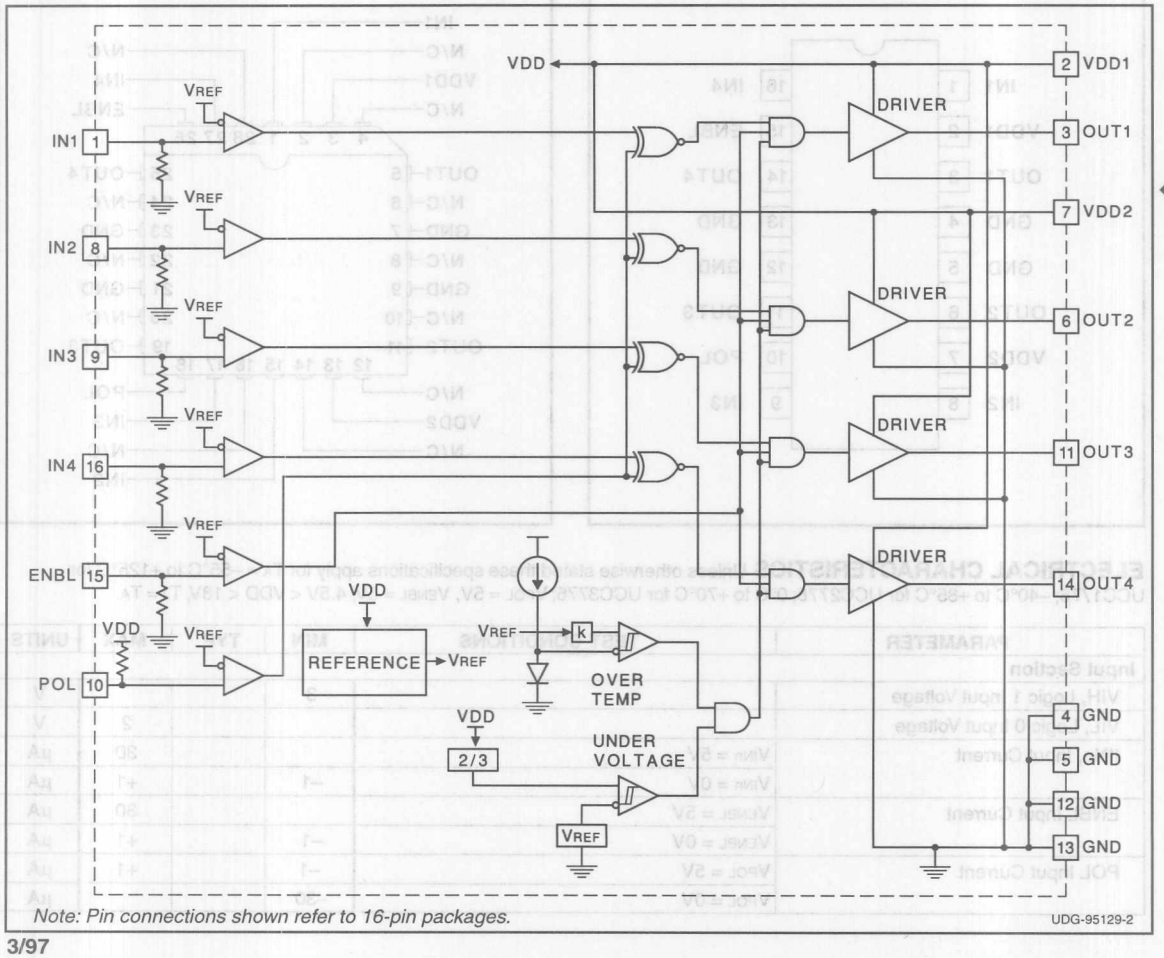
DESCRIPTION

The UCC3776 is a four output BCDMOS buffer/driver designed to drive highly capacitive loads such as power MOSFET gates at high speeds. The device can be configured as either an inverting or non-inverting driver via the POL pin. The outputs are enabled by ENBL. When disabled, all outputs are active low. The device incorporates thermal shutdown with hysteresis for stability. The device also includes an undervoltage lockout circuit (UVLO) with hysteresis which disables the outputs when VDD is below a preset threshold. The outputs are held low during undervoltage lockout, even in the absence of VDD power to the device. This helps prevent MOSFET turn-on due to capacitive current through the gate-drain capacitance of the power MOSFET in the presence of high dV/dts. The logic input thresholds are compatible with standard 5V HCMOS logic.

POWER DRIVERS

7

BLOCK DIAGRAM



Note: Pin connections shown refer to 16-pin packages.

UDG-95129-2

3/97

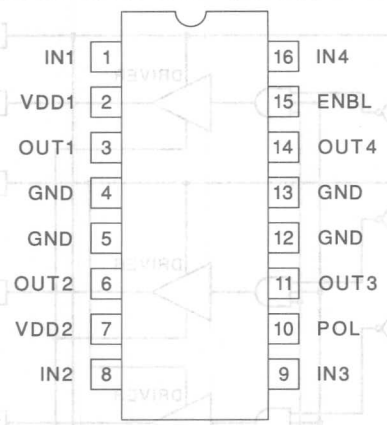
ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage, VDD1, VDD2 . . . . . .20V
Maximum DC Voltage Difference, VDD1 vs. VDD2 . . . . . .100mV
Logic Input, IN1, IN4, ENBL
Maximum forced voltage . . . . . –0.3 to VDD1 + 0.3V
Logic Inputs, IN2, IN3, POL
Maximum forced voltage . . . . . –0.3 to VDD2 + 0.3V
Latch-up Protection withstand Reverse Current
I_{REV}, OUT1, OUT2, OUT3, OUT4 . . . . . .500mA
Power Outputs, OUT1, OUT2, OUT3, OUT4
Maximum pulsed current (10% duty max, 10µsec max pulse width) 3A
Storage Temperature . . . . . –65°C to +150°C
Operating Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 Seconds) . . . . . .300°C

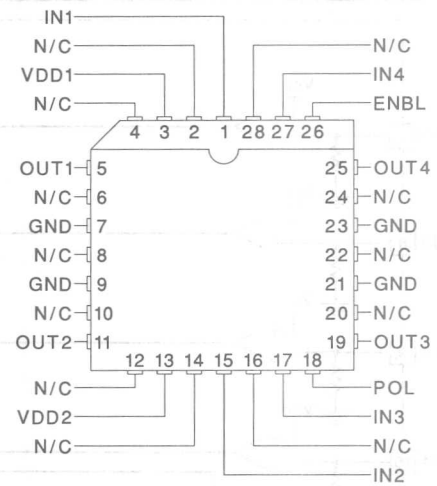
All currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAMS

DIL-16 (Top View)
N or J, DP Packages



PLCC-28 (Top View)
Q Package



ELECTRICAL CHARACTERISTICS

Unless otherwise stated these specifications apply for T_A = –55°C to +125°C for UCC1776; –40°C to +85°C for UCC2776; 0°C to +70°C for UCC3776; V_{POL} = 5V, V_{ENBL} = 5V, 4.5V < VDD < 18V, $T_J = T_A$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Section					
VIH, Logic 1 Input Voltage		3			V
VIL, Logic 0 Input Voltage				2	V
IINn, Input Current	V_{INn} = 5V			30	µA
	V_{INn} = 0V	–1		+1	µA
ENBL Input Current	V_{ENBL} = 5V			30	µA
	V_{ENBL} = 0V	–1		+1	µA
POL Input Current	V_{POL} = 5V	–1		+1	µA
	V_{POL} = 0V	–30			µA

ELECTRICAL CHARACTERISTICS (cont.) Unless otherwise stated these specifications apply for T_A = –55°C to +125°C for UCC1776; –40°C to +85°C for UCC2776; 0°C to +70°C for UCC3776; V_{POL} = 5V, V_{ENBL} = 5V, 4.5V < VDD < 18V, $T_J = T_A$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Section					
VOH, High Output Voltage	I_{OUTn} = -10mA, VDD1 = VDD2 = 12V, V_{INn} = 5V	VDD–1.0			V
VOL, Low Output Voltage	I_{OUTn} = 10mA, VDD1 = VDD2 = 12V, V_{INn} = 0V			0.15	V
Output Resistance	I_{OUTn} = 10mA, VDD1 = VDD2 = 12V, V_{INn} = 0V		6		Ω
Output High Peak Current	VDD1 = VDD2 = 12V, OUTn = 5V, V_{INn} = 5V, T_J = 25°C (Note 1)		–1.5		A
Output Low Peak Current	VDD1 = VDD2 = 12V, OUTn = 5V, V_{INn} = 0V, T_J = 25°C (Note 1)		2.0		A
UVLO Output Pull-down Voltage	VDD1 = VDD2 = 3V, I_{OUTn} = –10mA		0.8	1.5	V
Switching Time Section					
Output Rise Time	C_{OUTn} = 1nF, V_{OUTn} = 1V to 9V, VDD1 = VDD2 = 12V		25	50	nsec
Output Fall Time	C_{OUTn} = 1nF, V_{OUTn} = 9V to 1V, VDD1 = VDD2 = 12V		10	50	nsec
IN–>OUT Delay Time (Rising Output)	V_{INn} = 2.5V, V_{OUTn} = 0.1 • VDD, VDD1 = VDD2 = 12, C_{OUTn} = 0nF		40	100	nsec
IN–>OUT Delay Time (Falling Output)	V_{INn} = 2.5V, V_{OUTn} = 0.9 • VDD, VDD1 = VDD2 = 12V, C_{OUTn} = 0nF		50	100	nsec
Power Supply Section					
Power Supply Current	V(IN1–IN4) = 0V, V_{ENBL} = 0V, VDD1 = VDD2 = 12V			2	mA
UVLO Threshold				4.5	V
UVLO Hysteresis			0.5		V

Note 1: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

ENBL: Logic level input to enable the drivers. When ENBL is low, the drivers outputs will be at GND potential, regardless of the status of POL. The input threshold is designed to be 5 volt CMOS compatible, independent of the VDD voltage used on the device. There is a slight hysteresis in the input circuit to help reduce sensitivity to noise on the input signal or input ground.

GND: Ground for the device, the supply return for the VDDs. There are four GND pads on the device.

IN1 - IN4: Inputs to each driver (1-4). The input threshold is designed to be 5 volt CMOS compatible, independent of the VDD voltage used on the device. There is a slight hysteresis in the input circuit to help reduce sensitivity to noise.

OUT1 - OUT4: Outputs to each driver (1-4). The outputs are totem pole DMOS circuits. In the absence of VDD on the device, the outputs will stay off, even with a capacitive displacement current into the output node.

POL: Polarity selection for the drivers. A logic 0 selects inverting operation. A logic 1 selects non-inverting operation. The input threshold is designed to be 5 volt CMOS compatible, independent of the VDD voltage used on the device. There is a slight hysteresis in the input circuit to help reduce sensitivity to noise.

VDD1: Supply Voltage for drivers 1 and 4. Tied internally to VDD2.

VDD2: Supply Voltage for drivers 2 and 3. Tied internally to VDD1.

APPLICATION INFORMATION

Figure 1 depicts a block diagram of the UCC3776 Quad FET Driver. Four high current, high speed gate drivers with CMOS compatible input stages are provided. Polarity select and enable inputs provide circuit integration flexibility, while power packaging and high speed drive circuitry allow for driving high power MOSFET gates in high speed applications.

APPLICATION INFORMATION (cont.)

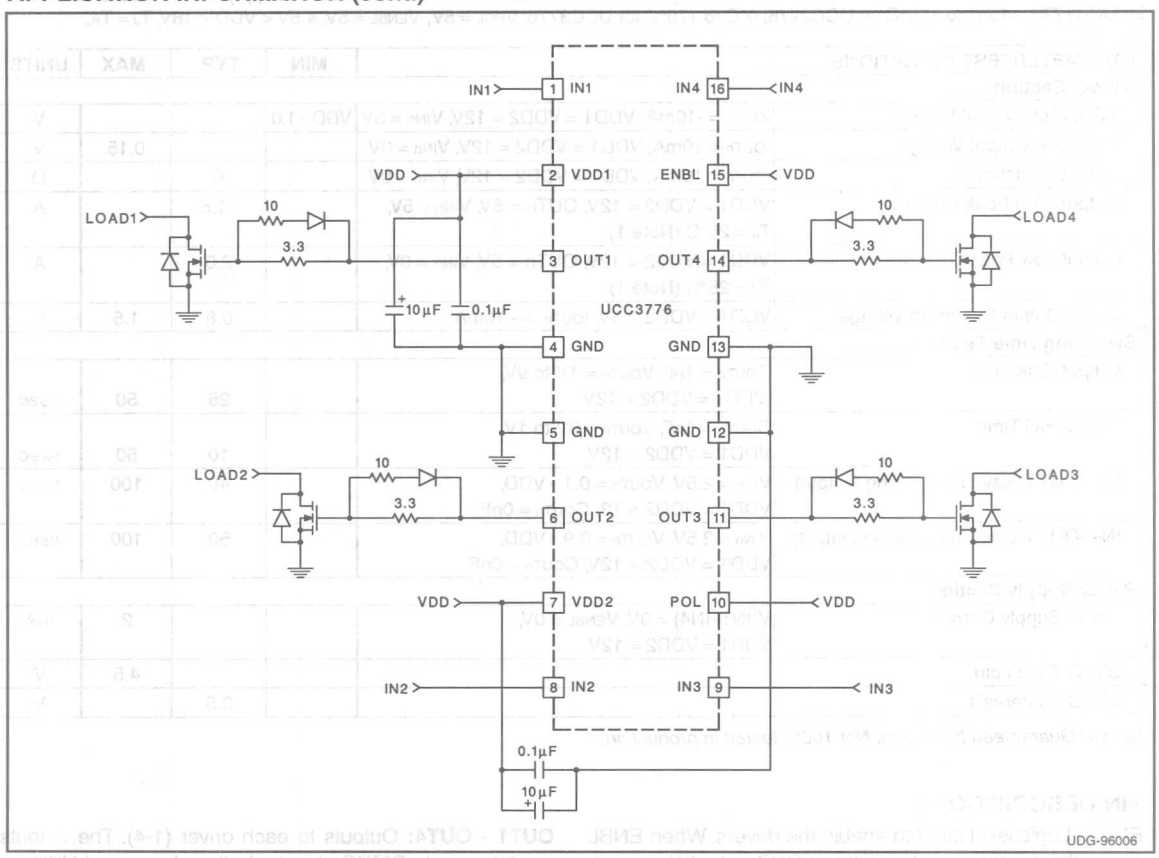


Figure 1. Typical FET Driver Application

Input Stage

Each of the four UCC3776 FET driver circuits provides an independent, CMOS compatible input stage. The allowable input voltage range extends from ground to VDD, allowing for easy interface to a wide variety of PWM and power supply support circuitry. The POL and ENBL inputs are tied to all four drivers, and all drivers must be configured as either inverting or noninverting, and all must be either enabled or not enabled.

To prevent oscillations in noisy PWM environments, any unused drivers should have their input stages tied to either VDD or ground. Unlike other CMOS FET drivers, quiescent power current is not significantly affected by the polarity of the driver input signal.

Output Stage/Gate Driver Considerations

Many power FET driver data sheets rely solely on rise and fall time specifications into a capacitive load to quantify speed performance. While these specifications are important, they do not provide all the required information. The UCC3776 specifies rise and fall times of 25ns and 10ns respectively into a load of 1nF. This specification can be used to calculate the average slew rate capability of the driver stage over the output voltage range.

However, the gate of a power MOSFET cannot be modeled accurately with a simple capacitor. The voltage/current requirements of the gate vary widely over several distinct phases of FET turn-on and turn-off. The most accurate way to calculate the switching times of power MOSFETs is to determine the total gate charge requirement (Qg), which is usually specified by the MOSFET manufacturer, and determine the peak current capability of the MOSFET gate driver. Ideally the driver's peak current can be delivered while the MOSFET gate is transitioning through its plateau or "Miller" level, when current demands are highest.

APPLICATION INFORMATION (cont.)

The UCC3776 specifies peak source and sink currents for a driver output voltage of 5V. This output voltage approximately coincides with the average gate plateau voltage of a power MOSFET. Outside of the plateau region the gate drive waveform is primarily limited by the slew rate capability of the driver. Through proper analysis of the MOSFET's gate drive requirements and the specifications for the UCC3776, an accurate model of AC performance can be created. For a detailed description of MOSFET AC gate drive requirements please see Unitrode Application Notes U-118 and U-137. Although the Unitrode power drivers referenced in these application notes are bipolar devices, the information relating to MOSFET gate drive characteristics is applicable.

Power Supply Decoupling/Grounding

The high peak currents required to charge high capacitance MOSFET gates make proper power supply decoupling and grounding essential. The UCC3776 provides two power supply inputs (VDD1 and VDD2) to allow for optimum internal circuit layout and minimum resistive voltage drop with high peak current loads. VDD1 provides the drive current for outputs 1 and 4, while VDD2 provides drive current for outputs 2 and 3. Both of these pins must be externally connected to the source power supply, and the DC potential difference between these two points should be limited to 100mV. Under no circumstances should an output driver be used with only one supply input connected.

To guarantee a low impedance current path over a wide frequency range, each supply input should be separately bypassed to ground with both a high value tantalum or electrolytic capacitor in parallel with a 0.1µF ceramic capacitor. The exact value of the tantalum or electrolytic capacitor will depend on the charge requirements of the MOSFET gate. For most applications a value between 1µF and 10µF should suffice. Connections for ground leads should be kept as short as possible. The driver chip and support electronics should be located over a large copper ground plane if layout conditions allow it.

Power Dissipation/Thermal Considerations

Being a CMOS device, the standby power dissipation of the UCC3776 is quite low. For a 15V supply, the maximum quiescent current of 2mA results in a maximum power loss of only 30mW. However, driving high frequency MOSFETs at high peak currents results in additional power dissipation. This is because each time the MOSFET gate is charged or discharged, the energy transfer is only 50% efficient. The same amount of energy that is transferred to the gate is lost in the drive stage.

In order to determine the average output stage loss, the gate drive energy (W_{GD}) is computed as:

$$1)\quad W_{GD} = 2 \bullet 0.5 \bullet C_G \bullet V^2 = \frac{Q_G}{V} \bullet V^2 = Q_G \bullet V$$

Where Q_G is the MOSFET's total gate charge, and V is the gate voltage. The factor of two results from the fact that the gate drive circuit must charge and discharge the gate every electrical cycle. Each time the gate is charged or discharged, the gate drive dissipates an amount of energy equal to the energy supplied to the gate. Power lost due to driving the gate is:

$$2)\quad PL_{GD} = \frac{W_{GD}}{T} = \frac{Q \bullet V}{T} = Q_G \bullet V \bullet F$$

Where F is the operating frequency of the MOSFET. This is a worst case assumption since the power loss is shared by the output driver and the gate resistor. If a relatively large value series gate resistor is used, the power loss in the gate driver is reduced. The penalty for this is slower switching speed, and therefore more loss in the MOSFET. For high power MOSFETs this power loss can be significant.

To illustrate a typical example of driver loss, consider a MOSFET with 70nC of gate charge and a 15V gate voltage. The power loss at 200kHz is:

$$3)\quad PL_{GD} = 70nC \bullet 15V \bullet 200kHz = 210mW$$

This analysis applies to one of the four drivers on the UCC3776. Four drivers operating under the same conditions results in a total power loss of 840mW. At higher frequencies the dissipation will be proportionally greater. This example demonstrates the need for power packaging which is available on the UCC3776, and not available on many other FET drivers.

After device power dissipation has been estimated, proper heat sinking must be provided to ensure that the device junction temperature does not exceed the specified maximum. Refer to the packaging section of the databook for package thermal impedance information.

Application Circuits

Figure 1 depicts a typical gate drive application circuit. Four independent, noninverting low side FET drivers are shown. Although series gate drive resistors are not required because all FET drivers have a finite peak current capability, it is good practice to include some series resistance to limit peak current and to prevent oscillations due to parasitic inductance and capacitance. The parallel diode and resistor allow for a faster gate turn off than turn on. This characteristic is often desirable for bridge driver applications to prevent MOSFET cross conduction in the power stage.

APPLICATION INFORMATION (cont.)

Figure 2 shows an applications circuit with paralleled output drivers. If it is required to drive high gate charge MOSFETs, the UCC3776 output drivers can be combined for higher peak current capability. It is good practice to provide separate gate resistor networks to each individual MOSFET as shown. This will ensure that each driver circuit will not see excessive current during the high gate charge portion of the switching waveform. This practice also tends to isolate driver circuits to reduce the possibility of ringing and crosstalk. If all four drivers are used to drive a single MOSFET, then four separate gate drive resistor networks should be used.

Figure 3 shows a transformer coupled full bridge power stage. The UCC3776 is ideally suited for interfacing between low power PWM outputs and high power output stages. Although the UC3879 phase shift controller is shown in this example, the UCC3776 can be used in many PWM controller applications where high power FET drivers are required.

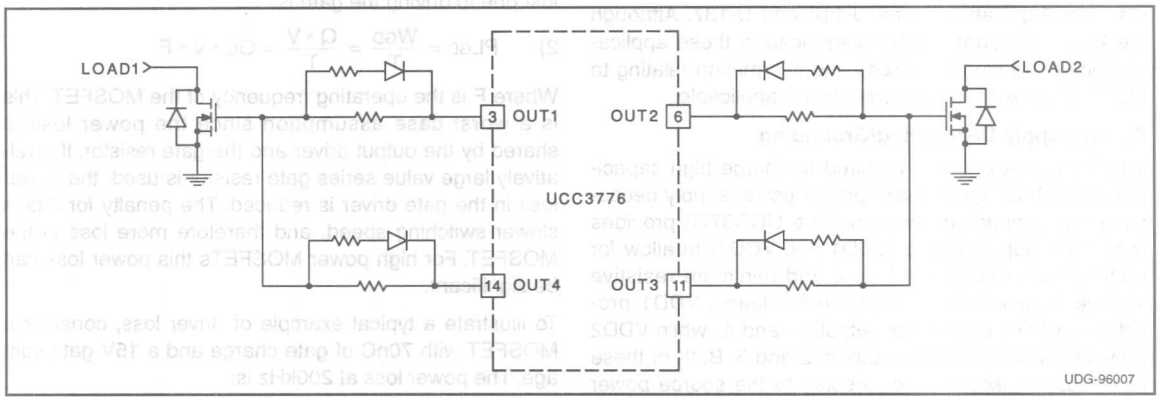


Figure 2. Parallel Output Drivers

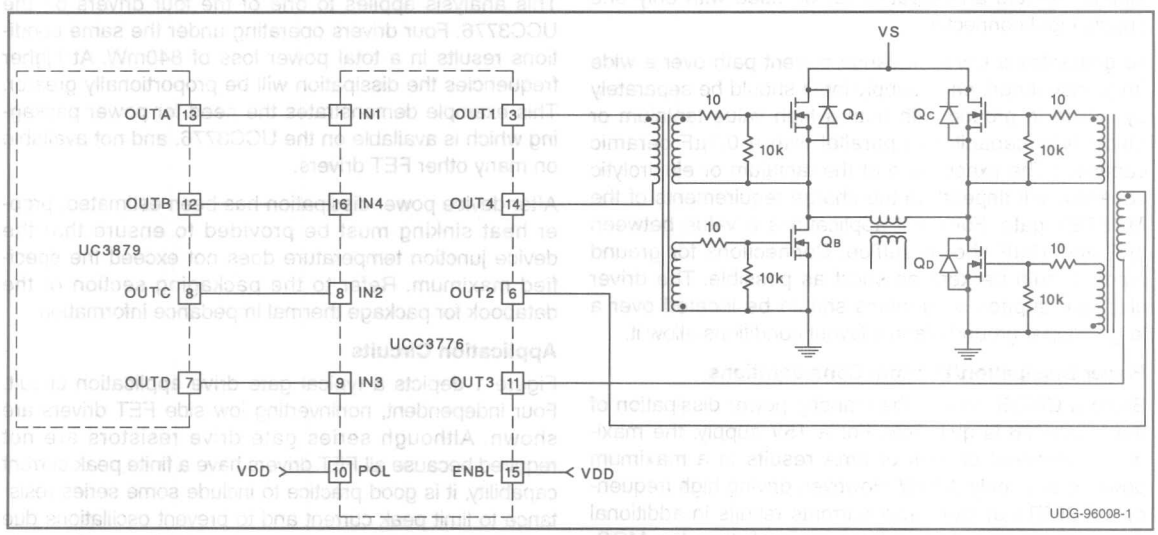


Figure 3. Full Bridge Driver Application

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Consult Applications Handbook for available applications/design notes.

Datasheets in this section are organized in numeric order using the commercial part number.

Portable Products

8

Packaging Note:

- *Values listed for recommended lead soldering time and temperature apply to ceramic thru-hole components only. Please consult the Packaging Section of this databook for recommendations on plastic SMD board attach processing.*

- *Unless otherwise noted, thermal resistance values listed on individual data sheets are for the device as it operates in a plastic thru-hole package. Results for other packaging options can be inferred by scaling the package rating values (thermal resistances) presented in the Packaging Section of this databook.*

Back Light, Battery Charger & Battery Protection Products

Back Light Products	UNITRODE PART NUMBER	
	UC3871	UC3872
Application	Zero Voltage Switched Fluorescent Lamp Driver with LCD Bias Supply	Zero Voltage Switched Fluorescent Lamp Driver
Topology	Push-pull	Push-pull
Voltage Range	4.5V to 20V	4.5V to 24V
Reference Tolerance	1.2%	1.2%
Open Lamp Detect	Y	Y
Soft Start	Y	Y
External Synchronization	Y	Y
Shutdown Current	1µA	1µA
Maximum Frequency	200kHz	200kHz
Lamp Intensity Control	Y	Y
Application/Design Note	U-141, U-148	DN-75, U-141, U-148

Battery Charger Products	UNITRODE PART NUMBER		
	UC3906	UC3909	UCC3956+
Battery Chemistry	Lead-Acid	Lead-Acid	Lithium-Ion
Control Topology	Linear	Switchmode	Switchmode
Reference Tolerance	1.3%	1%	1%
Temperature Compensation	Y	Y	N
Charge States	4	4	4
Over Charge Timer	N	N	Y
Status Bits	N	Y	Y
Average Current Mode Control	N/A	Y	Y
Application/Design Note	U-104, U-131	U-155	

Battery Protection Products	UNITRODE PART NUMBER		
	UCC3911+	UCC3951+	UCC3957+
Battery Chemistry	Lithium-Ion	Lithium-Ion	Lithium-Ion
Cells Protected	2	3, 4	3, 4
Threshold Tolerance	50mV	70mV	50mV
Protection FETs	Internal	External PMOS	External PMOS
Overcurrent Protection	Y	Y	Y
Overcurrent Delay	Y	Y	Y
Serial Bus	N	Y	N
A/D	N	Y	N
Shutdown Current	3.5µA	20µA	3.5µA

+ New Product

Linear Regulators	UNITRODE PART NUMBER		
	UCC381 ✚ ★	UCC383 ✚ ★	UCC384 ✚ ★
Output Voltage	3.3, 5, ADJ	3.3, 5, ADJ	5, 12, ADJ
Dropout Voltage	0.45V at 1A	0.45V at 3A	0.2V at 500mA
Quiescent Current	400µA	400µA	240µA
Maximum Input Voltage	9V	9V	–16V
Shutdown Current	10µA	10µA	20µA
Voltage Tolerance	2.5%	2.5%	2.5%
Line Regulation	0.01%/V	0.01%/V	0.01%/V
Load Regulation	0.1%, I_{OUT} = 0 to 1A	0.2%, I_{OUT} = 10mA to 3A	0.1%, I_{OUT} = 0 to 500mA

Power Management Products	UNITRODE PART NUMBER	
	UCC3930 ✚	UCC3941 ✚
Description	Cellular Telephone Power Converter	1V Synchronous Boost Converter
Application	3 Integrated Positive LDOs with Negative Supply	High Efficiency Integrated Boost Converter
Key Features	• Three Positive LDO Regulators • Negative Supply for MESFET Bias • Separate Logic Supply Enable • Power Good Indicator • Shutdown Mode	• Full Load Startup at 1V • Power Limit Control • Auxiliary 9V Supply • Output Disconnect • Shutdown Mode
Application/Design Note	DN-74	DN-73

Power Management Products (cont'd)	UNITRODE PART NUMBER	
	UCC3946	UCC3954 ✚
Description	Microprocessor Supervisor with Watchdog Timer	Single Cell Lithium-Ion to 3.3V Converter
Application	Accurate Microprocessor Supervision	High Efficiency Flyback Converter
Key Feature	• Programmable Reset Threshold • Programmable Reset Period • Programmable Watchdog Period • 1.5% Accurate Threshold • 4µA IDD	• Fixed 3.3V Output • 750mA Output Current • Low Battery Warning • Low Battery Disconnect • Shutdown Mode

✚ New Product
★ Refer to Linear Regulator Section for Product Data Sheet

IrDA Products	UNITRODE PART NUMBER				
	UCC5340	UCC5341✚	UCC5342✚	UCC5343✚	UCC5344✚
Device Type	Receiver	Receiver	Transceiver	Transceiver	Transceiver
Supply Voltage	3.3V or 5V	3.3V or 5V	3.3V or 5V	3.3V or 5V	3.3V or 5V
Data Rate	2.4kBPS to 115.2kBPS	2.4kBPS to 115.2kBPS	2.4kBPS to 115.2kBPS	2.4kBPS to 115.2kBPS	9.6kBPS to 4mBPS
Dynamic Range	150nA to 100mA	100nA to 100mA	100nA to 100mA	100nA to 100mA	100nA to 100mA
Quiescent Current	90µA	250µA	250µA	250µA	900µA
Encoder/Decoder	N	N	N	Y	N
IrDA Compliant	Y	Y	Y	Y	Y
LED Driver	N/A	N/A	500mA	500mA	500mA

✚ New Product


UNITRODE

UNITRODE

APPLICATION INFORMATION

UC1871
UC2871
UC3871

Resonant Fluorescent Lamp Driver

FEATURES

- 1µA ICC when Disabled
- PWM Control for LCD Supply
- Zero Voltage Switched (ZVS) on Push-Pull Drivers
- Open Lamp Detect Circuitry
- 4.5V to 20V Operation
- Non-saturating Transformer Topology
- Smooth 100% Duty Cycle on Buck PWM and 0% to 95% on Flyback PWM

DESCRIPTION

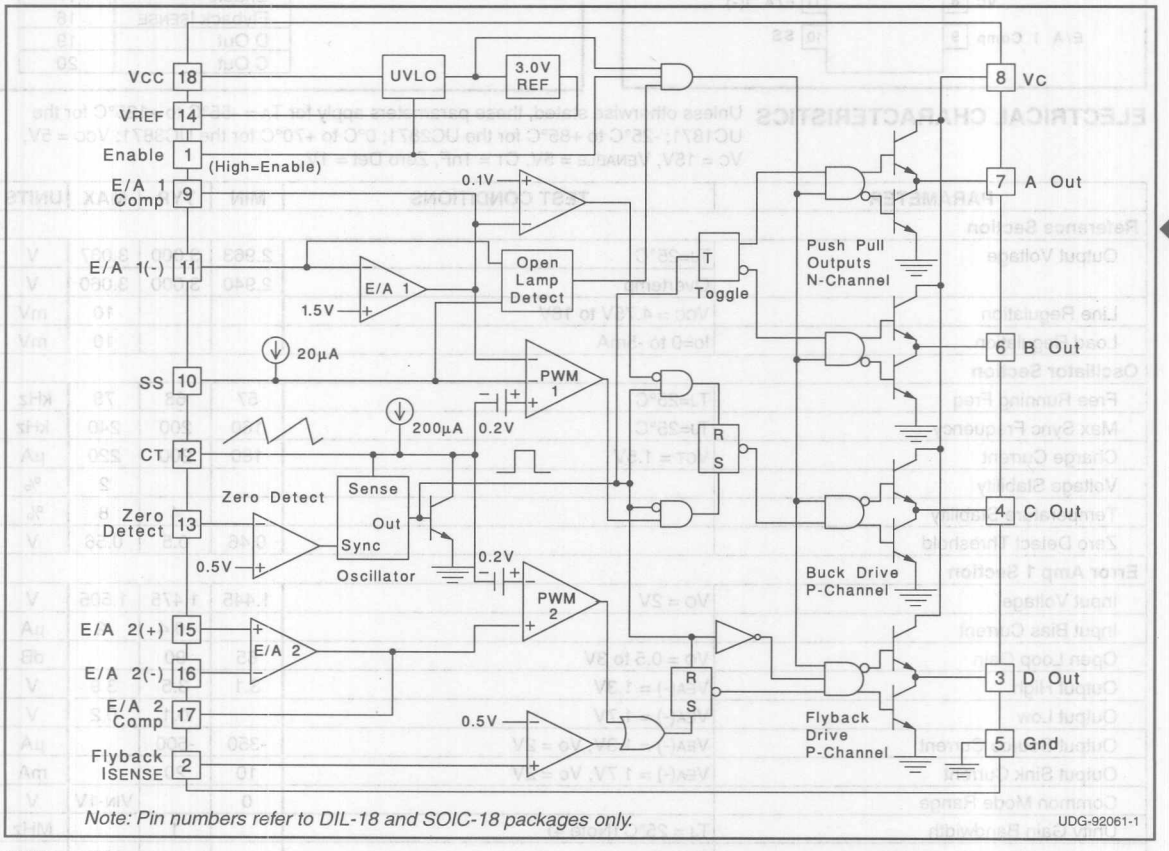
The UC1871 Family of IC's is optimized for highly efficient fluorescent lamp control. An additional PWM controller is integrated on the IC for applications requiring an additional supply, as in LCD displays. When disabled the IC draws only 1µA, providing a true disconnect feature, which is optimum for battery powered systems. The switching frequency of all outputs are synchronized to the resonant frequency of the external passive network, which provides Zero Voltage Switching on the Push-Pull drivers.

Soft-Start and open lamp detect circuitry have been incorporated to minimize component stress. An open lamp is detected on the completion of a soft-start cycle.

The Buck controller is optimized for smooth duty cycle control to 100%, while the flyback control ensures a maximum duty cycle of 95%.

Other features include a precision 1% reference, under voltage lockout, flyback current limit, and accurate minimum and maximum frequency control.

BLOCK DIAGRAM



Note: Pin numbers refer to DIL-18 and SOIC-18 packages only.

UDG-92061-1

10/94

PORTABLE PRODUCTS

8

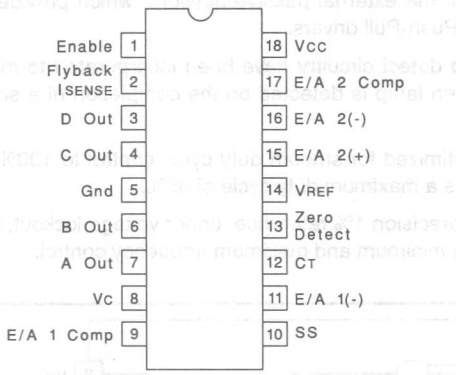
ABSOLUTE MAXIMUM RATINGS

Analog Inputs . . . . . –0.3 to +10V
Vcc, Vc Voltage . . . . . +20V
Zero Detect Input Current
  High Impedance Source . . . . . +10mA
Zero Detect
  Low Impedance Source. . . . . +20V
Power Dissipation at TA = 25°C 1W
Storage Temperature . . . . . -65°C to +150°C
Lead Temperature . . . . . 300°C

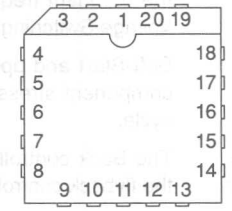
Note 1: Currents are positive into, negative out of the specified terminal.
Note 2: Consult Packaging Section of Databook for thermal limitations and considerations of package.

CONNECTION DIAGRAMS

DIL-18, SOIC-18 (TOP VIEW)
J or N, DW Package



PLCC-20 (Top View)
Q Package



PACKAGE PIN FUNCTION	
FUNCTION	PIN
Gnd	1
B Out	2
A Out	3
Vc	4
E/A 1 Comp	5
SS	6
E/A 1(-)	7
N/C	8
CT	9
Zero Detect	10
N/C	11
VREF	12
E/A 2(+)	13
E/A 2(-)	14
E/A 2 Comp	15
Vcc	16
Enable	17
Flyback ISENSE	18
D Out	19
C Out	20

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these parameters apply for TA = -55°C to +125°C for the UC1871; -25°C to +85°C for the UC2871; 0°C to +70°C for the UC3871; Vcc = 5V, Vc = 15V, VENABLE = 5V, CT = 1nF, Zero Det = 1V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Reference Section					
Output Voltage	TJ=25°C	2.963	3.000	3.037	V
	Overtemp	2.940	3.000	3.060	V
Line Regulation	Vcc = 4.75V to 18V			10	mV
Load Regulation	Io=0 to -5mA			10	mV
Oscillator Section					
Free Running Freq	TJ=25°C	57	68	78	kHz
Max Sync Frequency	TJ=25°C	160	200	240	kHz
Charge Current	VCT = 1.5V	180	200	220	µA
Voltage Stability				2	%
Temperature Stability			4	8	%
Zero Detect Threshold		0.46	0.5	0.56	V
Error Amp 1 Section					
Input Voltage	Vo = 2V	1.445	1.475	1.505	V
Input Bias Current			-0.4	-2	µA
Open Loop Gain	Vo = 0.5 to 3V	65	90		dB
Output High	VEA(-) = 1.3V	3.1	3.5	3.9	V
Output Low	VEA(-) = 1.7V		0.1	0.2	V
Output Source Current	VEA(-) = 1.3V, Vo = 2V	-350	-500		µA
Output Sink Current	VEA(-) = 1.7V, Vo = 2V	10	20		mA
Common Mode Range		0		VIN-1V	V
Unity Gain Bandwidth	TJ = 25°C (Note 4)		1		MHz
Maximum Source Impedance	Note 5			100k	Ω

CHARACTERISTICS (cont.)

-25°C to +85°C for the UC2871; 0°C to +70°C for the UC3871; V_{CC} = 5V, V_C = 15V, V_{ENABLE} = 5V, C_T = 1nF, Zero Det = 1V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Open Lamp Detect Section					
Soft Start Threshold	V_{EA}(-) = 0V	2.9	3.4	3.8	V
Error Amp Threshold	V_{SS} = 4.2V	0.7	1.0	1.3	V
Soft Start Current	V_{SS} = 2V	10	20	40	µA
Error Amp 2 Section					
Input Offset Voltage	V_O = 2V		0	10	mV
Input Bias Current			-0.2	-1	µA
Input Offset Current				0.5	µA
Open Loop Gain	V_O = 0.5 to 3V	65	90		dB
Output High	V_{ID} = 100mV, V_O = 2V	3.6	4	4.4	V
Output Low	V_{ID} = -100mv, V_O = 2V		0.1	0.2	V
Output Source Current	V_{ID} = 100mV, V_O = 2V	-350	-500		µA
Output Sink Current	V_{ID} = -100mV, V_O = 2V	10	20		mA
Common Mode Range		0		V_{IN}-2V	V
Unity Gain Bandwidth	T_J = 25°C (Note 4)		1		MHz
Isense Section					
Threshold		0.475	0.525	0.575	V
Output Section					
Output Low Level	I_{OUT} = 0, Outputs A and B		0.05	0.2	V
	I_{OUT} = 10mA		0.1	0.4	V
	I_{OUT} = 100mA		1.5	2.2	V
Output High Level	I_{OUT} = 0, Outputs C and D	14.7	14.9		V
	I_{OUT} = -10mA	13.5	14.3		V
	I_{OUT} = -100mA	12.5	13.5		V
Rise Time	T_J = 25°C, Cl = 1nF(Note 4)		30	80	ns
Fall Time	T_J = 25°C, Cl = 1nF(Note 4)		30	80	ns
Output Dynamics					
Out A and B Duty Cycle		48	49.9	50	%
Out C Max Duty Cycle	V_{EA1}(-) = 1V	100			%
Out C Min Duty Cycle	V_{EA1}(-) = 2V			0	%
Out D Max Duty Cycle	V_{EA2}(+)- V_{EA2}(-) = 100mV		92	96	%
Out D Min Duty Cycle	V_{EA2}(+)- V_{EA2}(-) = -100mV			0	%
Under Voltage Lockout Section					
Start-Up Threshold		3.7	4.2	4.5	V
Hysterisis		120	200	280	mV
Enable Section					
Input High Threshold		2			V
Input low Threshold				0.8	V
Input Current	V_{ENABLE} = 5V		150	400	µA
Supply Current Section					
VCC Supply Current	V_{CC} = 20V		8	14	mA
VC Supply Current	V_C=20V		7	12	mA
ICC Disabled	V_{CC} = 20V, V_{ENABLE} = 0V		1	10	µA

Note 3: Unless otherwise specified, all voltages are with respect to ground. Currents are positive into, and negative out of the specified terminal.
Note 4: Guaranteed by design but not 100% tested in production.
Note 5: Impedance below specified maximum guarantees proper operation of the Open Lamp Detect.

TYPICAL APPLICATION

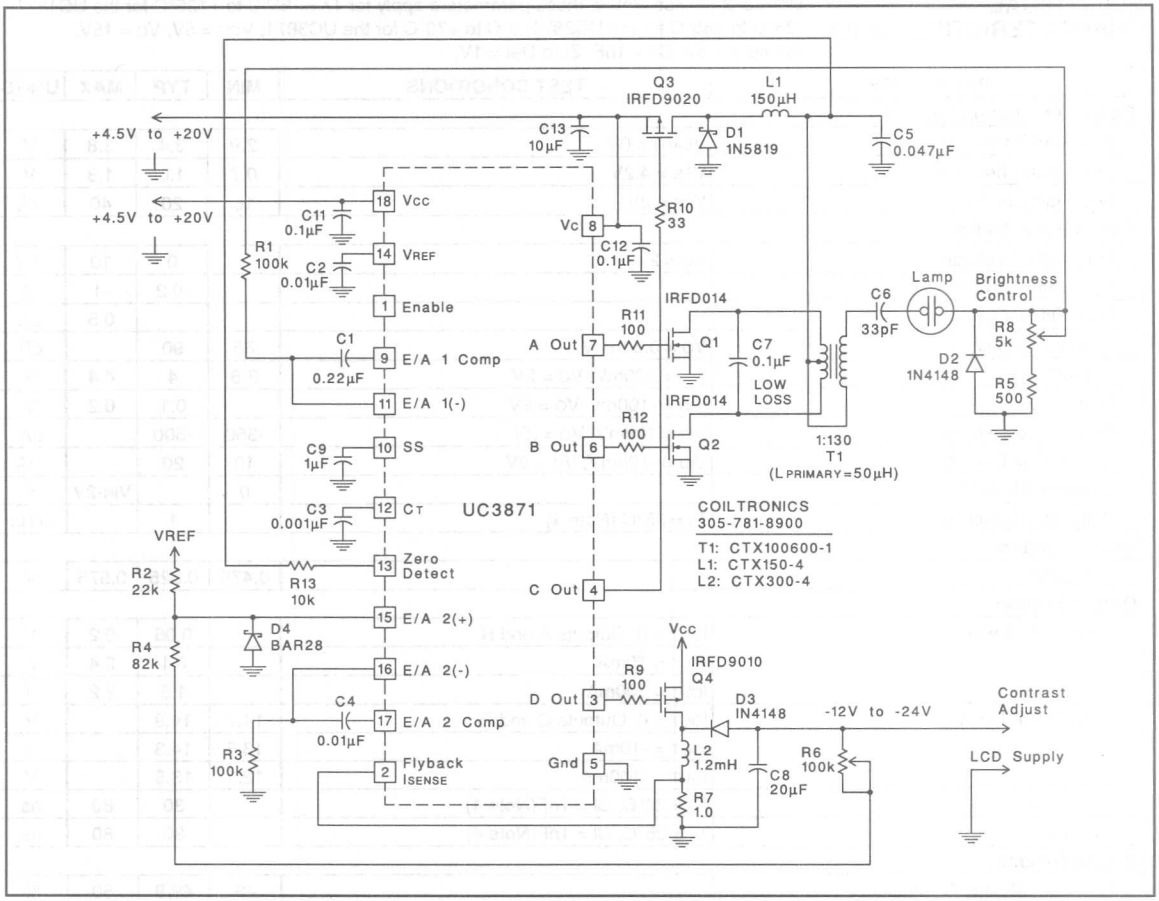


Figure 1

APPLICATION INFORMATION

Figure 1 shows a complete application circuit using the UC3871 Resonant Fluorescent lamp and LCD driver. The IC provides all drive, control and housekeeping functions to implement CCFL and LCD converters. The buck output voltage (transformer center-tap) provides the zero crossing and synchronization signal. The LCD supply modulator is also synchronized to the resonant tank.

The buck modulator drives a P-channel MOSFET directly, and operates over a 0-100% duty-cycle range. The modulation range includes 100%, allowing operation with minimal headroom. The LCD supply modulator also directly drives a P-channel MOSFET, but it's duty-cycle is limited to 95% to prevent flyback supply foldback.

The oscillator and synchronization circuitry are shown in Figure 2. The oscillator is designed to synchronize over a 3:1 frequency range. In an actual application however, the frequency range is only about 1.5:1. A zero detect comparator senses the primary center-tap voltage, generating a synchronization pulse when the resonant waveform falls to zero. The actual threshold is 0.5 volts, providing a small amount of anticipation to offset propagation delay.

The synchronization pulse width is the time that the 4mA current sink takes to discharge the timing capacitor to 0.1 volts. This pulse width sets the LCD supply modulator minimum off time, and also limits the minimum linear control range of the buck modulator. The 200µA current source charges the capacitor to a maximum of 3 volts. A comparator blanks the zero detect signal until the capacitor voltage exceeds 1 volt, preventing multiple synchronization pulse generation and setting the maximum frequency. If the capacitor voltage reaches 3 volts (a zero detection has not occurred) an internal clock pulse is generated to limit the minimum frequency.

APPLICATION INFORMATION (cont.)

UC3871 Oscillator Section

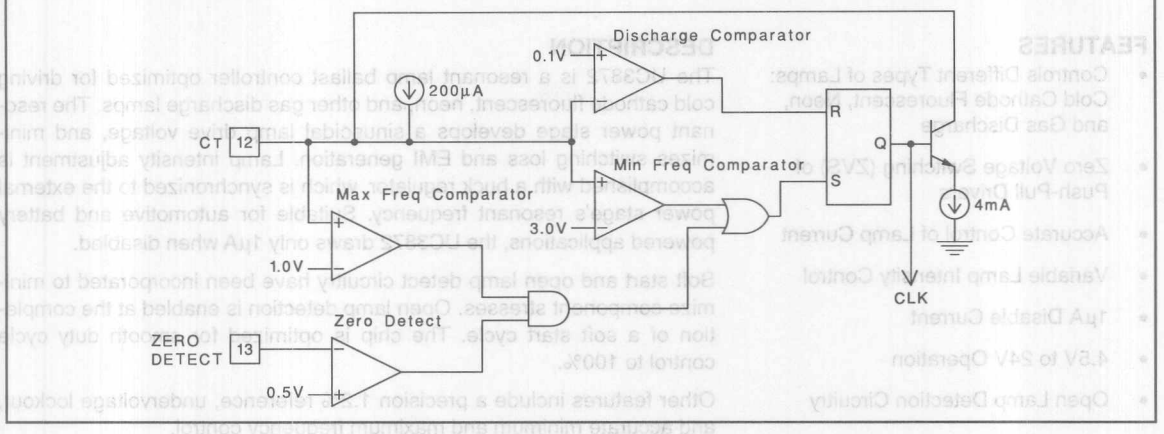


Figure 2

A unique protection feature incorporated in the UC3871 is the Open Lamp Detect circuit. An open lamp interrupts the current feedback loop and causes very high secondary voltage. Operation in this mode will usually breakdown the transformer's insulation, causing permanent damage to the converter. The open lamp detect circuit, shown in Figure 3 senses the lamp current feedback signal at the error amplifiers input, and shuts down the outputs if insufficient signal is present. Soft-start circuitry limits initial turn-on currents and blanks the open lamp detect signal.

Other features are included to minimize external circuitry requirements. A logic level enable pin shuts down the IC, allowing direct connection to the battery. During shutdown, the IC typically draws less than 1µA. The UC3871, operating from 4.5V to 20V, is compatible with almost all battery voltages used in portable computers. Under-voltage lockout circuitry disables operation until sufficient supply voltage is available, and a 1% voltage reference insures accurate operation. Both inputs to the LCD supply error amplifier are uncommitted, allowing positive or negative supply loop closure without additional circuitry. The LCD supply modulator also incorporates cycle-by-cycle current limiting for added protection.

UC1871 Open Lamp Detect Circuitry

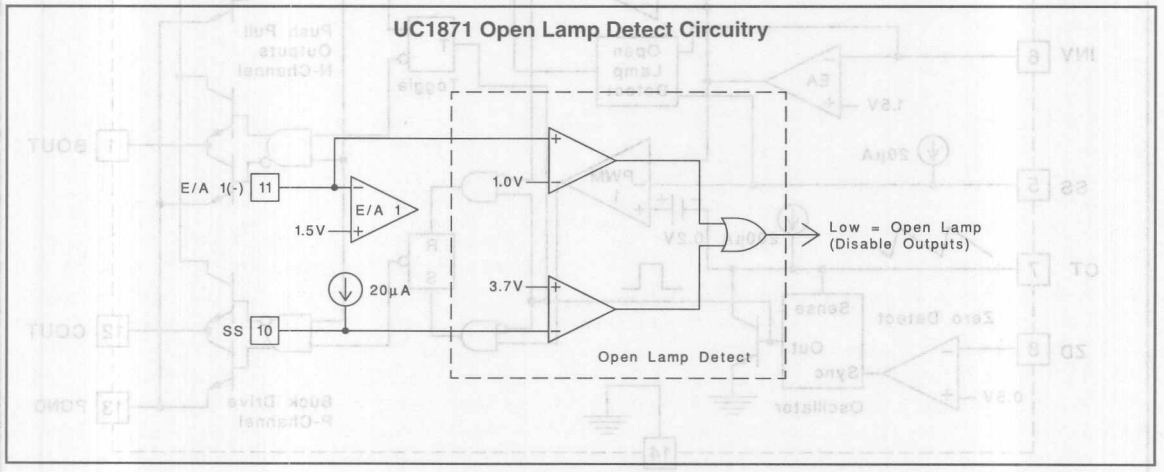


Figure 3

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TEL. (603) 424-2410 • FAX (603) 424-3460

UNITRODE

UC1872
UC2872
UC3872

Resonant Lamp Ballast Controller

FEATURES

- Controls Different Types of Lamps: Cold Cathode Fluorescent, Neon, and Gas Discharge
- Zero Voltage Switching (ZVS) of Push-Pull Drivers
- Accurate Control of Lamp Current
- Variable Lamp Intensity Control
- 1µA Disable Current
- 4.5V to 24V Operation
- Open Lamp Detection Circuitry

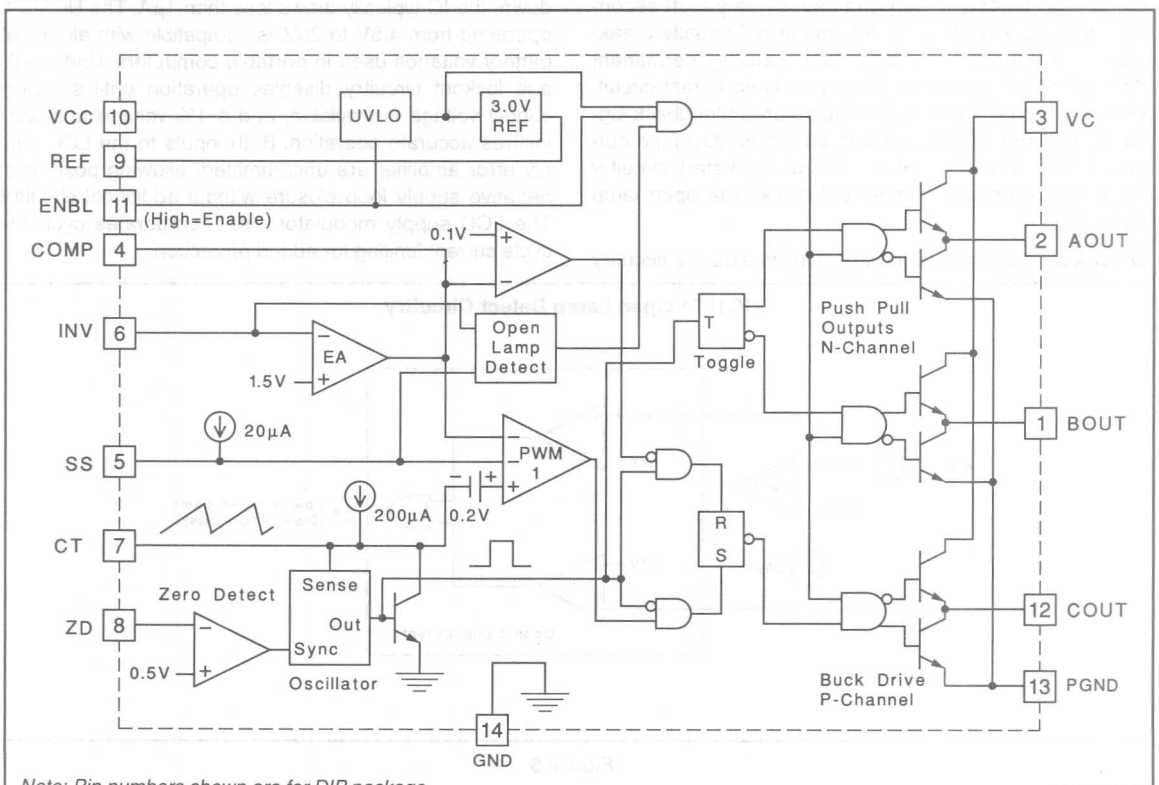
DESCRIPTION

The UC3872 is a resonant lamp ballast controller optimized for driving cold cathode fluorescent, neon, and other gas discharge lamps. The resonant power stage develops a sinusoidal lamp drive voltage, and minimizes switching loss and EMI generation. Lamp intensity adjustment is accomplished with a buck regulator, which is synchronized to the external power stage's resonant frequency. Suitable for automotive and battery powered applications, the UC3872 draws only 1µA when disabled.

Soft start and open lamp detect circuitry have been incorporated to minimize component stresses. Open lamp detection is enabled at the completion of a soft start cycle. The chip is optimized for smooth duty cycle control to 100%.

Other features include a precision 1.2% reference, undervoltage lockout, and accurate minimum and maximum frequency control.

BLOCK DIAGRAM



Note: Pin numbers shown are for DIP package.

UDG-93017-2

3/97

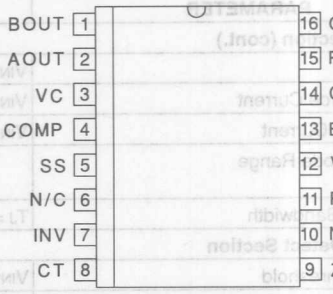
ABSOLUTE MAXIMUM RATINGS

Analog Inputs . . . . . –0.3 to +10V
VCC, VC Voltage . . . . . +24V
ZD Input Current
  High Impedance Source . . . . . +10mA
ZD Input Voltage
  Low Impedance Source. . . . . +24V
Power Dissipation at T_A = 25°C 1W
Storage Temperature . . . . . –65°C to +150°C
Lead Temperature . . . . . 300°C

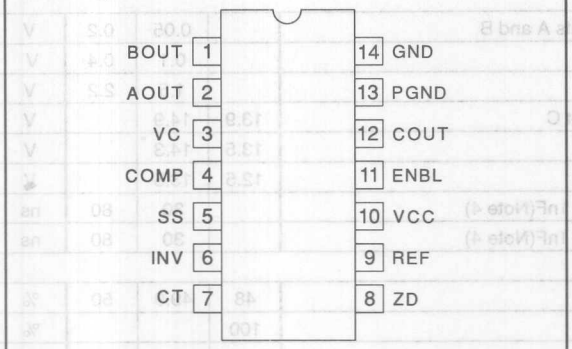
Note 1: Currents are positive into, negative out of the specified terminal.
Note 2: Consult Packaging Section of Databook for thermal limitations and considerations of package.

CONNECTION DIAGRAMS

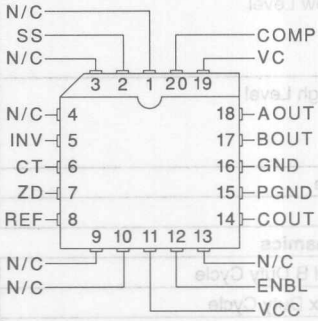
SOIC-16, SSOP-16 (TOP VIEW)
DW, M Package



DIL-14 (TOP VIEW)
N Package



PLCC-20 (Top View)
Q Package



ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these parameters apply for T_J = –55°C to +125°C for the UC1872, –40°C to +85°C for the UC2872, –0°C to +70°C for the UC3872; VCC= 5V, VC = 15V, V_{ENBL} = 5V, CT = 1nF, ZD = 1V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Reference Section					
Output Voltage	T_J = 25°C	2.963	3.000	3.037	V
	Over Temperature	2.940	3.000	3.060	V
Line Regulation	VCC = 4.75V to 18V			10	mV
Load Regulation	I_O = 0 to –5mA			10	mV
Oscillator Section					
Free Running Frequency	T_J = 25°C	57	68	78	kHz
Maximum Synchronization Frequency	T_J = 25°C	160	200	240	kHz
Charge Current	V_{CT} = 1.5V	180	200	220	µA
Voltage Stability				2	%
Temperature Stability			4	8	%
Zero Detect Threshold		0.46	0.5	0.56	V
Error Amp Section					
Input Voltage	V_O = 2V	1.445	1.475	1.505	V
Input Bias Current			–0.4	–2	µA
Open Loop Gain	V_O = 0.5 to 3V	65	90		dB
Output High	V_{INV} = 1.3V	3.1	3.5	3.9	V

ELECTRICAL CHARACTERISTICS (cont.): Unless otherwise stated, these parameters apply for T_J = –55°C to +125°C for the UC1872, –40°C to +85°C for the UC2872, –0°C to +70°C for the UC3872; VCC= 5V, VC = 15V, V_{ENBL} = 5V, CT = 1nF, ZD = 1V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Error Amp Section (cont.)					
Output Low	V_{INV} = 1.7V		0.1	0.2	V
Output Source Current	V_{INV} = 1.3V, Vo = 2V	–350	–500		µA
Output Sink Current	V_{INV} = 1.7V, Vo = 2V	10	20		mA
Common Mode Range		0		V_{IN}–1V	V
Unity Gain Bandwidth	T_J = 25°C (Note 4)		1		MHz
Open Lamp Detect Section					
Soft Start Threshold	V_{INV} = 0V	2.9	3.4	3.8	V
Open Lamp Detect Threshold	V_{SS} = 4.2V	0.6	1.0	1.4	V
Soft Start Current	V_{SS} = 2V	10	20	40	µA
Output Section					
Output Low Level	I_{OUT} = 0, Outputs A and B		0.05	0.2	V
	I_{OUT} = 10mA		0.1	0.4	V
	I_{OUT} = 100mA		1.5	2.2	V
Output High Level	I_{OUT} = 0, Output C	13.9	14.9		V
	I_{OUT} = –10mA	13.5	14.3		V
	I_{OUT} = –100mA	12.5	13.5		V
Rise Time	T_J = 25°C, Cl = 1nF(Note 4)		30	80	ns
Fall Time	T_J = 25°C, Cl = 1nF(Note 4)		30	80	ns
Output Dynamics					
Out A and B Duty Cycle		48	49.9	50	%
Out C Max Duty Cycle	V_{INV} = 1V	100			%
Out C Min Duty Cycle	V_{INV} = 2V			0	%
Under Voltage Lockout Section					
Startup Threshold Voltage		3.7	4.2	4.5	V
Hysteresis		120	200	280	mV
Enable Section					
Input High Threshold		2			V
Input low Threshold				0.8	V
Input Current	V_{ENBL} = 5V		150	400	µA
Supply Current Section					
VCC Supply Current	VCC = 24V		6	14	mA
VC Supply Current	VC = 24V		5	12	mA
ICC Disabled	VCC = 24V, V_{ENBL} = 0V		1	10	µA

Note 3: Unless otherwise specified, all voltages are with respect to ground. Currents are positive into, and negative out of the specified terminal.
Note 4: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

AOUT, BOUT: These outputs provide complementary drive signals for the push-pull N-channel MOSFETs. Each one is high for 50% of the time, switching states each time a zero-detect is sensed.

COMP: COMP is the output terminal of the error amplifier. Compensation components are normally connected between COMP and INV. Connecting a capacitor from this pin to ground limits turn on current and blanks the open lamp detect signal allowing the lamp to start.

COUT: This output directly drives the bulk regulator P-channel MOSFET. COUT turn-on is synchronized to each zero-detect, and therefore switches at twice the fre-

quency of AOUT and BOUT. The modulator controlling COUT is designed to provide smooth control up to 100% duty cycle.

CT: A capacitor connected between this pin and GND ground sets the synchronization frequency range. The capacitor is charged with approximately 200µA, creating a linear ramp which is used by COUT's (buck regulator driver) PWM comparator.

ENBL: When ENBL is driven high the device is enabled. When ENBL is pulled low, the IC is shut down and typically draws 1µA.

GND: This pin is the ground reference point for the internal reference and all thresholds.

INV: This pin is the inverting input to the error amplifier and the input for the open lamp detect circuitry. If the voltage at INV is below the 1V open lamp detect threshold, the outputs are disabled.

PGND: This pin is the high current ground connection for the three output drivers.

REF: This pin is connected to the 3V reference voltage which is used for the internal logic. Bypass REF to ground with a 0.01µF ceramic capacitor for proper operation.

VC: VC is the power supply voltage connection for the output drivers. Bypass it to ground with a 0.1µF ceramic capacitor for proper operation.

VCC: VCC is the positive supply voltage for the chip. Its operating range is from 4.2V to 24V. Bypass VCC to ground with a 0.1µF ceramic capacitor for proper operation.

ZD: The zero-detect input senses when the transformer's primary center tap voltage falls to zero to synchronize the sawtooth voltage waveform on CT. The threshold is approximately 0.5V, providing a small amount of offset such that with propagation delay, zero-volt switching occurs. A resistor (typically 10k) should be connected between ZD and the primary center tap to limit input current at turn off.

TYPICAL APPLICATION

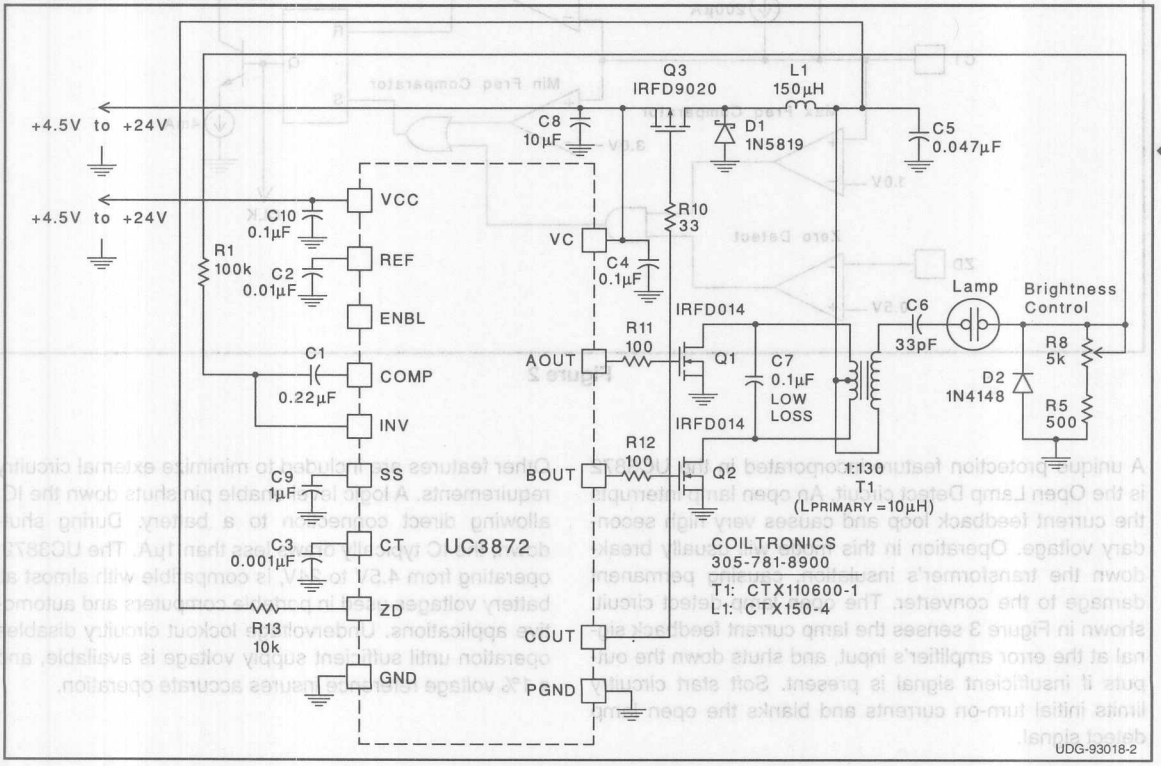


Figure 1

APPLICATION INFORMATION

Figure 1 shows a complete application circuit using the UC3872 Resonant Lamp Ballast Controller. The IC provides all drive, control and housekeeping functions. The buck output voltage (transformer center-tap) provides the zero crossing and synchronization signals.

The buck modulator drives a P-channel MOSFET directly, and operates over a 0-100% duty-cycle range. The modulation range includes 100%, allowing operation with minimal headroom.

The oscillator and synchronization circuitry are shown in Figure 2. The oscillator is designed to synchronize over a 3:1 frequency range. In an actual application however, the frequency range is only about 1.5:1. A zero detect comparator senses the primary center-tap voltage, generating a synchronization pulse when the resonant waveform falls to zero. The actual threshold is 0.5 volts, providing a small amount of anticipation to offset propagation delay.

The synchronization pulse width is the time required for the 4mA current sink to discharge the timing capacitor to 0.1 volts. This pulse width limits the minimum linear control range of the buck regulator. The 200µA current source charges the capacitor to a maximum of 3 volts. A comparator blanks the zero detect signal until the capacitor voltage exceeds 1 volt, preventing multiple synchronization pulse generation and setting the maximum frequency. If the capacitor voltage reaches 3 volts (a zero detection has not occurred) an internal clock pulse is generated to limit the minimum frequency.

UC3872 Oscillator Section

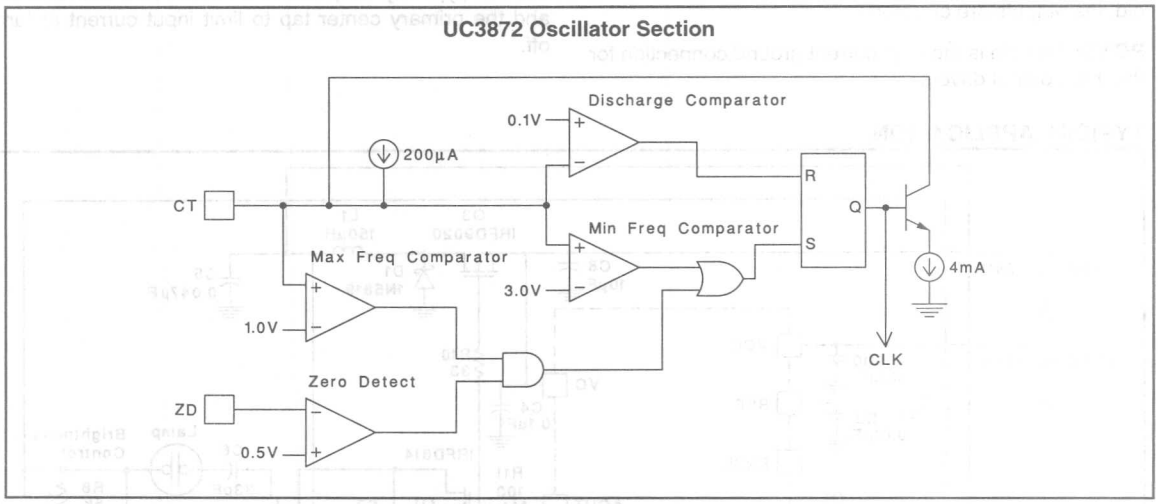


Figure 2

A unique protection feature incorporated in the UC3872 is the Open Lamp Detect circuit. An open lamp interrupts the current feedback loop and causes very high secondary voltage. Operation in this mode will usually breakdown the transformer's insulation, causing permanent damage to the converter. The open lamp detect circuit, shown in Figure 3 senses the lamp current feedback signal at the error amplifier's input, and shuts down the outputs if insufficient signal is present. Soft start circuitry limits initial turn-on currents and blanks the open lamp detect signal.

Other features are included to minimize external circuitry requirements. A logic level enable pin shuts down the IC, allowing direct connection to a battery. During shutdown, the IC typically draws less than 1µA. The UC3872, operating from 4.5V to 24V, is compatible with almost all battery voltages used in portable computers and automotive applications. Undervoltage lockout circuitry disables operation until sufficient supply voltage is available, and a 1% voltage reference insures accurate operation.

APPLICATION INFORMATION (cont.)

UC3872 Open Lamp Detect Circuitry

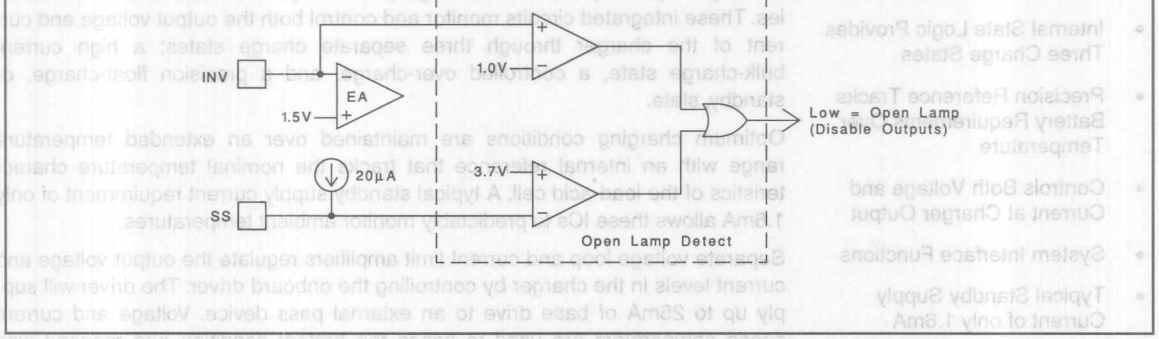
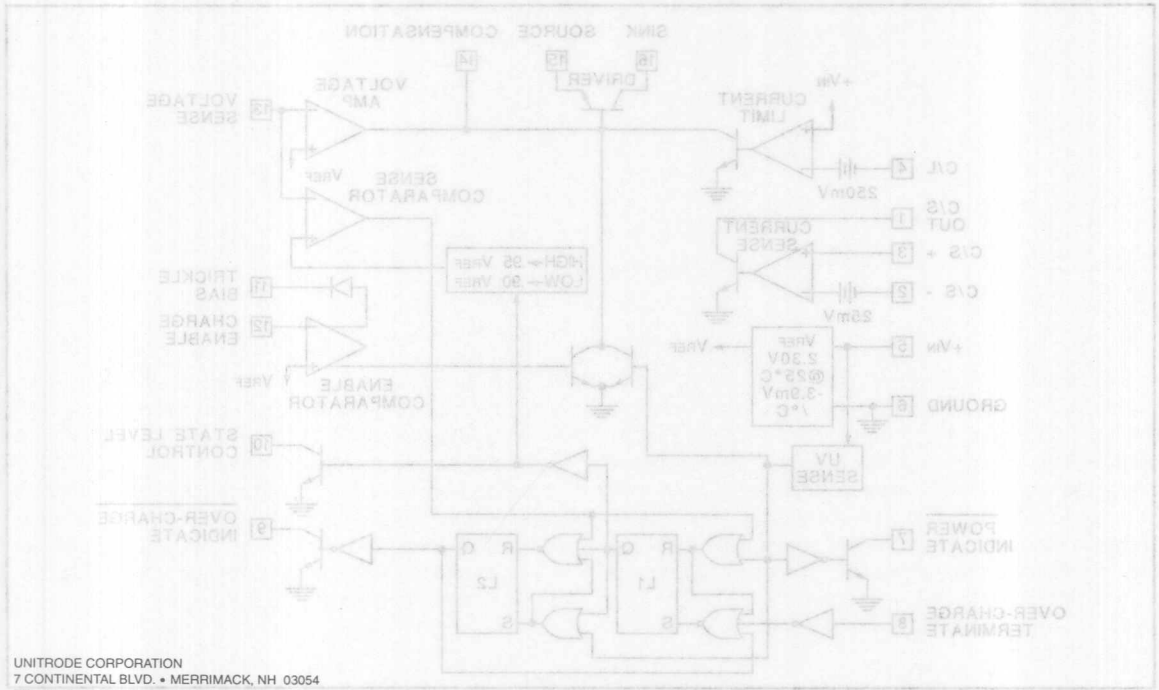


Figure 3



UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

Sealed Lead-Acid Battery Charger

FEATURES

- Optimum Control for Maximum Battery Capacity and Life
- Internal State Logic Provides Three Charge States
- Precision Reference Tracks Battery Requirements Over Temperature
- Controls Both Voltage and Current at Charger Output
- System Interface Functions
- Typical Standby Supply Current of only 1.6mA

DESCRIPTION

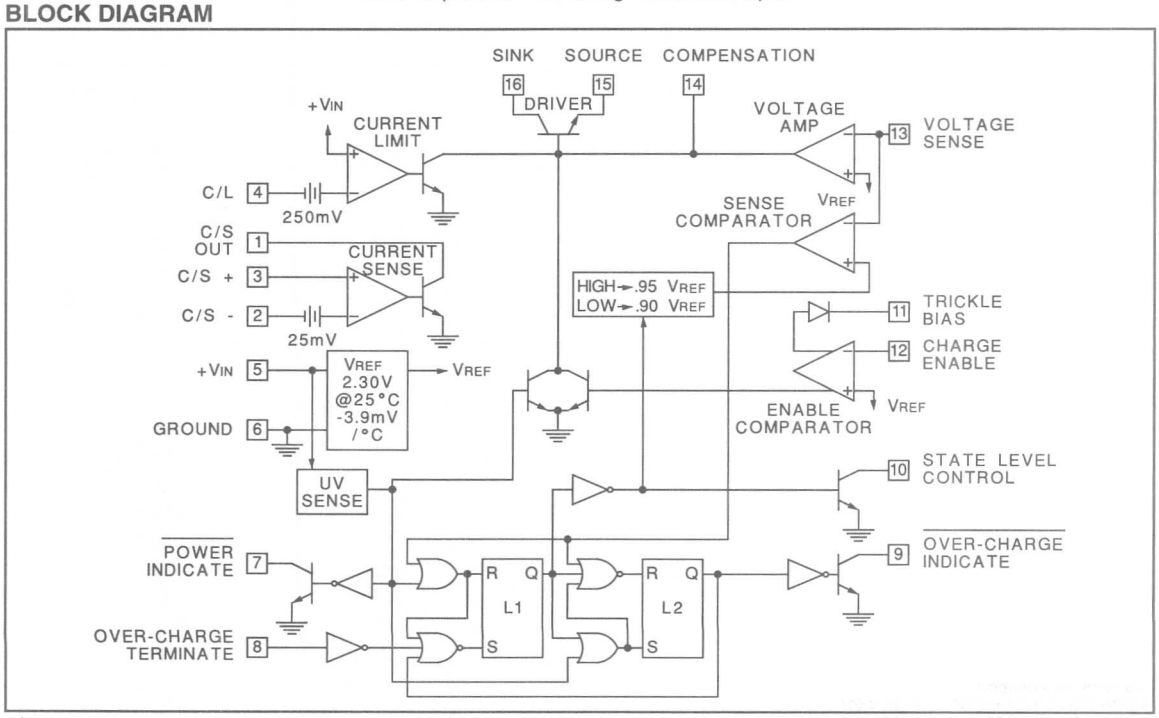
The UC2906 series of battery charger controllers contains all of the necessary circuitry to optimally control the charge and hold cycle for sealed lead-acid batteries. These integrated circuits monitor and control both the output voltage and current of the charger through three separate charge states; a high current bulk-charge state, a controlled over-charge, and a precision float-charge, or standby, state.

Optimum charging conditions are maintained over an extended temperature range with an internal reference that tracks the nominal temperature characteristics of the lead-acid cell. A typical standby supply current requirement of only 1.6mA allows these ICs to predictably monitor ambient temperatures.

Separate voltage loop and current limit amplifiers regulate the output voltage and current levels in the charger by controlling the onboard driver. The driver will supply up to 25mA of base drive to an external pass device. Voltage and current sense comparators are used to sense the battery condition and respond with logic inputs to the charge state logic. A charge enable comparator with a trickle bias output can be used to implement a low current turn-on mode of the charger, preventing high current charging during abnormal conditions such as a shorted battery cell.

Other features include a supply under-voltage sense circuit with a logic output to indicate when input power is present. In addition the over-charge state of the charger can be externally monitored and terminated using the over-charge indicate output and over-charge terminate input.

BLOCK DIAGRAM



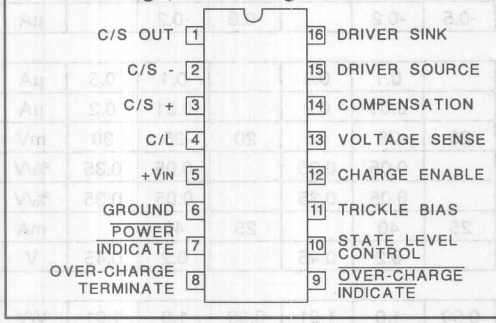
9/96

Amplifier and Comparator Input Voltages . . . -0.3V to +40V
Over-Charge Terminate Input Voltage . . . . . -0.3V to +40V
Current Sense Amplifier Output Current 80mA
Other Open Collector Output Currents. 20mA
Trickle Bias Voltage Differential with respect to VIN. . . -32V
Trickle Bias Output Current . . . . . -40mA
Driver Current. 80mA
Power Dissipation at TA = 25°C(Note 2) 1000mW
Power Dissipation at TC = 25°C (Note 2). 2000mW
Operating Junction Temperature . . . . . -55°C to +150°C
Storage Temperature . . . . . -65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) . . . . . 300°C

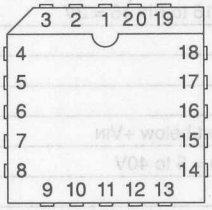
Note 1: Voltages are referenced to ground (Pin 6). Currents are positive into, negative out of, the specified terminals.

Note 2: Consult Packaging section of Databook for thermal limitations and considerations of packages.

DIL-16, SOIC-16 (TOP VIEW)
J or N Package, DW Package



Q, L Packages



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
C/S OUT	2
C/S-	3
C/S+	4
C/L	5
N/C	6
+VIN	7
GROUND	8
POWER INDICATE	9
OVER CHARGE TERMINATE	10
N/C	11
OVER CHARGE INDICATE	12
STATE LEVEL CONTROL	13
TRICKLE BIAS	14
CHARGE ENABLE	15
N/C	16
VOLTAGE SENSE	17
COMPENSATION	18
DRIVER SOURCE	19
DRIVER SINK	20

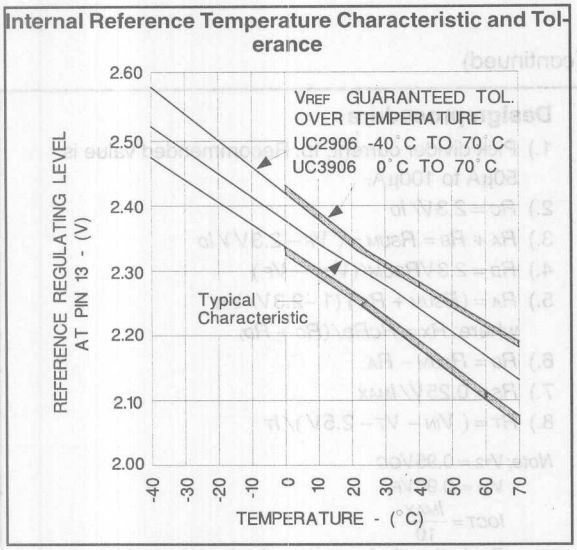
ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for TA = -40°C to +70°C for the UC2906 and 0°C to +70°C for the UC3906, +VIN = 10V, TA = TJ.

PARAMETER	TEST CONDITIONS	UC2906			UC3906			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Supply								
Supply Current	+VIN = 10V		1.6	2.5		1.6	2.5	mA
	+VIN = 40V		1.8	2.7		1.8	2.7	mA
Supply Under-Voltage Threshold	+VIN = Low to High	4.2	4.5	4.8	4.2	4.5	4.8	V
Supply Under-Voltage Hysteresis			0.20	0.30		0.20	0.30	V
Internal Reference (VREF)								
Voltage Level (Note 3)	Measured as Regulating Level at Pin 13 w/ Driver Current = 1mA, TJ = 25°C	2.275	2.3	2.325	2.270	2.3	2.330	V
Line Regulation	+VIN = 5 to 40V		3	8		3	8	mV
Temperature Coefficient			-3.9			-3.9		mV/°C
Voltage Amplifier								
Input Bias Current	Total Input Bias at Regulating Level	-0.5	-0.2		-0.5	-0.2		µA
Maximum Output Current	Source	-45	-30	-15	-45	-30	-15	µA
	Sink	30	60	90	30	60	90	µA
Open Loop Gain	Driver current = 1mA	50	65		50	65		dB
Output Voltage Swing	Volts above GND or below +VIN		0.2			0.2		V

Note 3. The reference voltage will change as a function of power dissipation on the die according to the temperature coefficient of the reference and the thermal resistance, junction-to-ambient.

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = -40°C to +70°C for the UC2906 and 0°C to +70°C for the UC3906, $+V_{IN}$ = 10V, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	UC2906			UC3906			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Driver								
Minimum Supply to Source Differential	Pin 16 = $+V_{IN}$, I_O = 10mA		2.0	2.2		2.0	2.2	V
Maximum Output Current	Pin 16 to Pin 15 = 2V	25	40		25	40		mA
Saturation Voltage			0.2	0.45		0.2	0.45	V
Current Limit Amplifier								
Input Bias Current			0.2	1.0		0.2	1.0	µA
Threshold Voltage	Offset below $+V_{IN}$	225	250	275	225	250	275	mV
Threshold Supply Sensitivity	$+V_{IN}$ = 5 to 40V		0.03	0.25		0.03	0.25	%/V
Voltage Sense Comparator								
Threshold Voltage	As a function of V_{REF}, L_1 = RESET	0.945	0.95	0.955	0.945	0.95	0.955	V/V
	As a function of V_{REF}, L_1 = SET	0.895	0.90	0.905	0.895	0.90	0.905	V/V
Input Bias Current	Total Input Bias at Thresholds	-0.5	-0.2		-0.5	-0.2		µA
Current Sense Comparator								
Input Bias Current			0.1	0.5		0.1	0.5	µA
Input Offset Current			0.01	0.2		0.01	0.2	µA
Input Offset Voltage	Referenced to Pin 2, I_{OUT} = 1mA	20	25	30	20	25	30	mV
Offset Supply Sensitivity	$+V_{IN}$ = 5 to 40V		0.05	0.35		0.05	0.35	%/V
Offset Common Mode Sensitivity	CMV = 2V to $+V_{IN}$		0.05	0.35		0.05	0.35	%/V
Maximum Output Current	V_{OUT} = 2V	25	40		25	40		mA
Output Saturation Voltage	I_{OUT} = 10mA		0.2	0.45		0.2	0.45	V
Enable Comparator								
Threshold Voltage	As a function of V_{REF}	0.99	1.0	1.01	0.99	1.0	1.01	V/V
Input Bias Current		-0.5	-0.2		-0.5	-0.2		µA
Trickle Bias Maximum Output Current	$V_{OUT} = +V_{IN} - 3V$	25	40		25	40		mA
Trickle Bias Maximum Output Voltage	Volts below $+V_{IN}$, I_{OUT} = 10mA		2.0	2.6		2.0	2.6	V
Trickle Bias Reverse Hold-Off Voltage	$+V_{IN}$ = 0V, I_{OUT} = -10µA	6.3	7.0		6.3	7.0		V
Over-Charge Terminate Input								
Threshold Voltage		0.7	1.0	1.3	0.7	1.0	1.3	V
Internal Pull-Up Current	At Threshold		10			10		µA
Open Collector Outputs (Pins 7, 9, and 10)								
Maximum Output Current	V_{OUT} = 2V	2.5	5		2.5	5		mA
Saturation Voltage	I_{OUT} = 1.6mA		0.25	0.45		0.25	0.45	V
	I_{OUT} = 50µA		0.03	0.05		0.03	0.05	V
Leakage Current	V_{OUT} = 40V		1	3		1	3	µA



OPERATION AND APPLICATION INFORMATION

Dual Level Float Charger Operations

The UC2906 is shown configured as a dual level float charger in Figure 1. All high currents are handled by the external PNP pass transistor with the driver supplying base drive to this device. This scheme uses the TRICKLE BIAS output and the charge enable comparator to give the charger a low current turn on mode. The output current of the charger is limited to a low-level until the battery reaches a specified voltage, preventing a high current charging if a battery cell is shorted. Figure 2 shows the state diagram of the charger. Upon turn on the UV sense circuitry puts the charger in state 1, the high rate bulk-charge state. In this state, once the enable threshold has been exceeded, the charger will supply a peak current that is determined by the 250mV offset in the C/L amplifier and the sensing resistor RS.

To guarantee full re-charge of the battery, the charger's voltage loop has an elevated regulating level, VOC, during state 1 and state 2. When the battery voltage reaches 95% of VOC, the charger enters the over-charge state, state 2. The charger stays in this state until the OVER-CHARGE TERMINATE pin goes high. In Figure 1, the charger uses the current sense amplifier to generate this signal by sensing when the charge current has tapered to a specified level, IOCT. Alternatively the over-charge could have been controlled by an external source, such as a timer, by using the OVER-CHARGE INDICATE signal at Pin 9. If a load is applied to the battery and begins to discharge it, the charger will contribute its full output to the load. If the battery drops 10% below the float level, the charger will reset itself to state 1. When the load is removed a full charge cycle will follow. A graphical representation of a charge, and discharge, cycle of the dual lever float charger is shown in Figure 3.

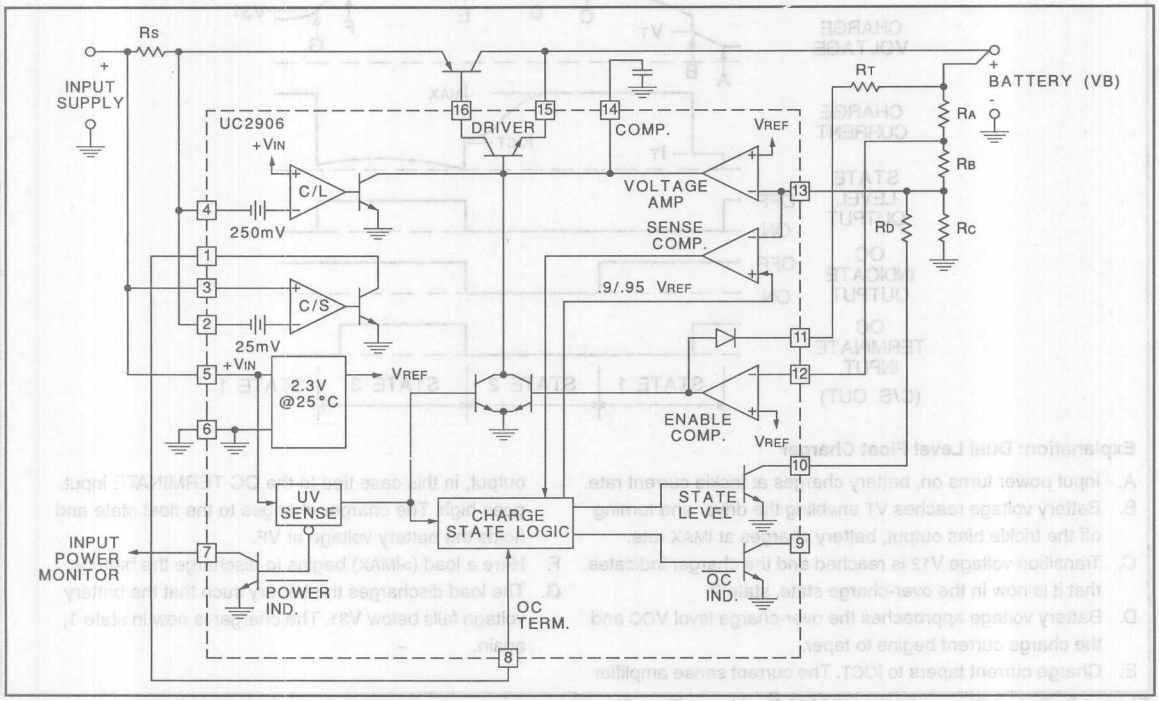
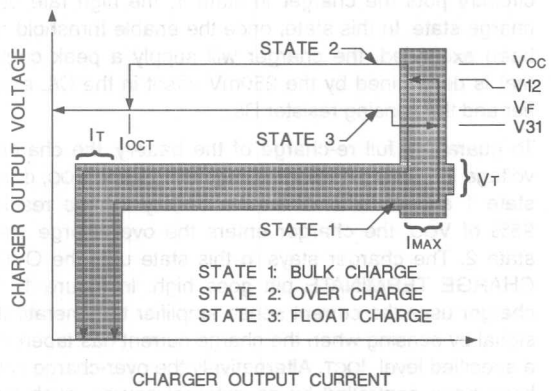


Figure 1. The UC2906 in a Dual Level Float Charger

OPERATION AND APPLICATION INFORMATION (continued)



Design procedure

1.) Pick divider current, I_D. Recommended value is 50μA to 100μA.

2.) $R_C = 2.3V / I_D$

3.) $R_A + R_B = R_{SUM} = (V_F - 2.3V) / I_D$

4.) $R_D = 2.3V R_{SUM} / (V_{OC} - V_F)$

5.) $R_A = (R_{SUM} + R_X)(1 - 2.3V / V_T)$
where: $R_X = R_C R_D / (R_C + R_D)$

6.) $R_B = R_{SUM} - R_A$

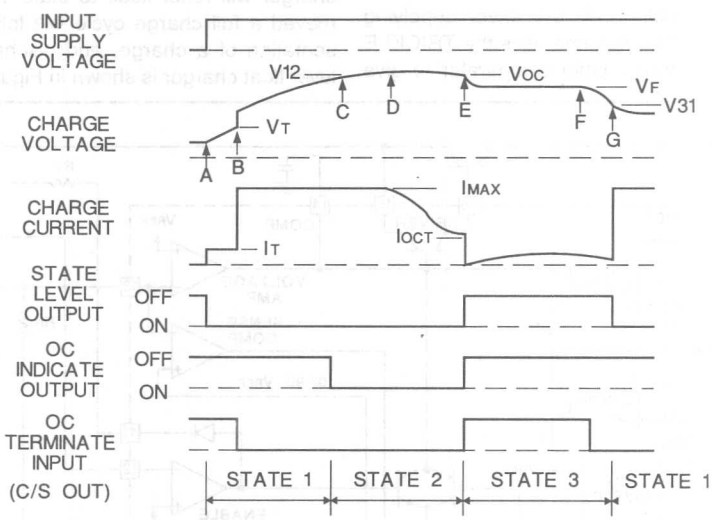
7.) $R_S = 0.25V / I_{MAX}$

8.) $R_T = (V_{IN} - V_T - 2.5V) / I_T$

Note: $V_{12} = 0.95 V_{OC}$
$V_{31} = 0.90 V_F$
$I_{OCT} = \frac{I_{MAX}}{10}$

For further design and application information see UICC Application Note U-104

Figure 2. State Diagram and Design Equations for the Dual Level Float Charger



Explanation: Dual Level Float Charger

A. Input power turns on, battery charges at trickle current rate.

B. Battery voltage reaches VT enabling the driver and turning off the trickle bias output, battery charges at IMAX rate.

C. Transition voltage V12 is reached and the charger indicates that it is now in the over-charge state, state 2.

D. Battery voltage approaches the over-charge level VOC and the charge current begins to taper.

E. Charge current tapers to IOCT. The current sense amplifier output, in this case tied to the OC TERMINATE input, goes high. The charger changes to the float state and holds the battery voltage at VF.

F. Here a load (>IMAX) begins to discharge the battery.

G. The load discharges the battery such that the battery voltage falls below V31. The charger is now in state 1, again.

Figure 3. Typical Charge Cycle: UC2906 Dual Level Float Charger

Compensated Reference Matches Battery Requirements

When the charger is in the float state, the battery will be maintained at a precise float voltage, VF. The accuracy of this float state will maximize the standby life of the battery while the bulk-charge and over-charge states guarantee rapid and full re-charge. All of the voltage thresholds on the UC2906 are derived from the internal reference. This reference has a temperature coefficient that tracks the temperature characteristic of the optimum-charge and hold levels for sealed lead-acid cells. This further guarantees that proper charging occurs, even at temperature extremes.

Dual Step Current Charger Operation

Figures 4, 5 and 6 illustrate the UC2906's use in a different charging scheme. The dual step current charger is useful when a large string of series cells must be charged. The holding-charge state maintains a slightly elevated voltage across the batteries with the holding current, 1H. This will tend to guarantee equal charge distribution between the cells. The bulk-charge state is similar to that of the float charger with the exception that when V12 is reached, no over-charge state occurs since Pin 8 is tied high at all times. The current sense amplifier is used to regulate the holding current. In some applications a series resistor, or external buffering transistor, may be required at the current sense output to prevent excessive power dissipation on the UC2906.

A PNP Pass Device Reduces Minimum Input to Output Differential

The configuration of the driver on the UC2906 allows a good bit of flexibility when interfacing to an external pass transistor. The two chargers shown in Figures 1 and 4 both use PNP pass devices, although an NPN device driven from the source output of the UC2906 driver can also be used. In situations where the charger must operate with low input to output differentials the PNP pass device should be configured as shown in Figure 4. The PNP can be operated in a saturated mode with only the series diode and sense resistor adding to the minimum differential. The series diode, D1, in many applications, can be eliminated. This diode prevents any discharging of the battery, except through the sensing divider, when the charger is attached to the battery with no input supply voltage. If discharging under this condition must be kept to an absolute minimum, the sense divider can be referenced to the POWER INDICATE pin, Pin 7, instead of ground. In this manner the open collector off state of Pin 7 will prevent the divider resistors from discharging the battery when the input supply is removed.

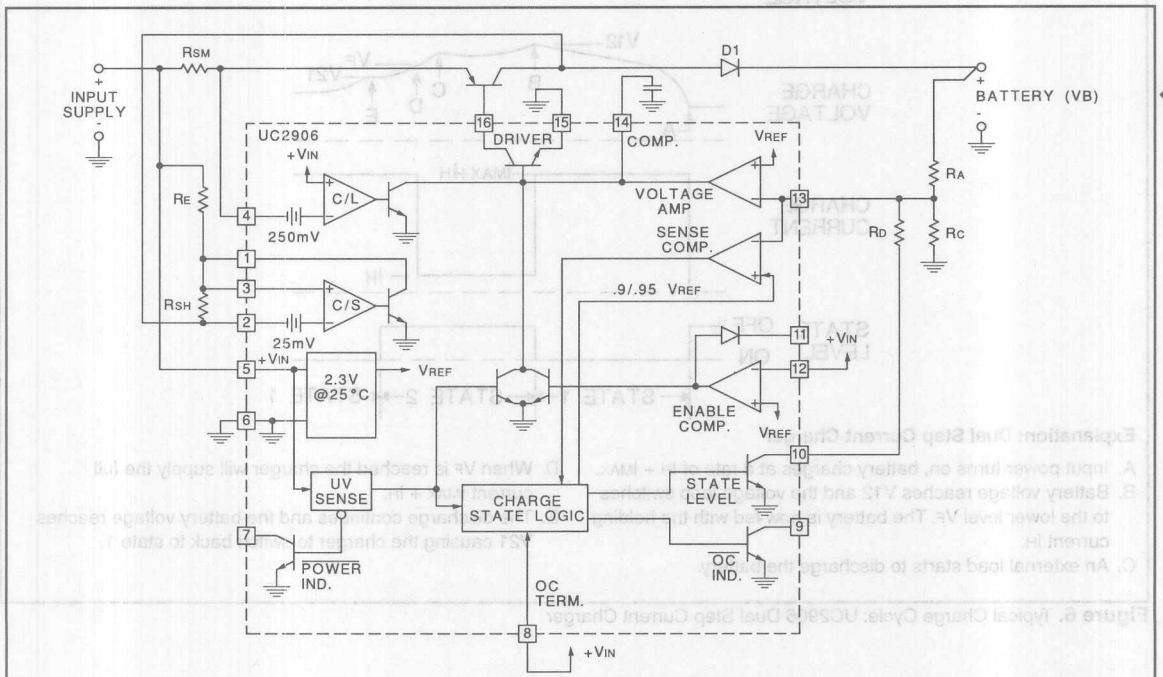


Figure 4. The UC2906 in a Dual Step Current Charger

OPERATION AND APPLICATION INFORMATION (continued)

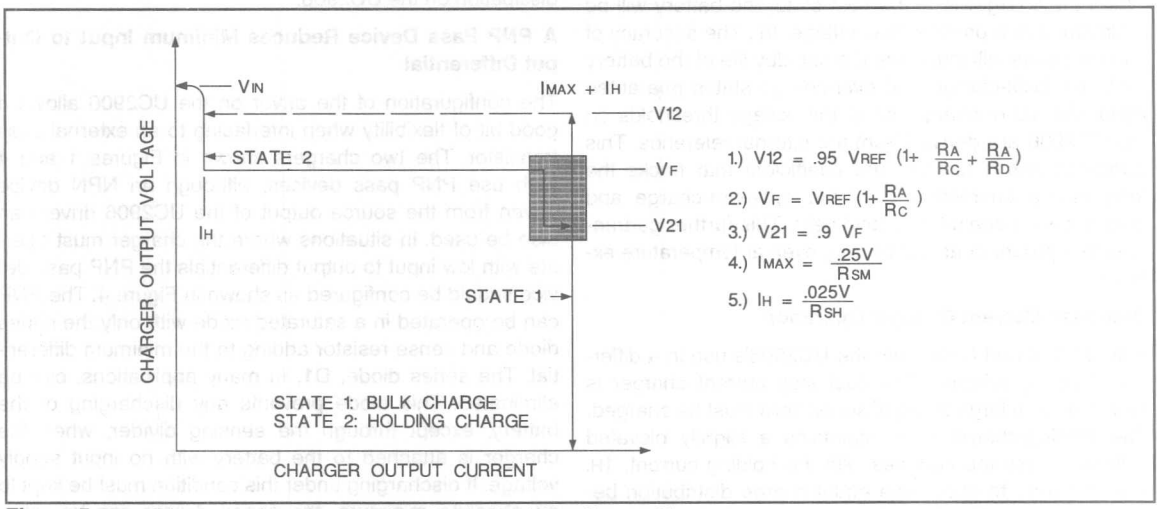
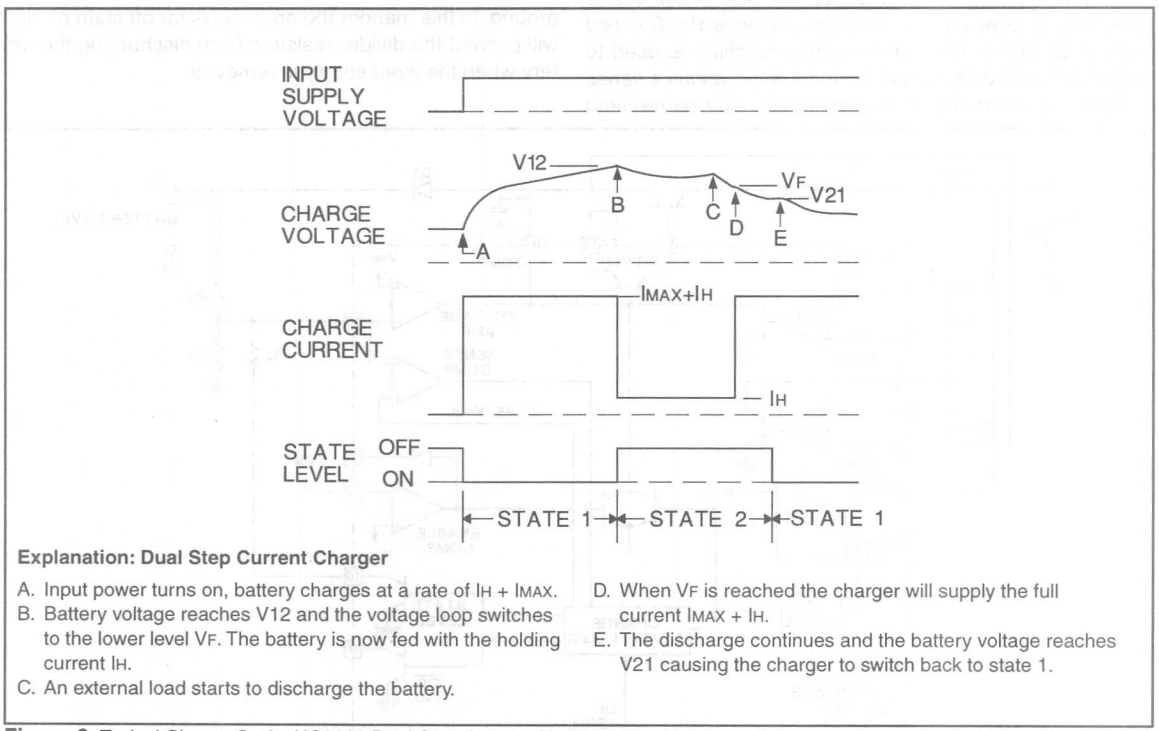


Figure 5. State Diagram and Design Equations for the Dual Step Current Charger



Explanation: Dual Step Current Charger

A. Input power turns on, battery charges at a rate of IH + IMAX.
B. Battery voltage reaches V12 and the voltage loop switches to the lower level VF. The battery is now fed with the holding current IH.
C. An external load starts to discharge the battery.
D. When VF is reached the charger will supply the full current IMAX + IH.
E. The discharge continues and the battery voltage reaches V21 causing the charger to switch back to state 1.

Figure 6. Typical Charge Cycle: UC2906 Dual Step Current Charger

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

Switchmode Lead-Acid Battery Charger

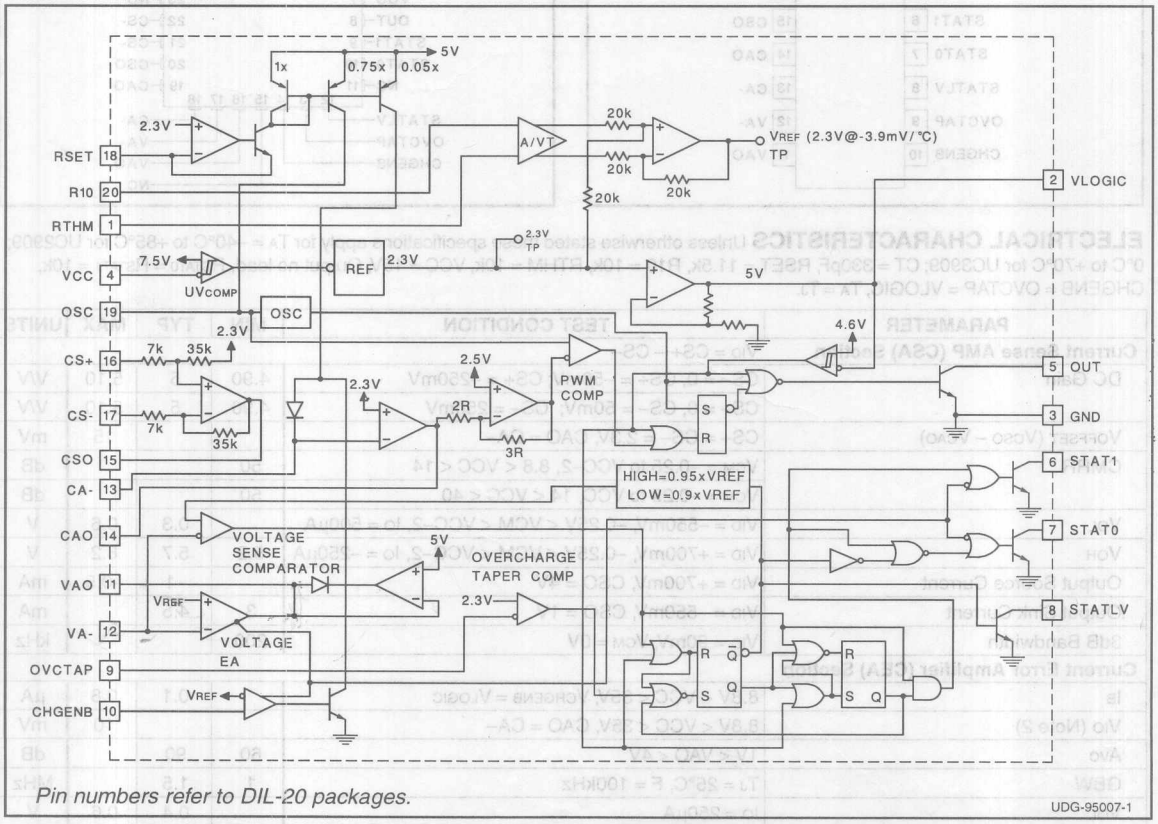
FEATURES

- Accurate and Efficient Control of Battery Charging
- Average Current Mode Control from Trickle to Overcharge
- Resistor Programmable Charge Currents
- Thermistor Interface Tracks Battery Requirements Over Temperature
- Output Status Bits Report on Four Internal Charge States
- Undervoltage Lockout Monitors VCC and VREF

DESCRIPTION

The UC3909 family of Switchmode Lead-Acid Battery Chargers accurately controls lead acid battery charging with a highly efficient average current mode control loop. This chip combines charge state logic with average current PWM control circuitry. Charge state logic commands current or voltage control depending on the charge state. The chip includes undervoltage lockout circuitry to insure sufficient supply voltage is present before output switching starts. Additional circuit blocks include a differential current sense amplifier, a 1.5% voltage reference, a -3.9mV/°C thermistor linearization circuit, voltage and current error amplifiers, a PWM oscillator, a PWM comparator, a PWM latch, charge state decode bits, and a 100mA open collector output driver.

BLOCK DIAGRAM



Pin numbers refer to DIL-20 packages.

UDG-95007-1

PORTABLE PRODUCTS

8

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (VCC), OUT, STAT0, STAT1 . . . . . .40V
Output Current Sink 0.1A
CS+, CS- . . . . . .–0.4 to VCC (Note 1)
Remaining Pin Voltages . . . . . .–0.3V to 9V
Storage Temperature . . . . . .–65°C to +150°C
Junction Temperature . . . . . .–55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . .+300°C

All currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

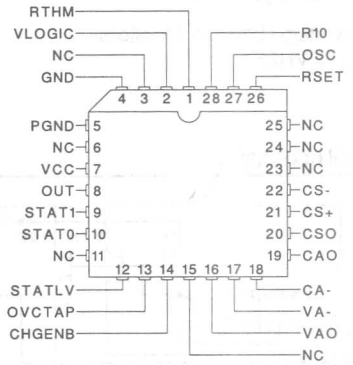
Note 1: Voltages more negative than –0.4V can be tolerated if current is limited to 50mA.

CONNECTION DIAGRAMS

DIL-20, (Top View)
J or N, DW Packages



LCC-28, PLCC-28 (Top View)
L, Q Packages



ELECTRICAL CHARACTERISTICS

Unless otherwise stated these specifications apply for T_A = –40°C to +85°C for UC2909; 0°C to +70°C for UC3909; CT = 330pF, RSET = 11.5k, R10 = 10k, RTHM = 10k, VCC = 15V, Output no load, R_{STAT0} = R_{STAT1} = 10k, CHGENB = OVCTAP = VLOGIC, T_A = T_J.

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
Current Sense AMP (CSA) Section	V_{ID} = CS+ – CS–				
DC Gain	CS– = 0, CS+ = –50mV; CS+ = –250mV	4.90	5	5.10	V/V
	CS+ = 0, CS– = 50mV; CS– = 250mV	4.90	5	5.10	V/V
V_{OFFSET} (V_{CSO} – V_{CAO})	CS+ = CS– = 2.3V, CAO = CA–			15	mV
CMRR	V_{CM} = –0.25 to VCC–2, 8.8 < VCC < 14	50			dB
	V_{CM} = –0.25 to VCC, 14 < VCC < 40	50			dB
V_{OL}	V_{ID} = –550mV, –0.25V < VCM < VCC–2, Io = 500µA		0.3	0.6	V
V_{OH}	V_{ID} = +700mV, –0.25V < VCM < VCC–2, Io = –250µA	5.2	5.7	6.2	V
Output Source Current	V_{ID} = +700mV, CSO = 4V		–1	–0.5	mA
Output Sink Current	V_{ID} = –550mV, CSO = 1V	3	4.5		mA
3dB Bandwidth	V_{ID} = 90mV, V_{CM} = 0V	200			kHz
Current Error Amplifier (CEA) Section					
I_B	8.8V < VCC < 35V, V_{CHGENB} = V_{LOGIC}		0.1	0.8	µA
V_{IO} (Note 2)	8.8V < VCC < 35V, CAO = CA–			10	mV
Avo	1V < VAO < 4V	60	90		dB
GBW	T_J = 25°C, F = 100kHz	1	1.5		MHz
V_{OL}	Io = 250µA		0.4	0.6	V
V_{OH}	Io = –5mA	4.5	5		V

ELECTRICAL CHARACTERISTICS (cont.) Unless otherwise stated these specifications apply for T_A = –40°C to +85°C for UC2909; 0°C to +70°C for UC3909; CT = 330pF, RSET = 11.5k, R10 = 10k, RTHM = 10k, VCC = 15V, Output no load, R_{STAT0} = R_{STAT1} = 10k, CHGENB = OVCTAP = VLOGIC, T_A = T_J.

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
Current Error Amplifier (CEA) Section (cont.)					
Output Source Current	CAO = 4V		–25	–12	mA
Output Sink Current	CAO=1V	2	3		µA
I_{CA-}, $I_{TRCK_CONTROL}$	V_{CHGENB} = GND	8.5	10	11.5	µA
Voltage Error Amplifier (VEA) Section					
I_B	Total Bias Current; Regulating Level		0.1	1	µA
V_{IO} (VAO – V_{REF}) (Note 2)	8.8V < VCC < 35V, VCM = 2.3V, VAO = VA–		1.2		mV
Avo	1V < CAO < 4V	60	90		dB
GBW	T_J = 25°C, F = 100kHz	0.250	0.500		MHz
V_{OL}	Io = 500µA		0.4	0.6	V
V_{OH}	Io = –500µA	4.75	5	5.25	V
Output Source Current	VAO = 4V	–2	–1		mA
Output Sink Current	VAO = 1V	2	2.5		mA
VAO Leakage: High Impedance State	V_{CHGENB} = GND, STAT0 = 0 & STAT1 = 0, VAO = 2.3V	–1		1	µA
Pulse Width Modulator Section					
Maximum Duty Cycle	CAO = 0.6V	90	95	100	%
Modulator Gain	CAO = 2.5V, 3.2V	63	71	80	%/V
OSC Peak			3		V
OSC Valley			1		V
Oscillator Section (OSC)					
Frequency	8.8V < VCC < 35V	198	220	242	kHz
Thermistor Derived Reference Section	V_{ID} = V_{RTHM} – V_{R10}				
Initial Accuracy, VAO (RTHM = 10k)	V_{ID} = 0, R10 = RTHM =10k (Note 3)	2.2655	2.3	2.3345	V
	V_{ID} = 0, R10 = RTHM =10k, –40°C ≤ T_A < 0°C (Note 3)	2.254	2.3	2.346	V
Line Regulation	VCC = 8.8V to 35V		3	10	mV
VAO	RTHM = 138k, R10 = 10k	2.458	2.495	2.532	V
	RTHM = 138k, R10 = 10k, –40°C ≤ T_A < 0°C	2.445	2.495	2.545	V
	RTHM = 33.63k, R10 = 10k	2.362	2.398	2.434	V
	RTHM = 33.63k, R10 = 10k, –40°C ≤ T_A < 0°C	2.350	2.398	2.446	V
	RTHM = 1.014k, R10 = 10k	2.035	2.066	2.097	V
	RTHM = 1.014k, R10 = 10k, –40°C ≤ T_A < 0°C	2.025	2.066	2.107	V
Charge Enable Comparator Section (CEC)					
Threshold Voltage	As a function of VA–	0.99	1	1.01	V/V
Input Bias Current	CHGENB = 2.3V	–0.5	–0.1		µA
Voltage Sense Comparator Section (VSC)					
Threshold Voltage	STAT0 = 0, STAT1 = 0, Function of V_{REF}	0.945	0.95	0.955	V/V
	STAT0 = 1, STAT1 = 0, Function of V_{REF}	0.895	0.9	0.905	V/V
Over Charge Taper Current Comparator Section (OCTIC)					
Threshold Voltage	Function of 2.3V REF, CA– = CAO	0.99	1	1.01	V/V
Input Bias Current	OVCTAP = 2.3V	–0.5	–0.1		µA
Logic 5V Reference Section (VLOGIC)					
VLOGIC	VCC = 15V	4.875	5.0	5.125	V
Line Regulation	8.8V < VCC < 35V		3	15	mV
Load Regulation	0 < Io < 10mA		3	15	mV
Reference Comparator Turn-on Threshold			4.3	4.8	V
Short Circuit Current	V_{REF} = 0V	30	50	80	mA

ELECTRICAL CHARACTERISTICS (cont.) Unless otherwise stated these specifications apply for T_A = –40°C to +85°C for UC2909; 0°C to +70°C for UC3909; CT = 330pF, RSET = 11.5k, R10 = 10k, RTHM = 10k, VCC = 15V, Output no load, R_{STAT0} = R_{STAT1} = 10k, CHGENB = OVCTAP = VLOGIC, T_A = T_J.

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
Output Stage Section					
I_{SINK} Continuous			50		mA
I_{PEAK}			100		mA
V_{OL}	Io = 50mA		1	1.3	V
Leakage Current	V_{OUT} = 35V			25	µA
STAT0 & STAT1 Open Collector Outputs Section					
Maximum Sink Current	V_{OUT} = 8.8V	6	10		mA
Saturation Voltage	I_{OUT} = 5mA		0.1	0.45	V
Leakage Current	V_{OUT} = 35V			25	µA
STATLV Open Collector Outputs Section					
Maximum Sink Current	V_{OUT} = 5V	2.5	5		mA
Saturation Voltage	I_{OUT} = 2mA		0.1	0.45	V
Leakage current	V_{OUT} = 5V			3	µA
UVLO Section					
Turn-on Threshold		6.8	7.8	8.8	V
Hysteresis		100	300	500	mV
Icc Section					
Icc (run)	See Graph, typical temperature variation of ICC		13	19	mA
Icc (off)	VCC = 6.5V		2		mA

Note 2: VIO is measured prior to packaging with internal probe pad.
Note 3: Thermistor initial accuracy is measured and trimmed with respect to VAO; VAO = VA-.

PIN DESCRIPTIONS

CA-: The inverting input to the current error amplifier.

CAO: The output of the current error amplifier which is internally clamped to approximately 4V. It is internally connected to the inverting input of the PWM comparator.

CS-, CS+: The inverting and non-inverting inputs to the current sense amplifier. This amplifier has a fixed gain of five and a common-mode voltage range of from –250mV to +VCC.

CSO: The output of the current sense amplifier which is internally clamped to approximately 5.7V.

CHGENB: The input to a comparator that detects when battery voltage is low and places the charger in a trickle charge state. The charge enable comparator makes the output of the voltage error amplifier a high impedance while forcing a fixed 10µA into CA- to set the trickle charge current.

GND: The reference point for the internal reference, all thresholds, and the return for the remainder of the device. The output sink transistor is wired directly to this pin.

OVCTAP: The overcharge current taper pin detects when the output current has tapered to the float threshold in the overcharge state.

OSC: The oscillator ramp pin which has a capacitor (C_T) to ground. The ramp oscillates between approximately 1.0V to 3.0V and the frequency is approximated by:

$$\text{frequency} \approx \frac{1}{1.2 \bullet C_T \bullet \text{RSET}}$$

OUT: The output of the PWM driver which consists of an open collector output transistor with 100mA sink capability.

R10: Input used to establish a differential voltage corresponding to the temperature of the thermistor. Connect a 10k resistor to ground from this point.

RSET: A resistor to ground programs the oscillator charge current and the trickle control current for the oscillator ramp.

The oscillator charge current is approximately

$$\frac{1.75}{\text{RSET}}.$$

The trickle control current ($I_{TRCK_CONTROL}$) is approximately

$$\frac{0.115}{\text{RSET}}.$$

RTHM: A 10k thermistor is connected to ground and is thermally connected to the battery. The resistance will vary exponentially over temperature and its change is used to vary the internal 2.3V reference by -3.9mV/°C. The recommended thermistor for this function is part number L1005-5744-103-D1, Keystone Carbon Company, St. Marys, PA.

STAT0: This open collector pin is the first decode bit used to decode the charge states.

STAT1: This open collector pin is the second decode bit used to decode the charge states.

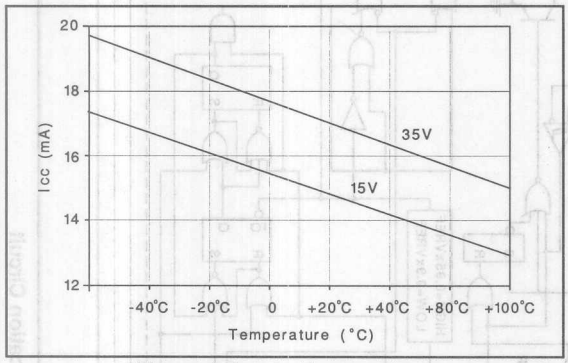


Figure 1. Icc vs. Temperature

STATLV: This bit is high when the charger is in the float state.

VA-: The inverting input to the voltage error amplifier.

VAO: The output of the voltage error amplifier. The upper output clamp voltage of this amplifier is 5V.

VCC: The input voltage to the chip. The chip is operational between 7.5V and 40V and should be bypassed with a 1µF capacitor. A typical Icc vs. temperature is shown in Figure 1.

VLOGIC: The precision reference voltage. It should be bypassed with a 0.1µF capacitor.

Charge State Decode Chart:

STAT0 and STAT1 are open collector outputs. The output is approximately 0.2V for a logic 0.

	STAT1	STAT0
Trickle Charge	0	0
Bulk Charge	0	1
Over Charge	1	0
Float Charge	1	1

APPLICATION INFORMATION

A Block Diagram of the UC3909 is shown on the first page, while a Typical Application Circuit is shown in Figure 2. The circuit in Figure 2 requires a DC input voltage between 12V and 40V.

The UC3909 uses a voltage control loop with average current limiting to precisely control the charge rate of a lead-acid battery. The small increase in complexity of average current limiting is offset by the relative simplicity of the control loop design.

CONTROL LOOP:

Current Sense Amplifier:

This amplifier measures the voltage across the sense resistor RS with a fixed gain of five and an offset voltage of 2.3V. This voltage is proportional to the battery current. The most positive voltage end of RS is connected to CS- ensuring the correct polarity going into the PWM comparator.

CSO = 2.3V when there is zero battery current.

RS is chosen by dividing 350mV by the maximum allowable load current. A smaller value for RS can be chosen to reduce power dissipation.

Maximum Charge Current, I_{BULK}, is set by knowing the maximum voltage error amplifier output, V_{OH} = 5V, the maximum allowable drop across RS, and setting the resistors RG1 and RG2 such that;

$$(1)\ \frac{RG1}{RG2} = \frac{5 \bullet V_{RS}}{VLOGIC - CA-} = \frac{5 \bullet V_{RS}}{5V - 2.3V}$$

$$= \frac{5 \bullet V_{RS}}{2.7V} = 1.852 \bullet I_{BULK} \bullet RS$$

The maximum allowable drop across RS is specified to limit the maximum swing at CSO to approximately 2.0V to keep the CSO amplifier output from saturating.

No charge/load current: V_{CSO} = 2.3V,

Max charge/load current: V_{MAX}(CSO) = 2.3V - 2.0V
0.3V

Voltage Error Amplifier:

The voltage error amplifier (VEA) senses the b
voltage and compares it to the 2.3V – 3.9mV/°C the
tor generated reference. Its output becomes the cu

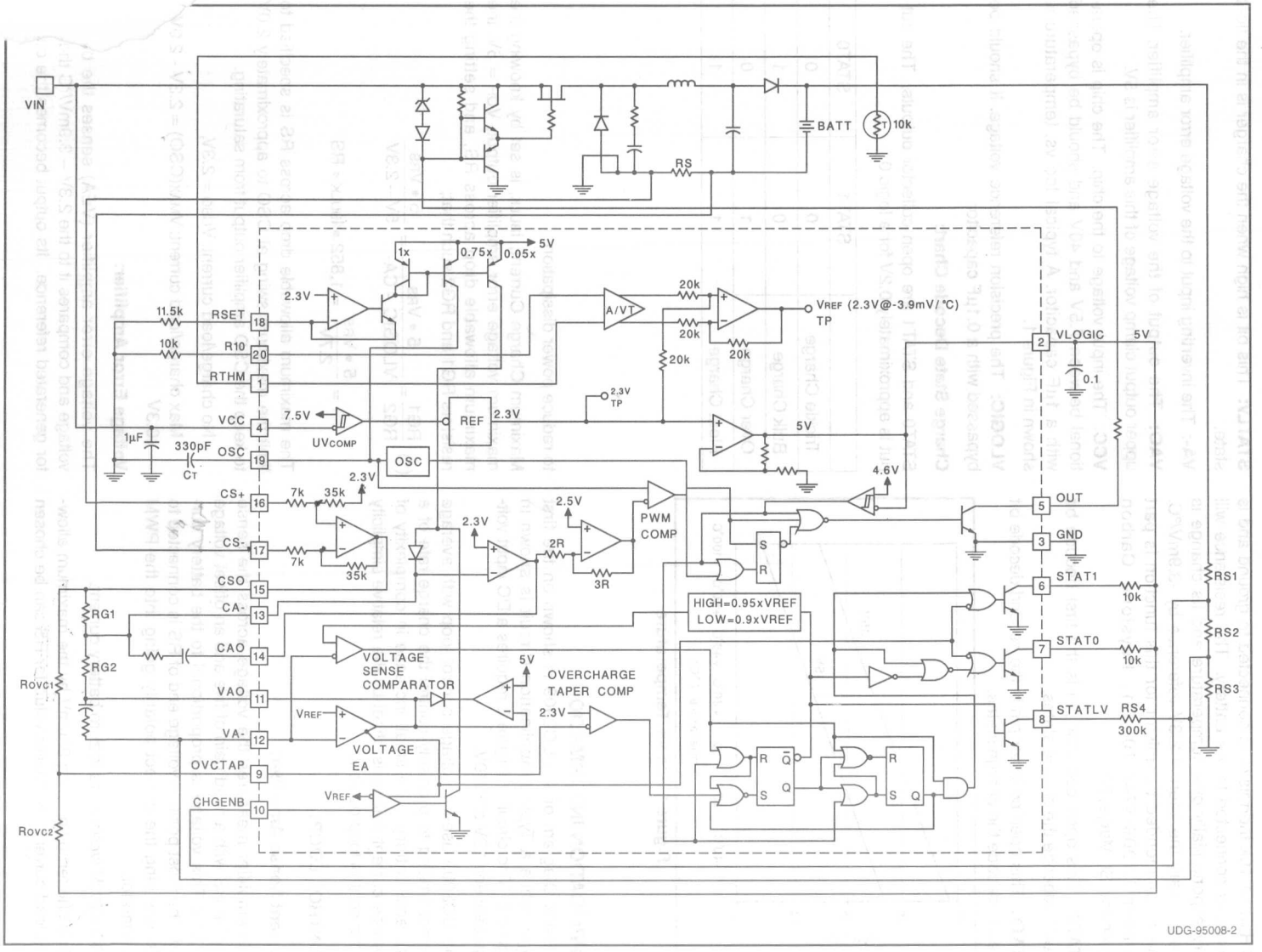


Figure 2. Typical Application Circuit

command signal and is summed with the current sense amplifier output. A 5.0V voltage error amplifier upper clamp limits maximum load current. During the trickle charge state, the voltage amplifier output is opened (high impedance output) by the charge enable comparator. A trickle bias current is summed into the CA- input which sets the maximum trickle charge current.

The VEA, V_{OH} = 5V clamp saturates the voltage loop and consequently limits the charge current as stated in Equation 1.

During the trickle bias state the maximum allowable charge current (ITC) is similarly determined:

$$(2)\ ITC = \frac{I_{TRCK_CONTROL} \bullet RG1}{RS \bullet 5}$$

$I_{TRCK_CONTROL}$ is the fixed control current into CA-. $I_{TRCK_CONTROL}$ is 10µA when RSET = 11.5k. See RSET pin description for equation.

Current Error Amplifier:

The current error amplifier (CA) compares the output of the current sense amplifier to the output of the voltage error amplifier. The output of the CA forces a PWM duty cycle which results in the correct average battery current. With integral compensation, the CA will have a very high DC current gain, resulting in effectively no average DC current error. For stability purposes, the high frequency gain of the CA must be designed such that the magnitude of the down slope of the CA output signal is less than or equal to the magnitude of the up slope of the PWM ramp.

CHARGE ALGORITHM

Refer to Figure 3 in UC3906 Data Sheet in the data book.

A) Trickle Charge State
STAT0 = STAT1 = STATLV = logic 0

When CHGNB is less than VREF (2.3V – 3.9mV/°C), STATLV is forced low. This decreases the sense voltage divider ratio, forcing the battery to overcharge (VOC).

$$(3)\ VOC = (VREF)\ \frac{(RS1 + RS2 + RS3\ ||\ RS4)}{(RS3\ ||\ RS4)}$$

During the trickle charge state, the output of the voltage error amplifier is high impedance. The trickle control current is directed into the CA- pin setting the maximum trickle charge current. The trickle charge current is defined in Equation 2.

B) Bulk Charge State
STAT1 = STATLV = logic 0, STAT0 = logic 1

As the battery charges, the UC3909 will transition from trickle to bulk charge when CHGENB becomes greater than 2.3V. The transition equation is

$$V_T = V_{REF} \bullet \frac{(RS1 + RS2 + RS3\ ||\ RS4)}{(RS2 + RS3\ ||\ RS4)}$$

STATLV is still driven low.

During the bulk charge state, the voltage error amplifier is now operational and is commanding maximum charge current (I_{BULK}) set by Equation 1. The voltage loop attempts to force the battery to VOC.

C) Overcharge State
STAT0 = STATLV = logic 0, STAT1 = logic 1

The battery voltage surpasses 95% of VOC indicating the UC3909 is in its overcharge state.

During the overcharge charge state, the voltage loop becomes stable and the charge current begins to taper off. As the charge current tapers off, the voltage at CSO increases toward its null point of 2.3V. The center connection of the two resistors between CSO and VLOGIC sets the overcurrent taper threshold (OVCTAP). Knowing the desired overcharge terminate current (I_{OCT}), the resistors R_{OVC1} and R_{OVC2} can be calculated by choosing a value of R_{OVC2} and using the following equation:

$$(4)\ R_{OVC1} = (1.8518) \bullet I_{OCT} \bullet RS \bullet R_{OVC2}$$

D) Float State
STAT0 = STAT1 = STATLV = logic 1

The battery charge current tapers below its OVCTAP threshold, and forces STATLV high increasing the voltage sense divider ratio. The voltage loop now forces the battery charger to regulate at its float state voltage (V_F).

$$(5)\ V_F = (V_{REF})\ \frac{(RS1 + RS2 + RS3)}{RS3}$$

If the load drains the battery to less than 90% of V_F, the charger goes back to the bulk charge state, STATE 1.

OFF LINE APPLICATIONS

For off line charge applications, either Figure 3 or Figure 4 can be used as a baseline. Figure 3 has the advantage of high frequency operation resulting in a small isolation transformer. Figure 4 is a simpler design, but at the expense of larger magnetics.

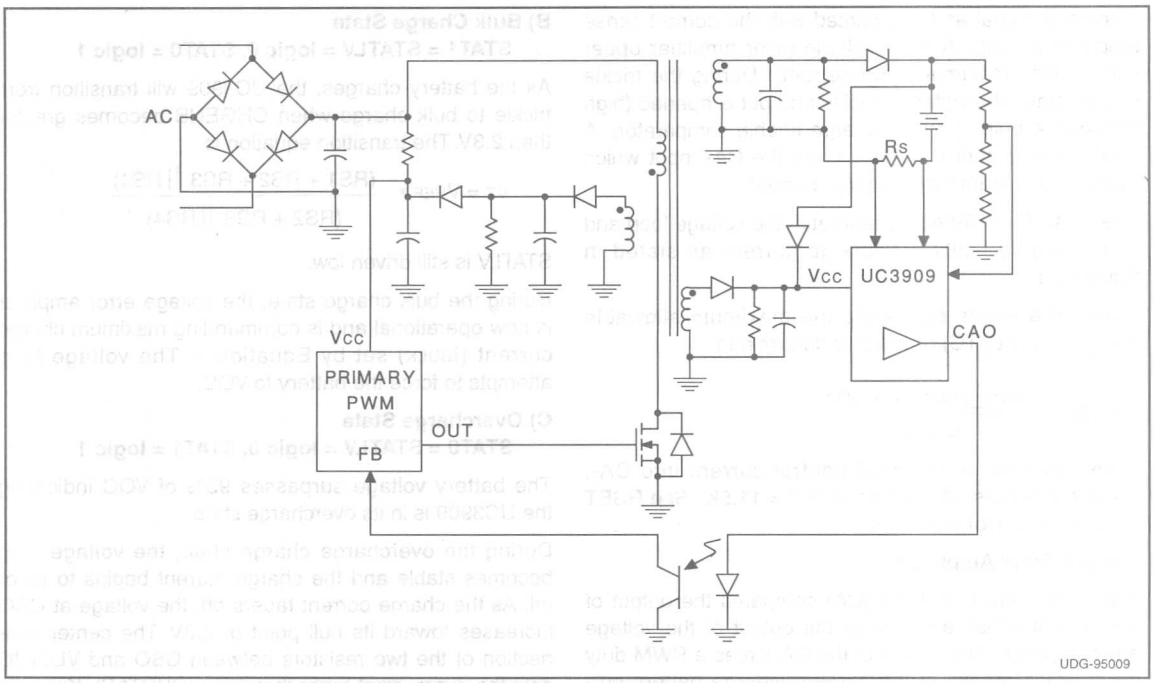


Figure 3. Off Line Charger with Primary Side PWM

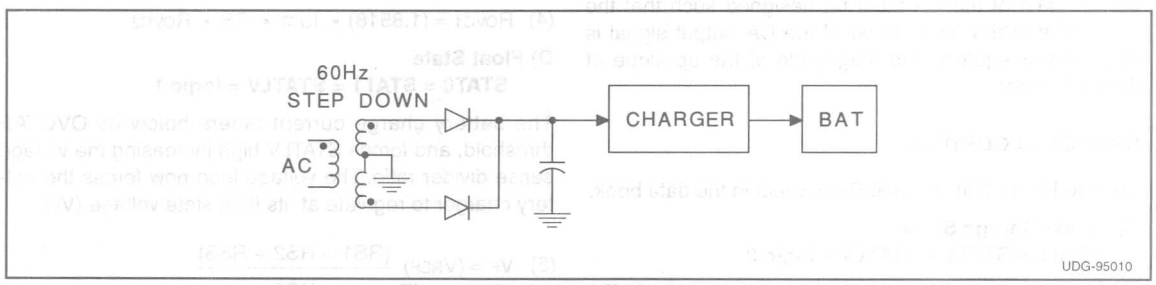


Figure 4. Isolated Off Line Charger

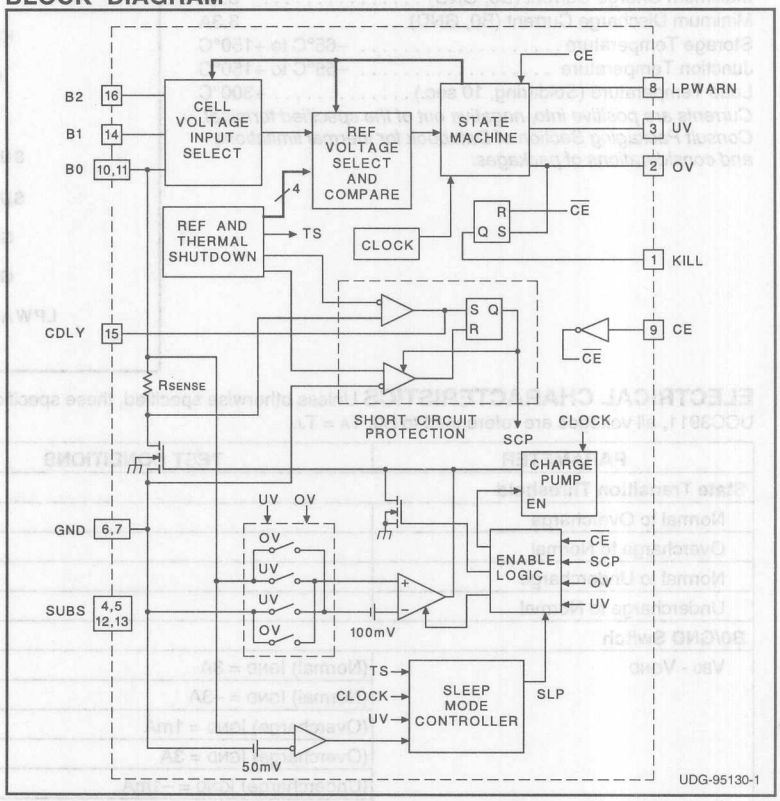
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Lithium-Ion Battery Protector

FEATURES

- Protects Sensitive Lithium-Ion Cells from Overcharging and Over-Discharging
- Used for Two-Cell Lithium-Ion Battery Packs
- No External FET Required
- Provides Protection Against Battery Pack Output Short Circuit
- Extremely Low Power Drain on Batteries of About 20µA
- Internal FET Switch Voltage Drop
- User Controllable Delay for Tripping Short Circuit Current Protector
- 3A Current Capacity
- No External Components Required (External Delay Capacitor Optional)

BLOCK DIAGRAM



DESCRIPTION

The UCC3911 is a two-cell lithium-ion battery pack protector IC that incorporates an on-chip series FET switch thus reducing manufacturing costs and increasing reliability. The IC's primary function is to protect both lithium-ion cells in a two-cell battery pack from being either overcharged or over-discharged. It employs a precision bandgap voltage reference that is used to detect when either cell is approaching an overcharged or over-discharged state. When on board logic detects either condition, the series FET switch opens to protect the cells.

A negative feedback loop controls the FET switch when the battery pack is in either the overcharged or over-discharged state. In the overcharged state the action of the feedback loop is to allow only discharge current to pass through the FET switch. In the over-discharged state, only charging current is allowed to flow. The op amp that drives the loop is powered only when in one of these two states. In the over-discharged state the chip enters sleep mode until it senses that the pack is being charged.

The FET switch is driven by a charge pump when the battery pack is in a normally charged state to achieve the lowest possible $R_{DS(ON)}$. In this state the negative feedback loop's op amp is powered down to conserve battery power. Short circuit protection for the battery pack is provided and has a nominal delay of 100µs before tripping. An external capacitor may be connected between CDLY and B0 to increase this delay time to allow longer overcurrent transients.

A chip enable (CE) pin is provided that while held low, inhibits normal operation of the chip to facilitate assembly of the battery pack.

The UCC3911 is specified for operation over the temperature range of –20°C to +70°C, the typical operating and storage temperature range of lithium-ion batteries.

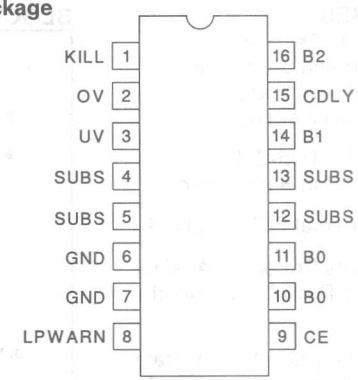
ABSOLUTE MAXIMUM RATINGS

Maximum Input Voltage (B2, GND) 14V
Minimum Input Voltage (B0, GND). . . . . –9.0V
Maximum Charge Current (B0, GND) 3.3A
Minimum Discharge Current (B0, GND). 3.3A
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

SOIC-16 (Top View)
DP Package



ELECTRICAL CHARACTERISTICS

Unless otherwise specified, these specifications apply for –20°C to +70°C for UCC3911, all voltages are referenced to B0, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
State Transition Threshold					
Normal to Overcharge		4.20	4.25	4.30	V
Overcharge to Normal		3.65	3.75	3.85	V
Normal to Undercharge		2.45	2.5	2.55	V
Undercharge to Normal		2.90	3.0	3.10	V
B0/GND Switch					
V_{B0} - V_{GND}	(Normal) I_{GND} = 3A	–500	–290		mV
	(Normal) I_{GND} = –3A		290	500	mV
	(Overcharge) I_{GND} = 1mA		–150		mV
	(Overcharge) I_{GND} = 3A		–450		mV
	(Undercharge) I_{GND} = –1mA		150		mV
	(Undercharge) I_{GND} = –3A		450		mV
I_{GND}	(Overcharge) V_{B0} = 8V	–5	0		µA
	(Undercharge) V_{B0} = –8V		0	5	µA
	(Overcharge) V_{B0} = 8V at T = 25°C		0		µA
	(Undercharge) V_{B0} = –8V at T = 25°C		0		µA
Chip Bias Current					
I_{B2}	Nominal		18	25	µA
I_{B2}	In Sleep Mode		3.5		µA
I_{B1}		–5	0	5	µA
Short Circuit Protection					
$I_{THRESHOLD}$		3.5	5.25	7	A
T_{DLY}	CDLY = Open (Note 1)		100		µs
Internal Clock Frequency	(Note 2)		7.5		kHz
T_{DLY} - OV	Delay for Chip to Register OV Condition (Note 1)		1.25	5	ms
T_{DLY} - UV	Delay for Chip to Register UV Condition (Note 1)		0.75	3.5	ms
OV, UV Output Characteristics	V_{DD} - V_{HIGH} with I_{PIN} = –1000µA			1.07	V
	V_{LOW} With I_{PIN} = 100µA			0.426	V
KILL Output Characteristics	V_{DD} - V_{HIGH} With I_{KILL} = –0.5mA			0.285	V

ELECTRICAL CHARACTERISTICS (cont.) Unless otherwise specified, these specifications apply for –20°C to +70°C for UCC3911, all voltages are referenced to B0, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Short Circuit Protection (cont.)					
KILL Output Characteristics	V_{LOW} With I_{KILL} = 0.5mA			0.265	V
LPWARN Output Characteristics	V_{DD} - V_{HIGH} With I_{LPWARN} = –0.3mA			0.413	V
	V_{LOW} With I_{LPWARN} = 0.3mA			0.361	V
CE Threshold Voltage	V_{DD} = 8.5V	3.2	4.2	5.2	V
	V_{DD} = 5V	2.05	2.45	4.05	V

Note 1: Guaranteed by design. Not 100% tested in production.
Note 2: Tested at functional probe only.

PIN DESCRIPTIONS

B0: Connects to the negative terminal of the lower cell in the battery pack.

B1: Connects to the junction of the positive terminal of the lower cell and the negative terminal of the upper cell in the battery pack.

B2: Connects to the positive terminal of the upper cell in the battery pack. This pin also connects to the positive of the two terminals that are presented to the user of the battery pack.

CDLY: Delay control pin for the short circuit protection feature. A capacitor connected between this pin and the B0 pin will lengthen the time delay from when an overcurrent situation is detected to when the protection circuitry is activated. This control will be useful for those applications where high peak load currents may momentarily exceed the protection circuit's threshold current and interruption of the battery current would be undesirable. The nominal delay time is internally set at 100µs. The equation for determining this delay is:

$$T_{DLY} \approx 25\mu s + (5 \bullet 10^{-5}) \bullet (25pF + CDLY) \bullet V_{DD}$$

To recover from an overcurrent "shutdown" the load must be removed momentarily from the pack.

CE: Chip Enable. While this signal is held low, the internal state of the state machine is held at 00 (or nominal) and the KILL latch is held in reset. CE is pulled high by a 2µA current source. This function was included to facilitate construction of the battery pack by preventing the KILL latch from being erroneously set during final assembly. The last step in the electrical assembly of the pack would be the cutting of a ground link holding this pin low.

GND: The second of the two terminals that are presented to the user of the battery pack. The internal FET switch connects this terminal to the B0 terminal to give the battery pack user appropriate access to the batteries. In an overcharged state, current is allowed to flow only into this terminal. Similarly, in an over-discharged state, current is allowed to flow only out of this terminal.

KILL: This active-high signal indicates that one or both of the cells has been overcharged. It can be used to drive a circuit breaker of some sort to permanently disable the battery pack as a safety feature. Note that when KILL goes active the chip simultaneously enters the OV state which inhibits further charging of the pack. The KILL latch is asynchronously reset by the CE signal.

LPWARN: This active-high signal is the low Power Warning. The voltage on this pin goes high (to B2 potential) as soon as either of the battery's cells voltage falls below 3.0V. Once the UV state is entered, this output goes back to low.

OV: This active-low signal indicates the state of the state machine's OV bit. When low, it indicates that one or both cells are overcharged. Further charging is inhibited by the opening of the FET switch. The internal signal also sets the KILL latch and activates the KILL output signal. The output buffer for this pin is sized to drive a very light load.

SUBS: The substrate connections for the UCC3911. Connect these points to a heat sink which is electrically isolated from all other IC pins.

UV: This active-low signal indicates the state of the state machine's UV bit. When low, it indicates that one or both cells are over- discharged. Further discharging is inhibited by the opening of the FET switch. The chip enters the "Sleep" mode when UV goes high and waits in this state until the chip detects that the battery pack has been placed in a charging circuit. The output buffer for this pin is likewise sized to drive a very light load.

APPLICATION INFORMATION

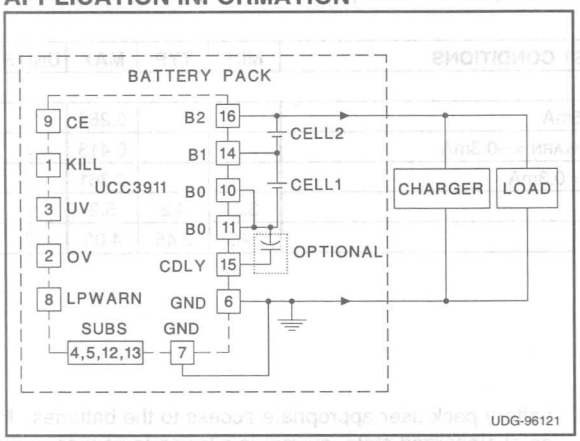
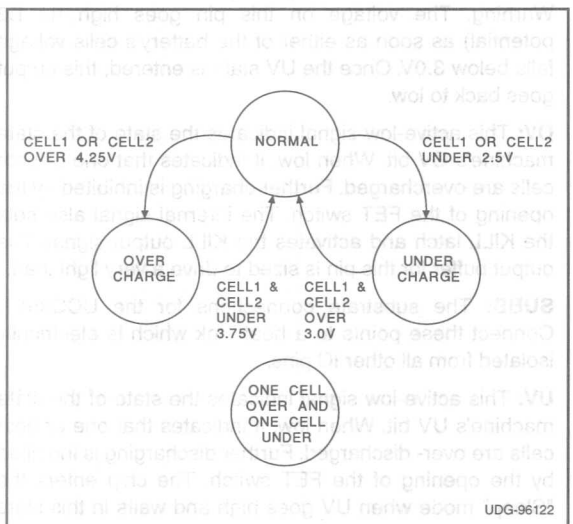


Figure 1. Sample Application Diagram

Figure 1 shows a typical application for the UCC3911 lithium-ion battery protector. All of the functions required to protect two series lithium-ion cells from overcharge and over-discharge, as well as provide short circuit protection, are included in a single chip. An internal state machine controls an internal power FET which allows either bi-directional or uni-directional battery current. An optional time delay capacitor can be included to slow the reaction time of the short circuit protection circuitry if desired.



Note: The "One Cell Over and One Cell Under" state is entered whenever one cell is overcharged and the other cell is simultaneously over-discharged. When in this state, the series FET switch is turned off inhibiting both charging and discharging of the battery pack. If the battery pack ever gets into this condition, it should be discarded.

Figure 2. State Diagram

The internal state machine constantly monitors the two cells for both overvoltage and undervoltage conditions. Figure 2 shows a state diagram which describes the operation of the protection circuitry. In the normal mode, both the OV and UV status bits are held high and full battery current is allowed through the internal power FET in either the charge or discharge direction.

If the voltage across one or both cells exceeds 4.25V, the OV signal goes low, and further charge current is not allowed. An internal feedback loop controls the power FET to allow only discharge current, allowing for battery recovery. The state machine will not reenter normal mode until the voltage across both cells decays to less than 3.75V. This feature is important to prevent circuit oscillation due to battery ESR when the circuitry transitions between states. The KILL output signal is also set high when the UCC3911 enters the OV state, and will remain set unless the CE pin is brought low. The KILL latch can be used to permanently disable the battery pack with additional circuitry if desired.

If the voltage across one or both battery cells falls below 3.0V, the LPWARN signal goes high indicating a low power condition. This signal can be used to signal the user that the battery pack is in need of charge.

If the voltage across one or both cells falls below 2.5V, the UV signal goes low, and a different feedback loop allows only charge current. The LPWARN signal goes low and the UCC3911 enters sleep mode which consumes only 3µA, limiting self discharge to a minimum. The circuit remains in this state until the voltage across both cells exceeds 3.0V. The battery pack can still be charged, unless the sum of the two cells voltages falls below 3.7V, which is the maximum guaranteed operating voltage for the IC.

If the battery cells become so poorly matched that the voltage across one cell exceeds 4.25V and the voltage across the other cell falls below 2.5V, the power FET will not allow either charge or discharge current, and both the OV and UV signals will be set high. The battery pack can not recover from this condition and should be discarded.

The normal high current path for battery current is through the B0 (10, 11) and GND (6, 7) pins of the UCC3911. The GND pins are intended to be connected to system ground for either the charger or the load. The SUBS pins (4, 5, 12, 13) are internally connected to the substrate of the UCC3911, which may be referenced to B0 or GND depending on the direction of pack current. If high battery currents are anticipated, the SUBS pins can be thermally connected to a heat sink to control the

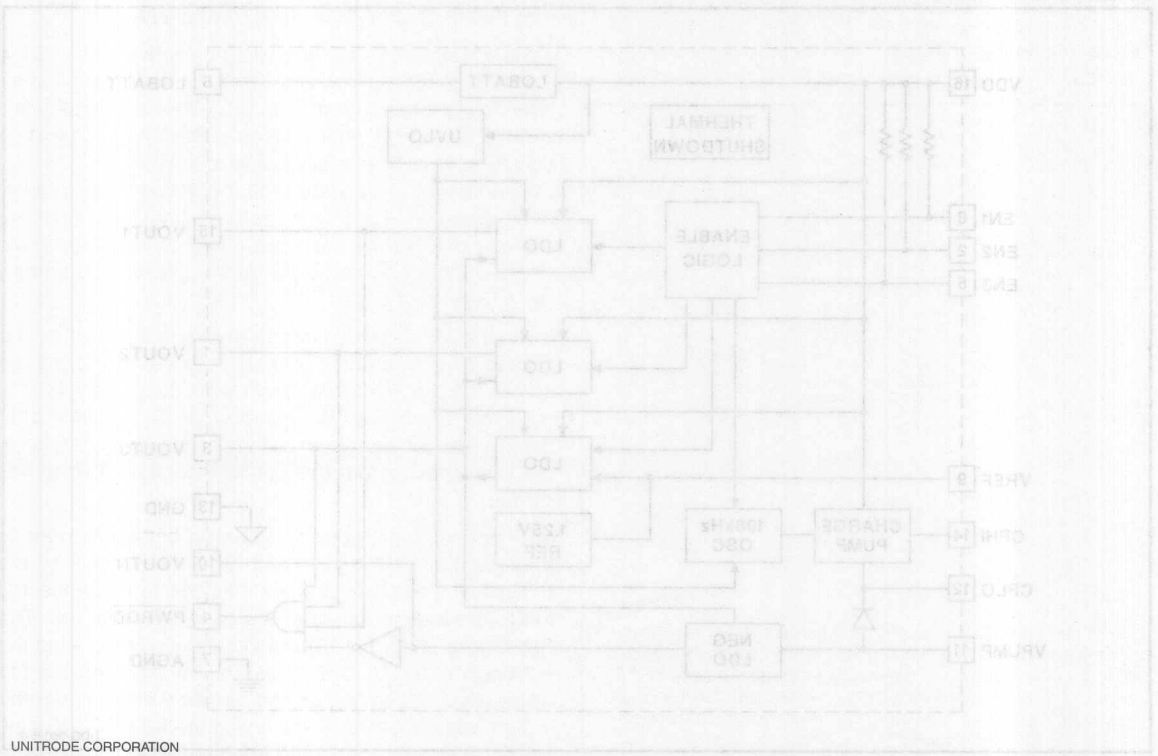
APPLICATION INFORMATION (cont.)

IC temperature. However, this heat sink must be electrically isolated from all other IC pins including ground. This is a critically important point, as heat sinking to the system ground is not possible.

If the discharge current exceeds 5.25A typically, the UCC3911 short circuit protection circuitry turns off the power FET and will not allow further discharge current. A nominal delay of 100µsec is provided to allow for short term transient conditions. If longer delays are required, a capacitor placed between CDLY and B0 increases the delay according to:

$$T_{DLY} \approx 25\mu s + (5 \bullet 10^{-5}) \bullet (25pF + CDLY) \bullet V_{DD}$$

The CE pin is used to initialize the state of the battery pack during assembly. Holding this pin low forces the state machine to the normal state. The last step in the assembly process would be to cut the trace between this pin and ground which allows the internal pull up to start the state machine.



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UCC3930-3/-5

PRELIMINARY

Cellular Telephone Power Converter

FEATURES

- BiCMOS Low Power RF/Cellular Power Management
- Negative Supply Voltage at 5mA for GaAs MESFET Amplifiers
- Separate Micro-Power Logic Supply Enable
- Low Quiescent, 3mA, Operating Current
- Three Low Dropout (200mV) Regulators
- Power Good Indicator for Managing Power Supply Sequencing
- Low Power Mode Input Quiescent Current, 2µA (Max)
- Low Battery Early Warning Detection Output

DESCRIPTION

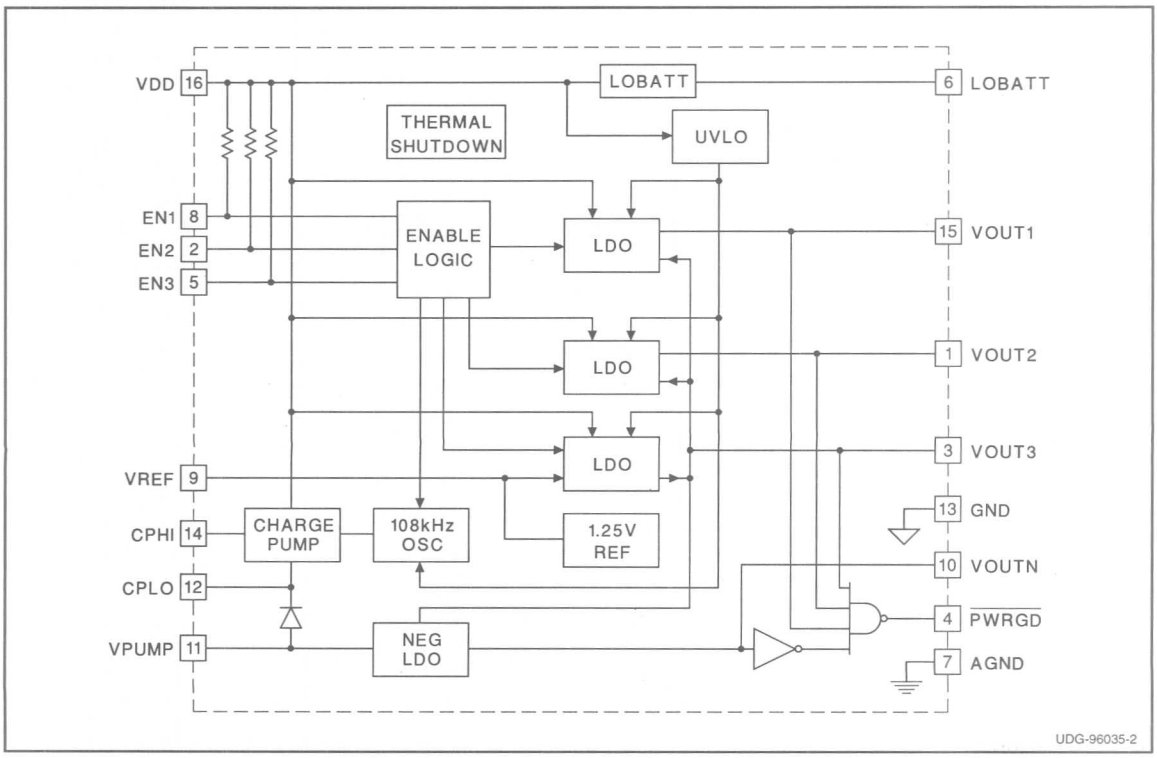
The UCC3930-3/-5 family of BiCMOS low power management controllers is designed for battery powered applications for RF/Cellular telephones, base stations, transmitters, receivers and pagers.

The circuit consists of three low dropout voltage regulators with <200mV maximum dropout, a low battery detection output, and a power good signal for managing power supply sequencing. Power management control is accomplished by the enable pins: EN1, EN2, and EN3 (See Table 1).

A negative supply for GaAs MESFET amplifiers is generated by a capacitive charge pump using a 0.1µF switching capacitor. The output noise of the negative supply is kept below 1mV by linearly regulating the coarse voltage present at the charge pump output.

Available packages include the 16-pin SSOP and 16-pin DIP. Consult Factory for exact SSOP-16 package dimensions.

BLOCK DIAGRAM



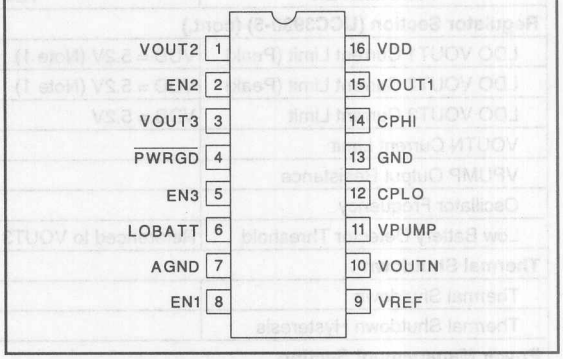
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ABSOLUTE MAXIMUM RATINGS

Input Voltage (VDD) . . . . . +8V
EN Signal Voltage . . . . . –0.3V to VDD +0.3V
Regulator Output Current 900mA
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C
Currents are positive into, negative out of the specified terminal.
Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

DIL-16 or SSOP-16 (Top View)
N or J, M Packages



ELECTRICAL CHARACTERISTICS

Unless otherwise specified, T_A = 0°C to 70°C for UCC3930-3/-5 and –40°C to +85°C for UCC2930-3/-5, C_{VPUMP} = 10µF, C_P = 0.1µF, C_{VOUT3} = C_{VOUTN} = 1.0µF, C_{VREF} = 0.1µF, C_{VDD} = 10µF, C_{VOUT1} = C_{VOUT2} = 2.2µF, 3.5V < VDD < 8.0V for the UCC3930-3 and 5.2V < VDD < 8.0V for the UCC3930-5, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Section (UCC3930-3)					
Shutdown Supply Current	EN1, EN2, EN3 = Open, 0°C ≤ T_A ≤ 70°C		2	10	µA
Low Power Operating Current	EN1 = 0V, EN2 and EN3 = Open		28	40	µA
VDD Operating Current	I_{LOAD} = 0 for All Outputs, EN1, EN2, EN3 = Low		3	4.5	mA
Undervoltage Lockout		3.0	3.2	3.4	V
Regulator Section (UCC3930-3)					
Output Voltage, VPUMP	VDD_{LOAD} = 0mA, $VOUTN_{LOAD}$ = –5mA, VDD = 3.5V			–2.5	V
Output Voltage, VOUTN	$VPUMP_{LOAD}$ = 0mA, $VOUTN_{LOAD}$ = –5mA	–2.7	–2.5	–2.3	V
Output Voltage, VOUT1, VOUT2	I_{LOAD} = 0mA to 50mA	3.22	3.3	3.383	V
Output Voltage, VOUT3	I_{LOAD} = 0mA to 5mA	3.22	3.3	3.383	V
	I_{LOAD} = 0mA to 5mA, EN1 = Low, EN2 = EN3 = Open	3.135		3.465	V
LDO VOUT1 Current Limit (Peak)	VDD = 3.5V (Note 1)	–900	–500		mA
LDO VOUT2 Current Limit (Peak)	VDD = 3.5V (Note 1)	–900	–500		mA
LDO VOUT3 Current Limit	VDD = 3.5V	–180	–100		mA
VOUTN Current Limit			80	150	mA
VPUMP Output Resistance			150		Ω
Oscillator Frequency			108		kHz
Low Battery Detector Threshold	Referenced to VOUT3	200			mV
Power Supply Section (UCC3930-5)					
Shutdown Supply Current	EN1, EN2, and EN3 = Open, 0°C ≤ T_A ≤ 70°C		2	10	µA
Low Power Operating Current	EN1 = 0V, EN2 and EN3 = Open		28	40	µA
VDD Operating Current	I_{LOAD} = 0 for All Outputs, EN1, EN2, EN3 = Low		3	4.5	mA
Undervoltage Lockout		4.15	4.65	5.15	V
Regulator Section (UCC3930-5)					
Output Voltage, VPUMP	VDD_{LOAD} = 0mA, $VOUTN_{LOAD}$ = –5mA, VDD = 5.2V			–4.5	V
Output Voltage, VOUTN	$VPUMP_{LOAD}$ = 0mA, $VOUTN_{LOAD}$ = –5mA	–4.6		–4.1	V
Output Voltage, VOUT1, VOUT2	I_{LOAD} = 0mA to 50mA	4.875	5	5.125	V
Output Voltage, VOUT3	I_{LOAD} = 0mA to 5mA	4.875	5	5.125	V
	I_{LOAD} = 0mA to 5mA, EN1 = Low, EN2 = EN3 = Open	4.75		5.25	V

ELECTRICAL CHARACTERISTICS (cont.) Unless otherwise specified, T_A = 0°C to 70°C for UCC3930-3/-5 and –40°C to +85°C for UCC2930-3/-5, C_{VPUMP} = 10µF, C_P = 0.1µF, C_{VOUT3} = C_{VOUTN} = 1.0µF, C_{VREF} = 0.1µF, C_{VDD} = 10µF, C_{VOUT1} = C_{VOUT2} = 2.2µF, 3.5V < VDD < 8.0V for the UCC3930-3 and 5.2V < VDD < 8.0V for the UCC3930-5, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Regulator Section (UCC3930-5) (cont.)					
LDO VOUT1 Current Limit (Peak)	VDD = 5.2V (Note 1)	–900	–500		mA
LDO VOUT2 Current Limit (Peak)	VDD = 5.2V (Note 1)	–900	–500		mA
LDO VOUT3 Current Limit	VDD = 5.2V	–180	–100		mA
VOUTN Current Limit			80	150	mA
VPUMP Output Resistance			150		Ω
Oscillator Frequency			108		kHz
Low Battery Detector Threshold	Referenced to VOUT3	200			mV
Thermal Shutdown					
Thermal Shutdown			165		°C
Thermal Shutdown Hysteresis			20		°C
Power Management Section					
Input Logic Low	Relative to GND			0.5	V
Input Logic High	Relative to VDD	VDD-0.5			V
Input Logic Pull-up Current	VDD = 8V	0.6	1.4	3	µA
Output Low Voltage	I_{LOAD} = 0.1mA, Relative to GND			0.5	V
Output High Voltage	I_{LOAD} = 0.1mA, Relative to VDD	VDD-0.5			V

Note 1: Once Thermal Cycling engages, the Average Current is much less in magnitude than this initial Peak Value.

PIN DESCRIPTIONS

AGND: This is the analog ground for power outputs.

CPHI, CPLO: These pins are used to connect a flying capacitor, typically 0.1µF, across the two internal single-pole, double-throw switches. The internal switches provide a charge pumped voltage on the VPUMP pin.

EN1, EN2, EN3: These input pins control the operating mode of the device. Operation follows the truth table presented below.

GND: This is the ground return for all on-chip switching functions. Typically this pin is connected to the ground plane. The bypass capacitors connected to GND should have the shortest possible lead lengths.

LOBATT: A digital output signal that indicates a low battery condition when the VDD–V_{OUT} differential is less than 200mV.

$\overline{PWRGD}$: This pin, when low, is a digital indication that all the regulators have exceeded 80% of their steady state output voltage.

VDD: Positive supply input for the regulator. Bypass this pin to GND with a 10µF low ESR, ESL capacitor.

VOUT1, VOUT2, VOUT3: These outputs are low dropout regulators with varying drive capabilities. They are internally short circuit current protected. The VOUT3 output is the primary reference for all supplies. This output is typically connected to non-switching loads such as battery back-up static RAM or low power analog circuitry. The 50mA regulators are output compensated with 2.2µF low ESR capacitors. The VOUT3 regulator is compensated with a single 1µF capacitor.

TABLE 1. ENABLE PINS

EN1	EN2	EN3	VOUT1	VOUT2	VOUT3	VOUTN	VPUMP
0	0	0	ON	ON	ON	ON	ON
0	0	1	ON	OFF	ON	ON	ON
0	1	0	OFF	ON	ON	ON	ON
0	1	1	OFF	OFF	ON	OFF	OFF
1	0	0	NOT VALID				
1	0	1	NOT VALID				
1	1	0	NOT VALID				
1	1	1	OFF	OFF	OFF	OFF	OFF

PIN DESCRIPTIONS (cont.)

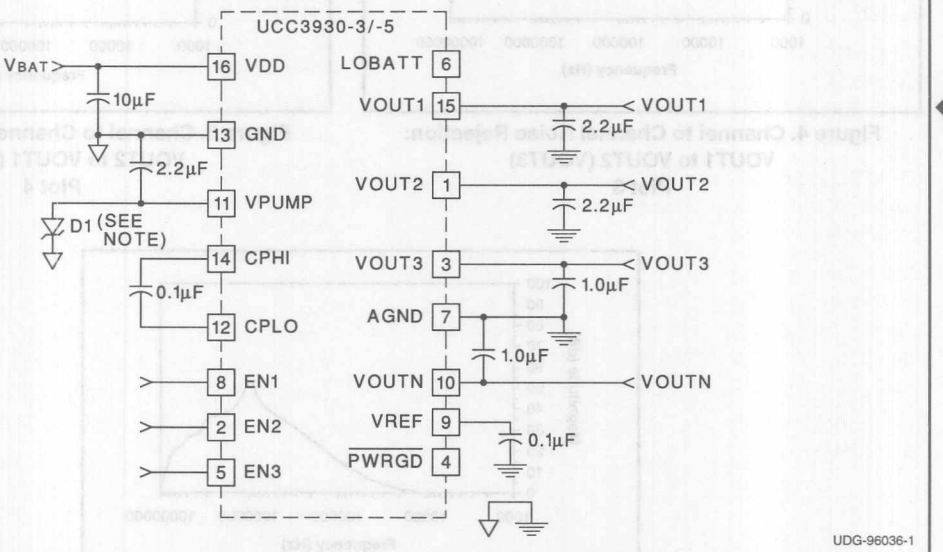
VOUTN: This pin is the power source for GaAs MESFET amplifiers. A single 1.0µF output capacitor connected to AGND will provide adequate loop compensation and filtering of the regulator.

VPUMP: This output is a coarsely regulated negative supply for preregulating the VOUTN GaAs MESFET supply. A single 2.2µF capacitor connected to GND will provide adequate filtering of the charge pump output.

VREF: This output is the internal 1.25V bandgap reference. The regulator is output compensated with a minimum 0.01µF capacitor. By utilizing external compensation, the reference voltage noise is kept to a minimum.

APPLICATION INFORMATION

An application circuit for the UCC3930-3/-5 is shown in Figure 1. Careful attention must be paid to proper layout and decoupling techniques to insure low noise operation. The VDD and VPUMP pins should be bypassed directly to GND, while the output regulators and VREF should be separately bypassed to AGND. A single point connection should connect these two points as close to the IC as possible.



Note: Schottky diode D1, #SK12DICT-ND is recommended on VPUMP when using the UCC3930-3 to ensure proper clamping during Short Circuit Fault conditions.

Figure 1. Typical Application Circuit

TYPICAL CHARACTERISTICS

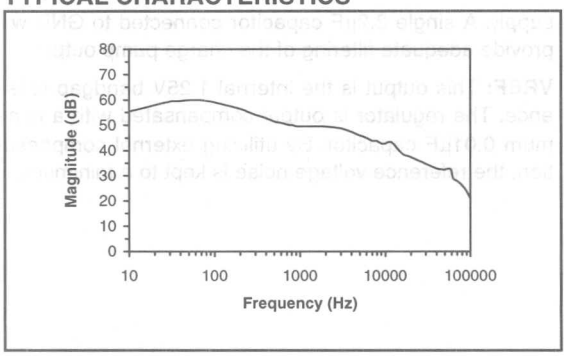


Figure 2. Ripple Rejection: VDD to VOUT1 (VOUT2)
Plot 1

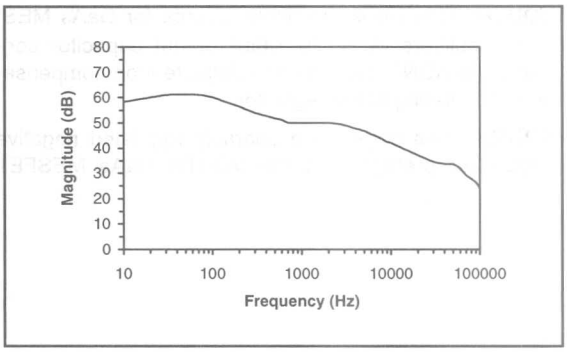


Figure 3. Ripple Rejection: VDD to VOUT3
Plot 2

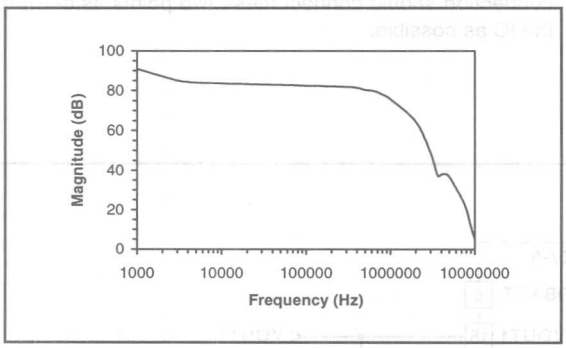


Figure 4. Channel to Channel Noise Rejection: VOUT1 to VOUT2 (VOUT3)
Plot 3

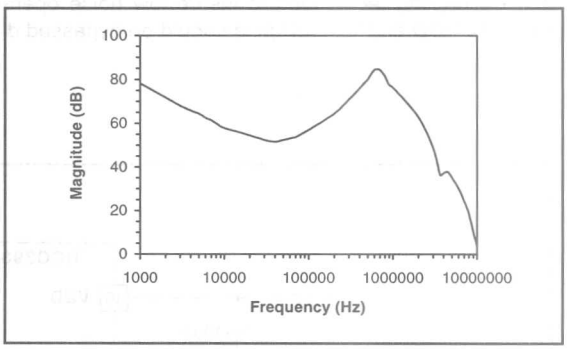


Figure 5. Channel to Channel Noise Rejection: VOUT2 to VOUT1 (VOUT3)
Plot 4

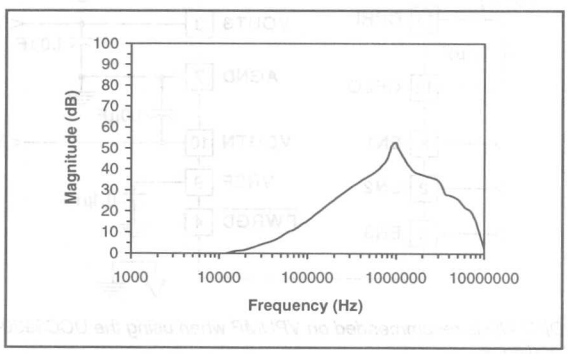


Figure 6. Channel to Channel Noise Rejection: VOUT3 to VOUT1 (VOUT2)
Plot 5

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

1V Synchronous Boost Converter

FEATURES

- 1V Input Voltage Operation Startup Guaranteed Under Full Load on Main Output With Operation Down to 0.4V
- Input Voltage Range of 1V to VOUT + 0.5V
- 500mW Output Power at Battery Voltages as Low as 0.8V
- Secondary 9V Supply From a Single Inductor
- Adjustable Output Power Limit Control
- Output Fully Disconnected in Shutdown
- Adaptive Current Mode Control for Optimum Efficiency
- 8µA Shutdown Supply Current

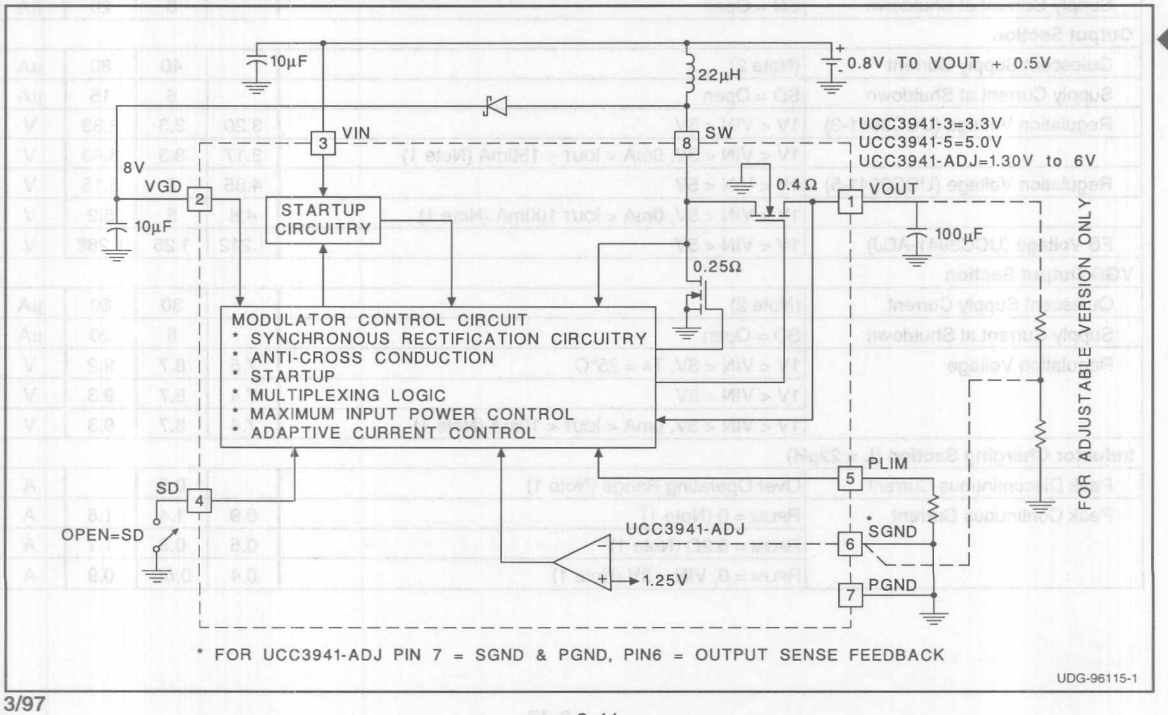
DESCRIPTION

The UCC3941 family of low input voltage single inductor boost converters are optimized to operate from a single or dual alkaline cell, and step up to a 3.3V, 5V, or an adjustable output at 500mW. The UCC3941 family also provides an auxiliary 9V 100mW output, primarily for the gate drive supply, which can be used for applications requiring an auxiliary output such as a 5V supply by linear regulating. The primary output will start up under full load at input voltages typically as low as 0.8V, with a guaranteed maximum of 1V, and will operate down to 0.4V once the converter is operating, maximizing battery utilization.

Demanding applications such as Pagers and PDA's require high efficiency from several milli-watts to several hundred milli-watts, and the UCC3941 family accommodates these applications with >80% typical efficiencies over the wide range of operation. The high efficiency at low output current is achieved by optimizing switching and conduction losses along with low quiescent current. At higher output current the 0.25Ω switch, and 0.4Ω synchronous rectifier, along with continuous mode conduction, provide high efficiency. The wide input voltage range on the UCC3941 family can accommodate other power sources such as NiCd and NiMH.

Other features include maximum power control and shutdown control. Packages available are the 8-pin SOIC (D) and 8-pin DIP (N or J).

SIMPLIFIED BLOCK DIAGRAM AND APPLICATION CIRCUIT



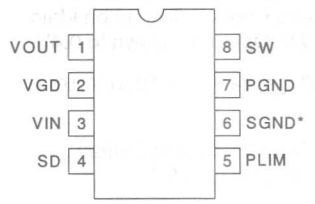
ABSOLUTE MAXIMUM RATINGS

VIN Voltage ..... –0.3V to 10V
SD Voltage ..... –0.3V to VIN
PLIM Voltage ..... –0.3V to 10V
VGD Voltage..... –0.3V to 15V
SW Voltage..... –0.3V to 15V
VOUT Voltage ..... –0.3V to 10V
Storage Temperature..... –65°C to +150°C
Junction Temperature ..... –55°C to +150°C
Lead Temperature (Soldering, 10 sec.)..... +300°C

Currents are positive into, negative out of the specified terminal.
Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

DIL-8, SOIC-8 (Top View)
N or J Package, D Package



Pin 6 is FB for UCC3941-ADJ.

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, T_A = 0°C to 70°C, VIN = 1.25V for UCC3941-3/-ADJ, VIN = 2.5V for UCC3941-5, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VIN Section					
Minimum Startup Voltage	No External VGD Load, T_J = 25°C, I_{OUT} = 100mA (Note 1)		0.8	1	V
Minimum Start Voltage	No External VGD Load, I_{OUT} = 100mA (Note 1)		0.9	1.1	V
Minimum Dropout Voltage	No External VGD Load, I_{OUT} = 100mA (Note 1)			0.5	V
Input Voltage Range		1		VOUT+ 0.5	V
Quiescent Supply Current	(Note 2)		10	25	µA
Supply Current at Shutdown	SD = Open		8	20	µA
Output Section					
Quiescent Supply Current	(Note 2)		40	80	µA
Supply Current at Shutdown	SD = Open		6	15	µA
Regulation Voltage (UCC3941-3)	1V < VIN < 3V	3.20	3.3	3.39	V
	1V < VIN < 3V, 0mA < I_{OUT} < 150mA (Note 1)	3.17	3.3	3.43	V
Regulation Voltage (UCC3941-5)	1V < VIN < 5V	4.85	5	5.15	V
	1V < VIN < 5V, 0mA < I_{OUT} 100mA (Note 1)	4.8	5	5.2	V
FB Voltage (UCC3941-ADJ)	1V < VIN < 5V	1.212	1.25	1.288	V
VGD Output Section					
Quiescent Supply Current	(Note 2)		30	60	µA
Supply Current at Shutdown	SD = Open		8	20	µA
Regulation Voltage	1V < VIN < 3V, T_A = 25°C	7.5	8.7	9.2	V
	1V < VIN < 3V	7.4	8.7	9.3	V
	1V < VIN < 3V, 0mA < I_{OUT} < 10mA (Note 1)	7.4	8.7	9.3	V
Inductor Charging Section (L = 22µH)					
Peak Discontinuous Current	Over Operating Range (Note 1)		0.5		A
Peak Continuous Current	R_{PLIM} = 0 (Note 1)	0.9	1.4	1.8	A
	R_{PLIM} = 6.2Ω (Note 1)	0.5	0.8	1.1	A
	R_{PLIM} = 0, VIN = 3V (Note 1)	0.4	0.65	0.9	A

ELECTRICAL CHARACTERISTICS (cont.): Unless otherwise specified, T_A = 0°C to 70°C, VIN = 1.25V for UCC3941-3/-ADJ, VIN = 2.5V for UCC3941-5, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Inductor Charging Section					
Charge Switch R_{DSON}	D Package		0.25	0.4	Ω
Current Limit Delay	(Note 1)		50		ns
Synchronous Rectifier Section					
Rectifier R_{DSON}	D Package		0.35	0.6	Ω

Note 1: Performance from application circuit shown in Figures 3 - 5 guaranteed by design and alternate testing methods, but not 100% tested as shown in production.

Note 2: For the UCC3941-3, VOUT = 3.47V and VGD = 9.3V. For the UCC3941-5, VOUT = 5.25V, VGD = 10.4V. For the UCC3941-ADJ, FB = 1.315V, VGD = 10.4V.

PIN DESCRIPTIONS

FB: Feedback control pin used in the UCC3941-ADJ version only. The internal reference for this comparator is 1.25V and external resistors provide the gain to the output voltage.

PGND: Power ground of the IC. The inductor charging current flows through this pin. For the UCC3941-ADJ signal ground and power ground lines are tied to a common pin.

PLIM: This pin is programmed to set the maximum input power for the converter. For example a 1A current limit at 1V would have a 333mA limit at 3V input keeping the input power constant at 1W. The peak current at VIN = 1V is programmed to 1.5A (1.5W) when this pin is grounded. The power limit is given by:

$$PL(W) = \frac{14.5}{R_{PL} + 6.5}$$

where R_{PL} is equal to the external resistor from the PLIM pin to ground. The peak current limit is given by:

$$I_{PK}(A) = \frac{14.5}{VIN \bullet (R_{PL} + 6.5)}.$$

Constant power gives several advantages over constant current such as lower output ripple.

SD: When this pin is open, the built in 2µA current source pulls up on the pin and programs the IC to go into sleep or shutdown mode. When this pin is tied to ground, the IC is enabled and both output voltages will regulate.

SGND: Signal ground of the IC. For the UCC3941-ADJ signal ground and power ground lines are tied to a common pin.

SW: An inductor is connected between this node and VIN. The VGD (Gate Drive Supply) flyback diode is also connected to this pin. When servicing the 3.3V supply, this pin will go low charging the inductor, then shut off, dumping the energy through the synchronous rectifier to the output. When servicing the VGD supply, the internal synchronous rectifier stays off, and the energy is diverted to VGD through the flyback diode. During discontinuous portions of the inductor current a MOSFET resistively connects VIN to SW damping excess circulating energy to eliminate undesired high frequency ringing.

VGD: The VGD pin which is coarsely regulated around 9V and is primarily used for the gate drive supply for the power switches in the IC. This pin can be loaded with up to 10mA as long as it does not present a load at voltages below 2V. This ensures proper startup of the IC. The VGD supply can go as low as 7.5V without interfering with the servicing of the 3.3V output. Below 7.5V, VGD will have the highest priority, although practically the voltage should not decay to that level if the output capacitor is sized properly.

VIN: Input voltage to supply the IC during startup. After the output is running the IC draws power from VOUT or VGD.

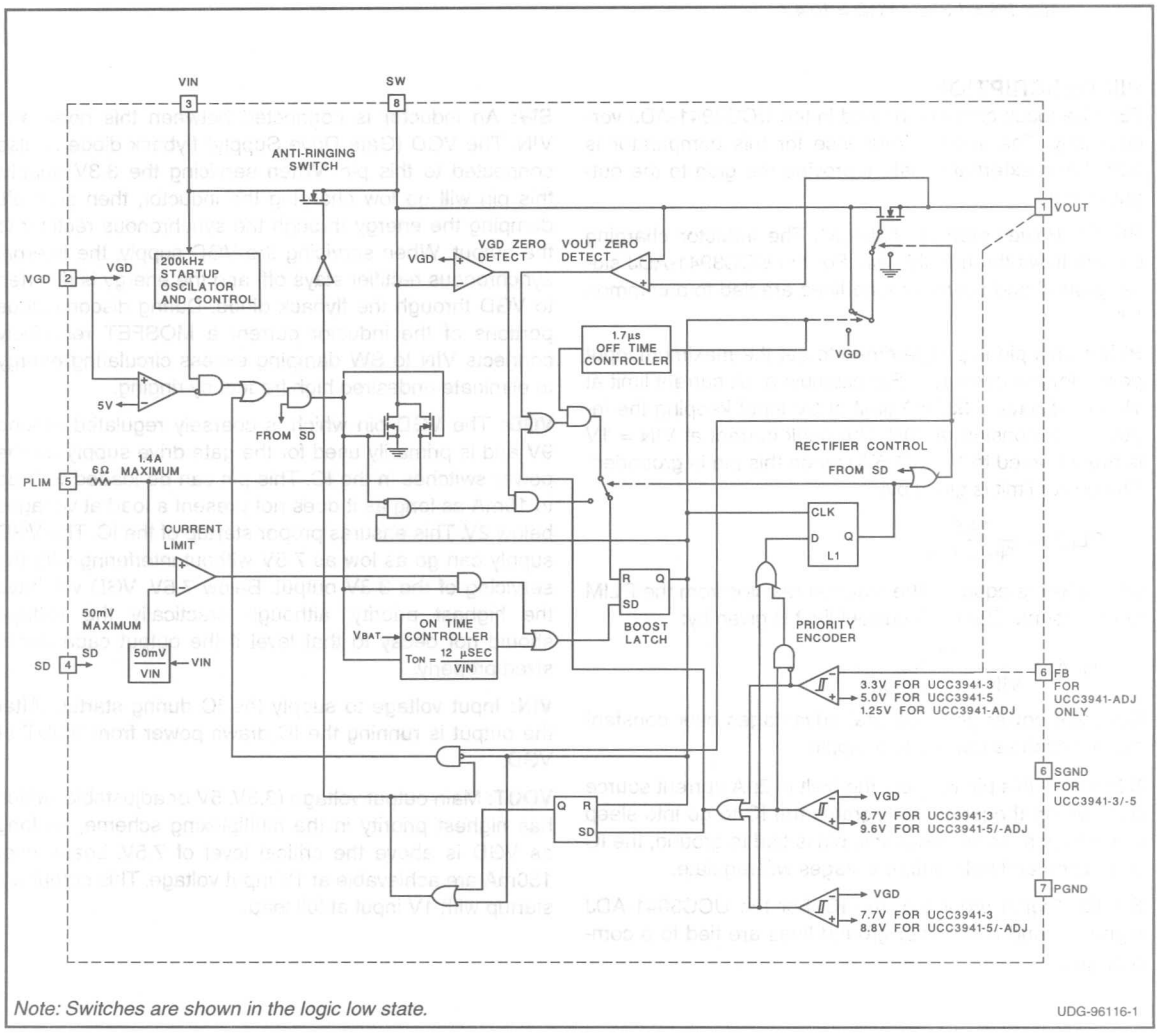
VOUT: Main output voltage (3.3V, 5V or adjustable) which has highest priority in the multiplexing scheme, as long as VGD is above the critical level of 7.5V. Loads over 150mA are achievable at 1V input voltage. This output will startup with 1V input at full load.

APPLICATION INFORMATION

A detailed block diagram of the UCC3941 is shown in Figure 1. Unique control circuitry provides high efficiency power conversion for both light and heavy loads by transitioning between discontinuous and continuous conduction based on load conditions. Figure 2 depicts converter waveforms for the application circuit shown in Figure 3. A single 22µH inductor provides the energy pulses required for a highly efficient 3.3V converter at up to 500mW output power.

At time t_1, the 3.3V output drops below its lower threshold, and the inductor is charged with an on time determined by:

$$T_{ON} = \frac{12\mu s}{VIN}.$$



Note: Switches are shown in the logic low state.

UDG-96116-1

Figure 1. 1V Synchronous Boost

APPLICATION INFORMATION (cont.)

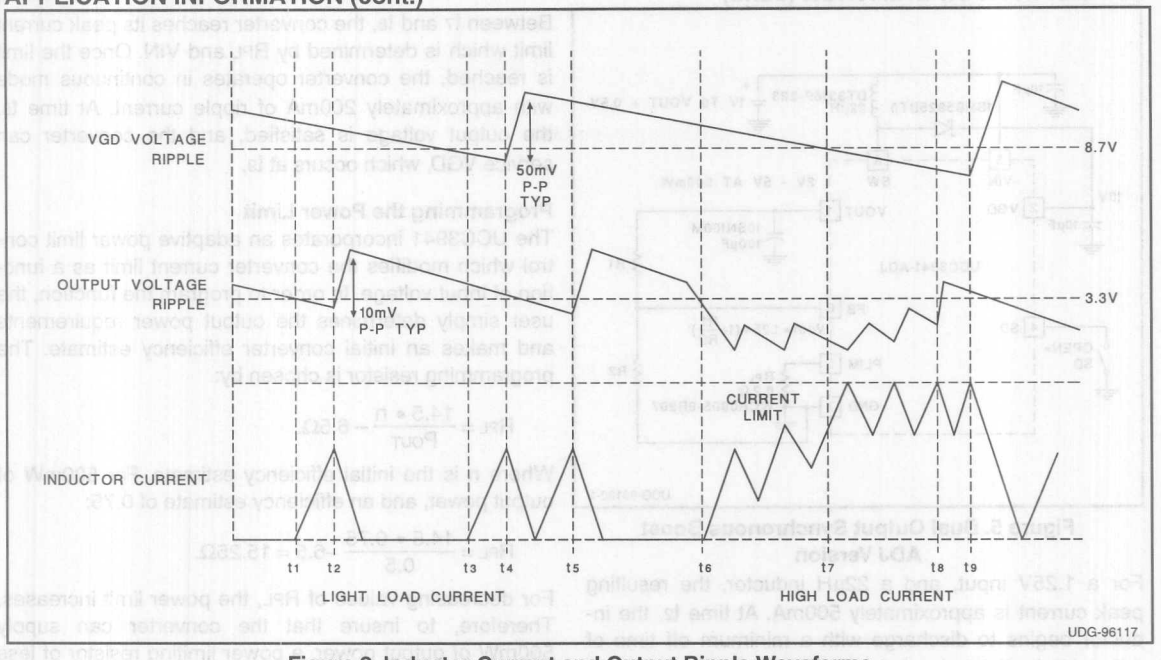


Figure 2. Inductor Current and Output Ripple Waveforms

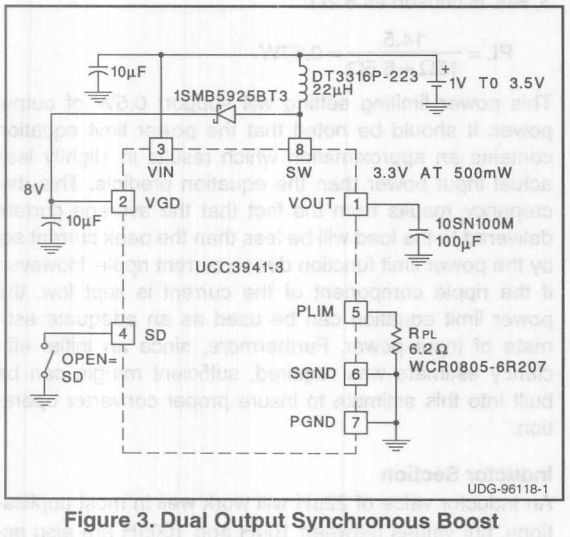


Figure 3. Dual Output Synchronous Boost 3.3V Version

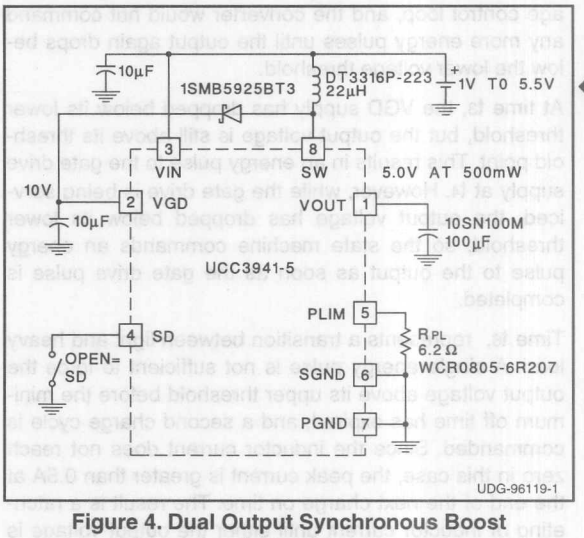


Figure 4. Dual Output Synchronous Boost 5V Version

APPLICATION INFORMATION (cont.)

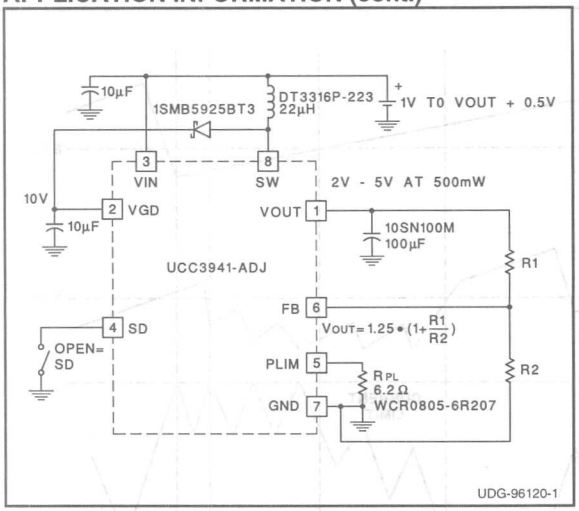


Figure 5. Dual Output Synchronous Boost ADJ Version

For a 1.25V input, and a 22µH inductor, the resulting peak current is approximately 500mA. At time t_2, the inductor begins to discharge with a minimum off time of 1.7µs. Under lightly loaded conditions, the amount of energy delivered in this single pulse would satisfy the voltage control loop, and the converter would not command any more energy pulses until the output again drops below the lower voltage threshold.

At time t_3, the VGD supply has dropped below its lower threshold, but the output voltage is still above its threshold point. This results in an energy pulse to the gate drive supply at t_4. However, while the gate drive is being serviced, the output voltage has dropped below its lower threshold, so the state machine commands an energy pulse to the output as soon as the gate drive pulse is completed.

Time t_6, represents a transition between light and heavy load. A single energy pulse is not sufficient to force the output voltage above its upper threshold before the minimum off time has expired, and a second charge cycle is commanded. Since the inductor current does not reach zero in this case, the peak current is greater than 0.5A at the end of the next charge on time. The result is a ratcheting of inductor current until either the output voltage is satisfied, or the converter reaches its programmed current limit. At time t_7, the gate drive voltage has dropped below its threshold but the converter continues to service the output because it has highest priority, unless VGD drops below 7.5V.

Between t_7 and t_8, the converter reaches its peak current limit which is determined by R_{PL} and VIN. Once the limit is reached, the converter operates in continuous mode with approximately 200mA of ripple current. At time t_8, the output voltage is satisfied, and the converter can service VGD, which occurs at t_9.

Programming the Power Limit

The UCC3941 incorporates an adaptive power limit control which modifies the converter current limit as a function of input voltage. In order to program the function, the user simply determines the output power requirements and makes an initial converter efficiency estimate. The programming resistor is chosen by:

$$R_{PL} = \frac{14.5 \bullet n}{P_{OUT}} - 6.5\Omega.$$

Where n is the initial efficiency estimate. For 500mW of output power, and an efficiency estimate of 0.75:

$$R_{PL} = \frac{14.5 \bullet 0.75}{0.5} - 6.5 = 15.25\Omega.$$

For decreasing values of R_{PL}, the power limit increases. Therefore, to insure that the converter can supply 500mW of output power, a power limiting resistor of less than 15Ω must be chosen. For the circuit shown in Figure 3, R_{PL} is chosen as 6.2Ω:

$$PL = \frac{14.5}{15\Omega + 6.5\Omega} = 0.67W.$$

This power limiting setting will support 0.5W of output power. It should be noted that the power limit equation contains an approximation which results in slightly less actual input power than the equation predicts. This discrepancy results from the fact that the average current delivered to the load will be less than the peak current set by the power limit function due to current ripple. However, if the ripple component of the current is kept low, the power limit equation can be used as an adequate estimate of input power. Furthermore, since an initial efficiency estimate was required, sufficient margin can be built into this estimate to insure proper converter operation.

Inductor Section

An inductor value of 22µH will work well in most applications, but values between 10µH and 100µH are also acceptable. Lower value inductors typically offer lower ESR and smaller physical size. Due to the nature of the "bang-bang" controllers, larger inductor values will typically result in larger overall voltage ripple, because once the output voltage level is satisfied the converter goes dis-

APPLICATION INFORMATION (cont.)

continuous, resulting in the residual energy of inductor causing overshoot.

It is recommended to keep the ESR of the inductor below 0.15Ω for 500mW applications. A Coilcraft DT3316P-223 surface mount inductor is one choice since it has a current rating of 1.5A and an ESR of 84mΩ. Other choices for surface mount inductors are shown in Table 1.

MANUFACTURER	PART NUMBERS
Coilcraft Cary, Illinois Tel: 708-639-2361 Fax: 708-639-1469	DT Series
Coiltronics Boca Raton, Florida Tel: 407-241-7876 Fax: 407-241-9339	CTX Series

Table 1. Inductor Suppliers

Output Capacitor Selection

Once the inductor value is selected the capacitor value will determine the ripple of the converter. The worst case peak to peak ripple of a cycle is determined by two components, one is due to the charge storage characteristic, and the other is the ESR of the capacitor. The worst case ripple occurs when the inductor is operating at maximum current and is expressed as follows:

$$\Delta V = \frac{(I_{CL})^2 \bullet L}{2 \bullet C \bullet (V_O - V_I)} + I_{CL} \bullet C_{ESR} \text{ where}$$

I_{CL} = the peak inductor current $\left(I_{CL} = \frac{\text{PowerLimit}}{V_{IN}}\right)$

ΔV = output ripple
V_O = output voltage
V_I = input voltage
C_{ESR} = ESR of the output capacitor

A Sanyo OS-CON series surface mount capacitor (10SN100M) is one recommendation. This part has an ESR rating of 90mΩ at 100µF. Other potential capacitor sources are shown in Table 2.

MANUFACTURER	PART NUMBER
Sanyo Video Components San Diego, California Tel: 619-661-6322 Fax: 619-661-1055	OS-CON Series
AVX Sanford, Maine Tel: 207-282-5111 Fax: 207-283-1941	TPS Series
Sprague Concord, New Hampshire Tel: 603-224-1961 Fax: 603-224-1430	695D Series

Table 2. Capacitor Suppliers

Input Capacitor Selection

Since the UCC3941 family does not require a large decoupling capacitor on the input voltage to operate properly, a 10µF capacitor is sufficient for most applications. Optimum efficiency will occur when the capacitor value is large enough to decouple the source impedance. This usually occurs for capacitor values in excess of 100µF.

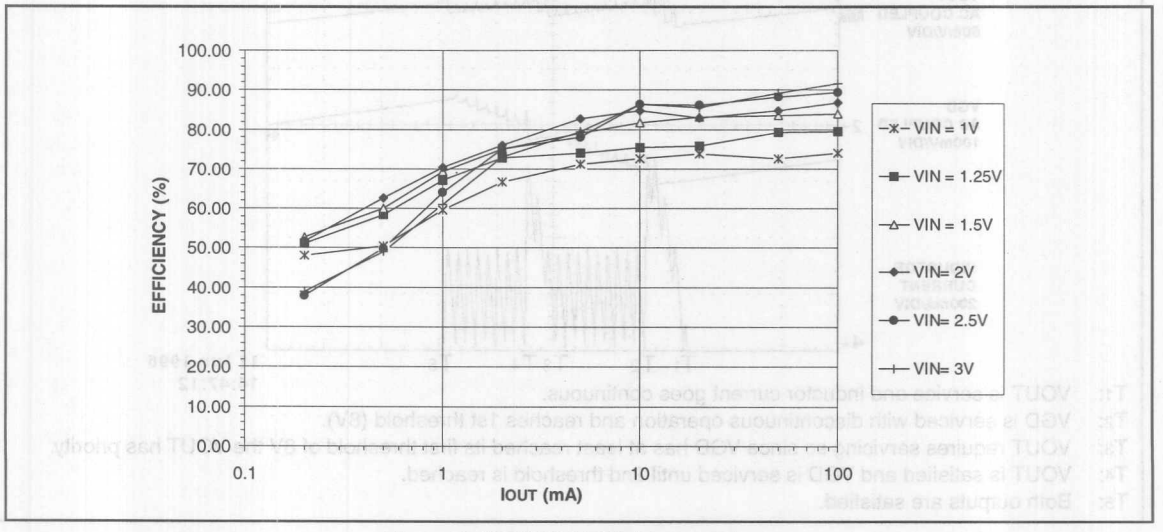
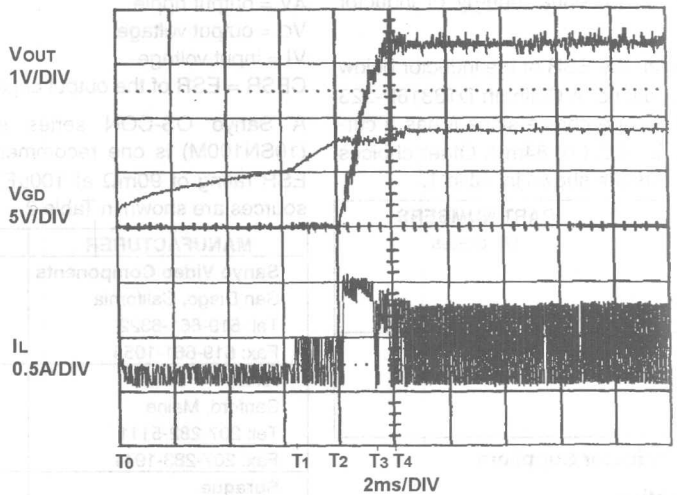


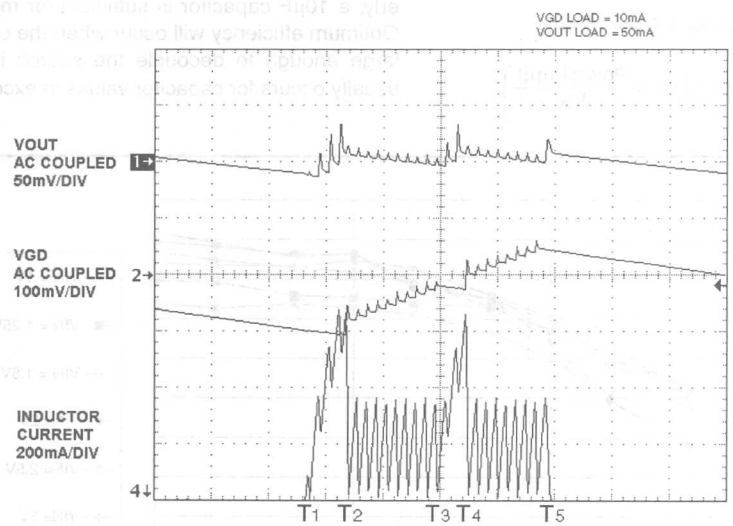
Figure A. UCC3941 Efficiency vs. I_{OUT}

APPLICATION INFORMATION (cont.)



T0: 200kHz startup oscillator starts VGD rising.
T1: VGD gets to a sufficient voltage (5V) to run IC in normal operating mode.
T2: VGD has reached a sufficient voltage (18V) to get VOUT started.
T3: VOUT is serviced and starting up.
T4: VOUT has reached a sufficient voltage and VGD is serviced until it reaches ≈ 9V.

Figure B. Startup Characteristics



T1: VOUT is service and inductor current goes continuous.
T2: VGD is serviced with discontinuous operation and reaches 1st threshold (8V).
T3: VOUT requires servicing so since VGD has at least reached its first threshold of 8V the VOUT has priority.
T4: VOUT is satisfied and VGD is serviced until 2nd threshold is reached.
T5: Both outputs are satisfied.

Figure C. Dual Output Example

APPLICATION INFORMATION (cont.)

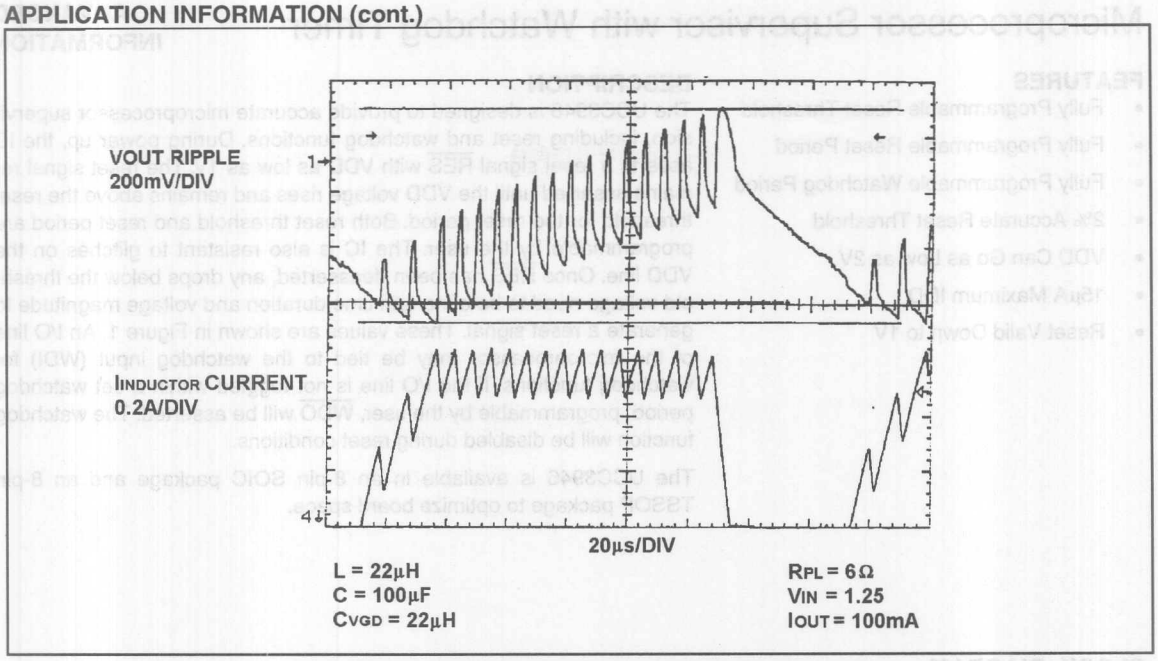


Figure D. Pseudo Continuous Mode Operation

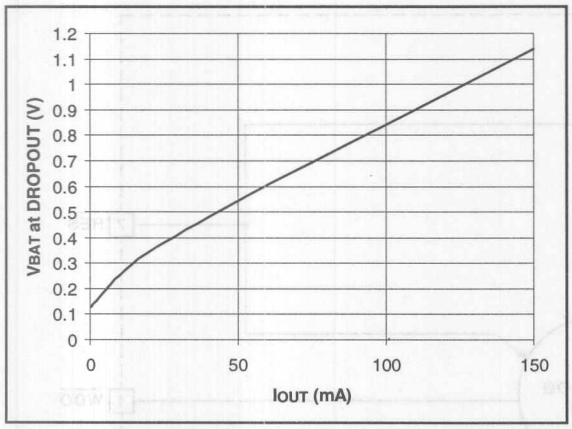


Figure E. UCC3941-3 Dropout vs. IOUT

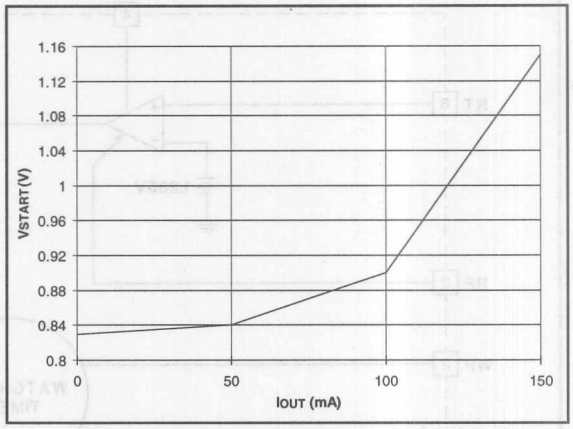


Figure F. Minimum Start Voltage vs. IOUT

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Microprocessor Supervisor with Watchdog Timer

ADVANCED INFORMATION

FEATURES

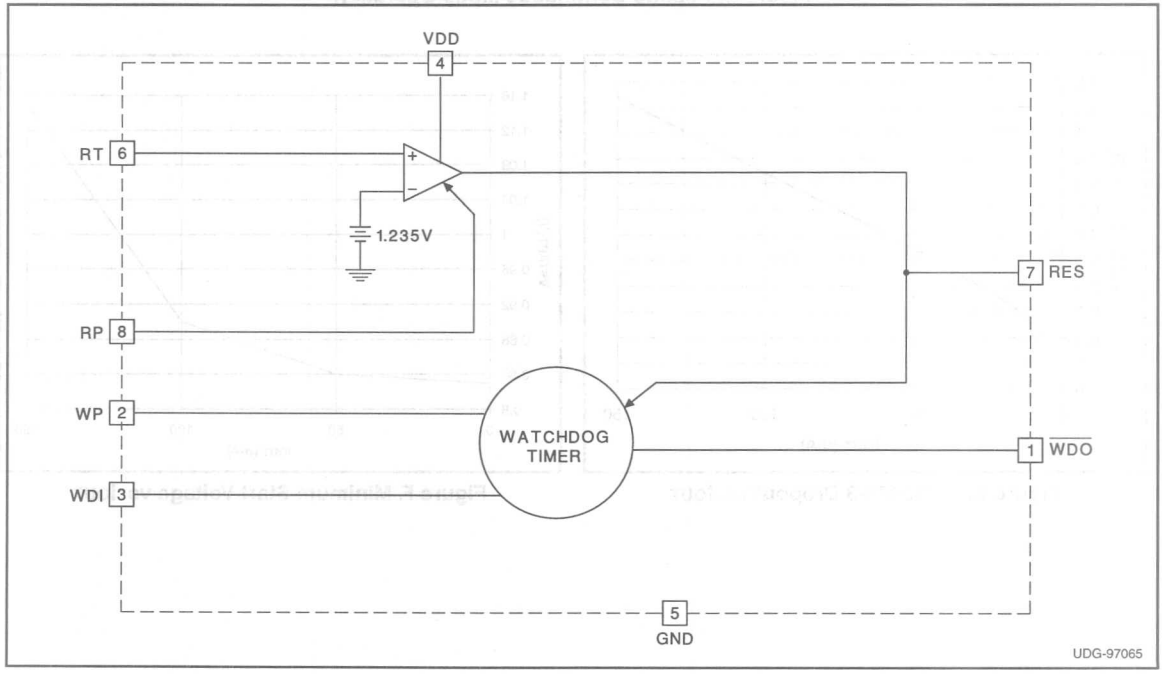
- Fully Programmable Reset Threshold
- Fully Programmable Reset Period
- Fully Programmable Watchdog Period
- 2% Accurate Reset Threshold
- VDD Can Go as Low as 2V
- 15µA Maximum IDD
- Reset Valid Down to 1V

DESCRIPTION

The UCC3946 is designed to provide accurate microprocessor supervision, including reset and watchdog functions. During power up, the IC asserts a reset signal $\overline{RES}$ with VDD as low as 1V. The reset signal remains asserted until the VDD voltage rises and remains above the reset threshold for the reset period. Both reset threshold and reset period are programmable by the user. The IC is also resistant to glitches on the VDD line. Once $\overline{RES}$ has been deasserted, any drops below the threshold voltage need to be of certain time duration and voltage magnitude to generate a reset signal. These values are shown in Figure 1. An I/O line of the microprocessor may be tied to the watchdog input (WDI) for watchdog functions. If the I/O line is not toggled within a set watchdog period, programmable by the user, $\overline{WDO}$ will be asserted. The watchdog function will be disabled during reset conditions.

The UCC3946 is available in an 8-pin SOIC package and an 8-pin TSSOP package to optimize board space.

BLOCK DIAGRAM



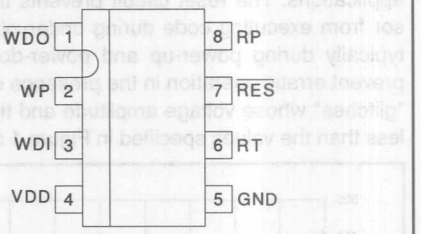
ABSOLUTE MAXIMUM RATINGS

VIN. 5.5V
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

Currents are positive into, negative out of the specified terminal. Consult Packaging Section of the Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

SOIC-8, TSSOP-8 (Top View)
D Package, PW Package



ELECTRICAL CHARACTERISTICS: Unless otherwise specified, VDD = 2V to 5.5V for UCC3946, VDD = 2.2V to 5.5V for UCC2946 and UCC1946; TA = 0°C to 70°C for UCC3946, –40°C to 85°C for UCC2946, and –55°C to 125°C for UCC1946. TA = TJ.

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
		UCC3946			UCC1946 & UCC2946			
Operating Voltage		2		5.5	2.2		5.5	V
Supply Current			10	15		12	18	µA
Minimum VDD	(Note 1)			1			1	V
Reset Section								
Reset Threshold	VDD Rising	1.21	1.235	1.26	1.15	1.235	1.26	V
Threshold Hysteresis			15			15		mV
Input Leakage				5			5	nA
Output High Voltage	ISOURCE = 2mA	VDD - 0.3			VDD - 0.3			V
Output Low Voltage	ISINK = 2mA			0.1			0.1	V
	VDD = 1V, ISINK = 20uA			0.3			0.6	V
VDD to Output Delay	VDD = -1mV/µs (Note 2)		50			50		µs
Reset Period	CRES = 80nF	160	200	240	140	200	260	ms
Watchdog Section								
Watchdog Period	CWD = 80nF	1.28	1.6	1.92	1.12	1.6	2.08	s
Watchdog Pulse Width		20			20			ns
Output High Voltage	ISOURCE = 2mA	VDD - 0.3			VDD - 0.3			V
Output Low Voltage	ISINK = 2mA			0.1			0.1	V
	VDD = 1V, ISINK = 20mA		0.3			0.6	V	

Note 1: This is the minimum supply voltage where $\overline{RES}$ is considered valid.
Note 2: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

GND: Ground reference for the IC.

$\overline{RES}$: This pin is high only if the voltage on the RT has risen above 1.235V. Once RT rises above the threshold, this pin remains low for the reset period. This pin will also go low and remain low if the RT voltage dips below 1.235V for an amount of time determined by Figure 1.

RT: This input compares its voltage to an internal 1.25V reference. By using external resistors, a user can program any reset threshold he wishes to achieve.

RP: This pin allows the user to program the reset period by adjusting an external capacitor.

VDD: Supply voltage for the IC.

WDI: This pin is the input to the watchdog timer. If this pin is not toggled or strobed within the watchdog period, $\overline{WDO}$ is asserted.

$\overline{WDO}$: This pin is the watchdog output. This pin will be asserted low if the WDI pin is not strobed or toggled within the watchdog period.

WP: This pin allows the user to program the watchdog period by adjusting an external capacitor.

APPLICATION INFORMATION

The UCC3946 supervisory circuit provides accurate reset and watchdog functions for a variety of microprocessor applications. The reset circuit prevents the microprocessor from executing code during undervoltage conditions, typically during power-up and power-down. In order to prevent erratic operation in the presence of noise, voltage "glitches" whose voltage amplitude and time duration are less than the values specified in Figure 1 are ignored.

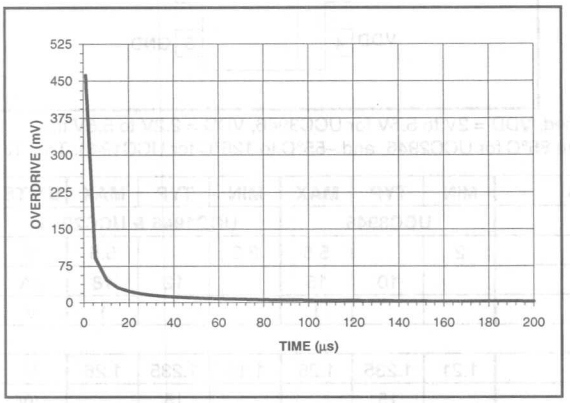


Figure 1. Typical Glitch Supression for the UCC3946

The watchdog circuit monitors the microprocessor's activity, if the microprocessor does not toggle WDI during the programmable watchdog period $\overline{WDO}$ will go low, alerting the microprocessor's interrupt of a fault. The $\overline{WDO}$ pin is typically connected to the non-maskable input of the microprocessor so that an error recovery routine can be executed.

Programming the Reset Voltage and Reset Period

The UCC3946 allows the reset trip voltage to be programmed with two external resistors. In most applications VDD is monitored by the reset circuit, however, the design allows voltages other than VDD to be monitored. Referring to Figure 2, the voltage below which reset will be asserted is determined by:

$$V_{RESET} = 1.235 \bullet \frac{R1 + R2}{R2}$$

In order to keep quiescent currents low, resistor values in the megaohm range can be used for R1 and R2. A manual reset can be easily implemented by connecting a momentary push switch in parallel with R2. $\overline{RES}$ is guaranteed to be low with VDD voltages as low as 1V. Once VDD rises above the programmed threshold, $\overline{RES}$ remains low for the reset period defined by:

$$T_{RP} = 2.5 \bullet C_{RP}$$

where T_{RP} is time in milliseconds and C_{RP} is capacitance in nanofarads. C_{RP} is charged with a precision current source of 500nA, a high quality, low leakage capacitor (such as an NPO ceramic) should be used to maintain timing tolerances. Figure 3 illustrates the voltage levels and timings associated with the reset circuit.

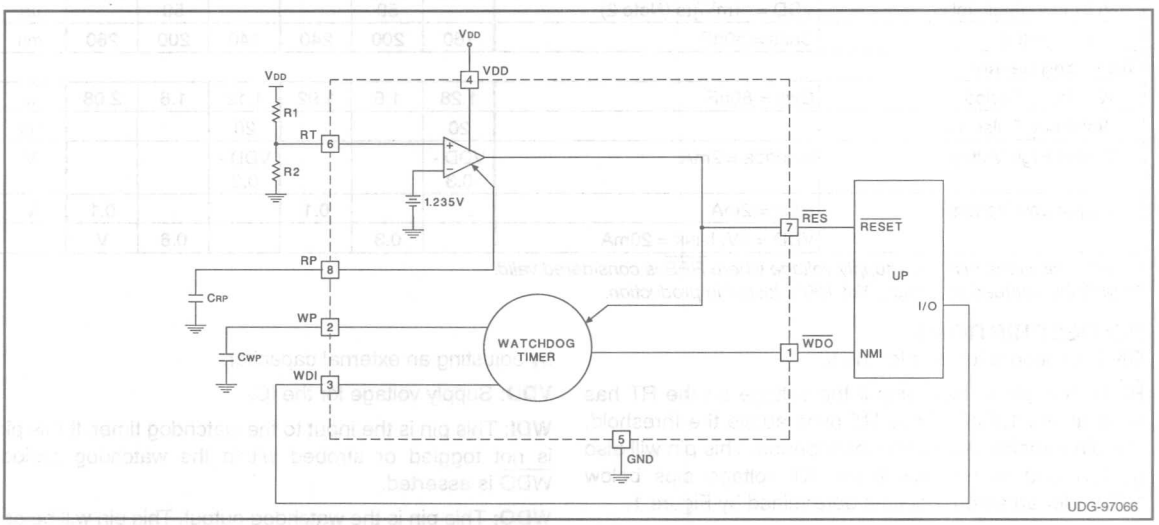
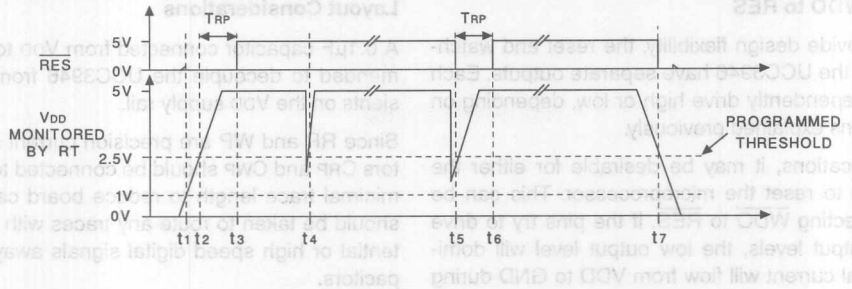


Figure 2. Typical Application Diagram

APPLICATION INFORMATION (cont.)



t1: VDD > 1V, $\overline{RES}$ is guaranteed low.

t2: VDD > programmed threshold, $\overline{RES}$ remains low for TRP.

t3: TRP expires, $\overline{RES}$ pulls high.

t4: Voltage glitch occurs, but is filtered at the RT pin, $\overline{RES}$ remains high.

t5: Voltage glitch occurs whose magnitude and duration is greater than the RT filter, $\overline{RES}$ is asserted for TRP.

t6: VDD dips below threshold (minus hysteresis), $\overline{RES}$ is asserted.

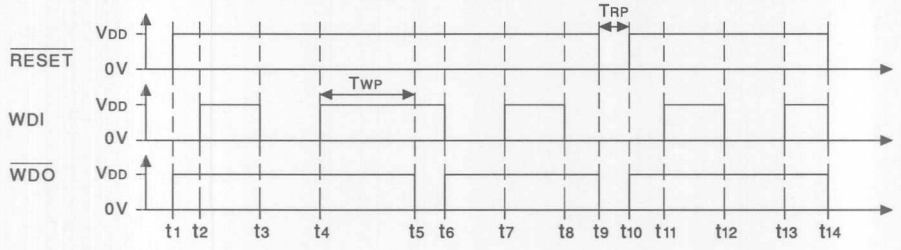
Figure 3. Reset Circuit Timings

Programming the Watchdog Period

The watchdog period is programmed with CWP as follows:

$$TWP = 20 \bullet CWP$$

where TWP is in milliseconds and CWP is in nanofarads. A high quality, low leakage capacitor should be used for CWP. The watchdog input WDI must be toggled with a high/low or low/high transition within the watchdog period to prevent $\overline{WDO}$ from assuming a logic level low. $\overline{WDO}$ will maintain the low logic level until WDI is toggled or $\overline{RES}$ is asserted. If at any time $\overline{RES}$ is asserted, $\overline{WDO}$ will assume a high logic state and the watchdog period will be reinitiated. Figure 4 illustrates the timings associated with the watchdog circuit.



t1: Microprocessor is reset, $\overline{WDO}$ pulls high.

t2: WDI is toggled some time after reset, but before TWP expires.

t3: WDI is toggled before TWP expires.

t4: WDI is toggled before TWP expires.

t5: WDI is not toggled before TWP expires and $\overline{WDO}$ asserts low, triggering the microprocessor to enter an error recovery routine.

t6: The microprocessor's error recovery routine is executed and WDI is toggled, reinitiating the watchdog timer.

t7: WDI is toggled before TWP expires.

t8: WDI is toggled before TWP expires.

t9: $\overline{RES}$ is momentarily triggered, $\overline{RES}$ and $\overline{WDO}$ assert low for TRP.

t10: Microprocessor is reset, $\overline{RES}$ pulls high.

t11: WDI is toggled some time after reset, but before TWP expires.

t12: WDI is toggled before TWP expires.

t13: WDI is toggled before TWP expires.

t14: VDD dips below the reset threshold $\overline{RES}$ and $\overline{WDO}$ are asserted.

Figure 4. Watchdog Circuit Timings

APPLICATION INFORMATION (cont.)

Connecting $\overline{WDO}$ to $\overline{RES}$

In order to provide design flexibility, the reset and watchdog circuits in the UCC3946 have separate outputs. Each output will independently drive high or low, depending on circuit conditions explained previously.

In some applications, it may be desirable for either the $\overline{RES}$ or $\overline{WDO}$ to reset the microprocessor. This can be done by connecting $\overline{WDO}$ to $\overline{RES}$. If the pins try to drive to different output levels, the low output level will dominate. Additional current will flow from VDD to GND during these states. If the application cannot support additional current (during fault conditions), $\overline{RES}$ and $\overline{WDO}$ can be connected to the inputs of an OR gate whose output is connected to the microprocessor's reset pin.

Layout Considerations

A 0.1µF capacitor connected from V_{DD} to GND is recommended to decouple the UCC3946 from switching transients on the V_{DD} supply rail.

Since RP and WP are precision current sources, capacitors C_{RP} and C_{WP} should be connected to these pins with minimal trace length to reduce board capacitance. Care should be taken to route any traces with high voltage potential or high speed digital signals away from these capacitors.

Resistors R1 and R2 generally have a high ohmic value, traces associated with these parts should be kept short in order to prevent any transient producing signals from coupling into the high impedance RT pin.

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Lithium-Ion Battery Monitor

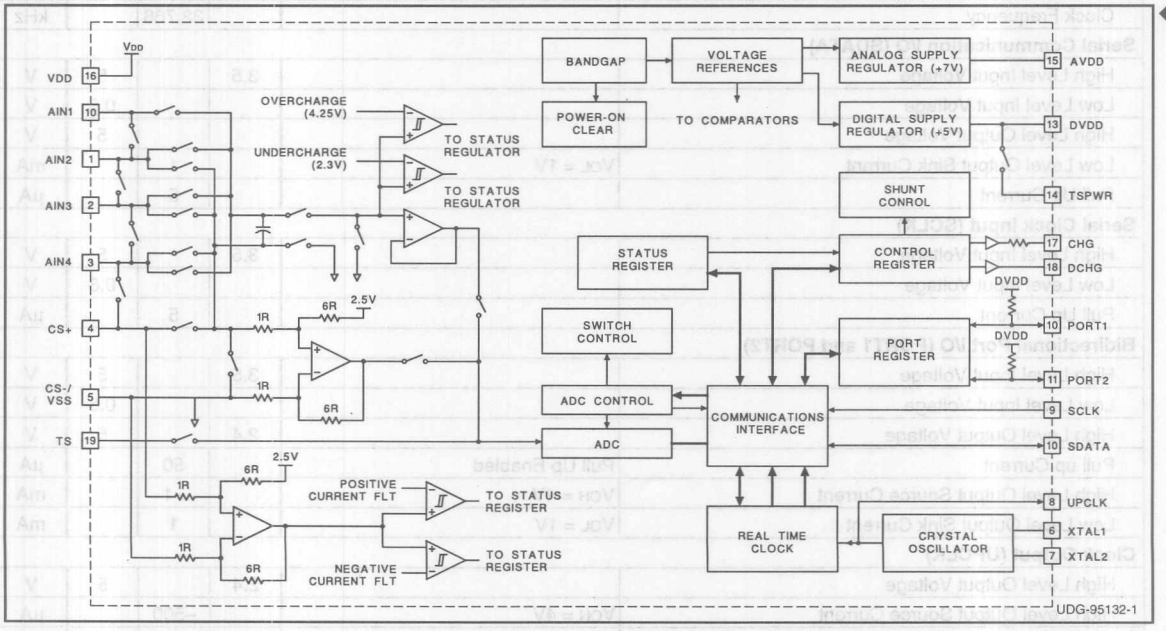
FEATURES

- Measures Individual Cell Voltage for Three or Four Lithium-Ion Cells
- Measures Battery Pack Current and Temperature
- 10 Bit A/D with Microprocessor Interface
- Hardware Overcharge, Over-Discharge, and Overcurrent Protection
- Communications Interface for Optional External EEPROM
- Two Year Real Time Clock
- Regulated 5V Microprocessor Supply

DESCRIPTION

The UCC3951 is a monolithic BCDMOS integrated circuit designed to reside inside a battery pack and measure under host microprocessor control any combination of battery parameters, such as cell voltage, pack current, and pack temperature. The UCC3951 is designed for the unique charging and safety concerns associated with lithium-ion cells, and includes protection features such as programmable current shunts for individual cell charge equalization, hardware monitoring of individual cell voltage and pack current, and isolation of the cells from charge and/or discharge currents.The UCC3951 is intended to be paired with a simple, low-cost host microprocessor such as an 80C51, that resides either inside or outside the battery pack. If the microprocessor is external to the pack, an optional serial EEPROM can be used inside the pack to retain battery information, such as number of cycles, pack serial numbers, or system calibration constants. The UCC3951 provides the clock to the host microprocessor and a regulated power source to the host, EEPROM and the thermistor. Operation of the 32kHz crystal during sleep mode consumes only 25µA. A real-time clock is provided to log elapsed time, which along with a recorded temperature profile, can be used to calculate battery self-discharge.The UCC3951 monitors the individual cell voltage of three or four series-connected lithium-ion cells and provides individual cell shunt capability under microprocessor control to maintain balanced charge between cells. The UCC3951 can also drive two external high-side P-channel power MOSFETs to disconnect the cells from either the charging supply, the load, or both. For accurate cell voltage readings near full charge, a factory trimmed bandgap voltage reference in conjunction with software calibration constants stored in external memory limits overall system measurement error to 1% at 4.2V.

BLOCK DIAGRAM



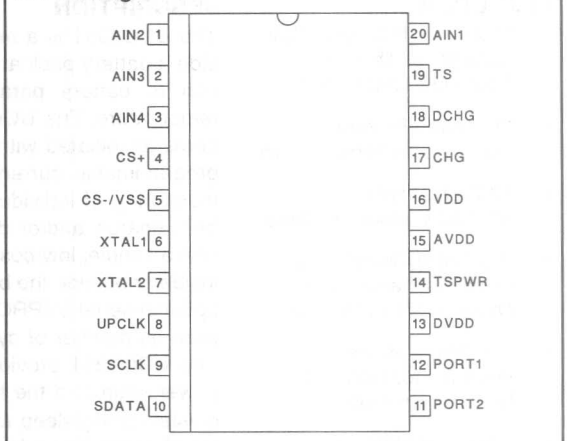
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ABSOLUTE MAXIMUM RATING

VDD 20V
All other pins..... VSS – 0.6V to VDD + 0.5V
Maximum Shunt Current 100mA
Maximum Power Dissipation 1000mW
Storage Temperature Range ..... –65°C to +150°C
Junction Temperature ..... –55°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Currents are positive into, negative out of the specified terminal.
Consult Packaging Section of the Databook for thermal limitations and consideration of packages.

CONNECTION DIAGRAM

SOIC-20 (Top View)
DW Package



ELECTRICAL CHARACTERISTICS: Unless otherwise stated, VDD = 14V, no load on any output, and ambient temperature T_A = 0°C to 70°C. $T_A = T_J$.

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
Overall					
Supply Voltage	Active Mode	7.2		18	V
	Monitor Mode	6.5		18	V
Supply Current	Active Mode		5		mA
	Monitor Mode		200		µA
	Sleep Mode		20	25	µA
Clock Frequency			32.768		kHz
Serial Communication I/O (SDATA)					
High Level Input Voltage		3.5		5	V
Low Level Input Voltage				0.8	V
High Level Output Voltage				5	V
Low Level Output Sink Current	V_{OL} = 1V		1		mA
Pull Up Current			5		µA
Serial Clock Input (SCLK)					
High Level Input Voltage		3.5		5	V
Low Level Input Voltage				0.8	V
Pull Up Current			5		µA
Bidirectional Port I/O (PORT1 and PORT2)					
High Level Input Voltage		3.5		5	V
Low Level Input Voltage				0.8	V
High Level Output Voltage		2.4		5	V
Pull up Current	Pull Up Enabled		50		µA
High Level Output Source Current	V_{OH} = 4V		–1		mA
Low Level Output Sink Current	V_{OL} = 1V		1		mA
Clock Output (UPCLK)					
High Level Output Voltage		2.4		5	V
High Level Output Source Current	V_{OH} = 4V		–500		µA
Low Level Output Sink Current	V_{OL} = 1V		500		µA

ELECTRICAL CHARACTERISTICS (cont.): Unless otherwise stated, VDD = 14V, no load on any output, and ambient temperature T_A = 0°C to 70°C. T_A = T_J.

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
FET Drive Output (CHG)					
High Level Output Voltage		2.4		5	V
High Level Output Sink Current	V_{OH} = 4V		–2		mA
Low Level Output Sink Current	V_{OL} = 1V		2		mA
FET Drive Output (DCHG)					
High Level Output Voltage		2.4		18	V
High Level Output Source Current	V_{OH} = 6.2V, VDD = 7.2V		–5		mA
Low Level Output Sink Current	V_{OL} = 1V		80		µA
Regulator Output (DVDD)					
Output Voltage	0 < I_{LOAD} < 15mA	4.75	5	5.25	V
Output Current				–15	mA
Thermistor Supply (TSPWR)					
Output Voltage		4.75	5	5.25	V
Output Current				–1	mA
Current Shunts (AIN1- AIN4)					
Shunt Current Capability			50	100	mA
On Resistance	V_{DS} = 2.4V, VDD = 7.2V, ID = 50mA			10	Ω
Leakage Current	Sleep Mode, V_{AINX} = 4.2V		TBD		µA
Analog to Digital Converter					
Input Voltage Range		0		5.11	V
Overall Slope (Gain) Error	Nominal Slope of 1 Bit = 5mV	–5		5	%
Gain Drift Over Temperature	T_A = 0°C to 70°C	–1		1	%FS
Offset Error	V_{ADC} = 0V	–1		1	%FS
Integral Linearity	V_{ADC} = 0.2V to 4.9V		TBD		%FS
Differential Amplifier: Current Measurement					
Current Sense Gain	CS+ = 100mV		6		V/V
Current Sense Reference Voltage	Autozero Enabled		2.5		V
Common Mode Voltage Range		–0.6		1	V
Voltage References					
Overvoltage Fault Threshold		4.18	4.25	4.32	V
Undervoltage Fault Threshold		2.2	2.3	2.4	V
Positive Current Fault Threshold	At CS+		350	400	mV
Negative Current Fault Threshold	At CS+	–400	–350		mV
Bus Timing					
Clock Frequency	See Bus Time Out			500	kHz
Clock High Time		500			ns
Clock Low Time		500			ns
SDATA and SCLK Rise Time				25	ns
SDATA and SCLK Fall Time				25	ns
Start Condition Setup Time		50			ns
Stop Condition Setup Time		50			ns
Start Condition Hold Time		50			ns
Data Input Setup Time		50			ns
Data Input Hold Time		50			ns
Data Output Hold Time				0	ns

ELECTRICAL CHARACTERISTICS (cont.): Unless otherwise stated, VDD = 14V, no load on any output, and ambient temperature T_A = 0°C to 70°C. T_A = T_J.

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
Bus Timing					
Data Low Output Valid From Clock	C_{LOAD} = 50pF, I_{EXT_PU} = 300µA			200	ns
Bus Time Out		250		500	ms
Bus Free Time		50			ns
ADC Measurement					
Conversion Time	ADC is Powered Up	62.5		187.5	ms
Time From ADC Power Up to Conversion Complete		125		250	ms
Time From Conversion Complete to ADC Power Down		1		2	s
Monitor Mode					
Cycle Time (AIN1 to AIN4)	Cell Voltage Monitoring		4		ms
Current Fault Response Time	Positive/Negative Current Fault	122		244	µs
Time From Sleep Mode Disable to Monitor Mode Enable		488		976	µs

PIN DESCRIPTIONS

AIN1: This input pin serves as the current shunt connection to the positive terminal of the top cell in the series stack. The pin is also the positive terminal connection for the differential voltage measurement of the top cell. If there are only three cells in series, then this pin should be tied to AIN2.

AIN2: This input pin serves as the current shunt connection to the positive terminal of the second cell in the series stack. The pin is also the positive terminal connection for the differential voltage measurement of the second series cell, or the negative terminal connection for the differential voltage measurement of the first cell.

AIN3: This input pin serves as the current shunt connection to the positive terminal of the third cell in the series stack. The pin is also the positive terminal connection for the differential voltage measurement of the third series cell, or the negative terminal connection for the differential voltage measurement of the second cell.

AIN4: This input pin serves as the current shunt connection to the positive terminal of the fourth cell in the series stack. The pin is also the positive terminal connection for the differential voltage measurement of the fourth series cell, or the negative terminal connection for the differential voltage measurement of the third cell.

AVDD: A 10µF capacitor on this pin provides compensation and decoupling for the internal analog supply regulator.

CHG: This current-limited output pin drives an external low-side small signal bipolar transistor or MOSFET that in turn drives a high-side P-channel power MOSFET. The FET is used to disconnect the series stack of lithium-ion cells from the charging supply. The FET can be used in tandem with a second P-MOSFET, driven by DCHG, to disconnect the cells from the charging input and/or the load.

CS+: This input pin is the positive connection for a ground referenced differential current sense amplifier. The current is measured as a voltage drop across a sense resistor. The pin is also the negative terminal of the battery pack.

CS-/VSS: This pin is both the supply ground for this device as well as the negative connection for the differential current sense input. The pin should have a solid star-point ground connection to the negative terminal of the bottom cell in the stack.

DCHG: This high-voltage output pin drives an external high-side P-channel power MOSFET. The FET is used to disconnect the series stack of lithium-ion cells from the load. The pin can be used in tandem with a second FET, driven by CHG, to disconnect the cells from the charging input and/or the load.

DVDD: The output of this pin is a regulated 15mA, +5V supply from an internal linear regulator for use in powering external components, such as the system host microprocessor, as well as the internal digital circuitry. A 10µF capacitor on this pin provides compensation and decoupling for the digital supply regulator.

PORT1, PORT2: These two pins are configurable bidirectional I/O ports controlled by bits in the Port Register. They can be used to communicate with a two-wire serial EEPROM. The pins have 50µA pull ups that can be enabled or disabled when the pin is driven externally.

SCLK: This pin is an input port used to clock serial data into and out of the UCC3950. The state of SDATA is latched whenever SCLK receives a logic high data strobe (clock pulse). The pin has a weak 5µA internal pull up to

PIN DESCRIPTIONS

prevent glitches on the pin when the pack is removed from an external host.

SDATA: The SDATA pin is a bidirectional pin used for transmitting to or receiving serial data from the system host. The pin has an open source output and relies on an external pull up provided by the host. A weak 5µA internal pull up prevents glitches on the pin when the pack is removed from an external host. The serial communications protocol is described in the Serial Communications Interface section.

TS: This temperature sense pin provides an input to the ADC for battery pack temperature measurements via an external temperature sensor.

TSPWR: This output provides a switched +5V supply to external components, such as a temperature sensor or a serial EEPROM. The on/off switch is controlled by bit 7 in the Command Register, and must be active before a temperature measurement is made. Otherwise, TSPWR should be turned off to conserve battery capacity.

UPCLK: This output pin provides a 32.768kHz clock for the external host microprocessor. The clock is always present on this pin.

VDD: This pin is the power supply connection for the UCC3951. The connection to VDD must be made at the top of the series stack of cells.

XTAL1: This pin is used together with XTAL2 as the connection to the 32.768kHz crystal used for on-chip timing and the real-time clock.

XTAL2: This pin is used together with XTAL1 as the connection to the 32.768kHz crystal used for on-chip timing and the real-time clock.

APPLICATION INFORMATION

The UCC3951 has three modes of operation to provide continuous protection against current or voltage conditions outside the specifications of a lithium-ion cell while keeping power consumption to a minimum.

In the primary mode of operation, the "monitor" mode, the UCC3951 cycles through the cell voltages, constantly checking each cell for overvoltage and undervoltage faults. Charge and discharge currents are also continuously monitored to guard against short circuits across the pack terminals.

If a host requests an ADC measurement, the UCC3951 temporarily interrupts the monitoring sequence and enters an "active" mode, during which a conversion on a cell voltage is made. Once the conversion is complete, the UCC3951 reenters the monitor mode. Charge and discharge currents are still watched during the active mode, and while servicing any other command, the UCC3951 continues to monitor the cell voltages.

If both of the external FETs are opened via a host command, effectively isolating the cells from charge or discharge currents, the UCC3951 enters a power saving "sleep" mode. No monitoring of voltage or current occurs during sleep, however any command to close any one of the external FETs will restart the monitoring sequence.

MONITOR MODE

The UCC3951 always monitors the cell voltages except when the IC is

1. Making an ADC measurement (current, autozero, temperature or a cell voltage), or
2. Placed into sleep mode.

The UCC3951 continues to monitor cell voltages even if an overvoltage or undervoltage fault has already occurred, since energy may still be added or removed from the battery pack. Overcurrent conditions are always monitored, even during ADC measurements, but they are not checked when the IC is in sleep mode.

Three or Four Cells

The UCC3951 checks for overvoltage and undervoltage faults on a default number of four cells. If only three cells are used, AIN1 must be connected to AIN2 and bit 5 of Command Register 3 must be set so that an inadvertent fault condition does not occur by checking for a cell that is not present. If bit 5 is set, monitoring for overvoltage and undervoltage conditions on cell #1 is not done, although measurement of that cell is possible.

Voltage Monitoring

The UCC3951 uses a flying capacitor to monitor each individual cell for an overvoltage and an undervoltage condition. The UCC3951 cycles through each one of the four cells beginning with the cell connected to AIN1 and ending with the cell connected to AIN4. For each cell, a sequence of switches transfers the differential cell voltage to a capacitor. The cell voltage on the capacitor is then transferred to a ground referenced value and compared to both an overvoltage and an undervoltage reference.

Overvoltage Fault

An overvoltage condition exists if any individual cell voltage is greater than the overvoltage limit (4.25V/cell). As

APPLICATION INFORMATION (cont.)

a result of the fault, a bit is set in the Status Register 1 that indicates which cell is exhibiting the overvoltage condition, and CHG is driven low so that the external P-MOSFET is opened (via an external pull up and transistor), cutting off the charging current. The overvoltage fault may be cleared by discharging the battery so that the cell voltage drops into a normal operating range. The bit displaying the fault will also be cleared. Command Register 3 bit 9 will reflect the change in the CHG pin status if the external FET is opened. The host cannot overwrite this bit (that is, close the FET) until the UCC3951 senses that the overvoltage condition is removed either through the monitor mode or through a cell voltage measurement. If an overvoltage condition occurs, the external FET is opened immediately. However, the event is not latched into Status Register 1 until 30µs later. In dynamic loading situations, where a smart charger is both charging a battery and powering a load, it may be possible for an overvoltage condition to appear, cause the external FET to open, and then disappear due to the load demand before the condition is latched into the Status Register.

Undervoltage Fault

An undervoltage condition exists if any individual cell voltage is less than the undervoltage limit (2.3V/cell). As a result of the fault, a bit is set in Status Register 1 that indicates which cell is exhibiting the undervoltage condition, and the DCHG pin is driven high so that the external P-MOSFET is opened, cutting off the discharge current. The undervoltage fault may be cleared by charging the battery so that the cell voltage rises into a normal operating range. The bit displaying the fault will also be cleared. Command Register 3 bit 8 is set if the DCHG pin status if the external FET is opened. The host cannot overwrite this bit (that is, close the FET) until the UCC3951 senses that the undervoltage condition is removed either through the monitor mode or through a cell voltage measurement. Note that both an overvoltage and an undervoltage fault must never exist at the same time. If both faults do exist, the FETs connected to the CHG and DCHG pins will be forced open and sleep mode will occur. The host will be unable to override either pin, and sleep mode will prevent the UCC3951 from detecting if the condition is removed. The IC must be powered down to clear the fault.

Current Monitoring

Current flowing into or out of the battery pack is constantly monitored for excessive charge or discharge levels. The overcurrent threshold is set at ±350mV at the CS+ pin relative to the CS-/VSS pin (about ±7A based on a 0.05Ω external sense resistor) and is gained up and referenced to 2.5V to allow measurement of both charge and discharge current. The voltage across the sense resistor is measured as:

$$V_{SENSE} = (V_{CS+} - V_{CS-}) \bullet A + V_R$$

where A is the amplifier gain (x6), and V_R is an internal 2.5V reference voltage. Thus the positive current fault is set internally at 4.6V (+0.35 • 6 + 2.5V), and the negative current fault is set internally at 0.4V (–0.35 • 6 + 2.5V).

Overcurrent Fault

If an overcurrent fault exists, a bit is set in Status Register 1 indicating that a fault exists, and the CHG output is driven low and DCHG is driven high so that both of the external FETs are opened after a 122µsec to 244µsec delay. Bits 8 and 9 in Command Register 3 are set reflecting CHG and DCHG status if the external FETs are opened. The UCC3951 will also enter a low current sleep mode as a result of the opening of the FETs to conserve battery capacity.

To clear an overcurrent response, the host microprocessor must acknowledge that the fault exists by clearing bit 1 or 0 in Status Register 1 before control of bits 8 and 9 in Command Register 3 closing the external FETs are returned to the host.

SLEEP MODE

The UCC3951 enters a low power sleep if the external FETs are opened by setting bits 8 and 9 in Command Register 3. Those bits may be set by,

1. A host command, or
2. A positive or negative overcurrent fault, or
3. An overvoltage fault if the external FET on the DCHG pin is already open, or
4. An undervoltage fault if the external FET on the CHG pin is already open.

All functions except the oscillator, real-time clock, low current bandgap, and the digital supply regulator are turned off to conserve power. All commands, such as those to measure temperature, voltage, or current are still available, however some additional power up time is required. No monitoring of voltage or current occurs during sleep since the battery pack is isolated by the open external P-MOSFETs. If a host command closes either one of the FETs, the UCC3951 awakes from sleep mode and restarts the voltage and current monitoring after a brief power up time of 976µs

APPLICATION INFORMATION (cont.)

ACTIVE MODE

Writing to bits 7 - 9 in ADC Control Register 0 places the UCC3951 into active mode and kicks off an analog-to-digital conversion. Once the bits have been written to, they are locked out until the conversion is complete (that is, new ADC commands are ignored until the previous one finishes). After the conversion ends, bits 7 - 9 are cleared.

While the conversion is ongoing, the ADC Busy flag (bit 6 in ADC Control) is set. The active mode status can be observed via bit 5 of ADC Control Register 0, which is set while the ADC is powered on.

Differential Cell Voltage Measurement

A novel dual flying capacitor design is used to accurately measure the voltage across a cell for use in an algorithm controlled charge termination. This design approach allows the use of an integrating ADC while preventing measurement errors due to any charge leakage. A sequence of switch closings and openings first transfers the cell voltage to one capacitor, and then to the ADC. While the conversion begins on the first capacitor, a second capacitor is switched across the same cell and then back to the ADC. The conversion continues on the second capacitor, allowing the first capacitor to be recharged across the cell. The sequence is continued until the conversion is completed. All switches are then opened for the next measurement.

Autozero Current Sense Amplifier

For accuracy, a calibration sequence to measure offsets should be performed by the host before every current measurement. A host command to ADC Control Register 0 to autozero the current sense amplifier opens switches to CS+ and CS- and closes the amplifier inputs to ground. A conversion measures the internal 2.5V reference. This calibration value can be subtracted from a current measurement. When the conversion is complete, all switches are opened again.

Differential Current Measurement

Pack current is measured as a voltage drop across the sense resistor, and is referenced to 2.5V to allow measurement of both charge and discharge current. When the current is measured, switches connecting the current sense amplifier across the sense resistor are closed. The voltage across the sense resistor is measured as:

$$V_{SENSE} = (V_{CS+} - V_{CS-}) \bullet A + V_R$$

where A is the amplifier gain (x6), and V_R is the 2.5V reference voltage. The sense resistor voltage will be the difference between the reference and the actual reading.

Temperature Measurement

The temperature sense supply (TSPWR) is switched on only when requested by setting bit 7 in Command Register 3. A precision IC temperature sensor can be placed between this pin and ground, with its output connected to TS.

If a thermistor is used, it should be connected between TSPWR (+5V) and a fixed resistor to ground. The voltage across the fixed resistor can be measured with the ADC via TS which is ground referenced internally. The voltage on the fixed resistor will increase with temperature, and dropping most of the voltage across the fixed resistor will reduce thermistor self-heating for improved accuracy.

Thermistors come in many different types and styles, but a common type used in battery pack applications are bead type or axial-lead thermistors with a typical value of 10kΩ at 25°C. Using a voltage divider consisting of a 10kΩ fixed resistor and a 10kΩ at 25°C thermistor in a configuration shown in Figures 3 and 4, a relatively linear change in voltage with temperature is developed at TS.

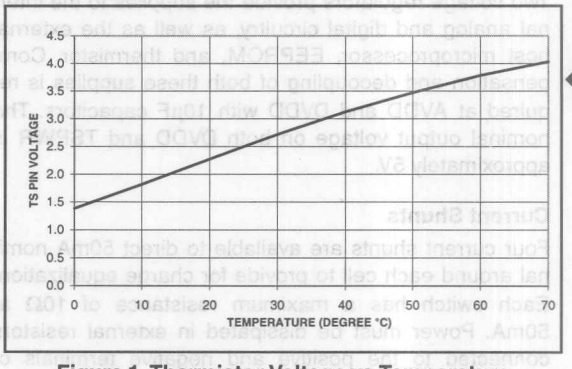


Figure 1. Thermistor Voltage vs Temperature

Analog To Digital Converter (ADC)

The ADC is used for measurement of the individual cell voltages, battery pack temperature and pack current. An ADC measurement is made whenever a combination of bits 7 - 9 in ADC Control Register 0 are set. The ADC has 10 bit resolution, and the design is based on a delta-sigma modulator. A pulse density modulated one-bit stream representing the measured voltage is integrated in a counter that can be read via ADC Conversion Register 4. The conversion complete status can be polled by the host via bit 6 in ADC Control Register 0.

APPLICATION INFORMATION (cont.)

To conserve energy, the ADC powers itself on whenever an ADC measurement is requested, and it powers itself down within 1 to 2 seconds after the last conversion (unless, of course, a measurement is requested within that time). The power up status can be checked with bit 5 in ADC Control Register 0.

If the real-time clock is stopped (via bit 8 in Register 5) while the ADC is powered on, then the ADC will remain powered on. When the timer is released, the ADC will power down 1 to 2 seconds later.

Voltage References

The UCC3951 contains a temperature stable on-chip bandgap voltage reference that is used by the ADC, voltage and current monitoring references, and the linear voltage regulators. Due to the accuracy requirements for the voltage readings of lithium-ion cells, the bandgap is trimmed to better than ±1%. The voltage monitoring references are derived from the bandgap, and are set at 4.25V for the overvoltage fault and 2.3V for the undervoltage fault. The current monitoring references are set at 4.6V for the positive current fault and 0.4V for the negative current fault.

Linear Voltage Regulators

Two voltage regulators provide the supplies to the internal analog and digital circuitry, as well as the external host microprocessor, EEPROM, and thermistor. Compensation and decoupling of both these supplies is required at AVDD and DVDD with 10µF capacitors. The nominal output voltage on both DVDD and TSPWR is approximately 5V.

Current Shunts

Four current shunts are available to direct 50mA nominal around each cell to provide for charge equalization. Each switch has a maximum resistance of 10Ω at 50mA. Power must be dissipated in external resistors connected to the positive and negative terminals of each cell. If shunts are not required in the application, the resistors shown in Figures 3 and 4 are not necessary.

Control of each shunt is done via bits 1 - 4 in Command Register 3. If a shunt is closed, overvoltage and undervoltage monitoring of that cell is ignored, although a measurement of the cell is possible. If an overvoltage or undervoltage fault occurs on a cell and that cell is then shunted, the fault condition will not be cleared since the cell is not monitored.

Only one cell should be shunted at any one time, although shunting more than one is allowed. While charging the battery, the cell with the highest voltage as measured with the ADC should be shunted first. Conversely, on discharge, the cell with the lowest voltage should be shunted first.

External MOSFET Drivers

The CHG and DCHG pins drive external P-MOSFETs that are used to isolate the series stack of cells from the charging supply and load. The P-MOSFET connected to the charging supply must be driven with a low side small signal bipolar or MOSFET (the CHG output is a current limited output.) The P-MOSFET with its gate pulled up by the stack of cells is driven directly by the DCHG pin.

Crystal Oscillator

A low current 32.768kHz crystal oscillator provides the clock to the internal logic, as well as to the host microprocessor. The clock is active even during sleep mode so that the UCC3951 can respond to host commands.

Real-Time Clock

A 26-bit real-time clock is available to log parameters such as storage time. The clock is updated every second. Twenty-six bits provides more than two years of elapsed time measurement for extended battery pack storage periods. The real-time clock can be cleared via bit 0 in the Command Register. If more than two years elapse, bit 7 in the Real-Time Clock Register 5 is set, and the real-time clock overflows. The real-time clock is broken up into three 10-bit registers. Reading all three registers requires a separate Read Data command for each register. To prevent the clock from updating while the registers are read, the following sequence should be used:

1. Set the Stop Timer bit 8 in the Real-Time Clock Register 5. This action halts the clock, and stores up to one second of elapsed time during which the real-time clock can be read.
2. Read all three real-time clock registers in one second.
3. Clear the Stop Timer bit to restart the real-time clock and to update the clock by the stored elapsed time.

Note that if the Stop Timer bit is not cleared, the timer stays halted. Also note that if it takes the host longer than one second to complete the sequence, the real-time clock will be inaccurate.

Bidirectional I/O Ports

Two pins (PORT1, PORT2) are provided for use as bidirectional ports under host control. Six bits in Port Regis-

APPLICATION INFORMATION (cont.)

ter 2 provide control over the direction of data flow, the value of the bit to be sent, and whether a pull up should be engaged to pull the pin high when data is not being sent. All input or output data uses +5V to equal a logic high.

When reading the ports configured as inputs, the value returned to the host represents the state of the pin, not the values in the Port Register 2. When reading the ports configured as outputs, the value returned to the host is the same as the value in the Port Register 2.

If these ports are used as an EEPROM interface, a standard two wire bidirectional interface can be implemented using one port as clock and the second port as data. Open collector outputs are typically used on EEPROMs, so the pull ups on the ports may be engaged.

Serial Communications Interface

The UCC3951 supports a bidirectional two wire bus and serial data transmission protocol for communicating with a host microprocessor. The bus is controlled by the host. Since the clock speed of the host microprocessor may be unknown, a clock pulse on SCLK must accompany each data bit on SDATA. The SCLK clock may operate asynchronous from the UCC3951 clock. All input clock and data or output data uses +5V to equal a logic high.

The data protocol is defined as follows (see also Figure 4).

BIT	DRIVEN BY	DATA CONTENT
X	Host	Start Configuration
0	Host	Read/Write (R/W) Direction Bit 1 for READ, 0 for WRITE
1	Host	Register Address Bit 2 (MSB)
2	Host	Register Address Bit 1
3	Host	Register Address Bit 0 (LSB)
4	WRITE: Host READ: UCC3951	Data Bit 9 (MSB) from Addressed Register
5 - 12	WRITE: Host READ: UCC3951	Data Bit 8 to 1 from Addressed Register
13	WRITE: Host READ: UCC3951	Data Bit 0 (LSB) from Addressed Register
X	Host	Stop Condition

Two commands are available to move data to or from the UCC3951. They are:

1. Read Data (from the UCC3951)
2. Write Data (to the UCC3951)

The host determines which command is activated via a Read/Write (R/W) direction bit included in every data transmission. Read Data or Write Data commands are always 14 bits long, even if the register contains less than 10 bits of data. Any unused or reserved bits should be written with a zero to account for future upgrades. Valid data is indeterminate on unused bits.

Data on SDATA must remain stable whenever SCLK is high. Changes in the data during a high SCLK will be interpreted as a Start or Stop condition. A Start condition must precede a data transmission, and a Stop condition must follow.

Write Data: On a Write Data command, the Stop condition writes the data into the addressed register. The R/W and Address bits are clocked in on the rising edge of SCLK, but the remaining Data bits are clocked in on the falling edge of SCLK.

The Write Data command can be interrupted with an early Stop condition at any time during data transfer. However, if more than 14 bits are inadvertently clocked in (a late Stop condition), the command is canceled. The command is also canceled if a second Start condition is received before a Stop condition.

Read Data: After the R/W and three Address bits of a Read Data command are clocked in, the UCC3951 takes control of the bus to send data to the host. The R/W and Address bits are clocked in on the rising edge of SCLK, but the remaining Data bits are clocked out on the falling edge. The Read Data command can only be canceled before the UCC3951 controls the bus. Once control is taken by the UCC3951, early Stop conditions or repeated Start conditions are ignored. The data of the addressed register must be clocked out via SCLK before the UCC3951 releases control of the bus and a new command can be accepted. If more than 14 bits are clocked out without a Stop command, the extra bits are indeterminate.

If a command is not completed within 250ms, the bus times out and the previous command is terminated. A new Start condition is required before the next command.

APPLICATION INFORMATION (cont.)

Registers

Eight 10-bit wide registers are available for monitoring and controlling the operation of the UCC3951. The ADC Control Register 0 controls ADC measurements and provides the status of the analog to digital converter. The Status Register 1 indicates if any fault conditions have occurred. The Port Control Register 2 writes and reads data on the PORT1 and PORT2 pins. The Command Register 3 provides the control and status of the shunts and the CHG, DCHG and TSPWR pins. The ADC Conversion Result Register 4 is the output of the ADC. The register is overwritten upon the completion of a conversion. The three Real-Time Clock Registers contain the data and control for the real-time clock.

Register Map

ADDRESS	REGISTER
0	ADC Control Register
1	Status Register
2	Port Control Register
3	Command Register
4	ADC Conversion Register
5	Real Time Clock (MSB) and Control Register
6	Real Time Clock Register
7	Real Time Clock (LSB) Register

Register 0: ADC CONTROL

Bit 9	Bit 8	Bit 7	Read/ Write	FUNCTION
0	0	0	R/W	All Channels Open
0	0	1	R/W	Measure Cell #1 Voltage
0	1	0	R/W	Measure Cell #2 Voltage
0	1	1	R/W	Measure Cell #3 Voltage
1	0	0	R/W	Measure Cell #4 Voltage
1	0	1	R/W	Measure Temperature
1	1	0	R/W	Measure Current
1	1	1	R/W	Autozero Current Sense Amplifier
BIT 6			R	ADC Busy (1) / ADC Ready (0)
BIT 5			R	ADC Power On (1) / Off (0)
BIT 4			-	-
BIT 3			-	-
BIT 2			-	-
BIT 1			-	-
BIT 0			-	-

Register 1: STATUS

Bit	Read/ Write	Function
9	R	Overvoltage on Cell #1 (1); Condition Cleared (0)
8	R	Overvoltage on Cell #2 (1); Condition Cleared (0)
7	R	Overvoltage on Cell #3 (1); Condition Cleared (0)
6	R	Overvoltage on Cell #4 (1); Condition Cleared (0)
5	R	Undervoltage on Cell #1 (1); Condition Cleared (0)
4	R	Undervoltage on Cell #2 (1); Condition Cleared (0)
3	R	Undervoltage on Cell #3 (1); Condition Cleared (0)
2	R	Undervoltage on Cell #4 (1); Condition Cleared (0)
1	R/W	Positive Current Fault (1); Condition Cleared (0)
0	R/W	Negative Current Fault (1); Condition Cleared (0)

Register 2: PORT CONTROL

Bit	Read/ Write	Function
9	R/W	Write Out Port #1 (1); Read In Port #1 (0)
8	R/W	Set Port #1 (1); Clear Port #1 (0)
7	R/W	Enable Port #1 pull up (1); Disable Port #1 pull up (0)
6	R/W	Write Out Port #2 (1); Read In Port #2 (0)
5	R/W	Set Port #2 (1); Clear Port #2 (0)
4	R/W	Enable Port #2 pull up (1); Disable Port #2 pull up (0)
3	-	reserved
2	-	reserved
1	-	reserved
0	-	reserved

Register 3: COMMAND

Bit	Read/ Write	Function
9	R/W	CHG Output High (1); CHG Output Low (0)
8	R/W	DCHG Output Low (1); DCHG Output High (0)
7	R/W	TSPWR Output On (1); TSPWR Output Off(0)
6	R/W	Real-Time Clock Reset (1)
5	R/W	Three lithium-ion Cells (1); Four lithium-ion Cells (0)
4	R/W	Shunt Cell #1 Closed (1); Shunt Cell #1 Open (0)
3	R/W	Shunt Cell #2 Closed (1); Shunt Cell #2 Open (0)
2	R/W	Shunt Cell #3 Closed (1); Shunt Cell #3 Open (0)
1	R/W	Shunt Cell #4 Closed (1); Shunt Cell #4 Open (0)
0	-	-

APPLICATION INFORMATION (cont.)

Register 4: ADC CONVERSION RESULT

Bit	Read/ Write	Function
9	R	ADC Conversion MSB
⇓	⇓	⇓
0	R	ADC Conversion LSB

Register 5: REAL-TIME CLOCK (MSB)

Bit	Read/ Write	Function
9	-	Reserved
8	R/W	Stop Timer (1), Start Timer (0)
7	R/W	Overflow of Real-Time Clock (1); Clear Overflow (0)
6	-	-
5	R	Real-Time Clock MSB (Bit 26)
⇓	⇓	⇓
0	R	Real-Time Clock (Bit 20)

Register 6: REAL-TIME CLOCK

Bit	Read/ Write	Function
9	R	Real-Time Clock (Bit 19)
⇓	⇓	⇓
0	R	Real-Time Clock (Bit 10)

Register 7: REAL-TIME CLOCK (LSB)

Bit	Read/ Write	Function
9	R	Real-Time Clock (Bit 9)
⇓	⇓	⇓
0	R	Real-Time Clock LSB (Bit 0)

Figure 3 shows the UCC3951 in a typical three cell battery pack application, incorporating a serial EEPROM to store battery data. The pack communicates with an external processor via the serial data and clock lines. The EEPROM is powered from the switchable TSPWR output to minimize current draw when not being used.

Low RDSON P-channel MOSFET's Q1 and Q2 control the charge and discharge currents respectively. High side switching is used to prevent opening of the ground line, and buffers the UCC3951 from the open-circuit voltage of the battery charger. The ground reference for the UCC3951 is referenced to the top of the current sense resistor to prevent CS+ from going several volts below substrate during a high current discharge pulse. The normal voltage drop between this ground reference and Pack (-) is only a few hundred millivolts maximum.

The gate of Q1 requires level shifting, performed by Q3, to stand off the open circuit charger voltage in the case of a charger fault. This can be done with a small N-channel MOSFET as shown, or with a bipolar transistor such as a 2N2222. The source current of the totem pole CHG output is internally limited to a few milliamps, so no base resistor is required if a bipolar is used. Note that this will increase the current draw whenever Q1 is turned on. Although the body diode will allow discharging with Q1 off, it would normally be turned on during discharge to minimize losses.

The gate of Q2 is driven directly by a totem pole style output, so no gate to source resistor is required. Note, however, that the sink current is internally limited by a 14K resistor. This was done to facilitate slew rate limiting. Adding a series RC from drain to gate will slew rate limit the output voltage of Q2, minimizing surge currents into highly capacitive loads (which may otherwise cause a current fault). An example is shown in Figure 2. Another alternative is to have the host retry several times by turning Q2 back on after a delay. This hiccup mode of operation will only work if the load capacitor is not discharged during the off time. The on-off duty cycle must be chosen so as not to exceed the safe operating area of Q2 under the applied conditions.

The nominal current fault delay of 183µsec is intended to allow charging of some capacitive loads while maintaining effective short circuit protection. A longer delay could destroy Q1 and Q2 under short circuit conditions due to the high short circuit current of some battery packs. The problem is compounded by the drop in battery voltage due to internal resistance. This drop reduces gate bias and may cause Q2 to operate in the linear region, raising power dissipation even further. (The power dissipation of Q1 is lower because its body diode becomes forward biased.)

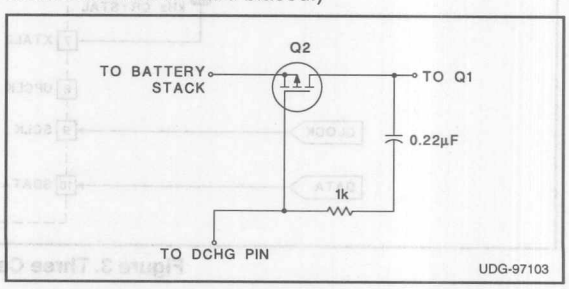


Figure 2. Slew Rate Limiting Discharge FET Turn On to Reduce Surge Current into Capacitive Loads

APPLICATION INFORMATION (cont.)

The circuit in Figure 4 shows a four cell pack with an internal host microprocessor. It may be powered from the regulated DVDD output. A clock is provided for the micro on pin 8. Also shown are two components to protect the gate of Q1 from possible overvoltage in cases where the charger open circuit voltage may exceed 20V.

To prevent the voltage on VDD from dropping below the UCC3951's minimum operating threshold during a short, an RCD may need to be added to hold up the VDD supply for a maximum of 244µsec. This is shown in Figure 4. The resistor value should be small enough to keep the drop across it less than 350 mV at full VDD load current. This includes whatever load current is applied to DVDD and TSPWR. Values of the resistor and capacitor, for three and four cell packs, are shown in Figure 4 The schottky diode prevents VDD from falling more than a diode drop below AIN1 when the battery voltage suddenly rises.

If cell balancing is required, the shunt current for each cell must be limited to less than 100 ma by an external resistor (R2, R3 and R6 in Figure 4). Note that a resistor is not required in series with the positive input of the top cell or the negative input of the bottom cell. (Only one cell should be shunted at a time.) To prevent shorting out the cell stack, never turn on all current shunts at once.

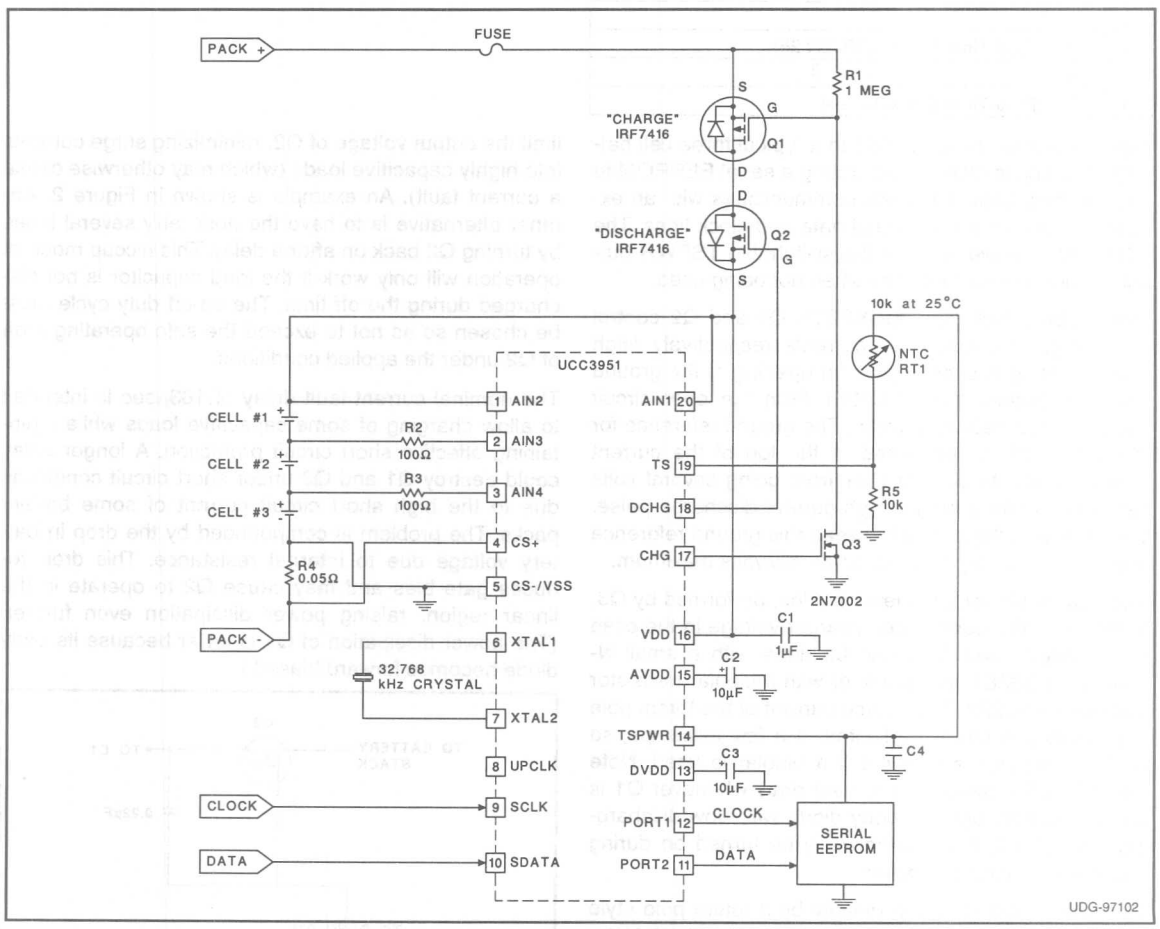
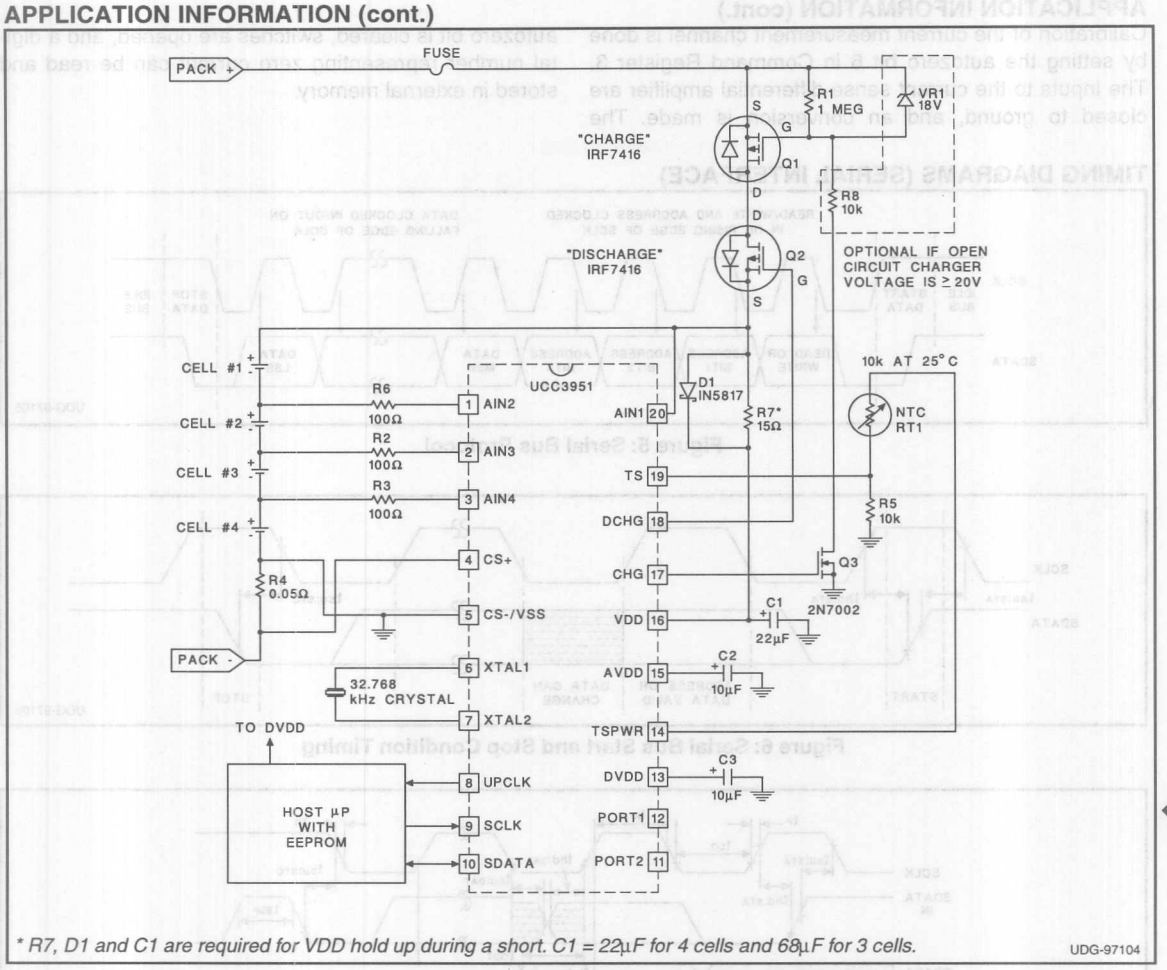


Figure 3. Three Cell Pack with EEPROM

APPLICATION INFORMATION (cont.)



** R7, D1 and C1 are required for VDD hold up during a short. C1 = 22µF for 4 cells and 68µF for 3 cells.* UDG-97104

Figure 4. Four Cell Pack withHost Microprocessor

System Calibration Strategy

Calibrating the voltage measurement channels connected to each of the four cells is necessary to meet the 1% tolerance on voltage measurement at 4.2V that is required for proper charge termination of lithium-ion cells. At the factory, the bandgap reference is trimmed to better than 1% tolerance to provide an accurate internal reference over temperature. The ADC is capable of 0.1% resolution (10 bits) at 4.2V. At final system test, a simple software calibration of each of the voltage measurement channels should be performed to obtain the highest accuracy. The test requires an accurate external voltage reference (to 1%) near 4.2V placed between one pair of AIN pins. A conversion on that external reference will provide a digital number representing the reference voltage. The number should be stored in external memory (host memory or EEPROM), and can be used in the following equation to calibrate future readings on that channel:

$$\text{Actual Voltage} = \text{ADC Reading} \bullet \frac{\text{Reference Voltage}}{\text{Reference ADC Reading}}$$

Channel calibration can also be done at different temperatures together with a thermistor reading to provide an accurate calibration of the channel as ambient temperature changes.

APPLICATION INFORMATION (cont.)

Calibration of the current measurement channel is done by setting the autozero bit 6 in Command Register 3. The inputs to the current sense differential amplifier are closed to ground, and an conversion is made. The autozero bit is cleared, switches are opened, and a digital number representing zero current can be read and stored in external memory.

TIMING DIAGRAMS (SERIAL INTERFACE)

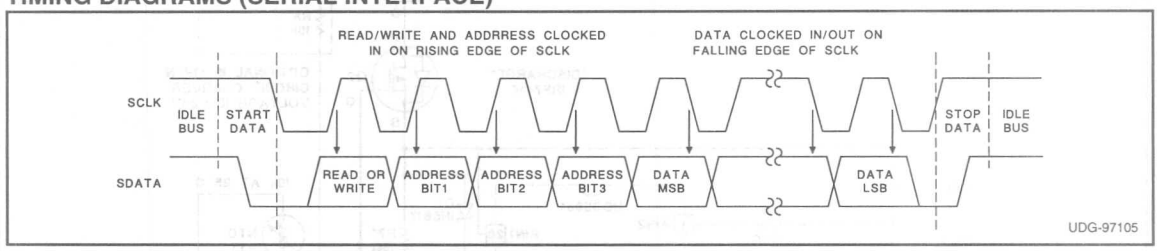


Figure 5: Serial Bus Protocol

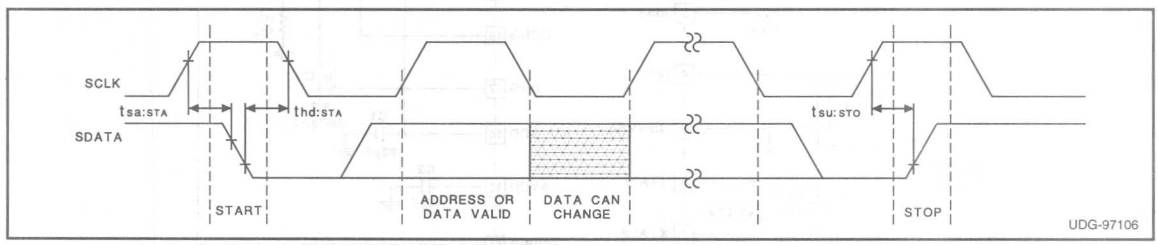


Figure 6: Serial Bus Start and Stop Condition Timing

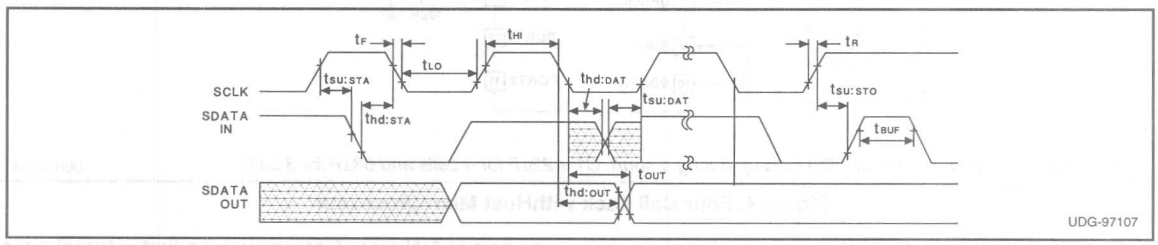


Figure 7. Serial Bus Timing Information

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Single Cell Lithium-Ion to +3.3V Converter

FEATURES

- Converts Lithium-Ion Cell to +3.3V at 750mA Load Current
- Load Disconnect in Shutdown
- High Efficiency Flyback Operation
- Internal 0.15Ω Switch
- Low Battery LED Driver
- Internal 2A Current Limit
- Internal 200kHz Oscillator
- 8 Pin D, N Packages

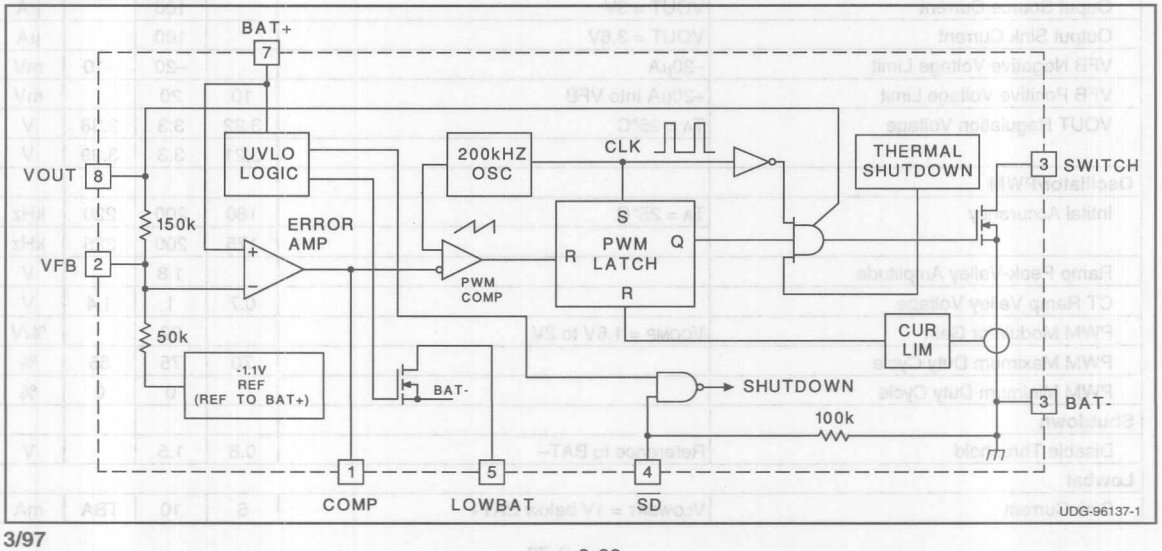
DESCRIPTION

The UCC3954, along with a few external components, develops a regulated +3.3V from a single lithium-ion battery whose terminal voltage can vary between 2.5V and 4.2V. The UCC3954 employs a simple flyback (Buck-Boost) technique to convert the battery energy to +3.3V. This is accomplished by referencing the lithium-ion cell's positive terminal to system ground. The negative terminal of the battery is the return point for the UCC3954. This approach enables the converter to maintain constant frequency operation whether the cell voltage is above or below the output voltage. An additional benefit of this technique is its inherent ability to disconnect the battery from the load in shutdown mode.

The UCC3954 operates as a fixed 200kHz switching frequency voltage mode flyback converter. The oscillator time base and ramp are internally generated by the UCC3954 and require no external components. A 2A current limit for the internal 0.15Ω power switch provides protection in the case of an output short circuit. When left open, an internal 100kΩ resistor pulls the $\overline{SD}$ pin to BAT–, which puts the UCC3954 in shutdown mode, and thereby reduces power consumption to sub-µA levels. A low battery detect function will drive the LOWBAT pin low (minimum of 5mA sink current) when the battery has been discharged to within 200mV of the predefined lockout voltage. The LOWBAT pin is intended for use with an external LED to provide visual warning that the battery is nearly exhausted. The lockout mode is activated when the battery is discharged to 2.55V. In lockout mode, the part consumes 15µA. Once the UCC3954 has entered lockout mode, the user must insert a fresh battery whose open circuit voltage is greater than 3.3V. This prevents a system-level oscillation of the lockout function due to the lithium-ion battery's large equivalent series resistance.

Additional features of the UCC3954 include a trimmed –1.1V reference and internal feedback scaling resistors, a precision error amplifier, low quiescent current drain in shutdown mode, and a softstart function. The UCC3954 is offered in the 8 pin D (surface mount), and N (through hole) packages.

BLOCK DIAGRAM



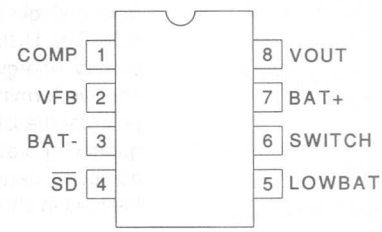
ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage (BAT+ to BAT–) 4.5V
VOUT
Maximum Forced Voltage (ref. to BAT+) 5.5V
SWITCH
Maximum Forced Voltage (ref. to BAT–) 10.2V
Maximum Forced Current. . . . . Internally Limited
$\overline{SD}$
Maximum Forced Voltage (ref. to BAT+) 5.5V
Maximum Forced Current. 10mA
COMP
Maximum Forced Voltage (ref. to BAT–) 4.5V
Maximum Forced Current. . . . . Self Limiting
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

Unless otherwise indicated, voltages are reference to ground and currents are positive into, negative out of the specified terminal. Pulsed is defined as a less than 10% duty cycle with a maximum duration of 500µs. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

DIL-8, SOIC-8 (Top View)
D Package, N Package



ELECTRICAL CHARACTERISTICS: Unless otherwise specified, T_A = –20°C to 70°C for the UCC3954, $\overline{SD}$ = V_{BAT+} = 3.5V (ref. to V_{BAT-}), VOUT = 3.3 (ref. to V_{BAT+}). T_A = T_J

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply					
Supply Current (total) – active	I_{BAT+} + I_{VOUT}		1	2	mA
Supply Current (BAT+)– Shutdown	V_{SDB} = 0V (reference to BAT–)		0.2	3	µA
Supply Current (BAT+) –UVLO			15	30	µA
BAT+ Turn On Threshold	New Battery Indicated (Note 1)	3	3.15	3.30	V
BAT+ Turn Off Threshold		2.5	2.55		V
Low BAT+ Indicate Threshold			2.7		V
Error Amplifier					
Input Offset		–5	0	5	mV
Output Voltage High	Maximum Duty Cycle	2.5	3	3.5	mV
Output Voltage Low	Zero Duty Cycle	0		1.5	V
Ouput Source Current	VOUT = 3V		100		µA
Output Sink Current	VOUT = 3.6V		100		µA
VFB Negative Voltage Limit	–20µA		–20	–10	mV
VFB Positive Voltage Limit	+20µA Into VFB	10	20		mV
VOUT Regulation Voltage	T_A = 25°C	3.22	3.3	3.38	V
		3.21	3.3	3.39	V
Oscillator/PWM					
Intital Accurancy	T_A = 25°C	180	200	220	kHz
		175	200	225	kHz
Ramp Peak-Valley Amplitude			1.8		V
CT Ramp Valley Voltage		0.7	1	1.4	V
PWM Modulator Gain	V_{COMP} = 1.6V to 2V		22		%/V
PWM Maximum Duty Cycle		70	75	85	%
PWM Minimum Duty Cycle			0	0	%
Shutdown					
Disable Threshold	Reference to BAT–	0.8	1.5		V
Lowbat					
Sink Current	V_{LOWBAT} = 1V below BAT+	5	10	TBA	mA

ELECTRICAL CHARACTERISTICS (cont.): Unless otherwise specified, T_A = –20°C to 70°C for the UCC3954, T_A = T_J. V_{BAT+} = 3.3V, V_{SD} = V_{BAT+} = 3.5V, VOUT = 3.3 (ref. to V_{BAT+}).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Soft Start					
VOUT Overshoot	RLOAD = 33Ω, C_{COMP} = 47nF	0		10	%
Output Switch					
Saturation Voltage	I_{SWITCH} = 200mA		30	60	mV
	I_{SWITCH} = 2A		300	600	mV
Short Circuit Current	Pulsed	2		3	A

Note 1: V_{BAT+} <2V to reset.
Note 2: V_{BAT+} <Low BAT+ indicate threshold (typically 2.75V).

PIN DESCRIPTIONS

BAT+: Logic supply voltage for the UCC3954. Connect to the positive terminal of the lithium-ion battery and system ground. Bypass with a low ESR, ESL capacitor if located more than 1 inch from the battery positive terminal. This is also the return for the +3.3V load

BAT–: Return for the UCC3954. Switch current flows through this pin to the negative terminal of the battery. Proper board layout precautions should be taken to minimize trace length in this path.

COMP: Output of the voltage error amplifier. Loop compensation component C_{COMP} is connected between COMP and VFB.

LOWBAT: An open drain output that will pull low and sink 10mA (typ) to drive an external LED if the battery voltage falls below the low BAT+ warning threshold. Note that this output pulls low to BAT-.

$\overline{SD}$: Shutdown input for the UCC3954. An internal 100kΩ resistor pulls $\overline{SD}$ to BAT– when the circuit is left open. Pulling $\overline{SD}$ up to system ground (BAT+) or to VOUT, starts the UCC3954. The UCC3954 enters a lockout mode when a dead battery is detected (<2.55V). Until a fresh battery is inserted (>3.3V), the part will remain in the low current lockout state.

SWITCH: Drain terminal of the internal 0.3Ω power switch. The current into this pin is internally limited.

VFB: This is the virtual ground of the error amplifier. Nominally at the same voltage as BAT+, the pin is provided for external compensation by means of a single capacitor to form a simple dominant pole.

VOUT: Regulated 3.3V supply feedback to the UCC3954.

APPLICATION INFORMATION

Circuit Topology

The UCC3954 uses a fixed frequency (200KHz), voltage mode PWM flyback topology. It can operate from a battery input voltage that is above or below the output voltage by referencing the battery's (+) terminal to the output (system) ground and the battery's (-) terminal to the IC's "ground" pin. It is typically operated in the continuous conduction mode (CCM), except at light loads to reduce losses due to high peak inductor current. The simplified diagrams below help to visualize the circuit topology.

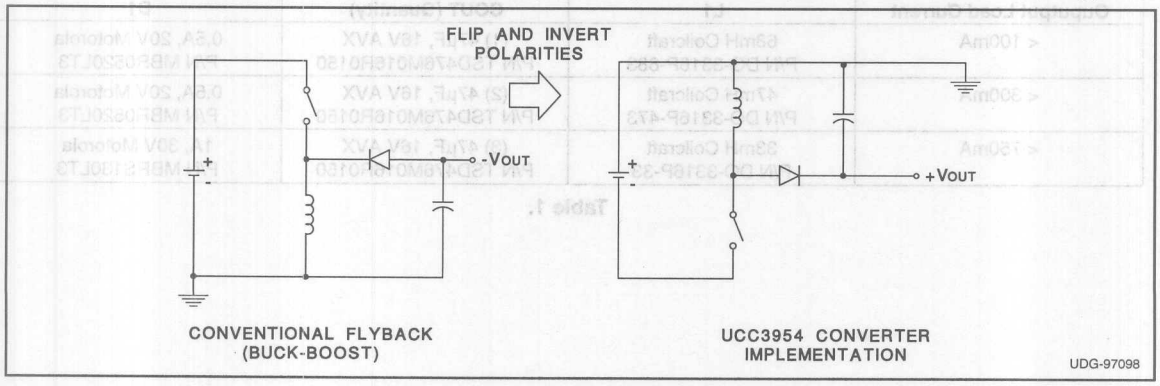


Figure 1.

APPLICATION INFORMATION (cont.)

Only a few external components are required to develop a regulated 3.3V output from a single Lithium-Ion cell. A low ESR (Equivalent Series Resistance) and ESL (Equivalent Series Inductance) decoupling capacitor should be placed as close as possible to BAT+ and BAT-. This is especially important when operating at low battery voltages, where the peak current could cause excessive input ripple, causing the input voltage to drop below the UCC3954's shutdown threshold. The other parts required are a compensation capacitor, inductor, Schottky diode and output filter capacitor. The output filter capacitor should also be a good low ESR/ESL capacitor made for high frequency switching power supplies.

Choosing an Inductor

The inductor value selected, for a given input voltage and load current, will determine if the converter is operating in the continuous or the discontinuous conduction mode. The efficiency will be higher in the continuous mode (larger inductor value), due to the lower peak currents. This also reduces the demands on the output filter capacitor and lowers output ripple voltage. Larger inductor values will also allow higher output load currents before reaching current limit, due to the lower peak current. However, a larger inductor value will also be physically larger for the same current rating, and reduces loop bandwidth, making it more difficult to compensate. For the input voltage range and fixed operating frequency of the UCC3954, an inductor value of around 33µH is a good compromise. See Table 1 for values and part numbers of inductors for specific ranges of load current.

Remember that the inductor must be able to maintain most of its inductance at the peak current.

Output Capacitor Selection

To minimize output voltage ripple, a good high frequency capacitor(s) must be used. Low ESR tantalums or Sanyo OSCON's are recommended. Surface mounting will eliminate the lead inductance. To prevent loop stability problems, don't overkill with 100's of µF. Suggested values and part numbers for COUT at different load currents are given in Table 1. The values and quantity were chosen for a maximum of 3% P - P output ripple. Note that a higher voltage rating than necessary was chosen to achieve the lowest ESR with the least amount of capacitance.

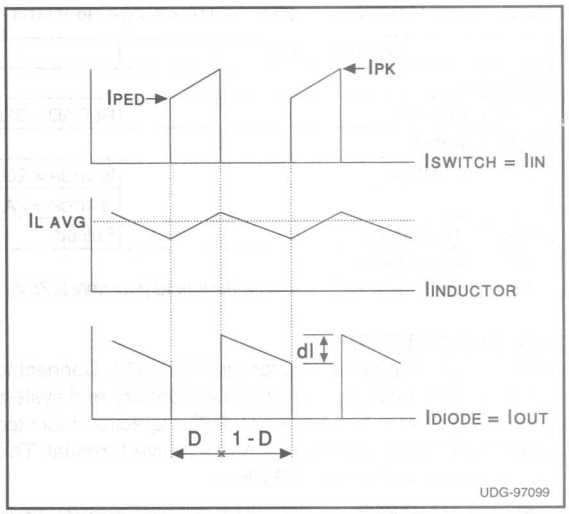


Figure 2.

Compensation Capacitor

The loop may be compensated with a single capacitor between COMP and VFB. This simple dominant pole method is recommended. The value shown in the Application Circuit provides good stability margin over a wide range of load, using the values for L1 and COUT given in Table 1.

Ouputput Load Current	L1	COUT (Quantity)	D1
< 100mA	68mH Coilcraft P/N DO-3316P-683	(1) 47µF, 16V AVX P/N TSD476M016R0150	0.5A, 20V Motorola P/N MBR0520LT3
< 300mA	47mH Coilcraft P/N DO-3316P-473	(2) 47µF, 16V AVX P/N TSD476M016R0150	0.5A, 20V Motorola P/N MBR0520LT3
< 750mA	33mH Coilcraft P/N DO-3316P-33	(3) 47µF, 16V AVX P/N TSD476M016R0150	1A, 30V Motorola P/N MBRS130LT3

Table 1.

APPLICATION INFORMATION (cont.)

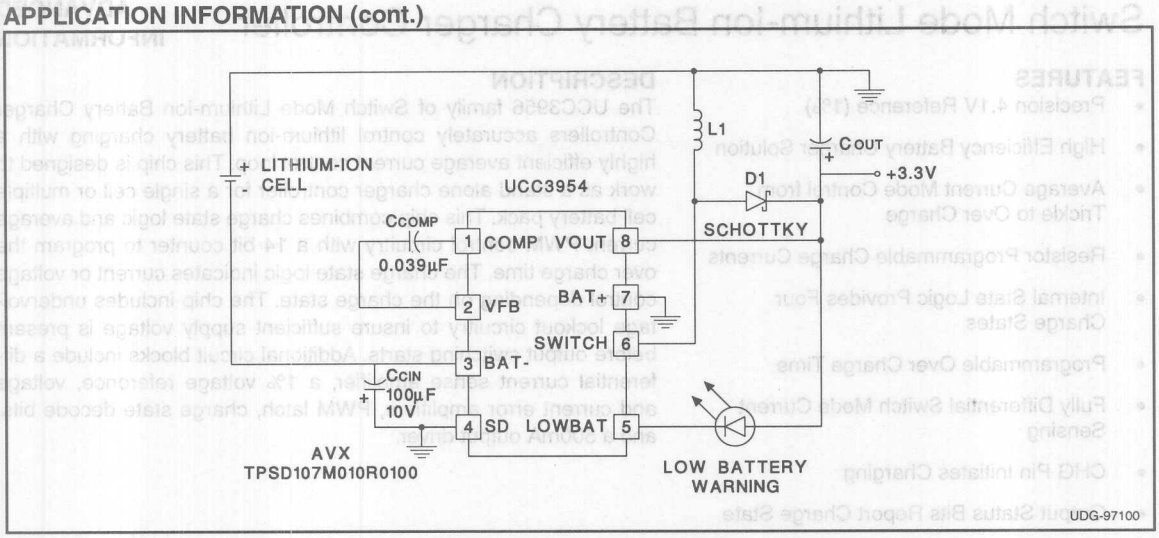


Figure 3. Application Circuit

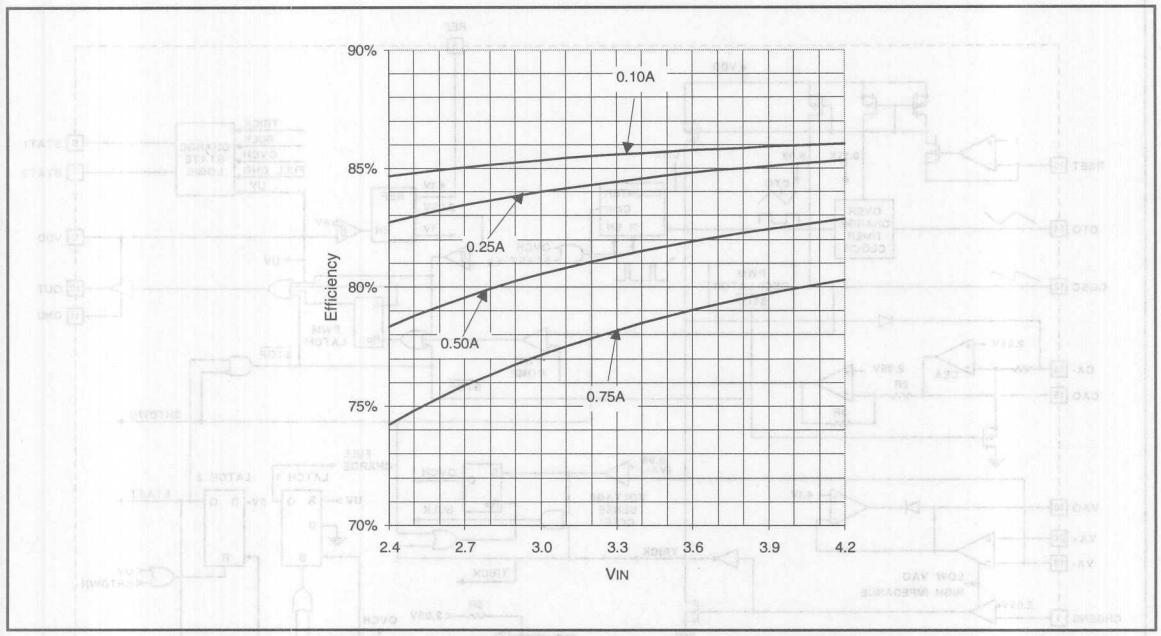


Figure 4. Calculated Overall Efficiency vs Line and Load

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Switch Mode Lithium-Ion Battery Charger Controller

ADVANCED INFORMATION

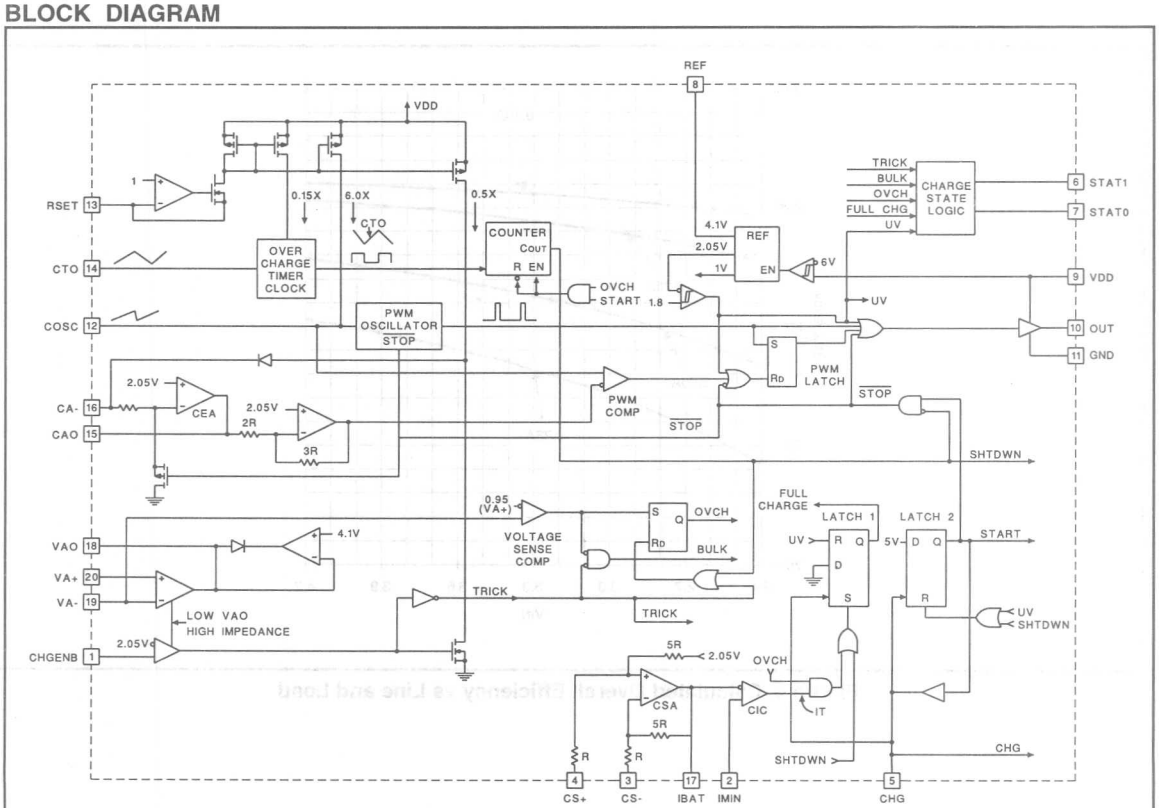
FEATURES

- Precision 4.1V Reference (1%)
- High Efficiency Battery Charger Solution
- Average Current Mode Control from Trickle to Over Charge
- Resistor Programmable Charge Currents
- Internal State Logic Provides Four Charge States
- Programmable Over Charge Time
- Fully Differential Switch Mode Current Sensing
- CHG Pin Initiates Charging
- Output Status Bits Report Charge State

DESCRIPTION

The UCC3956 family of Switch Mode Lithium-Ion Battery Charger Controllers accurately control lithium-ion battery charging with a highly efficient average current control loop. This chip is designed to work as a stand alone charger controller for a single cell or multiple cell battery pack. This chip combines charge state logic and average current PWM control circuitry with a 14 bit counter to program the over charge time. The charge state logic indicates current or voltage control depending on the charge state. The chip includes undervoltage lockout circuitry to insure sufficient supply voltage is present before output switching starts. Additional circuit blocks include a differential current sense amplifier, a 1% voltage reference, voltage and current error amplifiers, PWM latch, charge state decode bits, and a 500mA output driver.

BLOCK DIAGRAM



Note: Pin numbers refer to DIP-20 and SOIC-20 packages only.

UDG-96197

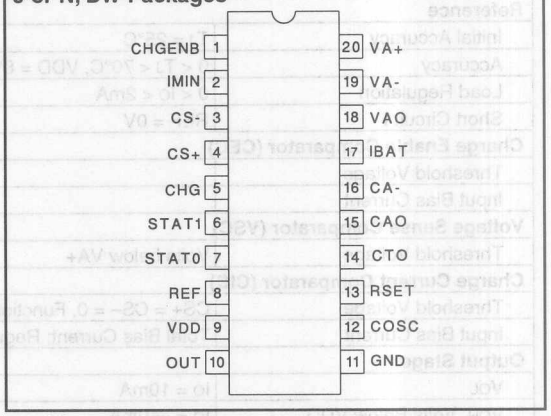
ABSOLUTE MAXIMUM RATINGS

Supply Voltage VDD, OUT 20V
Output Current Sink
  Continuous 120mA
  Peak. 600mA
Output Current Source
  Continuous 120mA
  Peak. 600mA
CS+, CS–
  Voltage. . . . . –0.5 to VDD
  Current with CS+, CS– less than –0.5 . . . . . 50mA
Remaining Pin Voltages . . . . . –0.3V to 6V
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

Currents are positive into, negative out of the specified terminal.
Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

DIP-20 (Top View)
J or N, DW Packages



ELECTRICAL CHARACTERISTICS: Unless otherwise specified, T_A = –40°C to +85 for UCC2956 and 0°C to +70°C for UCC3956, CT = 517pF, RSET = 49.9k, CTO = 1697nF, VDD = 12V, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Current Sense Amplifier (CSA)					
DC Gain	CS– = 0, CS+ = –50mV and CS+ = –250mV	4.9	5	5.1	V/V
	CS+ = 0, CS– = 50mV and CS– = 250mV	4.9	5	5.1	V/V
CAO	CS+ = CS– = 0V	1.99	2.05	2.11	mV
CMRR	V_{CM} = –0.2V to 18V, VDD = 18V	60			dB
V_{OL}	CS+ = –0.2V, CS– = 0.5V, IO = 1mA		0.3		V
V_{OH}	CS+ = 0.5V, CS– = –0.2V, IO = –500µA	3.7	4.1	4.4	V
Output Source Current	IBAT = 3V, VID = 700mV	–750			µA
Output Sink Current	IBAT = 1V, VID = –700mV	500			µA
3dB Bandwidth	V_{CM} = 0V, CS+ - CS– = 100mV	0.2	3		MHz
Current Error Amplifier (CEA)					
IB	8V < VCC < 18V, CHGENB = REF		0.1	0.1	µA
CA– Voltage	8V < VCC < 18V, CAO = CA–	1.99	2.05	2.11	V
AVO		60	90		dB
GBW	T_J = 25°C, F = 100kHz	1	3		MHz
V_{OL}	Io = 250µA, CA– = 3V		0.5		V
V_{OH}	Io = –1mA, CA– = 2V	3.7	4.1	4.4	V
$I_{CA–}$, Itrck_control	V_{CHGENB} = GND	8	10	12	µA
Voltage Error Amplifier (VEA)					
IB	Total Bias Current; Regulating Level		0.5	3	µA
VIO	8V < VCC < 18V, –0.2 < VCM < 5V			5	mV
AVO		60	90		dB
GBW	T_J = 25°C, F = 100kHz	0.75	3		MHz
V_{OL}	Io = 500µA, VA– = 3.8V		1		V
V_{OH}	Io = –500µA, VA– = 4.4V	3.8	4.1	4.3	V
VAO Leakage	V_{CHGENB} = GND, STAT0 = 0 and STAT1 = 0, VAO = 2.05V	–1		1	µA
Pulse Width Modulator					
Maximum Duty Cycle	CAO = 0.5V	85	92	100	%
Modulator Gain	CAO = 1.6V, 2.4V	73	80	87	%/V
PWM Oscillator (OSC)					
Frequency	7V < VDD < 18V	90	100	110	kHz
Over Charge Timer (OCT)					
Frequency	7V < VDD < 18V (Note 1)	3.8	4.48	5.15	kHz

ELECTRICAL CHARACTERISTICS (cont.): Unless otherwise specified, T_A = –40°C to +85 for UCC2956 and 0°C to +70°C for UCC3956, CT = 517pF, RSET = 49.9k, CTO = 169nF, VDD = 12V, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Reference					
Initial Accuracy	T_J = 25°C	4.06	4.1	4.14	V
Accuracy	0 < T_J < 70°C, VDD = 8V to 18V	4.05	4.1	4.15	V
Load Regulation	0 < I_O < 2mA		3	15	mV
Short Circuit I	REF = 0V	10	20	30	mA
Charge Enable Comparator (CEC)					
Threshold Voltage			2.05		V
Input Bias Current		–0.5	–0.2		µA
Voltage Sense Comparator (VSC)					
Threshold Voltage	Volts below VA+	50	125	200	mV
Charge Current Comparator (CIC)					
Threshold Voltage	CS+ = CS– = 0, Function of IBAT = 2.05V	2	2.05	2.1	V/V
Input Bias Current	Total Bias Current; Regulating Level	–0.5	–0.2		µA
Output Stage					
V_{OL}	I_O = 10mA		0.1	0.5	V
V_{OH}, Volts Below VDD	I_O = –10mA		0.1	0.5	V
Rise Time	C_{OUT} = 1nF		20	30	ns
Fall Time	C_{OUT} = 1nF		20	30	ns
STAT0 and STAT1 Open Drain Outputs					
Maximum Sink Current	V_{OUT} = 12V	6	10		mA
V_{OL}	I_{OUT} = 200mA		0.1	0.2	V
UVLO Section					
Turn-on Threshold		6.25	6.75	7	V
Hysteresis		150	200	250	mV
IDD					
IDD (Run)			5	8	mA
ICC (Off)			0.5		mA

Note 1: 14 bit timer functionality tested at higher frequency.

PIN DESCRIPTIONS

CA–: The inverting input to the current error amplifier.

CAO: The output of the current error amplifier and inverting input of the PWM comparator.

CS–, CS+: The inverting and non-inverting inputs to the current sense amplifier. This amplifier has a fixed gain of 5.

CHG: A rising edge triggered input pin that indicates charging. Once the internal 14 bit timer has timed out the chip enters its shutdown charge state. At this point CHG is pulled low by an internal buffer. Another low to high transition is required to reset the timer and restart charging.

CHGENB: The input to a comparator that detects when the battery voltage is low and places the charger in trickle charge. The charge enable comparator forces the output of the voltage error amplifier to a high impedance state while forcing a fixed 10µA current into the CA– to set the trickle charge.

COSC: The oscillator ramp pin which has a capacitor (COSC) to ground. The ramp oscillates between 1.5V to 3.5V and the frequency is determined by:

$$\text{Frequency} = \frac{0.012}{\text{COCS} \bullet (12 + 0.004 \bullet \text{RESET})}$$

CTO: The slow oscillator ramp pin which is used to generate a clock signal for the 14 bit timer to program the over charge time. A capacitor to ground is charged and discharged with equal currents at a frequency programmed between 0.75Hz to 5Hz. The ramp oscillates between 1.5V to 3.5V and the frequency is determined by:

$$\text{Frequency} = \frac{0.0375}{\text{CTO} \bullet \text{RSET}}$$

GND: The reference point for the internal reference, all thresholds, and the return for the remainder of the device.

IBAT: The output of the current sense amplifier.

IMIN: The minimum charge current programming pin is provided to program an optional charge termination in addition to the programmable timer.

PIN DESCRIPTIONS (cont.)

OUT: The output of the PWM driver.

REF: The 4.1V precision reference which should be bypassed with a 1µF capacitor.

RSET: This pin programs the charge current for the oscillator ramp. The oscillator charge current is determined by:

$$\frac{1V}{RSET}.$$

The trickle control current (Itrck_control) is determined by:

$$\frac{1V}{RSET \bullet 2}.$$

STAT0, STAT1: CMOS binary output decode pins indicating the four different charge states. The maximum high voltage sense comparator.

VA–: The inverting input to the voltage error amplifier that is used as a battery sense input. It is also the input to the voltage sense comparator. The bulk charge state is completed and over charge state is initiated when VA– reaches 95% of VA+.

VA+: The non-inverting input to the voltage error amplifier that is used a s the battery charge reference voltage.

VAO: The output of the voltage error amplifier. The upper output clamp of this amplifier is 5V.

VDD: The input voltage of the chip. This chip is operational between 6V and 20V and should be bypassed with a 1µF capacitor.

CHARGE STATE DECODE CHART

	STAT1	STAT0	
Trickle Charge	0	0	CHGENB < 2.05V
Bulk Charge	0	1	VA– < 95% of VA+ and CHGN > 2.05V
Over Charge	1	0	VA– > 95% VA+ and IBAT > IMIN

APPLICATION INFORMATION

The UCC3956 contains all the necessary control functions for implementing an efficient switch mode Lithium-Ion battery charger. Lithium-Ion batteries are rapidly becoming the battery of choice for rechargeable portable and lap top products. When compared to NiCd, NiMH, and Lead Acid batteries, Lithium-Ion offer less weight and volume for the same energy. Lithium-Ion batteries do not suffer from the memory effect found in NiCd batteries. This effect, caused by not completely discharging and charging a battery, will reduce battery capacity over several charge cycles. Because Lithium-Ion batteries have a high average cell voltage of around 3.6V, they can often replace 2 to 3 Nickel based cells.

The advantages that Lithium-Ion batteries offer come at the cost of a wide operating voltage. Near zero capacity, the cell will typically have a voltage of 2.5V. A fully charged cell will typically have a voltage of 4.1V. Unlike many so called "smart" or "universal" chargers, the UCC3956 is optimized for Lithium-Ion characteristics. In order to restore capacity quickly, the chip features both constant current and constant voltage modes of operation. A programmable over charge time, provided by the UCC3956 timer, allows the charger to predictably restore 100% capacity to the battery.

Charger Operation

When CHG is transitioned from a low to high logic level, the chip will cycle through several charge states. If the battery voltage is severely depleted, the charger will begin in a low current trickle charge state. When the battery voltage is above a user set threshold, the charger will initiate a constant current bulk charge state. Once the battery reaches 95% of it's final voltage, the charger will enter an over charge state. During the over charge state, the converter will transition from a constant current to a constant voltage mode of operation. Figure 2 shows typical current, voltage, and capacity levels of a Lithium-Ion battery during a complete charge cycle.

A Block Diagram of the UCC3956 is shown on the first page of the data sheet, while Figure 1 shows a typical application circuit for a Buck derived switch mode charger. The UCC3956 can be used for charging a single cell or multiple cells in series. If more than two cells are stacked in series, however, a level shifting gate drive will be needed to operate the buck switch. The application circuit charges a 1200mAh 2 cell stack at a 1C rate.

Setting the Oscillator Frequency

The frequency of operation for the converter is set by picking values for RSET and COSC.

$$f_{OCS} = \frac{0.012}{COSC \bullet (12 + 0.004 \bullet RSET)}$$

The UCC3956 is capable of operating at frequencies higher than 200kHz. However, the actual operating frequency of the buck converter will ultimately be determined by the usual tradeoffs of size, cost and efficiency. The application circuit frequency is set at 100kHz with COSC = 180pF and RSET = 162k.

APPLICATION INFORMATION (cont.)

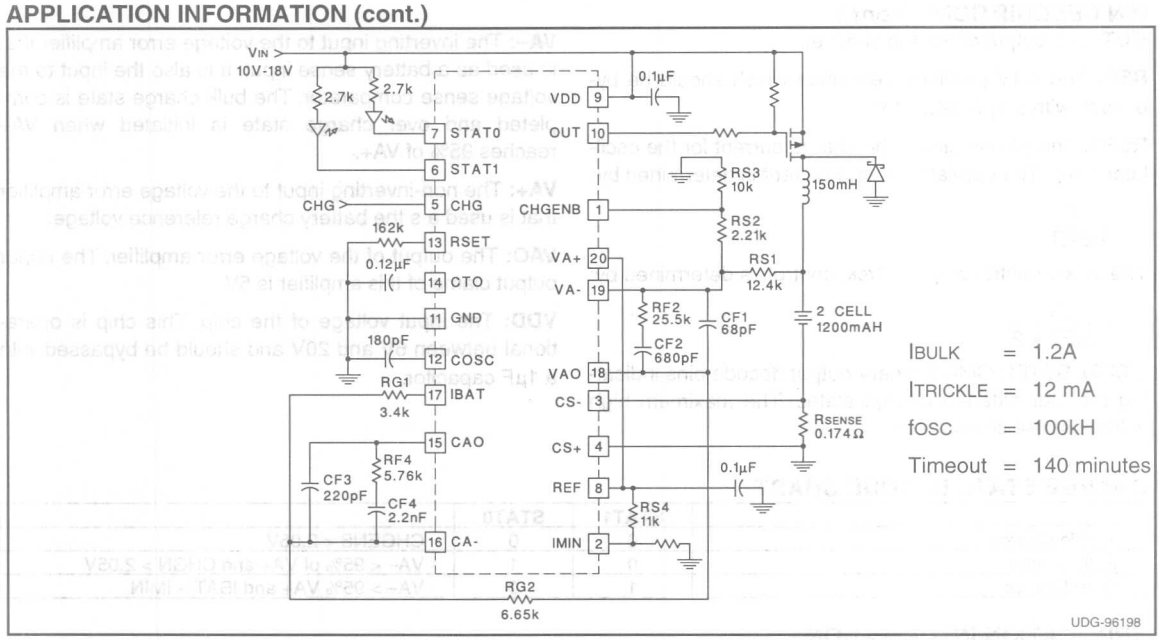


Figure 1. Typical Application Circuit

Trickle Charge State

When a battery's voltage is below a predetermined threshold, the battery is either deeply discharged or has shorted cells. The trickle charge state offers a low charging current to bring the battery up above zero capacity. In the case of shorted cells, the trickle charge state prevents the charger from delivering high currents during this fault condition. Stacking several cells makes the detection of a shorted cell more difficult.

For Lithium-Ion batteries, the trickle charge threshold is typically set to a value around 2.5V per cell (this corresponds to near zero capacity). When the cell voltage is below the threshold, only a trickle current will be applied to the battery. The threshold is established by programming CHGENB to 2.05V when the battery (or stack) voltage is at the threshold. Referring to the application circuit of Figure 1, the trickle charge voltage threshold is determined by:

$$V_{TRICKLE_THRESHOLD} = \frac{RS1 + RS2 + RS3}{RS3} \bullet 2.05$$

With a trickle threshold of 5V (for 2 cells) and setting RS3 to 10k, RS1+ RS2 should be approximately 14.4k.

The trickle charge current is often set to 1% of the bulk charge current. The current value is set by picking the appropriate value for RG1. Referring to the Block Diagram and Figure 1, during trickle charge a fixed current

$$\frac{0.05}{RSET}$$

flows out of the current amplifier's inverting input and into RG1. The voltage amplifier output is disabled during trickle charge and acts as a high impedance node. The resulting voltage at the output of the current sense amplifier sets the trickle charge current.

$$I_{TRICKLE} = \frac{RG1}{10 \bullet RSET \bullet R_{SENSE}}$$

In the application circuit the sense resistor is 0.174Ω and RSET is 162k, for a trickle current of about 12mA a 3.4k resistor is selected for RG1.

The converter is typically designed to run in discontinuous conduction mode during trickle charge. This allows a reasonably small value of inductance to be used. The average current mode of the UCC3956 provides improved discontinuous duty cycle control, when compared to peak current mode implementations.

In Figure 2, the trickle charge state corresponds to the time interval between t0 (when CHG is transitioned from low to high) and t1. During the trickle charge state STAT0 and STAT1 are logic level lows. At time t1 the trickle threshold is met, and the charger transitions to the bulk charge state. In many instances, the battery voltage will initially be above the trickle threshold. In this case, the trickle charge state will not be needed.

APPLICATION INFORMATION (cont.)

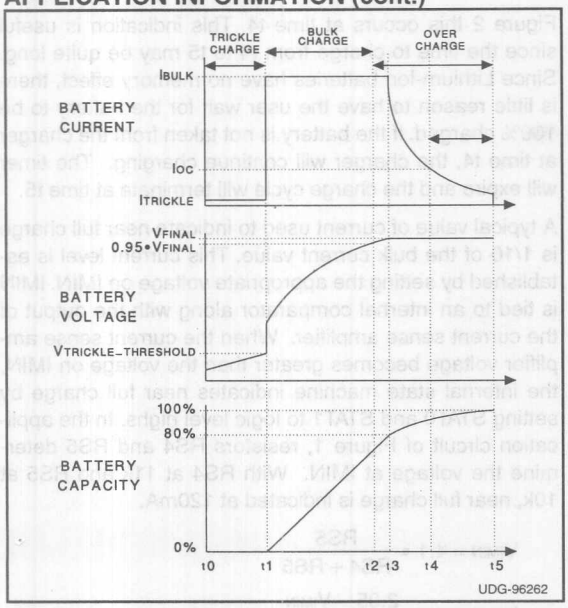


Figure 2. Typical Charge Cycle Levels

Bulk Charge State

As the name implies, the bulk charge state is responsible for restoring a majority of the charge back into the battery. The bulk charge current is determined by the C rate and the capacity of the battery. In the application circuit, 2 stacked 1200mAH batteries are charged at a 1C rate. This will require 1.2A of current during bulk charge. In this case, the battery will take about 60 minutes to reach approximately 80% capacity.

Both the voltage and current sense amplifiers are enabled during bulk charge. The voltage amplifier is saturated in this state as the battery voltage is slowly rising, but is not yet high enough to drive the voltage amplifier into regulation. The output of voltage amplifier is clamped at a nominal voltage of 4.1V. The current sense amplifier is configured such that its output voltage increases with decreasing RSENSE current. RSENSE should be sized such that the output voltage of the current sense amplifier VIBAT is within specification during bulk charge.

$$V_{IBAT(BULK)} = 2.05 - 5 \bullet I_{BULK} \bullet R_{SENSE}$$

With 1.2A of bulk current and setting the current sense amplifier output at 1V, a sense resistor of 0.174Ω is required. As always, power dissipation and converter efficiency must be considered when choosing RSENSE.

Referring to the Feedback Diagram of Figure 3, the output of the voltage and current sense amplifiers are summed together at the inverting input of the current amplifier. Assuming that the current amplifier is within regulation, the required value of RG2 can be calculated. The application circuit uses a value of 6.65k for RG2, setting the bulk current to 1.2A.

$$RG2 = \frac{2.05 \bullet RG1}{5 \bullet I_{BULK} \bullet R_{SENSE}}$$

Referring to Figure 2, the bulk charge state corresponds to the interval between t1 and t2. The step in voltage at time t1 is caused by bulk current flowing into the battery ESR and sense resistor. In the bulk charge state STAT0 is a logic level high and STAT1 is a logic level low.

Over Charge State

The over charge state of the converter starts when the battery reaches 95% of its final voltage (time t2 of Figure 2). The over charge state is initiated when the voltage at the inverting input of the voltage amplifier is 95% of the non-inverting input voltage. Using 95% rather than 100% of the final battery voltage assures that the over charge

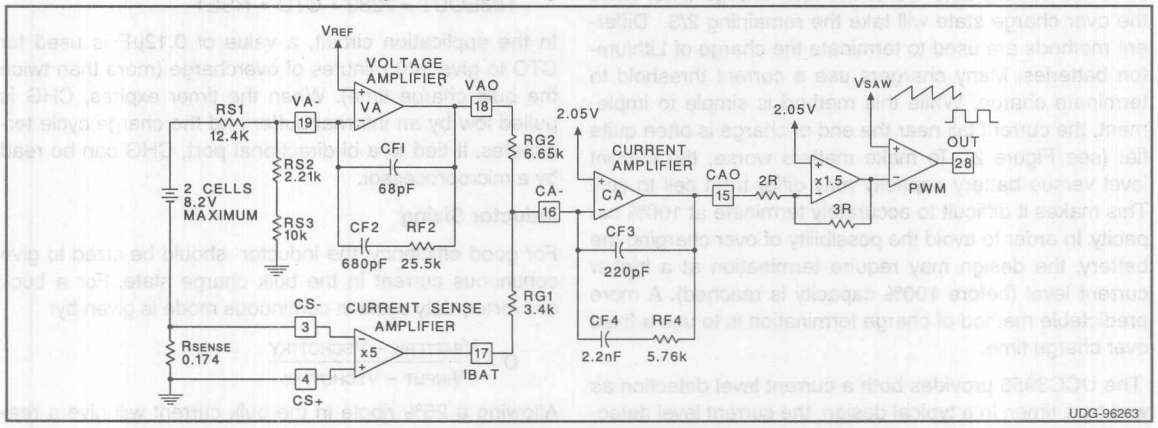


Figure 3. Simplified Feedback Diagram

APPLICATION INFORMATION (cont.)

timer will always be set, before the battery current tapers off. At the beginning of over charge STAT0 indicates a logic level high and STAT1 indicates a logic level low.

In the application circuit of Figure 1, the voltage at which over charge is initiated is set by resistors RS1, RS2 and RS3. These resistors are also used to set the trickle charge threshold. The battery (or stack) voltage that will initiate the over charge state is:

$$V_{OC_THRESHOLD} = 0.95 \bullet \frac{RS1 + RS2 + RS3}{RS2 + RS3} \bullet 4.1$$

For a single cell stack, RS1 should be 0Ω. This results in a final battery voltage of 4.1V. It is important not to charge a Lithium-Ion battery above 4.2V. When charging a battery stack, RS1 should be selected to properly set the final stack voltage. In the application circuit, RS1 is selected to be 12.4k and RS2 is selected to be 2.21k. This sets the over charge level at 8.2V, while setting the trickle charge threshold to about 5V.

The battery voltage at the beginning of the over charge state may not correspond to the voltage amplifier coming out of saturation. Therefore, bulk current may continue in the battery during the initial portion of the over charge state (see Figure 2). When the voltage amplifier comes into regulation, the amplifier's output voltage will begin to decrease. The current sense amplifier's output voltage will need to increase, in order for the current amplifier's inverting input to remain at 2.05V. This will translate into a decreasing battery current. The battery current will continue to decrease as the battery approaches 100% capacity.

Although the bulk charge state restores a majority of the capacity to the battery, the over charge state will typically take a majority of the charge cycle time. The bulk charge state will usually take 1/3 of the total charge time, while the over charge state will take the remaining 2/3. Different methods are used to terminate the charge of Lithium-Ion batteries. Many chargers use a current threshold to terminate charge. While this method is simple to implement, the current tail near the end of charge is often quite flat (see Figure 2). To make matters worse, the current level versus battery capacity may differ from cell to cell. This makes it difficult to accurately terminate at 100% capacity. In order to avoid the possibility of over charging the battery, the design may require termination at a higher current level (before 100% capacity is reached). A more predictable method of charge termination is to use a fixed over charge time.

The UCC3956 provides both a current level detection as well as a timer. In a typical design, the current level detection is used to give an indication of near full charge. In Figure 2 this occurs at time t4. This indication is useful since the time to charge from t4 to t5 may be quite long. Since Lithium-Ion batteries have no memory effect, there is little reason to have the user wait for the battery to be 100% charged. If the battery is not taken from the charger at time t4, the charger will continue charging. The timer will expire and the charge cycle will terminate at time t5.

A typical value of current used to indicate near full charge is 1/10 of the bulk current value. This current level is established by setting the appropriate voltage on IMIN. IMIN is tied to an internal comparator along with the output of the current sense amplifier. When the current sense amplifier voltage becomes greater than the voltage on IMIN, the internal state machine indicates near full charge by setting STAT0 and STAT1 to logic level highs. In the application circuit of Figure 1, resistors RS4 and RS5 determine the voltage at IMIN. With RS4 at 11k and RS5 at 10k, near full charge is indicated at 120mA.

$$V_{IMIN} = 4.1 \bullet \frac{RS5}{RS4 + RS5}$$

$$I_{NEAR_FULL} = \frac{2.05 - V_{IMIN}}{5 \bullet R_{SENSE}}$$

The UCC3956 timer has a 14 bit counter that allows long over-charge times with reasonable component values. As stated above, the charger will continue charging the battery until the timer expires (unless the battery is pulled from the charger). Referring to Figure 2, the timer starts at time t2 and expires at time t5. The frequency of the timer can be determined as follows:

$$f_{TIMER} = \frac{0.0375}{RSET \bullet CTO}$$

With a 14 bit counter the time-out period in minutes becomes:

$$TIMEOUT = 7282 \bullet CTO \bullet RSET$$

In the application circuit, a value of 0.12µF is used for CTO to give 140 minutes of overcharge (more than twice the bulk charge time). When the timer expires, CHG is pulled low by an internal buffer and the charge cycle terminates. If tied to a bi-directional port, CHG can be read by a microprocessor.

Inductor Sizing

For good efficiency, the inductor should be sized to give continuous current in the bulk charge state. For a buck converter, duty cycle in continuous mode is given by:

$$D = \frac{V_{BATTERY} - V_{SCHOTTKY}}{V_{INPUT} - V_{SCHOTTKY}}$$

Allowing a 25% ripple in the bulk current will give a reasonable value of inductance. The inductor value can be

APPLICATION INFORMATION (cont.)

calculated as follows:

$$L = \frac{4 \bullet (V_{INPUT} - V_{BAT}) \bullet D}{I_{BULK} \bullet f_{OSC}}$$

A 150µH inductor is used in the application circuit.

Current Control Loop

The UCC3956 features a voltage outer loop and an average current inner loop. The virtues of average current mode control are well documented in Reference [1]. A simplified block diagram of the feedback elements is provided in Figure 3. The feedback network for the current amplifier can be as simple as a single capacitor, providing a dominant pole response. In many battery charger circuits, a low frequency response may be quite adequate. The current amplifier feedback network in Figure 3 provides improved transient performance.

The network consisting of CF3, CF4, and RF4 will shape the current amplifier's response. In this example, components will be selected to give a constant gain from approximately $f_{OSC}/10$ up to f_{OSC}. At frequencies below, $f_{OSC}/10$ the network gain will increase at 20db/decade, giving an infinite gain at DC. Above the oscillator frequency, the network gain will attenuate at 20db/decade, giving good noise suppression. An optimal design will have the amplified inductor current down-slope approach the magnitude of the PWM saw-tooth slope [1]. This design will allow the current loop 3/4 of the saw-tooth slope, leaving the remaining 1/4 of the saw-tooth slope for the voltage loop. The current amplifier gain, with respect to the current sense amplifier, between $f_{OSC}/10$ and f_{OSC} is equal to:

$$\frac{RF4}{RG1}.$$

Referring to Figure 3, the current sense amplifies by 5 and an additional stage amplifies by 1.5. The equation below shows the relationship between the amplified inductor ramp and the saw-tooth ramp.

$$\frac{V_{BAT} + V_{SHOTTKY}}{L} \bullet R_{SENSE} \bullet 5 \bullet \frac{RF4}{RG1} \bullet 1.5 \leq \frac{3}{4} \bullet V_{SAWTOOTH} \bullet f_{OSC}$$

In the applications circuit, the right hand side of the inequality is equal to 127.5k ($V_{SAWTOOTH}$ = 1.7V). Assuming 8.2V for V_{BAT} and 0.5V for $V_{SCHOTTKY}$, a value of 5.76k for RF4 will give acceptable slope matching. Once RF4 is determined, CF3 and CF4 can be selected to give corner frequencies at $f_{OSC}/10$ and f_{OSC} respectively.

$$CF3 = \frac{1}{2 \bullet \pi \bullet f_{OSC} \bullet RF4}$$

$$CF4 = \frac{10}{2 \bullet \pi \bullet f_{OSC} \bullet RF4}$$

In the application circuit, a value of 220pF is used for CF3 and 2.2nF is used for CF4.

Figures 4a and 4b shows the predicted gain or phase of the application circuit's current loop from 10Hz to 10MHz. The power stage small signal gain can be approximated by:

$$\frac{V_{IN}}{sL + R_{SENSE} + BAT_{ESR}}$$

This gain multiplied by R_{SENSE} is represented as the power stage in Figure 4a. The current feedback gain in Figure 4a consists of the current amplifier gain, the PWM gain ($1/V_{SAW}$), as well as fixed gains of 5 and 1.5. The total open loop gain is the product of the feedback and power stage gains. The total open loop gain and phase are found in Figure 4b.

Adding the Voltage Control Loop

A feedback network similar to the current amplifier will be

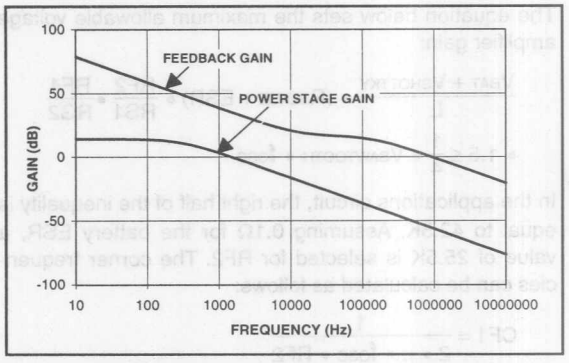


Figure 4a. Current Loop Power Stage and Feedback Gains

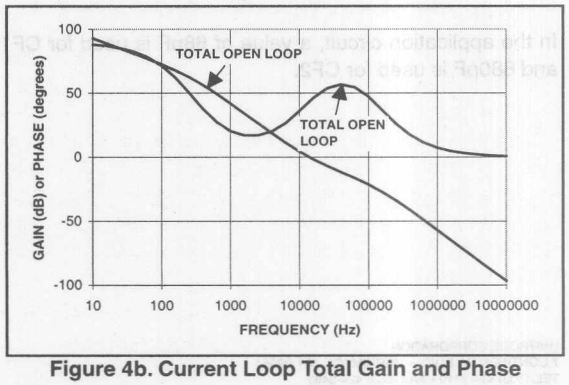


Figure 4b. Current Loop Total Gain and Phase

APPLICATION INFORMATION (cont.)

used for the voltage loop. The network consists of RF2, CF1, and CF2. The feedback design has allocated 1/4 of the saw-tooth ramp for voltage control. A small voltage ripple, caused by inductor current flowing into RSENSE and the ESR of the battery, will be present at the positive battery terminal. In the voltage control loop the ripple is amplified by the voltage amplifier, the current amplifier, and 1.5 before being compared to the oscillator ramp (see Figure 3). The voltage amplifier gain between fOSC/10 and fOSC will be

$$\frac{RF2}{RS1}.$$

For a single cell application, RS1 will have a zero value. A resistor placed between RS2 and the inverting input of the voltage amplifier will be needed to set the gain. The voltage amplifier output is resistively summed with the current sense amplifier output as shown in Figure 3. The current amplifier gain, with respect to the voltage amplifier, will be

$$\frac{RF4}{RG2}.$$

The equation below sets the maximum allowable voltage amplifier gain:

$$\frac{V_{BAT} + V_{SHOTTKY}}{L} \bullet (R_{SENSE} + ESR) \bullet \frac{RF2}{RS1} \bullet \frac{RF4}{RG2}$$

$$\bullet\ 1.5 \le \frac{1}{4} \bullet V_{SAWTOOTH} \bullet f_{OSC}$$

In the applications circuit, the right half of the inequality is equal to 42.5K. Assuming 0.1Ω for the battery ESR, a value of 25.5K is selected for RF2. The corner frequencies can be calculated as follows:

$$CF1 = \frac{1}{2 \bullet \pi \bullet f_{OSC} \bullet RF2}$$

$$CF2 = \frac{10}{2 \bullet \pi \bullet f_{OSC} \bullet RF2}$$

In the application circuit, a value of 68pF is used for CF1 and 680pF is used for CF2.

In the voltage loop, the power stage gain is multiplied by (RSENSE + ESR), shown in Figure 5a. The voltage feedback gain in Figure 5a consits of the voltage amplifier gain, the current amplifier gain, the PWM gain as well as the fixed gain of 1.5. The total gain (solid) and phase (dashed) of the voltage loop are shown in Figure 5b.

Reference

[1] L. Dixon, "Average Current Mode Control of Switching Power Supplies", Unitrode Power Supply Design Seminar, SEM700, Topic 5

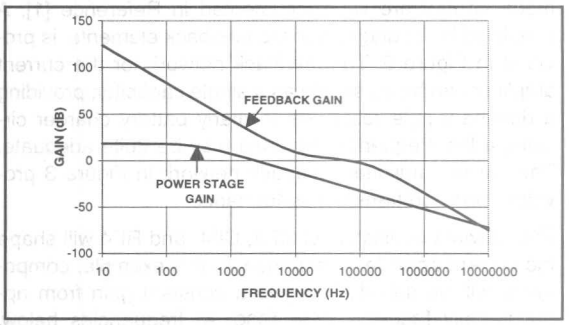


Figure 5a. Voltage Loop Power Stage and Feedback Gains

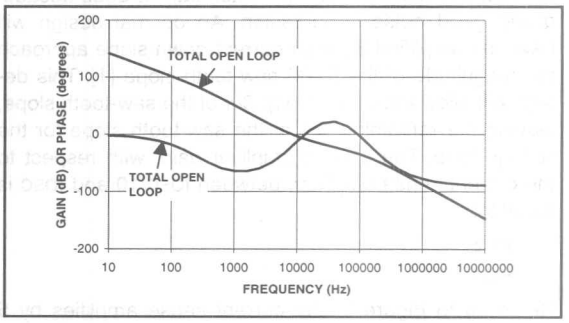


Figure 5b. Voltage Loop Total Gain and Phase

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UNITRODE

Three - Four Cell Lithium-Ion Protector Circuit

ADVANCED INFORMATION

FEATURES

- Three or Four Cell Operation
- Two Tier Overcurrent Limiting Scheme
- 30µA Typical Supply Current Consumption
- 3.5µA Typical Supply Current in Sleep Mode
- State Transition Thresholds at 4.2V, 4V, 2.6V, and 2.3V
- 6.5V to 20V VDD Supply Range
- Highly Accurate Internal Voltage Reference
- Externally Adjustable Delays in Overcurrent Controller
- 20mS Typical Response Time to Cell Over-Voltage
- Detection of Loss of Cell Sense Connections

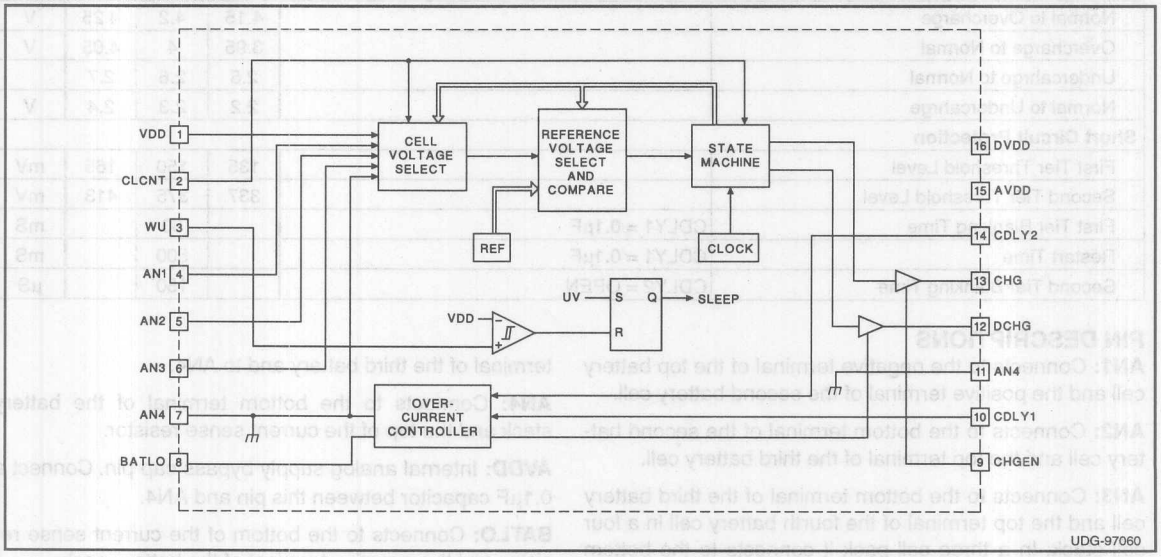
DESCRIPTION

The UCC3957 is a BiCMOS three or four cell lithium-ion battery pack protector designed to operate with external P-channel MOSFETs. Utilizing external P-channel MOSFETs provides the benefits of no loss of system ground in an overdischarge state, and protects the IC as well as battery cells from damage during an overcharge state. An internal state machine runs continuously to protect each lithium-ion cell from overcharge and overdischarge. A separate overcurrent protection block protects the battery pack from excessive discharge currents.

If any of the cell voltages exceeds the overvoltage threshold (4.2V), the appropriate external P-channel MOSFET is turned off, preventing further charge current. An external N-channel MOSFET is required to level shift to this high side P-channel MOSFET. Discharge current can still flow through the second PFET's body diode. Likewise, if any cell voltage falls below the undervoltage limit (2.3V), the second P-channel MOSFET is turned off and only charge current is allowed. Such a cell voltage condition will cause the chip to go into low power sleep mode. Attempting to charge the battery pack will wake up the chip. A cell count pin (CLCNT) is provided to program the IC for three or four cell operations.

A two tiered overcurrent controller and external current shunt protect the battery pack form excessive discharge currents. If the first overcurrent threshold level is exceeded, and internal timing circuit charges an external capacitor to provide a user programmable blanking time. If at the end of the blanking time the overcurrent condition still exists, the external discharge FET is turned off for a period 10 times longer than the first blanking period, and then the discharge FET is turned back on. If at any time a second higher overcurrent threshold is exceeded for more than 150µs, the discharge FET is turned off, and will remain off for the same period as the first tier off time. This two tiered overcurrent protection scheme allows for charging capacitive loads while retaining effective short circuit protection.

BLOCK DIAGRAM



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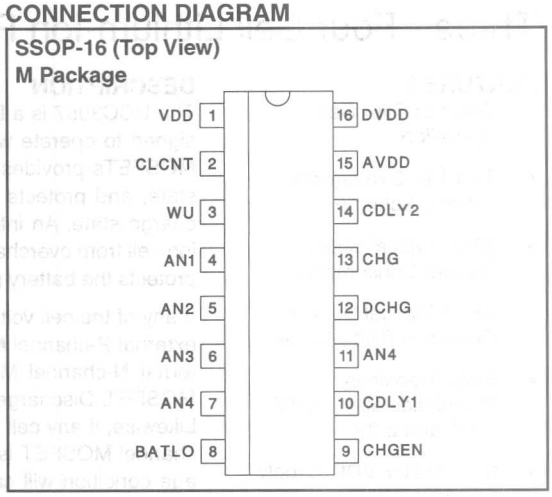
ABSOLUTE MAXIMUM RATINGS

Supply Voltage 20V
Supply Current 25mA
Output Current (CHG, DCHG) 25mA
WU Input Voltage 28V
BATLO Input Voltage ..... –0.3V to 2.5V
ANS1 and AN3 Input Voltage ..... VAN4 – VDD
CLCNT and CHGEN ..... VAN4 – VDD
Storage Temperature ..... –65°C to +150°C
Junction Temperature ..... –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

Unless otherwise indicated, voltages are referenced to AN4. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

SSOP-16 (Top View)
M Package



ELECTRICAL CHARACTERISTICS:

Unless otherwise specified, VDD = 16V and –20°C < TA < 70°C, TA = TJ. All voltages measured with respect to the AN4 terminal.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Section					
VDD		6.5		20	V
Supply Current			30	40	µA
Sleep Mode Supply Current			3.5	5	µA
Output Section					
DCHG Output Current	Driving Logic Low and Vo = 1V		70		µA
	Driving Logic High and Vo = VDD – 1		–7		mA
CHG Ouput Current	Driving Logic Low and Vo = 1V		70		µA
	Driving Logic High and Vo = VDD – 1V		–7		mA
State Transitions					
Normal to Overcharge		4.15	4.2	4.25	V
Overcharge to Normal		3.95	4	4.05	V
Undercahrge to Normal		2.5	2.6	2.7	
Normal to Undercahrge		2.2	2.3	2.4	V
Short Circuit Protection					
First Tier Threshold Level		135	150	165	mV
Second Tier Threshold Level		337	375	413	mV
First Tier Blanking Time	CDLY1 = 0.1µF		50		mS
Restart Time	CDLY1 = 0.1µF		500		mS
Second Tier Blanking Time	CDLY2 = OPEN		150		µS

PIN DESCRIPTIONS

AN1: Connects to the negative terminal of the top battery cell and the positive terminal of the second battery cell.

AN2: Connects to the bottom terminal of the second battery cell and the top terminal of the third battery cell.

AN3: Connects to the bottom terminal of the third battery cell and the top terminal of the fourth battery cell in a four cell stack. In a three cell pack it connects to the bottom terminal of the third battery and to AN4.

AN4: Connects to the bottom terminal of the battery stack and the top of the current sense resistor.

AVDD: Internal analog supply bypass cap pin. Connect a 0.1µF capacitor between this pin and AN4.

BATLO: Connects to the bottom of the current sense resistor and the negative terminal of the battery pack.

PIN DESCRIPTIONS

CHGEN: The charge enable input for the protection IC. This point must be driven high to allow charging of the battery pack.

CDLY1: Delay control pin for the short circuit protection feature. A capacitor connected between this point and AN4 will determine the time delay from when an overcurrent situation is detected to when the off. This capacitor also controls the hiccup mode timeout period.

CDLY2: An external cap can be tied between this pin and AN4 to extend the blanking time on the second current limit tier.

CLCNT: This pin programs the IC for three or four cell operation. Tying this pin low (to AN4) sets four cell operation, while tying it high (to VDD or the preferred DSPLY or ASPLY) sets three cell operation. pulled low, so open circuit conditions will always result in four cell mode.

DCHG: This pin is used to prevent overdischarge. If the state machine indicates that any cell is undervoltage, this pin will be driven high with respect to chip substrate so that the external P-channel further discharge. If all cell voltages are above the minimum threshold, this pin will be driven low.

CHG: This pin is used to control an external N-channel MOSFET, which in turn drives a P-channel MOSFET. If at least one cell voltage is over the OV threshold, this pin will be driven low with respect to chip voltages are below this threshold, this pin will be driven high.

DVDD: Internal digital supply bypass capacitor pin. Connect a 0.1µF capacitor between this pin and AN4.

VDD: Supply voltage to the IC. Connect this point to the top of the lithium-ion battery stack.

WU: This pin is used to provide a wake up signal to the IC during sleep mode. Connect this pin to the drain of the N-channel level shift MOSFET.

DESCRIPTION OF OPERATION

Cell Voltage Select

The Cell Voltage Select circuit employs a "flying-capacitor" to sample the voltage across each battery cell and then present the sampled voltage to the Reference Voltage Select and Compare block. If one of the lines AN1, AN2, (or AN3 in four cell mode) becomes disconnected a special feature of the Cell Voltage Select block will cause cells that were connected to the broken line to appear to be overvoltage and consequently disallow recharging of the pack.

Reference Voltage Select and Compare

The function of this block is to take the level shifted battery cell voltages from the Cell Voltage Select block and compare it against each of the four internal state transition thresholds. If any battery cell is found above the OV threshold, further charging of the entire pack is inhibited. If any cell if found to be below the UV threshold, then further discharging is inhibited and the chip puts itself into sleep mode in which current consumption is only about 3.5uA. The other two thresholds are called OV to Normal and UV to Normal. The chip exits the OV condition when all cells are found to be less than the OV to Normal threshold. It exits the UV condition when all cells are found to be above the UV to Normal threshold.

State Machine

There is only one comparator in the Reference Voltage Select and Compare block to reduce supply current consumption. The results of all the various comparisons done in this block are accumulated in a shift register in the State Machine. As its name would imply the State Machine block also contains a state machine that remembers what the current state is and based on the comparison results, decides what the next state should be.

Circuitry in the state machine block controls what battery cell will be looked at with the Cell Voltage Select block as well as what Referenc voltage the sampled battery voltage will be compared against in the Reference Voltage Select and Compare block.

Overcurrent Controller

Overcurrent protection circuitry operates in a hiccup mode to protect against excessive discharge currents. When the voltage drop across the external current shunt resistor exceeds the lower threshold level, an internal timer is started. Assuming that the upper threshold is not crossed when it times out, the discharge FET switch is turned off disabling further discharge current. Time out of the first timer triggers the start of a second timer that has ten times the delay of the first. When it times out, the discharge FET is re-enabled. If the load impedance is such that the upper threshold is crossed before the first timer times out, then the discharge FET is disabled after a nominal delay of 150µS; the first timer continues until it times out. The second timer then runs until it times out, and the discharge FET is then re-enabled.

DESCRIPTION OF OPERATION

Reference

The Reference block houses the precision voltage Reference for the chip. It provides the threshold levels to the Reference Voltage Select and Compare block as well as providing Referenceerence levels to the Overcurrent Controller and the Clock. It is curvature corrected to provide for better accuracy over temperature.

Clock

The Clock block houses the master timing oscillator for the chip. It runs at a base frequency of approximately 7.5kHz. The internal clock drives the Sleep Controller and the State Machine.

Sleep Controller

The Sleep Controller is shown in conceptual form on the block diagram. When it detects that the State Machine has declared a UV condition, it asserts the internal SLEEP signal. The SLEEP signal causes the internal Clock to freeze on a logic high, and it causes almost all of the analog functions on the chip to power down. It also powers up the comparator that monitors the WU (Wake Up) input. When it detects that the WU input level is slightly more positive in potential than the VDD input, it resets the flip-flop that generates the Sleep signal causing operation to continue at the same point the chip went to sleep.

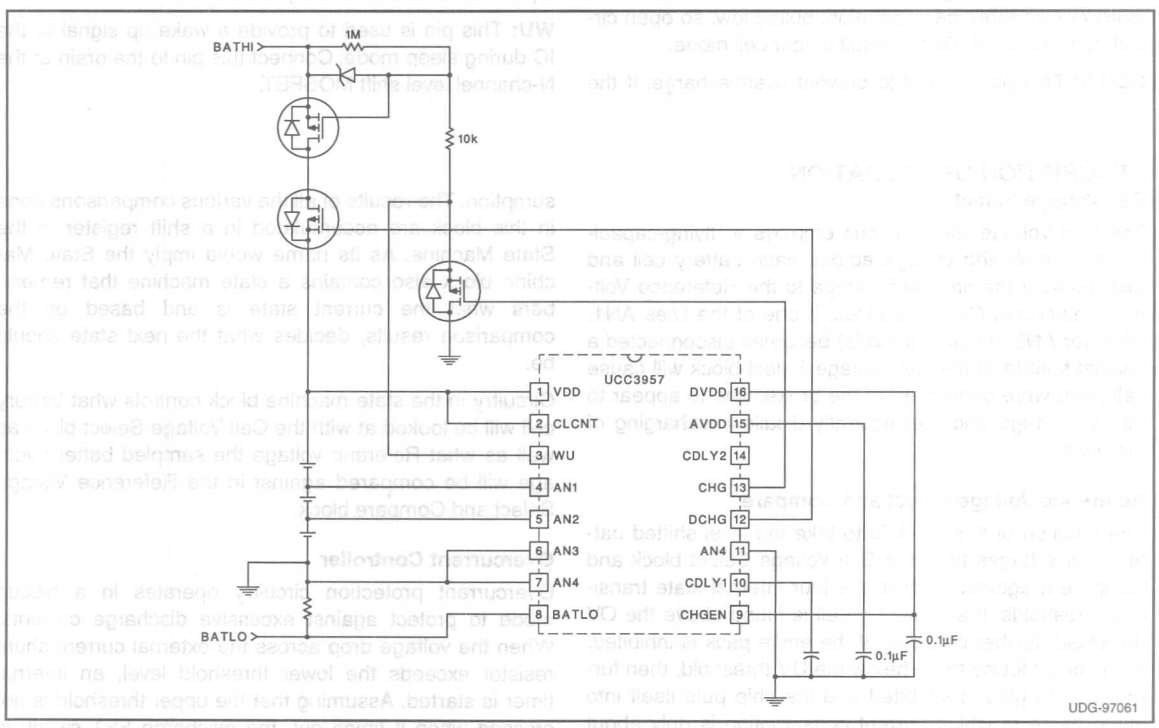


Figure 1. Three Cell Lithium-Ion Protector Application Diagram

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IrDA Receiver

FEATURES

- Micro Power, 90µA Typical Operating Current
- 3.3V or 5V Operation
- 8-Pin SOIC Package
- 1 cm to 1 Meter IrDA Link Compliance
- Directly Interfaces to IrDA Compatible UARTS and Super I/O Chips
- Supports Data Rates from 2400 to 115.2KBits/Second
- CMOS/TTL Compatible Output
- ASK Modulation Compatible
- Drop in compatible with Irvine Sensor SIR2

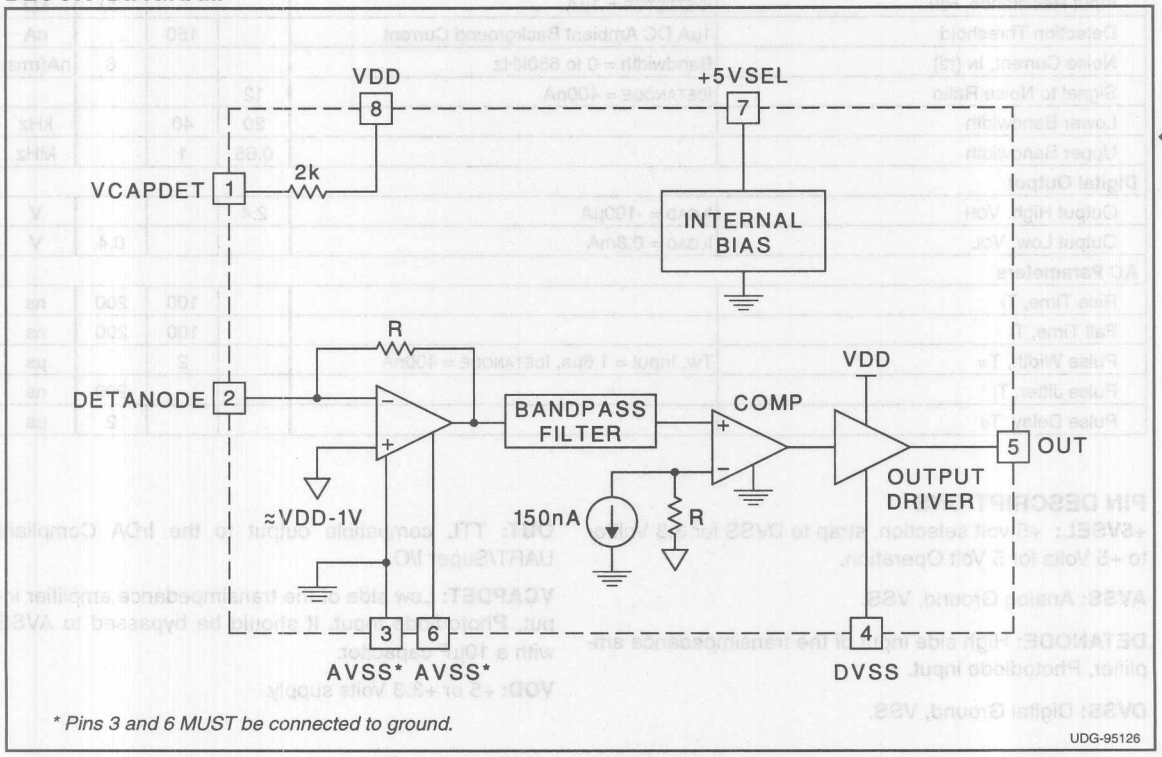
DESCRIPTION

The UCC5340 is a dual voltage, micropower, IrDA (Infrared Data Association) compliant receiver. It's high gain photodiode input amplifier incorporates a unique limiting circuit which permits operation over a very wide dynamic input range. The integrated bandpass filter includes additional limiting circuitry, further reducing device recovery time requirements, allowing the UCC5340 to directly interface with IrDA compatible detector diodes.

The output is capable of driving a 40pF load at CMOS/TTL levels for direct interfacing to IrDA compliant UARTs or Super I/O devices over a 2400BPS to 115.2kBPS range.

A control pin is provided to allow operation with either 3.3V or 5V supplies. The circuit requires only 90µA (nominal) operating current in either configuration. An internal 2kΩ resistor is provided for decoupling the detector supply, to minimize the number of external components required.

BLOCK DIAGRAM



** Pins 3 and 6 MUST be connected to ground.*

UDG-95126

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ABSOLUTE MAXIMUM RATINGS

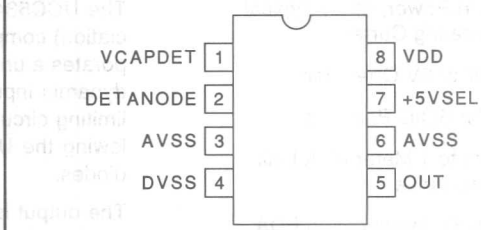
VDD ..... –0.3V TO +6V
Voltage at +5VSEL (r.t. GND) ..... –0.3V to VDD
Input Source Current to DETANODE..... 20mA
Package Power Dissipation 25mW
Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... –55°C to +125°C
Currents are positive into, negative out of the specified terminal.
Consult Packaging Section of Databook for thermal limitations and considerations of packages.

RECOMMENDED OPERATING CONDITIONS

VCC Voltage..... 3.0V to 5.5V

CONNECTION DIAGRAM

DIL-8, SOIC-8 (Top View)
N or D Packages



ELECTRICAL CHARACTERISTICS

Unless otherwise specified, 3.0V ≤ VDD ≤ 3.5V and +5VSEL = GND, or 4.5V ≤ VDD ≤ 5.5V and +5VSEL = VDD, $C_{DETECTOR}$ < 56pF, C_{LOAD} = 40pF, 0°C < T_A < 70°C, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current, I_{DD}	No Load, $I_{DETANODE}$ = 1µA		90	150	µA
Detector Decoupling Resistance, R_{DD}			2.0	3.0	kΩ
+5VSEL Input Leakage		–10		10	µA
Detector Amplifier					
I_{PDmax}	VDD = 3V	3	4		mA
	VDD = 5V	5			mA
Input Resistance, R_{IN}	$I_{DETECTOR}$ = 1µA			20	kΩ
Detection Threshold	1µA DC Ambient Background Current		150		nA
Noise Current, I_N (rti)	Bandwidth = 0 to 650kHz			6	nA(rms)
Signal to Noise Ratio	$I_{DETANODE}$ = 400nA	12			
Lower Bandwidth		20	40		kHz
Upper Bandwidth		0.65	1		MHz
Digital Output					
Output High, V_{OH}	I_{LOAD} = -100µA	2.4			V
Output Low, V_{OL}	I_{LOAD} = 0.8mA			0.4	V
AC Parameters					
Rise Time, T_r			100	200	ns
Fall Time, T_f			100	200	ns
Pulse Width, T_w	Tw, Input = 1.6µs, $I_{DETANODE}$ = 400nA		2		µs
Pulse Jitter, T_j				200	ns
Pulse Delay, T_d				2	µs

PIN DESCRIPTIONS

+5VSEL: +5 volt selection, strap to DVSS for 3.3 Volt or to +5 Volts for 5 Volt Operation.

AVSS: Analog Ground, VSS.

DETANODE: High side input of the transimpedance amplifier, Photodiode input.

DVSS: Digital Ground, VSS.

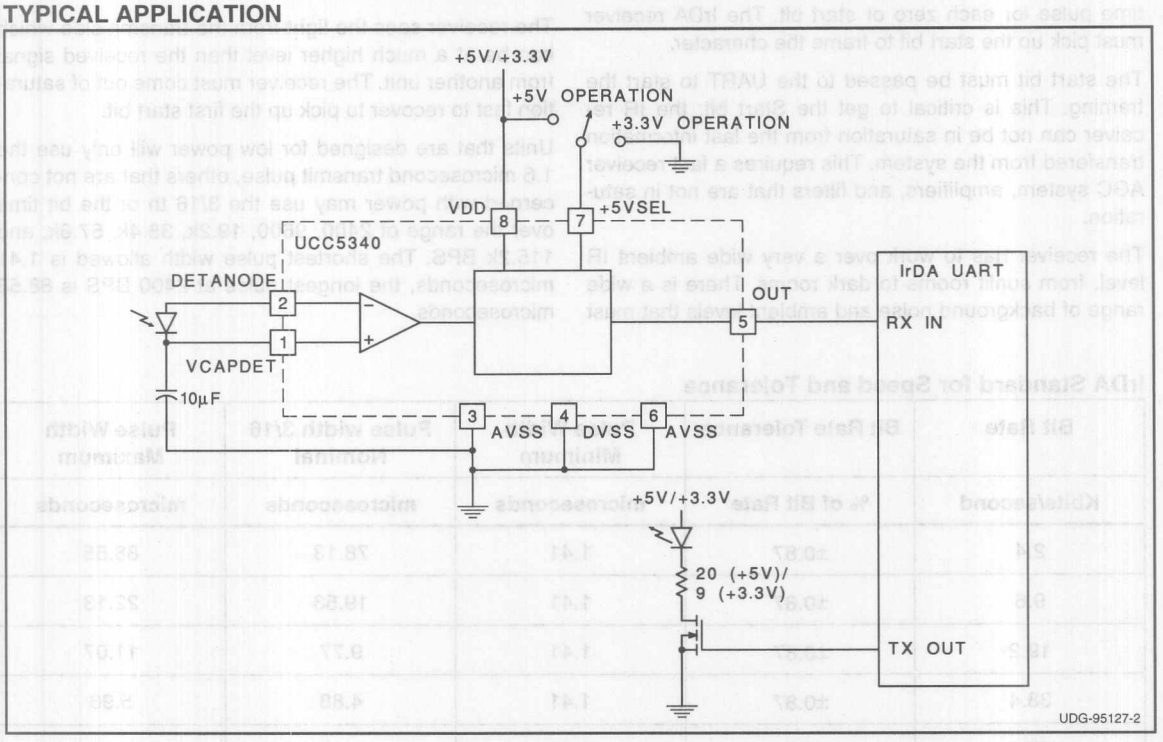
OUT: TTL compatible output to the IrDA Compliant UART/Super I/O.

VCAPDET: Low side of the transimpedance amplifier input, Photodiode input. It should be bypassed to AVSS with a 10µF capacitor.

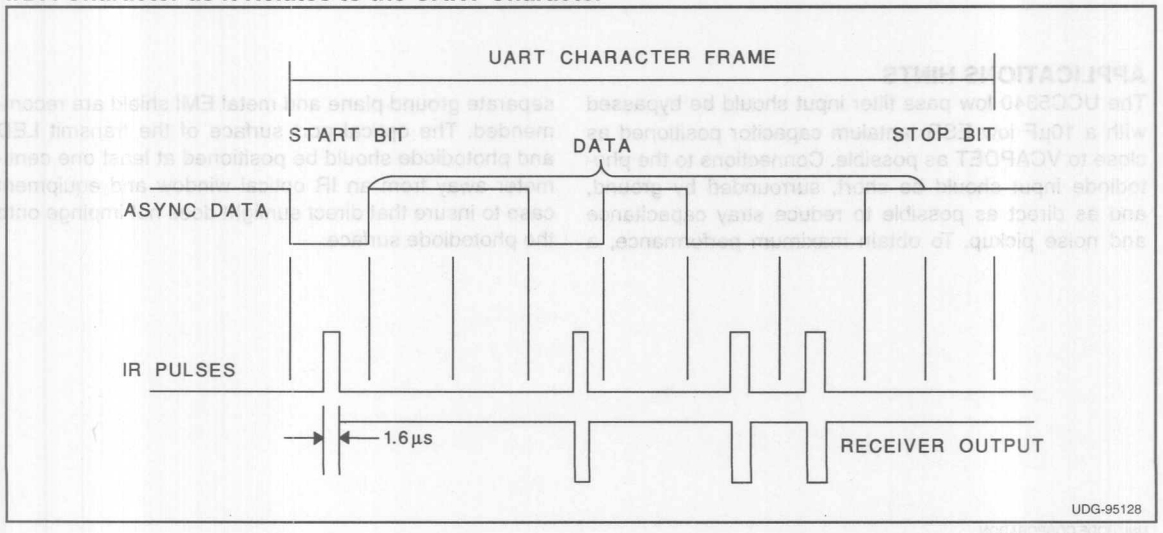
VDD: +5 or +3.3 Volts supply.

APPLICATIONS INFORMATION

TYPICAL APPLICATION



IrDA Character as it Relates to the UART Character



APPLICATIONS INFORMATION (cont.)

The IrDA stream is a 1.6 microsecond or 3/16 th of a bit time pulse for each zero or start bit. The IrDA receiver must pick up the start bit to frame the character.

The start bit must be passed to the UART to start the framing. This is critical to get the Start bit, the IR receiver can not be in saturation from the last information transfered from the system. This requires a fast receiver AGC system, amplifiers, and filters that are not in saturation.

The receiver has to work over a very wide ambient IR level, from sunlit rooms to dark rooms. There is a wide range of background noise and ambient levels that must be filtered out.

The receiver sees the light from the transmit side which can be at a much higher level than the received signal from another unit. The receiver must come out of saturation fast to recover to pick up the first start bit.

Units that are designed for low power will only use the 1.6 microsecond transmit pulse, others that are not concerned with power may use the 3/16 th of the bit time over the range of 2400, 9600, 19.2k, 38.4k, 57.6k, and 115.2k BPS. The shortest pulse width allowed is 1.41 microseconds, the longest pulse at 2400 BPS is 88.55 microseconds.

IrDA Standard for Speed and Tolerance

Bit Rate	Bit Rate Tolerance	Pulse Width Minimum	Pulse width 3/16 Nominal	Pulse Width Maximum
Kbits/second	% of Bit Rate	microseconds	microseconds	microseconds
2.4	±0.87	1.41	78.13	88.55
9.6	±0.87	1.41	19.53	22.13
19.2	±0.87	1.41	9.77	11.07
38.4	±0.87	1.41	4.88	5.96
57.6	±0.87	1.41	3.26	4.34
115.2	±0.87	1.41	1.63	2.71

APPLICATIONS HINTS

The UCC5340 low pass filter input should be bypassed with a 10µF low ESR tantalum capacitor positioned as close to VCAPDET as possible. Connections to the photodiode input should be short, surrounded by ground, and as direct as possible to reduce stray capacitance and noise pickup. To obtain maximum performance, a separate ground plane and metal EMI shield are recommended. The optical port surface of the transmit LED and photodiode should be positioned at least one centimeter away from an IR optical window and equipment case to insure that direct sunlight does not impinge onto the photodiode surface.

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IrDA 2.4kbps to 115.2kbps Receiver

FEATURES

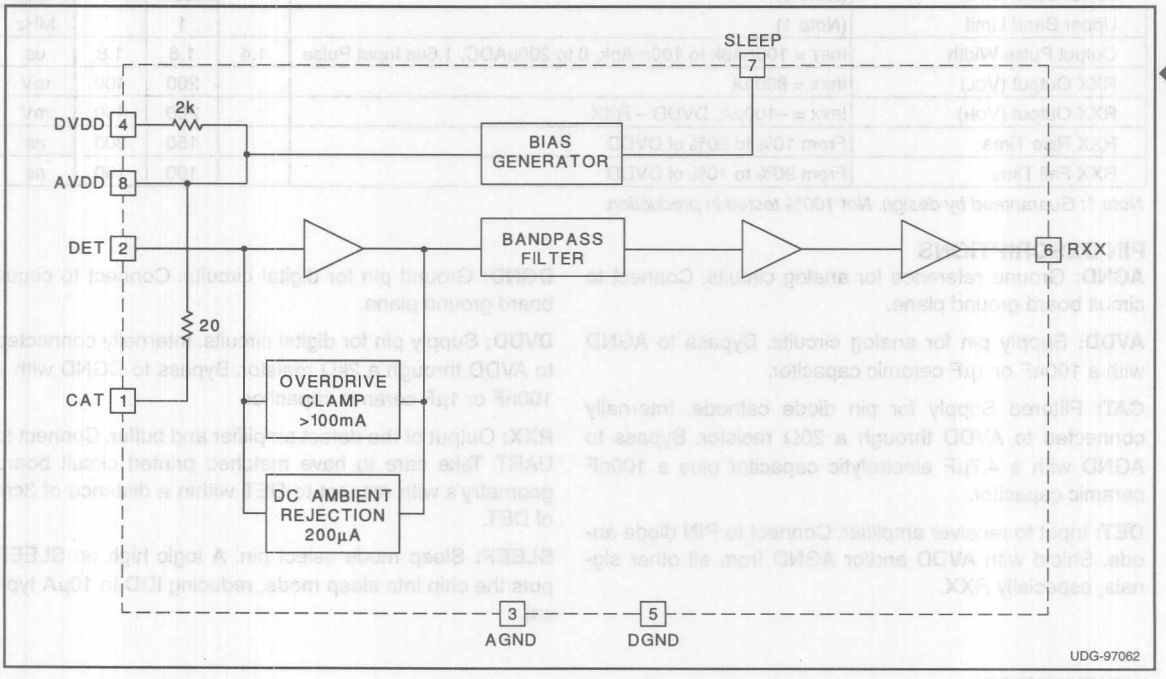
- Supports IrDA 2.4kbps to 115.2kbps Data Rates
- 3.3V and 5V Operation
- Wide Dynamic Receiver Range from 100nA to 100mA Typical
- IrDA Compliant I/O
- Very Low Quiescent Current In Active Mode (250µA Typical)
- Ultra Low Quiescent Current In Sleep Mode (10µA Typical)
- Compatible with IrDA Detector Diodes

DESCRIPTION

The UCC5341 IrDA (Infrared Data Association) Receiver supports the analog section of the IrDA standard. It has a limiting transresistance amplifier to detect a current signal from a PIN diode and drives RXX pulses to a UART. The amplifier is capable of input currents ranging from 100nA to greater than 100mA. The UCC5341 is bandpass limited to reduce interference from other IR sources. The UCC5341 also has very low current consumption in the active mode (250µA typically), making it excellent for power sensitive applications.

The output of the receiver is designed to drive CMOS and TTL levels, for direct interfacing to IrDA compliant UARTs and Super I/O devices, over the 2.4kbps to 115.2kbps range. Internal resistors are provided for decoupling the detector diode supply, thus minimizing the number of external components required.

BLOCK DIAGRAM



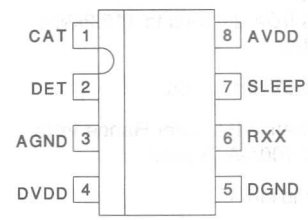
ABSOLUTE MAXIMUM RATINGS

AVDD, CAT, DVDD ..... –0.3V to 7V
CAT DET, DVDD, SLEEP, ... –0.3V to AVDD + 0.3V
IRXX ..... –10mA to 10 mA
IDET 250mA
Storage Temperature ..... –65°C to +150°C
Junction Temperature ..... –55°C to +150°C
Lead Temperature (Soldering, 10sec.) ..... +300°C

All voltages are with respect to respect to AGND. DGND must be connected to AGND. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of the Databook for thermal limitations and considerations of packages.

ABSOLUTE MAXIMUM RATINGS

SOIC-8 (Top View)
D, N Package



ELECTRICAL CHARACTERISTICS: Unless otherwise specified, T_A = 0°C to 70°C, AVDD = 3V to 5.5V, C_{AVDD} = 100nF, C_{DVDD} = 100nF, C_{CAT} = 4.7µF + 100nF, C_{RXX} = 40nF, C_{DET} < 56pF. All currents are positive into a specified pin. $T_A = T_J$

PARAMETER	TEST CONDITION	MIN	TYPE	MAX	UNITS
Supply Current Section					
I_{DD}	No Output Load, IDET = 1µA DC		250	350	µA
I_{DD}	SLEEP = V_{DD}		10	20	µA
R_{DVDD}	AVDD to DVDD	1.5	2	2.5	kΩ
R_{CAT}	AVDD to CAT	15	20	25	Ω
Receiver Section					
Input Refered Noise			10		pA/√Hz
Detection Threshold			100	150	nA
Signal to Noise Ratio	IDET = 150nA		11.8		nA
Lower Band Limit	(Note 1)		50		kHz
Upper Band Limit	(Note 1)		1		MHz
Output Pulse Width	IDET = 100nApk to 100mApk, 0 to 200µADC, 1.6us Input Pulse	1.4	1.6	1.8	us
RXX Output (V_{OL})	I_{RXX} = 800µA		200	400	mV
RXX Output (V_{OH})	I_{RXX} = –100µA, DVDD – RXX		200	400	mV
RXX Rise Time	From 10% to 90% of DVDD		150	200	ns
RXX Fall Time	From 90% to 10% of DVDD		100	150	ns

Note 1: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

AGND: Ground reference for analog circuits. Connect to circuit board ground plane.

AVDD: Supply pin for analog circuits. Bypass to AGND with a 100nF or 1µF ceramic capacitor.

CAT: Filtered Supply for pin diode cathode. Internally connected to AVDD through a 20Ω resistor. Bypass to AGND with a 4.7µF electrolytic capacitor plus a 100nF ceramic capacitor.

DET: Input to receiver amplifier. Connect to PIN diode anode. Shield with AVDD and/or AGND from all other signals, especially RXX.

DGND: Ground pin for digital circuits. Connect to circuit board ground plane.

DVDD: Supply pin for digital circuits. Internally connected to AVDD through a 2kΩ resistor. Bypass to DGND with a 100nF or 1µF ceramic capacitor.

RXX: Output of the detect amplifier and buffer. Connect to UART. Take care to have matched printed circuit board geometry's with respect to DET within a distance of 3cm of DET.

SLEEP: Sleep mode select pin. A logic high on SLEEP puts the chip into sleep mode, reducing IDD to 10µA typical.

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IrDA 2.4kbps to 115.2kbps Transceiver

FEATURES

- Supports IrDA 2.4kbps to 115kbps Data Rates
- 3.3V and 5V Operation
- Wide Dynamic Receiver Range from 100nA to 100mA Typical
- IrDA Compliant I/O
- 500mA LED Driver
- Very Low Quiescent Current in Active Mode (250µA Typical)
- Ultra Low Quiescent Current in Sleep Mode (10µA Typical)
- Compatible with IrDA Detector Diodes
- Available in both 8 and 14 Pin Packages

DESCRIPTION

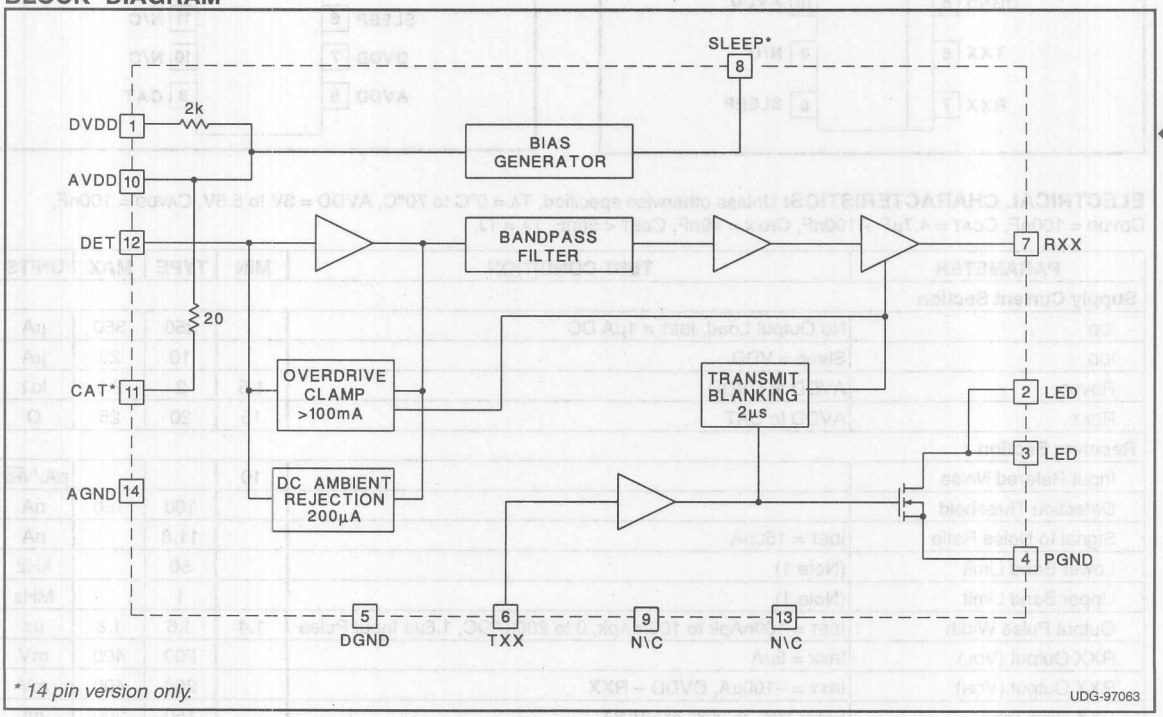
The UCC5342 IrDA (Infrared Data Association) Transceiver supports the analog section of the IrDA standard. The receiver has a limiting transresistance amplifier to detect a current signal from a PIN diode and drives RXX pulses to a UART. The amplifier is capable of input currents ranging from 100nA to greater than 100mA. The amplifier is bandpass limited to reduce interference from other IR sources.

The output of the receiver is designed to drive CMOS and TTL levels, for direct interfacing to IrDA compliant UARTs and Supper I/O devices, over the 2.4kbps to 115.2kbps range. Internal resistors are provided for decoupling the detector diode supply, thus minimizing the number of external components required.

The UCC5342 also has very low current consumption in the active mode (250µA typically), making it excellent for power sensitive applications. In the 14 pin packaged version, the UCC5342 also has a sleep mode, further reducing current to conserve battery power.

The transmitter portion of the chip has a low impedance open drain MOSFET output. It is capable of sinking 200mA from an output LED at 3.3V, and 500mA at 5V.

BLOCK DIAGRAM



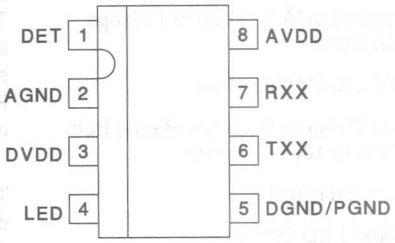
ABSOLUTE MAXIMUM RATINGS

AVDD, DVDD, CAT ..... –0.3V to 7V
SLEEP, DET, TXX, LED,
DVDD, CAT ..... –0.3mA to AVDD + 0.3mA
IRXX ..... –10mA to 10 mA
IDET 250mA
ILED 1A
Storage Temperature ..... –65°C to +150°C
Junction Temperature ..... –55°C to +150°C
Lead Temperature (Soldering, 10sec.) ..... +300°C

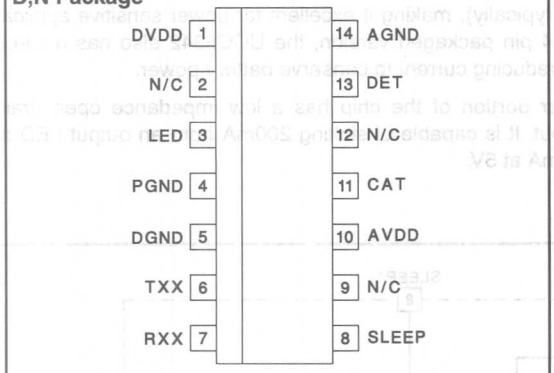
All voltages are with respect to respect to AGND. DGND and PGND must be connected to AGND. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of the Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

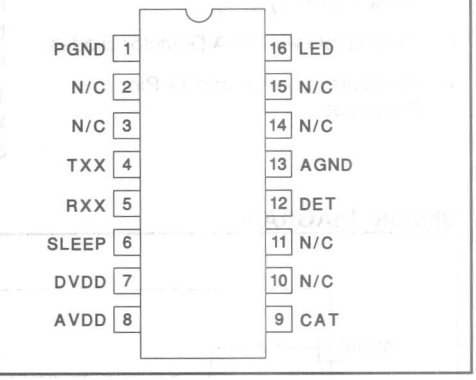
SOIC-8 (Top View)
D, N Package



SOIC-14 (Top View)
D,N Package



SSOP-16 (Top View)
M Package



ELECTRICAL CHARACTERISTICS: Unless otherwise specified, T_A = 0°C to 70°C, AVDD = 3V to 5.5V, C_{AVDD} = 100nF, C_{DVDD} = 100nF, C_{CAT} = 4.7µF + 100nF, C_{RXX} = 40nF, C_{DET} < 56pF. T_A = T_J.

PARAMETER	TEST CONDITION	MIN	TYPE	MAX	UNITS
Supply Current Section					
IDD	No Output Load, IDET = 1µA DC		250	350	µA
IDD	Sleep = VDD		10	20	µA
RDVDD	AVDD to DVDD	1.5	2	2.5	kΩ
RCAT	AVDD to CAT	15	20	25	Ω
Receiver Section					
Input Refered Noise		10			pA/√Hz
Detection Threshold			100	150	nA
Signal to Noise Ratio	IDET = 150nA		11.8		nA
Lower Band Limit	(Note 1)		50		kHz
Upper Band Limit	(Note 1)		1		MHz
Output Pulse Width	IDET = 100nApk to 100mApk, 0 to 200µADC, 1.6µs Input Pulse	1.4	1.6	1.8	µs
RXX Output (VOL)	IRXX = 8µA		200	400	mV
RXX Output (VOH)	IRXX = –100µA, DVDD – RXX		200	400	mV
RXX Rise Time	From 10% to 90% of DVDD		150	200	ns
RXX Fall Time	From 90% to 10% of DVDD		100	150	ns

ELECTRICAL CHARACTERISTICS (cont.): Unless otherwise specified, T_A = 0°C to 70°C, AVDD = 3V to 5.5V, C_{AVDD} = 100nF, C_{DVDD} = 100nF, C_{CAT} = 4.7µF + 100nF, C_{RXX} = 40nF, C_{DET} < 56pF. T_A = T_J.

PARAMETER	TEST CONDITION	MIN	TYPE	MAX	UNITS
Transmitter Section					
I_{TXX}	TXX = 0 to AVDD	–10		10	µA
TXX (V_{IH})			2	2.5	V
TXX (V_{IL})		0.8	1		V
LED	TXX = AVDD = 4.5V, I_{LED} = 500mA		0.3	0.6	V
	TXX = AVDD = 3V, I_{LED} = 300mA		0.3	0.6	V
I_{LED}	TXX = 0, LED = AVDD = 5.5V			10	µA

Note 1: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

AGND: Ground reference for analog circuits. Connect to circuit board ground plane.

AVDD: Supply pin for analog circuits. Bypass to AVSS with a 100nF or 1µF ceramic capacitor.

CAT: (14 Pin Version Only) Filtered supply for pin diode cathode. Internally connected to AVDD with a 20Ω resistor. Bypass to AVSS with a 4.7µF electrolytic capacitor plus a 100nF ceramic capacitor.

DET: Input to receiver amplifier. Connect to pin diode anode. Shield with a AVDD and/or AVSS from all other signals, especially RXX.

DGND: Ground pin for digital circuits. Connect to circuit board ground plane.

DVDD: Supply pin for digital circuits. Internally connected to AVDD with a 2kΩ resistor. Bypass to DVSS with a 100nF or 1µF ceramic capacitor.

LED: Open drain of transmitter output transistor. Connect to an external transmitting LED and current limiting series resistor.

PGND: Source of transmitter output transistor. Connect to circuit board ground plane. Common to DVSS in the 8 pin version.

RXX: Output of the detect amplifier and buffer. Connect to UART. Take care to have matched printed circuit board geometry's with respect to DET within a distance of 3cm of DET.

SLEEP: (14 Pin Version Only) Sleep mode select pin. A logic high on SLEEP puts the chip into sleep mode, reducing IDD to 10µA typical.

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IrDA Transceiver with Encoder/Decoder

FEATURES

- Micropower in the Receive Mode, (10µA)
- 3.3V and 5.5V Operation
- Wide Dynamic Receiver Range from 100nA to 100mA Typical
- Direct Interface to IrDA Compatible UARTs or Super I/O ICs
- Supports Data Rates from 2.4kbps to 115.2kbps
- Transmitter Output Stage Capable to 500mA Sink Current
- IrDA Compliant Modulation & Demodulation Scheme
- Direct Interface to Standard UART
- 16 Pin SSOP or SOIC Package

DESCRIPTION

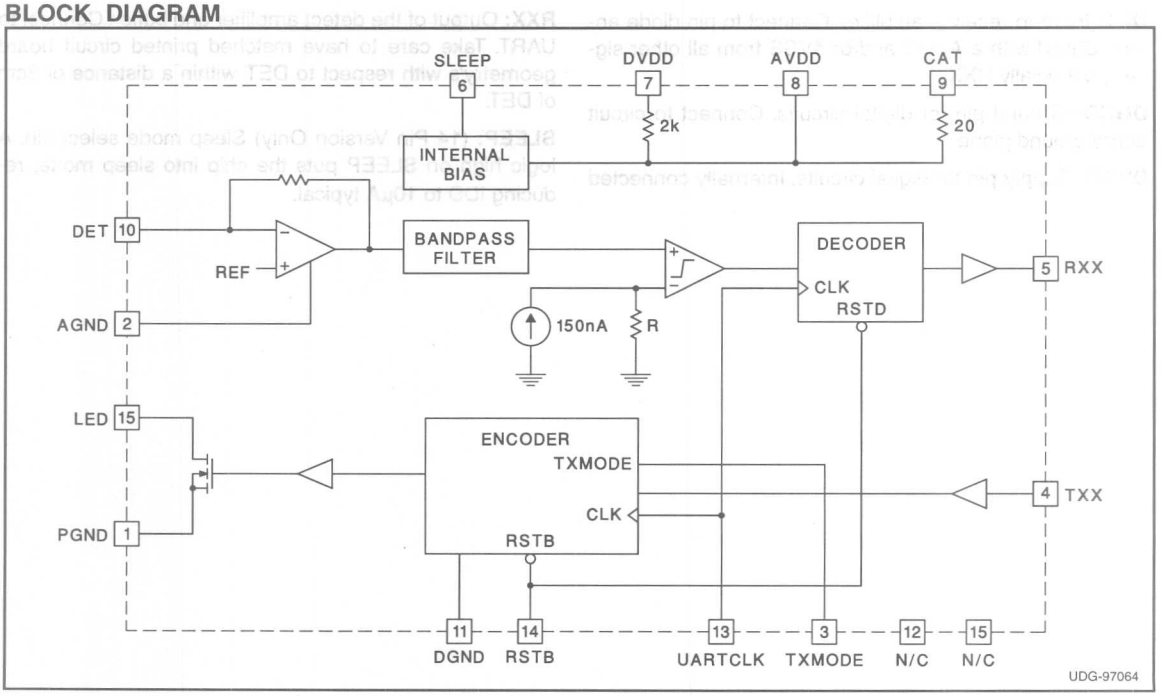
The UCC5343 IrDA Transceiver with Encoder/Decoder supports the Physical Layer specifications of the IrDA standard. Additional functionality is provided by data format translation between standard UART and IrDA formats. The UCC5343 is readily interfaced to a standard UART.

The Receiver has a limiting transresistance amplifier to detect a current signal from a pin diode and drives RXX pulses into a UART. The receiver is capable of detecting input currents ranging from 100nA to greater than 100mA. The receiver signal path is frequency limited by an internal bandpass filter to reduce interference from other sources of IR energy.

The output of the receiver is designed for direct interface to standard UARTs and Super I/O devices over the range of 2.4kbps to 155.2kbps. Internal resistors are provided for decoupling the pin diode supply, minimizing the number of required external components.

The UCC5343 has low current consumption in the active mode, making it excellent for applications with low power requirements. The transmitter section has a low impedance open drain MOSFET output. It is capable of sinking 300mA from an output LED at 3.3V and 500mA at LED at 5V.

BLOCK DIAGRAM



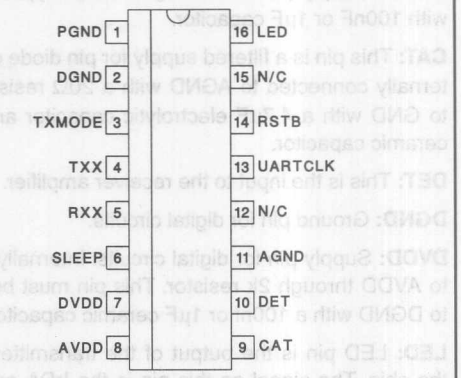
ABSOLUTE MAXIMUM RATINGS

AVDD, DVDD, CAT ..... –0.3V to 7V
SLEEP, DET, TXX, LED,
DVDD, CAT ..... –0.3mA to AVDD + 0.3mA
IRXX ..... –10mA to 10 mA
IDET 250mA
ILED 1A
Power Supply ..... TBA
Storage Temperature ..... –65°C to +150°C
Junction Temperature ..... –55°C to +150°C
Lead Temperature (Soldering, 10sec.) ..... +300°C

All voltages are positive with respect to AGND. DGND and PGND must be connected to AGND. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of the Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

SSOP-16, SOIC-16 (Top View)
M Package, D and N Packages



ELECTRICAL CHARACTERISTICS: Unless otherwise specified, 0°C < TA < 70°C TA = 0°C to 70°C, AVDD = 3V to 5.5V, CAVDD = 100nF, CDVDD = 100nF, CCAT = 4.7µF + 100nF, CRXX = 40nF, CDET < 56pF. TA = TJ.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current Section					
IDD	No Output Load, IDET = 1µA DC		280	400	µA
	SLEEP = AVDD		10	20	µA
RVDD	AVDD to DVDD	1.5	2	2.5	kΩ
RCAT	AVDD to CAT	15	20	25	Ω
Receiver Section					
Input Referred Noise			10		pA/√Hz
Detection Threshold			100	150	nA
DetectionThreshold Signal to Noise Ratio	IDET = 150nA			11.8	nA
Lower Band Limit	(Note 1)		50		kHz
Upper Band Limit	(Note 2)		1		MHz
Output Pulse Width	IDET = 100nA Peak to 100mA Peak and 0 to 200µADC, 1.6µS Peak	1.4	1.6	1.8	µS
RXX Output (VOL)	IRXX = 800µA		200	400	mV
RXX Output (VOH)	IRXX = –100µA, DVDD - RXX		200	400	mV
RXX Rise Time	10% to 90% of DVDD		150	200	nS
RXX Fall Time	90% to 10% of DVDD		100	150	nS
Transmitter Section					
ITXX	TXX = 0 to AVDD	–10		10	µA
TXX (VIH)	DVDD = 5	0.7 • DVDD		DVDD	V
TXX (VIL)	DVDD = 5	0		0.3 • DVDD	V
LED	TXX = AVDD = 4.5V, ILED = 500mA		0.3	0.6	V
	TXX = AVDD = 3V, ILED = 300mA		0.3	0.6	V
ILED	TXX = 0, LED = AVDD = 5.5V			10	µA
Encoder Transmit Direction					
Encoder Pulse Width	TXMODE = Logic 1	1.41		2.23	µS

Note 1: Guaranteed by Design. Not 100% tested in production.

PIN DESCRIPTIONS

AGND: Ground pin for analog circuits.

AVDD: Supply pin for analog circuits. Bypass to AGND with 100nF or 1µF capacitor.

CAT: This pin is a filtered supply for pin diode cathode. Internally connected to AGND with a 20Ω resistor. Bypass to GND with a 4.7µF electrolytic capacitor and a 100nF ceramic capacitor.

DET: This is the input to the receiver amplifier.

DGND: Ground pin for digital circuits.

DVDD: Supply pin for digital circuits. Internally connected to AVDD through 2k resistor. This pin must be bypassed to DGND with a 100nf or 1µF ceramic capacitor.

LED: LED pin is the output of the transmitter section of the chip. The signal on this pin is the IrDA encoded version of the UART transmit signal.

PGND: Ground pin for the transmitter power device. This pin should be connected to the circuit board ground plane.

RSTB: This active low input signal is used to reset the encoder and decoder sections of the chip. This signal must be provided by the system during startup.

RXX: RXX is the demodulated receive signal. Normally this pin is tied to SIN signal of UART. TTL/CMOS compatible output from the receiver stage to an IrDA UART. This output is digitally decoded (pulse stretched).

SLEEP: Sleep mode select pin. A logic high on SLEEP pin puts the chip into a low current mode.

TXMODE: TXMODE is used to select the modulation mode. If TXMODE is set high (1) the signal on TXD pin will have the output pulse width of 1.6µS. If TXMODE is set low (0), the output will have the pulse width of 3/16 of the UARTCLK frequency.

If TXMODE pin is left floating, the output will default to 1.6µS pulse width.

TXX: Input from the UART. This pin is normally tied to SOUT signal of UART.

UARTCLK: Input of the system clock. This frequency must set at 16 times the IrDA data rate, and must be available from the UART.

APPLICATION INFORMATION

Figures 1 and 2 outline the IrDA SIR encoding scheme. The encoding scheme relies on a clock being present. The clock must be set to 16 times the data transmission baud rate. The encoder sends a pulse for every space (0) that is sent. On a high to low transition of TXD signal, the generation of the pulse is delayed for 7 clock cycles of the 16XCLK before the pulse is set high for 3/16 of a bit time or 1.6µs the pulse width is selected by TXMODE. For consecutive spaces, pulses with 1 bit time delay are generated in series. If a logic 1 (mark) is sent, the encoder does not generate a pulse.

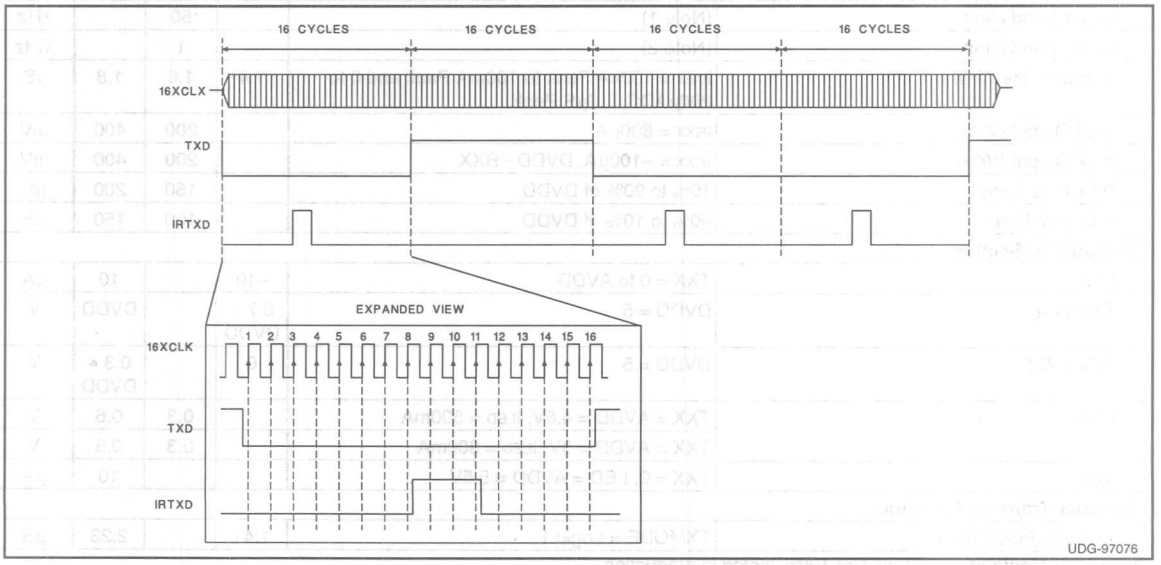


Figure 1. IrDA Encoder Timing Diagram

APPLICATION INFORMATION (cont.)

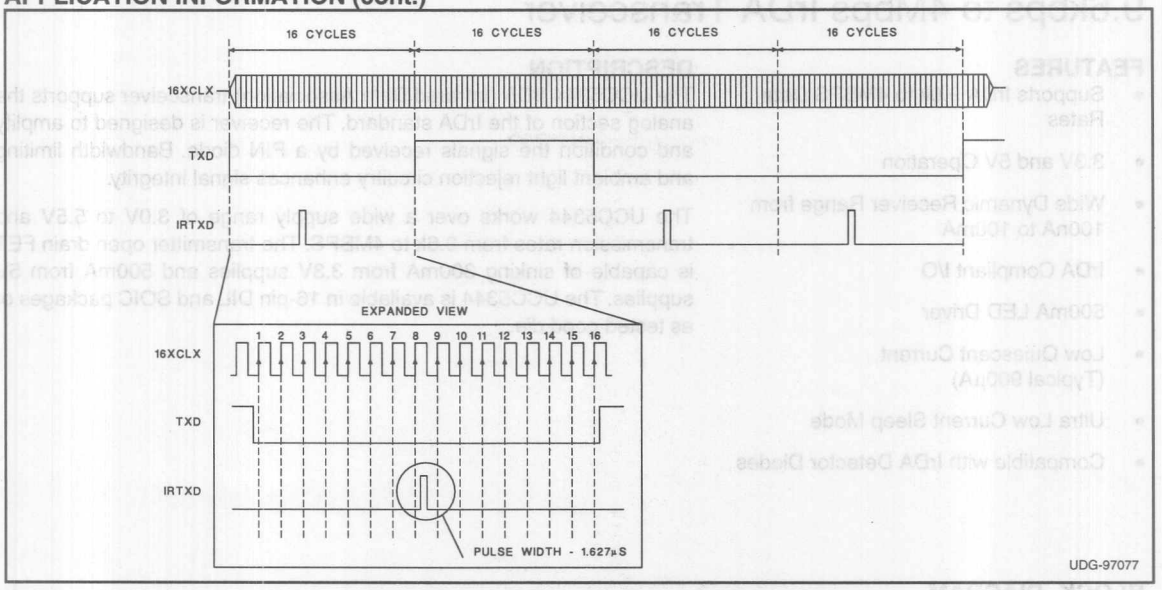


Figure 2. IrDA Encoder Timing Diagram (1.6µs Pulse Width)

The IrDA SIR decoding modulation method performs a pulse stretching function. Every high to low transition of the IRRXD line signifies an arrival of a 3/16th pulse. This pulse needs to be stretched to accommodate 1 bit time (or 16 of 16XCLK cycles). Every pulse that is received is translated into a space (0) on the RXD output. If a series of pulses separated by 1 bit time are received, then the result is a 1 bit time low pulse for every 3/16 pulse received. The decoding scheme is shown in Figure 3.

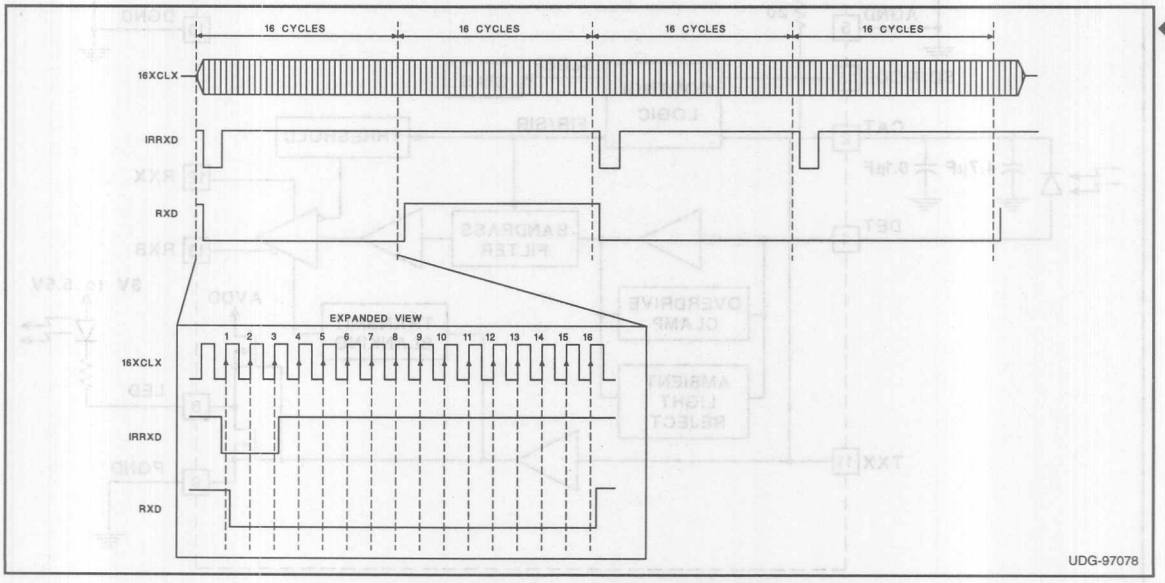


Figure 3. IrDA Decoder Timing Diagram

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9.6kbps to 4Mbps IrDA Transceiver

FEATURES

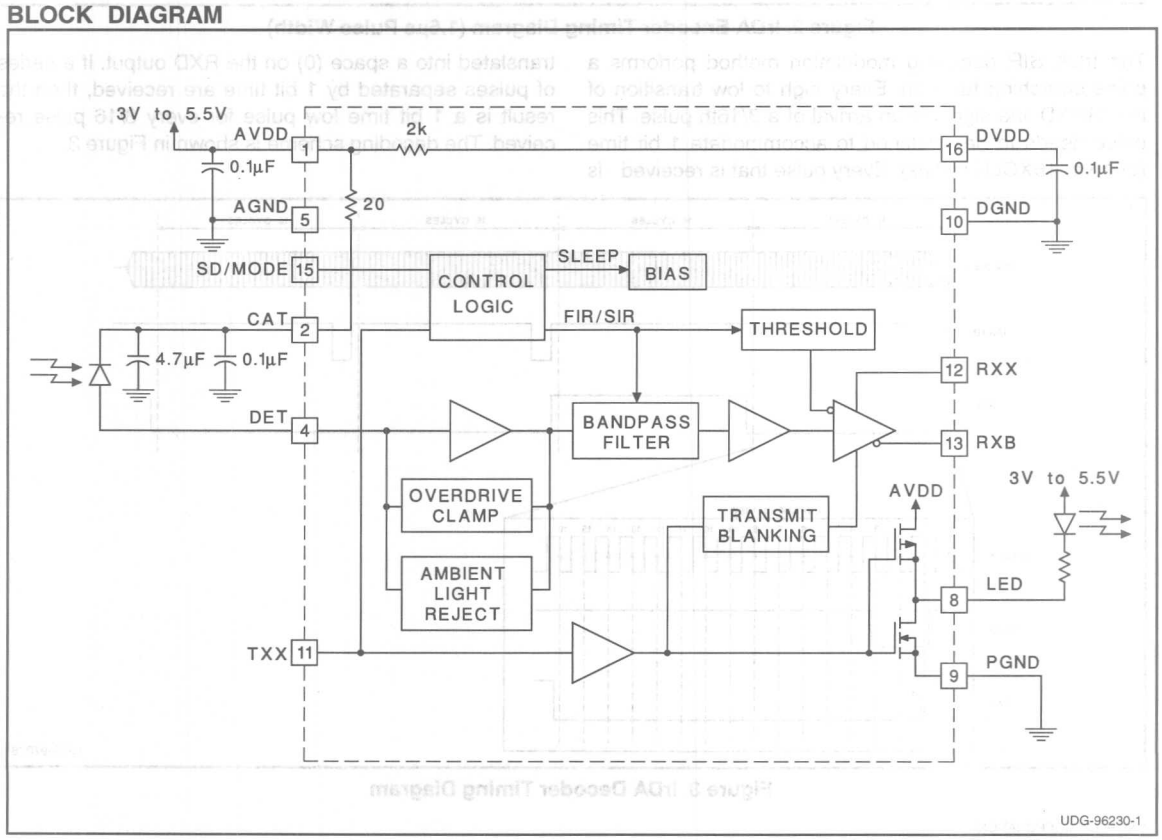
- Supports IrDA 9.6k to 4MBPS Data Rates
- 3.3V and 5V Operation
- Wide Dynamic Receiver Range from 100nA to 100mA
- IrDA Compliant I/O
- 500mA LED Driver
- Low Quiescent Current (Typical 900µA)
- Ultra Low Current Sleep Mode
- Compatible with IrDA Detector Diodes

DESCRIPTION

The UCC5344 IrDA (Infrared Data Association) transceiver supports the analog section of the IrDA standard. The receiver is designed to amplify and condition the signals received by a PIN diode. Bandwidth limiting and ambient light rejection circuitry enhances signal integrity.

The UCC5344 works over a wide supply range of 3.0V to 5.5V and transmission rates from 9.6k to 4MBPS. The transmitter open drain FET is capable of sinking 300mA from 3.3V supplies and 500mA from 5V supplies. The UCC5344 is available in 16-pin DIL and SOIC packages or as tested good die.

BLOCK DIAGRAM



3/97

ABSOLUTE MAXIMUM RATINGS

AVDD, DVDD, CAT Voltage ..... –0.3V to +7V
SD/MODE, DET, TXX,
LED, DVDD, CAT ..... –0.3V to AVDD + 0.3V
I_{RXX}, I_{RXB} ..... –10mA to +10mA
I_{DET} 250mA
I_{LED} 1A
Storage Temperature ..... –65°C to +150°C
Junction Temperature ..... –55°C to +150°C
Lead Temperature (Soldering, 10sec.) ..... +300°C

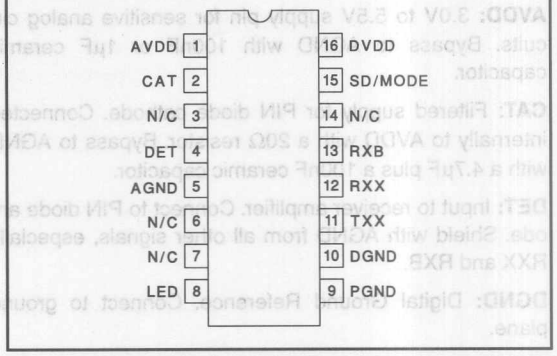
All voltages are with respect to AGND. DGND and PGND must be connected to AGND. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of the Databook for thermal limitations and considerations of packages.

RECOMMENDED OPERATING CONDITIONS

AVDD Voltage ..... 3.0V to 5.5V

CONNECTION DIAGRAM

DIL-16, SOIC-16 (Top View)
N Package, D Package



ELECTRICAL CHARACTERISTICS: Unless otherwise specified, T_A = 0°C to 70°C, AVDD = 3.0V to 5.5V, C_{AVDD} = 100nF, C_{DVDD} = 100nF, C_{CAT} = 4.7µF + 100nF, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current Section					
I_{AVDD}			0.9	1.5	mA
	SD/Mode = AVDD		0	1	µA
R_{DVDD}	AVDD to DVDD	1.5	2	2.5	kΩ
R_{CAT}	AVDD to CAT	15	20	25	kΩ
Receiver Section, 4 Mbps Mode (Programmed via SD/MODE)					
Input Referred Noise			10		pA/√Hz
Detection Threshold			100	400	nA
Signal to Noise	I_{DET} = 240nA, (I_{AMB} Diode ≤ 30µA)		11.8		A/A
Lower Band Limit	(Note 1)		100		kHz
Upper Band Limit	(Note 1)		8		MHz
Output Pulse Width	I_{DET} = 350nA$_{PK}$ to 100mApk and 0 to 200µADC, 125ns input pulse	110	125	140	ns
DVDD – RXX (V_{OH})	I_{RXX} = –100µA		220	330	mV
RXX (V_{OL})	I_{RXX} = 800µA		200	400	mV
Receiver Section, 115 kbps Mode (Programmed via SD/MODE)					
Input Referred Noise			10		pA/√Hz
Detection Threshold			100	200	nA
Signal to Noise	I_{DET} = 100nA (I_{AMB} Diode ≤ 30µA)		11.8		A/A
Lower Band Limit	(Note 1)		50		kHz
Upper Band Limit	(Note 1)		1		MHz
Output Pulse Width	I_{DET} = 100nA$_{PK}$ to 100mA$_{PK}$ and 0 to µADC, 1.6µs input pulse	1.4	1.6	1.8	µs
Transmitter Section					
I_{TXX}	TXX = 0 to AVDD	–10		10	µA
TXX (V_{IH})	AVDD = 3.3V		1.65	2.2	V
TXX (V_{IL})	AVDD = 3.3V	1.1	1.65		V
TXX (V_{IH})	AVDD = 5.0V		2.5	3.5	V
TXX (V_{IL})	AVDD = 5.0V	1.5	2.5		V
LED	TXX = AVDD = 4.5V, I_{LED} = 500mA		0.3	0.6	V
	TXX = AVDD = 3.0V, I_{LED} = 300mA		0.3	0.6	V
I_{LED}	TXX = 0, LED = AVDD = 5.5V			10	µA

Note 1: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

AGND: Ground reference for sensitive analog circuits. Connect to ground plane.

AVDD: 3.0V to 5.5V supply pin for sensitive analog circuits. Bypass to AGND with 100nF or 1µF ceramic capacitor.

CAT: Filtered supply for PIN diode cathode. Connected internally to AVDD with a 20Ω resistor. Bypass to AGND with a 4.7µF plus a 100nF ceramic capacitor.

DET: Input to receiver amplifier. Connect to PIN diode anode. Shield with AGND from all other signals, especially RXX and RXB.

DGND: Digital Ground Reference. Connect to ground plane.

DVDD: Supply pin for digital circuits. Internally connected to AVDD with a 2kΩ resistor. Bypass to DGND with a 100nF or 1µF ceramic capacitor.

LED: Open drain of transmit output transistor, connect to LED via current limiting resistor.

PGND: Source of the transmit output transistor. Connect to the ground plane.

RXX and RXB: Output and inverted output of the detect amplifier and buffer, connect to UART. Take care to have matched printed circuit board geometries with respect to DET for distance less than 3 centimeters of the DET.

SD/MODE: Shut down and mode select pin. A logic high on SD/MODE puts the chip into sleep mode. A 100ns pulse on SD/MODE will program the chip for FIR (0.576MBPS to 4MBPS) or SIR (9.6kBPS to 115.2kBPS) mode. TXX = 0 on the falling edge of SD/MODE programs SIR mode. TXX = 1 on the falling edge of SD/MODE programs FIR mode. The chip powers up and wakes up in SIR mode.

TXX: Input to the transmit buffer. Connect to UART.

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Consult Applications Handbook for available applications/design notes.

Datasheets in this section are organized in numeric order using the commercial part number.

Please note Hot Swap Power Managers were formerly known as "Electronic Circuit Breakers".

Hot Swap Power Managers

9

Packaging Note:

- *Values listed for recommended lead soldering time and temperature apply to ceramic thru-hole components only. Please consult the Packaging Section of this databook for recommendations on plastic SMD board attach processing.*

- *Unless otherwise noted, thermal resistance values listed on individual data sheets are for the device as it operates in a plastic thru-hole package. Results for other packaging options can be inferred by scaling the package rating values (thermal resistances) presented in the Packaging Section of this databook.*

Hot Swap Power Managers

Hot Swap Power Managers	UNITRODE PART NUMBER				
	UCC3912	UCC3913	UC3914+	UCC3915	UCC3916+
Voltage Range	3V to 8V	–10V to External Limitation	5V to 35V	7V to 15V	4V to 6V
Current Range	0A to 3A	Externally Limited	Externally Limited	0A to 3A	0A to 1.65A
Integrated Power FET	Y	N	N	Y	Y
R_{DSon}	150mΩ	N/A	N/A	150mΩ	220mΩ
Programmable Fault Threshold	Y	Y	Y	Y	N
Programmable Time Delay	Y	Y	Y	Y	Y
Latched Fault Mode	N	N	Y	N	N
Average Power Limiting	Y	Y	Y	Y	Y
Application/Design Note	DN-58, DN-68, U-151	DN-67			

Hot Swap Power Managers (cont'd)	UNITRODE PART NUMBER				
	UCC3917+	UCC3918+	UCC3919+	UCC3920+	UCC3921+
Voltage Range	7V to External Limitation	3V to 6V	3V to 8V	–3V to –15V	–10V to External Limitation
Current Range	Externally Limited	0A to 4A	Externally Limited	0A to 3A	Externally Limited
Integrated Power FET	N	Y	N	Y	N
R_{DSon}	N/A	75mΩ	N/A	100mΩ	N/A
Programmable Fault Threshold	Y	Y	Y	Y	Y
Programmable Time Delay	Y	Y	Y	Y	Y
Latched Fault Mode	Y	N	Y	N	Y
Average Power Limiting	Y	Y	Y	Y	Y

+ New Product


UNITRODE

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Programmable Hot Swap Power Manager

FEATURES

- Integrated 0.15 ohm Power MOSFET
- 3V to 8V Operation
- Digital Programmable Current Limit from 0 to 3A
- Electronic Circuit Breaker Function
- 1µA Icc when Disabled
- Programmable on Time
- Programmable Start Delay
- Fixed 3% Duty Cycle
- Uni-Directional Switch
- Thermal Shutdown
- Fault Output Indicator
- Maximum Output Current can be set to 1A above the Programmed Fault Level or to a full 4A
- Power SOIC, Low Thermal Resistance Packaging

DESCRIPTION

The UCC3912 Hot Swap Power Manager provides complete power management, hot swap capability, and circuit breaker functions. The only component required to operate the device, other than supply bypassing, is the fault timing capacitor, CT. All control and housekeeping functions are integrated, and externally programmable. These include the fault current level, maximum output sourcing current, maximum fault time,and start-up delay. In the event of a constant fault, the Internal fixed 3% duty cycle ratio limits average output power.

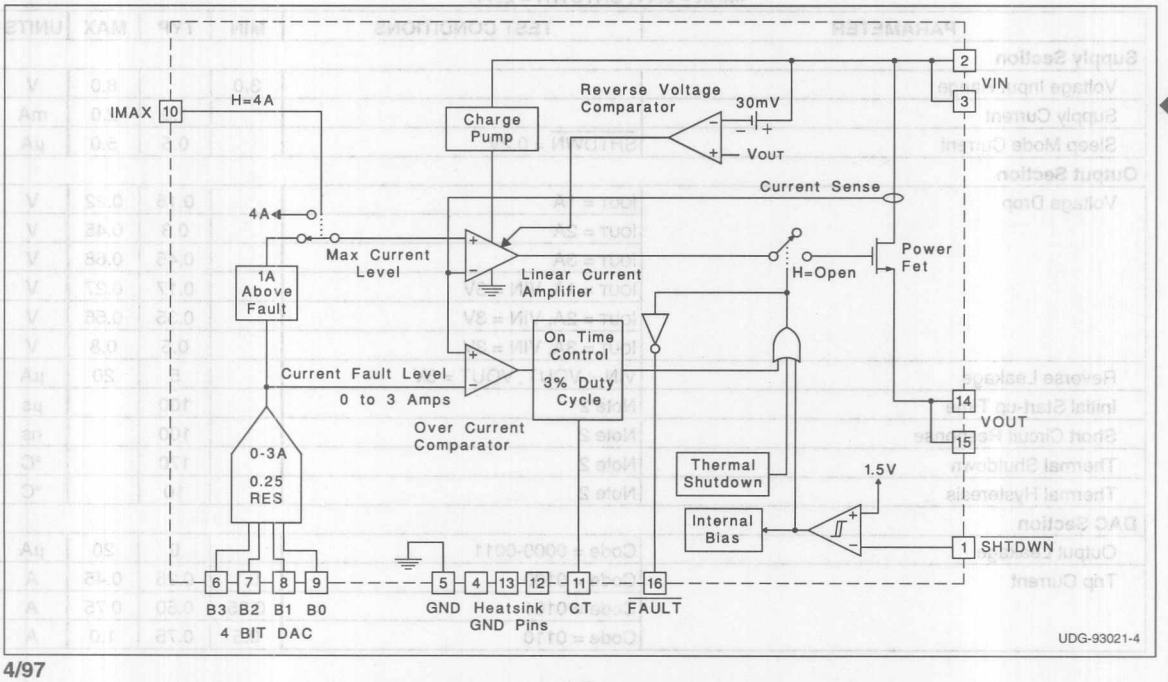
The internal 4 bit DAC allows programming of the fault level current from 0 to 3A with 0.25A resolution. The IMAX control pin sets the maximum sourcing current to 1A above the fault level when driven low, and to a full 4A when driven high for applications which require fast output capacitor charging.

When the output current is below the fault level, the output MOSFET is switched on with a nominal on resistance of 0.15 ohms. When the output current exceeds the fault level, but is less than the maximum sourcing level, the output remains switched on, but the fault timer starts charging CT. Once CT charges to a preset threshold, the switch is turned off, and remains off for 30 times the programmed fault time. When the output current reaches the maximum sourcing level, the MOSFET transitions from a switch to a constant current source.

The UCC3912 is designed for unidirectional current flow, emulating an ideal diode in series with the power switch. This feature is particularly attractive in

continued

BLOCK DIAGRAM



mon bus, such as with SCSI Termpwr.

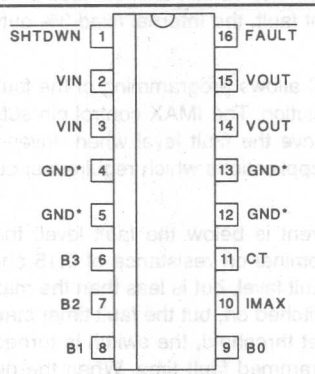
The UCC3912 can be put into sleep mode drawing only 1µA of supply current. The $\overline{\text{SHTDWN}}$ pin has a preset threshold hysteresis which allows the user the ability to set a time delay upon start-up to achieve sequencing of power. Other features include an open drain Fault output

$\overline{\text{FAULT}}$ Sink Current 50mA
$\overline{\text{FAULT}}$ Voltage ..... –0.3 to VIN
Output Current ..... Self Limiting
TTL Input Voltage ..... –0.3 to VIN
Storage Temperature ..... –65°C to +150°C
Junction Temperature ..... –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

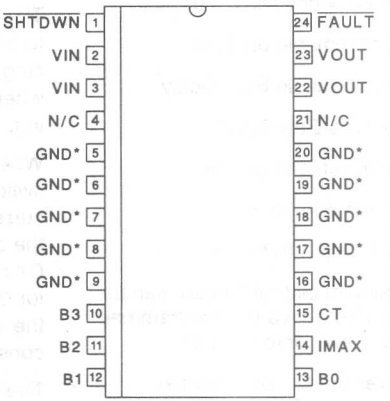
CONNECTION DIAGRAMS

DIL-16, SOIC-16 (Top View) N, DP Package



**Pin 5 serves as lowest impedance to the electrical ground; Pins 4, 12, and 13 serve as heat sink/ground. These pins should be connected to large etch areas to help dissipate heat.*
For N Package, pins 4, 12, and 13 are N/C.

TSSOP-24 (Top View) PWP Package



ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply for TJ = 0°C to 70°C, VIN = 5V, IMAX = 0.4V, $\overline{\text{SHTDWN}}$ = 2.4V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Section					
Voltage Input Range		3.0		8.0	V
Supply Current			1.0	2.0	mA
Sleep Mode Current	$\overline{\text{SHTDWN}}$ = 0.2V		0.5	5.0	µA
Output Section					
Voltage Drop	IOUT = 1A		0.15	0.22	V
	IOUT = 2A		0.3	0.45	V
	IOUT = 3A		0.45	0.68	V
	IOUT = 1A, VIN = 3V		0.17	0.27	V
	IOUT = 2A, VIN = 3V		0.35	0.56	V
	IOUT = 3A, VIN = 3V		0.5	0.8	V
Reverse Leakage	VIN < VOUT , VOUT = 5V		5	20	µA
Initial Start-up Time	Note 2		100		µs
Short Circuit Response	Note 2		100		ns
Thermal Shutdown	Note 2		170		°C
Thermal Hysteresis	Note 2		10		°C
DAC Section					
Output Leakage	Code = 0000-0011		0	20	µA
Trip Current	Code = 0100	0.1	0.25	0.45	A
	Code = 0101	0.25	0.50	0.75	A
	Code = 0110	0.5	0.75	1.0	A

ELECTRICAL CHARACTERISTICS (cont.)

Unless otherwise stated, these specifications apply for TJ = 0°C to 70°C, VIN = 5V, IMAX = 0.4V, $\overline{SHTDWN}$ = 2.4V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DAC Section (cont.)					
	Code = 0111	0.75	1.00	1.25	A
	Code = 1000	1.0	1.25	1.5	A
	Code = 1001	1.25	1.50	1.75	A
	Code = 1010	1.5	1.75	2.0	A
Trip Current	Code = 1011	1.7	2.00	2.3	A
	Code = 1100	1.9	2.25	2.58	A
	Code = 1101	2.1	2.50	2.9	A
	Code = 1110	2.3	2.75	3.2	A
	Code = 1111	2.5	3.0	3.5	A
Max Output Current	Code = 0000 to 0011			0.02	mA
Max Output Current Over Trip (Current Source Mode)	Code = 0100 to 1111, IMAX = 0V	0.5	1.0	1.8	A
Max Output Current (Current Source Mode)	Code = 0100 to 1111, IMAX = 2.4V	3.0	4.0	5.2	A
Timer Section					
CT Charge Current	VCT = 1.0V	–45.0	–36.0	–27.0	µA
CT Discharge Current	VCT = 1.0V	0.9	1.2	1.5	µA
Output Duty Cycle	VOUT = 0V	2.0	3.0	6.0	%
CT Fault Threshold		1.3	1.5	1.7	V
CT Reset Threshold		0.4	0.5	0.6	V
Shutdown Section					
Shutdown Threshold		1.1	1.5	1.9	V
Shutdown Hysteresis			100		mV
Input Current	$\overline{SHTDWN}$ = 1V		100	500	nA
Fault Output Section					
Output Leakage Current				500	nA
Low Level Output Voltage	IOUT = 10mA		0.4	0.8	V
TTL Input DC Characteristics Section					
TTL Input Voltage High	(can be connected to VIN)	2.0			V
TTL Input Voltage Low				0.8	V
TTL Input High Current	VIH = 2.4V		3	10	µA
TTL Input Low Current	VIL = 0.4V			1	µA

Note 1: All voltages are with respect to Ground. Current is positive into and negative out of the specified terminal.
Note 2: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

B0 - B3: These pins provide digital input to the DAC which sets the fault current threshold. They can be used to provide a digital soft-start, adaptive current limiting.

CT: A capacitor connected to ground sets the maximum fault time. The maximum fault time must be more than the time to charge the external capacitance in one cycle. The maximum fault time is defined as FAULT = 27.8 • 10^3 • CT. Once the fault time is reached the output will shut-down for a time given by: TSD = 833 • 10^3 • CT, this equates to a 3% duty cycle.

$\overline{FAULT}$: Open drain output which pulls low upon any condition which causes the output to open: Fault, Thermal Shutdown, or Shutdown.

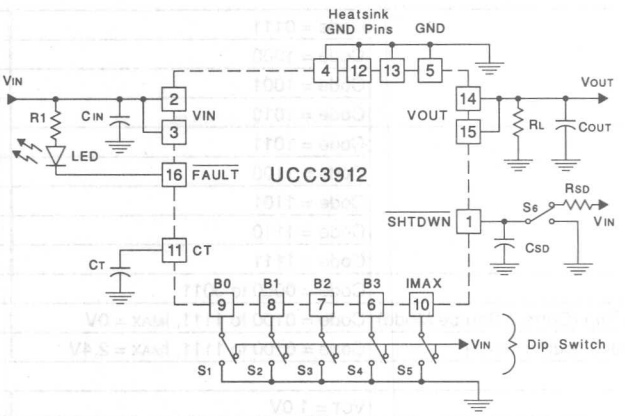
IMAX: When this pin is set to logic low the maximum sourcing current will always be 1A above the programmed fault level. When set to logic high, the maximum sourcing current will be a constant 4A for applications which require fast charging of load capacitance.

$\overline{SHTDWN}$: When this pin is brought to a logic low, the IC is put into a sleep mode drawing typically less than 1µA of ICC. The input threshold is hysteretic, allowing the user to program a start-up delay with an external RC circuit.

VIN: Input voltage to the UCC3912. The recommended voltage range is 3 to 8 volts. Both VIN pins should be connected together and to the power source.

VOUT: Output voltage from the UCC3912. When switched the output voltage will be approximately VIN - (0.15Ω • IOUT). Both VOUT pins should be connected together and to the load.

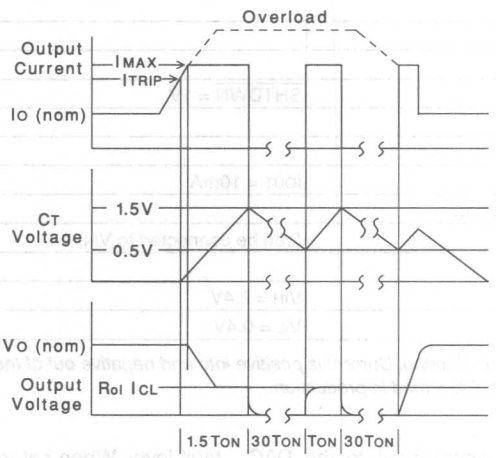
Evaluation Circuit



Note: For Demonstration Board Schematic see Design Note DN-58.

UDG-93020-3

Load Current, Timing Capacitor Voltage, and Output Voltage of the UCC3912 under Fault Conditions.



UDG-93019-4

Estimating Maximum Load Capacitance

For hot swap applications, the rate at which the total output capacitance can be charged depends on the maximum output current available and the nature of the load. For a constant-current current-limited controller, the output will come up if the load asks for less than the maximum available short-circuit current.

To guarantee recovery of a duty-cycle from a short-circuited load condition, there is a maximum total output capacitance which can be charged for a given unit ON time (Fault time). The design value of ON or Fault time can be adjusted by changing the timing capacitor C_T.

For worst-case constant-current load of value just less than the trip limit; $C_{OUT(max)}$ can be estimated from:

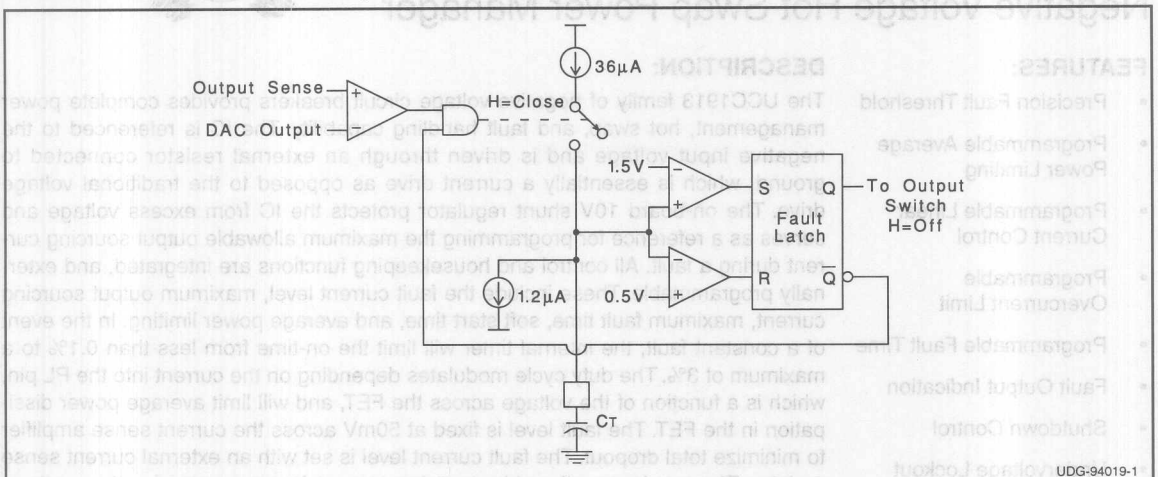
$$C_{OUT(max)} \approx (I_{MAX} - I_{LOAD}) \bullet \left(\frac{28 \bullet 10^3 \bullet C_T}{V_{OUT}} \right)$$

Where V_{OUT} is the output voltage.

For a resistive load of value RI, the value of $C_{OUT(max)}$ can be estimated from:

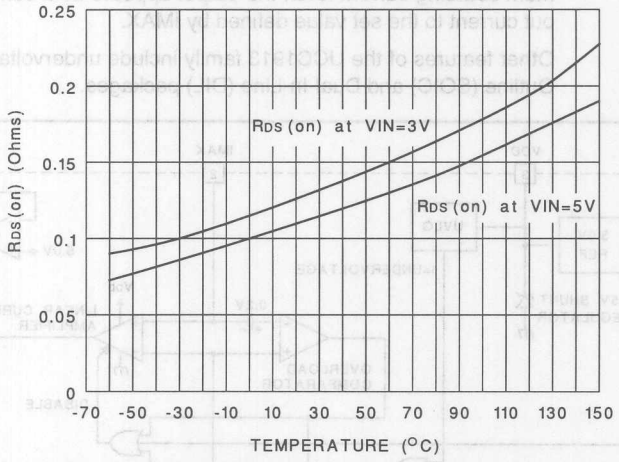
$$C_{OUT(max)} \approx \left(\frac{28 \bullet 10^3 \bullet C_T}{R_L \bullet \left[\frac{1}{1 - \frac{V_{OUT}}{I_{MAX} \bullet R_L}} \right]} \right) \bullet \ln$$

UCC3912 On Time Control Circuitry



The overcurrent comparator senses both the DAC output and a representation of the output current. When the output current exceeds the programmed level the timing capacitor CT charges with 36µA of current. If the fault occurs for the time it takes for CT to charge up to 1.5V, the fault latch is set and the output switch is opened. The output remains opened until CT discharges to 0.5V with a 1.2µA current source. Once the 0.5V is reached the output is enabled and will either appear as a switch, if the fault is removed, or a current source if the fault remains. If the over current condition is still present then CT will begin charging, starting the cycle over, resulting in approximately a 3% on time.

RDS(on) vs Temperature at 2A Load Current



SAFETY RECOMMENDATIONS

Although the UCC3912 is designed to provide system protection for all fault conditions, all integrated circuits can ultimately fail short. For this reason, if the UCC3912 is intended for use in safety critical applications where UL or some other safety rating is required, a redundant safety device such as a fuse should be placed in series with the device. The UCC3912 will prevent the fuse from blowing virtually all fault conditions, increasing system reliability and reducing maintainence cost, in addition to providing the hot swap benefits of the device.

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Negative Voltage Hot Swap Power Manager

FEATURES:

- Precision Fault Threshold
- Programmable Average Power Limiting
- Programmable Linear Current Control
- Programmable Overcurrent Limit
- Programmable Fault Time
- Fault Output Indication
- Shutdown Control
- Undervoltage Lockout
- 8-Pin SOIC

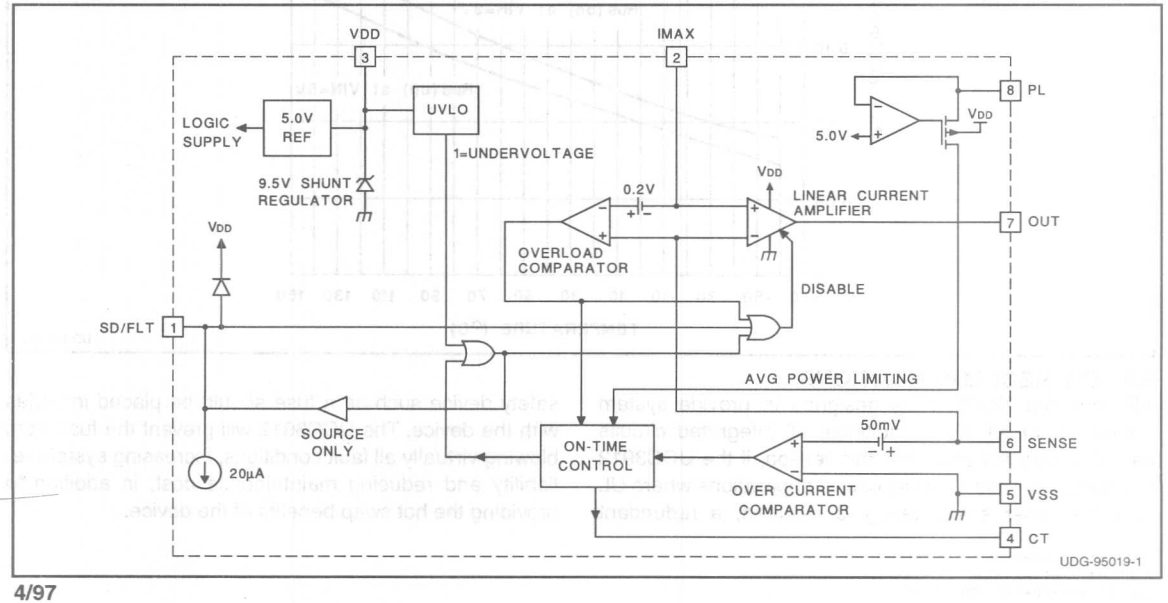
DESCRIPTION:

The UCC1913 family of negative voltage circuit breakers provides complete power management, hot swap, and fault handling capability. The IC is referenced to the negative input voltage and is driven through an external resistor connected to ground, which is essentially a current drive as opposed to the traditional voltage drive. The on-board 10V shunt regulator protects the IC from excess voltage and serves as a reference for programming the maximum allowable output sourcing current during a fault. All control and housekeeping functions are integrated, and externally programmable. These include the fault current level, maximum output sourcing current, maximum fault time, soft start time, and average power limiting. In the event of a constant fault, the internal timer will limit the on-time from less than 0.1% to a maximum of 3%. The duty cycle modulates depending on the current into the PL pin, which is a function of the voltage across the FET, and will limit average power dissipation in the FET. The fault level is fixed at 50mV across the current sense amplifier to minimize total dropout. The fault current level is set with an external current sense resistor. The maximum allowable sourcing current is programmed with a voltage divider from VDD to generate a fixed voltage on the IMAX pin. The current level, when the output appears as a current source, is equal to VIMAX/RSENSE. If desired, a controlled current startup can be programmed with a capacitor on the IMAX pin.

When the output current is below the fault level, the output device is switched on. When the output current exceeds the fault level, but is less than the maximum sourcing level programmed by the IMAX pin, the output remains switched on, and the fault timer starts charging CT. Once CT charges to 2.5V, the output device is turned off and performs a retry some time later. When the output current reaches the maximum sourcing current level, the output appears as a current source, limiting the output current to the set value defined by IMAX.

Other features of the UCC1913 family include undervoltage lockout, and 8-pin Small Outline (SOIC) and Dual-In-Line (DIL) packages.

BLOCK DIAGRAM



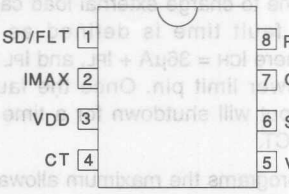
ABSOLUTE MAXIMUM RATINGS

IVCC 50mA
SHUTDOWN Current 10mA
PL Current 10mA
IMAX Input Voltage VCC
Storage Temperature .....–65°C to +150°C
Junction Temperature .....–55°C to +150°C
Lead Temperature (Soldering, 10 sec.) .....+300°C

All voltages are with respect to VSS (The most Negative voltage). All currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

DIL-8, SOIC-8 (Top View)
N or J, D Package



ELECTRICAL CHARACTERISTICS

Unless otherwise stated these specifications apply for TA = –55°C to +125°C for UCC1913; –40°C to +85°C for UCC2913; 0°C to +70°C for UCC3913; IVDD = 2mA, CT = 4.7pF, TA = TJ.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VDD Section					
IDD			1.0	2.0	mA
Regulator Voltage	ISOURCE = 2mA to 10mA	8.5	9.5	10.5	V
UVLO Off Voltage		6	7	8	V
Fault Timing Section					
Overcurrent Threshold	TJ = 25°C	47.5	50	53	mV
Overcurrent Threshold	Over Operating Temperature	46	50	53.5	mV
Overcurrent Input Bias			50	500	nA
CT Charge Current	VCT = 1.0V, IPL = 0	–50	–36	–22	µA
	Overload Condition, VSENSE – VIMAX = 300mV	–1.7	–1.2	–0.7	mA
CT Discharge Current	VCT = 1.0V, IPL = 0	0.6	1	1.5	µA
CT Fault Threshold		2.2	2.4	2.6	V
CT Reset Threshold		0.32	0.5	0.62	V
Output Duty Cycle	Fault Condition, IPL = 0	1.7	2.7	3.7	%
Output Section					
Output High Voltage	IOUT = 0A	8.5	10		V
	IOUT = –1mA	6	8		V
Output Low Voltage	IOUT = 0A; VSENSE – VIMAX = 100MV		0	0.01	V
	IOUT = 2mA; VSENSE – VIMAX = 100MV		0.2	0.6	V
Linear Amplifier Section					
Sense Control Voltage	IMAX = 100mV	85	100	115	mV
	IMAX = 400mV	370	400	430	mV
Input Bias			50	500	nA
Shutdown/Fault Section					
Shutdown Threshold		1.4	1.7	2.0	V
Input Current	Shutdown = 5V	15	25	45	µA
Fault Output High		6	7.5	9	V
Fault Output Low			0	0.01	V
Delay to Output	Note 1		150	300	ns
Power Limiting Section					
VSENSE Reg. Voltage	IPL = 64µA	4.35	4.85	5.35	V
Duty Cycle Control	IPL = 64µA	0.6	1.2	1.7	%
	IPL = 1mA	0.045	0.1	0.17	%
Overload Section					
Delay to Output	Note 1		300	500	ns
Output Sink Current	VSENSE – VIMAX = 300mV	40	100		mA
Threshold	Relative to IMAX	140	200	260	mV

Note 1 : Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

CT: A capacitor is connected to this pin in order to set the maximum fault time. The maximum fault time must be more than the time to charge external load capacitance. The maximum fault time is defined as $T_{FAULT} = (2 \cdot CT)/ I_{CH}$, where $I_{CH} = 36\mu A + I_{PL}$, and I_{PL} is the current into the power limit pin. Once the fault time is reached the output will shutdown for a time given by: $T_{SD} = 2 \cdot 10^6 \cdot CT$.

IMAX: This pin programs the maximum allowable sourcing current. Since VDD is a regulated voltage, a voltage divider can be derived from VDD to generate the program level for the IMAX pin. The current level at which the output appears as a current source is equal to the voltage on the IMAX pin over the current sense resistor. If desired, a controlled current startup can be programmed with a capacitor on the IMAX pin, and a programmed start delay can be achieved by driving the shutdown with an open collector/drain device into an RC network.

OUT: Output drive to the MOSFET pass element.

PL: This feature ensures that the average MOSFET power dissipation is controlled. A resistor is connected from this pin to the drain of the NMOS pass element. When the voltage across the NMOS exceeds 5V, current will flow into the PL pin which adds to the fault timer charge current, reducing the duty cycle from the 3% level. When I_{PL}>>36µA then the average MOSFET power dissipation is given by:

$$P_{FET\ AVG} = IMAX \cdot 1 \cdot 10^{-6} \cdot R_{PL}.$$

SENSE: Input voltage from the current sense resistor. When there is greater than 50mV across this pin with respect to VSS, then a fault is sensed, and CT starts to charge.

SD/FLT: This pin provides fault output indication and shutdown control. Interphase into and out of this pin is usually performed through level shift transistors. When 20µA is sourced into this pin, shutdown drives high causing the output to disable the NMOS pass device. When opened, and under a non-fault condition, the SD/FLT pin will pull to a low state. When a fault is detected by the fault timer, or undervoltage lockout, this pin will drive to a high state, indicating the output FET is OFF.

VDD: Current driven with a resistor to a voltage at least 10V more positive than VSS. Typically a resistor is connected to ground. The 10V shunt regulator clamps VDD at 10V above the VSS pin, and is also used as an output reference to program the maximum allowable sourcing current.

VSS: Ground reference for the IC and the most negative voltage available.

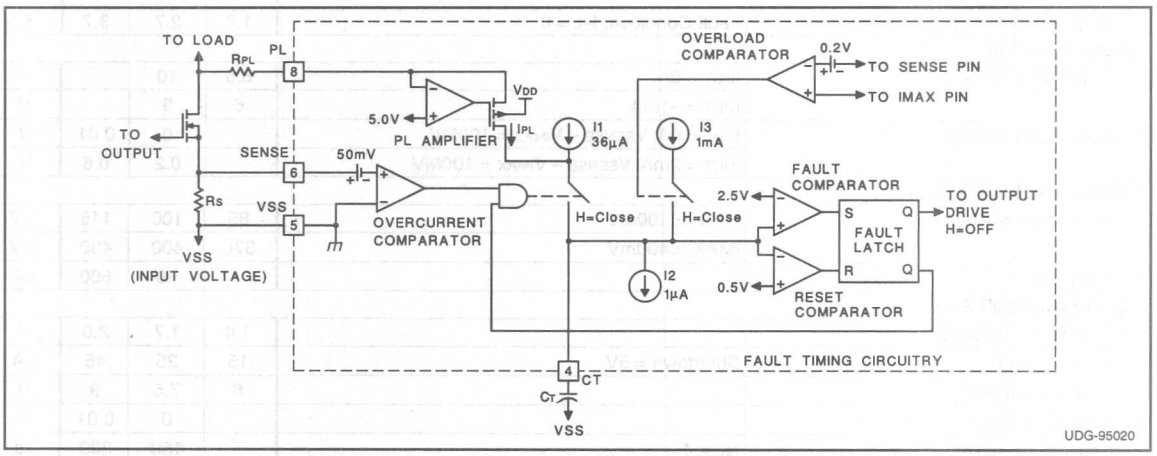
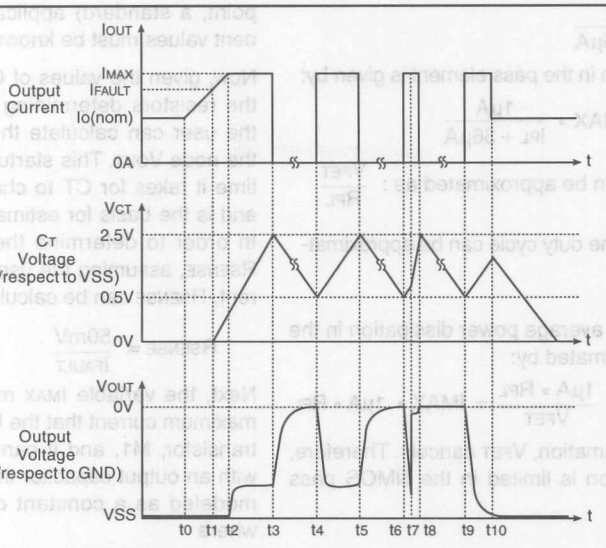


Figure 1. Fault timing circuitry for the UCC1913, including power limit overload.

Figure 1 shows the detailed circuitry for the fault timing function of the UCC1913. For the time being, we will discuss a typical fault mode, therefore, the overload comparator, and current source I3 does not work into the operation. Once the voltage across the current sense resistor, Rs, exceeds 50mV, a fault has occurred. This causes the timing capacitor to charge with a combination of 36µA plus the current from the power limiting amplifier. The PL amplifier is designed to only source current into the CT pin and to begin sourcing current once the voltage across the output FET exceeds 5V. The current I_{PL} is related to the voltage across the FET with the following expression:



t_0: safe condition – output current is nominal, output voltage is at the negative rail, VSS.

t_1: fault control reached – output current rises above the programmed fault value, CT begins to charge at ≅36µA.

t_2: max current reached – output current reaches the programmed maximum level and becomes a constant current with value I_{MAX}.

t_3: fault occurs – CT has charged to 2.5V, fault output goes high, the FET turns off allowing no output current to flow, V_{OUT} floats up to ground.

t_4: retry – CT has discharged to 0.5V, but fault current is still exceeded, CT begins charging again, FET is on, V_{OUT} pulled down to VSS.

$t_5 = t_3$: illustrates 3%duty cycle.

$t_6 = t_4$

t_7: output short circuit - if V_{OUT} is short circuited to ground, CT charges at a higher rate depending upon the values for VSS and R_{PL}.

t_8: fault occurs – output is still short circuited, but the occurrence of a fault turns the FET off so no current is conducted.

$t_9 = t_4$: output short circuit released, still in fault mode.

$t_{10} = t_0$: fault released, safe condition – return to normal operaton of the circuit breaker.

Figure 2. Typical Timing Diagram

$$I_{PL} = \frac{V_{FET} - 5V}{R_{PL}}$$

Where V_{FET} is the voltage across the NMOS pass device.

Later it will be shown how this feature will limit average power dissipation in the pass device. Note that under a condition where the output current is more than the fault level, but less than the max level, V_{OUT} ~ VSS (input voltage), I_{PL} = 0, the CT charging current is 36µA.

During a fault, CT will charge at a rate determined by the internal charging current and the external timing capacitor. Once CT charges to 2.5V, the fault comparator switches and sets the fault latch. Setting of the fault latch causes both the output to switch off and the charging switch to open. CT must now discharge with the 1µA current source, I2, until 0.5V is reached. Once the voltage at CT reaches 0.5V, the fault latch resets, which re-enables the output and allows the fault circuitry to regain control of the charging switch. If a fault is still present, the fault comparator will close the charging switch causing the cycle to begin. Under a constant fault, the duty cycle is given by:

$$\text{Duty cycle} = \frac{1\mu A}{I_{PL} + 36\mu A}$$

Average power dissipation in the pass element is given by:

$$P_{FET\ AVG} = V_{FET} \bullet IMAX \bullet \frac{1\mu A}{I_{PL} + 36\mu A}$$

Where V_{FET} >> 5V I_{PL} can be approximated as : $\frac{V_{FET}}{R_{PL}}$

and where I_{PL} >> 36µA, the duty cycle can be approximated as : $\frac{1\mu A \bullet R_{PL}}{V_{FET}}$

Therefore, the maximum average power dissipation in the MOSFET can be approximated by:

$$P_{FET\ AVG} = V_{FET} \bullet IMAX \bullet \frac{1\mu A \bullet R_{PL}}{V_{FET}} = IMAX \bullet 1\mu A \bullet R_{PL}$$

Notice that in the approximation, V_{FET} cancels. Therefore, average power dissipation is limited in the NMOS pass element.

Overload Comparator

The linear amplifier in the UCC1913 ensures that the output NMOS does not pass more than IMAX (which is V_{IMAX}/Rs). In the event the output current exceeds the programmed IMAX by 0.2V/Rs, which can only occur if the output FET is not responding to a command from the IC, the CT pin will begin charging with I3, 1mA, and continue to charge to approximately 8V. This allows a constant fault to show up on the SD/FLT pin,and also since the voltage on CT will only charge past 2.5V in an overload fault mode, it can be used for detection of output FET failure or to build in redundancy in the system.

Determining External Component Values

Referring now to Figure 3. To set Rvdd the following must be achieved

$$\frac{V_{INmin}}{R_{VDD}} > \frac{10V}{R1 + R2} + 2mA$$

In order to estimate the minimum timing capacitor, C_T, several things must be taken into account. For example, given the schematic below as a possible (and at this point, a standard) application, certain external component values must be known in order to estimate C_{Tmin}.

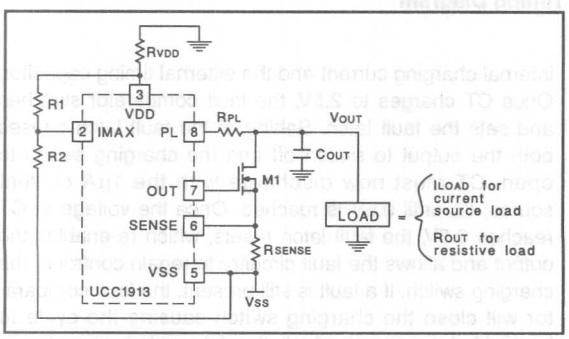


Figure 3.

Now, given the values of C_{OUT}, Load, R_{SENSE}, VSS, and the resistors determining the voltage on the IMAX pin, the user can calculate the approximate startup time of the node V_{OUT}. This startup time must be faster than the time it takes for CT to charge to 2.5V (relative to VSS), and is the basis for estimating the minimum value of CT. In order to determine the value of the sense resistor, R_{SENSE}, assuming the user has determined the fault current, R_{SENSE} can be calculated by:

$$R_{SENSE} = \frac{50mV}{I_{FAULT}}$$

Next, the variable I_{MAX} must be calculated. I_{MAX} is the maximum current that the UCC1913 will allow through the transistor, M1, and it can be shown that during startup with an output capacitor the power MOSFET, M1, can be modeled as a constant current source of value IMAX where

$$I_{MAX} = \frac{V_{IMAX}}{R_{SENSE}} \text{ where } V_{IMAX} = \text{voltage on pin IMAX.}$$

Given this information, calculation of the startup time is now possible via the following:

Current Source Load:

$$T_{START} = \frac{C_{OUT} \bullet |VSS|}{I_{MAX} - I_{LOAD}}$$

Resistive Load:

$$T_{START} = C_{OUT} \bullet R_{OUT} \bullet Ln\left(\frac{I_{MAX} \bullet R_{OUT}}{I_{MAX} \bullet R_{OUT} - |VSS|} \right)$$

Once T_{START} is calculated, the power limit feature of the UCC1913 must be addressed and component values derived. Assuming the user chooses to limit the maximum allowable average power that will be associated with the circuit breaker, the power limiting resistor, R_{PL}, can be easily determined by the following:

$$R_{PL} = \frac{P_{FET\ AVG}}{1\mu A \bullet I_{MAX}} \text{ where a minimum } R_{PL} \text{ exists}$$

defined by $R_{PLmin} = \frac{|VSS|}{5mA}$

Finally, after computing the aforementioned variables, the minimum timing capacitor can be derived as such:

Current Source Load:

$$C_{Tmin} = \frac{3 \bullet T_{START} \bullet (62\mu A \bullet R_{PL} + |VSS| - 10V)}{10 \bullet R_{PL}}$$

Resistive Load:

$$C_{Tmin} = \frac{3 \bullet T_{START} \bullet (31\mu A \bullet R_{PL} + |VSS| - 5V - I_{MAX} \bullet R_{OUT})}{5 \bullet R_{PL}} + \frac{3 \bullet R_{OUT} \bullet |VSS| \bullet C_{OUT}}{5 \bullet R_{PL}}$$

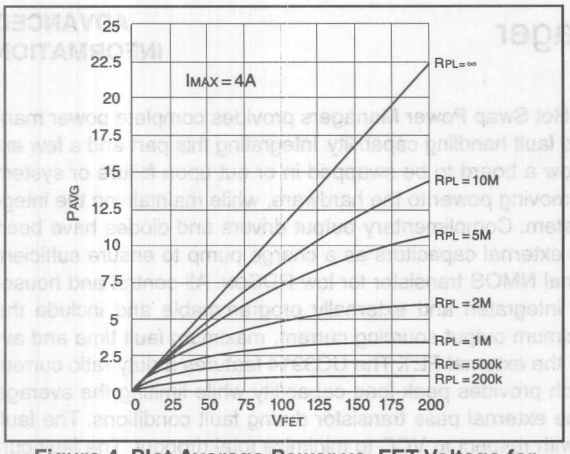


Figure 4. Plot Average Power vs. FET Voltage for Increasing Values of R_{PL}.

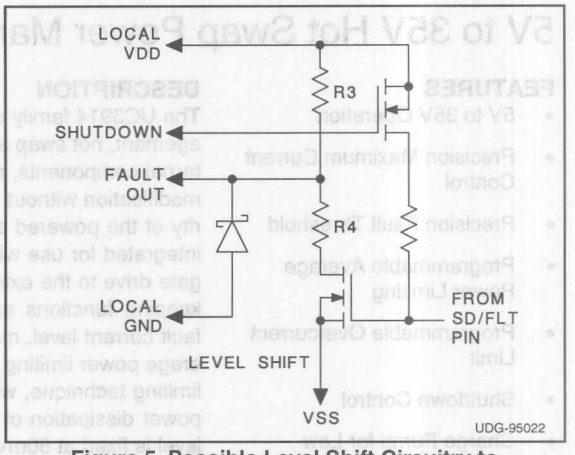
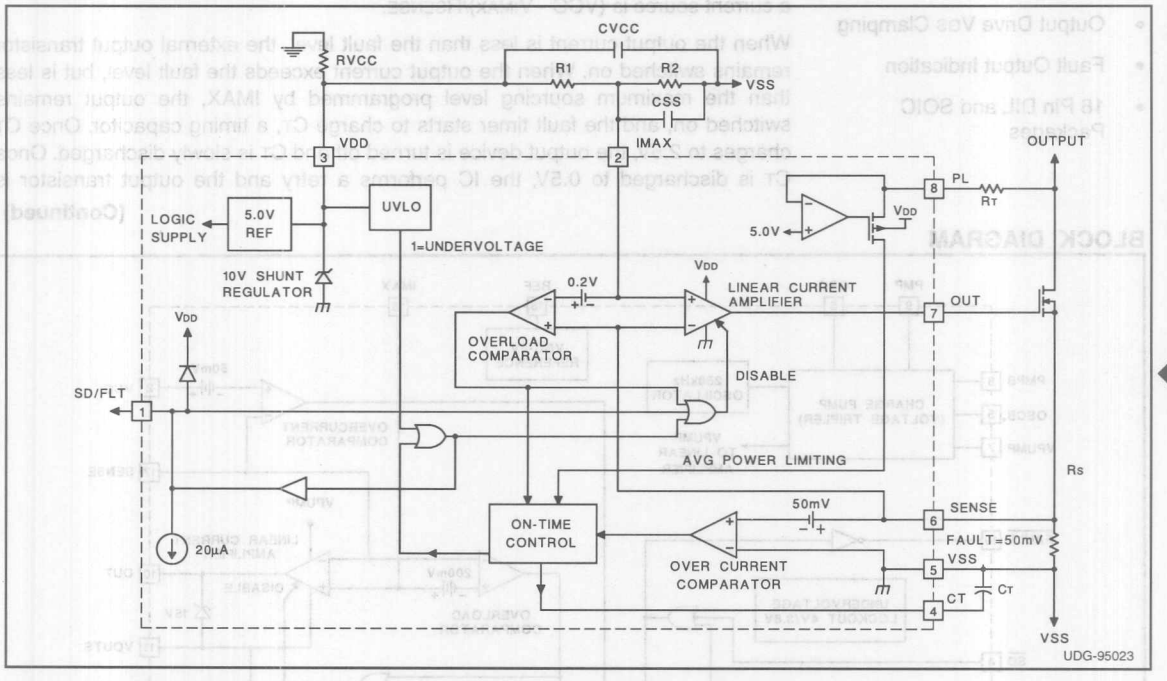


Figure 5. Possible Level Shift Circuitry to Interface to the UCC1913.

APPLICATION DIAGRAM



SAFETY RECOMMENDATIONS

Although the UCC3913 is designed to provide system protection for all fault conditions, all integrated circuits can ultimately fail short. For this reason, if the UCC3913 is intended for use in safety critical applications where UL or some other safety rating is required, a redundant safety device such as a fuse should be placed in series with the device. The UCC3913 will prevent the fuse from blowing for virtually all fault conditions, increasing system reliability and reducing maintenance cost, in addition to providing the hot swap benefits of the device.

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UNITRODE

UC1914
UC2914
UC3914

5V to 35V Hot Swap Power Manager

ADVANCED INFORMATION

FEATURES

- 5V to 35V Operation
- Precision Maximum Current Control
- Precision Fault Threshold
- Programmable Average Power Limiting
- Programmable Overcurrent Limit
- Shutdown Control
- Charge Pump for Low RDSON High-Side Drive
- Latch Reset Function Available
- Output Drive VGS Clamping
- Fault Output Indication
- 18 Pin DIL and SOIC Packages

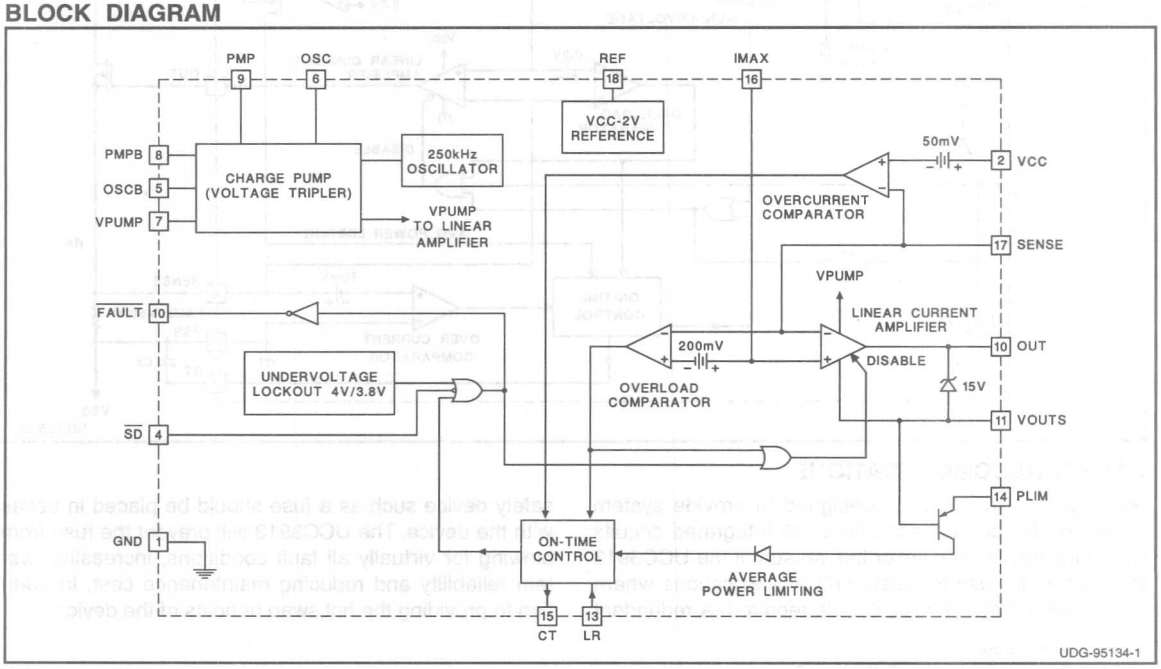
DESCRIPTION

The UC3914 family of Hot Swap Power Managers provides complete power management, hot swap and fault handling capability. Integrating this part and a few external components, allow a board to be swapped in or out upon failure or system modification without removing power to the hardware, while maintaining the integrity of the powered system. Complimentary output drivers and diodes have been integrated for use with external capacitors as a charge pump to ensure sufficient gate drive to the external NMOS transistor for low RDSON. All control and housekeeping functions are integrated and externally programmable and include the fault current level, maximum output sourcing current, maximum fault time and average power limiting of the external FET. The UC3914 features a duty ratio current limiting technique, which provides peak load capability while limiting the average power dissipation of the external pass transistor during fault conditions. The fault level is fixed at 50mV with respect to VCC to minimize total dropout. The fault current level is set with an external current sense resistor. The maximum allowable sourcing current is programmed by using a resistor divider from VCC to REF to set the voltage on IMAX. The maximum current level when the output appears as a current source is (VCC - VIMAX)/RSENSE.

When the output current is less than the fault level, the external output transistor remains switched on. When the output current exceeds the fault level, but is less than the maximum sourcing level programmed by IMAX, the output remains switched on, and the fault timer starts to charge CT, a timing capacitor. Once CT charges to 2.5V, the output device is turned off and CT is slowly discharged. Once CT is discharged to 0.5V, the IC performs a retry and the output transistor is

(Continued)

BLOCK DIAGRAM



5/97

DESCRIPTION (cont.)

switched on again. The UC3914 offers two distinct reset modes. In one mode with LR left floating or held low, the IC will repeatedly try to reset itself if a fault occurs as described above. In the second mode with LR held high, once a fault occurs, the output is latched off until either LR is toggled low, the part is shutdown then re-enabled using $\overline{SD}$, or the power to the part is turned off and then on again.

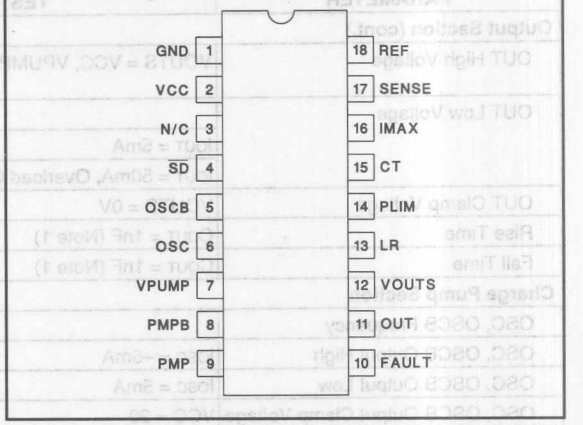
This part is offered in both 18 pin DW (SOIC) and Dual-In-Line (DIL) packages.

ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage, VCC. 40V
Maximum Forced Voltage
$\overline{SD}$ 12V
IMAX VCC
LR 12V
Maximum Current
$\overline{FAULT}$ 20mA
PLIM 10mA
Maximum Voltage, $\overline{FAULT}$ 40V
Reference Output Current . . . . . Internally Limited
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C
Unless otherwise indicated, voltage are reference to ground.
Currents are positive into, negative out of specified terminal.
Consult Packaging Section of Databook for thermal limitations and considerations of package.

CONNECTION DIAGRAM

DIL-18, SOIC-18 (Top View)
N or J Package, DW Package



ELECTRICAL CHARACTERISTICS:

Unless otherwise specified, T_A = 0°C to 70°C for the UC3914, –40°C to 85°C for the UC2914, and –55°C to 125°C for the UC1914. VCC = 12V, VPUMP = VPUMP max, CP1 = CP2 = C_{PUMP} = 0.01µF. T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VCC Section					
Icc			8		mA
	VCC = 35V		12		mA
Shutdown Icc	$\overline{SD}$ = 0V		500		µA
UVLO	Turn on threshold		4		V
UVLO Off Voltage			3.8		V
Fault Timing Section					
Overcurrent Threshold	T_J = 25°C, Respect to VCC	–45	–50	–55	mV
	Over Operating Temperature, Respect to VCC		-50		mV
IMAX Input Bias			–1		µA
CT Charge Current	CT = 1V		–100		µA
CT Discharge Current	CT = 1V		3		µA
CT Charge Current	CT = 1V, Overload Condition		–3		mA
CT Fault Threshold			2.5		V
CT Reset Threshold			0.5		V
Output Duty Cycle	Fault Condition, I_{PL} = 0		3		%
Output Section					
OUT High Voltage	VOUTS = VCC, VPUMP = VPUMP max		VPUMP - 1		V

ELECTRICAL CHARACTERISTICS (cont.): Unless otherwise specified, T_A = 0°C to 70°C for the UC3914, –40°C to 85°C for the UC2914, and –55°C to 125°C for the UC1914. VCC = 12V, VPUMP = VPUMP max, CP1 = CP2 = C_{PUMP} = 0.01µF. T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Section (cont.)					
OUT High Voltage	VOUTS = VCC, VPUMP = VPUMP max, I_{OUT} = –2mA		VPUMP – 1.5		V
OUT Low Voltage			0.8		V
	I_{OUT} = 5mA		1		V
	I_{OUT} = 50mA, Overload Condition, VOUTS = 0V		1.2		V
OUT Clamp Voltage	VOUTS = 0V		13		V
Rise Time	C_{OUT} = 1nF (Note 1)		750		ns
Fall Time	C_{OUT} = 1nF (Note 1)		250		ns
Charge Pump Section					
OSC, OSCB Frequency			125		kHz
OSC, OSCB Output High	I_{OSC} = –5mA		11		V
OSC, OSCB Output Low	I_{OSC} = 5mA		0.2		V
OSC, OSCB Output Clamp Voltage	VCC = 20		13		V
OSC, OSCB Output Current Limit	High Side Only		–10		mA
Pump Diode Voltage Drop	I_{DIODE} = 10mA, Measured from PMP to PMPB, PMPB to VPUMP		1.2		V
PMP Clamp Voltage	VCC = 20		13		V
VPUMP Maximium Voltage	VCC = 12, VOUTS = VCC, Voltage Where Charge Pump Disabled		22		V
	VCC = 35V, VOUTS = VCC, Voltage Where Charge Pump Disable		45		V
VPUMP Hysteresis	VCC = 12, VOUTS = VCC, Voltage Where Charge Pump Reenabled		1		V
	VCC = 35V, VOUTS = VCC, Charge Pump Reenabled		1		V
Linear Current Section					
Input Offset Voltage		–15	0	15	mV
Voltage Gain			80		dB
SENSE Control Voltage	IMAX = VCC		VCC		V
	IMAX = REF		REF		V
SENSE Input Bias			–1		µA
Reference Section					
REF Output Voltage	Respect to VCC		–2		V
REF Current Limit			20		mA
Load Regulation	I_{VREF} = 1mA to 10mA		25		mV
Line Regulation	VCC = 5V to 35V		25		mV
Shutdown Section					
Shutdown Threshold			1.5		V
Input Current	$\overline{SD}$ = 5V		150		µA
Delay to Output	(Note 1)		450		ns
Fault Section					
Fault Output Low	I_{FAULT} = 1mA		100		mV
Fault Output Leakage	V_{FAULT} = 35V		500		nA
Latch Section					
LR Threshold	High to Low	0.8	1.4	2	V
Input Current	LR = 5V		500		µA

ELECTRICAL CHARACTERISTICS (cont.): Unless otherwise specified, T_A = 0°C to 70°C for the UC3914, –40°C to 85°C for the UC2914, and –55°C to 125°C for the UC1914. VCC = 12V, VPUMP = VPUMP max, CP1 = CP2 = CPUMP = 0.01µF. $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Power Limiting Section					
Duty Cycle Control	In Fault, I_{PLIM} = 200µA		1		%
	In Fault, I_{PLIM} = 3mA		0.1		%
Overload Section					
Delay to Output	(Note 1)		250		ns
Threshold	Respect to IMAX		–200		mV

Note 1: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

CT: A capacitor is connected to this pin in order to set the maximum fault time. The maximum fault time must be more than the time to charge external load capacitance. The maximum fault time is defined as:

$$T_{FAULT} = \frac{2 \bullet C_T}{I_{CH}}$$

where I_{CH} = 100µA + I_{PL}, and I_{PL} is the current into the power limit pin. Once the fault time is reached the output will shutdown for a time given by:

$$T_{SD} = \frac{2 \bullet C_T}{I_{DIS}}$$

where Idis is nominally 3µA.

$\overline{\text{FAULT}}$: Open collector output which pulls low upon any of the following conditions: Timer fault, Shutdown, UVLO.

GND: Ground reference for the IC.

IMAX: This pin programs the maximum allowable sourcing current. Since VREF is a –2V reference (with respect to VCC), a voltage divider can be derived from VCC to REF in order to generate the program level for the IMAX pin. The current level at which the output appears as a current source is equal to the voltage on the IMAX pin, with respect to VCC, over the current sense resistor. If desired, a controlled current startup can be programmed with a capacitor on IMAX to VCC.

LR: If this pin is held high and a a fault occurs, the timer will be prevented from resetting the fault latch when CT is discharged below the reset comparator threshold. The part will not retry until this pin is brought to a logic low or a power-on-reset is caused. Pulling this pin low before the reset time is reached will not clear the fault until the reset time is reached. Floating or holding this pin low will result in the part repeatedly trying to reset itself if a fault occurs.

OUT: Output drive to the MOSFET pass element. Internal clamping ensures that the maximum V_{GS} drive is 15V.

OSC, OSCB: Complimentary output drivers for intermediate charge pump stages. A 0.01µF capacitor should be placed between OSC and PMP, and OSCB and PMPB.

PLIM: This feature ensures that the average MOSFET power dissipation is controlled. A resistor is connected from this pin to VCC. Current will flow into PLIM which adds to the fault timer charge current, reducing the duty cycle from the typical 3% level. When I_{PL} >> 100µA then the average MOSFET power dissipation is given by: P_{FET_AVG} = IMAX • 3 • 10^{-6} • R_{PL}.

PMP, PMPB: Complimentary pins which couple charge pump capacitors to internal diodes and are used to provide charge to the reservoir capacitor tied to VPUMP. Typical capacitor values used are 0.01µF.

REF: –2V reference with respect to VCC used to program the IMAX pin voltage. A 0.1µF ceramic or tantalum capacitor MUST be tied between this pin and VCC to ensure proper operation of the chip.

$\overline{\text{SD}}$: When this TTL compatible input is brought to a logic low, the output of the linear amplifier is driven low, $\overline{\text{FAULT}}$ is pulled low and the IC is put inot a low power mode.

SENSE: Input voltage from current sense resistor. When there is greater than 50mV across this pin with respect to VCC, a fault is sensed and C_T begins to charge.

VCC: Input voltage to the IC. Typical voltages are 4.5V to 35V. The minimum input voltage required for operation is 4.5V.

VOUTS: Source connection ot external N-channel MOSFET and sensed output voltage of load.

VPUMP: Charge pump output voltage. A capacitor should be tied between this pin and VOUTS with a typical value being 0.01µF.

APPLICATION INFORMATION

The UC3914 is to be used in conjunction with external passive components and an N-channel MOSFET (NMOS) to facilitate hot swap capability of application modules. A typical application set-up is given in Figure 7. The term hot swap refers to the system requirement that submodules be swapped in or out upon failure or system modification without removing power to the operating hardware. The integrity of the power bus must not be compromised due to the addition of an unpowered module. Significant power bus glitches can occur due to the substantial initial charging current of on-board module bypass capacitance and other load conditions (for more information on hot swapping and power management applications, see Application Note U-151). The UC3914 provides protection by monitoring and controlling the output current of an external NMOS to charge this capacitance and provide load current. The addition of the NMOS, a sense resistor, R_{SENSE}, and two other resistors, R1 and R2 set the programmed maximum current level the NMOS can source to charge the load in a controlled manner. The equation for this current, I_{MAX}, is:

$$I_{MAX} = \frac{VCC - V_{IMAX}}{R_{SENSE}}$$

where V_{IMAX} is the voltage generated at the IMAX pin. Analysis of the application circuit shows that V_{IMAX} can be defined as:

$$V_{IMAX} = \frac{(VCC - V_{REF}) \bullet R1}{R1 + R2} = \frac{2V \bullet R1}{R1 + R2}$$

where V_{REF} is the voltage is the voltage on the REF pin and whose internally generated potential is two volts below VCC. The UC3914 also has an internal overcurrent comparator which monitors the voltage between SENSE and VCC. If this voltage exceeds 50mV, the comparator determines that a fault has occurred, and a timing capacitor, C_T, will begin to charge. This can be rewritten as a current which causes a fault, I_{FAULT}:

$$I_{FAULT} = \frac{50mV}{R_{SENSE}}.$$

Fault Timing

Figure 1 shows the circuitry associated with the fault timing function of the UC3914. A typical fault mode, where the overload comparator and current source I3 do not factor into operation (switch S2 is open), will first be considered. Once the voltage across R_{SENSE} exceeds 50mV, a fault has occurred. This causes the timing capacitor, C_T, to charge with a combination of 100µA (I1) plus the current from the power limiting circuitry (I_{PL}).

Figure 2a shows typical fault timing waveforms for the external NMOS output current, the voltage on the CT pin, and the output load voltage, V_{OUT}, with LR left floating or grounded. The output voltage waveforms have assumed an RC characteristic load and time constants will vary depending upon the component values. Prior to time t_0, the load is fully charged to almost VCC and the NMOS is supplying the current, I_O, to the load. At t_0, the current begins to ramp up due to a change in the load conditions until, at t_1, the fault current level, I_{FAULT}, has been reached to cause switch S1 to close. This results in C_T being charged with the current sources I1 and I_{PL}. During this time, V_{OUT} is still almost equal to VCC except for small losses from voltage drops across the sense resistor and the NMOS. The output current reaches the programmed maximum level, I_{MAX}, at t_2. The C_T voltage continues to rise since I_{MAX} is still greater than I_{FAULT}. The load output voltage drops because the current load requirements have become greater than the controlled maximum sourcing current. The C_T voltage reaches the upper comparator threshold (Figure 1) of 2.5V at t_3, which promptly shuts off the gate drive to the NMOS (not shown but can be inferred from the fact that no output current is provided to the load), latches in the fault and opens switch S1 disconnecting the charging currents I1 and I_{PL} from C_T. Since no output current is supplied, the load voltage decays at a rate determined by the load characteristics and the capacitance. The 3µA current source, I2, discharges CT to the 0.5V reset comparator threshold. This time is significantly longer than the charging time and is the basis for the duty cycle current limiting technique. When the C_T voltage reaches 0.5V at t_4, the part performs a retry, allowing the NMOS to again source current to the load and cause V_{OUT} to rise. In this particular example, I_{MAX} is still sourced by the NMOS at each attempted retry and the fault timing sequence is repeated until time t_7 when the load requirements change to I_O. Since I_O is less than the fault current level at this time, switch S1 is opened, I2 discharges C_T and V_{OUT} rises to almost VCC.

Figure 2b shows fault timing waveforms similar to those depicted in Figure 2a except that the latch reset (LR) function is utilized. Operation is the same as described above until t_4 when the voltage on C_T reaches the reset threshold. Holding LR high prevents the latch from being reset, preventing the IC from performing a retry (sourcing current to the load). The UC3914 is latched off until either LR is pulled to a logic low, or the chip is forced into an under voltage lockout (UVLO) condition and back out of UVLO causing the latch to automatically perform a power on reset. Figure 2b illustrates LR being toggled low at t_5, causing the part to perform a retry. Time t_6 again illustrates what happens when a fault is detected. The LR pin is toggled low and back high at time t_7, prior to the volt-

APPLICATION INFORMATION (cont.)

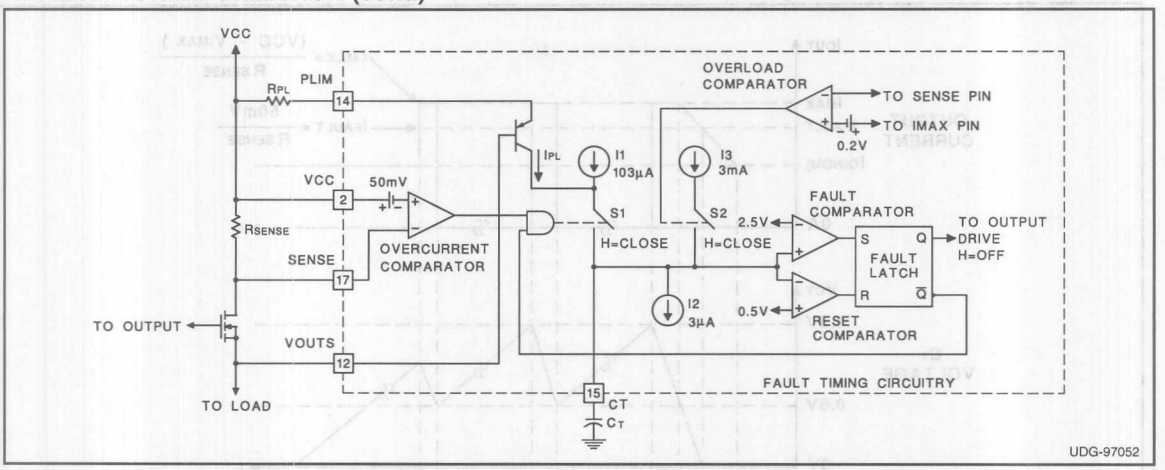


Figure 1. Fault Timing Circuitry for the UC3914, Including Power Limit and Overcurrent

age on the CT pin hitting the reset threshold. This information tells the UC3914 to allow the part to perform a retry when the lower reset threshold is reached, which occurs at t_8. Time t_9 corresponds to when load conditions change to where a fault is not present as described for Figure 2a.

Power Limiting

The power limiting circuitry is designed to only source current into the CT pin. To implement this feature, a resistor, R_{PL}, should be placed between VCC and PLIM. The current, I_{PL} (show in Figure 1) is given by the following expression:

$$I_{PL} = \frac{VCC - VOUTS}{R_{PL}}, \text{ for VOUTS } 1V + VCT$$

where VCT is the voltage on the CT pin. For VOUTS < 1V + VCT the common mode range of the power limiting circuitry causes I_{PL} = 0 leaving only the 100µA current source to charge C_T. VCC - VOUTS represents the voltage across the NMOS pass device.

Later it will be shown how this feature will limit average power dissipation in the pass device. Note that under a fault condition where the output current is just above the fault level, but less than the maximum level, VOUTS ~ VCC, I_{PL} = 0 and the C_T charging current is 100µA.

During a fault, the CT pin will charge at a rate determined by the internal charging current and the external timing capacitor, C_T. Once C_T charges to 2.5V, the fault comparator trips and sets the fault latch. When this occurs, OUT is pulled down to VOUTS, causing the external NMOS to shut off and the charging switch, S1, to open. C_T will be discharged with I2 until the C_T potential reaches 0.5V. Once this occurs, the fault latch will reset (unless LR is being held high, whereby a fault can only be cleared by pulling this pin low or going through a power-on-reset cycle), which re-enables the output of the linear amplifier and allows the fault circuitry to regain control of the charging switch. If a fault is still present, the overcurrent comparator will close the charging switch causing the cycle to repeat. Under a constant fault the duty cycle is given by:

$$\text{Duty Cycle} = \frac{3\mu A}{I_{PL} + 100\mu A}$$

Average power dissipation can be limited using the PLIM pin. Average power dissipation in the pass element is given by:

$$PFET_{AVG} = (VCC - VOUTS) \bullet IMAX \bullet \text{Duty Cycle}$$

$$= (VCC - VOUTS) \bullet IMAX \bullet \frac{3\mu A}{I_{PL} + 100\mu A}$$

VCC – VOUTS is the drain to source voltage across the FET. When IPL >> 100µA, the duty cycle equation given above can be rewritten as:

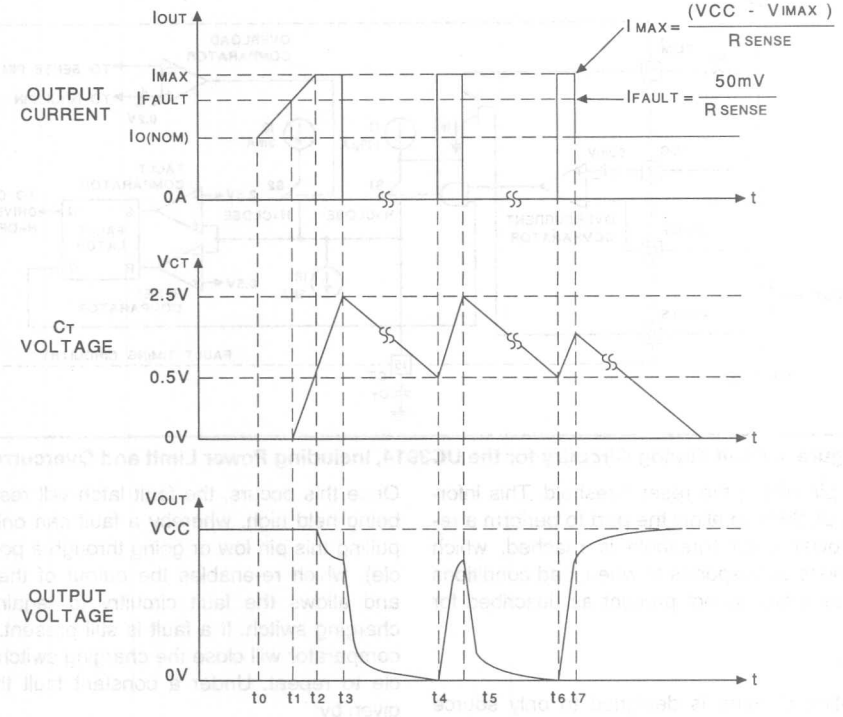
$$\text{Duty Cycle} = \frac{R_{PL} + 3\mu A}{VCC - VOUTS}$$

and the average power dissipation of the MOSFET is given by:

$$PFET_{AVG} = (VCC - VOUTS) \bullet IMAX \bullet \frac{R_{PL} + 3\mu A}{VCC - VOUTS}$$

$$= IMAX \bullet R_{PL} \bullet 3\mu A$$

The average power is limited by the programmed IMAX current and the appropriate value for R_{PL}.



t0: Normal conditions - output current is nominal, output voltage is at positive rail, VCC

t1: Fault control reached - output current rises above the programmed fault value, CT begins to charge with ≅ 100µA + IPL.

t2: Maximum current reached - output current reaches the programmed maximum level and becomes a constant current with value IMAX.

t3: Fault occurs - CT has charged to 2.5V, fault output goes low, the FET turns off allowing no output current to flow, VOUT discharge to GND.

t4: Retry - CT has discharged to 0.5V, but fault current is still exceeded, CT begins charging again, FET is on, VOUT increases.

t5 = t3: Illustrates <3% duty cycle depending upon RPL selected.

t6 = t4

t7 = t0: Fault released, normal condition - return to normal operation of the hot swap power manager.

Figure 2a: Typical Timing Diagram

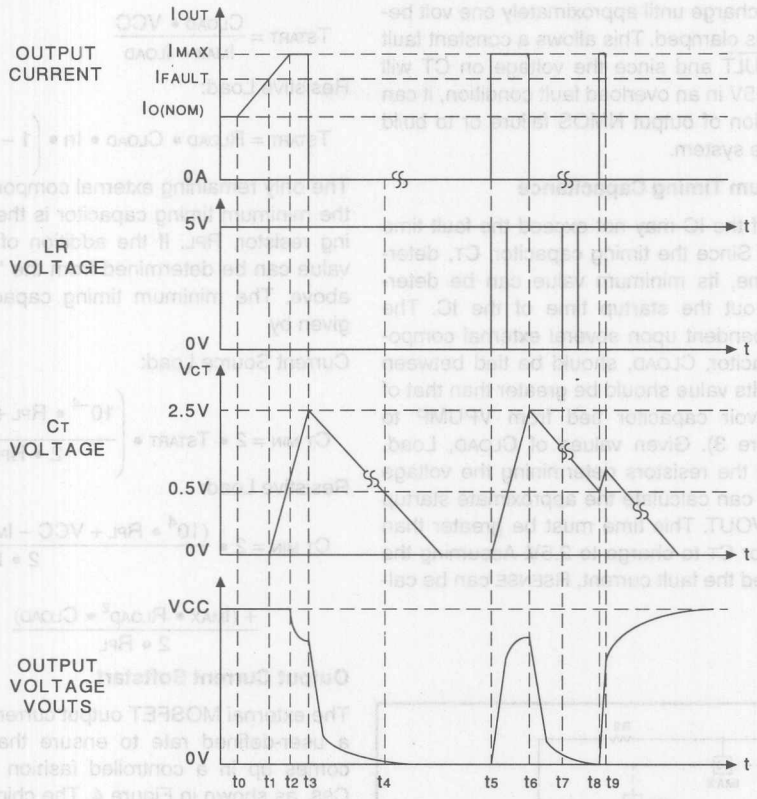
Overload Comparator

The linear amplifier in the UC3914 ensures that the external NMOS does not source more than the current IMAX, defined above as:

$$I_{MAX} = \frac{VCC - V_{IMAX}}{R_{SENSE}}.$$

In the event that output current exceeds the programmed IMAX by more than 200mV/RSENSE, the output of the linear amplifier will immediately be pulled low (with respect to VOUTS) providing no gate drive to the NMOS, and preventing current from being delivered to the load. This situation could occur if the external NMOS is not responding to a command from the IC or output load conditions change quickly to cause an overload condition before the linear amplifier can respond. For example, if the NMOS is sourcing current into a load and the load suddenly becomes short circuited, an overload condition may occur. The short circuit will cause the VGS of the NMOS to immediately increase, resulting in increased load current and voltage drop across RSENSE. If this drop exceeds the overload comparator threshold, the amplifier output will be quickly pulled low. It will also cause the CT pin to be-

APPLICATION INFORMATION (cont.)



t0: Normal conditions - output current is nominal, output voltage is at positive rail, VCC

t1: Fault control reached - output current rises above the programmed fault value, CT begins to charge with ≅ 100µA + IPL.

t2: Maximum current reached - output current reaches the programmed maximum level and becomes a constant current with value IMAX.

t3: Fault occurs - CT has charged to 2.5V, fault output goes low, the FET turns off allowing no output current to flow, VOUT discharge to GND.

t4: Reset comparator threshold reached but no retry since LR pin held high.

t5 = t3: LR toggled low, NMOS turned on and sources current to load.

t6 = t3

t7: LR toggled low before VCT reaches reset comparator threshold, causing retry.

t8: Since LR toggled low during present cycle, NMOS turned on and sources current to load.

t9 = t0: Fault released, normal condition - return to normal operation of the hot swap power manager.

Figure 2b. Typical Timing Diagram Utilizing LR (Latch Reset) Function

APPLICATION INFORMATION (cont.)

gin charging with I3, a 3mA current source (refer to Figure 1) and continue to charge until approximately one volt below VCC, where it is clamped. This allows a constant fault to show up on $\overline{FAULT}$ and since the voltage on CT will only charge past 2.5V in an overload fault condition, it can be used for detection of output NMOS failure or to build redundancy into the system.

Estimating Minimum Timing Capacitance

The startup time of the IC may not exceed the fault time for the application. Since the timing capacitor, CT, determines the fault time, its minimum value can be determined by finding out the startup time of the IC. The startup time is dependent upon several external components. A load capacitor, CLOAD, should be tied between VOUTS and GND. Its value should be greater than that of CPUMP, the reservoir capacitor tied from VPUMP to VOUTS (see Figure 3). Given values of CLOAD, Load, RSENSE, VCC and the resistors determining the voltage on IMAX, the user can calculate the approximate startup time of the node VOUT. This time must be greater than the timer it takes for CT to charge to 2.5V. Assuming the user has determined the fault current, RSENSE can be calculated by:

$$R_{SENSE} = \frac{50mV}{I_{FAULT}}.$$

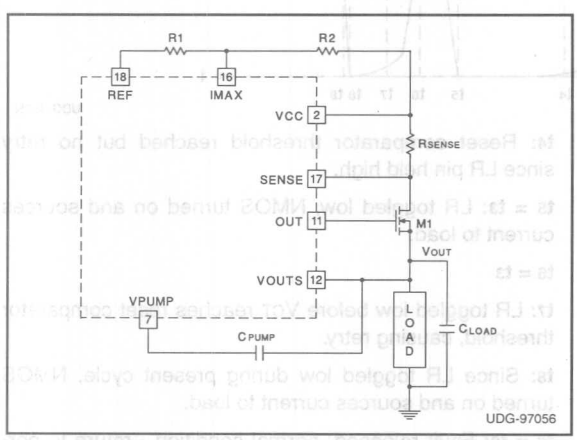


Figure 3. Estimating Minimum Timing Capacitor

IMAX is the maximum current the UC3914 will allow through the transistor M1. During startup with an output capacitor, M1 can be modeled as a constant current source of value IMAX where:

$$I_{MAX} = \frac{VCC - V_{IMAX}}{R_{SENSE}}$$

Given this information, calculation of startup time is now possible via the following:

Current Source Load:

$$T_{START} = \frac{C_{LOAD} \bullet VCC}{I_{MAX} - I_{LOAD}}$$

Resistive Load:

$$T_{START} = R_{LOAD} \bullet C_{LOAD} \bullet \ln \bullet \left(1 - \frac{VCC}{I_{MAX} \bullet R_{LOAD}}\right)$$

The only remaining external component which may affect the minimum timing capacitor is the optional power limiting resistor, RPL. If the addition of RPL is desirable, its value can be determined from the "Fault Timing" section above. The minimum timing capacitor values are now given by

Current Source Load:

$$C_{T\,MIN} = 2 \bullet T_{START} \bullet \left(\frac{10^{-4} \bullet R_{PL} + \frac{VCC}{2}}{2 \bullet R_{PL}}\right)$$

Resistive Load:

$$C_{T\,MIN} = 2 \bullet \frac{(10^4 \bullet R_{PL} + VCC - I_{MAX} \bullet R_{LOAD}) \bullet T_{START}}{2 \bullet R_{PL}}$$

$$+ \frac{(I_{MAX} \bullet R_{LOAD}^2 \bullet C_{LOAD})}{2 \bullet R_{PL}}$$

Output Current Softstart

The external MOSFET output current can be increased at a user-defined rate to ensure that the output voltage comes up in a controlled fashion by adding capacitor, CSS, as shown in Figure 4. The chip does place one constraint on the soft start time and that is that the charge pump time constant has to be much less than the soft-start time constant to ensure proper soft start operation. The time constant determining the startup time of the charge pump is given by:

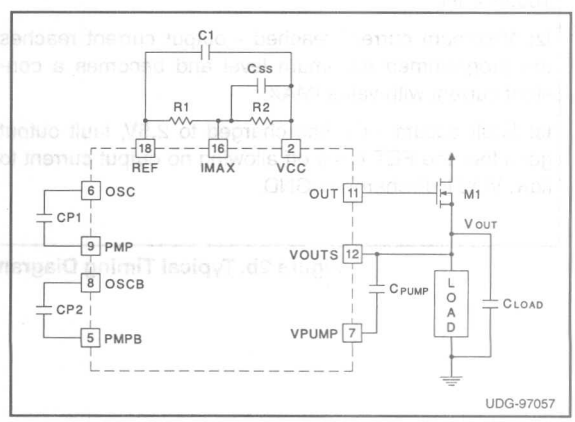


Figure 4. MOSFET Soft Start Diagram

APPLICATION INFORMATION (cont.)

$\tau_{CP} = R_{OUT} \bullet C_{PUMP}$

ROUT is the output impedance of the charge pump given by:

$$R_{OUT} = \frac{1}{f_{PUMP} \bullet C_P}$$

where fPUMP is the charge pump frequency (125kHz) and CP = CP1 = CP2 are the charge pump flying capacitors. For typical values of CP1, CP2 and CPUMP (0.01µF) and a switching frequency of 125kHz, the output impedance is 800Ω and the charge pump time constant is 8µs. The charge pump should be close to being fully charged in 3 time constants or 24µs. By placing a capacitor from VCC to IMAX, the voltage at IMAX, which sets the maximum output current of the FET, will exponentially decay from VCC to the desired value set by R1 and R2. The output current of the MOSFET will be controlled via soft start as long as the soft start time constant (τ_{SS}) is much greater than the charge pump time constant τ_{CP}, given by

$\tau_{SS} = (R1 \,||\, R2) \bullet C_{SS}$

Minimizing Total Dropout under Low Voltage Operation

In a typical application, the UC3914 will be used to control the output current of an external NMOS during hot swapping situations. Once the load has been fully charged, the desired output voltage on the load, VOUT, will be required to be as close to VCC as possible to minimize total dropout. For a resistive load, RLOAD, the output voltage is given by:

$$V_{OUT} = \frac{R_{LOAD}}{R_{LOAD} + R_{SENSE} + RDS_{ON}} \bullet VCC$$

RSENSE was picked to set the fault current, IFAULT. RDSON, the on-resistance of the NMOS, should be made as small as possible to ensure VOUT is as close to VCC as possible. The equation to calculate RDSON is

$$RDS_{ON} = \frac{1}{\left(\mu C_{OX} \bullet \frac{W}{L_{EFF}} \bullet (V_{GS} - V_T)\right)}, \text{ for } V_{DS} < V_{GS} - V_T$$

where µ is the mobility of electrons in the channel, Cox is the per unit area capacitance of the gate, W is the width of the gate, LEFF is the effective channel length of the gate, VGS is the gate to source voltage, VDS is the drain to source voltage and VT is the threshold voltage of the device. For a given NMOS, the manufacturer will specify the RDSON for a certain VGS (maybe 7V to 10V). The source potential of the NMOS is VOUT. In order to ensure sufficient VGS, this requires the gate of the NMOS, which is the output of the linear amplifier, to be many volts above VCC. The UC3914 provides the capability to generate this voltage through the addition of 3 capacitors, CP1, CP2 and CPUMP as shown in Figure 5. These capacitors should be used in conjunction with the complimentary output drivers and internal diodes included on-chip to create a charge pump or voltage tripler. The circuit boosts VCC by charging capacitors CP1, CP2 and CPUMP so that the voltage at VPUMP approximately equals 3 • (VCC - VDIODE), almost tripling the input supply voltage to the chip.

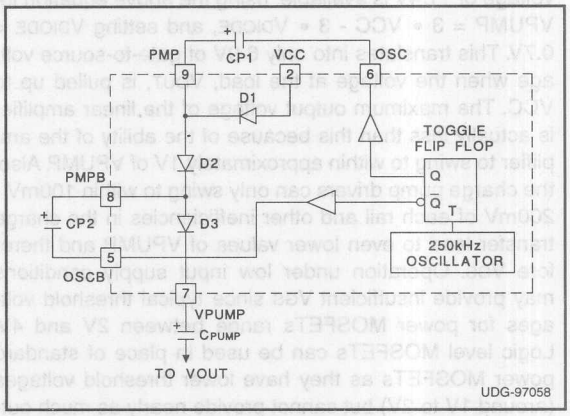


Figure 5. Charge Pump Block Diagram

On each complete cycle, CP1 is charged up to approximately VCC – VDIODE (unless VCC is greater than 15V causing internal clamping to limit this charging voltage to about 13V) when the output Q of the toggle flip flop is low. When $\overline{Q}$ is transistioned low (and Q correspondingly is brought high), the negative side of CP2 is pulled to ground, and CP1 charges CP2 up to about 2 • VCC – 2 • VDIODE. When $\overline{Q}$ is toggled high, the negative side of CP2 is brought to VCC. Since the voltage across a capacitor cannot change instantaneously with time, the positive side of the capacitor swings up to 3 • VCC – 2 •VDIODE. This charges CPUMP up to 3 • VCC – 3 • VDIODE.

A circuit operating at the 4.5V minimum input supply voltage for the IC poses a potential issue in ensuring sufficient gate drive to the external NMOS. The desired output current sourcing limit of the external NMOS, IMAX, is set by:

$$\frac{VCC - V_{IMAX}}{R_{SENSE}}$$

but whether the MOSFET will actually be able to source this current will depend upon what gate-to-source voltage is required to produce this current and other parameters discussed above. When the output device acts like a current source the drain current is given by:

APPLICATION INFORMATION (cont.)

$$I_D = \frac{\mu \bullet C_{OX}}{2} \bullet \frac{W}{L_{EFF}} \bullet (V_{GS} - V_T)^2, \text{ for } V_{DS} > V_{GS} - V_T$$

and is also equal to I_{MAX}, the programmed sourcing current. For a given FET, all device parameters in the above two equations are fixed including I_{MAX} and determine V_{GS}, provided enough charge pump voltage is available. When the NMOS acts like a resistor, the gate to source voltage wants to be maximized to ensure low R_{DSON}. For a 4.5V input supply voltage, a maximum charge pump voltage of 11.4V is available, using the above equation for VPUMP = 3 • VCC - 3 • V_{DIODE}, and setting V_{DIODE} = 0.7V. This translates into only 6.9V of gate-to-source voltage when the voltage at the load, V_{OUT}, is pulled up to VCC. The maximum output voltage of the linear amplifier is actually less than this because of the ability of the amplifier to swing to within approximately 1V of VPUMP. Also, the charge pump drivers can only swing to within 100mV - 200mV of each rail and other inefficiencies in the charge transfer lead to even lower values of VPUMP and therefore V_{GS}. Operation under low input supply conditions may provide insufficient V_{GS} since typical threshold voltages for power MOSFETs range between 2V and 4V. Logic level MOSFETs can be used in place of standard power MOSFETs as they have lower threshold voltages (around 1V to 2V) but cannot provide nearly as much output current, which may exclude them for use in certain applications.

Figure 6 shows a way to use the existing drivers with external diodes (or schottky diodes for even higher pump voltages but with additional cost) and capacitors to make a voltage quadrupler. The additional charge pump stage will provide a sufficient pump voltage (VPUMP = 4 • VCC – 4 • V_{DIODE}) to generate the maximum V_{GS}. Operation is similar to the case described above. This additional circuitry is not necessary for higher input voltages because the UC3914 has internal clamping which only allows VPUMP to be 10V greater than VOUTS.

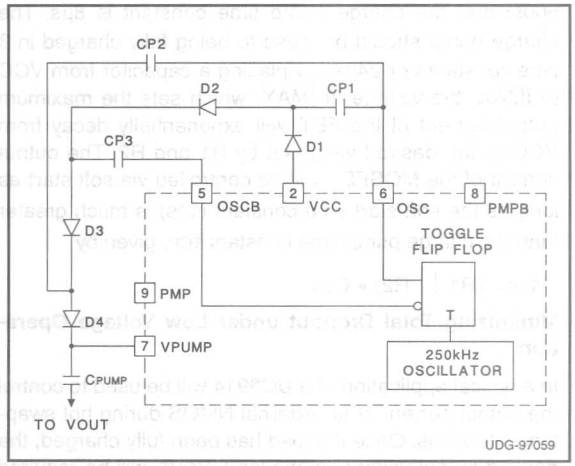


Figure 6. Low Voltage Operation to Produce Higher Pump Voltage

APPLICATION INFORMATION (cont.)

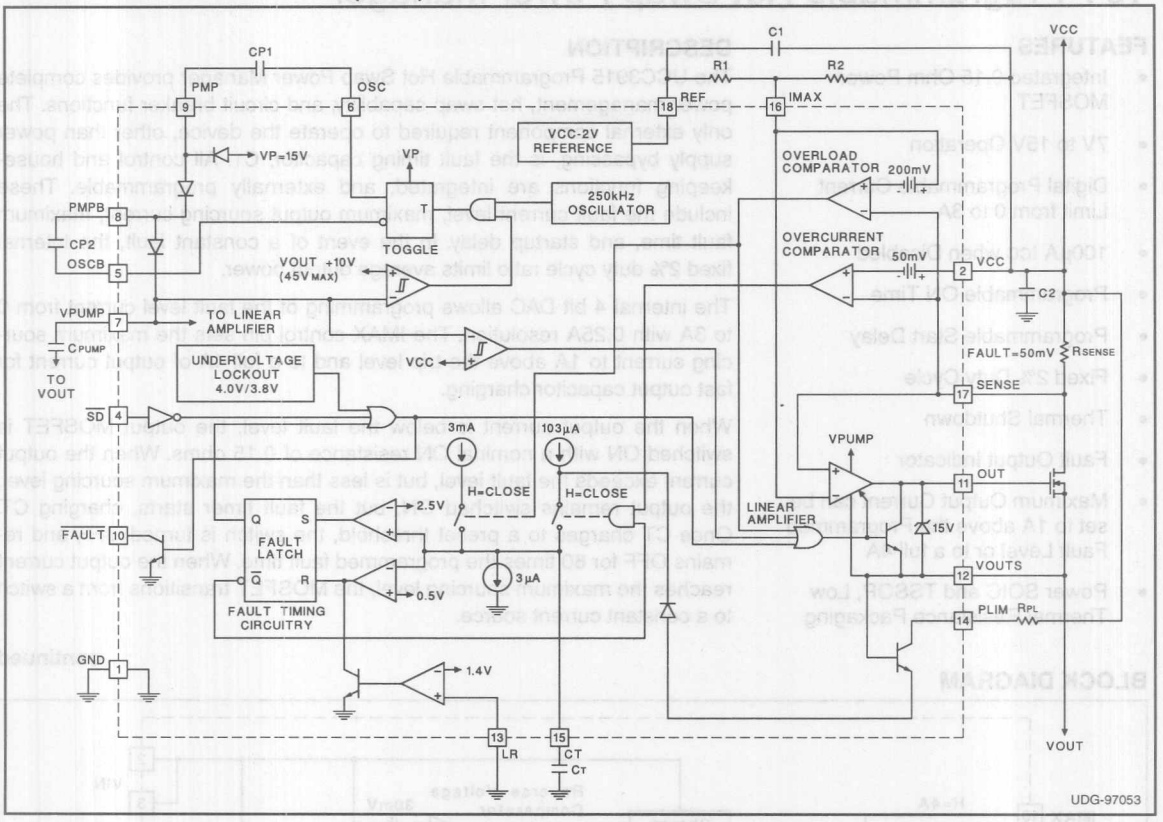


Figure 7. Typical Application

SAFETY RECOMMENDATIONS

Although the UC3914 is designed to provide system protection for all fault conditions, all integrated circuits can ultimately fail short. For this reason, if the UC3914 is intended for use in safety critical applications where UL or some other safety rating is required, a redundant safety device such as a fuse should be placed in series with the device. The UC3914 will prevent the fuse from blowing virtually all fault conditions, increasing system reliability and reducing maintainence cost, in addition to providing the hot swap benefits of the device.

UNITRODE CORPORATION
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15V Programmable Hot Swap Power Manager

FEATURES

- Integrated 0.15 Ohm Power MOSFET
- 7V to 15V Operation
- Digital Programmable Current Limit from 0 to 3A
- 100µA Icc when Disabled
- Programmable ON Time
- Programmable Start Delay
- Fixed 2% Duty Cycle
- Thermal Shutdown
- Fault Output Indicator
- Maximum Output Current can be set to 1A above the Programmed Fault Level or to a full 4A
- Power SOIC and TSSOP, Low Thermal Resistance Packaging

DESCRIPTION

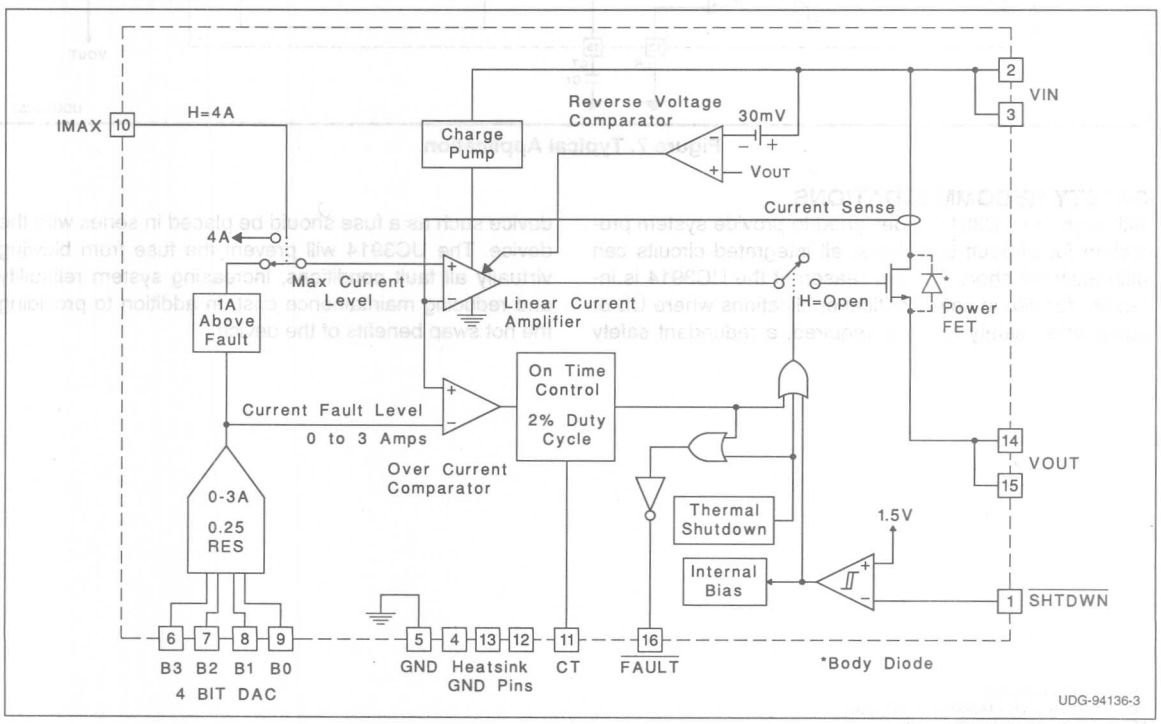
The UCC3915 Programmable Hot Swap Power Manager provides complete power management, hot swap capability, and circuit breaker functions. The only external component required to operate the device, other than power supply bypassing, is the fault timing capacitor, CT. All control and housekeeping functions are integrated, and externally programmable. These include the fault current level, maximum output sourcing current, maximum fault time, and startup delay. In the event of a constant fault, the Internal fixed 2% duty cycle ratio limits average output power.

The internal 4 bit DAC allows programming of the fault level current from 0 to 3A with 0.25A resolution. The IMAX control pin sets the maximum sourcing current to 1A above the trip level and to a full 4A of output current for fast output capacitor charging.

When the output current is below the fault level, the output MOSFET is switched ON with a nominal ON resistance of 0.15 ohms. When the output current exceeds the fault level, but is less than the maximum sourcing level, the output remains switched ON, but the fault timer starts, charging CT. Once CT charges to a preset threshold, the switch is turned OFF, and remains OFF for 60 times the programmed fault time. When the output current reaches the maximum sourcing level, the MOSFET transitions from a switch to a constant current source.

continued

BLOCK DIAGRAM



DESCRIPTION (cont.)

The UCC3915 can be put into sleep mode, drawing only 100µA of supply current. Other features include an open drain Fault Output Indicator, Thermal Shutdown, Undervoltage Lockout, 7V to 15V operation, and low thermal resistance SOIC and TSSOP Power Packages.

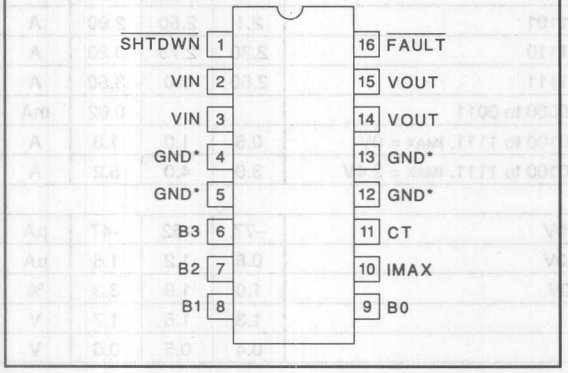
ABSOLUTE MAXIMUM RATINGS

VIN ..... +15.5 Volts
$\overline{\text{VOUT}}$ – VIN 0.3V
$\overline{\text{FAULT}}$ Sink Current 50mA
$\overline{\text{FAULT}}$ Voltage ..... –0.3 to 8V
Output Current ..... Self Limiting
TTL Input Voltage ..... –0.3 to VIN
Storage Temperature ..... –65°C to +150°C
Junction Temperature ..... –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

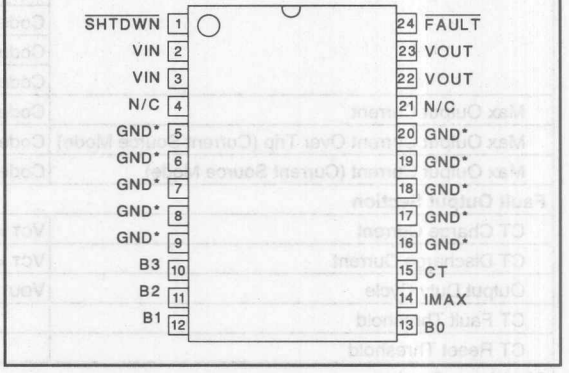
Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAMS

DIL-16, SOIC-16 (Top View)
N, DP Package



PWP-24 (Top View)
TSSOP Package



**Pin 5 serves as lowest impedance to the electrical ground; Pins 4, 12, and 13 serve as heat sink/ground. These pins should be connected to large etch areas to help dissipate heat. For N Package, pins 4, 12, and 13 are N/C.*

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply for TA = –40°C to +85°C for the UCC2915 and 0°C to 70°C for the UCC3915, VIN = 12V, IMAX = 0.4V, $\overline{\text{SHTDWN}}$ = 2.4V, TA = TJ.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Section					
Voltage Input Range		7.0		15.0	V
Supply Current			1.0	2.0	mA
Sleep Mode Current	$\overline{\text{SHTDWN}}$ = 0.2V		100	150	µA
Output Section					
Voltage Drop	IOUT = 1A (10V to 12V)		0.15	0.3	V
	IOUT = 2A (10V to 12V)		0.3	0.6	V
	IOUT = 3A (10V to 12V)		0.45	0.9	V
	IOUT = 1A, VIN = 7V and 15V		0.2	0.4	V
	IOUT = 2A, VIN = 7V and 15V		0.4	0.8	V
	IOUT = 3A, VIN = 7V, 12V Max.		0.6	1.2	V
Initial Startup Time	Note 2		100		µs
Short Circuit Response	Note 2		100		ns
Thermal Shutdown	Note 2		165		°C
Thermal Hysteresis	Note 2		10		°C

ELECTRICAL CHARACTERISTICS (cont.) Unless otherwise stated, these specifications apply for T_A = –40°C to +85°C for the UCC2915 and 0°C to 70°C for the UCC3915, VIN = 12V, IMAX = 0.4V, SHTDWN = 2.4V, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DAC Section					
Trip Current	Code = 0000-0011 (Device Off)				
	Code = 0100	0.15	0.25	0.35	A
	Code = 0101	0.35	0.50	0.65	A
	Code = 0110	0.60	0.75	0.90	A
	Code = 0111	0.85	1.00	1.15	A
	Code = 1000	1.0	1.25	1.5	A
	Code = 1001	1.25	1.50	1.75	A
	Code = 1010	1.5	1.75	2.0	A
	Code = 1011	1.70	2.00	2.3	A
	Code = 1100	1.90	2.25	2.58	A
	Code = 1101	2.1	2.50	2.90	A
	Code = 1110	2.30	2.75	3.20	A
	Code = 1111	2.50	3.0	3.50	A
Max Output Current	Code = 0000 to 0011			0.02	mA
Max Output Current Over Trip (Current Source Mode)	Code = 0100 to 1111, I_{MAX} = 0V	0.5	1.0	1.8	A
Max Output Current (Current Source Mode)	Code = 0100 to 1111, I_{MAX} = 2.4V	3.0	4.0	5.2	A
Fault Output Section					
CT Charge Current	V_{CT} = 1.0V	–77	–62	–47	µA
CT Discharge Current	V_{CT} = 1.0V	0.8	1.2	1.6	µA
Output Duty Cycle	V_{OUT} = 0V	1.0	1.9	3.3	%
CT Fault Threshold		1.3	1.5	1.7	V
CT Reset Threshold		0.4	0.5	0.6	V
Shutdown Section					
Shutdown Threshold		1.1	1.5	1.9	V
Shutdown Hysteresis			150		mV
Input Current			100	500	nA
Open Drain Output Section					
High Level Output Current	FAULT = 5V			250	µA
Low Level Output Voltage	I_{OUT} = 10mA		0.2	0.8	V
TTL Input DC Characteristics Section					
TTL Input Voltage High		2.0			V
TTL Input Voltage Low				0.8	V
TTL Input High Current	V_{IH} = 2.4V		3	10	µA

Note 1: All voltages are with respect to Ground. Current is positive into and negative out of the specified terminal.
Note 2: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

B0 - B3: These pins provide digital input to the DAC, which sets the fault current threshold. They can be used to provide a digital soft-start and adaptive current limiting.

CT: A capacitor connected to ground sets the maximum fault time. The maximum fault time must be more than the time required to charge the external capacitance in one cycle. The maximum fault time is defined as $T_{FAULT} = 16.1 \bullet 10^3 \bullet CT$. Once the fault time is reached the output will shutdown for a time given by $T_{SD} = 833 \bullet 10^3 \bullet CT$, this equates to a 1.9% duty cycle.

$\overline{\text{FAULT}}$: Open drain output, which pulls low upon any fault or interrupt condition, Fault, or Thermal Shutdown.

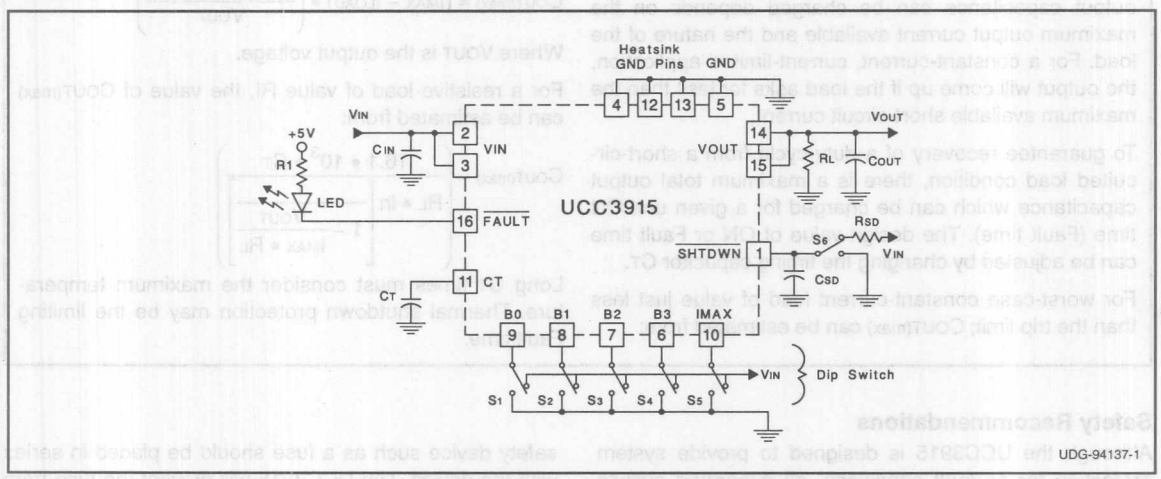
IMAX: When this pin is set to a logic low, the maximum sourcing current will always be 1A above the programmed fault level. When set to a logic high, the maximum sourcing current will be a constant 4A for applications which require fast charging of load capacitance.

$\overline{\text{SHTDWN}}$: When this pin is brought to a logic low, the IC is put into a sleep mode drawing typically less than 100µA of I_{CC}.The input threshold is hysteretic, allowing the user to program a startup delay with an external RC circuit.

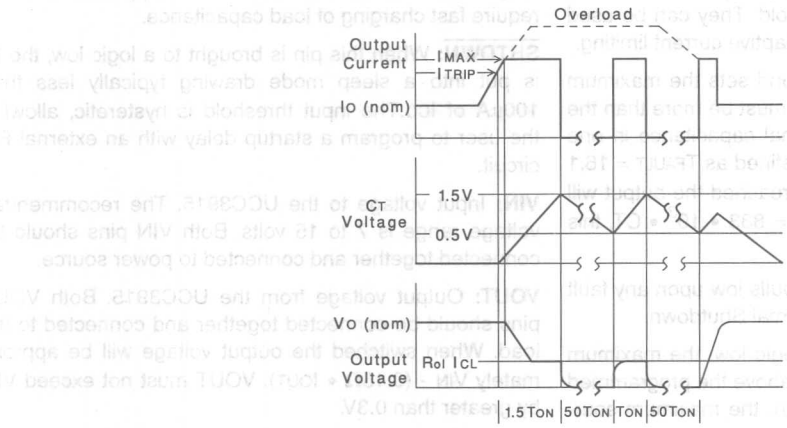
VIN: Input voltage to the UCC3915. The recommended voltage range is 7 to 15 volts. Both VIN pins should be connected together and connected to power source.

VOUT: Output voltage from the UCC3915. Both VOUT pins should be connected together and connected to the load. When switched the output voltage will be approximately $V_{IN} - (0.15\Omega \bullet I_{OUT})$. VOUT must not exceed VIN by greater than 0.3V.

Evaluation Circuit



Load Current, Timing Capacitor Voltage, and Output Voltage of the UCC3915 under Fault Conditions.



UDG-94138

Estimating Maximum Load Capacitance

For hot swap applications, the rate at which the total output capacitance can be charged depends on the maximum output current available and the nature of the load. For a constant-current, current-limited application, the output will come up if the load asks for less than the maximum available short-circuit current.

To guarantee recovery of a duty-cycle from a short-circuited load condition, there is a maximum total output capacitance which can be charged for a given unit ON time (Fault time). The design value of ON or Fault time can be adjusted by changing the timing capacitor C_T.

For worst-case constant-current load of value just less than the trip limit; $C_{OUT(max)}$ can be estimated from:

$$C_{OUT(max)} \approx (I_{MAX} - I_{LOAD}) \bullet \left(\frac{16.1 \bullet 10^3 \bullet C_T}{V_{OUT}} \right)$$

Where V_{OUT} is the output voltage.

For a resistive load of value RI, the value of $C_{OUT(max)}$ can be estimated from:

$$C_{OUT(max)} \approx \left(\frac{16.1 \bullet 10^3 \bullet C_T}{R_L \bullet \ln \left[\frac{1}{1 - \frac{V_{OUT}}{I_{MAX} \bullet R_L}} \right]} \right)$$

Long C_T times must consider the maximum temperature. Thermal shutdown protection may be the limiting Fault time.

Safety Recommendations

Although the UCC3915 is designed to provide system protection for all fault conditions, all integrated circuits can ultimately fail short. For this reason, if the UCC3915 is intended for use in safety critical applications where UL or some other safety rating is required, a redundant safety device such as a fuse should be placed in series with the device. The UCC3915 will prevent the fuse from blowing for virtually all fault conditions, increasing system reliability and reducing maintenance cost, in addition to providing the hot swap benefits of the device.

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
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SCSI Termpower Manager

FEATURES

- Integrated Circuit Breaker Function
- Integrated 0.2 Ohm Power FET
- SCSI, SCSI-2, SCSI-3 Compliant
- 1µA ICC When Disabled
- Programmable On Time
- Accurate 1.65A Trip Current/ 2.1A Max Current
- Fixed 3% Duty Cycle
- Uni-Directional Switch
- Thermal Shutdown

DESCRIPTION

The UCC3916 SCSI termpower manager provides complete power management, hot swap capability, and circuit breaker functions with minimal external components. For most applications, the only external component required to operate the device, other than supply bypassing, is a timing capacitor which sets the fault time.

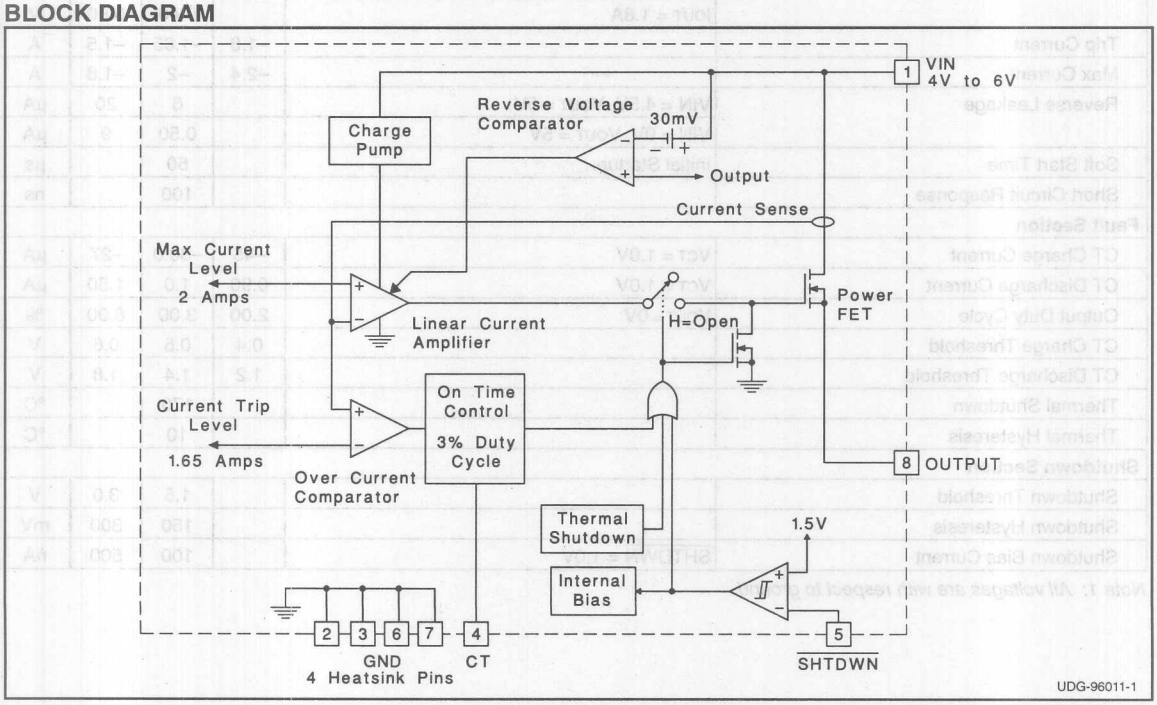
The current trip level is internally set at 1.65A, and the maximum current level is also internally programmed for 2A. While the output current is below the trip level of 1.65A, the internal power MOSFET is switched on at a nominal 220mΩ. When the output current exceeds the trip level but remains less than the maximum current level, the MOSFET remains switched on, but the fault timer starts charging CT. Once the fault time is reached, the circuit will shut off for a time which equates to a 3% duty cycle. Finally, when the output current reaches the maximum current level, the MOSFET transitions from a switch to a constant current source.

The UCC3916 is designed for uni-directional current flow, emulating a diode in series with the power MOSFET.

The UCC3916 can be put in a sleep mode, drawing only 1µA of supply current.

Other features include thermal shutdown and low thermal resistance Small Outline Power package.

BLOCK DIAGRAM



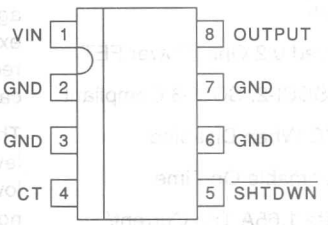
ABSOLUTE MAXIMUM RATINGS

VIN . . . . . +6V
Output Current
DC . . . . . Self Limiting
Pulse (Less than 100ns) 20A
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C

Currents are positive into, negative out of the specified terminal.
Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAMS

SOIC-8 (Top View)
DP Package



ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these parameters apply for T_J = 0°C to +70°C; VIN = 5V, $\overline{SHTDWN}$ = 2.4V, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current Section					
ICC			1.00	2.00	mA
ICC - Sleep Mode	$\overline{SHTDWN}$ = 0.2V		0.50	5	µA
Output Section					
Voltage Drop	I_{OUT} = 1A		0.22	0.33	V
	I_{OUT} = 1.5A		0.33	0.50	V
	I_{OUT} = 1.8A		0.40	0.60	V
Trip Current		–1.8	–1.65	–1.5	A
Max Current		–2.4	–2	–1.8	A
Reverse Leakage	VIN = 4.5V, V_{OUT} = 5V		6	20	µA
	VIN = 0V, V_{OUT} = 5V		0.50	9	µA
Soft Start Time	Initial Startup		50		µs
Short Circuit Response			100		ns
Fault Section					
CT Charge Current	V_{CT} = 1.0V	–45	–36.0	–27	µA
CT Discharge Current	V_{CT} = 1.0V	0.90	1.0	1.50	µA
Output Duty Cycle	V_{OUT} = 0V	2.00	3.00	6.00	%
CT Charge Threshold		0.4	0.5	0.6	V
CT Discharge Threshold		1.2	1.4	1.8	V
Thermal Shutdown			170		°C
Thermal Hysteresis			10		°C
Shutdown Section					
Shutdown Threshold			1.5	3.0	V
Shutdown Hysteresis			150	300	mV
Shutdown Bias Current	$\overline{SHTDWN}$ = 1.0V		100	500	nA

Note 1: All voltages are with respect to ground.

PIN DESCRIPTIONS

CT: A capacitor is applied between this pin and ground to set the maximum fault time. The maximum fault time must be more than the time to charge external capacitance. The maximum fault time is defined as

$$T_{FAULT} = 28 \bullet 10^3 \bullet CT.$$

Once the fault time is reached the output will shutdown for a time given by:

$$T_{SD} = 1 \bullet 10^6 \bullet CT$$

this results in a 3% duty cycle. 0.1µF is recommended for SCSI applications to achieve the normal maximum capacitance on the Termpwr line.

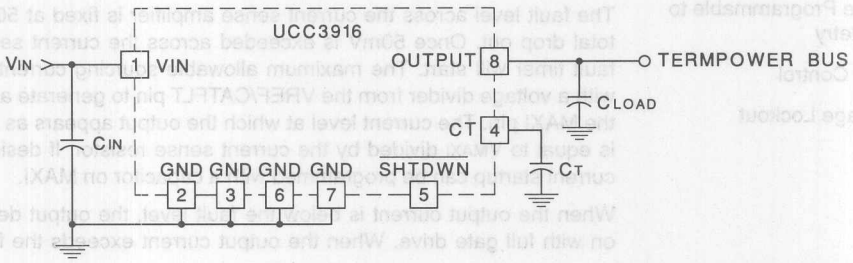
$\overline{SHTDWN}$: When this pin is brought low, the IC is put into sleep mode.

VIN: Input voltage to the circuit breaker, ranging from 4V to 6V.

VOUT: Output voltage of the circuit breaker. When switched, the output voltage is approximately:

$$V_{OUT} = VIN - (220m\Omega) \bullet I_{OUT}.$$

TYPICAL APPLICATION



UDG-97094

SAFETY RECOMMENDATIONS

Although the UCC3916 is designed to provide system protection for all fault conditions, all integrated circuits can ultimately fail short. For this reason, if the UCC3916 is intended for use in safety critical applications where UL or some other safety rating is required, a redundant safety device such as a fuse should be placed in series with the device. The UCC3916 will prevent the fuse from blowing virtually all fault conditions, increasing system reliability and reducing maintainence cost, in addition to providing the hot swap benefits of the device.

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Positive Floating Hot Swap Power Manager

ADVANCED INFORMATION

FEATURES

- Precision Fault Threshold
- Programmable Average Power Limiting
- Programmable Linear Current Control
- Programmable Overcurrent Limit
- Programmable Fault Time
- Internal Charge Pump to Control External NMOS Device
- Fault Output and Catastrophic Fault Indication
- Fault Mode Programmable to Latch or Retry
- Shutdown Control
- Undervoltage Lockout

DESCRIPTION

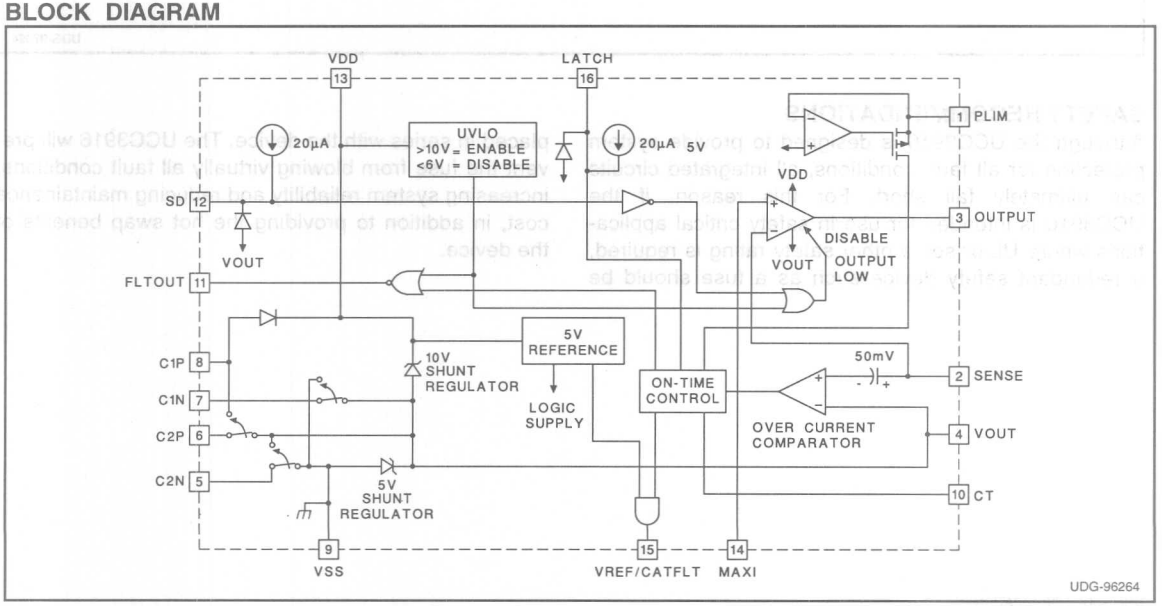
The UCC3917 family of positive floating hot swap managers provides for complete power management, hot swap, and fault handling capability for PC boards. The voltage limitation of the application is only restricted by the external component voltage limitation and not the IC. The IC provides it's own supply rail via a charge pump off of VOUT. The charge pump derives its power from the onboard 5V shunt regulator, and thus, IDD is provided by the output load. The onboard 10V shunt regulator protects the IC from excess voltage. The IC also has catastrophic fault indication to alert the user that the ability to shut off the output NMOS has been bypassed. All control and housekeeping functions are integrated and externally programmable. These include the fault current level, maximum output sourcing current, maximum fault time, soft start time, and average NMOS power limiting. In the event of a constant fault, the internal timer will limit the on time/off time ratio from less than 0.1% to a maximum 3%, depending on the fault condition. In order to maintain constant average output power, the PLIM pin is provided to sense the drain voltage of the external NMOS through a resistor, and modulate duty cycle accordingly.

The fault level across the current sense amplifier is fixed at 50mV to minimize total drop out. Once 50mV is exceeded across the current sense resistor, the fault timer will start. The maximum allowable sourcing current is programmed with a voltage divider from the VREF/CATFLT pin to generate a fixed voltage on the MAXI pin. The current level at which the output appears as a current source is equal to V_{MAXI} divided by the current sense resistor. If desired, a controlled current startup can be programmed with a capacitor on MAXI.

When the output current is below the fault level, the output device is switched on with full gate drive. When the output current exceeds the fault level, but is

Continued

BLOCK DIAGRAM



DESCRIPTION (cont.)

less than maximum allowable sourcing level programmed by MAXI, the output remains switched on, and the fault timer starts charging CT. Once CT charges to 2.5V, the output device is turned off and attempts either a retry sometime later or waits for the state on the LATCH pin to charge if in latch mode. When the output current reaches the maximum sourcing current level, the output device appears as a current source.

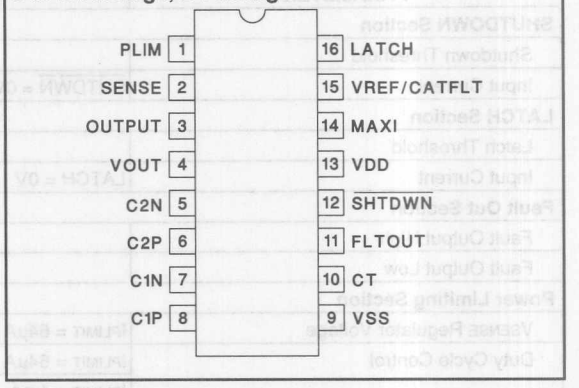
ABSOLUTE MAXIMUM RATINGS

IDD 5mA
SHTDWN Current 250µA
LATCH Current 250µA
VREF Current 250µA
PLIM Current 5mA
MAXI Input Voltage ..... VIN
Storage Temperature ..... –65°C to +150°C
Junction Temperature ..... –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

Currents are positive into, negative out of the specified terminal.
Consult Packaging Section of Databook for thermal limitations and considerations of package.

CONNECTION DIAGRAM

DIL-16, SOIC-16 (Top View)
J or N Package, D Package



ELECTRICAL CHARACTERISTICS: Unless otherwise specified, T_A = 0°C to 70°C for the UCC3917, –40°C to 85° for the UCC2917 and –55°C to 125°C for the UCC1917, C_T = 4.7nF. T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VCC Section					
Icc	From VOUT		5		mA
UVLO Turn On Threshold			10		V
UVLO Off Voltage			6.5		V
VSS Regulator Voltage			–5		V
Fault Timing Section					
Overcurrent Threshold	T_A = 25°C		50		mV
	Over Operating Temperature		50		mV
Overcurrent Input Bias			50		nA
CT Charge Current	V_{CT} = 1V		36		µA
CT Discharge Current	V_{CT} = 1V		1		µA
CT Fault Threshold			2.5		V
CT Reset Threshold			0.5		V
Output Duty Cycle	Fault Condition		3		%
Output Section					
Output High Voltage			V_{IN}+7	V_{IN}+9	V
	I_{OUT} = –500µA VIN+5	V_{IN}+5	V_{IN}+7	V_{IN}+9	V
Output Low Voltage			0		V
	I_{OUT} = 500µA		0.7		V
	VDD = V_{IN} + 9V, I_{OUT} = 1mA		1.2		V
Linear Current Section					
Sense Control Votlage	MAXI = 100mV		100		mV
	MAXI = 400mV		400		mV
Input Bias			50		nA

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, T_A = 0°C to 70°C for the UCC3917, –40°C to 85° for the UCC2917 and –55°C to 125°C for the UCC1917, C_T = 4.7nF. T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SHUTDOWN Section					
Shutdown Threshold			2.5		V
Input Current	$\overline{SHTDWN}$ = 0V		20		µA
LATCH Section					
Latch Threshold			2.5		V
Input Current	LATCH = 0V		20		µA
Fault Out Section					
Fault Output High			4		V
Fault Output Low			0.05		V
Power Limiting Section					
V_{SENSE} Regulator Voltage	I_{PLIMIT} = 64µA		5		V
Duty Cycle Control	I_{PLIMIT} = 64µA		1		%
	I_{PLIMIT} = 1mA		0.1		%
VREF/CATFLT Section					
V_{REF} Regulator Voltage			5		V
Fault Output Low			0.05		V
Delay to Output	(Note 2)		50		ns
Output Sink Current	V_{SENSE} – V_{MAXI} = 300mV		5		mA
Threshold	Relative to MAXI		200		mV

Note 1: All voltages are with respect to VOUT. Current is positive into and negative out of the specified terminal.
Note 2: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

C1N: Negative side of the upper charge pump capacitor.

C1P: Positive side of the upper charge pump capacitor.

C2N: Negative side of the lower charge pump capacitor.

C2P: Positive side of lower charge pump capacitor.

CT: A capacitor is connected to this pin to set the maximum fault time. The maximum fault time must be more than the time to charge the external load capacitance (see Application Information). The maximum fault time is defined as

$$T_{FAULT} = \frac{2 \bullet C_T}{I_{CH}},$$

where I_{CH} = 36µA + I_{PLIM}, and I_{PLIM} is the current into the power limit pin. Once the fault time is reached, the output will shutdown for a time given by: $T_{SD} = 2 \bullet 10^6 \bullet CT$.

FLTOUT: This pin provides fault output indication. Interface to this pin is usually performed through level shift transistors. Under a non-fault condition, FLTOUT will pull to a high state. When shutdown is driven high, the output disables the NMOS pass device. When brought low, shutdown is disabled and the IC functions as intended. Users should note there will be an RC delay to the output dependent upon the external capacitor at this pin.

LATCH: Pulling this pin low causes a fault to latch until this pin is brought high or a power on reset is attempted. However, pulling this pin high before the reset time is reached will not clear the fault until the reset time is reached. Keeping LATCH high will result in normal operation of the fault timer. Users should note there will be an RC delay dependent upon the external capacitor at this pin.

MAXI: This pin programs the maximum allowable sourcing current. Since VREF/CATFLT is a regulated voltage, a voltage divider can be derived to generate the program level for MAXI. The current level at which the output appears as a current source is equal to the voltage on MAXI over the current sense resistor. If desired, a controlled current start up can be programmed with a capacitor on MAXI (to VOUT), and a programmed start delay can be achieved by driving the shutdown with an open collector/drain device into an RC network.

OUTPUT: Output device to the NMOS pass element.

PLIM: This feature ensures that the average NMOS power dissipation is controlled. A resistor is connected from this pin to the drain of the NMOS pass element. When the voltage across the NMOS exceeds 5V, current will flow into PLIM which adds to the fault timer charge

PIN DESCRIPTIONS (cont.)

current, reducing the duty cycle form the 3% level. When $P_{FET\ AVG} = IMAX \bullet 1 \bullet 10^6 \bullet RPL$.

SENSE: Input voltage from the current sense resistor. When there is greater than 50mV across this pin with respect to VOUT, a fault is sensed, and CT starts to charge.

$\overline{\text{SHTDWN}}$: This pin provides shutdown control. Interface to this pin is usually performed through level shift transistors. When shutdown is driven high, the output disables the NMOS pass device. When brought low, shutdown is disabled and the IC functions as intended. Users should note there will be an RC delay to the output dependent upon the external capacitor at this pin.

VDD: Power to the chip. On startup, power is current fed from a resistor (and a series diode) to VIN. In normal operation, power will be supplied by the charge pump.

VOUT: Ground reference for the IC.

VREF/CATFLT: This pin primarily provides an output reference for the programming of MAXI. Secondarily, it provides catastrophic fault output indication. Under a catastrophic fault, when the IC is unsuccessfully attempting to shutdown the NMOS pass device, this pin will pull to a low state. In and application, this pin could be connected to a second NMOS transistor in series with the main NMOS for redundancy. Due to the primary function of this pin, full gate drive would not be available to the series NMOS.

VSS: Negative reference out of the chip. Normally current fed via a resistor to ground.

APPLICATION INORMATION

Fault Timing

Figure 1 shows the detailed circuitry for the fault timing function of the UCC3917. For simplicity, we first consider a typical fault mode where the overload comparator and the current source 13 do not come into play. A typical fault occurs once the voltage across the current sense resistor, RS, exceeds 50mV. This causes the over current comparator to trip and the timing capacitor to charge with current source I1 plus the current from the power limiting amplifier, or PLIM amplifier. The PLIM amplifier is designed to only source current into the CT pin and to begin sourcing current once the voltage across the output FET exceeds 5V. The current IPL is related to the voltage across the FET with the following expression:

$$I_{PL} = \frac{(V_{IN} - VOUT) - 5V}{R_{PL}}$$

Later, it will be shown how this feature will limit average power dissipation in the pass device. Note that under normal fault conditions where the output current is just above the fault level, VOUT ≅ VIN, IPL = 0, and the CT charging current is just I1 or 36µA.

During a fault, CT will charge at a rate determined by the internal charging current and the external timing capaci-

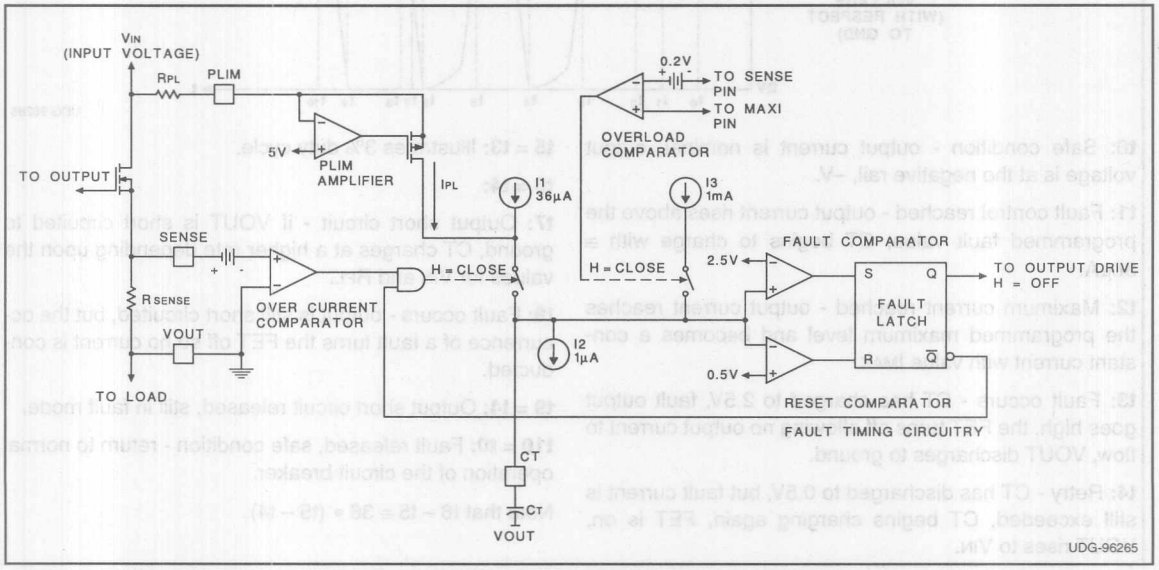


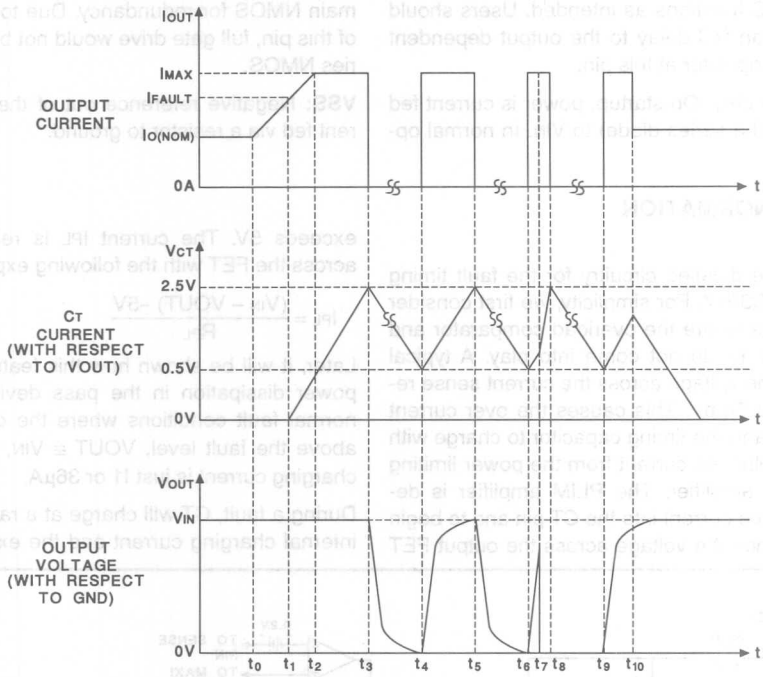
Figure 1. Fault Timing Circuitry for the UCC3917, Including Power Limit and Overload.

APPLICATION INFORMATION (cont.)

tor. Once CT charges to 2.5V, the fault comparator switches and sets the fault latch. Setting the fault latch causes both the output to switch off and the charging switch to open. CT must now discharge with current source I2 until 0.5V is reached. Once the voltage at CT reaches 0.5V, the fault latch resets (assuming LATCH is high, otherwise the fault latch will not reset until the LATCH pin is brought high or a power on reset occurs) which re-enables the output and allows the fault circuitry to regain control of the charging switch. If a fault is still present, the overcurrent comparator will close the charging switch causing the cycle to repeat. Under a constant fault the duty cycle is given by:

$$\text{Duty Cycle} = \frac{1\mu A}{I_{PL} + 36\mu A}$$

where I_{PL} is 0µA under normal operations (see Figure 2).



t0: Safe condition - output current is nominal, output voltage is at the negative rail, –V.

t1: Fault control reached - output current rises above the programmed fault value, CT begins to charge with ≅ 36µA.

t2: Maximum current reached - output current reaches the programmed maximum level and becomes a constant current with value IMAX.

t3: Fault occurs - CT has charged to 2.5V, fault output goes high, the FET turns off allowing no output current to flow, VOUT discharges to ground.

t4: Retry - CT has discharged to 0.5V, but fault current is still exceeded, CT begins charging again, FET is on, VOUT rises to VIN.

t5 = t3: Illustrates 3% duty cycle.

t6 = t4:

t7: Output short circuit - if VOUT is short circuited to ground, CT charges at a higher rate depending upon the values for VIN and RPL.

t8: Fault occurs - output is still short circuited, but the occurrence of a fault turns the FET off so no current is conducted.

t9 = t4: Output short circuit released, still in fault mode.

t10 = t0: Fault released, safe condition - return to normal operation of the circuit breaker.

Note that t6 – t5 ≅ 36 • (t5 – t4).

Figure 2. Nominal Timing Diagram

APPLICATION INFORMATION (cont.)

However, under large transients, average power dissipation can be limiting using the PLIM pin. A proof follows, average dissipation in the pass element is given by:

$$P_{FET\ AVG} = (V_{IN} - VOUT) \bullet I_{MAX} \bullet \text{Duty Cycle}$$

$$= (V_{IN} - VOUT) \bullet I_{MAX} \bullet \frac{1\mu A}{I_{PL} + 36\mu A}$$

Where $(V_{IN} - VOUT) >> 5V$,

$$I_{PL} \cong \frac{V_{IN} - VOUT}{R_{PL}}$$

and where $I_{PL} >> 36\mu A$, the duty cycle can be approximated as:

$$\frac{1\mu A \bullet R_{PL}}{V_{IN} - VOUT}.$$

Therefore the average power dissipation in the MOSFET can be approximated by:

$$P_{FET\ AVG} = (V_{IN} - VOUT) \bullet I_{MAX} \bullet \frac{1\mu A \bullet R_{PL}}{V_{IN} - VOUT}$$

$$= I_{MAX} \bullet 1\mu A \bullet R_{PL}$$

Notice that since $(V_{IN} - VOUT)$ cancels, average power dissipation is limited in the NMOS pass element (see Figure 3). Also, a value for RPL can be roughly determined from this approximation.

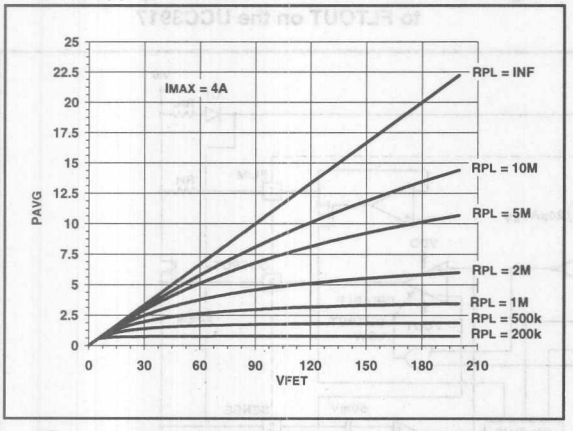


Figure 3. Plot of Average Power vs. FET Voltage for Increasing Values of RPL

Overload Comparator

The linear amplifier in the UCC3917 ensures that the output NMOS does not pass more than IMAX (which is VMAXI/RS). In the event the output current exceeds the programmed IMAX by 0.2V/RS, which can only occur if the output FET is not responding to a command from the IC, CT will begin charging with I3, 1mA, and continue to charge eventually tripping a catastrophic fault comparator not shown. This comparator will then drive VREF/CATFLT low, which can be used to build redundancy into the system if desirable (as outlined in the pin description for VREF/CATFLT).

Selecting Minimum Timing Capacitance

The startup time of the IC may not exceed the fault time for the application. Since the timing capacitor, CT, determines the fault time, it's minimum value can be determined by first finding out the startup time. The startup time is dependent on several external components. For example, a capacitive load is required for the IC to startup, and will be referred to as CLOAD. CIN, also required and equal to 0.1µF, represents the capacitor between the VDD and VOUT pins. There also exists a relationship between the two capacitor values which states that

$$\frac{V_{IN} \bullet C_{IN}}{(C_{IN} + C_{LOAD})} < 15V$$

Let IMAX be the maximum current allowable through the external NMOS device (programmed via MAXI, of course). Then, we can define the startup time of the IC as such:

Current Source Load:

$$T_{START} = \frac{1.2 \bullet C_{LOAD} \bullet V_{IN}}{I_{MAX} - I_{LOAD}}$$

Resistive Load:

$$T_{START} = \frac{1.2 \bullet C_{LOAD} \bullet V_{IN}}{I_{MAX} - I_{LOAD}}$$

The only remaining external component which may affect the minimum timing capacitor value is the optional power limiting resistor, RPL. If RPL is desired, it's value can be determined form the "Fault Timing" section above. Finally, the minimum timing capacitor can now be calculated.

Current Source Load:

$$C_{Tmin} = \frac{3 \bullet T_{START} \bullet (62\mu A \bullet R_{PL} + V_{IN} - 10V)}{10V \bullet R_{PL}}$$

Resistive Load:

$$C_{Tmin} = \frac{3 \bullet T_{START} \bullet (31\mu A \bullet R_{PL} + V_{IN} - 5V - I_{MAX} \bullet R_{LOAD})}{5V \bullet R_{PL}}$$

$$+ \frac{3 \bullet R_{LOAD}\ V_{IN} \bullet C_{LOAD}}{5V \bullet R_{PL}}$$

If RPL is not used and PLIM is left unconnected, the equations simplify to $C_{Tmin} = 18.6\Omega \bullet T_{START}$ for either load condition.

APPLICATION INFORMATION (cont.)

Selecting Other External Components

Other external components are necessary for correct operation of the IC. Referring to the application diagram at the back of the data sheet, resistors RSENSE, RSS, R1, R2 and R3 are required and follow certain equations with a brief description following where applicable:

$$R_{SENSE} = \frac{50mV}{I_{FAULT}} \text{ (Sense Resistor)}$$

$$R_{SS} = \frac{V_{IN} - 5V}{5mA} \text{ (Connected between VSS and GND)}$$

$$R3 = \frac{V_{IN} - 10}{5mA} \text{ (Used in series with a diode to connect VIN to VDD)}$$

$(R1 + R2) > 20k\Omega$ (Current limit out of VREF)

Lastly, the external capacitors used for the charge pump are required and need to equal 0.1µF, i.e. CIN = CH = C1 = C2 = 0.1µF.

Level Shift Circuitry (Optional)

The level shift circuitry shown in Figure 4 and Figure 5 represents one way of performing interface to LATCH, SD, and FLTOUT. These pins provide functionality that is not necessary for normal operation of the IC but may prove useful to the application. The resistor, R, shown in both figures is used for current limiting and follows RMIN = VIN/250µA. The capacitor, C, shown in both figures is optional to the level shift circuitry and keeps spurious signals from occurring during transients. It's minimum value is CMIN = 0.1nF. It should be noted that the use of the capacitor, C, will cause delays into and out of these pins.

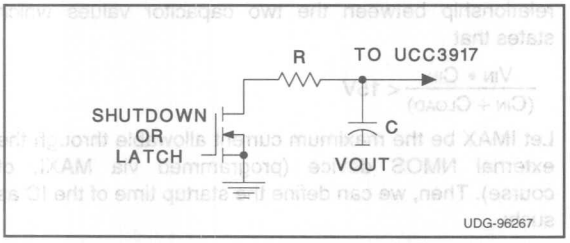


Figure 4. Potential Level Shift Circuitry to Interface to LATCH AND $\overline{\text{SHTDWN}}$ on the UCC3917

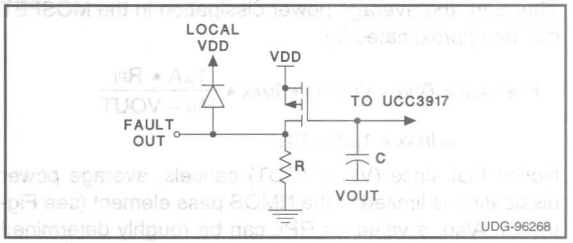


Figure 5. Potential Level Shift Circuitry to Interface to FLTOUT on the UCC3917

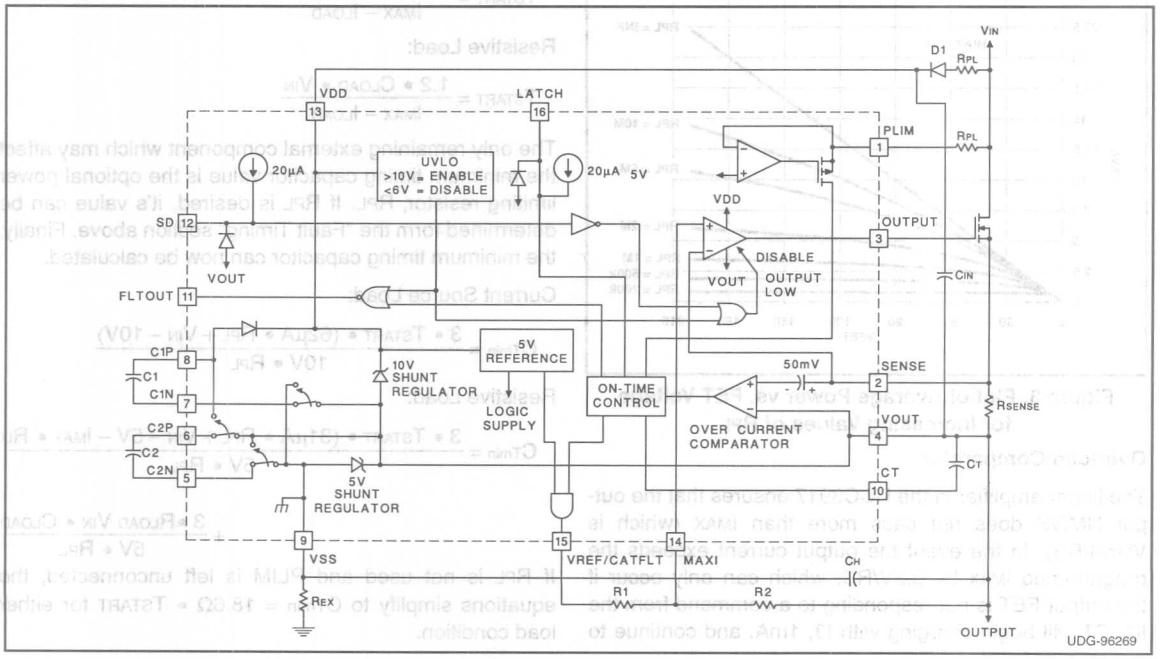


Figure 5. Positive Floating Hot Swap Power Manager

SAFETY RECOMMENDATIONS

Although the UCC3917 is designed to provide system protection for all fault conditions, all integrated circuits can ultimately fail short. For this reason, if the UCC3917 is intended for use in safety critical applications where UL or some other safety rating is required, a redundant safety device such as a fuse should be placed in series with the power device. The UCC3917 will prevent the fuse from blowing for virtually all fault conditions, increasing system reliability and reducing maintenance cost, in addition to providing the hot swap benefits of the device.

UNITRODE CORPORATION
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Low On Resistance Hot Swap Power Manager

PRELIMINARY

FEATURES

- Integrated 0.06Ω Power MOSFET
- 3V to 6V Operation
- External Analog control of Fault Current from 0A to 4A
- Independent Analog Control of Current Limit up to 5A
- Fast Overload Protection
- Minimal External Components
- 1µA Icc when Disabled
- Programmable On Time
- Programmable Start Delay
- Fixed 3% Duty Cycle

DESCRIPTION

The UCC3918 Low on Resistance Hot Swap Power Manager provides complete power management, hot swap capability, and circuit breaker functions. The only components needed to operate the device, other than supply bypassing, are a timing capacitor, and 2 programming resistors. All control and housekeeping functions are integrated, and externally programmable. These include the fault current level, maximum output sourcing current, maximum fault time, and startup delay. In the event of a constant fault, the internal fixed 3% duty cycle ratio limits the average output power. The IFAULT pin allows linear programming of the fault level current from 0A to 5A.

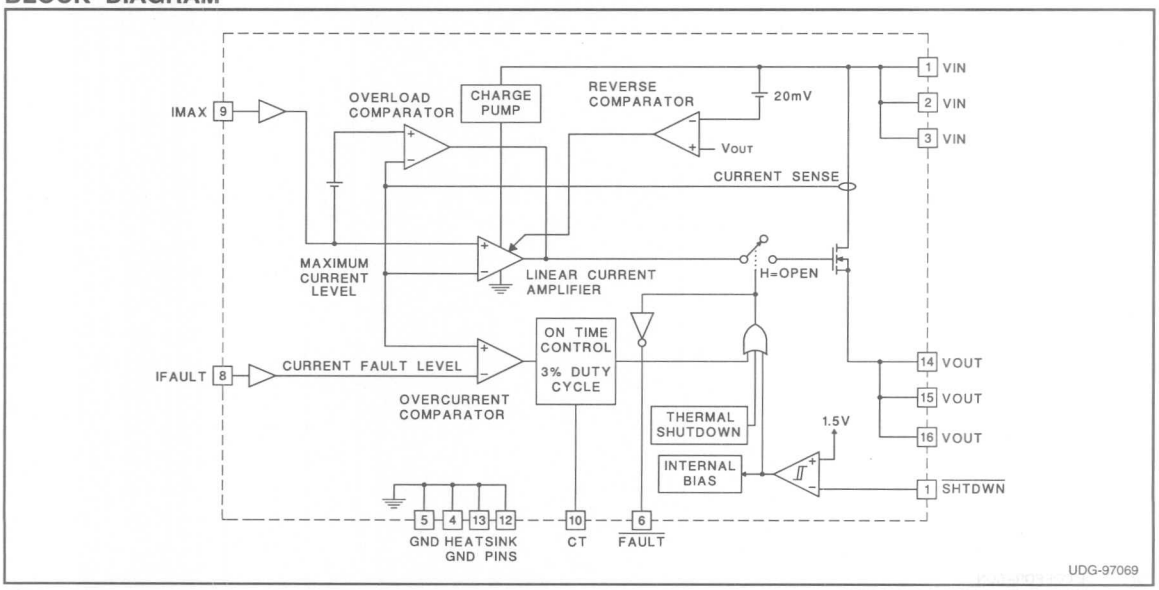
Fast overload protection is accomplished by an additional overload comparator. Its threshold is internally set above the maximum sourcing current limit setting. In the event of a short circuit or extreme current condition, this comparator is tripped, shutting down the output. This function is needed since the maximum sourcing current limit loop has a finite bandwidth.

When the output current is below the fault level, the output MOSFET is switched on with a nominal resistance of 0.06Ω. When the output current exceeds the fault level of the maximum sourcing level, the output remains on, but the fault timer starts charging CT. Once CT charges to a preset threshold, the switch is turned off, and remains off for 30 times the programmed fault time. When the output current reaches the maximum sourcing level, the MOSFET transitions form a switch to a constant current source.

The UCC3918 is designed for unidirectional current flow, emulating an ideal diode in series with the power switch. This feature is particularly attractive in applications where many devices are powering a common bus, such as with SCSI

Continued

BLOCK DIAGRAM



DESCRIPTION (cont.)

TERMPWR. The UCC3918 can also be put into the sleep mode, drawing only 1µA of supply current.

Other features include an open drain fault output indicator, thermal shutdown, undervoltage lockout, 3V to 6V operation, and a low thermal resistance small outline power package.

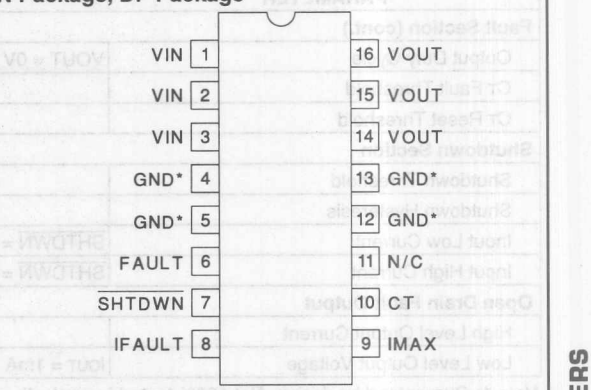
ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage (VIN) 8V
SOIC Power Dissipation 2.5W
Fault Output Sink Current 50mA
Fault Output Voltage ..... VIN
Output Current (DC) ..... Internally Limited
TTL Input Voltage ..... –0.3V to VIN
Storage Temperature ..... –65°C to +150°C
Junction Temperature ..... –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

Unless otherwise indicated, voltages are reference to ground and currents are positive into, negative out of the specified terminal. Pulsed is defined as a less than 10% duty cycle with a maximum duration of 500µS. Consult Packaging Section of Databook for thermal limitations and considerations of package.

CONNECTION DIAGRAM

DIL-16, SOIC-16 (Top View)
N Package, DP Package



** Pin 5 serves as the lowest impedance to the electrical ground. Pins 4, 12, and 13 serve as heat sink/ground. These pins should be connected to large etch PCB areas to help dissipate heat.*
For N Package, pins 4, 12, and 13 are N/C.

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, TA = 0°C to 70°C for the UCC3918, –40°C to 85° for the UCC2918, VIN = 5V. RIMAX = 42.2k, RIFAULT = 52.3k, SHTDWN = 2.4. TA = TJ.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Section					
Voltage Input Range, VIN		3	5	6	V
VDD Supply Current	No Load		1	2	mA
Sleep Mode Current	SHTDWN = 0.2V		0.5	5	µA
Output Section					
RDSON	IOUT = 1A to 4A, VIN = 5V, TA = 25°C		0.075	0.095	Ω
	IOUT = 1A to 4A, VIN = 3V, TA = 25°C		0.09	0.116	Ω
	IOUT = 1A to 4A, VIN = 5V		0.75	0.125	Ω
	IOUT = 1A to 4A, VIN = 3V		0.09	0.154	Ω
Initial Startup Time	(Note 1)		100		µS
Thermal Shutdown	(Note 1)		170		DEG
Thermal Hysteresis	(Note 1)		10		DEG
Output Leakage	SHTDWN = 0.2V			20	µA
Trip Current	RIFAULT = 105k	0.75	1	1.25	A
	RIFAULT = 52.3k	1.7	2	2.3	A
	RIFAULT = 34.8k	2.5	3	3.5	A
	RIFAULT = 25.5k	3.3	4	4.7	A
Maximum Output Current	RIMAX = 118k	0.5	1	2	A
	RIMAX = 60.4k	1	2	3	A
	RIMAX = 42.2k	2	3	4	A
	RIMAX = 33.2k	3	4	5	A
	RIMAX = 27.4k	3.75	5	6.25	A
Fault Section					
CT Charge Current	VCT = 1V	–50	–36	–22	µA
CT Discharge Current	VCT = 1V	0.72	1.2	1.6	µA

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, T_A = 0°C to 70°C for the UCC3918, –40°C to 85° for the UCC2918, VIN = 5V. R_{IMAX} = 42.2k, R_{IFAULT} = 52.3k, $\overline{SHTDWN}$ = 2.4. T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Fault Section (cont.)					
Output Duty Cycle	VOUT = 0V	1.5	3	6	%
C_T Fault Threshold		1	1.3	1.6	V
C_T Reset Threshold		0.25	0.5	0.75	V
Shutdown Section					
Shutdown Threshold		1.1	1.5	1.9	V
Shutdown Hysteresis			100		mV
Input Low Current	$\overline{SHTDWN}$ = 0V	–500	0	500	nA
Input High Current	$\overline{SHTDWN}$ = 2V	–2	–1	–0.5	µA
Open Drain Fault Output					
High Level Output Current				1	µA
Low Level Output Voltage	I_{OUT} = 1mA		0.4	0.9	V

Note 1: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

CT: A capacitor connected to this pin sets the maximum fault time. The maximum must be more than the time to charge external load capacitance. The maximum fault time is defined as

$$T_{FAULT} = 27.8^3 \bullet C_T.$$

Once the fault time is reached the output will shutdown for a time given by

$$T_{SD} = 8.33^6 \bullet C_T,$$

this equates to a 3% duty cycle.

FAULT: Open drain output, which pulls low upon any condition which causes the output to open; Fault, Thermal Shutdown, Shutdown, and maximum sourcing current greater than the fault time.

GND: This is the most negative voltage in the circuit. All 4 ground pins should be used, and properly heat sunk on the PCB.

IFAULT: A resistor connected from this pin to ground sets the fault threshold. The resistor vs fault current is set by the formula

$$R_{FAULT} = \frac{97.5k}{I_{TRIP}}$$

IMAX: A resistor connected from this pin to ground sets the maximum sourcing current. The resistor vs the output sourcing current is set by the formula,

$$R_{IMAX} = \frac{86.45k}{\text{Maximum Sourcing Current}}$$

A resistor and capacitor combination can also be connected from this pin to VIN to provide a controlled sourcing current startup delay.

$\overline{SHTDWN}$: When this pin is brought low, the IC is put into sleep mode. The input threshold is hysteretic, allowing the user to program a startup delay with an external RC circuit.

VIN: This is the input voltage to the UCC3918. The recommended operating voltage range is 3V to 6V. All VIN pins should be connected together and to the power source.

VOUT: Output voltage for the circuit breaker. When switched the output voltage will be approximately VIN - 0.06Ω • I_{OUT}. All VOUT pins should be connected together and to the load.

APPLICATION INORMATION

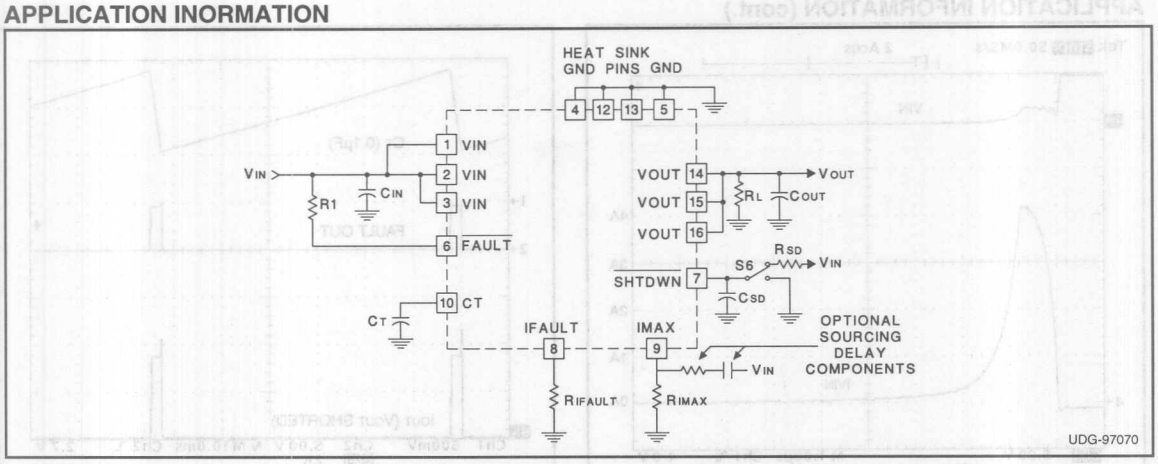
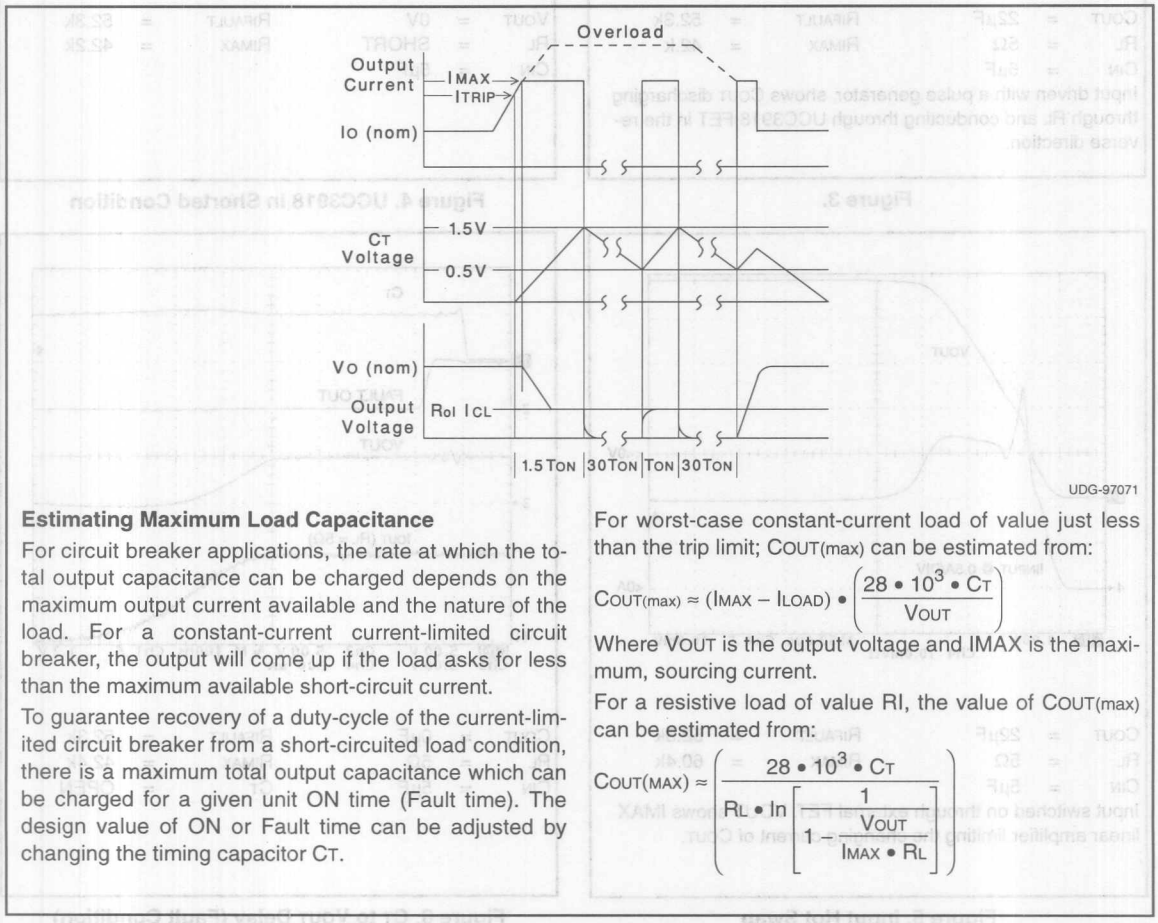


Figure 1. Evaluation Circuit



Estimating Maximum Load Capacitance

For circuit breaker applications, the rate at which the total output capacitance can be charged depends on the maximum output current available and the nature of the load. For a constant-current current-limited circuit breaker, the output will come up if the load asks for less than the maximum available short-circuit current.

To guarantee recovery of a duty-cycle of the current-limited circuit breaker from a short-circuited load condition, there is a maximum total output capacitance which can be charged for a given unit ON time (Fault time). The design value of ON or Fault time can be adjusted by changing the timing capacitor C_T.

For worst-case constant-current load of value just less than the trip limit; $C_{OUT(max)}$ can be estimated from:

$$C_{OUT(max)} \approx (I_{MAX} - I_{LOAD}) \bullet \left(\frac{28 \bullet 10^3 \bullet C_T}{V_{OUT}} \right)$$

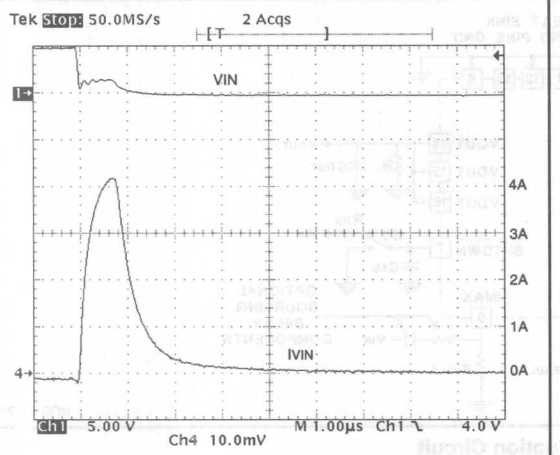
Where V_{OUT} is the output voltage and IMAX is the maximum, sourcing current.

For a resistive load of value RI, the value of $C_{OUT(max)}$ can be estimated from:

$$C_{OUT(MAX)} \approx \left(\frac{28 \bullet 10^3 \bullet C_T}{R_L \bullet \ln \left[\frac{1}{1 - \frac{V_{OUT}}{I_{MAX} \bullet R_L}} \right]} \right)$$

Figure 2. Load Current, Timing Capacitor Voltage and Output Voltage of the UCC3918 Under Fault Conditions

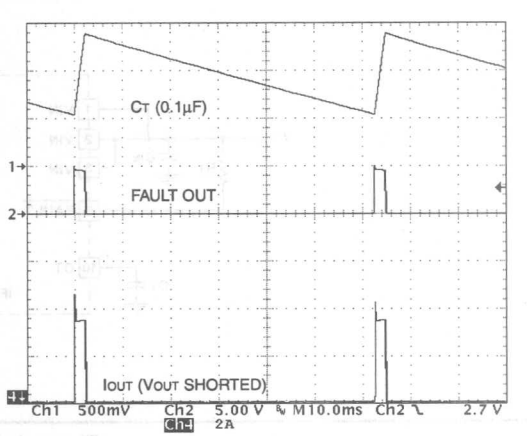
APPLICATION INFORMATION (cont.)



COUT	=	22µF	RIFAULT	=	52.3k
RL	=	5Ω	RIMAX	=	42.k
CIN	=	5µF			

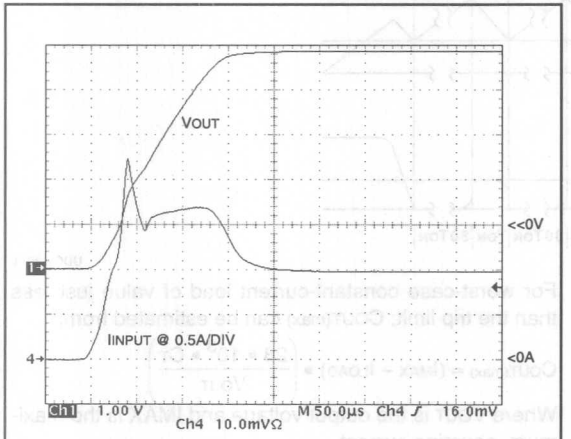
Input driven with a pulse generator, shows COUT discharging through RL and conducting through UCC3918 FET in the reverse direction.

Figure 3.



VOUT	=	0V	RIFAULT	=	52.3k
RL	=	SHORT	RIMAX	=	42.2k
CIN	=	5µF			

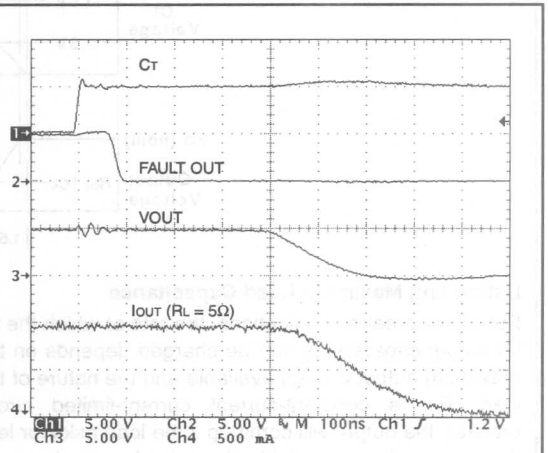
Figure 4. UCC3918 in Shorted Condition



COUT	=	22µF	RIFAULT	=	52.3k
RL	=	5Ω	RIMAX	=	60.4k
CIN	=	5µF			

Input switched on through external FET. VOUT shows IMAX linear amplifier limiting the changing current of COUT.

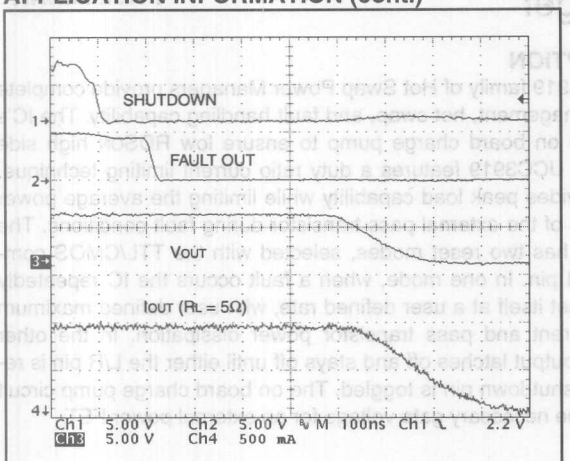
Figure 5. Input Hot Swap



COUT	=	0µF	RIFAULT	=	52.3k
RL	=	5Ω	RIMAX	=	42.4k
CIN	=	5µF	CT	=	OPEN

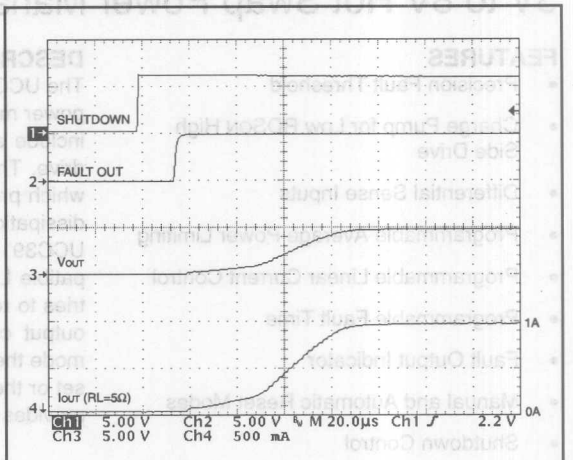
Figure 6. CT to VOUT Delay (Fault Condition)

APPLICATION INFORMATION (cont.)



COUT = 0µF
RL = 5Ω
CIN = 5µF
RIFAULT = 52.3k
RIMAX = 42.4k

Figure 7. Shutdown Delay to VOUT Off



COUT = 0µF
RL = 5Ω
CIN = 5µF
RIFAULT = 52.3k
RIMAX = 42.4k
VOUT rising shows ramp time of internal charge pump driving on chip FET.

Figure 8. Shutdown Delay to VOUT On

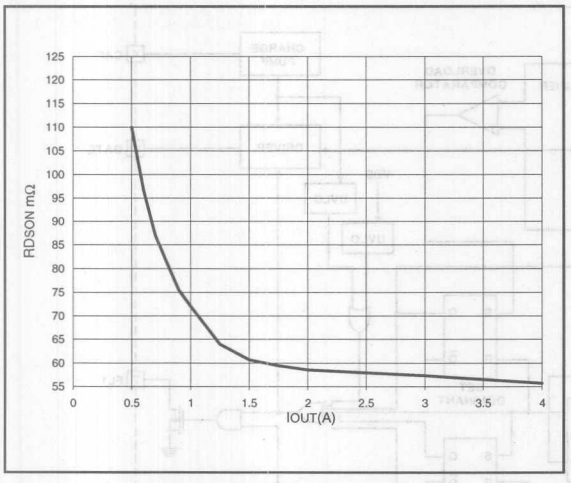


Figure 9. RDSON vs IOUT

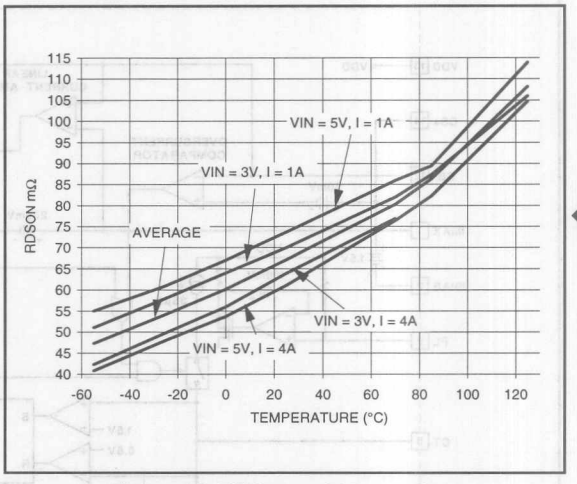


Figure 10. RDSON vs Temperature

SAFETY RECOMMENDATIONS

Although the UCC3918 is designed to provide system protection for all fault conditions, all integrated circuits can ultimately fail short. For this reason, if the UCC3918 is intended for use in safety critical applications where UL or some other safety rating is required, a redundant safety device such as a fuse should be placed in series with the power device. The UCC3918 will prevent the fuse from blowing for virtually all fault conditions, increasing system reliability and reducing maintenance cost, in addition to providing the hot swap benefits of the device.

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

3V to 8V Hot Swap Power Manager

PRELIMINARY

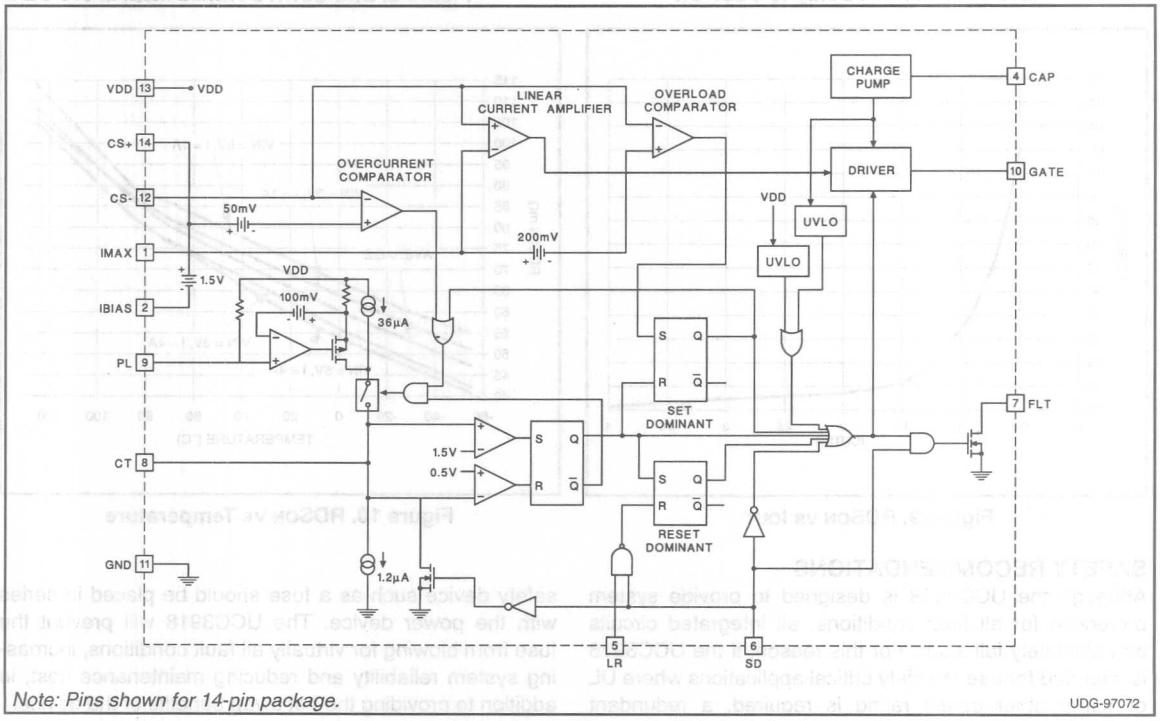
FEATURES

- Precision Fault Threshold
- Charge Pump for Low RDSON High Side Drive
- Differential Sense Inputs
- Programmable Average Power Limiting
- Programmable Linear Current Control
- Programmable Fault Time
- Fault Output Indicator
- Manual and Automatic Reset Modes
- Shutdown Control
- Undervoltage Lockout
- Electronic Circuit Breaker Function

DESCRIPTION

The UCC3919 family of Hot Swap Power Managers provide complete power management, hot swap, and fault handling capability. The IC's include an on board charge pump to ensure low RDSON high side drive. The UCC3919 features a duty ratio current limiting technique, which provides peak load capability while limiting the average power dissipation of the external pass transistor during fault conditions. The UCC3919 has two reset modes, selected with the TTL/CMOS compatible L/R pin. In one mode, when a fault occurs the IC repeatedly tries to reset itself at a user defined rate, with user defined maximum output current and pass transistor power dissipation. In the other mode the output latches off and stays off until either the L/R pin is reset or the shutdown pin is toggled. The on board charge pump circuit provides the necessary gate voltage for an external power FET.

BLOCK DIAGRAM



Note: Pins shown for 14-pin package.

UDG-97072

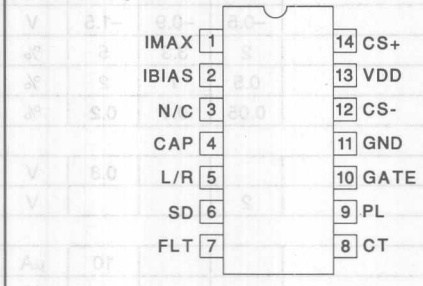
ABSOLUTE MAXIMUM RATINGS

VDD ..... –0.3V to 10V
Pin Voltage (All pins except CAP and GATE) ..... –0.3V to VDD + 0.3V
Pin Voltage (CAP and GATE) ..... –0.3V to 15V
PL Current ..... 0.5mA to –10mA
IBIAS Current ..... 0mA to 3mA
Storage Temperature ..... –65°C to +150°C
Junction Temperature ..... –55°C to +150°C
Lead Temperature (Soldering, 10sec.) ..... +300°C

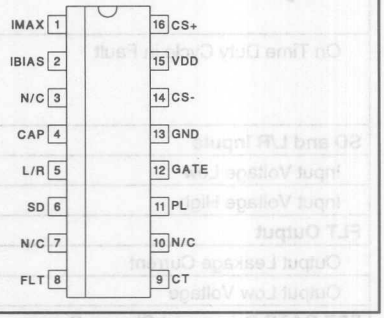
Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of package.

CONNECTION DIAGRAM

DIL-14, (Top View)
N, J Packages



SOIC-16 (Top View)
D Package



ELECTRICAL CHARACTERISTICS: Unless otherwise specified, VDD = 5V, TA = 0°C to 70°C for the UCC3919, –40°C to 85° for the UCC2919 and –55°C to 125°C for the UCC1919. All voltages are with respect to GND. TA = TJ.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply					
Supply Current	VDD = 3V		0.5	1	mA
	VDD = 8V		1	1.5	mA
Shutdown Current	SD = 0.2V		1	5	µA
Undervoltage Lockout					
Minimum Voltage to Start		2.5	2.75	3	V
Minimum Voltage after Start		2	2.25	2.5	V
Hysteresis		0.25	0.5	0.75	V
IBIAS					
Output Voltage (IOUT = 1mA)	25°C, referred to CS+	1.47	1.5	1.53	V
	Over Temperature Range, referred to CS+	1.44	1.5	1.56	V
Maximum Output Current		1	2		mA
Maximum Bypass Capacitance				2	nF
Current Sense					
Over Current Comparator Offset	Referred to CS+	–55	–50	–45	mV
Linear Current Amplifier Offset	VIMAX = 100mV, Referred to CS+	–120	–100	–80	mV
	VIMAX = 400mV, Referred to CS+	–440	–400	–360	mV
Overload Comparator Offset	VIMAX = 100mV, Referred to CS+	–360	–300	–240	mV
CS- Input Voltage Range	Referred to VDD, 3V ≤ VDD ≤ 8V	–1.5		0.2	V
CS+ Input Voltage Range	Referred to VDD, 3V ≤ VDD ≤ 8V	0		0.2	V
Input Bias Current CS-			1	5	µA
Input Bias Current CS+			100	200	µA

ELECTRICAL CHARACTERISTICS (cont.): Unless otherwise specified, VDD = 5V, T_A = 0°C to 70°C for the UCC3919, –40°C to 85° for the UCC2919 and –55°C to 125°C for the UCC1919. All voltages are with respect to GND. T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Current Fault Timer					
CT Charge Current	V_{CT} = 1V	–56	–35	–16	µA
CT Discharge Current	V_{CT} = 1V	0.5	1.2	1.9	µA
On Time Duty Cycle in Fault	I_{PL} = 0	2	3.3	5	%
CT Fault Threshold		1.3	1.5	1.7	V
CT Reset Threshold		0.4	0.5	0.6	V
IMAX					
Input Bias Current		10	16	22	µA
Power Limiting Section					
Voltage on PL	I_{PL} = –250µA, Referred to VDD	–0.10	–0.15	–0.25	V
	I_{PL} = –1.5mA, Referred to VDD	–0.5	–0.9	–1.5	V
On Time Duty Cycle in Fault	I_{PL} = 0µA	2	3.3	5	%
	I_{PL} = –250µA	0.5	1	2	%
	I_{PL} = –1.5mA	0.05	0.1	0.2	%
SD and L/R Inputs					
Input Voltage Low				0.8	V
Input Voltage High		2			V
FLT Output					
Output Leakage Current	VDD = 5V			10	µA
Output Low Voltage	I_{OUT} = 10mA			1	V
FET GATE Driver and Charge Pump					
Peak Output Current		–2	–1.5	–1	mA
Peak Sink Current			100		mA
On Time During Fault			200		nS
Maximum Output Voltage	VDD = 3V, Average I_{OUT} = 1µA	10	11	11.5	V
	VDD = 8V, Average I_{OUT} = 1µA	13	14	15	V
Charge Pump Source Impedance	VDD = 5V, Average I_{OUT} = 1µA		80		kΩ

PIN DESCRIPTIONS

CAP: A capacitor is placed from this pin to ground to filter the output of the on board charge pump. A 0.1µF capacitor is recommended .

CS-: The negative current sense input signal.

CS+: The positive current sense input signal.

CT: Input to the duty cycle timer. A capacitor is connected from this pin to ground, setting the off time and the maximum on time of the overcurrent protection circuits.

FLT: Fault indicator. This open drain output will pull low under any fault condition where the output driver is disabled. This output is disabled when the IC is in low current standby mode.

GATE: The output of the MOSFET driver. This pin drives the gate of an N-channel MOSFET pass transistor. The error amplifier/driver control loop is internally compensated, and guaranteed stable for output load (gate) capacitance between 100pF and 10nF.

GND: The ground reference for the device.

IBIAS: Output of the on board bias generator internally regulated to 1.5V below CS+. A resistor divider between this pin and CS+ can be used to generate the IMAX voltage. The bias circuit is internally compensated, and requires no bypass capacitance. If an external bypass is required due to a noisy environment, the circuit will be stable with up to 1nF of capacitance. The bypass must be to CS+, since the bias voltage is generated with respect to CS+.

IMAX: Used to program the maximum allowable sourcing current. The voltage on this pin is with respect to CS+. If the voltage across the shunt resistor exceeds this voltage a linear amplifier lowers the voltage at GATE to limit the output current to this level. If the voltage across the shunt resistor goes more than 200mV beyond this voltage, the gate drive pin GATE is immediately driven low and kept low for one full off time interval.

PIN DESCRIPTIONS (cont.)

L/R: Latch/Reset. This pin sets the reset mode. If L/R is low and a fault occurs the device will begin duty ratio current limiting. If L/R is high and a fault occurs, GATE will go low and stay low until L/R is set low. This pin is internally pulled low by a 3µA nominal pulldown.

PL: Power Limit. This pin is used to control average power dissipation in the external MOSFET. If a resistor is connected from this pin to the source of the external MOSFET, the current in the resistor will be roughly proportional to the voltage across the FET. As the voltage across the FET increases, this current is added to the fault timer charge current, reducing the on time duty cycle from its nominal value of 3% and limiting the average power dissipation in the FET.

SD: Shutdown pin. If this pin is taken low, GATE will go low, and the IC will go into a low current standby mode and CT will be discharged. This TTL compatible input must be driven high to turn on.

Shutdown Characteristics

When the SD pin is set to TTL high (above 2V) the UCC3919 is guaranteed to be enabled. When SD is set to a low TTL (below 0.8V) the UCC3919 is guaranteed to be disabled, but may not be in ultra low current sleep mode. When SD is set to 0.2V or less, the UCC3919 is guaranteed to be disabled and in ultra low current sleep mode.

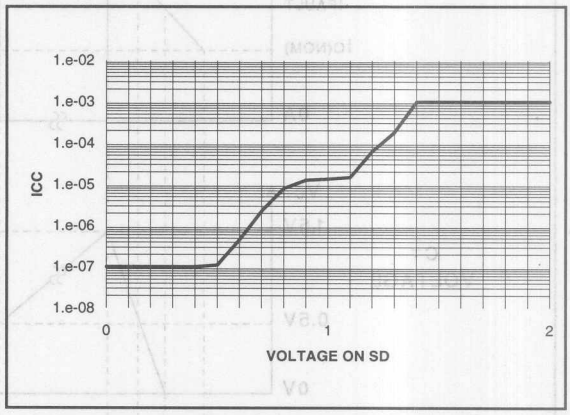


Figure 5. Typical Shutdown Current

APPLICATION INFORMATION

The UCC3919 monitors the voltage drop across a high side sense resistor and compares it against three different voltage thresholds. These are discussed below. Figure 1 shows the UCC3919 waveforms under fault conditions.

Fault Threshold

The first threshold is fixed at 50mV. If the current is high enough such that the voltage on CS- is 50mV below CS+, the timing capacitor C_T begins to charge at about 35µA if the PL pin is open. (Power limiting will be discussed later). If this threshold is exceeded long enough for C_T to charge to 1.5V, a fault is declared and the external MOSFET will be turned off. It will either be latched off (until the power to the circuit is cycled, the L/R pin is taken low, or the SD pin is toggled), or will retry after a fixed off time (when C_T has discharged to 0.5V), depending on whether the L/R pin is set high or low by the user. The equation for this current threshold is simply:

$$I_{FAULT} = \frac{0.05}{R_{SENSE}} \quad (1)$$

The first time a fault occurs, C_T is at ground, and must charge 1.5V. Therefore:

$$t_{FAULT} = t_{ONsec} \cong \frac{C_T(\mu F) \bullet 1.5}{35} \quad (2)$$

In the retry mode, the timing capacitor will already be charged to 0.5V at the end of the off time, so all subsequent cycles will have a shorter ton time, given by:

$$t_{FAULT} = t_{ONsec} \cong \frac{C_T(\mu F)}{35} \quad (3)$$

Note that these equations for ton are without the power limiting feature (R_{PL} pin open). The effects of power limiting on ton will be discussed later.

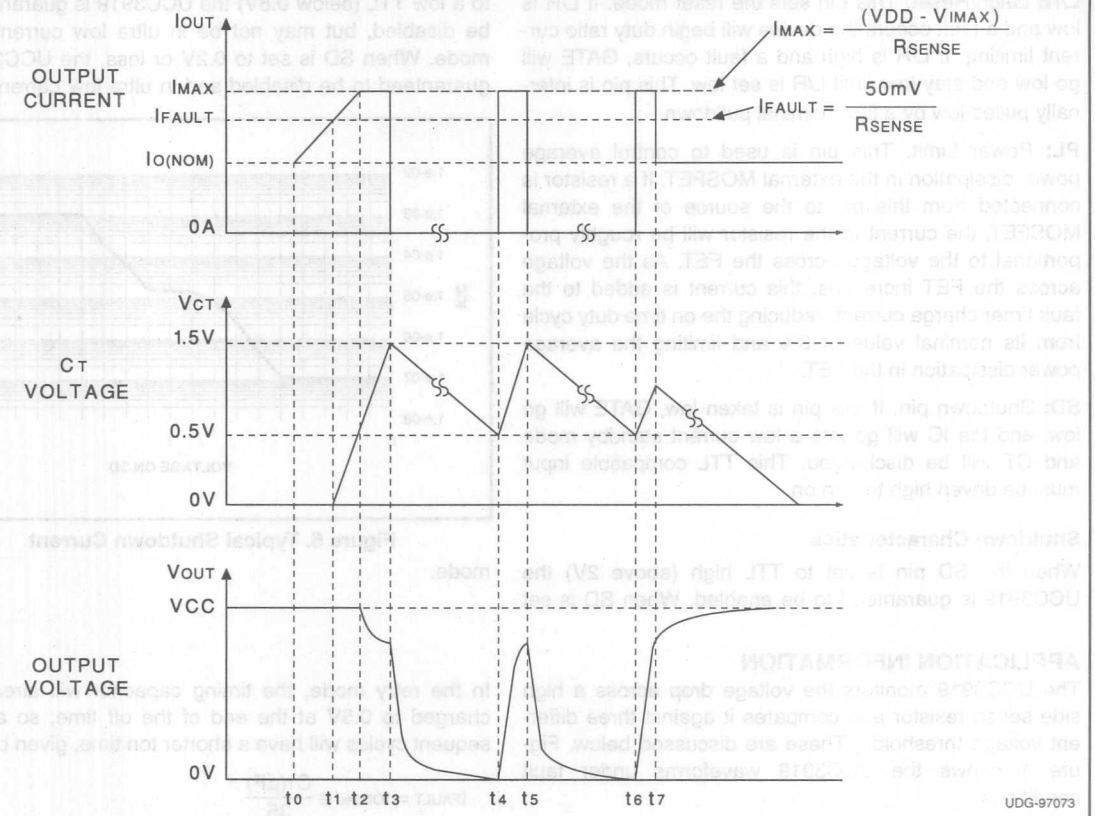
The off time in the retry mode is set by C_T and an internal 1.2µA sink current. It is the time it takes C_T to discharge from 1.5V to 0.5V. The equation for the off time is therefore:

$$t_{OFFsec} = \frac{C_T(\mu F)}{1.2} \quad (4)$$

IMAX Threshold

The second threshold is programmed by the voltage on IMAX (measured with respect to the CS+ pin). This controls the maximum current, I_{MAX}, that the UCC3919 will allow to flow into the load during the MOSFET on time. A resistive divider connected between IBIAS and CS+ generates the programming voltage. When the drop across the sense resistor reaches this voltage, a linear amplifier reduces the voltage on GATE to control the external MOSFET in a constant current mode.

APPLICATION INFORMATION (cont.)



t0: Normal condition - Output current is nominal, output voltage is at positive rail, VCC.

t1: Fault control reached - Output current rises above the programmed fault value, CT begins to charge with 35µA + IPL.

t2: Maximum current reached - Output current reaches the programmed maximum level and becomes a constant current with value IMAX.

t3: Fault occurs - CT has charged to 1.5V, fault output goes low, the FET turns off allowing no output current to flow, VOUT discharges to GND.

t4: Retry - CT has discharged to 0.5V, but fault current is still exceeded, CT begins charging again, FET is on, VOUT increases.

t3 to t5: Illustrates <3% duty cycle depending upon RPL selected.

t6 = t4

t7: Fault released, normal condition - return to normal operation of the circuit breaker.

Figure 1. Typical Timing Diagram

APPLICATION INFORMATION (cont.)

During this time CT is charging, as described above. If this condition lasts long enough for CT to charge to 1.5V, a fault will be declared and the MOSFET will be turned off. The IMAX current is calculated as follows:

$$I_{MAX} = \frac{V_{CS+} - V_{IMAX}}{R_{SENSE}} \quad (5)$$

Note that if the voltage on the IMAX pin is programmed to be less than 50mV below CS+, then the UC3919 will control the MOSFET in a constant current mode all the time. No fault will be declared and the MOSFET will remain on because IMAX is less than IFAULT.

Overload Threshold

There is a third threshold which, if exceeded, will declare a fault and shutdown the external MOSFET immediately, without waiting for CT to charge. This "Overload" threshold is 200mV greater than the IMAX threshold (again, this is with respect to CS+). This feature protects the circuit in the event that the external MOSFET is on, with a load current below IMAX, and a short is quickly applied across the output. This allows hot-swapping in cases where the UCC3919 is already powered up (on the backplane) and capacitors are added across the output bus. In this case, the load current could rise too quickly for the linear amplifier to reduce the voltage on GATE and limit the current to IMAX. If the overload threshold is reached, the MOSFET will be turned off quickly and a fault declared. A latch is set so that CT can be charged, guaranteeing that the MOSFET will remain off for the same period as defined above before retrying. The overload current is:

$$I_{OVERLOAD} = \frac{V_{CS+} - V_{IMAX} + 0.2}{R_{SENSE}} = I_{MAX} + \frac{0.2}{R_{SENSE}} \quad (6)$$

Note that IOVERLOAD may be much greater than IMAX, depending on the value of RSENSE.

Power Limiting

A power limiting feature is included which allows the power dissipated in the external MOSFET to be held relatively constant during a short, for different values of input voltage. This is accomplished by connecting a resistor from the output (source of the external MOSFET) to PL. When the output voltage drops due to a short or overload, an internal bias current is generated which is equal to:

$$I_{PL} \cong \frac{V_{IN} - V_{OUT}}{600 + R_{PL}} - \frac{0.1}{600}, \text{ for a shorted output:} \quad (7)$$

$$I_{PL} \cong \frac{V_{IN}}{600 + R_{PL}} - \frac{0.1}{600}$$

This current is used to help charge the timing capacitor in the event that the load current exceeds IFAULT. (A simplified schematic of the circuit internal to the UCC3919 is shown in Figure 2.) The result is that the on time of the MOSFET during current limit is reduced as the input voltage is increased. This reduces the effective duty cycle, holding the average power dissipated constant.

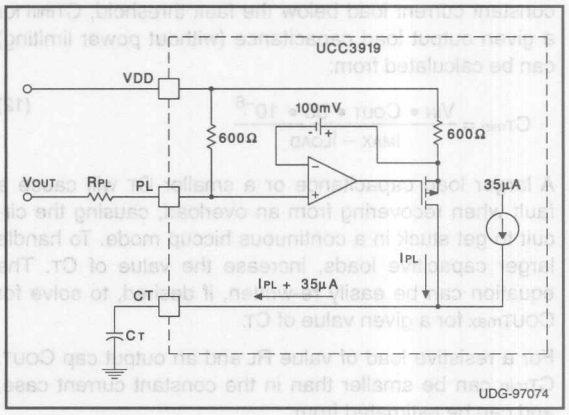


Figure 2. Power Limiting Circuit

It can be seen that power limiting will only occur when IPL is > 0 (it cannot be negative). For power limiting to begin to occur, RPL must be below a certain value for a given VIN, as approximated by:

$$R_{PL}(k\Omega) < \frac{V_{IN}}{0.17} \quad (8)$$

The on time using RPL is defined as:

$$t_{ON} = \frac{C_T}{I_{PL} + 35 \bullet 10^{-6}} \quad (9)$$

The graph in Figure 3 illustrates the effect of RPL on the average MOSFET power dissipation into a short. The equation for the average power dissipation during a short is:

$$P_{DISS} = \frac{I_{MAX} \bullet V_{IN} \bullet 1.2 \bullet 10^{-6}}{I_{PL} + 35 \bullet 10^{-6}}, \text{ or} \quad (10)$$

$$P_{DISS} = \frac{I_{MAX} \bullet V_{IN} \bullet t_{ON}}{t_{ON} + t_{OFF}}$$

If PL is left unconnected, the power limiting feature will not be exercised. In the retry mode, the duty cycle during a fault will be nominally 3.3%, independent of input voltage. The average power dissipation in the external MOSFET with a shorted output will be proportional to input voltage, as shown by the equation:

$$P_{DISS} = I_{MAX} \bullet V_{IN} \bullet 0.033 \quad (11)$$

APPLICATION INFORMATION (cont.)

Calculating C_{Tmin} for a Given Load Capacitance without Power Limiting

To guarantee recovery from an overload when operating in the retry mode, there is a maximum total output capacitance which can be charged for a given t_{ON} (fault time) before causing a fault. For a worst case situation of a constant current load below the fault threshold, C_{Tmin} for a given output load capacitance (without power limiting) can be calculated from:

$$C_{Tmin} = \frac{V_{IN} \bullet C_{OUT} \bullet 35 \bullet 10^{-6}}{I_{MAX} - I_{LOAD}} \quad (12)$$

A larger load capacitance or a smaller C_T will cause a fault when recovering from an overload, causing the circuit to get stuck in a continuous hiccup mode. To handle larger capacitive loads, increase the value of C_T. The equation can be easily re-written, if desired, to solve for C_{OUTmax} for a given value of C_T.

For a resistive load of value R_L and an output cap C_{OUT}, C_{Tmin} can be smaller than in the constant current case, and can be estimated from:

$$C_{Tmin} = \frac{-C_{OUT} \bullet R_L \bullet 1n\left(1 - \frac{V_{IN}}{I_{MAX} \bullet R_L}\right)}{28 \bullet 10^3} \quad (13)$$

Note that in the latch mode (or when first turning on in the retry mode), since the timing capacitor is not recovering from a previous fault, it is charging from 0V rather than 0.5V. This allows up to 50% more load capacitance without causing a fault.

Estimating C_{Tmin} When Using Power Limiting

If power limiting is used, the calculation of C_{Tmin} for a given C_{OUT} becomes considerably more complex, especially with a resistive load. This is because the C_T charge current becomes a function of V_{OUT}, which is changing with time. The amount of capacitance that can be charged (without causing a fault) when using power limiting will be significantly reduced for the same value C_T, due to the shorter ton time.

Equations will be given for making a conservative calculation of C_{Tmin} for constant current and resistive loads. To simplify the calculation, the following approximation will be made:

$$I_{PL} \cong \frac{V_{IN} - V_{OUT}}{R_{PL}} \quad (14)$$

This will yield a conservative value for C_{Tmin}, because the UCC3919's internal 600Ω resistor and 100mV offset (shown in Figure 2) are being ignored.

Constant Current Load

For a constant current load, the output capacitor will charge linearly. During that time:

$$I_{PLavg} \cong \frac{V_{IN}}{2 \bullet R_{PL}} \quad (15)$$

Modifying equation (12) yields:

$$C_{Tmin} \cong \frac{V_{IN} \bullet C_{OUT} \bullet \left(\frac{V_{IN}}{2 \bullet R_{PL}} + 35 \bullet 10^{-6}\right)}{I_{MAX} - I_{LOAD}} \quad (16)$$

Resistive Load

Determining $C_{T\,MIN}$ for a resistive load is more complex. First, the expression for the output voltage as a function of time is:

$$V_{OUT}(t) = I_{MAX} \bullet R_{LOAD} \bullet \left(1 - e^{\frac{-t}{R_{LOAD} \bullet C_{OUT}}}\right) \quad (17)$$

Solving for t when $V_{OUT} = V_{IN}$ yields:

$$t = -R_{LOAD} \bullet C_{OUT} \bullet Ln\left(1 - \left(\frac{V_{IN}}{I_{MAX} \bullet R_{LOAD}}\right)\right) \quad (18)$$

Assuming that the device is operating in the retry mode, where C_T is charging from 0.5V to just below 1.5V in time t, C_T is defined as:

$$C_T = \frac{I_{CT} \bullet dt}{dV} = I_{CT} \bullet dt \text{ where } I_{CT} = \left(I_{PL} + 35 \bullet 10^{-6}\right) \quad (19)$$

Substituting equation (14) and (19) yields:

$$C_{Tmin} = \left(\frac{V_{IN} - V_{OUT}}{R_{PL}} + 35 \bullet 10^{-6}\right) \bullet dt \quad (20)$$

Now substitute equation (17) for V_{OUT} and integrate (20) over time t. This yields the following expression for $C_{T\,MIN}$ for a resistive load with power limiting:

$$C_{Tmin} \cong t \bullet \left(35 \bullet 10^{-6} + \left(\frac{(V_{IN} - (I_{MAX} \bullet R_{LOAD})}{R_{PL}}\right)\right) + \left(\frac{V_{IN} \bullet R_{LOAD} \bullet C_{LOAD}}{R_{PL}}\right) \quad (21)$$

By substituting the value calculated for t in equation (18), C_{Tmin} is determined.

Example

The example in Figure 4 shows the UCC3919 in a typical application. A low value sense resistor and N-channel MOSFET minimize losses. With the values shown for R1,

APPLICATION INFORMATION (cont.)

R2, and RS, the overcurrent fault will be 5A nominal. Linear current limiting (I_{MAX}) will occur at 7.14A and the overload comparator will trip at 27A. The calculations are shown below.

$$I_{FAULT} = \frac{0.05}{R_S} = \frac{0.05}{0.01} = 5A \quad (22)$$

$$I_{MAX} = \frac{V_{CS+} - V_{IMAX}}{R_S} = \frac{1.5 \bullet R1}{(R1 + R2) \bullet R_S} = 7.14A \quad (23)$$

$$I_{OVERLOAD} = I_{MAX} + \left(\frac{0.2}{R_S}\right) = 7.14 + \left(\frac{0.2}{0.01}\right) = 27.14A \quad (24)$$

$$t_{OFFsec} = \frac{C_T\mu F}{1.2} = \frac{0.01}{1.2} = 8.33ms \quad (25)$$

With the value shown for R_{PL}:

$$I_{PL}\ (shorted) = \frac{V_{IN}}{R_{PL} + 600} - \frac{0.10}{600} \quad (26)$$

$$= \frac{5}{10{,}600} - \frac{0.10}{600} = 305\mu A$$

$$t_{ON}\ (shorted) = \frac{C_T}{I_{PL} + 35 \bullet 10^{-6}} \quad (27)$$

$$= \frac{0.01 \bullet 10^{-6}}{340 \bullet 10^{-6}} = 29\mu s$$

$$P_{DISS}\ (shorted) = \frac{I_{MAX} \bullet V_{IN} \bullet t_{ON}}{t_{ON} + t_{OFF}} \quad (28)$$

$$= \frac{7.14 \bullet 5 \bullet 29 \bullet 10^{-6}}{29 \bullet 10^{-6} + 8.33 \bullet 10^{-3}} = 0.12W$$

For a worst case 1Ω resistive load: $C_{OUTmax} \cong 39\mu F$.

For a worst case 5A constant current load: $C_{OUTmax} \cong 15\mu F$.

With L/R grounded, the part will operate in the retry or "hiccup" mode. The values shown for C_T and R_{PL} will yield a nominal duty cycle of 0.35% and an off time of 8.3ms. With a shorted output, the average steady state power dissipation in Q1 will be less than 200mW over the full input voltage range.

If power limiting is disabled by opening R_{PL}, then:

$$t_{FAULT} = t_{ONsec} = \frac{C_T(\mu F) \bullet 1}{35} = 287\mu s \quad (29)$$

$$P_{DISS}\ (shorted) = \frac{I_{MAX} \bullet V_{IN} \bullet t_{ON}}{t_{ON} + t_{OFF}} \quad (30)$$

$$= \frac{7.14 \bullet 5 \bullet 287 \bullet 10^{-6}}{287 \bullet 10^{-6} + 8.33 \bullet 10^{-3}}$$

$$= 1.2W\ (with\ V_{IN} = 5V)$$

For a worst case 1Ω resistive load: $C_{OUTmax} \cong 240\mu F$.

For a worst case 5A constant current load: $C_{OUTmax} \cong 120\mu F$.

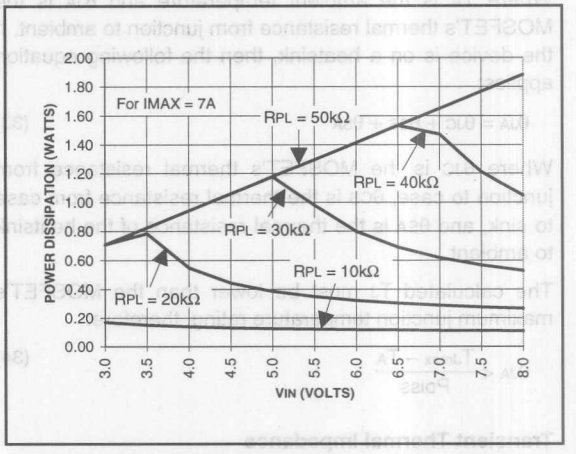


Figure 3. MOSFET Average Short Circuit Power Dissipation vs V_{IN} for Values of R_{PL}

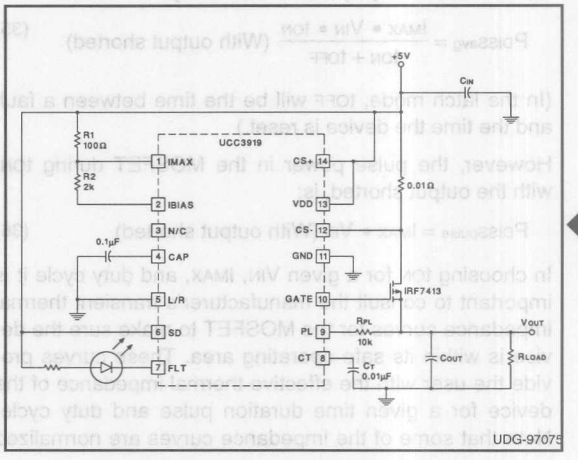


Figure 4. Application Circuit

THERMAL CONSIDERATIONS

Stead State Conditions

In normal operation, with a steady state load current below I_{FAULT}, the power dissipation in the external MOSFET will be:

$$P_{DISS} = RDS_{ON} \bullet I_{LOAD}^2 \quad (31)$$

THERMAL CONSIDERATIONS (cont.)

The junction temperature of the MOSFET can be calculated from:

$$T_J = T_A + (P_{DISS} \bullet \theta_{JA}) \quad (32)$$

Where T_A is the ambient temperature and θ_{JA} is the MOSFET's thermal resistance from junction to ambient. If the device is on a heatsink, then the following equation applies:

$$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA} \quad (33)$$

Where θ_{JC} is the MOSFET's thermal resistance from junction to case, θ_{CS} is the thermal resistance from case to sink, and θ_{SA} is the thermal resistance of the heatsink to ambient.

The calculated T_J must be lower than the MOSFET's maximum junction temperature rating, therefore:

$$\theta_{JA} < \frac{T_{Jmax} - T_A}{P_{DISS}} \quad (34)$$

Transient Thermal Impedance

During a fault condition in the retry mode, the average MOSFET power dissipation will generally be quite low due to the low duty cycle, as defined by:

$$P_{DISSavg} = \frac{I_{MAX} \bullet V_{IN} \bullet t_{ON}}{t_{ON} + t_{OFF}} \text{ (With output shorted)} \quad (35)$$

(In the latch mode, t_{OFF} will be the time between a fault and the time the device is reset.)

However, the pulse power in the MOSFET during t_{ON}, with the output shorted, is:

$$P_{DISSpulse} = I_{MAX} \bullet V_{IN} \text{ (With output shorted)} \quad (36)$$

In choosing t_{ON} for a given V_{IN}, I_{MAX}, and duty cycle it is important to consult the manufacturer's transient thermal impedance curves for the MOSFET to make sure the device is within its safe operating area. These curves provide the user with the effective thermal impedance of the device for a given time duration pulse and duty cycle. Note that some of the impedance curves are normalized to one, in which case the transient impedance values must be multiplied by the DC (steady state) thermal resistance, θ_{JC}.

For duty cycles not shown in the manufacturer's curves, the transient thermal impedance for any duty cycle and ton time (given a square pulse) can be estimated from [1]:

$$\theta_{JCtrans} = (D \bullet \theta_{JC}) + (1 - D) \bullet \theta_{SP} \quad (37)$$

Where D is the duty cycle

$$\frac{t_{ON}}{t_{ON} + t_{OFF}},$$

and θ_{SP} is the single pulse thermal impedance given in the transient thermal impedance curves for the time duration of interest (t_{ON}). Note that these are absolute numbers, not normalized. If the given single pulse impedance is normalized, it must first be multiplied by θ_{JC} before using in the equation above.

This effective transient thermal impedance, when multiplied by the pulse power, will give the transient temperature rise of the die. To keep the junction temperature below the maximum rating, the following must be true:

$$\theta_{JCtrans} < \frac{T_{Jmax} - T_C}{P_{DISSpulse}} \quad (38)$$

If necessary, the junction temperature rise can be reduced by reducing ton (using a smaller value for C_T), or by reducing the duty cycle using the power limiting feature already discussed. Note that in either case, the amount of load capacitance, C_{OUT}, that can be charged before causing a fault, will also be reduced.

References

[1] International Rectifier, HEXFET Power MOSFET Designer's Manual, Application Note 949B, "Current Ratings, Safe operating Area, and High Frequency Switching Performance of Power HEXFET's", pp. 1553-1565, September 1993.

SAFETY RECOMMENDATIONS

Although the UCC3919 is designed to provide system protection for all fault conditions, all integrated circuits can ultimately fail short. for this reason, if the UCC3919 is intended for use in safety critical applications where UL or some other safety rating is required, a redundant safety device such as a fuse should be placed in series with the device. The UCC3919 will prevent the fuse from blowing for virtually all fault conditions, increasing system reliability and reducing maintenance cost, in addition t providing the hot swap benefits of the device.

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–3V to –15V Hot Swap Power Manager

FEATURES

- Integrated 0.1Ω Power MOSFET
- –3V to –15V Operation
- Programmable Electronic Circuit Breaker
- Digital Programmable Current Limit from 0A to 3A
- Programmable Maximum Output Current from 0A to 4A
- Programmable On Time
- Fixed 2% Fault Duty Cycle
- Thermal Shutdown
- Fault Output Indicator
- Power SOIC Package

DESCRIPTION

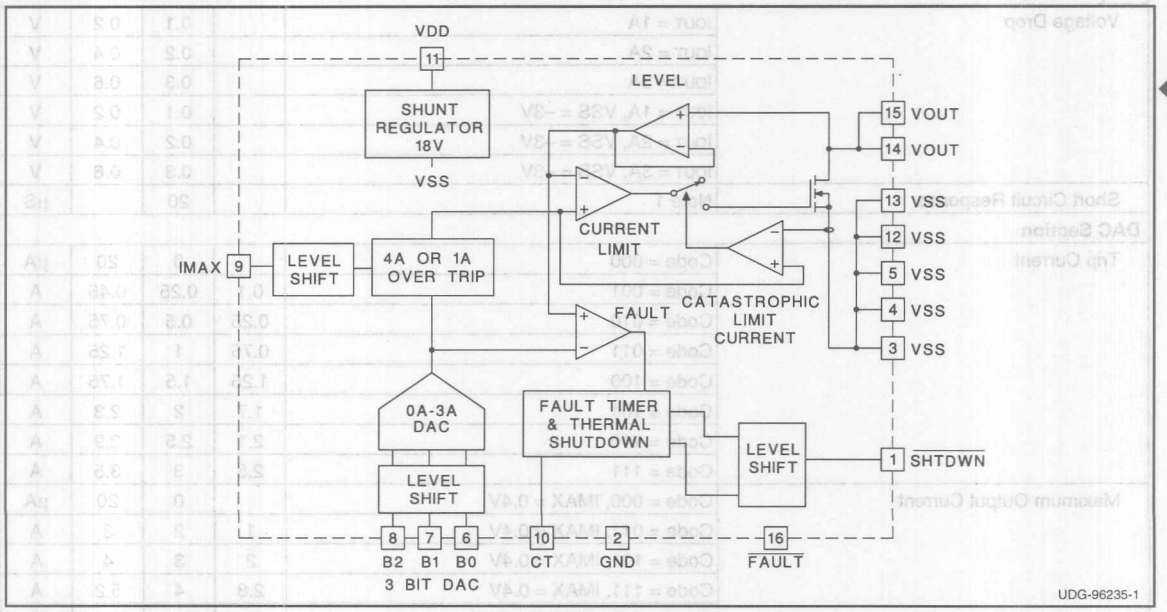
The UCC3920 Low RDSon Hot Swap Power Manager provides complete power management, hot swap capability, and circuit breaker functions. The only component needed to operate the device, other than supply bypassing, is the fault timing capacitor, CT. All control and housekeeping functions are integrated and externally programmable. These include the fault current level, maximum output sourcing current, maximum fault time, and start up delay. In the event of a constant fault, the internal fixed 2% duty cycle ratio limits the average output power.

The internal 3 bit DAC allows programming of the fault level current from 0mA to 500mA with 250mA resolution, and from 500mA to 3A with 500mA resolution. The IMAX control pin sets the maximum sourcing current to 1A above the fault level when driven low, and to a full 4A when driven high for applications which require fast output charging.

When the output current is below the fault level, the output MOSFET is switched on with a nominal resistance of 0.1Ω. When the output current exceeds the fault level or the maximum sourcing level, the output remains on, but the fault timer starts charging CT. Once CT charges to a preset threshold, the switch is turned off, and remains off for 50 times the programmed fault time. When the output current reaches the maximum sourcing level, the MOSFET transitions form a switch to a constant current source, regulating the output current at a constant level.

Other features include an Open Drain Fault Output Indicator, Thermal Shutdown, Undervoltage Lockout, –3V to –15V operation, and a low thermal resistance Small Outline Power Package. All level shifting is done internally, which means that the DAC, IMAX and Shutdown Inputs can be driven form the logic supply. The fault output is also referenced to the logic GND, so this can easily interface back to the logic supply.

BLOCK DIAGRAM



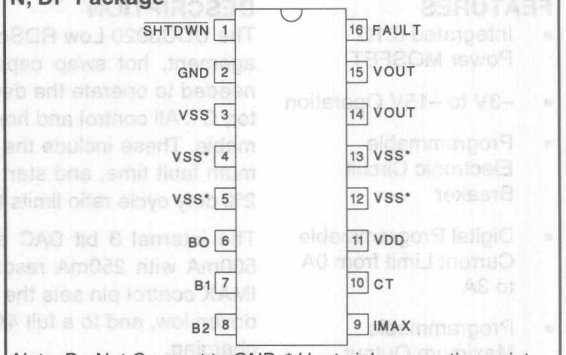
ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage
(VDD) . . . . . +7V
(VSS) . . . . . –15V
Maximum Differential Suppy (VDD - VSS) 18V
Maximum Supply Shunt Current 20mA
Fault Output Sink Current 20mA
Fault Output Voltage 7V
Output Current (DC) . . . . . Internally Limited
TTL Input Voltage . . . . . -0.3 to 7V
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

Currents are positive into, negative out of the specified terminal. Pulsed is defined as a less than 10% duty cycle with a maximum duration of 500µS. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

DIL-16, SOIC-16 (Top View)
N, DP Package



*Note: Do Not Connect to GND. * Heat sink connection points - electronically connected to Vss.*
For N Package, pins 4, 12, and 13 are N/C.

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specificaiton apply for T_A = 0°C to 70°C for the UCC3920 and T_A = –40°C to 85°C for the UCC2920, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Section					
Voltage Input Range - VDD	Minimum < VDD < Maximum (Note 3)	3	5	5.5	V
Voltage Input Range - VSS	Minimum < VSS < Maximum	–13.2	–12	–3	V
VSS Supply Current			0.5	2	mA
VDD Supply Current			0.5	2	mA
Sleep Mode Current	Shutdown = 0.2V		0.5	2	mA
Shunt Clamp Voltage - (VDD - VSS)	I = 2mA to 10mA, Note 3	16.2	18	20	V
Output Section					
Voltage Drop	I_{OUT} = 1A		0.1	0.2	V
	I_{OUT} = 2A		0.2	0.4	V
	I_{OUT} = 3A		0.3	0.6	V
	I_{OUT} = 1A, VSS = –3V		0.1	0.2	V
	I_{OUT} = 2A, VSS = –3V		0.2	0.4	V
	I_{OUT} = 3A, VSS = –3V		0.3	0.6	V
Short Circuit Response	Note 1		20		µS
DAC Section					
Trip Current	Code = 000		0	20	µA
	Code = 001	0.1	0.25	0.45	A
	Code = 010	0.25	0.5	0.75	A
	Code = 011	0.75	1	1.25	A
	Code = 100	1.25	1.5	1.75	A
	Code = 101	1.7	2	2.3	A
	Code = 110	2.1	2.5	2.9	A
	Code = 111	2.5	3	3.5	A
Maximum Output Current	Code = 000, IMAX = 0.4V		0	20	µA
	Code = 011, IMAX = 0.4V	1	2	3	A
	Code = 101, IMAX = 0.4V	2	3	4	A
	Code = 111, IMAX = 0.4V	2.8	4	5.2	A
	IMAX = 2.4V, All Codes	3	4	5.2	A

ELECTRICAL CHARACTERISTICS (cont.) Unless otherwise stated, these specificaiton apply for T_A = 0°C to 70°C for the UCC3920 and T_A = –40°C to 85°C for the UCC2920, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Fault Section					
CT Charge Current	V_{CT} = 1V, Note 2	–50	–36	–22	µA
CT Discharge Current	V_{CT} = 1V, Note 2	0.36	0.6	1	µA
Output Duty Cycle	VOUT = 0V	1	2	4	%
CT Fault Threshold	Note 2	1.25	1.5	1.75	V
CT Reset Threshold	Note 2	0.25	0.5	0.75	V
Shutdown Section					
Shutdown Threshold		1.1	1.5	1.9	V
Shutdown Hysterisis			50		mV
Open Drain Fault Output					
High Level Output Current				1	µA
Low Level Output Voltage	IOUT = 2mA			0.4	V
	IOUT = 10mA			0.9	V
Logic Input DC Characteristics					
Input Voltage High		2			V
Input Voltage Low				0.8	V
Input High Current	VIH = 2.4V		3	10	µA
Input Low Current	VIL = 0.4V			1	µA

Note 1: Guaranteed by design. Not 100% tested in production.
Note 2: Voltages measured with respect to VSS.
Note 3: An external resistor in series with VDD could be used to limit the current to 10mA if an input voltage higher than 15V is desired.

PIN DESCRIPTIONS

BO - B2: These pins provide a digital input to the DAC. They can be used to provide a digital soft start, adaptive current limiting, or be strapped for static applications.

CT: A capacitor connected to CT sets the maximum fault time. The maximum must be more than the time to charge external load capacitance. The maximum fault time is defined as $T_{FAULT} = 28 \bullet 10^3 \bullet CT$. Once the fault time is reached the output will shutdown for a time given by: $TSD = 1.67 \bullet 10^6 \bullet CT$, this equates to a 2% duty cycle.

FAULT: Open drain output which, pulls low, from VDD to GND, upon any condition which causes the output to open: Fault, Thermal Shutdown, or Shutdown.

GND: Reference return for VDD and VSS (VIN). This serves as the reference point for digital signals.

IMAX: When this pin is at a logic low the linear output current will always be 1A above the programmed trip level, and with a logic high the linear current will always be a constant 4A for applications which require fast charging of load capacitance.

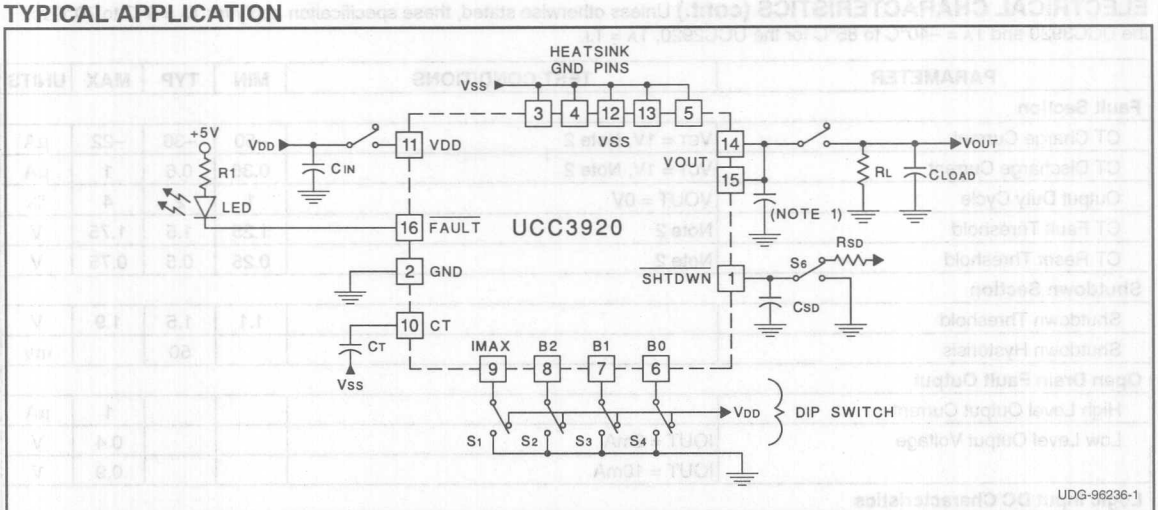
$\overline{\text{SHTDWN}}$: When this pin is brought down low the IC is put into a sleep mode.

VDD: Positive input voltage to the circuit breaker. The input voltage range is 3V to 5.5V. If the total voltage excursion, VDD - VSS could be 15V or greater, VDD should have an external limiting resistor in series with it.

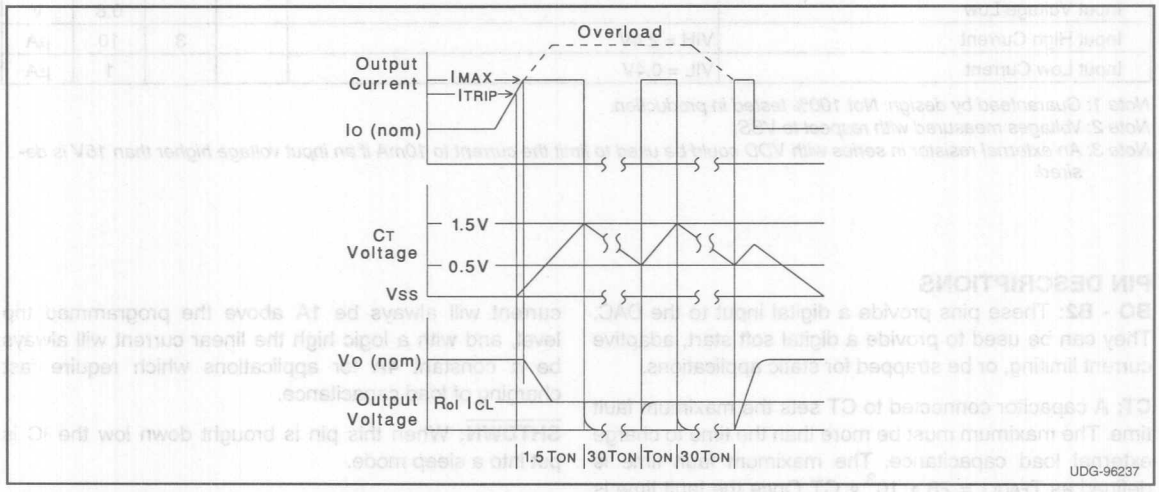
VSS: The input voltage to the circuit breaker. The recommended voltage range is –3.3V to –15V.

VOUT: Output voltage for the circuit breaker. When switched the output voltage will be approximately VIN + 0.1Ω • IOUT.

TYPICAL APPLICATION



Note 1: Most applications will require a capacitor mounted between VOUT and GND at the IC pins to cancel out stray inductance.



Estimating Maximum Load Capacitance

For power management applications, the rate at which the total output capacitance can be charged depends on the maximum output current available and the nature of the load. For a constant-current current-limited circuit, the output will rise if the load asks for less than the maximum available short-circuit current.

To guarantee duty-cycle recovery of the current-limited power manager from a short-circuited load condition, there is a maximum total output capacitance which can be charged for a given unit ON time (Fault time). The design value of ON or Fault time can be adjusted by changing the timing capacitor C_T.

For a worst-case constant-current load of value just less than the trip limit; $C_{OUT(max)}$ can be estimated from:

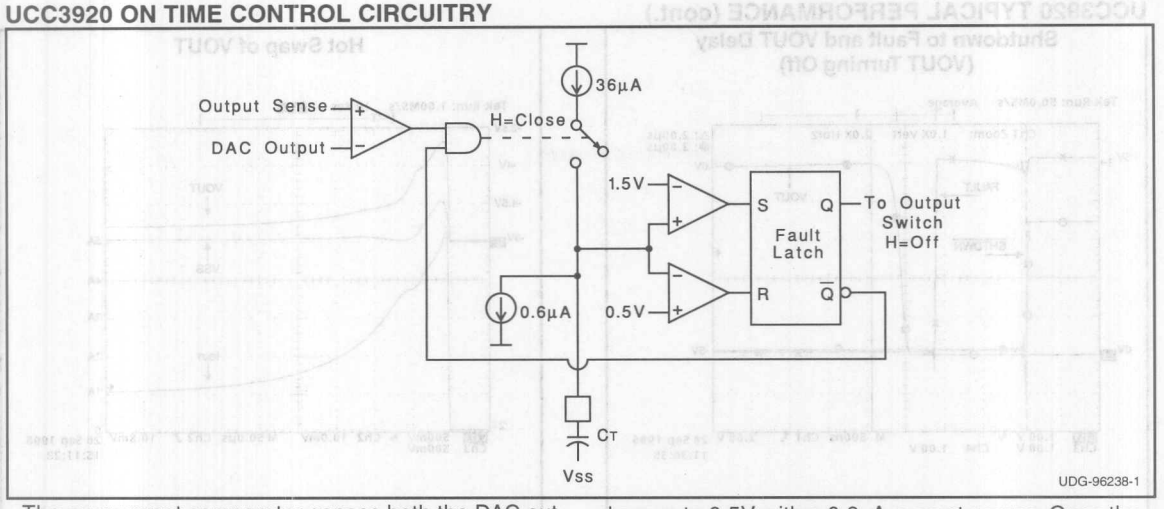
$$C_{OUT(max)} \approx (I_{MAX} - I_{LOAD}) \bullet \left(\frac{28 \bullet 10^3 \bullet C_T}{V_{OUT}} \right)$$

Where V_{OUT} is the output voltage.

For a resistive load of value RI, the value of $C_{OUT(max)}$ can be estimated from:

$$C_{OUT(max)} \approx \left(\frac{28 \bullet 10^3 \bullet C_T}{R_L \bullet \ln \left[\frac{1}{1 - \frac{V_{OUT}}{I_{MAX} \bullet R_L}} \right]} \right)$$

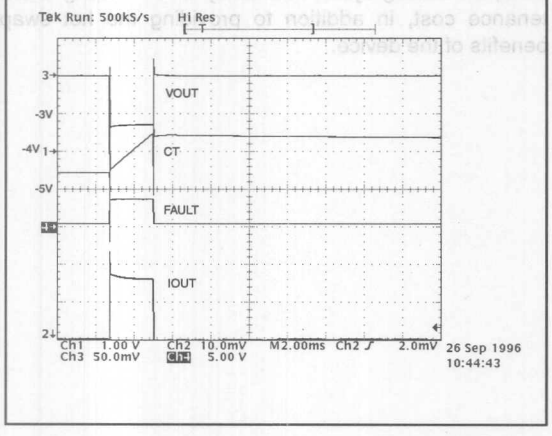
UCC3920 ON TIME CONTROL CIRCUITRY



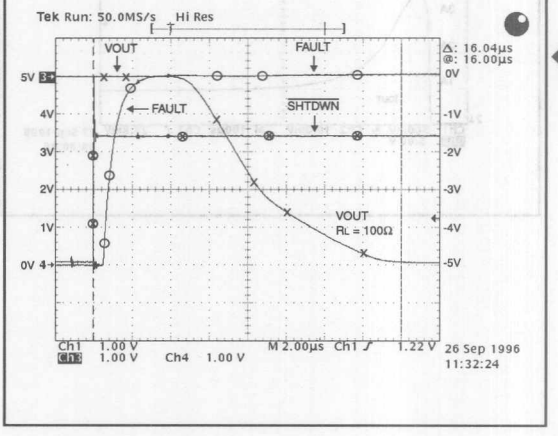
The overcurrent comparator senses both the DAC output and a representation of the output current. When the output current exceeds the programmed level the timing capacitor C_T charges with 36µA of current. If the fault occurs for the time it takes for C_T to charge up to 1.5V, the fault latch is set and the output switch is opened. The output remains opened until C_T discharges to 0.5V with a 0.6µA current source. Once the 0.5V is reached the output is enabled and will either appear as a switch, if the fault is removed, or a current source if the fault remains. If the over current condition is still present then C_T will begin charging, starting the cycle over, resulting in approximately a 2% duty cycle.

UCC3920 TYPICAL PERFORMANCE

IFAULT Response

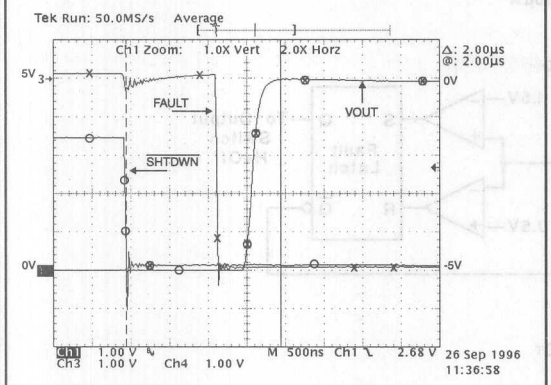


Shutdown to VOUT Delay (VOUT Turning On)

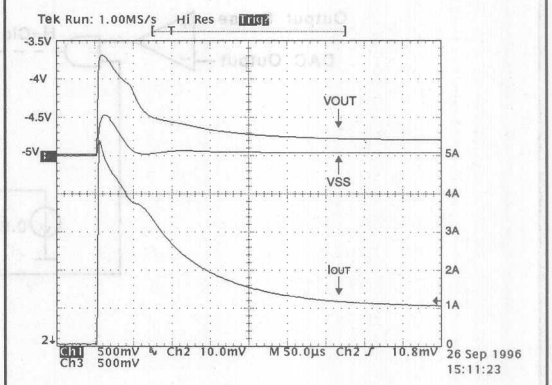


UCC3920 TYPICAL PERFORMANCE (cont.)

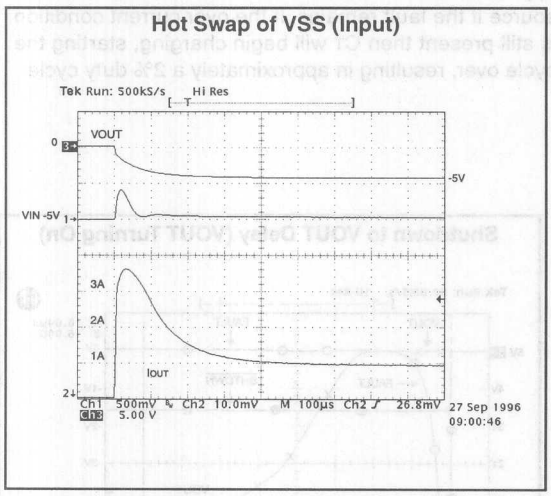
Shutdown to Fault and VOUT Delay (VOUT Turning Off)



Hot Swap of VOUT



Hot Swap of VSS (Input)



SAFETY RECOMMENDATION

Although the UCC3920 is designed to provide system protection for all fault conditions, all integrated circuits can ultimately fail short. For this reason, if the UCC3920 is intended for use in safety critical applications where UL or some other safety rating is required, a redundant safety device such as a fuse should be placed in series with the device. The UCC3920 will prevent the fuse from blowing for virtually all fault conditions, increasing system reliability and reducing maintenance cost, in addition to providing the hot swap benefits of the device.

UNITRODE CORPORATION
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TEL. (603) 424-2410 • FAX (603) 424-3460

Latchable Negative Floating Hot Swap Power Manager

PRELIMINARY

FEATURES

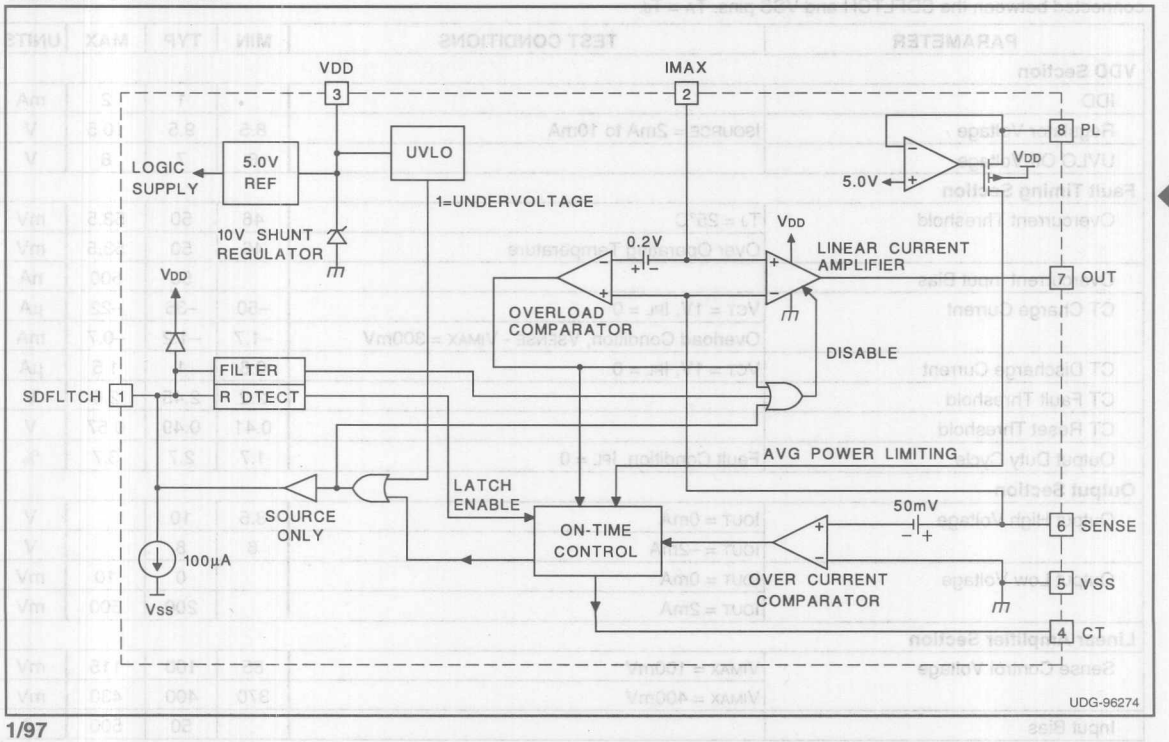
- Precision Fault Threshold
- Programmable: Average Power Limiting, Linear Current Control, Overcurrent Limit and Fault Time
- Fault Output Indication Signal
- Automatic Retry Mode or Latched Operation Mode
- Shutdown Control
- Undervoltage Lockout
- 250µs Glitch Filter on the SDFLTCH pin
- 8-Pin DIL and SOIC

DESCRIPTION

The UCC3921 family of negative floating hot swap power managers provides complete power management, hot swap, and fault handling capability. The IC is referenced to the negative input voltage and is powered through an external resistor connected to ground, which is essentially a current drive as opposed to the traditional voltage drive. The onboard 10V shunt regulator protects the IC from excess voltage and serves as a reference for programming the maximum allowable output sourcing current during a fault. All control and housekeeping functions are integrated, and externally programmable. These include the fault current level, maximum output sourcing current, maximum fault time, selection of Retry or Latched mode, soft start time, and average power limiting. In the event of a constant fault, the internal timer will limit the on time from less than 0.1% to a maximum of 3% duty cycle. The duty cycle modulation depends on the current into PL, which is a function of the voltage across the FET, thus limiting average power dissipation in the FET. The fault level is fixed at 50mV across the current sense amplifier to minimize total dropout. The fault current level is set with an external current sense resistor, while the maximum allowable sourcing current is programmed with a voltage divider from VDD to generate a fixed voltage on IMAX. The current level, when the output acts as a current source, is equal to VIMAX/RSENSE. If desired, a controlled current start up can be programmed with a capacitor on IMAX.

Continued

BLOCK DIAGRAM



1/97

DESCRIPTION (cont.)

When the output current is below the fault level, the output device is switched on. When the output current exceeds the fault level, but is less than the maximum sourcing level programmed by IMAX, the output remains switched on, and the fault timer starts charging CT. Once CT charges to 2.5V, the output device is turned off and performs a retry some time later (provided that the selected mode of operation is Automatic Retry Mode). When the output current reaches the maximum sourcing current level, the output acts as a current source, limiting the output current to the set value defined by IMAX.

Other features of the UCC3921 include undervoltage lockout, 8-pin Small Outline (SOIC) and Dual-In-Line (DIL) packages, and a Latched Operation Mode option, in which the output is latched off once CT charges to 2.5V and stays off until either SDFLTCH is toggled (for greater than 1ms) or the IC is powered down and then back up.

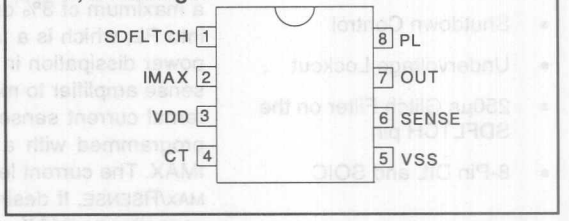
ABSOLUTE MAXIMUM RATINGS

IVDD 50mA
SDFLTCH Current 10mA
PL Current 10mA
IMAX Input Voltage. . . . . VDD
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

All voltages are with respect to VSS (the most negative voltage). Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

DIL-8 , SOIC-8 (Top View)
N or J, D Packages



ELECTRICAL CHARACTERISTICS Unless otherwise specified, TA = 0°C to 70°C for the UCC3921 and –40°C to 85°C for the UCC2921, and –55°C to 125°C for the UCC1921; IVDD = 2mA, CT = 1nF (the minimum allowable value), there is no resistor connected between the SDFLTCH and VSS pins. TA = TJ.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VDD Section					
IDD			1	2	mA
Regulator Voltage	ISOURCE = 2mA to 10mA	8.5	9.5	10.5	V
UVLO Off Voltage		6	7	8	V
Fault Timing Section					
Overcurrent Threshold	TJ = 25°C	46	50	53.5	mV
	Over Operating Temperature	46	50	53.5	mV
Overcurrent Input Bias			50	500	nA
CT Charge Current	VCT = 1V, IPL = 0	–50	–36	–22	µA
	Overload Condition, VSENSE - VIMAX = 300mV	–1.7	–1.2	–0.7	mA
CT Discharge Current	VCT = 1V, IPL = 0	0.6	1	1.5	µA
CT Fault Threshold		2.2	2.45	2.6	V
CT Reset Threshold		0.41	0.49	0.57	V
Output Duty Cycle	Fault Condition, IPL = 0	1.7	2.7	3.7	%
Output Section					
Output High Voltage	IOUT = 0mA	8.5	10		V
	IOUT = –2mA	6	8		V
Output Low Voltage	IOUT = 0mA		0	10	mV
	IOUT = 2mA		200	500	mV
Linear Amplifier Section					
Sense Control Voltage	VIMAX = 100mV	85	100	115	mV
	VIMAX = 400mV	370	400	430	mV
Input Bias			50	500	nA

ELECTRICAL CHARACTERISTICS (cont.) Unless otherwise specified, T_A = 0°C to 70°C for the UCC3921 and –40°C to 85°C for the UCC2921, and –55°C to 125°C for the UCC1921; I_{VDD} = 2mA, C_T = 1nF (the minimum allowable value), there is no resistor connected between the SDFLTCH and VSS pins. $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Power Limiting Section					
V_{SENSE} Regulator Voltage	I_{PL} = 64µA	4.35	4.85	5.35	V
Duty Cycle Control	I_{PL} = 64µA	0.6	1.2	1.7	%
	I_{PL} = 1mA	0.045	0.1	0.17	%
Overload Section					
Delay to Output	Note 1		50		ns
Output Sink Current	$V_{SENSE} - V_{IMAX}$ = 300mV	40	100		mA
Threshold	Relative to IMAX	140	200	260	mV
Shutdown/Fault/Latch Section					
Shutdown Threshold		3	5	VDD+1	V
Input Current	$V_{SDFLTCH}$ = 5V	50	110	250	µA
Filter Delay Time (Delay to Output)		250	500	1000	µs
Fault Output High		6	9.5		V
	$I_{SDFLTCH}$ = –100µA	5	8.5		V
Fault Output Low			0	10	mV
Output Duty Cycle	Fault Condition, I_{PL} = 0	1.7	2.7	3.7	%
	$I_{SDFLTCH}$ = –100µA, Fault Condition, I_{PL} = 0			0	%
Delay to Output	Note 1		150	300	ns

Note 1: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

CT: A capacitor is connected to this pin in order to set the maximum fault time. The maximum fault time must be more than the time to charge external load capacitance. The maximum fault time is defined as:

$$T_{FAULT} = \frac{2 \bullet C_T}{I_{CH}}$$

where I_{CH} = 36µA + I_{PL}, and I_{PL} is the current into the power limit pin. Once the maximum fault time is reached the output will shutdown for a time given by:

$$T_{SD} = 2 \bullet 10^6 \bullet C_T$$

IMAX: This pin programs the maximum allowable sourcing current. Since VDD is a regulated voltage, a voltage divider can be derived from VDD to generate the program level for IMAX. The current level at which the output appears as a current source is equal to the voltage on IMAX over the current sense resistor. If desired, a controlled current start up can be programmed with a capacitor on IMAX, and a programmed start delay can be achieved by driving the shutdown with an open collector/drain device into an RC network.

OUT: This pin provides gate output drive to the MOSFET pass element.

PL: This feature ensures that the average MOSFET power dissipation is controlled. A resistor is connected from this pin to the drain of the NMOS pass element. When the voltage across the NMOS exceeds 5V, current will flow into the PL pin which adds to the fault timer charge current, reducing the duty cycle from the 3% level. When I_{PL}>>36µA, then the average MOSFET power dissipation is given by:

$$P_{MOSFET\ AVG} = IMAX \bullet 1 \bullet 10^6 \bullet R_{PL}$$

SENSE: Input voltage from the current sense resistor. When there is greater than 50mV across this pin with respect to VSS, then a fault is sensed, and C_T starts to charge.

SDFLTCH: This pin provides fault output indication, shutdown control, and operating mode selection. Interface into and out of this pin is usually performed through level shift transistors. When open, and under a non-fault condition, this pin pulls to a low state. When a fault is detected by the fault timer, or undervoltage lockout, this pin will drive to a high state, indicating the NMOS pass element is OFF. When > 250µA is sourced into this pin for > 1ms, it drives high causing the output to disable the NMOS pass device.

If an 5k < R_{LATCH} < 250kΩ resistor is placed from this pin to VSS, then the latched operating mode will be invoked. Upon the occurrence of a fault, under the latched mode of operation, once the C_T capacitor charges up to 2.5V

PIN DESCRIPTION (cont.)

the NMOS pass element latches off. A retry will not periodically occur. To reset the latched off device, SDFLTCH must be toggled high for a duration greater than 1ms or the IC is powered down and then up.

VDD: Current driven with a resistor to a voltage at least 10V more positive than VSS. Typically a resistor is connected to ground. The 10V shunt regulator clamps VDD at 10V above VSS, and is also used as an output reference to program the maximum allowable sourcing current.

VSS: Ground reference for the IC and the most negative voltage available.

APPLICATION INFORMATION

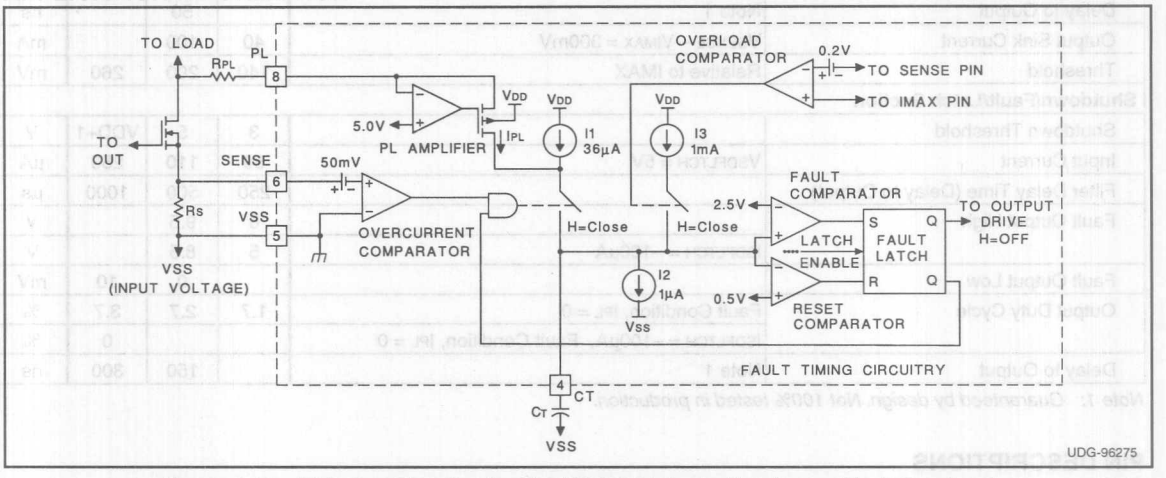


Figure 1. Fault Timing Circuitry for the UCC3921, Including Power Limit Overload

Figure 1 shows the detailed circuitry for the fault timing function of the UCC3921. For the time being, we will discuss a typical fault mode, therefore, the overload comparator, and current source I3 does not work into the operation. Once the voltage across the current sense resistor, RS, exceeds 50mV, a fault has occurred. This causes the timing capacitor to charge with a combination of 36µA plus the current from the power limiting amplifier. The PL amplifier is designed to only source current into the CT pin and to begin sourcing current once the voltage across the output FET exceeds 5V. The current IPL is related to the voltage across the FET with the following expression:

$$I_{PL} = \frac{V_{FET} - 5V}{R_{PL}}$$

where VFET is the voltage across the NMOS pass device. Later it will be shown how this feature will limit average power dissipation in the pass device. Note that under a condition where the output current is more than the fault level, but less than the max level, VOUT ~ VSS (input voltage), IPL = 0, the CT charging current is 36µA. During a fault, CT will charge at a rate determined by the internal charging current and the external timing capacitor. Once CT charges to 2.5V, the fault comparator switches and sets the fault latch. Setting of the fault latch causes both the output to switch off and the charging switch to open. CT must now discharge with the 1µA current source, I2, until 0.5V is reached. Once the voltage at CT reaches 0.5V, the fault latch resets, which re-enables the output and allows the fault circuitry to regain control of the charging switch. If a fault is still present, the fault comparator will close the charging switch causing the cycle to repeat. Under a constant fault, the duty cycle is given by:

$$\text{Duty Cycle} = \frac{1\mu A}{I_{PL} + 36\mu A}$$

Average power dissipation in the pass element is given by:

$$P_{FET\,AVG} = V_{FET} \bullet IMAX \bullet \frac{1\mu A}{I_{PL} + 36\mu A}$$

Where VFET>>5V IPL can be approximated as:

$$\frac{V_{FET}}{R_{PL}}$$

and where IPL>>36µA, the duty cycle can be approximated as :

APPLICATION INFORMATION (cont.)

$$\frac{1\mu A \bullet R_{PL}}{V_{FET}}$$

Therefore, the maximum average power dissipation in the MOSFET can be approximated by:

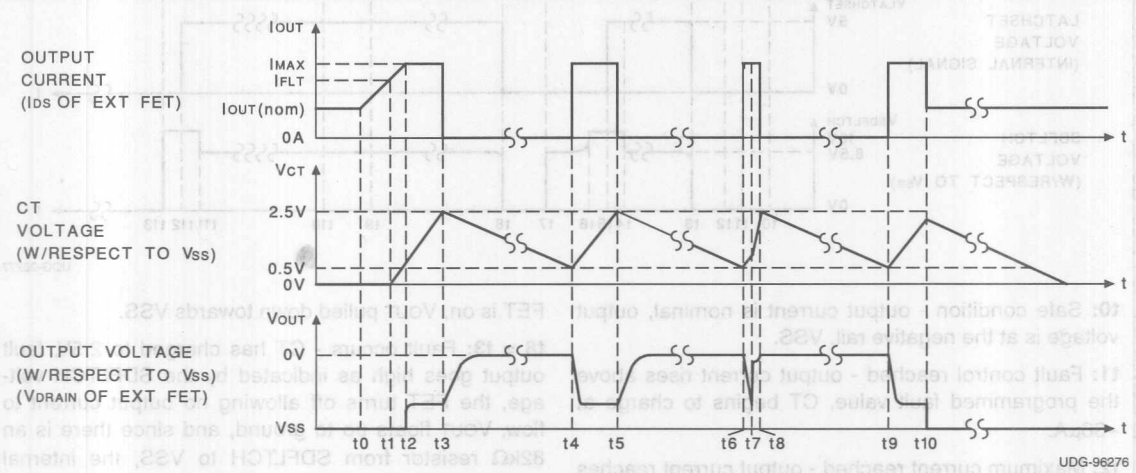
$$P_{FET\,AVG} = V_{FET} \bullet IMAX \bullet \frac{1\mu A \bullet R_{PL}}{V_{FET}}$$

$$= IMAX \bullet 1\mu A \bullet R_{PL}$$

Notice that in the approximation, V_{FET} cancels, thereby limiting the average power dissipation in the NMOS pass element.

Overload Comparator

The linear amplifier in the UCC3921 ensures that the output NMOS does not pass more than IMAX (which is VIMAX/RS). In the event the output current exceeds the programmed IMAX by 0.2V/Rs, which can only occur if the output FET is not responding to a command from the IC, CT will begin charging with I3, 1mA, and continue to charge to approximately 8V. This allows a constant fault to show up on the SDFLTCH pin,and also since the voltage on CT will only charge past 2.5V in an overload fault mode, it can be used for detection of output FET failure or to build in redundancy in the system.



t0: Safe condition - output current is nominal, output voltage is at the negative rail, VSS.

t1: Fault control reached - output current rises above the programmed fault value, CT begins to charge at ~36µA.

t2: Maximum current reached - output current reaches the programmed maximum level and becomes a constant current with value IMAX.

t3: Fault occurs - CT has charged to 2.5V, fault output goes high, the FET turns off allowing no output current to flow, VOUT floats up to ground.

t4: Retry - CT has discharged to 0.5V, but fault current is still exceeded, CT begins charging again, FET is on, VOUT pulled down towards VSS.

t5 = t3: Illustrates 3% duty cycle.

t6 = t4: Retry - CT has discharged to 0.5V, but fault is still exceeded, CT begins charging again, FET is on, VOUT pulled down towards VSS.

t7: Output short circuit - if VOUT is short circuited to ground, CT charges at a higher rate depending upon the values for VSS and RPL.

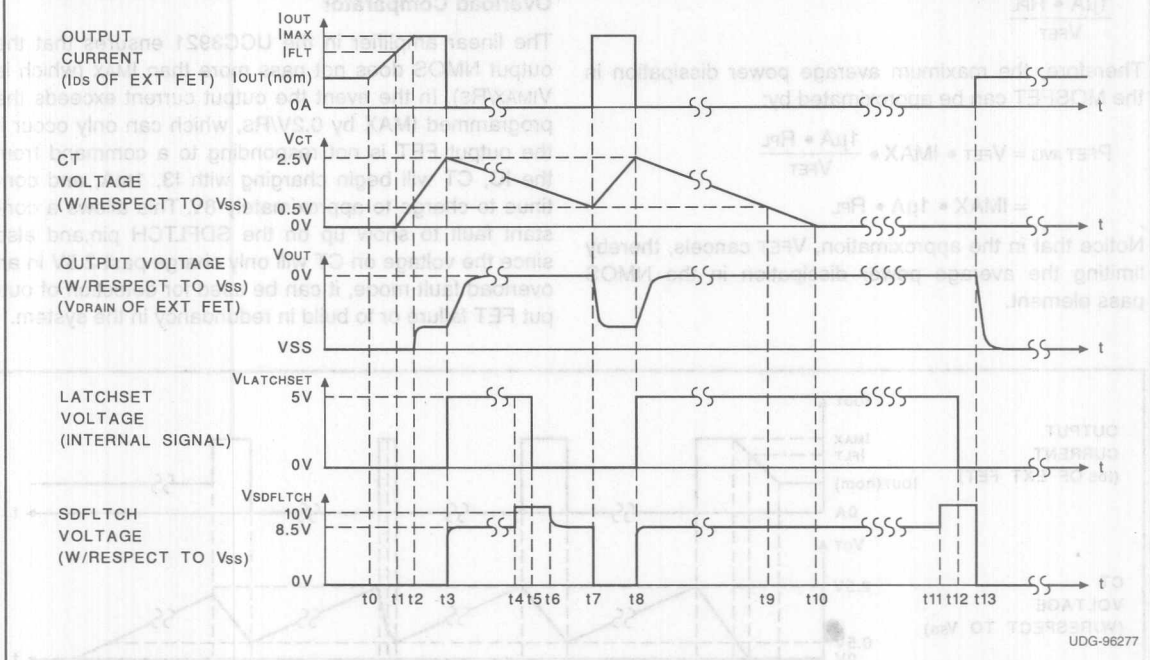
t8: Fault occurs - output is still short circuited, but the occurrence of a fault turns the FET off so no current is conducted.

t9 = t4: output short circuit released, still in fault mode.

t10 = t0: fault released, safe condition - return to normal operation of the hot swap power manager.

Figure 2. Retry Operation Mode

APPLICATION INFORMATION (cont.)



t0: Safe condition - output current is nominal, output voltage is at the negative rail, VSS.

t1: Fault control reached - output current rises above the programmed fault value, CT begins to charge at ~36µA.

t2: Maximum current reached - output current reaches the programmed maximum level and becomes a constant current with value IMAX.

t3: Fault occurs - CT has charged to 2.5V, fault output goes high as indicated by the SDFLTCH voltage. The FET turns off allowing no output current to flow, VOUT floats up to ground, and since there is an 82kΩ resistor from the SDFLTCH pin to VSS, the internal latchset signal goes high.

t4: Since the user does not want the chip to LATCH off during this cycle, he toggles SDFLTCH high for greater than 1ms {t6 - t4 > 1ms}.

t5: The latchset signal is reset.

t6: Forcing of SDFLTCH is released after having been applied for > 1ms.

t7: Retry (since the latchset signal has been reset to its' low state) - CT has discharged to 0.5V, but fault current is still exceeded, CT begins charging again, FET is on, VOUT pulled down towards VSS.

t8 = t3: Fault occurs - CT has charged to 2.5V, fault output goes high as indicated by the SDFLTCH voltage, the FET turns off allowing no output current to flow, VOUT floats up to ground, and since there is an 82kΩ resistor from SDFLTCH to VSS, the internal latchset signal goes high.

t9: Output is latched off - even though CT has discharged to 0.5V, there will not be a retry since the latchset signal was allowed to remain high.

t10: Output remains latched off - CT has discharged all the way to 0V.

t11: The output has been latched off for quite some time. The user now wishes to reset the latched off output, thus toggling SDFLTCH high for greater than 1ms {t13 - t11}.

t12 = t15: The latchset signal is reset.

t13: Forcing of SDFLTCH is released after having been applied for > 1ms, the fault had also been released during the time the output was latched off, safe condition, return to normal operation of the hot swap power manager.

Figure 3. Latched Operation Mode: RLATCH = 82k

APPLICATION INFORMATION (cont.)

Determining External Component Values

Referring now to Figure 4. To set Rvdd the following must be achieved:

$$\frac{V_{INmin}}{R_{VDD}} > \frac{10V}{R1 + R2} + 2mA$$

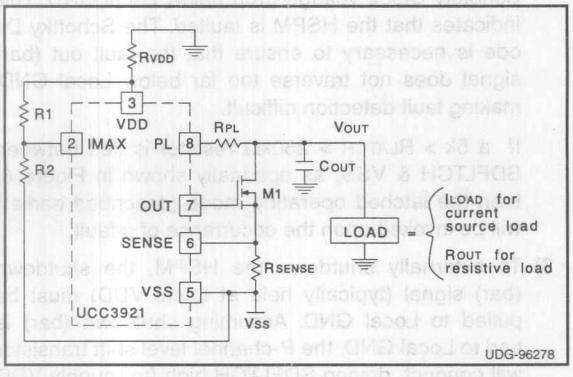


Figure 4.

In order to estimate the minimum timing capacitor, CT, several things must be taken into account. For example, given the schematic in Figure 4 as a possible (and at this point, a standard) application, certain external component values must be known in order to estimate CTMIN. Now, given the values of COUT, Load, RSENSE, VSS, and the resistors determining the voltage on the IMAX pin, the user can calculate the approximate startup time of the node VOUT. This startup time must be faster than the time it takes for CT to charge to 2.5V (relative to VSS), and is the basis for estimating the minimum value of CT. In order to determine the value of the sense resistor, RSENSE, assuming the user has determined the fault current, RSENSE can be calculated by:

$$R_{SENSE} = \frac{50mV}{I_{FAULT}}$$

Next, the variable IMAX must be calculated. IMAX is the maximum current that the UCC3921 will allow through the transistor, M1, and it can be shown that during startup with an output capacitor the power MOSFET, M1, can be modeled as a constant current source of value IMAX where

$$I_{MAX} = \frac{V_{IMAX}}{R_{SENSE}}$$ where VIMAX = voltage on pin IMAX.

Given this information, calculation of the startup time is now possible via the following:

Current Source Load:

$$T_{START} = \frac{C_{OUT} \bullet |VSS|}{I_{MAX} - I_{LOAD}}$$

Resistive Load:

$$T_{START} = C_{OUT} \bullet R_{OUT} \bullet L_N\left(\frac{I_{MAX} \bullet R_{OUT}}{I_{MAX} \bullet R_{OUT} - |VSS|}\right)$$

Once TSTART is calculated, the power limit feature of the UCC3921 must be addressed and component values derived. Assuming the user chooses to limit the maximum allowable average power that will be associated with the hot swap power manager, the power limiting resistor, RPL, can be easily determined by the following:

$$R_{PL} = \frac{P_{FET\ AVG}}{1\mu A \bullet I_{MAX}}$$ where a minimum RPL exists

defined by $R_{Pmin} = \frac{|VSS|}{5mA}$ (Refer to Figure 5).

Finally, after computing the aforementioned variables, the minimum timing capacitor can be derived as such:

Current Source Load:

$$C_{Tmin} = \frac{3 \bullet T_{START} \bullet (62\mu A \bullet R_{PL} + |VSS| - 10V)}{10 \bullet R_{PL}}$$

Resistive Load:

$$C_{Tmin} =$$

$$\frac{3 \bullet T_{START}(31\mu A \bullet R_{PL} + |VSS| - 5V - IMAX \bullet R_{OUT})}{5 \bullet R_{PL}} +$$

$$\frac{3 \bullet R_{OUT} \bullet |VSS| \bullet C_{OUT}}{5 \bullet R_{PL}}.$$

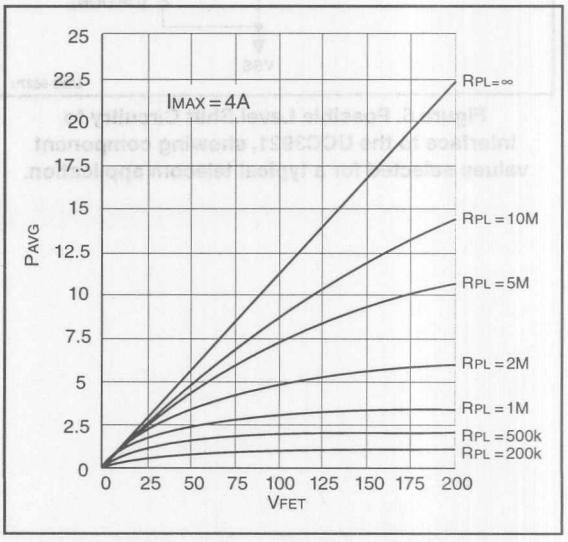


Figure 5. Plot Average Power vs FET Voltage for Increasing Values of RPL

APPLICATION INFORMATION (cont.)

Level Shift Circuitry to Interface with SDFLTCH

Some type of circuit is needed to interface with the UCC3921 via SDFLTCH, such as opto-couplers or level shift circuitry. Figure 6 depicts one implementation of level shift circuitry that could be used, showing component values selected for a typical –48V telecommunications application. There are three communication conditions which could occur; two of which are Hot Swap Power Manager (HSPM) state output indications, and the third being an External Shutdown.

1) When open, and under a non-fault condition, SDFLTCH is pulled to a low state. In Figure 6, the N-channel level shift transistor is off, and the fault out (bar) signal is pulled to Local VDD through R3. This indicates that the HSPM is not faulted.

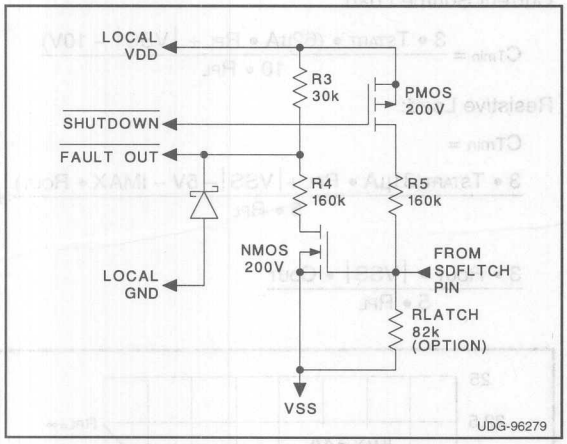


Figure 6. Possible Level Shift Circuitry to Interface to the UCC3921, showing component values selected for a typical telecom application.

2) When a fault is detected by the fault timer or undervoltage lockout, this pin will drive to a high state, indicating that the external power FET is off. In Figure 6, the N-channel level shift transistor will conduct, and the fault out (bar) signal will be pulled to a Schottky Diode voltage drop below Local GND. This indicates that the HSPM is faulted. The Schottky Diode is necessary to ensure that the fault out (bar) signal does not traverse too far below Local GND, making fault detection difficult.

   If a 5k > R_{LATCH} > 250kΩ resistor is tied between SDFLTCH & VSS, as optionally shown in Figure 6, then the latched operating mode (described earlier) will be invoked upon the occurrence of a fault.

3) To externally shutdown the HSPM, the shutdown (bar) signal (typically held at Local VDD) must be pulled to Local GND. Assuming shutdown (bar) is tied to Local GND, the P-channel level shift transistor will conduct, driving SDFLTCH high (to roughly VDD plus a diode). By sourcing > 250µA into SDFLTCH for > 1ms the output to the external power FET will be disabled. The current sourced into SDFLTCH must be limited to 10mA or less: $I_{SDFLTCHMAX}$ < 10mA.

SAFETY RECOMMENDATIONS

Although the UCC3921 is designed to provide system protection for all fault conditions, all integrated circuits can ultimately fail short. For this reason, if the UCC3921 is intended for use in safety critical applications where UL or some other safety rating is required, a redundant safety device such as a fuse should be placed in series with the external power FET. The UCC3921 will prevent the fuse from blowing for virtually all fault conditions, increasing system reliability and reducing maintenance cost, in addition to providing the hot swap benefits of the device.

APPLICATION INFORMATION (cont.)

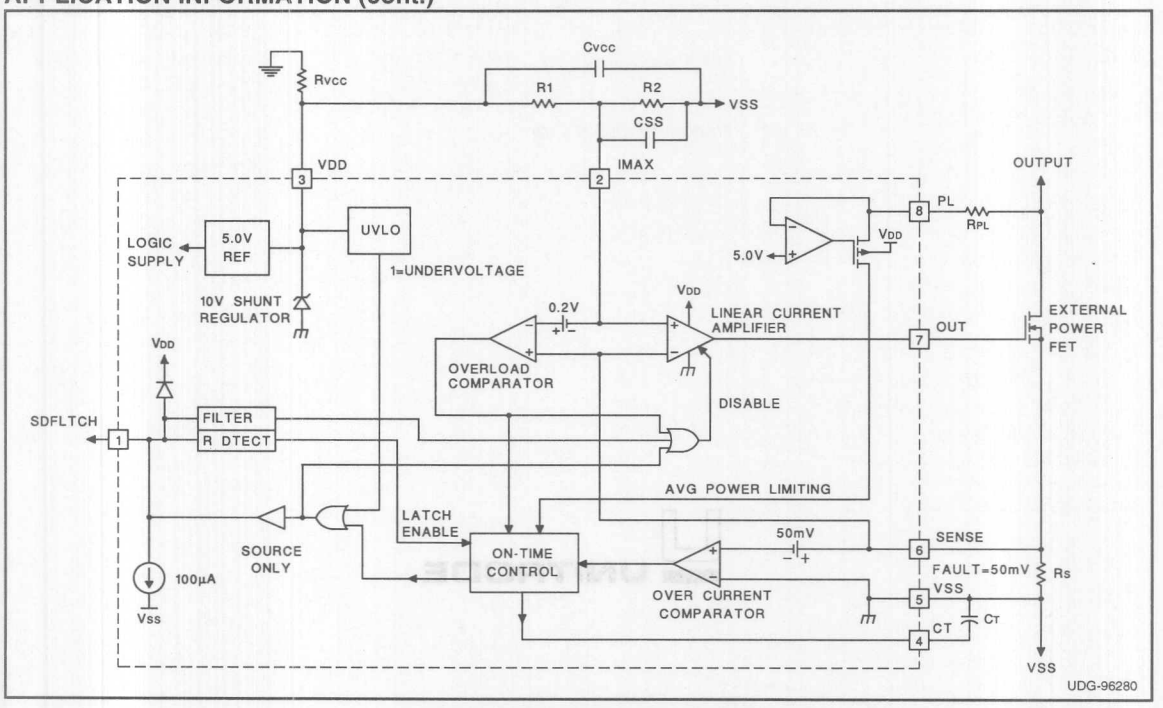
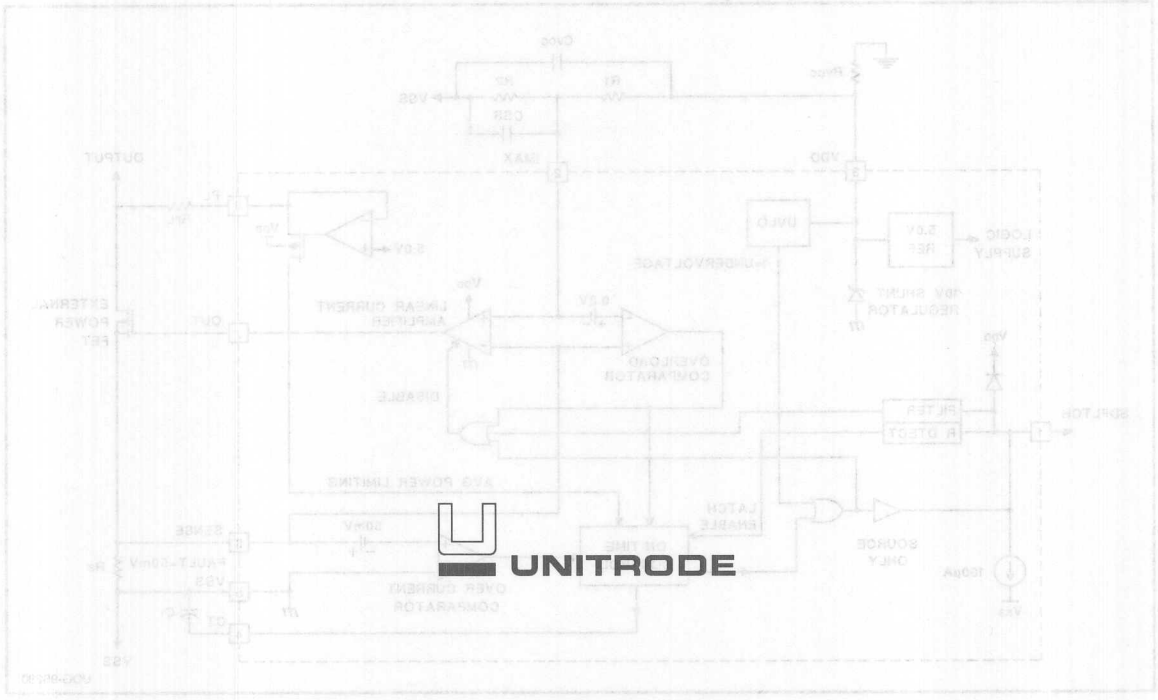


Figure 7. Application Diagram

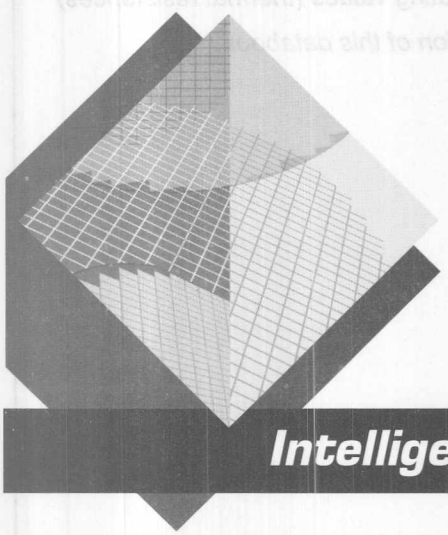
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Consult Applications Handbook for available applications/design notes.

Datasheets in this section are organized in numeric order using the commercial part number.



Intelligent Motion Circuits

10

Packaging Note:

- *Values listed for recommended lead soldering time and temperature apply to ceramic thru-hole components only. Please consult the Packaging Section of this databook for recommendations on plastic SMD board attach processing.*

- *Unless otherwise noted, thermal resistance values listed on individual data sheets are for the device as it operates in a plastic thru-hole package. Results for other packaging options can be inferred by scaling the package rating values (thermal resistances) presented in the Packaging Section of this databook.*

DC Brush Motor, 3 Phase Brushless DC Motor, & Stepper Motor Products

DC Brush Motor Products	UNITRODE PART NUMBER					
	L293	L293D	UC3637	UC3638 ✚	UC3717	UC3717A
Output Clamp Diodes		Y			Y	Y
Output Current per Output (A)	1	0.6	0.1	0.1/0.05	0.8	1
Operating Voltage (V)	4.5 - 36	4.5 - 36	5 - 36	10 - 36	10 - 45	10 - 46
Differential Current Sense Amplifier				Y		
Thermal Shutdown	Y	Y			Y	Y
Current Limit			Y	Y	Y	Y
Application/Design Note			DN-53A, U-102, U-112, U-120	U-120	U-99	U-99

DC Brush Motor Products (cont'd)	UNITRODE PART NUMBER					
	UC3770A/B	UC3172A	UC3173A	UC3175B	UC3176/7	UC3178
Output Clamp Diodes	Lower	Y	Y	Y	Y	Y
Output Current per Output (A)	1.3	1	0.55	0.8	2	0.45
Operating Voltage (V)	10 - 50	4 - 15	4 - 15	4 - 15	3 - 35	3 - 15
Differential Current Sense Amplifier		Y	Y	Y	Y	Y
Thermal Shutdown	Y	Y	Y	Y	Y	Y
Current Limit	Y	Y	Y	Y	Y	Y

3 Phase Brushless DC Motor Products	UNITRODE PART NUMBER	
	UC3625	UCC3626
Hall Logic	Y	Y
Tachometer	Y	Y
Output Current per Output (A)	0.1	0.01
Operating Voltage	10 - 18	11 - 15
Differential Current Sense Amplifier	Y	Y
Current Limit	Y	
Application/Design Note	DN-50, U-115, U-120, U-130	U-120

Stepper Motor Products	UNITRODE PART NUMBER					
	L293	L293D	UC3517	UC3717	UC3717A	UC3770A/B
Output Clamp Diodes		Y		Y	Y	Lower
Output Current per Output (A)	1	0.6	0.35	0.8	1	1.3
Operating Voltage (V)	4.5 - 36	4.5 - 36	10 - 40	10 - 45	10 - 46	10 - 50
Thermal Shutdown	Y	Y		Y	Y	Y
Current Limit				Y	Y	Y
Application/Design Note				U-99	U-99	

✚ New Product

Linear Power Amplifier Products	UNITRODE PART NUMBER				
	UC3172A	UC3173A	UC3175B	UC3176/7	UC3178
Four Quadrant	Y	Y	Y	Y	Y
Number of Outputs	2	2	2	2	2
BW (MHz)	2	2	2	1	2
Operating Voltage (V)	4 - 15	4 - 15	4 - 15	3 - 35	3 - 15
Output Current per Output (A)	1	0.55	0.8	2	0.45
Thermal Shutdown	Y	Y	Y	Y	Y
Differential Current Sense Amplifier	Y	Y	Y	Y	Y

Phase Locked Frequency Controller Products	UNITRODE PART NUMBER		
	UC3633	UC3634	UC3635
Internal Oscillator	Y	Y	Y
Divider Output Provided			Y
External Phase Detector Inputs			Y
2 Phase Drive Logic		Y	Y
Divide Logic Select	4/5 & 2/4/8	2/4/8	2/4
Operating Voltage (V)	8 - 15	8 - 15	8 - 15
Thermal Shutdown			
Maximum Frequency (MHz)	10	10	10
Application/Design Note	U-113	U-113	U-113

Power Supply Support Products	UNITRODE PART NUMBER		
	UC3610 ★	UC3611 ★	UC3612 ★
Description	Dual Schottky Diode Bridge	Quad Schottky Diode Array	Dual Schottky Diode
Application	Eight-diode Array for High Current, Low Duty Cycle Flyback Voltage Clamping for Inductive Loads	Four-diode Array for High Current Bridges and Voltage Clamps	Two-diode Array for High Current, Low Duty Cycle Flyback Voltage Clamping for Inductive Loads
Key Features	• Monolithic Eight-diode Array • High Peak Current • Low Forward Voltage • Fast Recovery Time	• Matched, Four-diode Monolithic Array • High Peak Current • Low Forward Voltage • Parallelable for Higher Current or Lower Voltage Drop	• Monolithic Two-diode Array • High Peak Current • Low Forward Voltage • Fast Recovery Time

★ Refer to General Power Supply Circuits Section for Product Data Sheet

Push-Pull Four Channel Driver

FEATURES

- Output Current 1A Per Channel (600mA for L293D)
- Peak Output Current 2A Per Channel (1.2A for L293D)
- Inhibit Facility
- High Noise Immunity
- Separate Logic Supply
- Over-Temperature Protection

DESCRIPTION

The L293 and L293D are quad push-pull drivers capable of delivering output currents to 1A or 600mA per channel respectively. Each channel is controlled by a TTL-compatible logic input and each pair of drivers (a full bridge) is equipped with an inhibit input which turns off all four transistors. A separate supply input is provided for the logic so that it may be run off a lower voltage to reduce dissipation.

Additionally the L293D includes the output clamping diodes within the IC for complete interfacing with inductive loads.

Both devices are available in 16-pin Batwing DIP packages. They are also available in Power SOIC and Hermetic DIL packages.

TRUTH TABLE

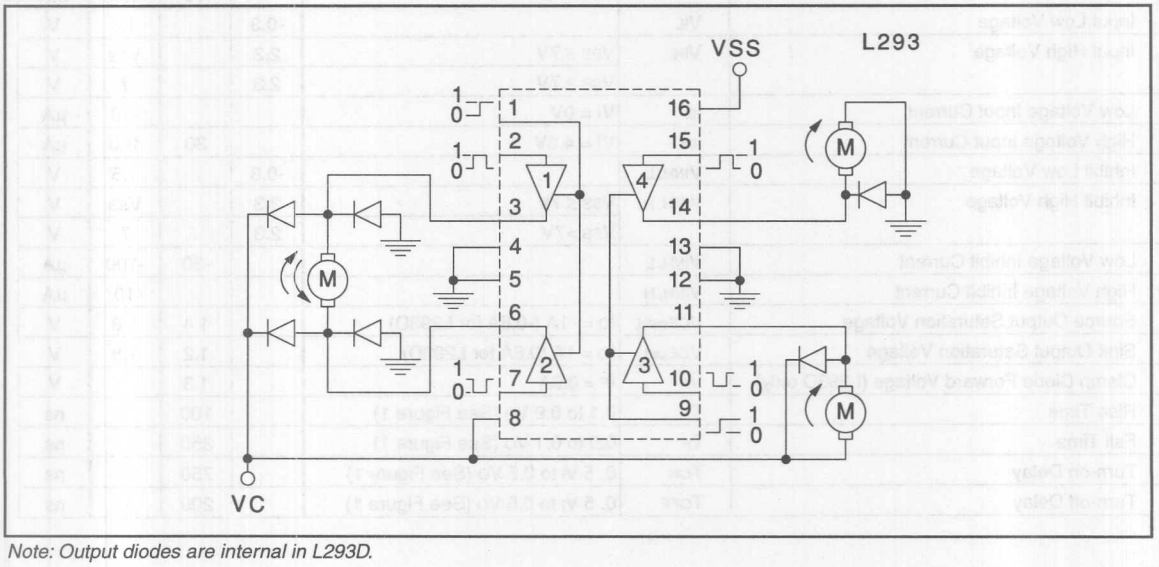
V_I (each channel)	V_{INH}*	V_O
H	H	H
L	H	L
H	L	X**
L	L	X**

**Relative to the considered channel*
***High output impedence*

ABSOLUTE MAXIMUM RATINGS

Collector Supply Voltage, V_C 36V
Logic Supply Voltage, V_{SS} 36V
Input Voltage, V_I 7V
Inhibit Voltage, V_{INH} 7V
Peak Output Current (Non-Repetitive), I_{OUT} (L293) 2A
I_{OUT} (L293D) 1.2A
Total Power Dissipation
at Tground-pins = 80°C, N Batwing pkg, (Note) 5W
Storage and Junction Temperature, Tstg, T_J . . . . . -40 to +150°C
Note:Consult packaging section of Databook for thermal limitations and considerations of packages.

BLOCK DIAGRAM

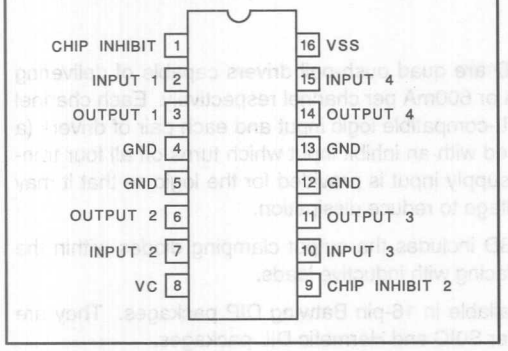


Note: Output diodes are internal in L293D.

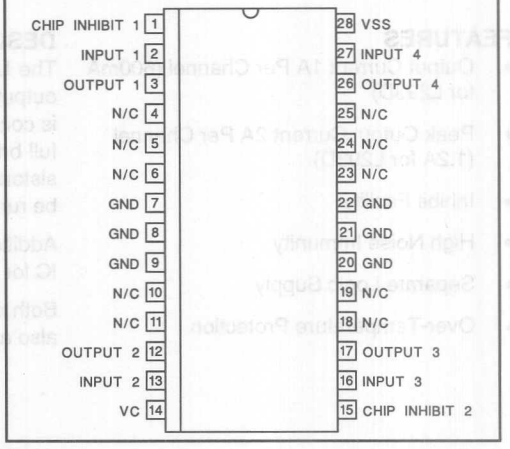
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CONNECTION DIAGRAMS

DIL-16 (TOP VIEW)
N Package, SP Package



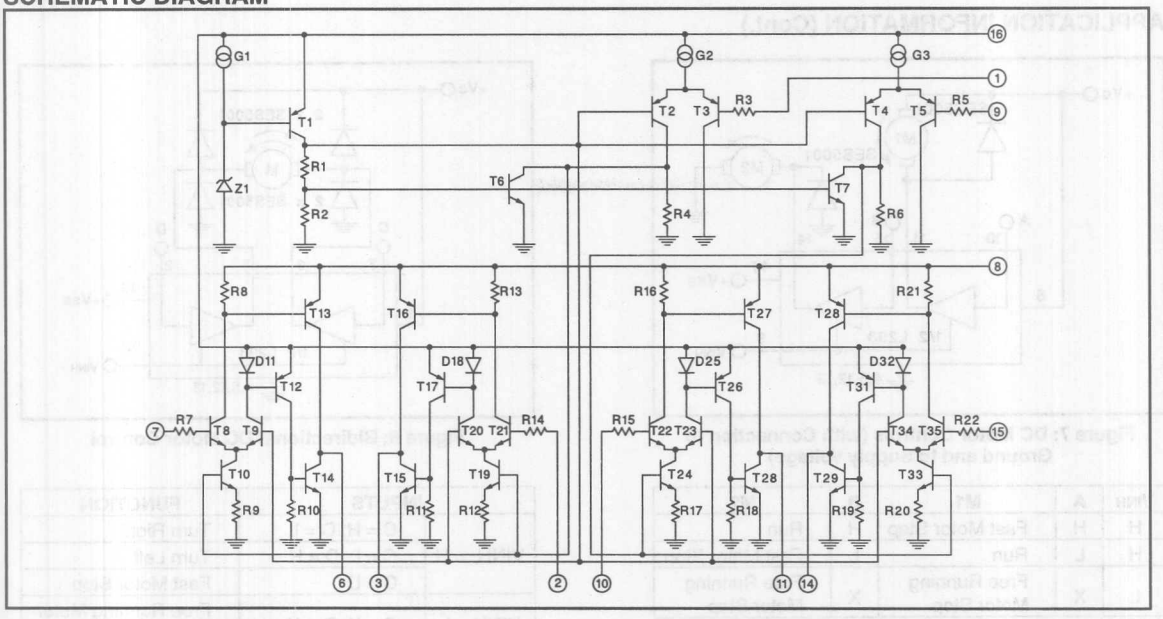
SOIC-28 (TOP VIEW)
DWP Package



ELECTRICAL CHARACTISTICS: (For each channel, V_C = 24V, V_{SS} = 5V, T_{AMB} = 25°C, unless otherwise specified; $T_A = T_J$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Collector Supply Voltage	V_C				36	V
Logic Supply Voltage	V_{SS}		4.5		36	V
Collector Supply Current	I_C	V_I = L, I_O = 0, V_{INH} = H		2	6	mA
		V_I = H, I_O = 0, V_{INH} = H		16	24	mA
		V_{INH} = L			4	mA
Total Quiescent Logic Supply Current	I_{SS}	V_I = L, I_O = 0, V_{INH} = H		44	60	mA
		V_I = H, I_O = 0, V_{INH} = H		16	22	mA
		V_{INH} = L		16	24	mA
Input Low Voltage	V_{IL}		-0.3		1.5	V
Input High Voltage	V_{IH}	$V_{SS} \leq 7V$	2.3		V_{SS}	V
		$V_{SS} \geq 7V$	2.3		7	V
Low Voltage Input Current	I_{IL}	V_I = 0V			-10	µA
High Voltage Input Current	I_{IH}	V_I = 4.5V		30	100	µA
Inhibit Low Voltage	$V_{INH, L}$		-0.3		1.5	V
Inhibit High Voltage	$V_{INH, H}$	$V_{SS} \leq 7V$	2.3		V_{SS}	V
		V_{SS} >7V	2.3		7	V
Low Voltage Inhibit Current	$V_{INH, L}$			-30	-100	µA
High Voltage Inhibit Current	$V_{INH, H}$				10	µA
Source Output Saturation Voltage	V_{CEsatH}	I_O = -1A (-0.6A for L293D)		1.4	1.8	V
Sink Output Saturation Voltage	V_{CEsatL}	I_O = 1A (0.6A for L293D)		1.2	1.8	V
Clamp Diode Forward Voltage (L293D only)	V_F	I_F = 0.6A		1.3		V
Rise Time	T_R	0.1 to 0.9 V_O (See Figure 1)		100		ns
Fall Time	T_F	0.9 to 0.1 V_O (See Figure 1)		350		ns
Turn-on Delay	T_{ON}	0. 5 V_I to 0.5 V_O (See Figure 1)		750		ns
Turn-off Delay	T_{OFF}	0. 5 V_I to 0.5 V_O (See Figure 1)		200		ns

SCHEMATIC DIAGRAM



APPLICATION INFORMATION

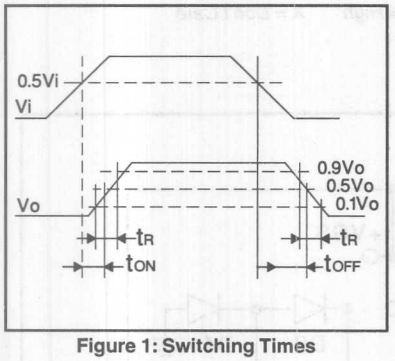


Figure 1: Switching Times

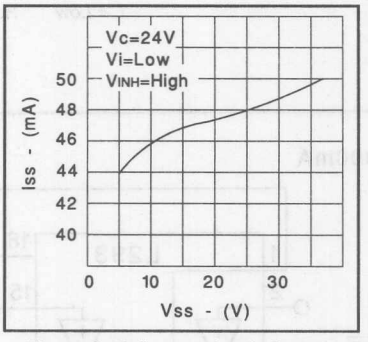


Figure 2: Quiescent Logic Supply Current vs Logic Supply Voltage

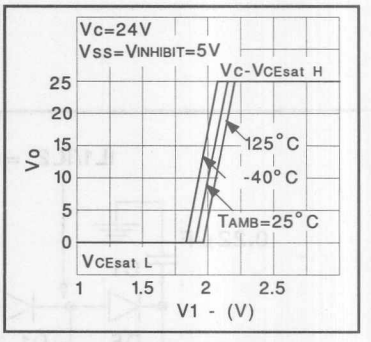


Figure 3: Output Voltage vs Input Voltage

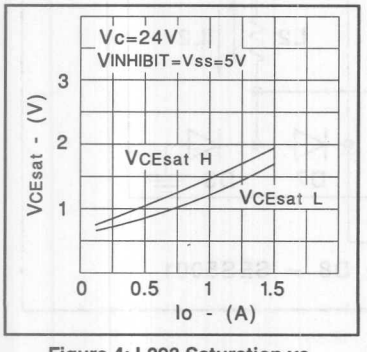


Figure 4: L293 Saturation vs Output Currrent

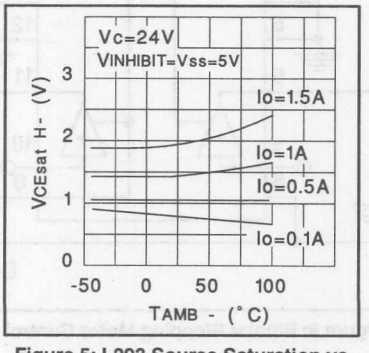


Figure 5: L293 Source Saturation vs Ambient Temperature

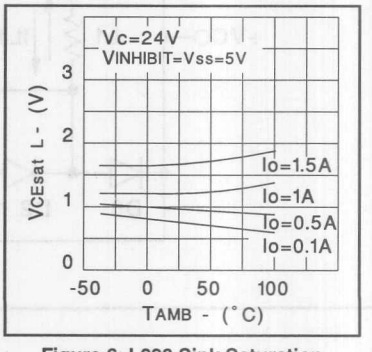


Figure 6: L293 Sink Saturation Voltage vs Ambient Temperature

NOTE: For L293D curves, multiply output current by 0.6.

APPLICATION INFORMATION (Cont.)

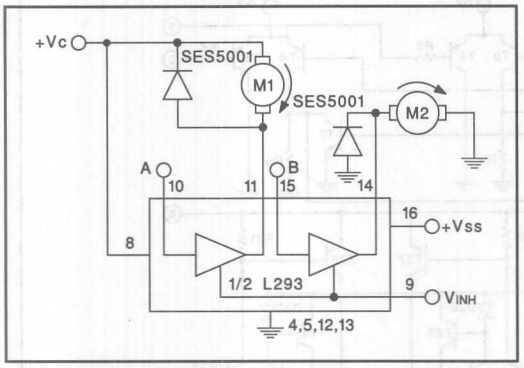


Figure 7: DC Motor Controls (with Connection to Ground and to Supply Voltage)

VINH	A	M1	B	M2
H	H	Fast Motor Stop	H	Run
H	L	Run	L	Fast Motor Stop
L	X	Free Running Motor Stop	X	Free Running Motor Stop

L = Low H = High X = Don't Care

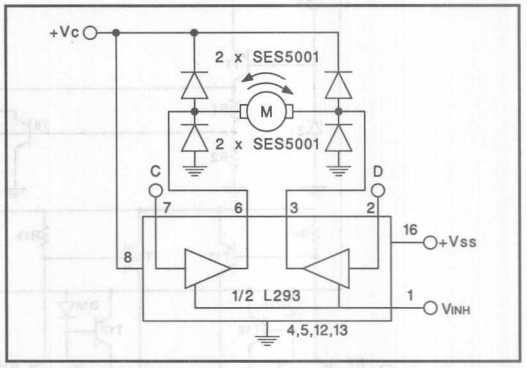


Figure 8: Bidirectional DC Motor Control

INPUTS		FUNCTION
VINH = H	C = H; D = L	Turn Right
	C = L; D = H	Turn Left
	C = D	Fast Motor Stop
VINH = L	C = X; D = X	Free Running Motor Stop

L = Low H = High X = Don't Care

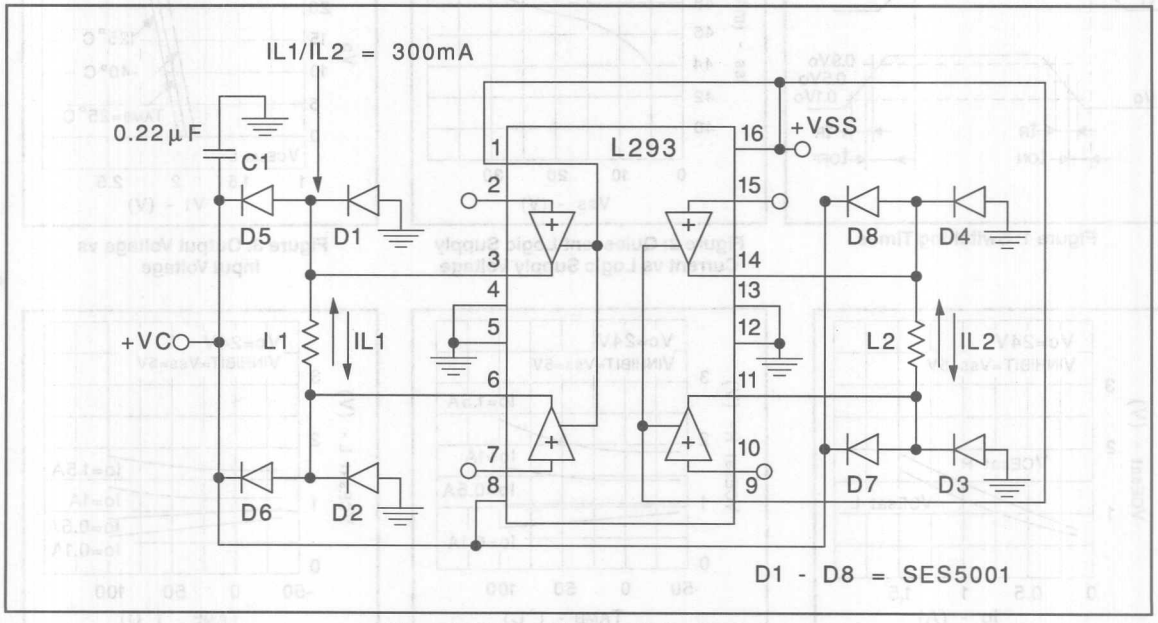


Figure 9: Bipolar Stepping Motor Control

MOUNTING INSTRUCTIONS

The Rthj-amp of the L293 can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board or to an external heatsink.

The diagram of Figure 13 shows the maximum package power Ptot and the θJA as a function of the side "l" of two equal square copper areas having a thickness of 35µ (see Figure 10). In addition, it is possible to use an external heatsink (see Figure 11).

During soldering the pins' temperature must not exceed 260°C and the soldering time must not be longer than 12 seconds.

The external heatsink or printed circuit copper area must be connected to electrical ground.

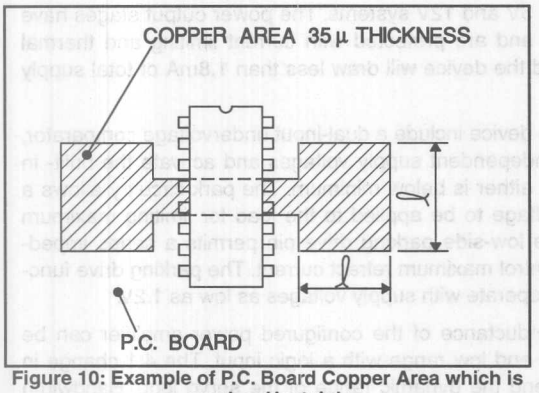


Figure 10: Example of P.C. Board Copper Area which is used as Heatsink

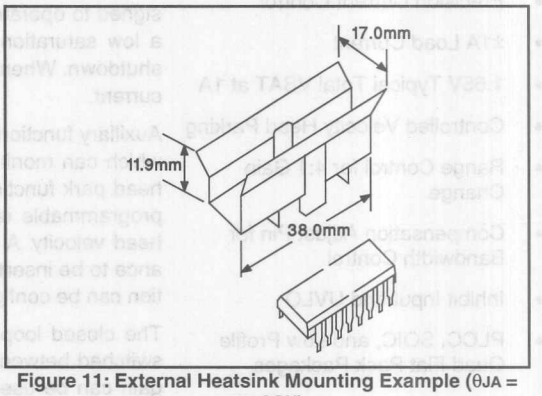


Figure 11: External Heatsink Mounting Example (θJA = 25°C/W)

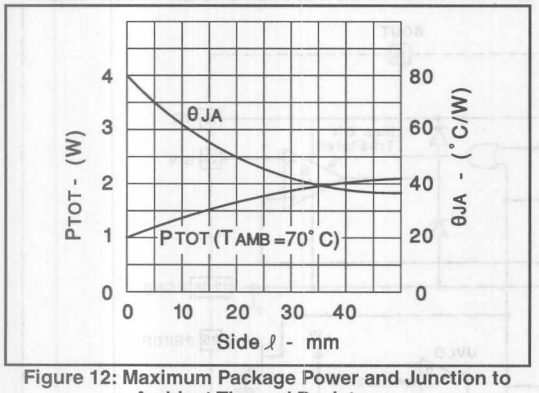


Figure 12: Maximum Package Power and Junction to Ambient Thermal Resistance

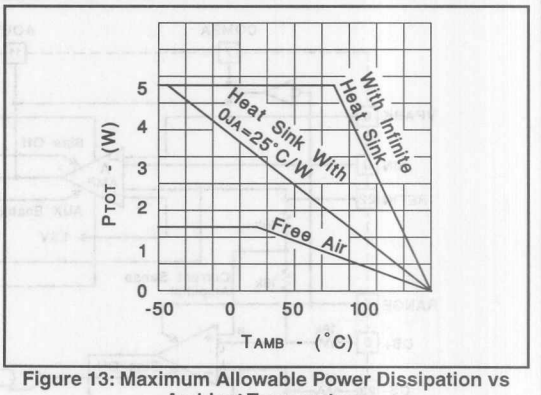


Figure 13: Maximum Allowable Power Dissipation vs Ambient Temperature

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

UNITRODE

Full Bridge Power Amplifier

FEATURES

- Plug-in Compatibility with the UC3173A
- 5V or 12V Operation
- 13mA Quiescent Supply Current
- 1.8mA Standby Current
- Precision Current Control
- ±1A Load Current
- 1.65V Typical Total VSAT at 1A
- Controlled Velocity Head Parking
- Range Control for 4:1 Gain Change
- Compensation Adjust Pin for Bandwidth Control
- Inhibit Input and UVLO
- PLCC, SOIC, and Low Profile Quad Flat Pack Packages

DESCRIPTION

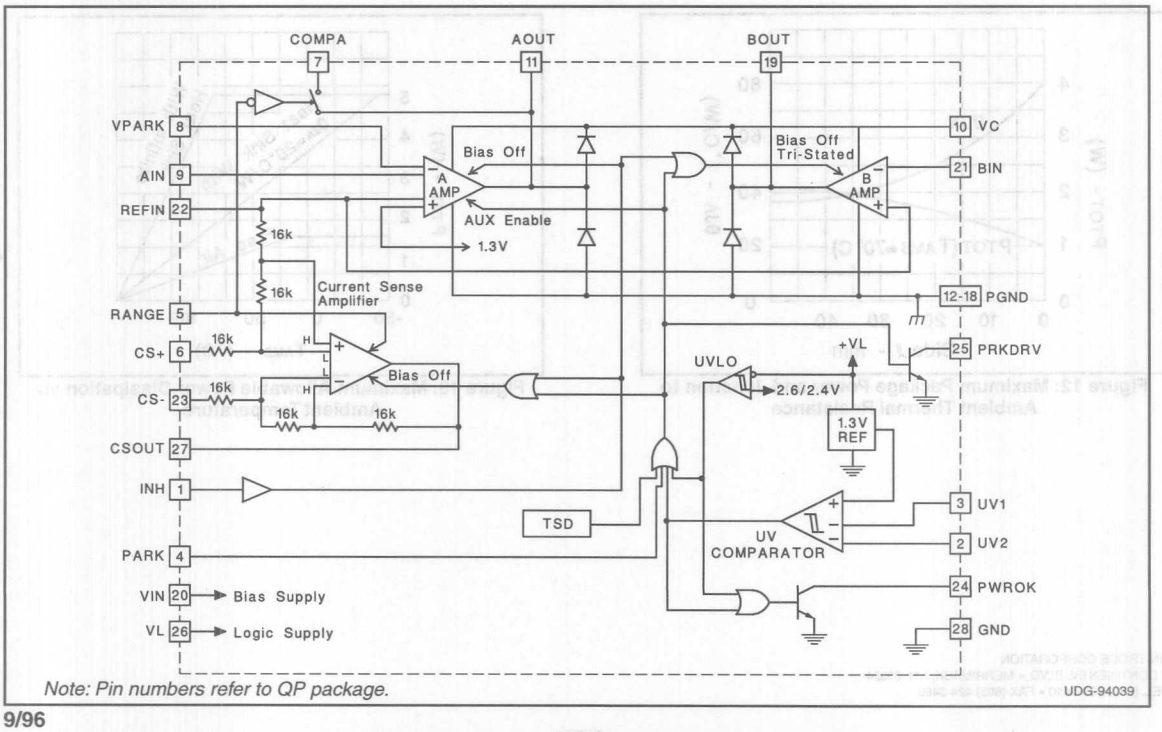
The UC3172A power amplifier is pin-for-pin compatible with the UC3173A. Improvements have been made to allow more liberal application of the device.

This full bridge power amplifier, rated for continuous output current of 1A, is intended for use in demanding servo applications such as head positioning for high-density disk drives. This device includes a precision current sense amplifier that senses load current with a single resistor in series with the load. The UC3172A is optimized to consume a minimum of supply current, and is designed to operate in both 5V and 12V systems. The power output stages have a low saturation voltage and are protected with current limiting and thermal shutdown. When inhibited the device will draw less than 1.8mA of total supply current.

Auxiliary functions on this device include a dual-input undervoltage comparator, which can monitor two independent supply voltages and activate the built- in head park function when either is below minimum. The park circuitry allows a programmable retract voltage to be applied to the load for limiting maximum head velocity. A separate low-side parking drive pin permits a series impedance to be inserted to control maximum retract current. The parking drive function can be configured to operate with supply voltages as low as 1.2V.

The closed loop transconductance of the configured power amplifier can be switched between a high and low range with a logic input. The 4:1 change in gain can be used to extend the dynamic range of the servo loop. Bandwidth variations that would otherwise result with the gain change can be controlled with a compensation adjust pin.

BLOCK DIAGRAM



Note: Pin numbers refer to QP package.

UDG-94039

ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Supply Voltage, (VIN, VC, VL) 18V
UV Comparator
  Maximum Forced Voltage ..... –0.3V to 6V
  Maximum Forced Current ..... ±10mA
Logic Inputs and REFIN
  Maximum Forced Voltage ..... –0.3V to 10V
  Maximum Forced Current ..... ±10mA
B Amplifier Inverting Input ..... –0.3V to VIN + 1.0
A Amplifier Inverting Inputs,
  (Aux. and Normal) ..... –0.3V to VC + 1.0V
Open Collector Output Voltages 20V
A and B Output Currents (Continuous)
  Source ..... Internally Limited
  Sink 1A
Parking Drive (PRKDRV) Output Current
  Continuous 150mA
  Pulsed 1A
Output Diode Current (Pulsed) 1A
Power OK (PWROK) Output Current
  Continuous 30mA
  Pulsed (Note 2) 150mA
Operating Junction Temperature ..... – 55°C to +150°C
Storage Temperature ..... – 65°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

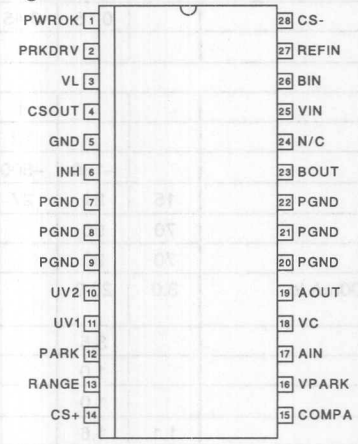
Note 1: Unless otherwise indicated, voltages are referenced to ground and currents are positive into, negative out of, the specified terminals, "Pulsed" is defined as a less than 10% duty cycle pulse with a maximum duration of 500µs.

Note 2: The PWROK output will safely discharge a capacitive load of up to 30 nanojoules.

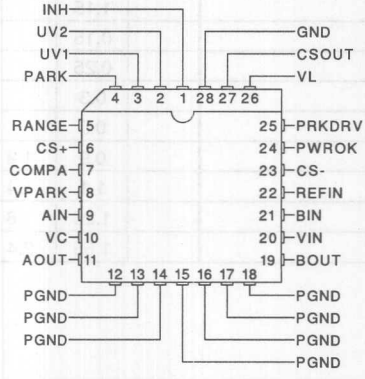
Note 3: Consult Packaging Section of Unitrode Integrated Circuits databook for thermal specifications and limitations of packages.

CONNECTION DIAGRAMS

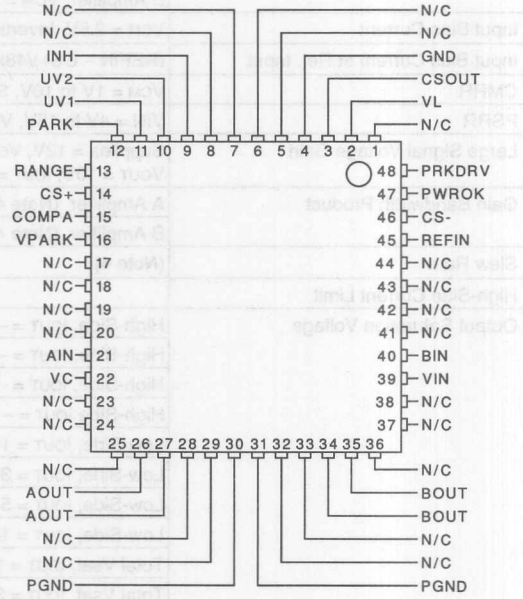
SOIC-28 (Top View)
DWP Package



PLCC-28 (Top View)
QP Package



TQFP-48 (Top View)
FQ Package



ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for T_A = 0 to +70°C, VIN = 5V, VC = VIN = VL, REFIN = VIN/2, RANGE, PARK, and INH = 0V, and T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply					
VIN Supply Current	Low Range Mode		11	15	mA
	High Range Mode		17	23	mA
VC Supply Current	I_{OUT} = 0A, Low Range Mode		1.2	2.5	mA
	I_{OUT} = 0A, High Range Mode		1.2	2.5	mA
VL Supply Current	Low Range Mode		0.75	1.1	mA
	High Range Mode		0.8	1.2	mA
Total Supply Current	Supplies = 5V, I_{OUT} = 0A, Low Range Mode		13	17	mA
	Supplies = 12V, I_{OUT} = 0A, Low Range Mode		14	20	mA
	Supplies = 5V, I_{OUT} = 0A, High Range Mode		19	25	mA
	Supplies = 12V, I_{OUT} = 0A, High Range Mode		21	29	mA
VL UVLO Threshold	Low to High		2.6	2.8	V
UVLO Threshold Hysteresis			200		mV
Under Voltage (UV) Comparator					
Input Bias Current	Max at Either UV Input		–0.25	–1.0	µA
UV Thresholds	Low to High, Other Input = 5V	1.28	1.3	1.32	V
UV Threshold Hysteresis		19	24	29	mV
PWROK Vsat	I_{OUT} = 5mA, UV Input Low		0.15	0.45	V
PWROK Leakage	V_{OUT} = 20V			5	µA
Power Amplifiers A and B					
Input Offset Voltage	A Amplifier, V_{CM} = 2.5V			4	mV
	B Amplifier, V_{CM} = 2.5V			12	mV
Input Bias Current	V_{CM} = 2.5V, Inverting Inputs Only		–150	–500	nA
Input Bias Current at Ref. Input	(REFIN – CS+)/48kohms, T_J = 25°C	15	21	27	µA/V
CMRR	V_{CM} = 1V to 10V, Supplies = 12V	70	90		dB
PSRR	VIN = 4V to 15V, Vcm = 1.5V	70	90		dB
Large Signal Voltage Gain	Supplies = 12V, V_{OUT} = 1V, I_{OUT} = 300mA to V_{OUT} = 10V, I_{OUT} = –300mA	3.0	20.0		V/mV
Gain Bandwidth Product	A Amplifier (Note 4)		3.5		MHz
	B Amplifier (Note 4)		1.0		MHz
Slew Rate	(Note 4)		1.0		V/µs
High-Side Current Limit		1.1	1.6		A
Output Saturation Voltage	High-Side, I_{OUT} = –100mA (Note 5)		0.75		V
	High-Side, I_{OUT} = –300mA (Note 5)		0.85		V
	High-Side, I_{OUT} = –550mA (Note 5)		0.95		V
	High-Side I_{OUT} = –1A (Note 5)		1.15		V
	Low-Side, I_{OUT} = 100mA		0.15		V
	Low-Side, I_{OUT} = 300mA		0.25		V
	Low-Side, I_{OUT} = 550mA		0.3		V
	Low-Side, I_{OUT} = 1A		0.5		V
	Total Vsat, I_{OUT} = 100mA		0.9	1.2	V
	Total Vsat, I_{OUT} = 300mA		1.1	1.4	V
	Total Vsat, I_{OUT} = 550mA		1.25	1.6	V
	Total Vsat, I_{OUT} = 1A		1.65	2.4	V

ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for T_A = 0 to +70°C, VIN = 5V, VC = VIN = VL, REFIN = VIN/2, RANGE, PARK, and INH = 0V, and T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Power Amplifiers A and B (cont.)					
VC to VIN Headroom	Volts below VIN, delta High-Side, Vsat = 100mV, I_{OUT} = –550mA (Note 5)	0.23	0.4		V
High-Side Diode, V_F	Id = 1A		1.5		V
Low-Side Diode, V_F	Id = 1A, INH Activated, B Amplifier Only		1.5		V
Current Sense Amplifier					
Common-mode Range	Supplies = 12V (Note 4)	–3		13	V
Input Offset Voltage	V_{CM} = 2.5V, Low Range Mode			2.0	mV
	V_{CM} = 2.5V, High Range Mode			4.0	mV
Input Offset Change with Common Mode Input	V_{CM} = 0V to 13V, Supplies = 12V, Low Range Mode			2000	µV/V
	V_{CM} = 0V to 13V, Supplies = 12V, High Range Mode			4000	µV/V
Voltage Gain	V_{DIFF} = +1.0 to –1.0V, V_{CM} = 2.5V, High Range Mode	0.485	0.50	0.515	V/V
	V_{DIFF} = +1.0 to –1.0V, V_{CM} = 2.5V, Low Range Mode	1.95	2.0	2.05	V/V
Saturation Voltage	Low-Side, I_{OUT} = 1mA		0.1	0.3	V
	High-Side, I_{OUT} = –1mA, Referenced to VIN		0.1	0.3	V
Parking Function					
PARK Threshold Voltage		0.6	1.1	1.7	V
PARK Threshold Current	Internal Pull-Up, PARK = 0.6V		50	75	µA
PRKDRV Saturation Voltage	I_{OUT} = 50mA		0.15	0.35	V
PRKDRV Leakage	V_{OUT} = 20V			50	µA
Regulating Voltage at VPARK Input		1.275	1.30	1.325	V
Amplifier A Auxiliary Input Bias Current			–300	–750	nA
Amplifier A Parking High-Side Saturation Voltage	I_{OUT} = –50mA, VIN = 0V, VC = VL = 5V, PARK Open, VC to AOUT		0.8	0.95	V
Minimum Parking Supply	At VC and VL, VIN = 0V, AOUT - PRKDRV Vsat > 0.5V, I_{PARK} = 50mA		1.4	1.7	V
Minimum Supply for Parking Drive and Power OK Operation	At VL, VC = VIN = 0V, Vsat < 0.5V, PRKDRV I_{OUT} = 50mA, Rl = 30 ohms to 2V		1.1	1.4	V
	PWROK I_{OUT} = 5mA, Rl = 300 ohms to 2V		1.2	1.6	V
VL Parking Supply Current	PARK Open, VL = 5V, VC = 1.6V, VIN = 0V, PWROK I_{OUT} = 5mA, PRKDRV I_{OUT} = 50mA		1.6	3.0	mA
Auxiliary Functions					
INH Threshold		0.6	1.1	1.7	V
INH Current	INH = 1.7V		–0.5	–1.0	µA
RANGE Threshold		0.6	1.1	1.7	V
RANGE Current	RANGE = 1.7V		50	100	µA
COMPA Pin Saturation Voltage	RANGE = 0V, Pin Current = ±500µA, Referenced to A_{OUT}		0.02	0.1	V
COMPA Leakage Current	RANGE = 1.7V, Supplies = 12V, A_{OUT} – V_{COMPA} = ±6V			5	µA
Total Supply Current when Inhibited	VIN, VC, and VL currents		1.0	1.8	mA
Thermal Shutdown Temperature	(Note 4)		165		°C

Note 4: Guaranteed by design. Not 100% tested in production.
Note 5: The high -side saturation performance of the UC3172A is referenced to the VIN supply pin. The VC supply pin can operate about 400mV below the VIN supply input without affecting the performance.

PIN DESCRIPTIONS

AIN: Inverting input to the A amplifier. Used as the summing node to close the loop on the overall power amplifier.

AOUT: Output for the A power amplifier, providing one end of the differential drive to the load during normal operation and during park. During a UVLO condition at the VL supply pin, this output is forced to a high, source only state. When the UC3172A is inhibited, this output will be set high, in a source only state.

BIN: Inverting input to the B amplifier. Used to program the gain of the B amplifier to guarantee maximum voltage swing to the load.

BOUT: Output for the B power amplifier, providing one end of the differential drive to the load during normal operation. During park and while inhibited this pin is tri-stated.

COMPA: The compensation adjust pin allows the user to provide an auxiliary compensation network for the A amplifier that is only active when the current sense amplifier is in the low range. With this option, the user can control the change in bandwidth that would otherwise result from the gain change in the feedback loop.

CS+: The non-inverting input to the current sense amplifier is typically tied to the connection between AOUT and the series current sense resistor.

CS-: The inverting input to the current sense amplifier is typically tied to the load side of the current sense resistor connected in series with the load. This pin can be pulled below ground during an abrupt load current change with an inductive load.

CSOUT: The output of the current sense amplifier has a 1.5mA current source pull-up and an active NPN pull-down. The output will pull to within 0.3V of either rail with a load current of less than 1mA.

GND: Reference point for the internal reference, UV comparator, and other low-level circuitry.

INH: A high impedance logic input that disables the A and B power amplifiers, as well as the current sense amplifier. The UV comparators and logic functions of the UC3172A remain active. This input has an internal pull-up that will inhibit the device if the input is left open. The INH function is overridden by any condition that forces the park function to be activated.

PARK: Logic input that forces the park condition on the UC3172A. This input has an internal pull-up that will force the park condition if the pin is left open.

PGND: Current return for all high level circuitry, this pin should be connected to the same potential as GND.

PRKDRV: A 100mA drive output that is active low during a park operation. This pin is normally used to supply the low-side drive to the load during parking, in place of the B amplifier. A series resistor can be added between this pin and the load to limit current during park.

PWROK: Indicates with an active low condition that either of the UV inputs are low, or that the supply voltage at the VL input to the UC3172A has dropped below the UVLO threshold. This output will remain active low until the VL supply has dropped to below approximately 1.2V.

RANGE: When this pin is open or at a logic low potential, the current sense amplifier will be in its low range mode. In this mode the voltage gain of the current sense amplifier will be 2. If this pin is brought to a logic high, the gain of the current sense amplifier will change into its high range value of 0.5. This factor of four change in gain will vary the overall transconductance of the power amplifier by the same ratio, with the transconductance being the highest in the high mode. This feature allows improved dynamic range of load current control for a given control input range and resolution.

REFIN: Reference for input control signals to the power amplifier, as well as, the non-inverting inputs to the A and B amplifiers, and the output level shift for the CS amplifier.

VC: High current supply to the collectors of the high-side NPN output devices on the A and B amplifiers. This supply should be powered whenever the A or B amplifiers are activated. This pin can operate approximately 400mV below the VIN supply without affecting the voltage available to the load. This supply pin provides drive to the power amplifiers during a parking operation.

VIN: Provides bias supply to both the power amplifiers and the current sense amplifiers. The high-side drive to the power stages on both the A and B amplifiers is referenced to this pin. The high side saturation voltages are specified and measured with respect to this supply pin. The parking function of the device is fully operational independent of the voltage at this pin.

VL: Logic portions of the UC3172A are powered by this supply pin, including the reference, UVLO, the UV comparators, and the PRKDRV and PWROK outputs. This pin is a low current supply that would normally be tied to the VC pin, or to a parking hold up capacitor for extended parking operation with very low recovered back EMF.

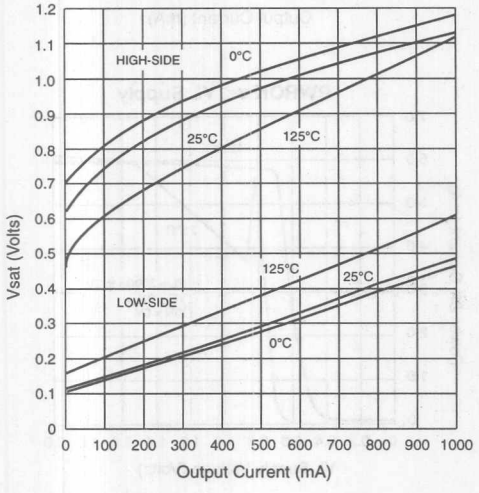
PIN DESCRIPTIONS (cont.)

VPARK: The auxiliary inverting input to the A amplifier, activated during park conditions on the UC3172A. An internal auxiliary non-inverting input is connected to the 1.3V reference. When the auxiliary inputs are activated, the A amplifier will force a programmed voltage at its output for a maximum back-EMF/velocity retract of the head. The park condition on the UC3172A is always activated by any one of the following four conditions, 1: a low condition on either of the UV inputs, 2: a high input level at the PARK input, 3: a UVLO condition at the VL supply pin, and 4: activation of the TSD (thermal shutdown) protection circuit. During a UVLO condition at the VL pin the auxiliary inputs to the A amplifier are over-ridden, and the A amplifier output is forced to its high state.

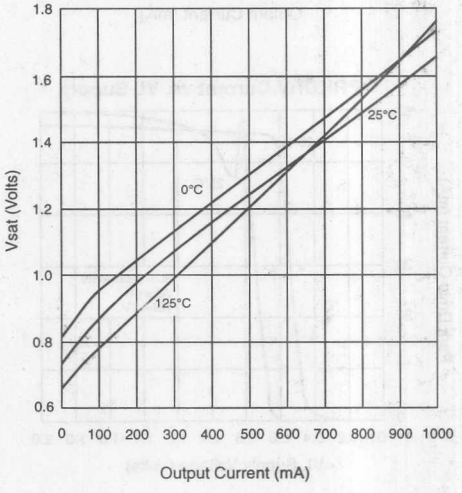
UV1 & 2: Inputs to the UV comparator, these inputs are high impedance sensing points used to monitor external supply conditions. Either of the inputs going low will force the device into a park condition, and force the PWROK output to an active low state. If either of these inputs is not used it should be connected to a voltage greater than 1.3V.

APPLICATION INFORMATION

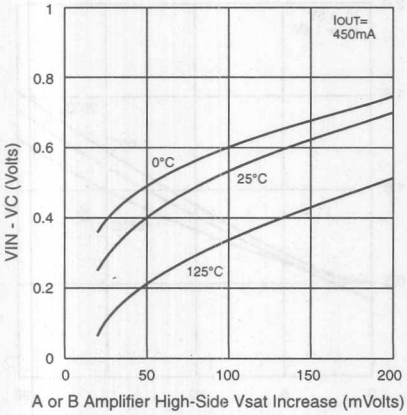
A and B Amplifier High and Low Vsats



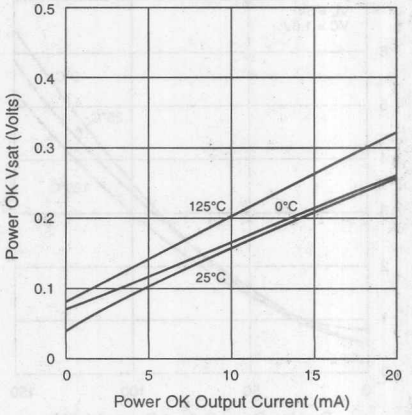
A and B Amplifier Total Vsat



VIN to VC Headroom

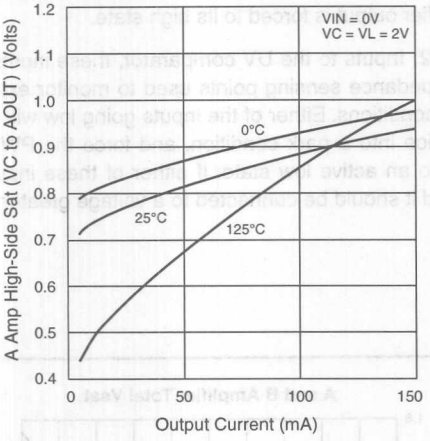


PWROK Saturation Voltage

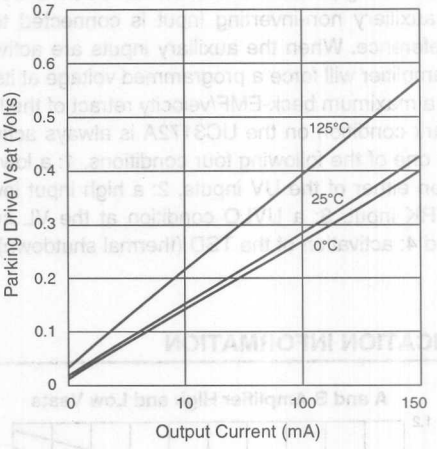


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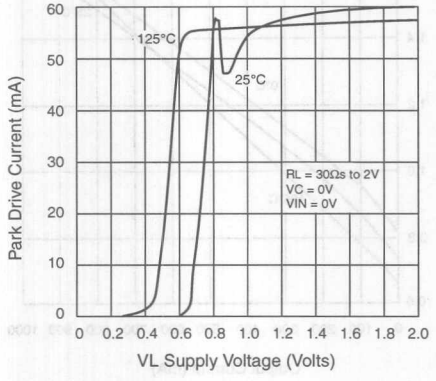
A Amplifier High-Side Vsat in Park Mode



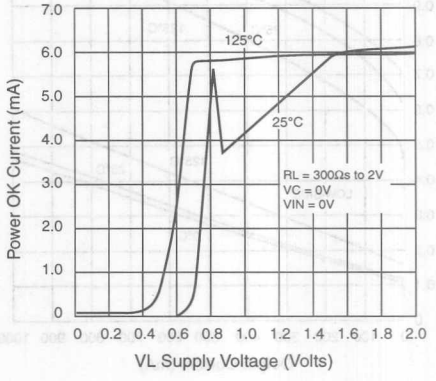
PRKDRV Saturation Voltage



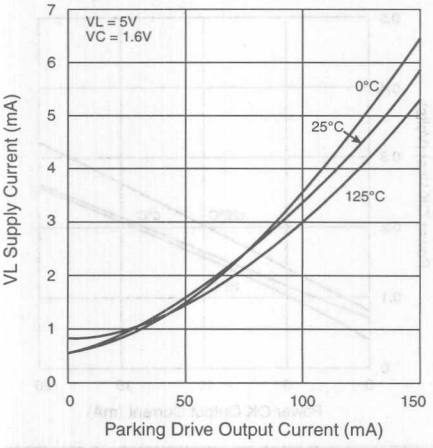
PRKDRV Current vs. VL Supply



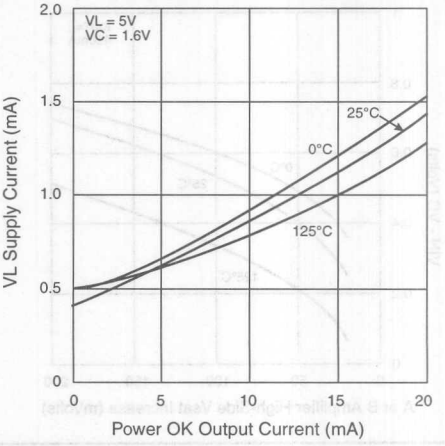
PWROK vs. VL Supply



VL Current vs. PRKDRV Current



VL Current vs. PWROK Current



APPLICATION INFORMATION (cont.)

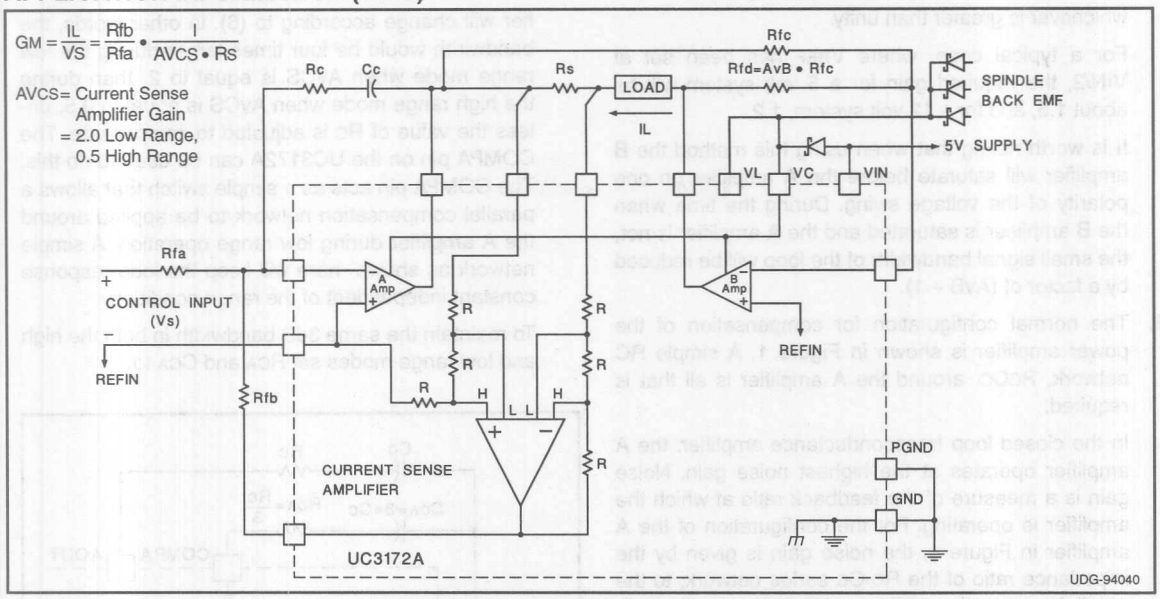


Figure 1. Typical Application

Design Procedure for Application of the UC3172A

The following is a simple design flow that can be used to configure the UC3172A or UC3173A Full Bridge Power Amplifiers as shown in Figure 1.

Definitions:

- f_{3dB} = the closed loop 3dB bandwidth
- A_{VB} = B amplifier closed loop gain, = Rfd/Rfc
- A_{VCS} = current sense amplifier gain, = 0.5 in high range, and 2.0 in low range
- f_{GBWA} = gain bandwidth product of the A amplifier
- G_{MHR} = closed loop transconductance in high range mode
- G_{MLR} = closed loop transconductance in low range mode
- L = load inductance
- R_L = load resistance

A. Choose R_S to be as large as head room will tolerate, this is the series current sense resistor.

B. Choose a value of R_{FB} to be less than the peak current sense amplifier swing divided by 1mA. A value in the range of 3k to 10k is suggested.

C. Calculate R_{FA} according to:

$$(1)\quad R_{FA} = \frac{R_{FB}}{0.5 \cdot R_S \cdot G_{MHR}}$$

If the range change option is not going to be used, it is recommended that the device be set in the low range mode and R_{FA} be calculated by:

$$(2)\quad R_{FA} = \frac{R_{FB}}{2 \cdot R_S \cdot G_{MLR}}$$

D. In order to assure that maximum voltage drive to the load is achievable, there are some precautions that should be taken. In a standard configuration, the B amplifier is slaved to the A amplifier. The bias point of the REFIN and the gain of the B amplifier, as well as the saturation voltages of the power output stages, will affect the voltage available to the load.

There are two simple procedures to follow, either will insure that the capabilities of the device are fully utilized. The first is to set the REFIN voltage at the center of the available voltage swing at the output of the power amplifiers. This optimum reference is defined by equation (3).

$$(3)\quad V_{REF}\ (\text{optimum}) = \frac{VIN - V_{HSsat} + V_{LSsat}}{2}$$

where: V_{HSsat} = high-side Vsat at maximum load
V_{LSsat} = low-side Vsat at maximum load.

A second approach is to raise the gain of the B amplifier to insure maximum swing. For a given REFIN voltage the gain of the B amplifier, set by the ratio of the feedback resistors, can be made greater than unity as given by:

$$(4)\quad A_{VB} = \frac{VIN - V_{HSsat} + V_{REF}}{V_{REF} - V_{LSsat}} \quad \text{or,}$$

$$\frac{V_{REF} - V_{LSsat}}{VIN - V_{HSsat} - V_{REF}}$$

APPLICATION INFORMATION (cont.)

whichever is greater than unity.

For a typical case, where V_{REF} has been set at VIN/2, the required gain for a 5 volt system will be about 1.5, and for a 12 volt system, 1.2.

It is worth noting that when using this method the B amplifier will saturate before the A amplifier on one polarity of the voltage swing. During the time when the B amplifier is saturated and the A amplifier is not, the small signal bandwidth of the loop will be reduced by a factor of (A_VB + 1).

E. The normal configuration for compensation of the power amplifier is shown in Figure 1. A simple RC network, R_CC_C, around the A amplifier is all that is required.

In the closed loop transconductance amplifier, the A amplifier operates at the highest noise gain. Noise gain is a measure of the feedback ratio at which the amplifier is operating. For the configuration of the A amplifier in Figure 1, the noise gain is given by the impedance ratio of the R_C-C_C series network, to the parallel combination of R_{FA} and R_{FB}. For the A amplifier to operate at its expected closed loop gain, the noise gain at any frequency must not exceed its Gain Bandwidth Product (GBW) divided by that frequency. Applying this to the expression above will yield a result for the maximum 3dB bandwidth that can be achieved for a given configuration.

$$(5)\ f_{3dBmax} = \left(\frac{f_{GBWA} \bullet (1+A_VB) \bullet A_VCS \bullet R_S \bullet R_{FA}}{2\pi L \bullet (R_{FA}+R_{FB})}\right)\frac{1}{2}$$

In the UC3172A, to accommodate wider power amplifier bandwidths, the f_{GBWA} has been extended to 3.5MHz.

The bandwidth of the closed loop amplifier can be set by choosing the value of R_C. Calculate R_C according to:

$$(6)\ R_C = \frac{2\pi L \bullet f_{3dB} \bullet R_{FB}}{(1 + A_VB)A_VCS \bullet R_S}$$

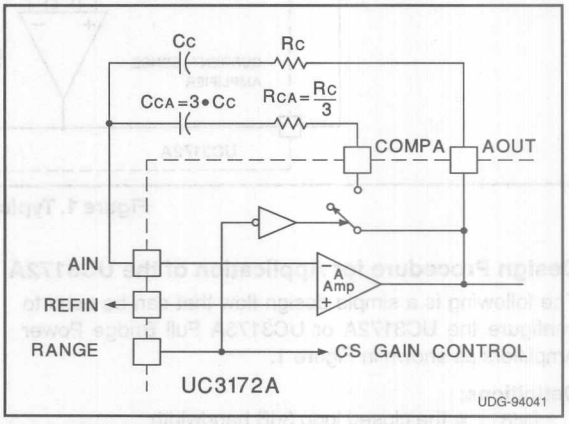
Use A_VCS = 0.5 if range changing is to be used, and A_VCS = 2.0 if only the low range mode of operation is to be used.

The compensation zero is typically set to coincide with the L/R time constant of the load. C_C can then be calculated by:

$$(7)\ C_C = \frac{L}{R_C(R_S + R_L)}$$

F. When the range change feature of the UC3172A is used, the closed loop bandwidth of the power amplifier will change according to (6). In other words, the bandwidth would be four times larger during the low range mode when A_VCS is equal to 2, than during the high range mode when A_VCS is equal to 0.5, unless the value of R_C is adjusted to compensate. The COMPA pin on the UC3172A can be used to do this. The COMPA pin acts as a simple switch that allows a parallel compensation network to be applied around the A amplifier during low range operation. A simple network as shown here will keep the loop response constant independent of the range condition.

To maintain the same 3dB bandwidth in both the high and low range modes set R_{CA} and C_{CA} to:



The COMPA pin switches in a parallel compensation network to stabilize the small signal bandwidth with range changes.

$$(8)\ R_{CA} = \frac{R_C}{3},\ C_{CA} = 3C_C$$

Head Parking

In Figure 2, the UC3172A is shown configured to force a programmed voltage at the A amplifier output upon the activation of a park condition. A pair of feedback resistors R1 and R2 set this voltage as defined by:

$$(9)\ R1 = R2\left(\frac{V_{PARK}}{1.3} - 1\right)$$

R2 is typically chosen in the range of 10kΩ to 100kΩ.

The B amplifier output is tri-stated during park, this side of the load is driven low by the PRKDRV pin. A series resistor, RP in the figure, can be inserted in series with the load to limit the peak current if required.

The UV thresholds for the supply monitors are set by picking R4 and R6 values in the 10kΩ to 100kΩ range and then calculating R3 and R5 according to:

APPLICATION INFORMATION (cont.)

(10) $R3 = R4\left(\frac{UV1}{1.3} - 1\right)$, and $R5 = R6\left(\frac{UV2}{1.3} - 1\right)$

During park, supply to the load, and the UC3172A, is typically recovered from the back EMF of the spindle motor. When the supply voltage at the VL supply pin drops below the UVLO voltage, (2.4V high-to-low), the output of the A amplifier is forced high, over-riding the programmed park voltage. The UC3172A will maintain drive to the load down to low supply levels. For example, with 1.5 volts of recovered back EMF, the UC3172A can still deliver 50mA of drive to a 10Ω load.

Parking With Very Low Back EMF

The UC3172A can also be configured to get parking drive to the load with very low recovered back EMF. Figure 3 illustrates how the PWROK pin can be used to drive an external PNP device to achieve very low parking drive Vsat losses. With this configuration, the UC3172A will be able to force approximately one volt across the load with a recovered back EMF voltage of 1.3V.

During system commanded parking with the supplies present, the VPARK pin is still used to set the maximum voltage to the load. The logic function of the PWROK pin is still available since the external PNP will provide isolation to this output when it is high.

Base drive to the PRKDRV and PWROK pins are provided by the VL supply pin. By using a hold up capacitor, CHOLD, the drive can be maintained to the load as the back EMF drops to below 1 volt. A variation on this approach is to add a connection between the VL pin and the recovered back EMF, this will eliminate the need for the holdup capacitor and provide operation down to about 1.2V of back EMF recovery. Care with this approach should be taken in case the 5V supply hangs at just below the programmed UV threshold. In this situation large currents could flow from this supply through the external PNP and into the A output which, until the supply

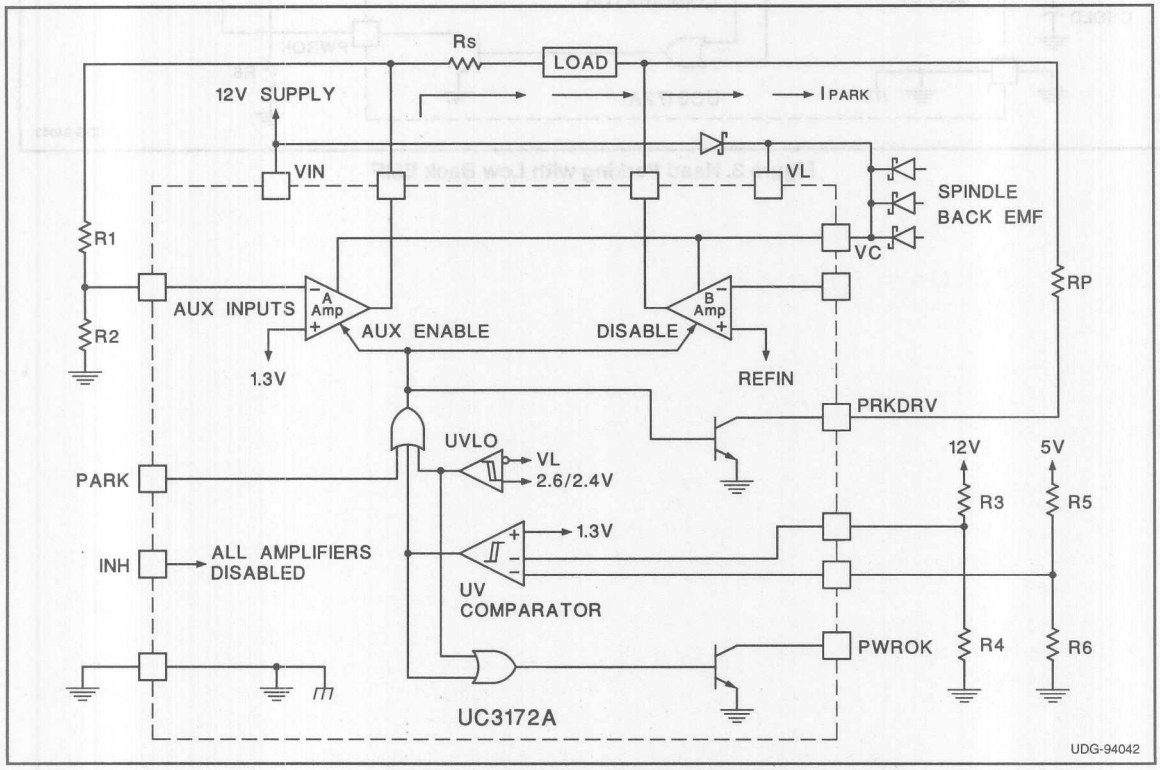


Figure 2. Controlled Velocity Head Parking

APPLICATION INFORMATION (cont.)

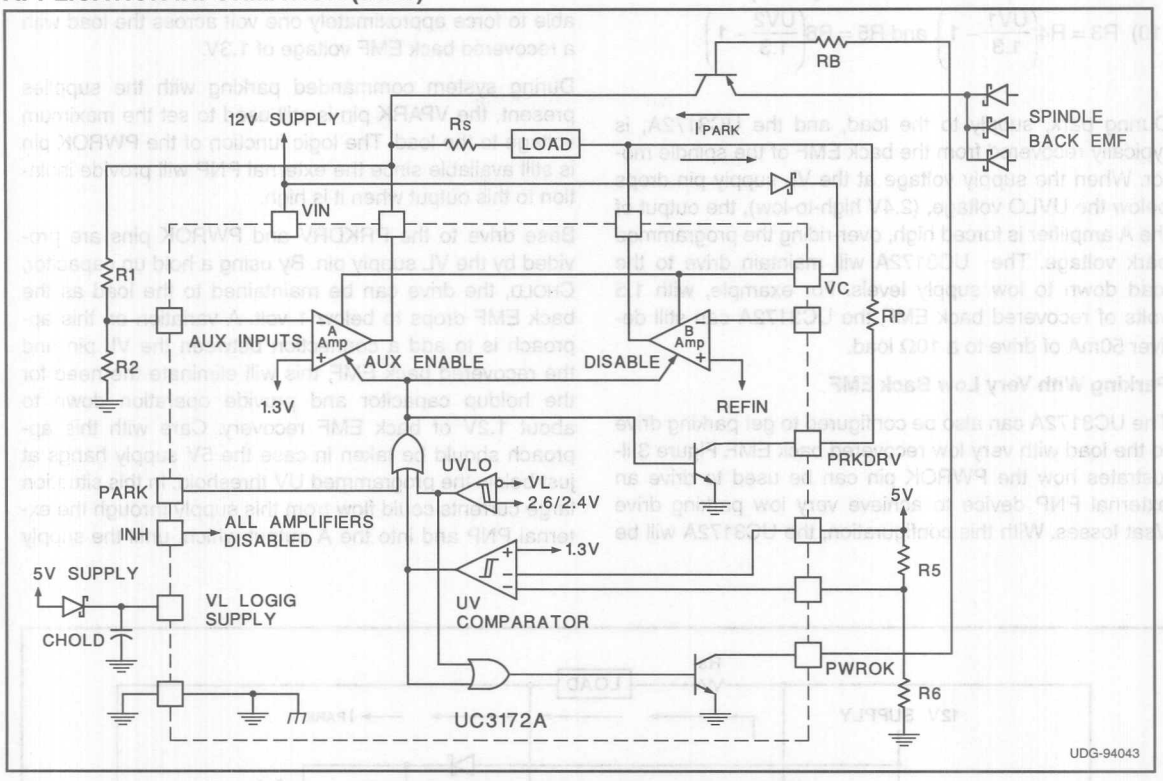


Figure 3. Head Parking with Low Back EMF

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

UNITRODE

Full Bridge Power Amplifier

FEATURES

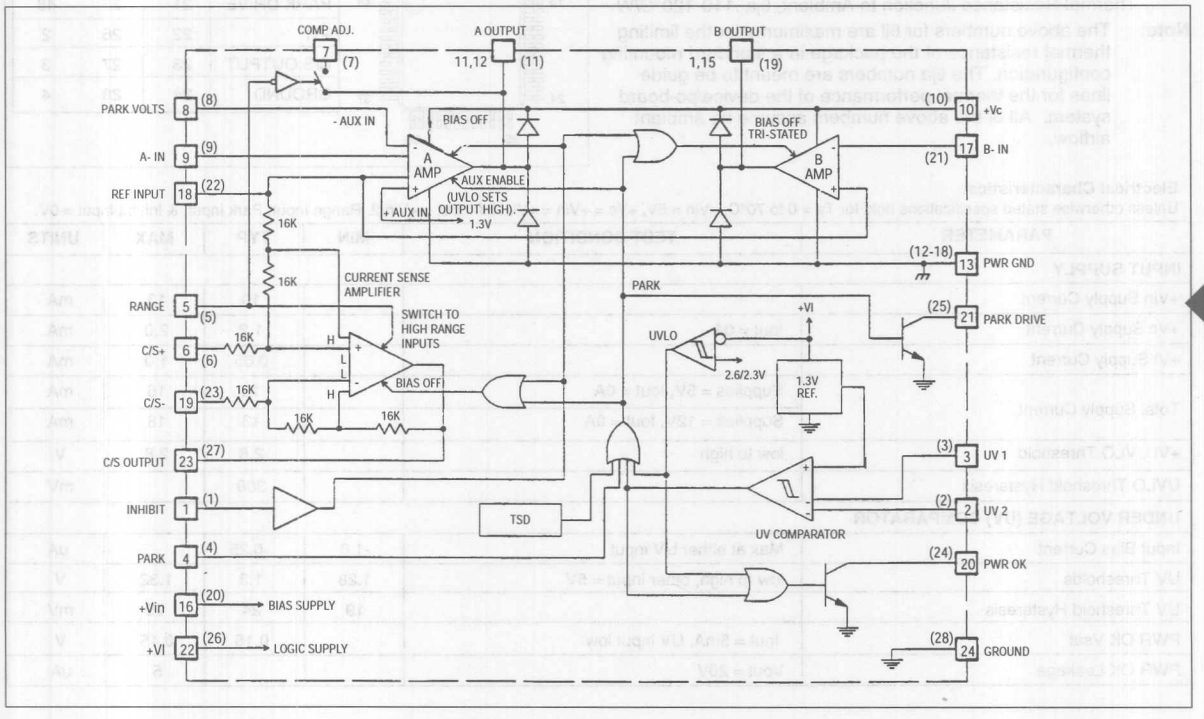
- Precision Current Control
- +/- 550mA Load Current
- 1.3V Typical Total Vsat at 550mA
- Controlled Velocity Head Parking
- Precision Dual Supply Monitor with Indicator
- Range Control for 4:1 Gain Change
- Compensation Adjust Pin for Bandwidth Control
- Inhibit Input and UVLO
- 5V or 12V Operation
- 12mA Quiescent Supply Current
- PLCC, SOIC, and Low Profile Quad Flat Pack Packages

DESCRIPTION

This full-bridge power amplifier, rated for continuous output current of 0.55 Amperes, is intended for use in demanding servo applications such as head positioning for high-density disk drives. This device includes a precision current sense amplifier that senses load current with a single resistor in series with the load. The UC3173A is optimized to consume a minimum of supply current, and is designed to operate in both 5V and 12V systems. The power output stages have a low saturation voltage and are protected with current limiting and thermal shutdown. When inhibited the device will draw less than 1.5mA of total supply current.

Auxiliary functions on this device include a dual-input under-voltage comparator, which can monitor two independent supply voltages and activate the built-in head park function when either is below minimum. The park circuitry allows a programmable retract voltage to be applied to the load for limiting maximum head velocity. A separate low-side parking drive pin permits a series impedance to be inserted to control maximum retract current. The parking drive function can be configured to operate with supply voltages as low as 1.2V.

The closed loop transconductance of the configured power amplifier can be switched between a high and low range with a single logic input. The 4:1 change in gain can be used to extend the dynamic range of the servo loop. Bandwidth variations that would otherwise result with the gain change can be controlled with a compensation adjust pin.



Pin numbers shown are for "DW" PKG., ( ) numbers are for "QP" PKG.

ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage, (+Vin, +Vc, +Vl).....20V
UV Comparator, Logic Inputs, and Ref Input
maximum forced voltage.....-0.3V to 10V
maximum forced current.....+/- 10mA
B Amplifier Inverting Input.....-0.3V to +Vin + 1.0V
A Amplifier Inverting Inputs,(Aux. and normal).-0.3Vto +Vc + 1.0V
Open Collector Output Voltages 20V
A and B Output Currents (continuous)
source .....Internally Limited
sink 0.6A
Parking Drive Output Current
continuous 150mA
pulsed 1A
Output Diode Current (pulsed) 0.6A
Power OK Output Current(continuous) 30mA
Operating Junction Temperature .....- 55°C to +150°C
Storage Temperature .....- 65°C to +150°C

Note 1: Unless otherwise indicated, voltages are reference to ground and currents are positive into, negative out of, the specified terminals, "Pulsed" is defined as a less than 10% duty cycle pulse with a maximum duration of 500uS.

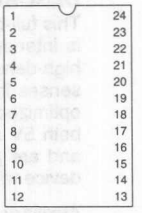
THERMAL DATA

QP package: (see packaging section of UICC data book for more details on thermal performance)
Thermal Resistance Junction to Leads, θjl .....15°C/W
Thermal Resistance Junction to Ambient, θja....30°-40°C/W
DW package:
Thermal Resistance Junction to Leads, θjl ..... 35°C/W
Thermal Resistance Junction to Ambient, θja....60°-70°C/W
FQ package:
Thermal Resistance Junction to Leads, θjl .....60°C/W
Thermal Resistance Junction to Ambient, θja .110-120°C/W

Note: The above numbers for θjl are maximums for the limiting thermal resistance of the package in a standard mounting configuration. The θja numbers are meant to be guide lines for the thermal performance of the device/pc-board system. All of the above numbers assume no ambient airflow.

CONNECTION DIAGRAMS

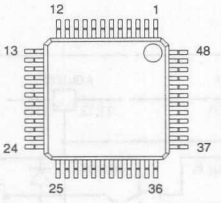
SOIC - 24 (TOP VIEW)
DW PACKAGE



PLCC-28 (TOP VIEW)
QP PACKAGE



TQFP-48 (TOP VIEW)
FQ PACKAGE



PACKAGE PIN FUNCTIONS

FUNCTION	DW	QP	FQ
INHIBIT	1	1	9
UV 2	2	2	10
UV 1	3	3	11
PARK	4	4	12
RANGE	5	5	13
C/S+	6	6	14
COMP ADJ	7	7	15
PARK VOLTS	8	8	16
A- IN	9	9	21
+Vc	10	10	22
A OUTPUT	11,12	11	26, 27
POWER GND	13	12-18	30, 31
B OUTPUT	14,15	19	34, 35
+Vin	16	20	39
B- IN	17	21	40
REF INPUT	18	22	45
C/S-	19	23	46
PWR OK	20	24	47
PARK DRIVE	21	25	48
+Vl	22	26	2
C/S OUTPUT	23	27	3
GROUND	24	28	4

Electrical Characteristics:
Unless otherwise stated specifications hold for Ta = 0 to 70°C, +Vin = 5V, +Vc = +Vin = +Vl, Ref Input = +Vin/2, Range Input, Park Input, & Inhibit Input = 0V.

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
INPUT SUPPLY					
+Vin Supply Current			10	13	mA
+Vc Supply Current	Iout = 0A		1.2	2.0	mA
+Vl Supply Current			0.65	1.0	mA
Total Supply Current	Supplies = 5V, Iout = 0A		12	16	mA
	Supplies = 12V, Iout = 0A		13	18	mA
+Vl UVLO Threshold	low to high		2.6	2.8	V
UVLO Threshold Hysteresis			300		mV
UNDER VOLTAGE (UV) COMPARATOR					
Input Bias Current	Max at either UV input	-1.0	-0.25		uA
UV Thresholds	low to high, other input = 5V	1.28	1.3	1.32	V
UV Threshold Hysteresis		19	24	29	mV
PWR OK Vsat	Iout = 5mA, UV input low		0.15	0.45	V
PWR OK Leakage	Vout = 20V			5	uA

Electrical Characteristics (Continued):
Unless otherwise stated specifications hold for Ta = 0 to 70°C, +Vin = 5V, +Vc = +Vin = +VI, Ref Input = +Vin/2, Range Input, Park Input, & Inhibit Input = 0V.

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
POWER AMPLIFIERS A AND B					
Input Offset Voltage	A Amplifier, Vcm = 2.5V			4	mV
	B Amplifier, Vcm = 2.5V			12	mV
Input Bias Current	Vcm = 2.5V, Inverting inputs only	-500	-150		nA
Input Bias Current at Ref. Input	(Ref. Input - C/S+)/48Kohms, Tj = 25°C	15	21	27	uA/V
CMRR	Vcm = 1 to 10V, Supplies = 12V	70	90		dB
PSRR	+Vin = 4 to 15V, Vcm = 1.5V	70	90		dB
Large Signal Voltage Gain	Supplies = 12V, Vout = 1V, Iout = 300mA to Vout = 11V, Iout = -300mA	3.0	15.0		V/mV
Gain Bandwidth Product	Note 1, A Amplifier		2.0		MHz
	Note 1, B Amplifier		1.0		MHz
Slew Rate	Note 1		1.0		V/uS
High-Side Current Limit		0.55	0.6		A
Output Saturation Voltage	High-Side, Iout = -100mA, Note 2		0.7		V
	High-Side, Iout = -300mA, Note 2		0.8		V
	High-Side, Iout = -550mA, Note 2		0.95		V
	Low-Side, Iout = 100mA		0.2		V
	Low-Side, Iout = 300mA		0.25		V
	Low-Side, Iout = 550mA		0.35		V
	Total Vsat, Iout = 100mA		0.9	1.2	V
	Total Vsat, Iout = 300mA		1.05	1.4	V
	Total Vsat, Iout = 550mA		1.3	1.7	V
+Vc to +Vin Headroom	Volts below +Vin, delta High-Side Vsat = 100mV, Iout = -550mA, Note 2	0.23	0.4		V
High-Side Diode, Vf	Id = 550mA		1.0		V
Low-Side Diode, Vf	Id = 550mA, Inhibit activated, B amplifer only		1.0		V
CURRENT SENSE AMPLIFIER					
Input Offset Voltage	Vcm = 2.5V, Low range mode			2.0	mV
	High range mode			4.0	mV
Input Offset Change with Common Mode Input	Vcm = -1V to 13V, Supplies = 12V Low Range Mode			2000	uV/V
	High Range Mode			4000	uV/V
Voltage Gain	Vdiff = +1.0 to -1.0V, Vcm = 2.5V High range mode	0.485	0.50	0.515	V/V
	Low range mode	1.95	2.0	2.05	V/V
Saturation Voltage	Low-Side, Iout = 1mA,		0.1	0.3	V
	High-Side, Iout = -1mA, Referenced to +Vin		0.1	0.3	V
PARKING FUNCTION					
Park Input Threshold Voltage		0.6	1.1	1.7	V
Park Input Threshold Current	Internal pull-up, Vin = 0.6V		50	75	uA
Park Drive Saturation Voltage	Iout = 50mA		0.15	0.35	V
Park Drive Leakage	Vout = 20V			50	uA
Regulating Voltage at Park Volts Input		1.275	1.30	1.325	V

Note 1: This specification not tested in production

Note 2: The high-side saturation performance of the UC3173A is referenced to the +Vin supply pin. The +Vc suppy pin can operate slightly below the +Vin supply input, about 400 mV, without affecting this performance.

Electrical Characteristics (Continued):
Unless otherwise stated specifications hold for Ta = 0 to 70°C, +Vin = 5V, +Vc = +Vin = +Vl, Ref Input = +Vin/2, Range Input, Park Input, & Inhibit Input = 0V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
PARKING FUNCTION (CONTINUED)					
Amplifier A Auxiliary Input Bias Current		-750	-300		nA
Amplifier A Parking High-Side Saturation Voltage	Iout = -50mA, +Vin = 0V, +Vc = +Vl = 5V, Park Input Open, +Vc to Vout		0.8	0.95	V
Minimum Parking Supply	At +Vc and +Vl, +Vin = 0V, A Amplifier out - Vsat Parking Drive>0.5V Ipark = 50mA		1.4	1.7	V
Minimum Supply for Parking Drive and Power OK Operation	At +Vl, +Vc = +Vin = 0V, Vsats < 0.5V, Iout Parking Drive = 50mA, Rl = 30ohms to 2V		1.1	1.4	V
	Iout Power OK = 5mA, Rl = 300ohms to 2V		1.2	1.6	V
+Vl Parking Supply Current	Park Input Open, +Vl = 5V, +Vc = 1.6V, +Vin = 0V Power OK Iout = 5mA, Parking Drive Iout = 50mA		1.6	3.0	mA
AUXILIARY FUNCTIONS					
Inhibit Input Threshold		0.6	1.1	1.7	V
Inhibit Input Current	Inhibit Input = 1.7V	-1.0	-0.5		uA
Range Input Threshold		0.6	1.1	1.7	V
Range Input Current	Range Input = 1.7V		50	100	uA
Comp Adjust Pin Saturation Voltage	Range Input = 0V, Pin Current = +/-500uA Referenced to Aout		0.02	0.1	V
Comp Adjust Leakage Current	Range Input = 1.7V, Supplies = 12V Aout-V Comp Adj = +/-6V			5	uA
Total Supply Current when Inhibited	+Vin, +Vc, and +Vl currents		1.0	1.5	mA
Thermal Shutdown Temperature	Note 1		165		°C

Note 1: This specification not tested in production

PIN FUNCTIONAL DESCRIPTION

+Vin Provides bias supply to both the power amplifiers and the current sense amplifiers. The high-side drive to the power stages on both the A and B amplifiers is referenced to this pin. The high-side saturation voltages are specified and measured with respect to this supply pin. The parking function of the device is fully operational independent of the voltage at this pin.

+Vc +Vc supply pin is the high current supply to the collectors of the high-side NPN output devices on the A and B amplifiers. This supply should be powered whenever the A, or B amplifiers are to be activated. This pin can operate approximately 400mV below the +Vin supply without affecting the voltage available to the load. This supply pin provides drive to the power amplifiers during a parking operation.

+Vl Logic portions of the UC3173A are powered by this supply pin, including the reference, UVLO, the UV comparators, and the PARKING DRIVE and POWER OK outputs. This pin is a low current supply that would normally be tied to the +Vc pin, or to a parking hold-up capacitor for extended parking operation with very low recovered back-emf.

GND Reference point for the internal reference, UV comparator, and other low-level circuitry.

PWR GND Current return for all high level circuitry, this pin should be connected to the same potential as **GND**.

A Out Output for the A power amplifier, providing one end of the differential drive to the load during normal operation, and during park. During a UVLO condition at the +Vin supply pin, this output is forced to a high, source only state.

B Out Output for the B power amplifier, providing one end of the differential drive to the load during normal operation. During park and while inhibited this pin is tri-stated.

A- In Inverting input to the A amplifier. Used as the summing node to close the loop on the overall power amplifier.

B- In Inverting input to the B amplifier. Used to program the gain of the B amplifier to guarantee maximum voltage swing to the load.

Ref Input Reference for input control signals to the power amplifier, as well as, the non-inverting inputs to the A and B amplifiers, and the output level shift for the C/S amplifier.

C/S+ The non-inverting input to the current sense amplifier is typically tied to the load side of the series current sense resistor. This pin can be pulled below ground during an abrupt load current change with an inductive load. Proper operation of the current sense amplifier will result if this pin does not go below ground by an amount greater than:

Ref Input / 2 - 0.3V, in low range mode, and
2 • **Ref Input** - 0.9V, in high range mode.

PIN FUNCTIONAL DESCRIPTION (CONTINUED)

C/S- The inverting input to the current sense amplifier is typically tied to the connection between the B amplifier output and the current sense resistor that is in series with the load.

C/S Output The output of the current sense amplifier has a 1.5mA current source pull-up and an active NPN pull-down. The output will pull to within 0.3V of either rail with a load current of less than 1mA.

Range When this pin is open or at a logic **low** potential, the current sense amplifier will be in its low range mode. In this mode the voltage gain of the amplifier will be 2. If this pin is brought to a logic **high**, the gain of the current sense amplifier will change into its **high** range value of 0.5. This factor of four change in gain will vary the overall transconductance of the power amplifier by the same ratio, with the transconductance being the highest in the high mode. This feature allows improved dynamic range of load current control for a given control input range and resolution.

Comp Adj The compensation adjust pin allows the user to provide an auxiliary compensation network for the A amplifier that is only active when the current sense amplifier is in the low range. With this option, the user can control the change in bandwidth that would otherwise result from the gain change in the feedback loop.

UV 1 & 2 Inputs to the UV comparator, these inputs are high impedance sensing points used to monitor external supply conditions. Either of the inputs going low will force the device into a park condition, and force the **Power OK** output to an active low state. If either of these inputs is not used it should be connected to a voltage greater than 1.3V.

Power OK Indicates with an active low condition that either of the **UV** inputs are low, or that the supply voltage at the **+VI** input to the UC3173A has dropped below the UVLO threshold. This output will remain active low until the **+VI** supply has dropped to below approximately 1.2V.

Park Volts The auxiliary inverting input to the A amplifier, activated during park conditions on the UC3173A. An internal auxiliary non-inverting input is connected to the 1.3V reference. When the auxiliary inputs are activated, the A amplifier will force a programmed voltage at its output for a maximum back-emf/velocity retract of the head. The park condition on the UC3173A is **always** activated by any one of the following four conditions, 1: a low condition on either of the **UV** inputs, 2: a high input level at the **Park** input, 3: a UVLO condition at the **+VI** supply pin, and 4: activation of the **TSD**, (thermal shutdown) protection circuit. During a UVLO condition at the **+VI** pin the auxiliary inputs to the A amplifier are over-ridden, and the A amplifier output is forced to its high state.

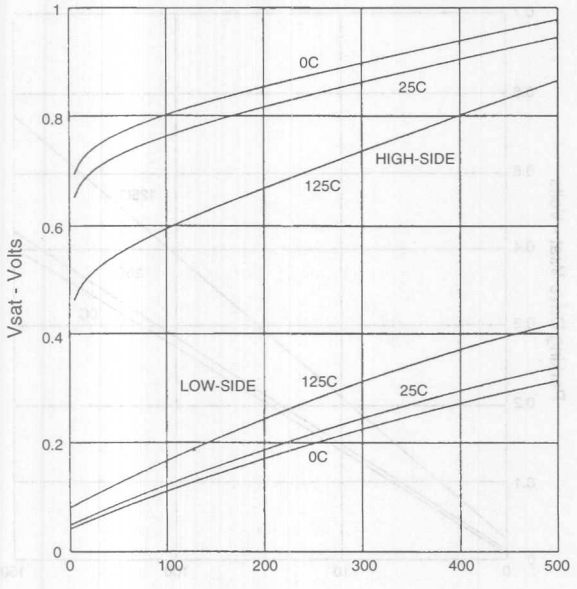
Park Logic input that forces the park condition on the UC3173A. This input has an internal pull-up that will force the park condition if the pin is left open.

Park Drive A 100mA drive output that is active low during a park operation. This pin is normally used to supply the low-side drive to the load during parking, in place of the B amplifier. A series resistor can be added between this pin and the load to limit current during park.

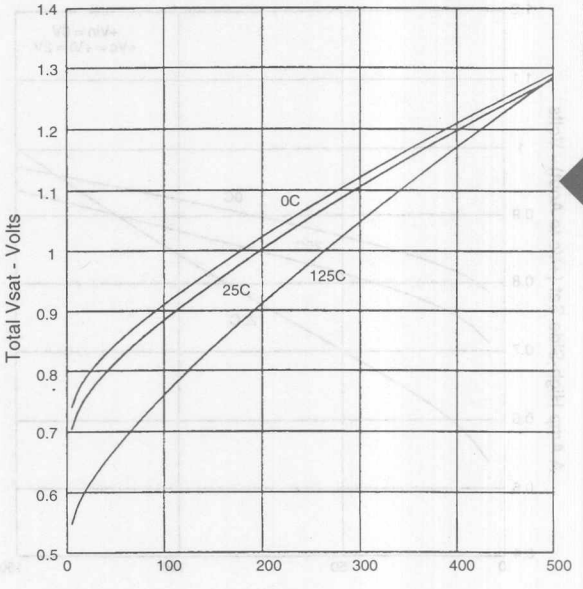
Inhibit A high impedence logic input that disables the A and B power amplifiers, as well as the Current Sense amplifier. The UV comparators and logic functions of the UC3173A remain active. This input has an internal pull-up that will inhibit the device if the input is left open. The **Inhibit** function is over-ridden by any condition that forces the park function to be activated.

CHARACTERISTIC CURVES

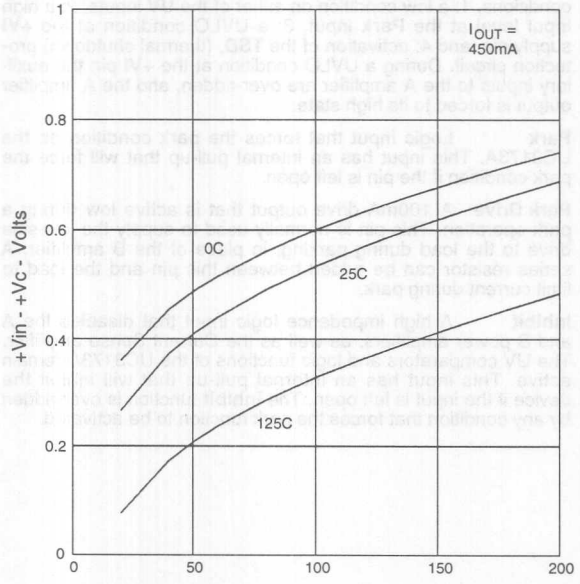
A AND B AMPLIFIER HIGH AND LOW VSATS



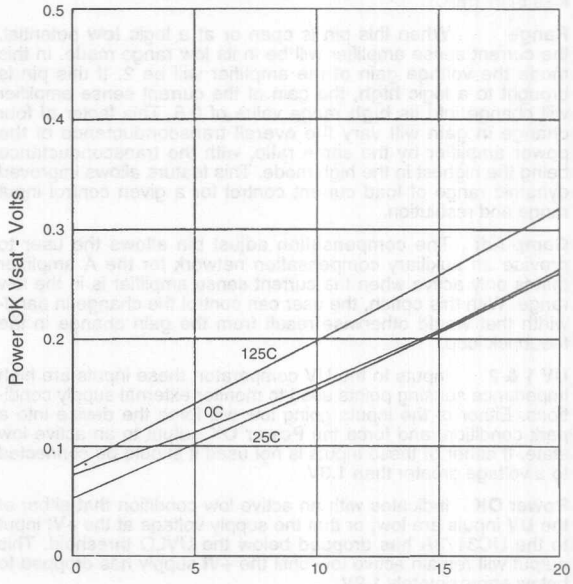
A AND B AMPLIFIER TOTAL VSAT



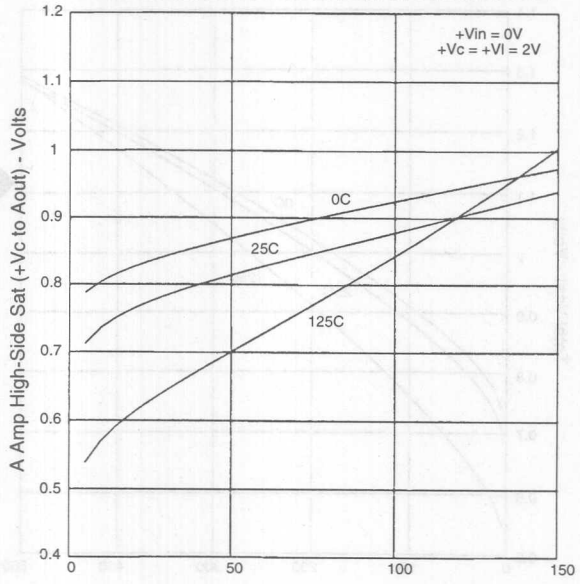
+Vin TO +Vc HEADROOM



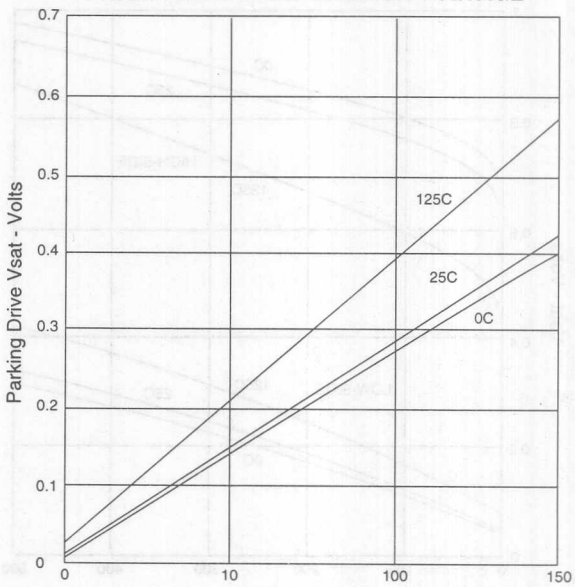
POWER OK SATURATION VOLTAGE



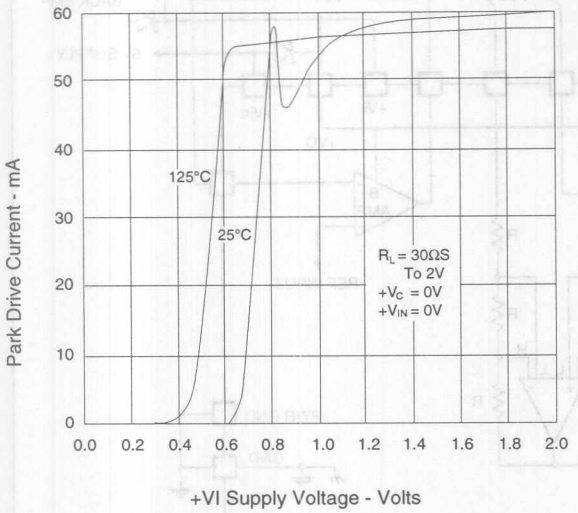
A AMPLIFIER HIGH-SIDE Vsat IN PARK MODE



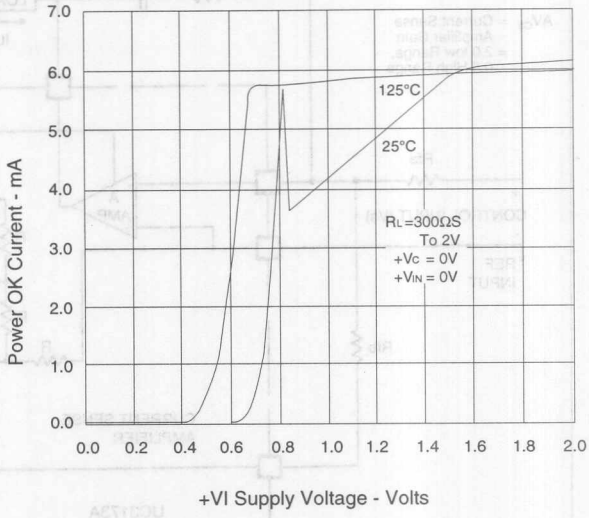
PARKING DRIVE SATURATION VOLTAGE



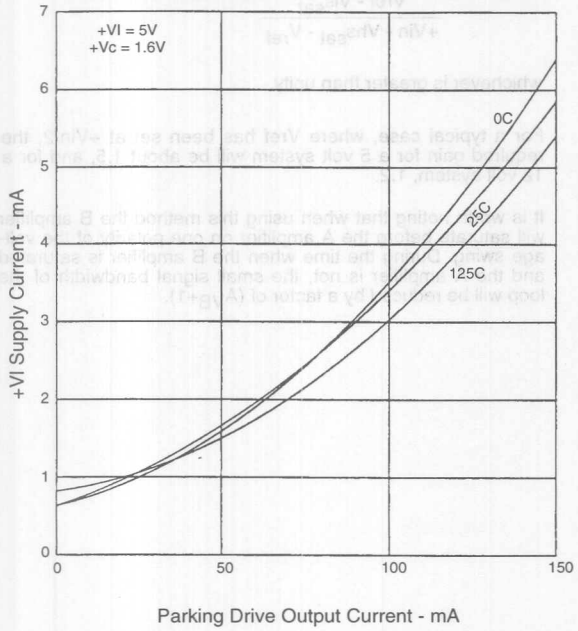
PARK DRIVE CURRENT vs. +VI SUPPLY



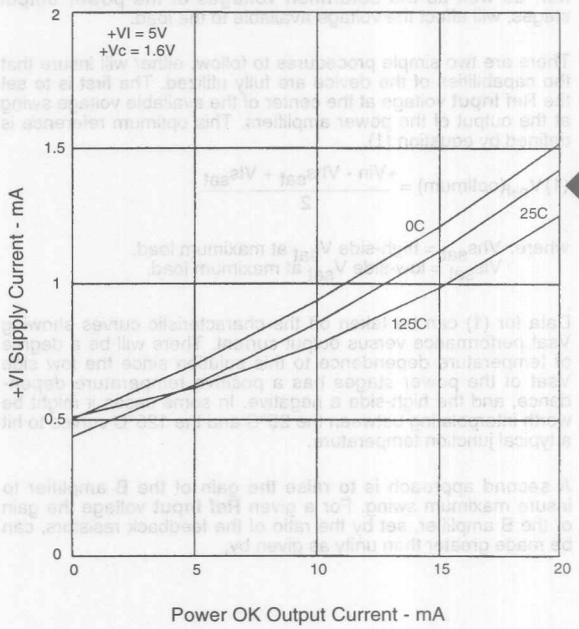
POWER OK CURRENT vs. +VI SUPPLY



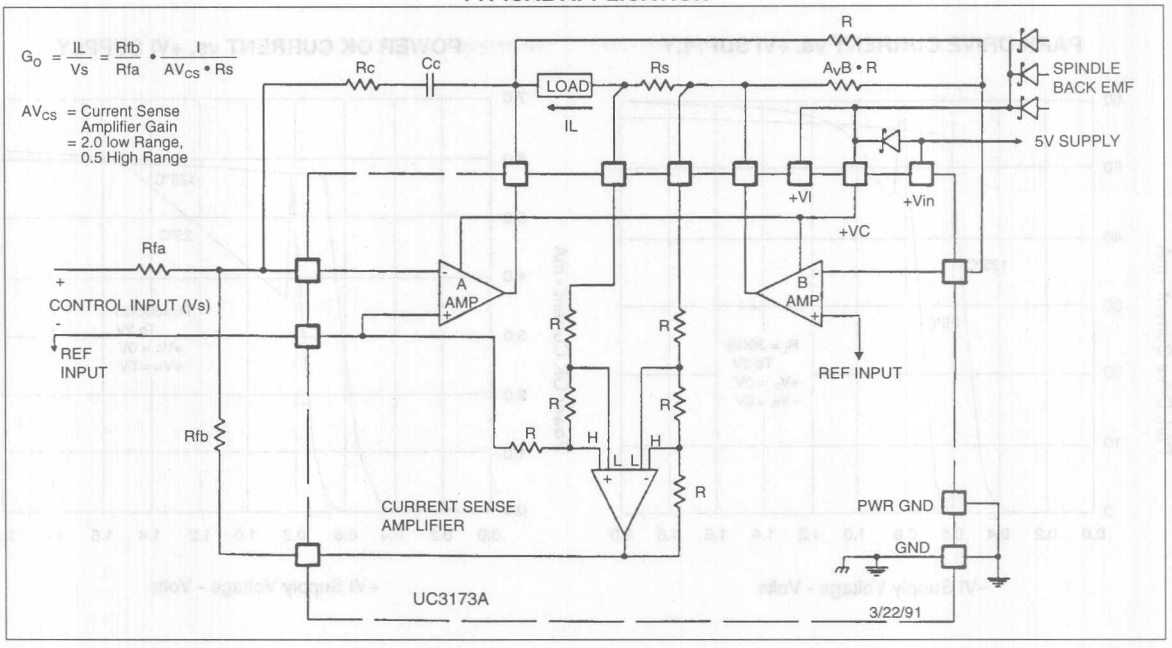
+VI CURRENT VERSUS PARK DR CURRENT



+VI CURRENT VERSUS PWR OK CURRENT



TYPICAL APPLICATION



Maximizing the Voltage to the Load

In order to assure that maximum voltage drive to the load is achievable there are some precautions that should be taken. In a standard configuration, the B amplifier is slaved to the A amplifier. The bias point of the **Ref Input** and the gain of the B amplifier, as well as the saturation voltages of the power output stages, will affect the voltage available to the load.

There are two simple procedures to follow, either will insure that the capabilities of the device are fully utilized. The first is to set the **Ref Input** voltage at the center of the available voltage swing at the output of the power amplifiers. This optimum reference is defined by equation (1).

$$(1)\ V_{ref}(optimum) = \frac{+Vin - Vhs_{sat} + Vls_{sat}}{2}$$

where: Vhs_{sat} = high-side V_{sat} at maximum load.
Vls_{sat} = low-side V_{sat} at maximum load.

Data for (1) can be taken off the characteristic curves showing Vsat performance versus output current. There will be a degree of temperature dependence to this solution since the low side Vsat of the power stages has a positive temperature dependence, and the high-side a negative. In some cases it might be worth interpolating between the 25°C and the 125°C curves to hit a typical junction temperature.

A second approach is to raise the gain of the B amplifier to insure maximum swing. For a given **Ref Input** voltage the gain of the B amplifier, set by the ratio of the feedback resistors, can be made greater than unity as given by,

$$(2)\ A_{VB} = \frac{+Vin - Vhs_{sat} - V_{ref}}{V_{ref} - Vls_{sat}}$$

or,

$$\frac{Vref - Vls_{sat}}{+Vin - Vhs_{sat} - V_{ref}}$$

whichever is greater than unity.

For a typical case, where Vref has been set at +Vin/2, the required gain for a 5 volt system will be about 1.5, and for a 12 volt system, 1.2.

It is worth noting that when using this method the B amplifier will saturate before the A amplifier on one polarity of the voltage swing. During the time when the B amplifier is saturated and the A amplifier is not, the small signal bandwidth of the loop will be reduced by a factor of (A_{VB}+1).

Setting and Maximizing the Loop Bandwidth

The normal configuration for compensation of the power amplifier is shown in the ***Typical Application*** drawing. A simple RC network. RcCc time constant is typically chosen to correspond to the electrical time constant of the load, given by Rl/L. Where Rl is the total load and sense resistanace between the bridge outputs, and L is the load inductance.

The 3dB frequency(f_{3dB}) of the closed loop amplifier is given by the following expression:

$$(3)\, f_{3dB} = \frac{(1 + A_VB) \bullet A_VCS \bullet Rs \bullet Rc}{2\pi L \bullet Rfb}$$

assuming $f_{3dB} >> (2\pi Rc \bullet Cc)^{-1}$

where: A_VB is the voltage gain of the B amplifier.
A_VCS is the CS amplifier voltage gain.

In the closed loop transconductance amplifier, the A amplifier operates at the highest noise gain. Noise gain is a measure of the feedback ratio at which the amplifier is operating. For the configuration of the A amplifier in the typical application drawing, the noise gain is given by the impedance ratio of the Rc-Cc series network, to the parallel combination of Rfa and Rfb. For the A amplifier to operate at its expected closed loop gain, the noise gain at any frequency must not exceed its Gain Bandwidth Product(GBW) divided by that frequency. Applying this to the expression above will yield a result for the maximum 3dB bandwidth that can be achieved for a given configuration.

$$(4)\, f_{3dBmax} = \left(\frac{f_{gbw}A \bullet (1+A_VB) \bullet A_VCS \bullet Rs \bullet Rfa}{2\pi L \bullet (Rfa + Rfb)}\right)^{1/2}$$

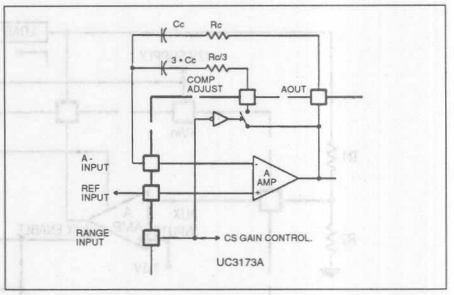
where: $f_{gbw}A$ is the GBW of the A amplifier.

In the UC3173A, to accommodate wider power amplifier bandwidths, the GBW Product of the A amplifier has been extended to 2MHz. A loop compensated in this manner will have a second order closed response with the poles split around the 3dB frequency given in (3). The loop phase margin will be approximately 45°. The value of Rc required to set the above conditions is given by

$$(5)\, Rc_{max} = Rfb \bullet \left(\frac{f_{gbw}A \bullet 2\pi L \bullet Rfa}{(A_VB + 1) \bullet A_VCS \bullet Rs \bullet (Rfa + Rfb)}\right)^{1/2}$$

Range Change Bandwidth Control

When the range change feature of the UC3173A is used the closed loop bandwidth of the power amplifier will change according to (3). In other words, the bandwidth would be four times larger during the low range mode when AVCS is equal to 2, than during the high range mode when AVCS is equal to 0.5, unless the value of Rc is adjusted to compensate. The **Comp Adjust** pin on the UC3173A can be used to do this. The **Comp Adjust** pin acts as a simple switch that allows a parallel compensation network to be applied around the A amplifier during low range operation. A simple network as shown here will keep the loop response constant independent of the range condition.



The Comp Adjust pin switches in a parallel compensation network tostabilize the small signal bandwidth with range changes.

Head Parking

In the application figure, ***Controlled Velocity Head Parking,*** the UC3173A is shown configured to force a programmed voltage at the A amplifier output upon the activation of a park condition. A pair of feedback resistors R1 and R2 set this voltage as defined by

$$(6)\, V_{park} = 1.3 \bullet \left(1 + \frac{R1}{R2}\right)$$

The B amplifier output is tri-stated during park, this side of the load is driven low by the **Park Drive** pin. A series resistor, Rp in the figure, can be inserted in series with the load to limit the peak current if required.

During park, supply to the load, and the UC3173A, is typically recovered from the back EMF of the spindle motor. When the supply voltage at the **+Vl** supply pin drops below the UVLO voltage,(2.3V high-to-low), the output of the A amplifier is forced high, over-riding the programmed park voltage. The UC3173A will maintain drive to the load down to low supply levels. For example, with 1.5 Volts of recovered back EMF, the UC3173A can still deliver 50mA of drive to a 10 ohm load.

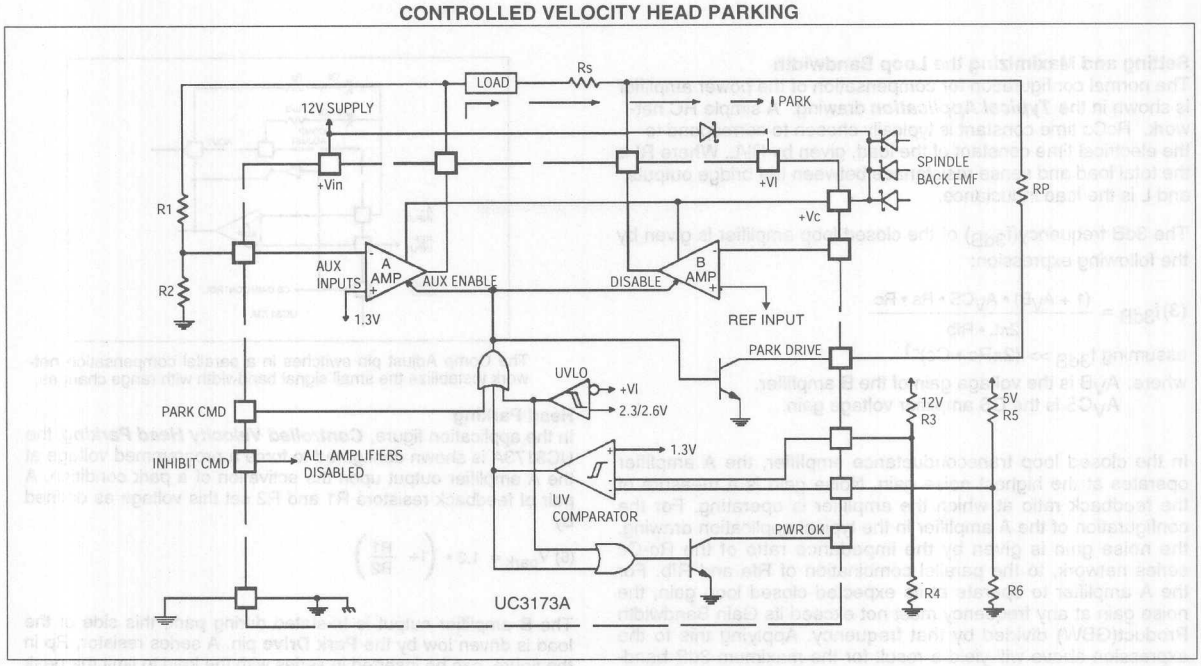
Parking With Very Low Back EMF

The UC3173 can also be configured to get parking drive to the load with very low recovered back EMF. The figure titled ***Head Parking with Low Back EMF*** illustrates how the **Power OK** pin can be used to drive an external PNP device to achieve very low parking drive Vsat losses. With this configuration, the UC3173A will be able to force approximately one volt across the load with a recovered back EMF voltage of 1.3V.

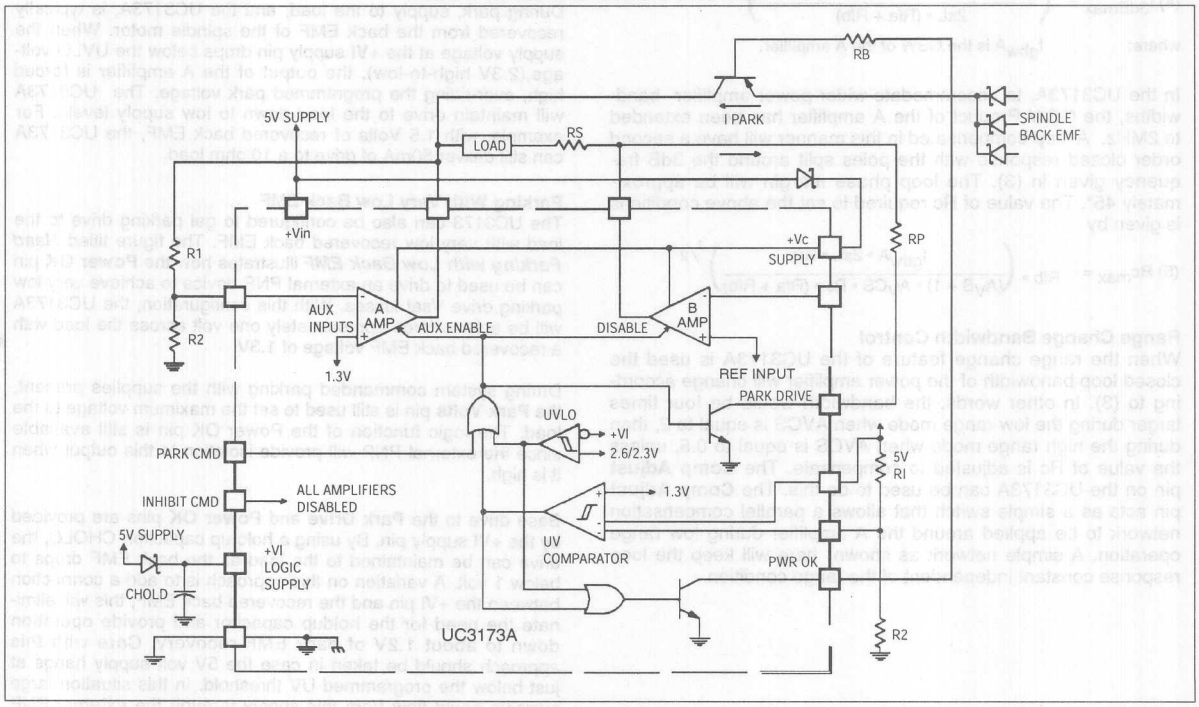
During system commanded parking with the supplies present, the **Park Volts** pin is still used to set the maximum voltage to the load. The logic function of the Power OK pin is still available since the external PNP will provide isolation to this output when it is high.

Base drive to the **Park Drive** and **Power OK** pins are provided by the **+Vl** supply pin. By using a hold up capacitor, CHOLD, the drive can be maintained to the load as the back EMF drops to below 1 volt. A variation on this approach is to add a connection between the +Vl pin and the recovered back EMF, this will eliminate the need for the holdup capacitor and provide operation down to about 1.2V of back EMF recovery. Care with this approach should be taken in case the 5V volt supply hangs at just below the programmed UV threshold. In this situation large currents could flow from this supply through the external PNP and into the A output which, until the supply drops below a certain level, is forcing a programmed voltage.

CONTROLLED VELOCITY HEAD PARKING



HEAD PARKING WITH LOW BACK EMF



UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

UNITRODE

Full-Bridge Power Amplifier

FEATURES

- Precision Current Control
- ±800mA Load Current
- 1.25V Total VSAT at 800mA
- Controlled Velocity Head Parking
- Precision Dual Supply Monitor with Indicator
- Limit Input to Force Output Extremes
- Inhibit Input and UVLO
- 4V to 15V Operation

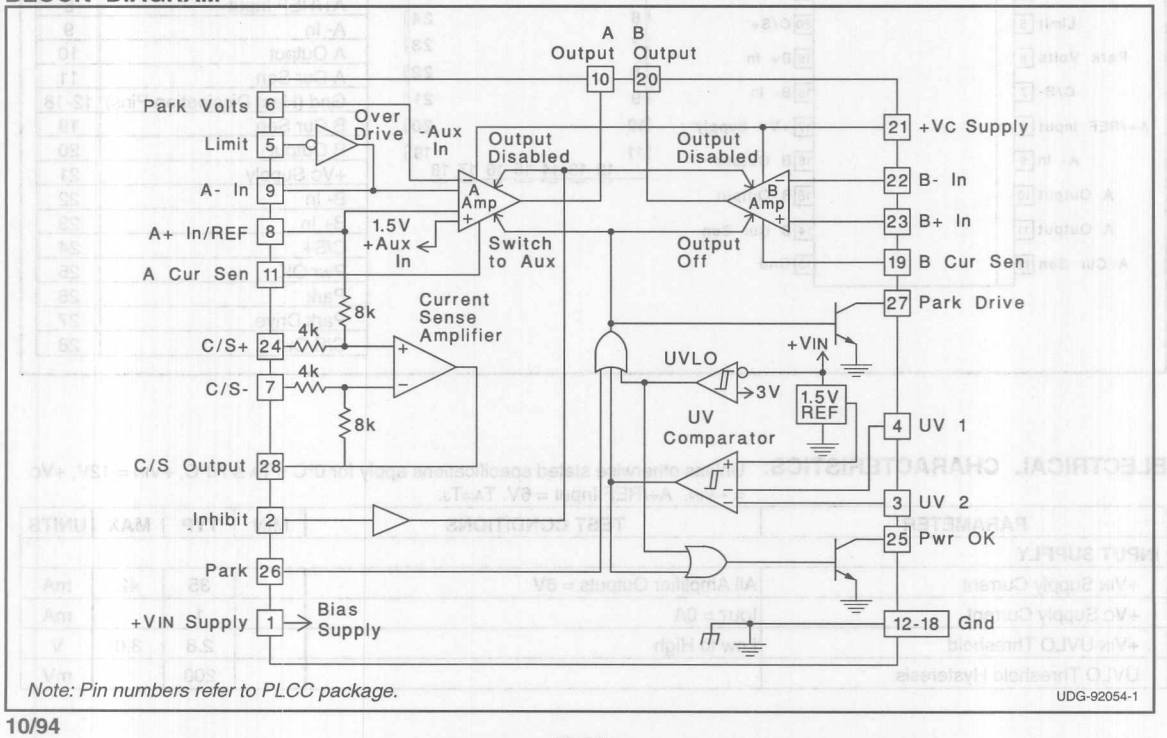
DESCRIPTION

This full-bridge power amplifier is rated for continuous output current of 0.8 Amperes and is intended for use in demanding servo applications such as head positioning for high-density disk drives. The device includes a precision current sense amplifier that provides accurate control of load current. Current is sensed with a single resistor in series with the load. The power amplifier has a very low output saturation voltage and will operate down to 4V supply levels. Power output stage protection includes current limiting and thermal shutdown.

Auxiliary functions on this device include a dual-input under-voltage comparator, which can monitor two independent supply voltages and force a built-in head park function when either is below minimum. When activated by either the UV comparator, or a command at the separate PARK input, the park circuitry will override the amplifier inputs to convert the power outputs to a programmable constant voltage source which will hold regulation as the supply voltage falls to below 3.0 Volts. Added features include a POWER OK flag output, a LIMIT input to force the drive output to its maximum level in either polarity, and a overriding INHIBIT input to disable all amplifiers and reduce quiescent supply current.

This device is packaged in a power PLCC surface mount configuration which maintains a standard 28-pin outline, but with 7 pins along one edge allocated to ground for optimum thermal transfer. And is also available in a 24-pin surface mount SOIC package.

BLOCK DIAGRAM



Note: Pin numbers refer to PLCC package.

UDG-92054-1

ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage, (+VIN,+VC) 20V
UV Comparator, and Digital Inputs
  Maximum forced voltage . . . . . -0.3V to 10V
  Maximum forced current . . . . . ±10mA
C/S Inputs
  Maximum forced voltage . . . . . -0.3V to 20V
  A and B Amplifier Inputs . . . . . -0.3V to +VIN
Open Collector Output Voltages. 20V
A and B Output Currents (continuous)
  Source . . . . . Internally Limited
  Sink 1.0A
Parking Drive Output Current
  Continuous 150mA
  Pulsed 1A
Output Diode Current (pulsed) 1A
Power OK Output Current(continuous) 30mA
Operating Junction Temperature . . . . . -55°C to +150°C
Storage Temperature . . . . . -65°C to +150°C

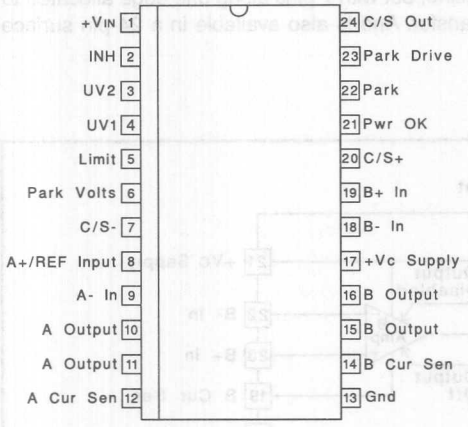
Note 1: Unless otherwise indicated, voltages are referenced to ground and currents are positive into, negative out of, the specified terminals. "Pulsed" is defined as a less than 10% duty cycle pulse with a maximum duration of 500µs.
Note 2: See Unitrode Integrated Circuits databook for information regarding thermal specifications and limitations of packages.

Thermal Data

QP Package:
Thermal Resistance Junction to Leads,
  θJL . . . . . 15°C/W
Thermal Resistance Junction to Ambient,
  θJA . . . . . 40°C/W

CONNECTION DIAGRAMS

SOIC-24 (Top View)
DW Package



PLCC-28 (Top View)
QP Package



PACKAGE PIN FUNCTION	
FUNCTION	PIN
+VIN	1
INH	2
UV2	3
UV1	4
Limit	5
Park Volts	6
C/S-	7
A+/REF Input	8
A- In	9
A Output	10
A Cur Sen	11
Gnd (Heat Dissipation Pins)	12-18
B Cur Sen	19
B Output	20
+Vc Supply	21
B- In	22
B+ In	23
C/S+	24
Pwr OK	25
Park	26
Park Drive	27
C/S Out	28

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated specifications apply for 0°C ≤ TA ≤ 70°C, +VIN = 12V, +VC = +VIN, A+/REF Input = 6V. TA=TJ.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY					
+VIN Supply Current	All Amplifier Outputs = 6V		35	42	mA
+VC Supply Current	IOUT = 0A		1		mA
+VIN UVLO Threshold	Low to High		2.8	3.0	V
UVLO Threshold Hysteresis			200		mV

ELECTRICAL CHARACTERISTICS (cont.) Unless otherwise stated specifications apply for 0°C ≤ T_A ≤ 70°C, +V_{IN} = 12V, +V_C = +V_{IN}, A+/REF INPUT = 6V. T_A=T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
UNDER VOLTAGE (UV) COMPARATOR					
Input Bias Current		-1.5	-0.5		µA
UV Thresholds	Low to High, Other Input = 5V	1.48	1.50	1.52	V
UV Threshold Hysteresis		15	25	40	mV
Pwr OK V_{SAT}	I_{OUT} = 5mA			0.45	V
Pwr OK Leakage	V_{OUT} = 20V			5	µA
POWER AMPLIFIERS A and B					
Input Offset Voltage	V_{CM} = 6V, A Amplifier			8	mV
	B Amplifier			12	mV
Input Offset Drift	Note 1, A Amplifier Only			25	µV/°C
Input Bias Current	V_{CM} = 6V, except A+/REF Input	-500	-150		nA
Input Offset Current	V_{CM} = 6V, B Amplifier Only			200	nA
Input Bias Current at A+/Ref Input	(A+/Ref–C/S+)/12k, T_J = 25°C	60	84	105	µA/V
CMRR	1V ≤ V_{CM} ≤ 10V	70	90		dB
PSRR	+V_{IN} = 4V to 15V, V_{CM} = 1.5V	70	90		dB
Large Signal Voltage Gain	V_{OUT} = 1V, Sinking 500mA to V_{OUT} = 11V, Sourcing 500mA	3.0	15.0		V/mV
Slew Rate	1 to 13V, 13 to 1V, T_J = 25°C		1	2.1	V/µs
Unity Gain Bandwidth	Note 1, A Amplifier		2		MHz
	Note 1, B Amplifier		1		MHz
High-Side Current Limit		0.8	1.0		A
Output Saturation Voltage	High-Side, I_{SOURCE} = 250mA		0.7		V
	High-Side, I_{SOURCE} = 800mA		0.85		V
	Low-Side, I_{SINK} = 250mA		0.3		V
	Low-Side, I_{SINK} = 800mA		0.4		V
	Total, I_{OUT} = 250mA		1.0	1.2	V
	Total, I_{OUT} = 800mA		1.25	1.6	V
High Side Diode V_F	I_D = 800mA, Inhibit Activated		1.0		V
Low Side Diode V_F	I_D = 800mA, Inhibit Activated		1.0		V
CURRENT SENSE AMPLIFIER					
Input Offset Voltage	V_{CM} = 6V			2.0	mV
Input Offset Change with Common Mode Input	0V ≤ V_{CM} ≤ 12V			1500	µV/V
Input Offset Drift	Note 1			8	µV/°C
Voltage Gain	-1.0V ≤ V_{DIFF} ≤ +1.0V, V_{CM} = 6V	1.95	2.00	2.05	V
Output Saturation Voltage	Low-Side, I_{SINK} = 1.5mA		0.3	0.5	V
	High-Side, I_{SOURCE} = 1.5mA		0.4	0.7	V
Maximum A+/Ref Input	Volts Below +V_{IN}, C/S+ & C/S- = B_{OUTPUT} Max @ 10mA Output Current, +V_{IN} = 4.5V, C/S VIO ≤ 5mV		2.6	3.0	V
PARKING FUNCTION					
Park Input Threshold		0.7	1.1	1.7	V
Park Input Current	Park Input = 1.7V		60	100	µA
Park Drive Saturation Voltage, PD_{VSAT}	I_{SINK} = 100mA		0.3	0.5	V
Parking Drive Leakage	V_{OUT} = 20V			100	µA
Amplifier A Aux Input Bias Current		-500	-150		nA

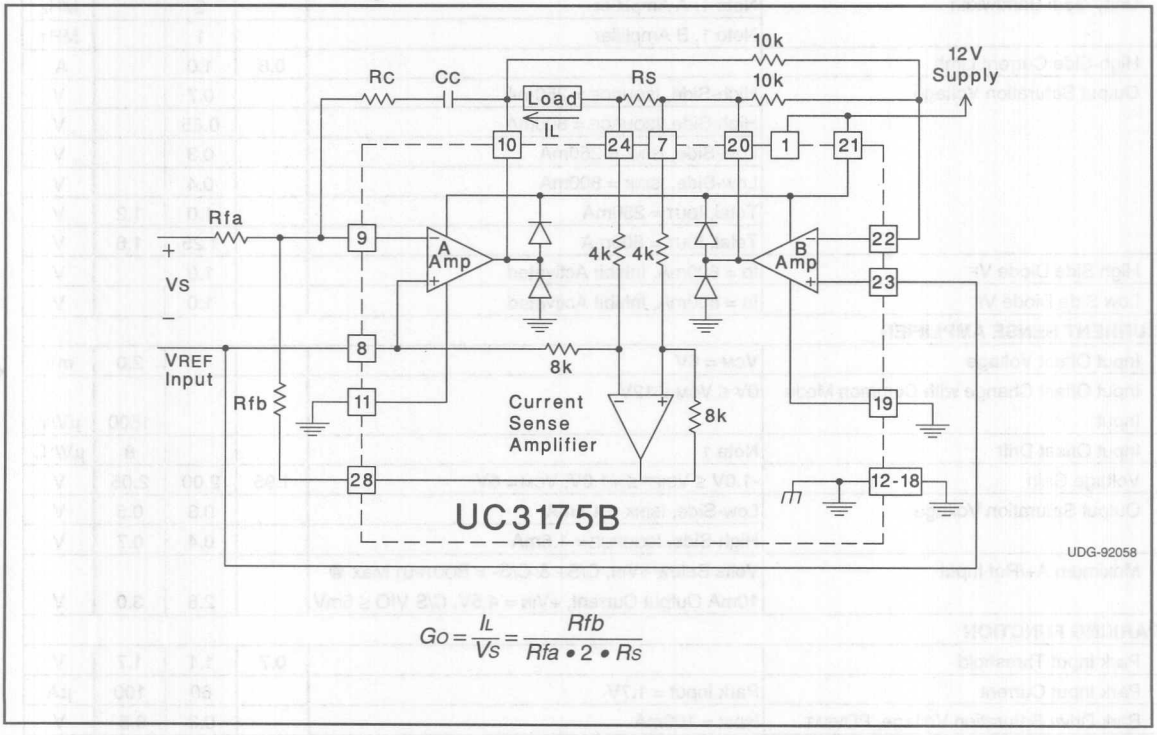
ELECTRICAL CHARACTERISTICS (cont.)

Unless otherwise stated specifications apply for 0°C ≤ T_A ≤ 70°C, +V_{IN} = 12V, +V_C = +V_{IN}, A+/REF Input = 6V. T_A=T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
PARKING FUNCTIONS (cont.)					
Amplifier A Saturation Voltage, A_{HVSAT}	I_{SOURCE} = 50mA, +V_{IN} = 3V		0.65	0.8	V
Regulating Voltage at Park Volts		1.47	1.50	1.53	V
Minimum Parking Supply Voltage	A_{HVSAT} + PD_{VSAT} ≤ 1.3V @ 50mA		1.7	1.9	V
AUXILIARY FUNCTIONS					
Limit Input Low Voltage	A Output Forced Low	0.7	0.8		V
Limit Input High Voltage	A Output Forced High		2.2	2.3	V
Limit Inactive		1.2		1.8	V
Limit Open Circuit Voltage		1.45	1.50	1.55	V
Limit Input Resistance	1.2V ≤ Limit Input ≤ 1.8V		10		kΩ
Inhibit Input Threshold		0.7	1.1	1.7	V
Inhibit Input Current	Inhibit Input = 1.7V		400	700	µA
Supply Current when Inhibited	The sum of +V_{IN} and +V_C currents		2	6	mA
Thermal Shutdown Temperature			165		°C

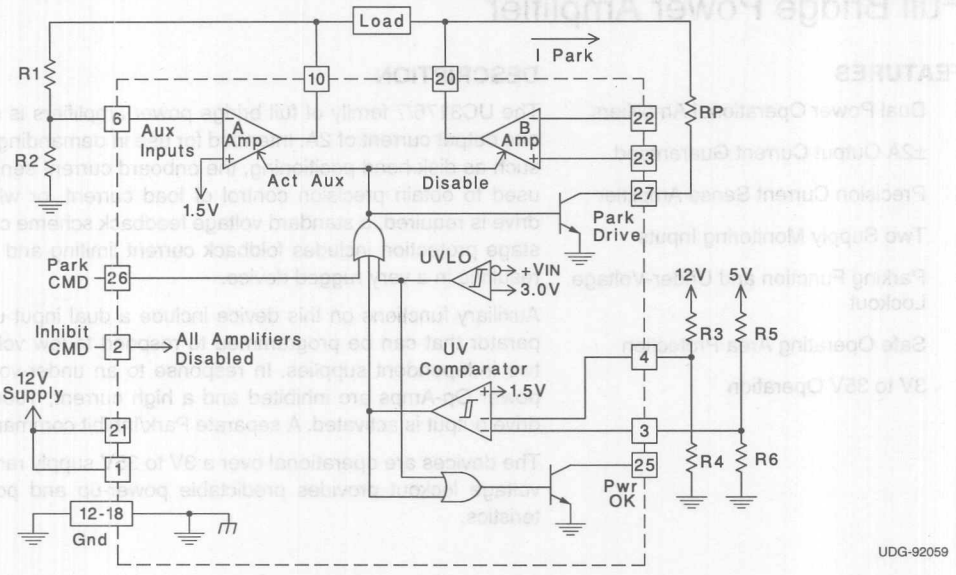
Note 1: This specification not tested in production.

UC3175B Series Current Sensing



$$Go = \frac{I_L}{Vs} = \frac{Rfb}{Rfa \bullet 2 \bullet Rs}$$

Parking Function



Notes: *Parking voltage* $= \dfrac{1.5V \bullet R1 + R2}{R2 - (I_L \bullet RP)}$

RP is optional for current limiting.
Inhibit and Park Inputs are active high.
Pwr OK is low on power failure.

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UNITRODE

Full Bridge Power Amplifier

FEATURES

- Dual Power Operational Amplifiers
- ±2A Output Current Guaranteed
- Precision Current Sense Amplifier
- Two Supply Monitoring Inputs
- Parking Function and Under-Voltage Lockout
- Safe Operating Area Protection
- 3V to 35V Operation

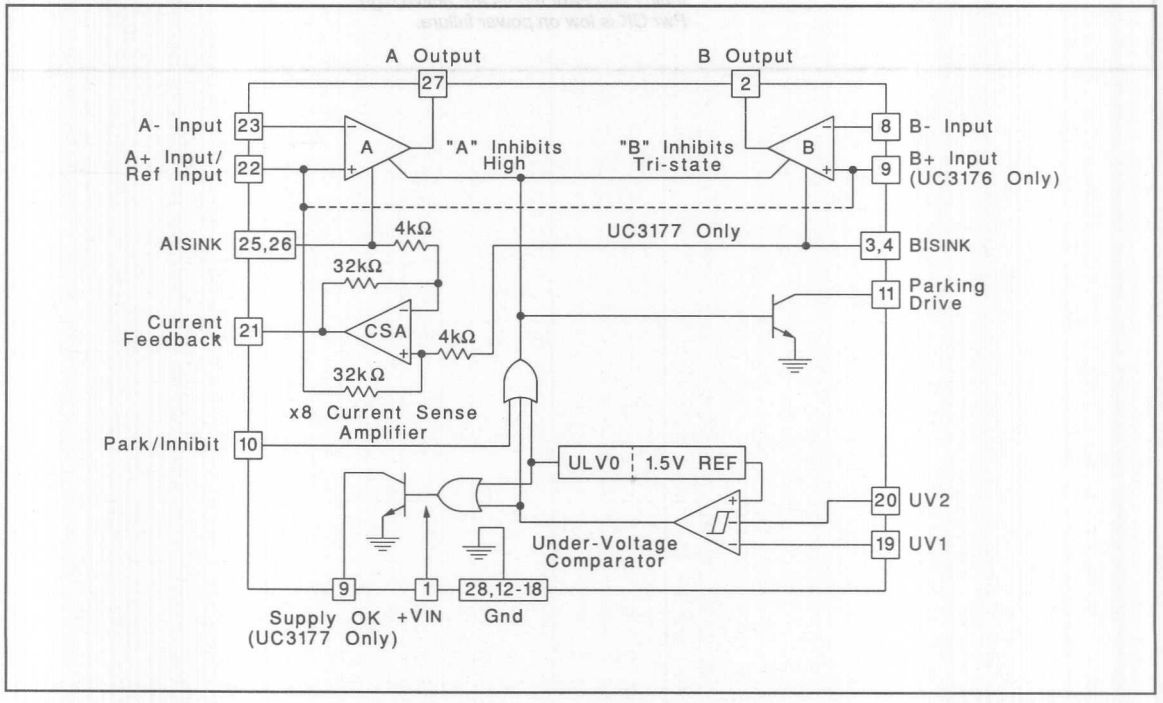
DESCRIPTION

The UC3176/7 family of full bridge power amplifiers is rated for a continuous output current of 2A. Intended for use in demanding servo applications such as disk head positioning, the onboard current sense amplifier can be used to obtain precision control of load current, or where voltage mode drive is required, a standard voltage feedback scheme can be used. Output stage protection includes foldback current limiting and thermal shutdown, resulting in a very rugged device.

Auxiliary functions on this device include a dual input under-voltage comparator that can be programmed to respond to low voltage conditions on two independent supplies. In response to an under-voltage condition the power Op-Amps are inhibited and a high current, 100mA, open collector drive output is activated. A separate Park/Inhibit command input.

The devices are operational over a 3V to 35V supply range. Internal under-voltage lockout provides predictable power-up and power-down characteristics.

BLOCK DIAGRAM



10/94

ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Supply voltage, (+VIN) 40V
Park/Inhibit, UV1 and UV2 inputs (zener clamped)
  Maximum forced voltage . . . . . -0.3V to 10V
  Maximum forced current. . . . . ±10mA
Other Input Voltages. . . . . -0.3V to +VIN
AISINK and BISINK Voltages . . . . . -0.3V to 6V
Open Collector Output Voltages. 40V
A and B Output Currents (Continuous)
  Source . . . . . Internally Limited
  Sink. 2.5A
Total Supply Current (Continuous). 4A
Parking Drive Output Current (Continuous) 200mA
Supply OK Output Current, UC3177 (Continuous) . . . 30mA
Operating Junction Temperature . . . . . -55°C to +150°C
Power Dissipation at TC = +75°C
  QP package. 4W
Storage Temperature . . . . . -65°C to +150°C

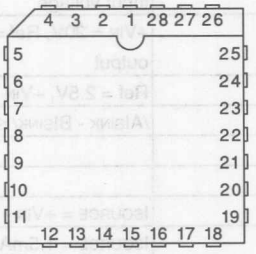
Note 1: Unless otherwise indicated, voltages are reference to ground and currents are positive into, negative out of, the specified terminals.

THERMAL DATA

QP package:
Thermal Resistance Junction to Leads, θJL . . . . . 15°C/W
Thermal Resistance Junction to Ambient, θJA . . . . 50°C/W

CONNECTION DIAGRAM

PLCC-28 (Top View)
QP Package



PACKAGE PIN FUNCTION	
FUNCTION	PIN
+VIN	1
B Output	2
BISINK(Sense)	3
BISINK	4
N/C	5-7
B- Input	8
*	9
Park/Inhibit	10
Parking Drive	11
Gnd (Heat Flow Pins)	12-18
UV1	19
UV2	20
Current Feedback	21
A+ Input	22
A- Input	23
N/C	24
AISINK	25
AISINK(Sense)	26
A Output	27
Gnd	28

**Pin 9: UC3176, B+ Input*
UC3177, Supply OK

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, specifications hold for TA = 0 to 70°C, +VIN = 12V, TA = TJ.

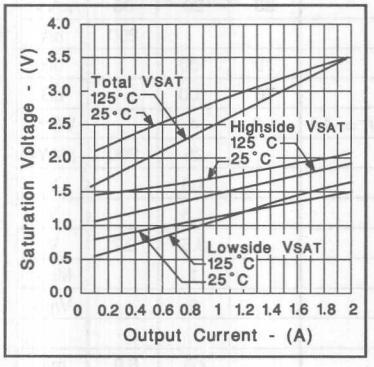
PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Supply					
Supply Current	+VIN = 12V		18	25	mA
	+VIN = 35V		21	30	mA
UVOL Threshold	+VIN low to high		2.8	3.0	V
	Threshold Hysteresis		220	300	mV
Power, Amplifier, A and B					
Input Offset Voltage	VCM = 6V, VOUT = 6V			8	mV
Input Bias Current	VCM = 6V, Except A+ Input	-500	-100		nA
Input Bias Current at A+/Reference Input	(A+/Ref - BISINK)/36kohms; TJ = 25°C	23	28	35	µA/V
Input Offset Current B Amp (UC3176 Only)	VCM = 6V			200	nA
CMRR	VCM = 1 to 33V, +VIN =35V, VOUT = 6V	70	100		dB
PSRR	+VIN = 5 to 35V, VCM = 2.5V	70	100		dB
Large Signal Voltage Gain	VOUT = 3V, w/IOUT = 1A to VOUT = 9V, w/IOUT = -1A	1.5	4		V/mV
Thermal Feedback	+VIN = 20V, Pd = 20W at opposite output		25	200	µV/W
Saturation Voltage	IOUT = -2A, High Side, TJ = 25°		1.9		V
	CIOUT = 2A, Low Side, TJ = 25°C		1.6		V
	Total VSAT at 2A, TJ = 25°C		3.5	3.7	V
Unity Gain Bandwidth			1		MHz
Slew Rate			1		V/µs
Differential IOUT Sense Error Current	IOUT(A) = -IOUT(B), /IOUT/- /AISINK - BISINK/				
in Bridge Configuration	IOUT ≤200mA		3.0	6.0	mA
	IOUT ≤ 2A		5.0	10	mA
High Side Current Limiting	=VIN - VOUT < 12V		-2.7	-2.0	A

ELECTRICAL CHARACTERISTICS:

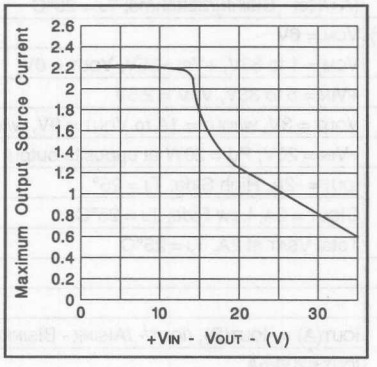
Unless otherwise stated, specifications hold for T_A = 0 to 70°C, $+V_{IN}$ = 12V, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Current Sense Amplifier					
Input Offset Voltage	V_{CM} = 0V, A+/Ref at 6V			3	mV
	Ref = 2V to 20V, $+V_{IN}$ = 35, change with Ref input voltage			600	µV/V
Thermal Gradient Sensitivity	$+V_{IN}$ = 20V, Ref = 10V Pd = 20W @ A or B output		5.0	75	µV/W
PSRR	Ref = 2.5V, $+V_{IN}$ = 5 to 35V	70	100		dB
Gain	/A_{ISINK} - B_{ISINK}/ ≤ 0.5V	7.8	8	8.1	V/V
Slew Rate			2		V/µS
3dB Bandwidth			1		MHz
Max Output Current	I_{SOURCE} = $+V_{IN}$ - V_{OUT} = 0.5V	2.5	3.5		mA
Output Saturation Voltage	I_{SOURCE} = 1.5mA, High Side		0.15	0.30	V
	I_{SINK} = 5mA, Low Side		1.4	1.7	V
Under-Voltage Comparator					
Threshold Voltage	Low to High, other input at 5V	1.44	1.50	1.56	V
	Threshold Hysteresis	50	70	80	mV
Input Current	Input = 2V, other input at 5V	-2	-.05		µA
Supply OK V_{SAT} (UC3177 Only)	I_{OUT} = 5mA			0.45	V
Supply OK Leakage (UC3177 Only)	V_{OUT} = 35V			5	µA
Park/Inhibit					
Park/Inhibit Thl'd		1.1	1.3	1.7	V
Park/Inhibit Input Current	At threshold		60	100	µA
Parking Drive Saturation Voltage	I_{OUT} = 100mA		0.3	0.7	V
Parking Drive Leakage	V_{OUT} = 35V			15	µA
Thermal Shutdown					
Shutdown Temperature			165		°C

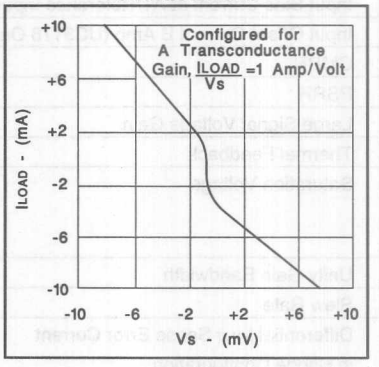
Output Saturation Voltage vs Current



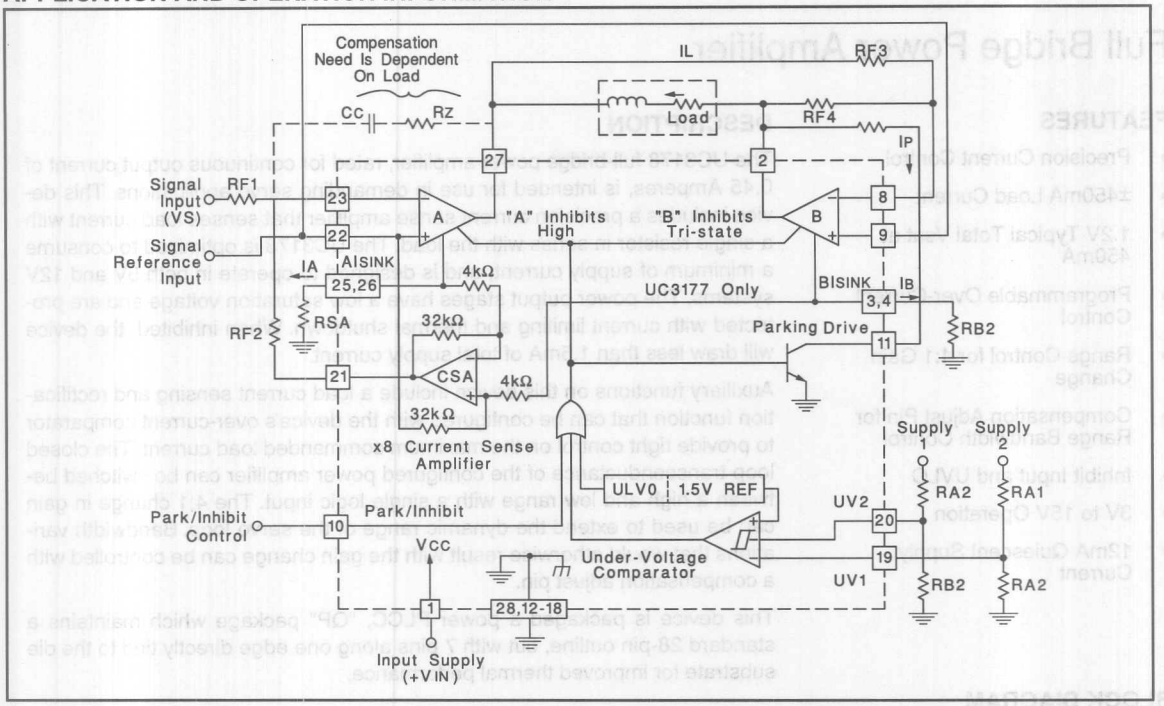
Maximum Source Current vs +VIN - VOUT



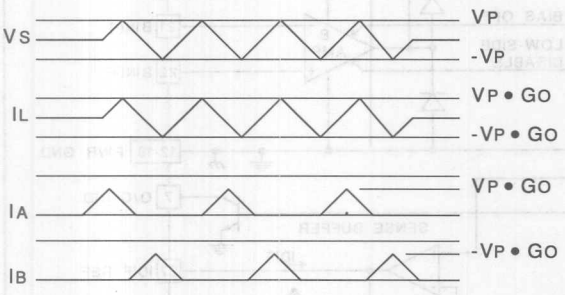
Crossover Current Error Characteristic



APPLICATION AND OPERATION INFORMATION



WAVEFORMS FOR ABOVE APPLICATION



DESIGN EQUATIONS

$$\text{Transconductance } (G_O) = \frac{I_L}{V_S} = \frac{R_{F2}}{R_{F1}} \times \left(\frac{1}{8R_S}\right)$$

with: $R_{SA} = R_{SB}$ and $R_{F3} = R_{F4}$

$$\text{Parking Current } (I_P) = \frac{V_{IN} - 1.5}{R_P + R_L}$$

where: R_L = load resistance

Under-Voltage Thresholds, at Supplies
High to Low Threshold, $(V_{LH}) = 1.425\ (R_A + R_B)/R_B$
Low to High Threshold, $(V_{HL}) = 1.5\ (R_A + R_B)/R_B$

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UNITRODE

Full Bridge Power Amplifier

FEATURES

- Precision Current Control
- ±450mA Load Current
- 1.2V Typical Total Vsat at 450mA
- Programmable Over-Current Control
- Range Control for 4:1 Gain Change
- Compensation Adjust Pin for Range Bandwidth Control
- Inhibit Input and UVLO
- 3V to 15V Operation
- 12mA Quiescent Supply Current

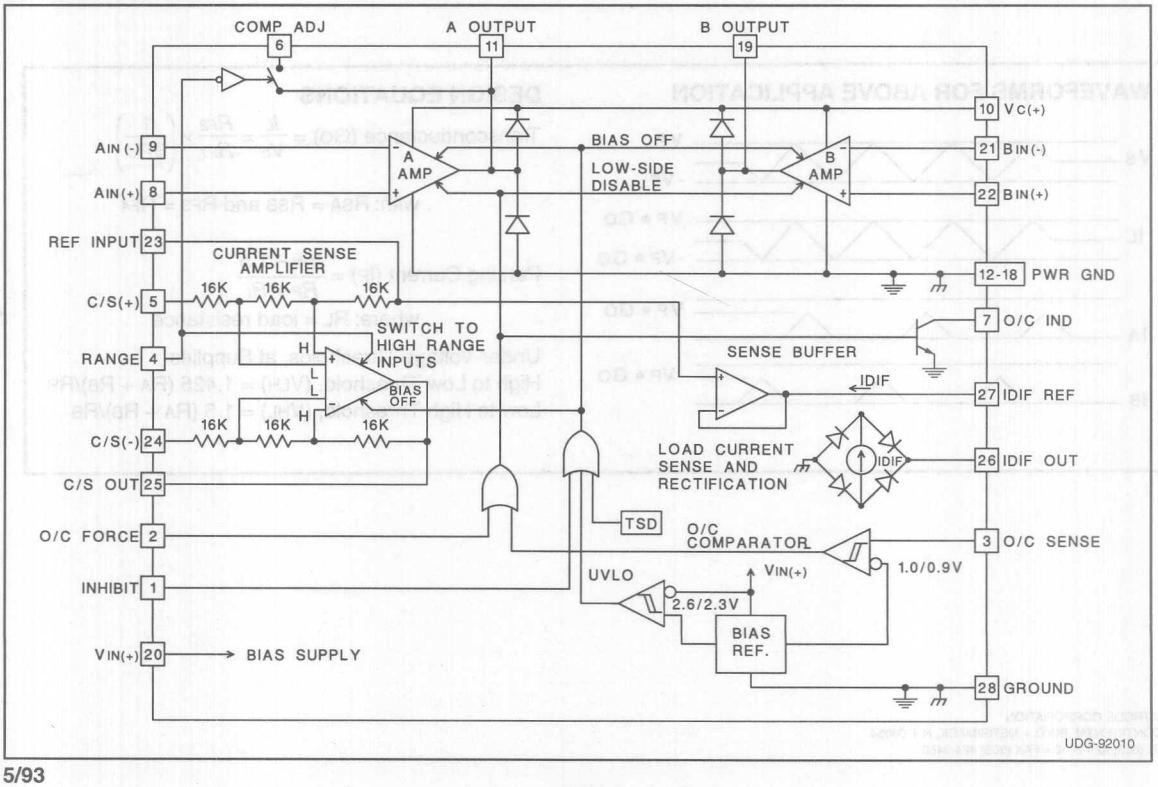
DESCRIPTION

The UC3178 full-bridge power amplifier, rated for continuous output current of 0.45 Amperes, is intended for use in demanding servo applications. This device includes a precision current sense amplifier that senses load current with a single resistor in series with the load. The UC3178 is optimized to consume a minimum of supply current, and is designed to operate in both 5V and 12V systems. The power output stages have a low saturation voltage and are protected with current limiting and thermal shutdown. When inhibited, the device will draw less than 1.5mA of total supply current.

Auxiliary functions on this device include a load current sensing and rectification function that can be configured with the device's over-current comparator to provide tight control on the maximum commanded load current. The closed loop transconductance of the configured power amplifier can be switched between a high and low range with a single logic input. The 4:1 change in gain can be used to extend the dynamic range of the servo loop. Bandwidth variations that would otherwise result with the gain change can be controlled with a compensation adjust pin.

This device is packaged a power PLCC, "QP" package which maintains a standard 28-pin outline, but with 7 pins along one edge directly tied to the die substrate for improved thermal performance.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage, (V_{IN}(+), V_C(+)) 20V
O/C Sense, Logic Inputs, and REF Input
  Maximum forced voltage . . . . . -0.3V to 10V
  Maximum forced current . . . . . ±10mA
A & B Amplifier Inputs . . . . . -0.3V to (V_{IN}(+) + 1.0V)
O/C Indicate Open Collector Output Voltage 20V
A and B Output Currents(continuous)
  Source . . . . . Internally Limited
  Sink 0.6A
Output Diode Current (pulsed)* 0.5A
O/C Ind Output Current(continuous) 20mA
Operating Junction Temperature . . . . . +150°C
Storage Temperature . . . . . -65°C to +150°C

**Notes: Unless otherwise indicated, voltages are referenced to ground and currents are positive into, negative out of, the specified terminals, "Pulsed" is defined as a less than 10% duty cycle pulse with a maximum duration of 500µs.*

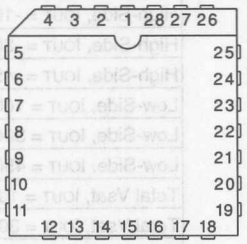
THERMAL DATA

QP package: (see packaging section of UICC data book for more details on thermal performance)
  Thermal Resistance Junction to Leads, θjl . . . . . 15°C/W
  Thermal Resistance Junction to Ambient, θja . . . 30-40°C/W

Note: The above numbers for θjl are maximums for the limiting thermal resistance of the package in a standard mounting configuration. The θja numbers are meant to be guidelines for the thermal performance of the device/pc-board system. All of the above numbers assume no ambient airflow.

CONNECTION DIAGRAM

PLCC - 28 (Top View)
QP Package



PACKAGE PIN FUNCTION	
FUNCTION	PIN
Inhibit	1
O/C Force	2
O/C Sense	3
Range	4
C/S(+)	5
Comp Adj	6
O/C Ind	7
A_{IN}(+)	8
A_{IN}(-)	9
V_C(+) Supply	10
A Output	11
Pwr Gnd	12
Pwr Gnd	13
Pwr Gnd	14
Pwr Gnd	15
Pwr Gnd	16
Pwr Gnd	17
Pwr Gnd	18
B Output	19
V_{IN}(+)	20
B_{IN}(-)	21
B_{IN}(+)	22
REF Input	23
C/S(+)	24
C/S Out	25
IDIF Out	26
IDIF REF	27
Ground	28

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated specifications hold for T_A = 0°C to 70°C, V_C(+) = V_{IN}(+) = 12V, REF Input = V_{IN}(+)/2, O/C Input & Inhibit Input = 0V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply					
V_{IN} (+)Supply Current			12	16	mA
V_C(+) Supply Current	I_{OUT} = OA		1.2	2.0	mA
Total Supply Current	Supplies = 5V, I_{OUT} = OA		12	16	mA
	Supplies = 12V, I_{OUT} = OA		13	18	mA
V_{IN}(+) UVLO Threshold	low to high		2.6	2.8	V
UVLO Threshold Hysterisis			300		mV
Over-Current (O/C) Comparator					
Input Bias Current	V input = 0.8V	-1.0	-.01		µA
Thresholds	low to high	0.97	1.0	1.03	V
Threshold Hysterisis		85	100	115	mV
O/C IND Vsat	I_{OUT} = 5mA, V input low		0.2	0.45	V
O/C IND Leakage	V_{OUT} = 20V			5.0	µA
Power Amplifiers A and B					
Input Offset Voltage	A Amplifier, V_{CM} = 6V			4.0	mV
	B Amplifier, V_{CM} = 6V			12.0	mV
Input Bias Current	V_{CM} = 6V	-500	-50		µA
CMRR	V_{CM} = 0.5 to 13V, Supplies = 15V	70	90		dB
PSRR	V_{IN}(+) = 4 to 15V, V_{CM} = 1.5V	70	90		dB
Large Signal Voltage Gain	Supplies = 12V, V_{OUT} = 1V, I_{OUT} = 300mA to V_{OUT} = 10.5V, I_{OUT} = -300mA	3.0	15.0		V/mV

ELECTRICAL CHARACTERISTICS (cont.): Unless otherwise stated specifications hold for T_A = 0°C to 70°C , $V_{C(+)}$ = $V_{IN(+)}$ = 12V, REF Input = $V_{IN(+)}$/2, O/C Input & Inhibit Input = 0V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Power Amplifiers A & B (cont.)					
Gain Bandwith Product	A Amplifier		2.0		MHz
	B Amplifier		1.0		MHz
Slew Rate			1.0		V/µs
High-Side Current Limit		0.45	0.65		A
Output Saturation Voltage	High-Side, I_{OUT} = -100mA		0.75		V
	High-Side, I_{OUT} = -300mA		0.85		V
	High-Side, I_{OUT} = -450mA		0.9		V
	Low-Side, I_{OUT} = 100mA		0.2		V
	Low-Side, I_{OUT} = 300mA		0.25		V
	Low-Side, I_{OUT} = 450mA		0.30		V
	Total Vsat, I_{OUT} = 100mA		0.95	1.2	V
	Total Vsat, I_{OUT} = 300mA		1.05	1.4	V
	Total Vsat, I_{OUT} = 450mA		1.25	1.6	V
High-Side Diode, Vf	I_D = 450mA		1.30		V
Current Sense Amplifier					
Input Offset Voltage	V_{CM} = 6V, Low range mode			2.0	mV
	High range mode			4.0	mV
Input Offset Change with Common Mode Input	V_{CM} = -1V to 13V, Supplies = 12V, Low Range Mode			2000	µV/V
	V_{CM} = -1V to 13V, Supplies = 12V, High Range Mode			4000	µV/V
Voltage Gain	V_{DIFF} = +1.0 to -1.0V, Vcm = 6V, High Range Mode	0.485	0.50	0.515	V/V
	V_{DIFF} = +1.0 to -1.0V, Vcm = 6V, Low Range Mode	1.95	2.0	2.05	V/V
Saturation Voltage	Low-Side, I_{OUT} = 1mA		0.1	0.3	V
	High-Side, I_{OUT} = -1mA, Referenced to = $V_{IN(+)}$		0.1	0.3	V
Input Bias Current at Ref. Input	(REF Input - C/S(+))/48kohms, Tj = 25°C	15	21	27	µA/V
Load Current Sense and Rectification					
Sense Buffer Offset Voltage	REF Input to IDIF REF, I_{OUT} = ±1mA			10	mV
Sense Buffer CMRR	I_{OUT} = ±1mA, REF Input = 2V to 10V	70	90		dB
IDIF REF to IDIF Out Current Ratio	IDIF = ± 100µA, IDIF Out = 1V	0.95	1.0	1.05	A/A
	IDIF = ±1mA, IDIF Out = 1V	0.94	1.0	1.06	A/A
IDIF Out Supply Sensitivity	IDIF Out = ± 1mA, $V_{IN(+)}$ = 4V to 15V,REF Input = 2V		1.0	5.0	µA/V
IDIF Out Common Mode Sensitivity (delta IDIF Out/delta REF Input)	I_{OUT} = ±1mA, REF Input = 2V to10V, IDIF Out = 1V		1.0	5.0	µA/V
Auxiliary Functions					
Inhibit Input Threshold		0.6	1.1	1.7	V
Inhibit Input Current	Inhibit Input = 1.7V	-1.0	-0.5		µA
O/C Force Input Threshold		0.6	1.1	1.7	V
O/C Force Input Current	O/C Force Input = 1.7V		50	100	µA
Range Input Threshold		0.6	1.1	1.7	V
Range Input Current	Range Input = 1.7V		50	100	µA
COMP ADJ Pin Saturation Voltage	Range Input = 0V, Pin Current = ±500µA, Referenced to A_{OUT}		0.02	0.1	V
COMP ADJ Leakage Current	Range Input = 1.7V, Supplies = 12V				
	A_{OUT}-$V_{Comp\ Adj}$ = ±6V			5.0	µA
Total Supply Current When Inhibited	$V_{IN(+)}$ and $V_{C(+)}$ currents		1.0	1.5	mA
Thermal Shutdown Temperature			165		°C

PIN DESCRIPTIONS:

A & B OUT: Outputs for the A & B power amplifiers, providing differential drive to the load during normal operation. During a UVLO, Inhibit, or O/C condition both of these outputs will be in a high, source only state. High-side diodes are included to catch inductive load currents flowing into these pins, inductive kicks on the low-side are caught by the high-side output transistors.

AIN(+): Non-inverting input to the A amplifier. Normally tied to the REF Input when the current sense amplifier is used.

AIN(-): Inverting input to the A amplifier. Used as the summing node to close the loop on the overall power amplifier.

BIN(+): Non-inverting input to the B amplifier. This pin normally sets the reference point for the differential voltage swing at the load.

BIN(-): Inverting input to the B amplifier. Used to program the gain of the B amplifier.

COMP ADJ: The compensation adjust pin allows the user to provide an auxiliary compensation network for the A amplifier that is only active when the current sense amplifier is in the low range. With this option, the user can control the change in bandwidth that would otherwise result from the gain change in the feedback loop.

C/S(+): The non-inverting input to the current sense amplifier is typically tied to the load side of the series current sense resistor. This pin can be pulled below ground during an abrupt load current change with an inductive load. Proper operation of the current sense amplifier will result if this pin does not go below ground by an amount greater than:

(REF Input / 2) - 0.3V.

C/S(-): The inverting input to the current sense amplifier is typically tied to the connection between the B amplifier output and the current sense resistor that is in series with the load.

C/S Output: The output of the current sense amplifier has a 1.5mA current source pull-up and an active NPN pull-down. The output will pull to within 0.3V of either rail with a load current of less than 1mA.

GND: Reference point for the internal reference, O/C comparator, and other low-level circuitry.

IDIF OUT: Current source output pin. The value of the output current is nominally equal to the magnitude of the current through the IDIF REF pin.

IDIF REF: Output of the IDIF sense buffer. Voltage on this pin will track the applied voltage on the REF Input pin. Current through this pin is full wave rectified and appears as a current sourced from the IDIF OUT pin.

Inhibit : A high impedance logic input that disables the A and B power amplifiers, the IDIF sense buffer, and the Current Sense amplifier. This input has an internal pull-up that will inhibit the device if the input is left open.

O/C Force: Logic input that forces the O/C condition.

O/C IND: Open collector ouput that indicates, with an active low state, an O/C condition.

O/C Sense: Input to the Over Current Comparator. When this input is above its 1V threshold the low-side devices of both the A & B power amplifiers will be disabled forcing a high, source only, state at both outputs.

PWR GND: Current return for all high level circuitry, this pin should be connected to the same potential as GND.

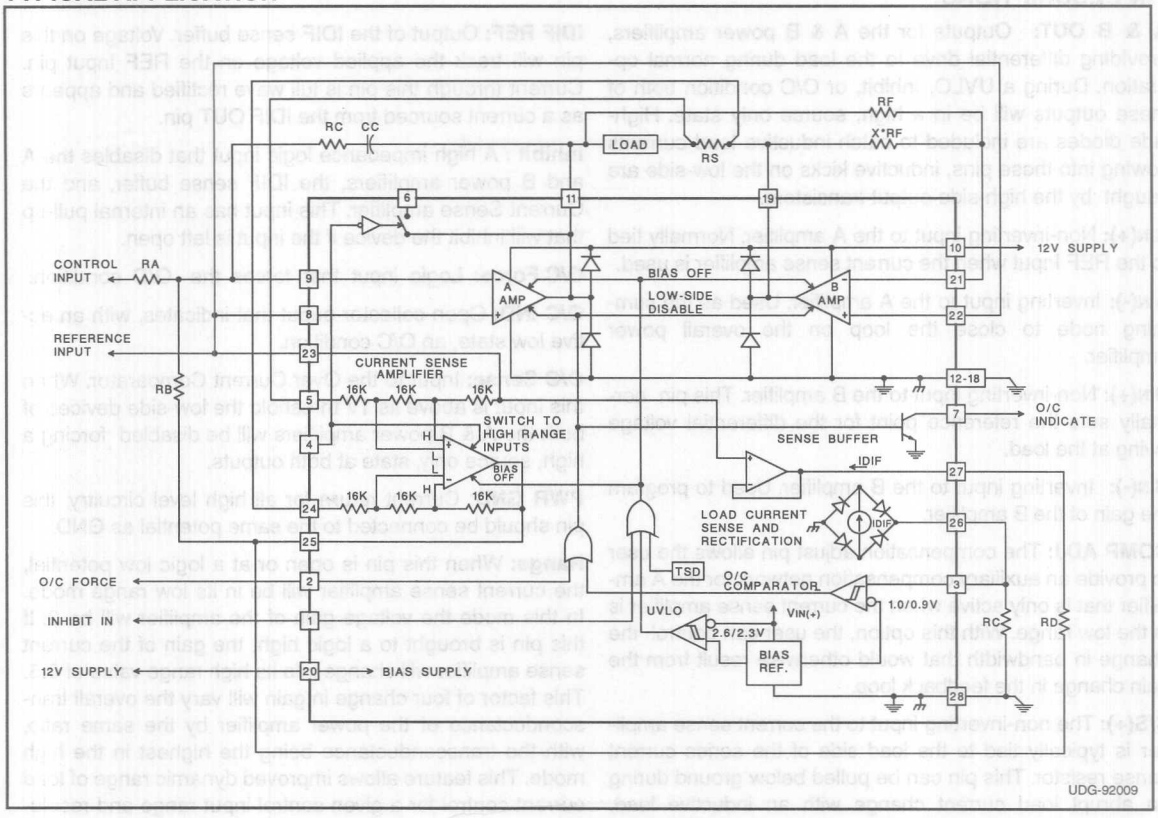
Range: When this pin is open or at a logic low potential, the current sense amplifier will be in its low range mode. In this mode the voltage gain of the amplifier will be 2. If this pin is brought to a logic high, the gain of the current sense amplifier will change into its high range value of 0.5. This factor of four change in gain will vary the overall transconductance of the power amplifier by the same ratio, with the transconductance being the highest in the high mode. This feature allows improved dynamic range of load current control for a given control input range and resolution.

REF Input: Sets the Reference level at the C/S Output, and is normally tied to the system reference level for inputs to the power amplifier.

VIN(+): Provides bias supply to the device. The High-Side drive to the power stages on both the A and B amplifiers is referenced to this pin. The High-side saturation voltages, and UVLO are specified and measured with respect to this supply pin.

VC(+): This supply pin is the high current supply to the collectors of the high-side NPN output devices on the A and B amplifiers. This supply should be powered whenever the A or B amplifiers are to be activated. This pin can operate approximately 400mV below the VIN(+) supply without affecting the voltage available to the load.

TYPICAL APPLICATION



Power amplifier transconductance

$$Go = \frac{Il}{Vs} = \frac{RB}{RA} \bullet \frac{1}{AVCS \bullet RS}$$

Peak commanded load current

$$Il_{MAX} = V_{O/C} \bullet \frac{RD}{RS \bullet AV_{CS} \bullet RE}$$

where:

Il is the load current

Vs is the input command voltage

AV_{CS} is the current sense amplifier gain

= 2.0 in low range mode

= 0.5 in high range mode

$V_{O/C}$ is the 1.0V over-current comparator threshold

UNITRODE CORPORATION
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Stepper Motor Drive Circuit

FEATURES

- Complete Motor Driver and Encoder
- Continuous Drive Capability 350mA per Phase
- Contains all Required Logic for Full and Half Stepping
- Bilevel Operation for Fast Step Rates
- Operates as a Voltage Doubler
- Useable as a Phase Generator and/or as a Driver
- Power-On Reset Guarantees Safe, Predictable Power-Up

DESCRIPTION

The UC3517 contains four NPN drivers that operate in two-phase fashion for full-step and half-step motor control. The UC3517 also contains two emitter followers, two monostables, phase decoder logic, power-on reset, and low-voltage protection, making it a versatile system for driving small stepper motors or for controlling large power devices.

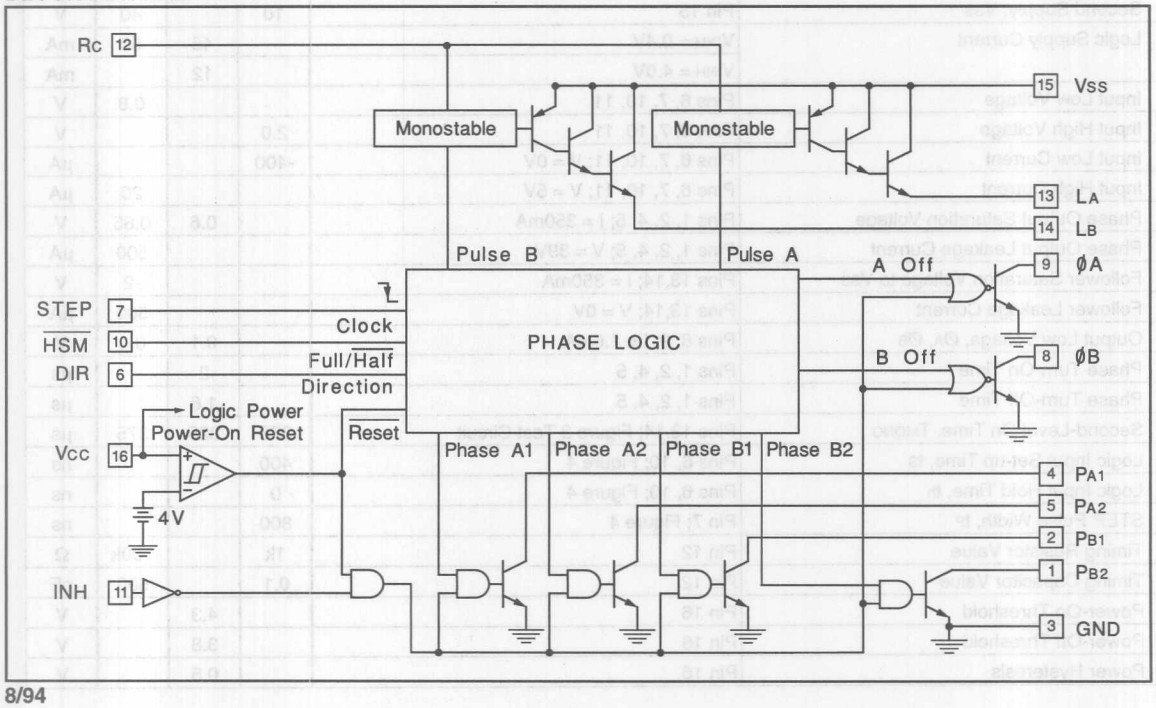
The emitter followers and monostables in the UC3517 are configured to apply higher-voltage pulses to the motor at each step command. This drive technique, called "Bilevel," allows faster stepping than common resistive current limiting, yet generates less electrical noise than chopping techniques.

ABSOLUTE MAXIMUM RATINGS

Second Level Supply, Vss 40V
Phase Output Supply, VMM 40V
Logic Supply, Vcc 7V
Logic Input Voltage ..... -.3V to +7V
Logic Input Current ..... ±10mA
Output Current, Each Phase 500mA
Output Current, Emitter Follower ..... -500mA
Power Dissipation, (Note) 1W
Power Dissipation, (Note) 2W
Junction Temperature ..... 150°C
Ambient Temperature, UC1517 ..... -55°C to +125°C
Ambient Temperature, UC3517 ..... 0°C to +70°C
Storage Temperature ..... -55°C to +150°C

Note: Consult Packaging section of Databook for thermal limitations and considerations of package.

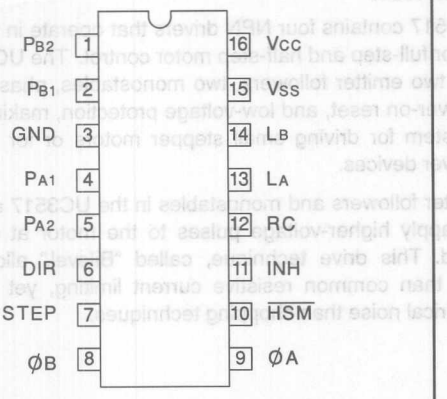
BLOCK DIAGRAM



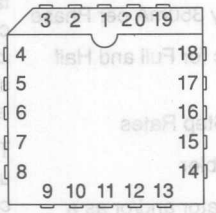
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CONNECTION DIAGRAMS

DIL-16 (TOP VIEW)
J or N Package



PLCC-20, LCC-20
(TOP VIEW)
Q & L PACKAGE



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
P_{B2}	2
P_{B1}	3
GND	4
P_{A1}	5
N/C	6
P_{A2}	7
DIR	8
STEP	9
$Ø_B$	10
N/C	11
$Ø_A$	12
$\overline{HSM}$	13
INH	14
RC	15
N/C	16
L_A	17
L_B	18
V_{SS}	19
V_{CC}	20

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1517 and 0°C to +70°C for the UC3517, V_{CC}=5V, V_{SS} = 20V, T_A=T_J. Pin numbers refer to DIL-16 package.

PARAMETER	TEST CONDITIONS	UC1517 / UC3517			UNITS
		MIN	TYP	MAX	
Logic Supply, V_{CC}	Pin 16	4.75		5.25	V
Second Supply, V_{SS}	Pin 15	10		40	V
Logic Supply Current	V_{INH} = 0.4V		45	60	mA
	V_{INH} = 4.0V		12		mA
Input Low Voltage	Pins 6, 7, 10, 11			0.8	V
Input High Voltage	Pins 6, 7, 10, 11	2.0			V
Input Low Current	Pins 6, 7, 10, 11; V = 0V	-400			µA
Input High Current	Pins 6, 7, 10, 11; V = 5V			20	µA
Phase Output Saturation Voltage	Pins 1, 2, 4, 5; I = 350mA		0.6	0.85	V
Phase Output Leakage Current	Pins 1, 2, 4, 5; V = 39V			500	µA
Follower Saturation Voltage to V_{SS}	Pins 13,14; I = 350mA			-2	V
Follower Leakage Current	Pins 13,14; V = 0V			500	µA
Output Low Voltage, $Ø_A$, $Ø_B$	Pins 8, 9; I = 1.6mA		0.1	0.4	V
Phase Turn-On Time	Pins 1, 2, 4, 5		2		µs
Phase Turn-Off Time	Pins 1, 2, 4, 5		1.8		µs
Second-Level On Time. T_{MONO}	Pins 13,14; Figure 3 Test Circuit	275	325	375	µs
Logic Input Set-up Time, t_S	Pins 6, 10; Figure 4	400			ns
Logic Input Hold Time, t_h	Pins 6, 10; Figure 4	0			ns
STEP Pulse Width, t_P	Pin 7; Figure 4	800			ns
Timing Resistor Value	Pin 12	1k		100k	Ω
Timing Capacitor Value	Pin 12	0.1		500	nF
Power-On Threshold	Pin 16		4.3		V
Power-Off Threshold	Pin 16		3.8		V
Power Hysteresis	Pin 16		0.5		V

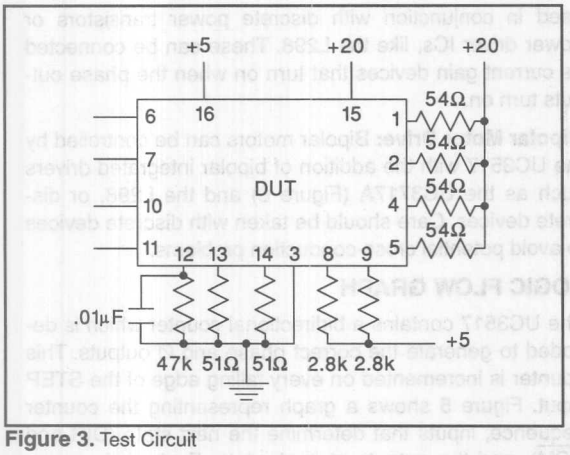


Figure 3. Test Circuit

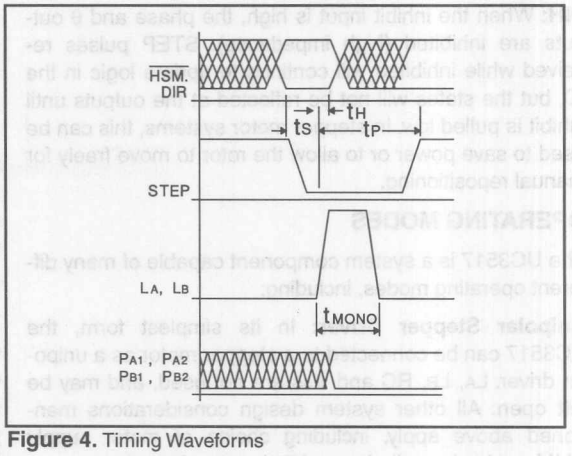


Figure 4. Timing Waveforms

PIN DESCRIPTION

VCC: VCC is the UC3517's logic supply. Connect to a regulated 5VDC, and bypass with a 0.1µF ceramic capacitor to absorb switching transients.

VMM: VMM is the primary motor supply. It connects to the UC3517 phase outputs through the motor windings. Limit this supply to less than 40V to prevent breakdown of the phase output transistors. Select the nominal VMM voltage for the desired continuous winding current.

VSS: VSS is the secondary motor supply. It drives the LA and LB outputs of the UC3517 when a monostable in the UC3517 is active. In the bilevel application, this supply is applied to the motor to charge the winding inductance faster than the primary supply could. Typically, VSS is higher in voltage than VMM, although VSS must be less than 40V. The VSS supply should have good transient capability.

GROUND: The ground pin is the common reference for all supplies, inputs and outputs.

RC: RC controls the timing functions of the monostables in the UC3517. It is normally connected to a resistor (RT) and a capacitor (CT) to ground, as shown in Figure 3. Monostable on time is determined by the formula $T_{ON} \approx 0.69\ R_T\ C_T$. To keep the monostable on indefinitely, pull RC to VCC through a 50k resistor. The UC3517 contains only one RC pin for two monostables. If step rates comparable to TON are commanded, incorrect pulsing can result, so consider maximum step rates when selecting RT and CT. Keep $T_{ON} \leq T_{STEP\ MAX}$.

ØA and ØB: These logic outputs indicate half-step position. These outputs are open-collector, low-current drivers, and may directly drive TTL logic. They can also drive CMOS logic if a pull-up resistor is provided. Systems which use the UC3517 as an encoder and use a different driver can use these outputs to disable the external driver, as shown in Figure 8. The sequencing of these outputs is shown in Figure 5.

PA1, PA2, PB1, and PB2: The phase outputs pull to ground sequentially to cause motor stepping, according to the state diagram of Figure 5. The sequence of stepping on these lines, as well as with the LA and LB lines is controlled by STEP input, the DIR input, and the $\overline{HSM}$ input. Caution: If these outputs or any other IC pins are pulled too far below ground either continuously or in a transient, step memory can be lost. It is recommended that these pins be clamped to ground and supply with high-speed diodes when driving inductive loads such as motor windings or solenoids. This clamping is very important because one side of the winding can "kick" in a direction opposite the swing of the other side.

LA and LB: These outputs pull to VSS when their corresponding monostable is active, and will remain high until the monostable time elapses. Before and after, these outputs are high-impedance. For detail timing information, consult Figure 5.

STEP: This logic input clocks the logic in the UC3517 on every falling edge. Like all other UC3517 inputs, this input is TTL/CMOS compatible, and should not be pulled below ground.

DIR: This logic input controls the motor rotation direction by controlling the phase output sequence as shown in Figure 5. This signal must be stable 400ns before a falling edge on STEP, and must remain stable through the edge to insure correct stepping.

$\overline{HSM}$: This logic input switches the UC3517 between half-stepping ($\overline{HSM}$ = low) and full-stepping ($\overline{HSM}$ = high) by controlling the phase output sequence as show in Figure 5. This line requires the same set-up time as the DIR input, and has the same hold requirement.

INH: When the inhibit input is high, the phase and θ outputs are inhibited (high impedance). STEP pulses received while inhibited will continue to update logic in the IC, but the states will not be reflected at the outputs until inhibit is pulled low. In stepper motor systems, this can be used to save power or to allow the rotor to move freely for manual repositioning.

OPERATING MODES

The UC3517 is a system component capable of many different operating modes, including:

Unipolar Stepper Driver: In its simplest form, the UC3517 can be connected to a stepper motor as a unipolar driver. L_A, L_B, RC and Vss are not used, and may be left open. All other system design considerations mentioned above apply, including choice of motor supply VMM, undershoot diodes and timing considerations.

Unipolar Bilevel Stepper Driver: If increased step rates are desired, the application circuit of Figure 6 makes use of the monostables and emitter followers as well as the configuration mentioned above to provide high-voltage pulses to the motor windings when the phase is turned on. For a given dissipation level, this mode offers faster step rates, and very little additional electrical noise.

The choice of monostable components can be estimated based on the timing relationship of motor current and voltage: V = Ldl/dt. Assuming a fixed secondary supply voltage (V_{SS}), a fixed winding inductance (L_M), a desired winding peak current (I_W), and no back EMF from the motor, we can estimate that $R_TC_T = 1.449\ I_W L_M / V_{SS}$. In practice, these calculations should be confirmed and adjusted to accommodate for effects not modeled.

Voltage-Doubled Mode: The UC3517 can also be used to generate higher voltages than available with the system power supplies using capacitors and diodes. Figure 9 shows how this might be done, and gives some estimates for the component values.

Higher Current Operation: For systems requiring more than 350mA of drive per phase, the UC3717A can be used in conjunction with discrete power transistors or power driver ICs, like the L298. These can be connected as current gain devices that turn on when the phase outputs turn on.

Bipolar Motor Drive: Bipolar motors can be controlled by the UC3517 with the addition of bipolar integrated drivers such as the UC3717A (Figure 8) and the L298, or discrete devices. Care should be taken with discrete devices to avoid potential cross-conduction problems.

LOGIC FLOW GRAPH

The UC3517 contains a bidirectional counter which is decoded to generate the correct phase and Ø outputs. This counter is incremented on every falling edge of the STEP input. Figure 5 shows a graph representing the counter sequence, inputs that determine the next state (DIR and $\overline{HSM}$), and the outputs at each state. Each circle represents a unique logic state, and the four inside circles represent the half-step states.

The four bits inside the circles represent the phase outputs in each state (P_{A1}, P_{A2}, P_{B1}, and P_{B2}). For example, the circle labeled 1010 is immediately entered when the device is powered up, and represents P_{A1} off ("1" or high), P_{A2} on ("0" or low), P_{B1} off ("1" or high) and P_{B2} on ("0" or low). The $Ø_A$ and $Ø_B$ outputs are both low (unidentified).

The arrows in the graph show the state changes. For example, if the IC is in state 0110, DIR is high, $\overline{HSM}$ is high, and STEP falls, the next state will be 0101, and a pulse will be generated on the L_B line by the monostable.

Inhibit will not effect the logic state, but it will cause all phase outputs and both Ø outputs to go high (off). A falling edge on STEP will still cause a state change, but inhibit will have to toggle low for the state to be apparent.

A falling edge on STEP with $\overline{HSM}$ high will cause the counter to advance to the next full step state regardless of whether or not it was in a full step state previously.

No L_A or L_B pulses are generated entering half-states.

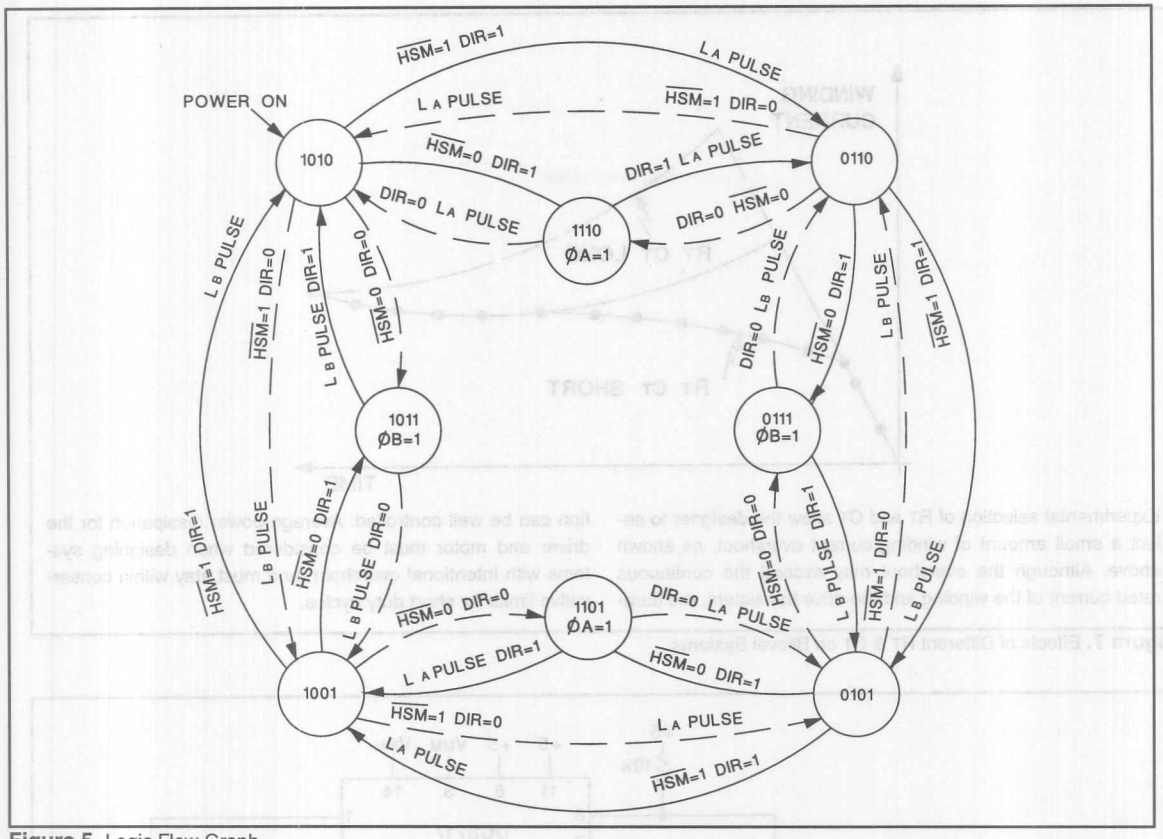
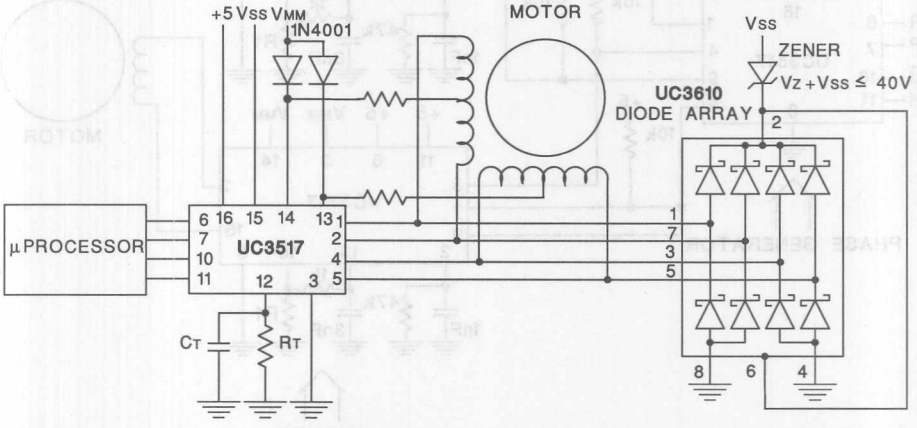
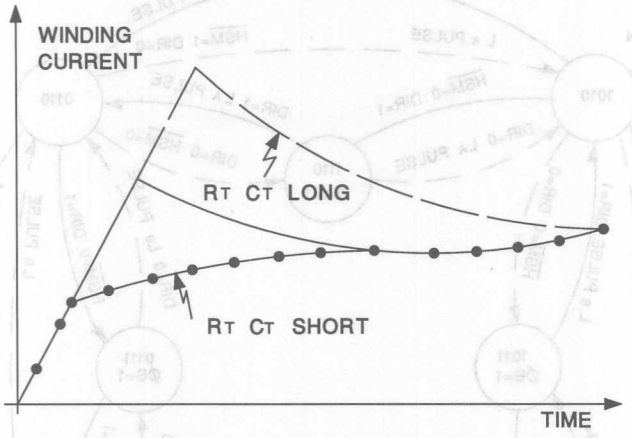


Figure 5. Logic Flow Graph



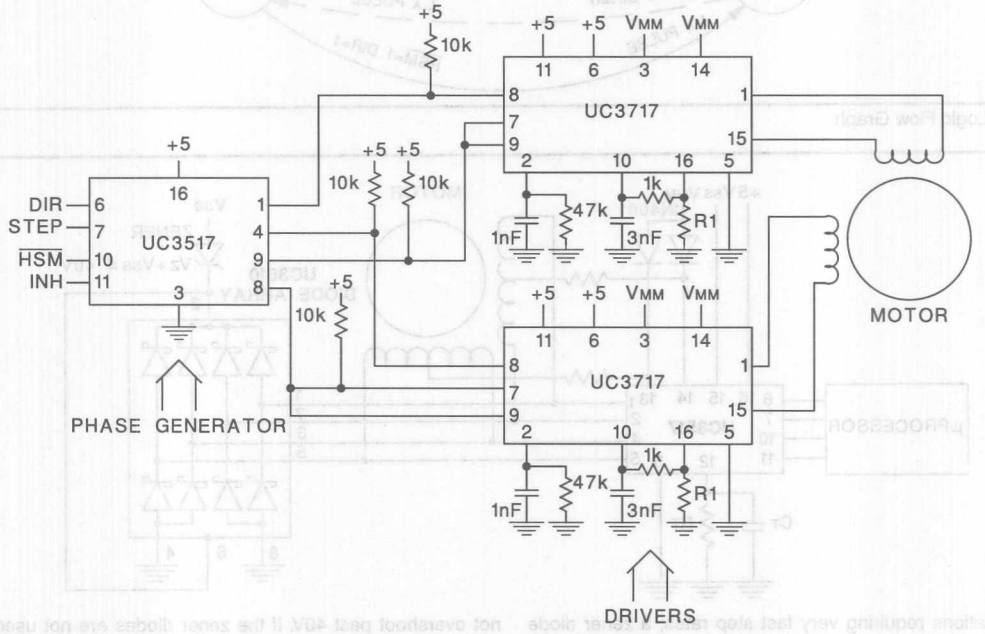
For applications requiring very fast step rates, a zener diode permits windings to discharge at higher voltages, and higher rates. Driver transistor breakdown must be considered when selecting Vss and zener voltage to insure that the outputs will not overshoot past 40V. If the zener diodes are not used and UC3610 pin 2 is connected directly to Vss then higher Vss can be used.

Figure 6. Bilevel Motor Driver



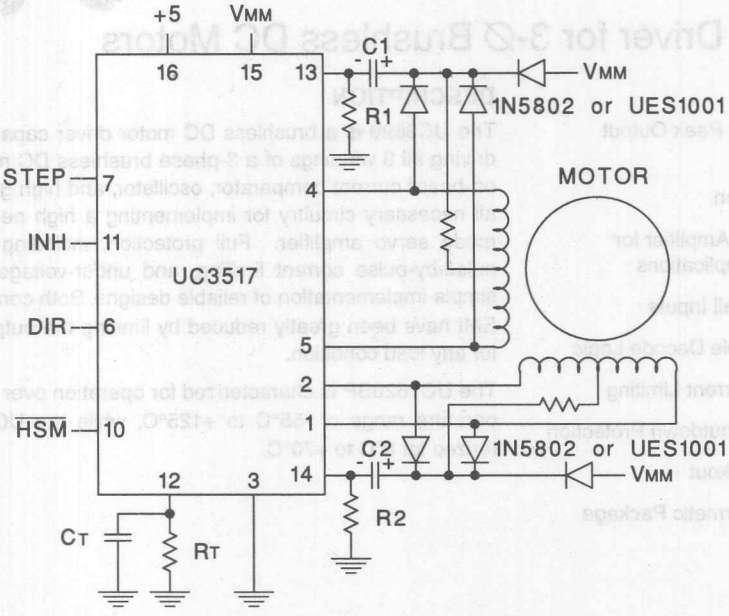
Experimental selection of RT and CT allow the designer to select a small amount of winding current overshoot, as shown above. Although the overshoot may exceed the continuous rated current of the winding and the drive transistors, the duration can be well controlled. Average power dissipation for the driver and motor must be considered when designing systems with intentional overshoot, and must stay within conservative limits for short duty cycles.

Figure 7. Effects of Different RT & CT on Bilevel Systems



In this application, the ØA and ØB outputs of the UC3517 are connected to the current program inputs of the UC3717. This allows the UC3517 inhibit signal to inhibit the UC3717, and also allows half-step operation of the UC3717. Peak motor winding current will be limited to approximately .42V/R1 by chopping.

Figure 8. Interface to UC3717 Bipolar Driver



Although component values can be best optimized experimentally, good starting values speed development. For this design, start with:

$R_T C_T = 3 L_W/R_W$
$C_1 = C_2 = L_W I_R/R_W$
$R_1 = R_2 = 2.9 T_{MIN}/C1$

where:

L_W is winding inductance,
R_W is winding resistance,
I_R is rated winding current, and
T_{MIN} is minimum step period expected.

Figure 9. Using the UC3517 as a Voltage Doubler

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

Switchmode Driver for 3-∅ Brushless DC Motors

FEATURES

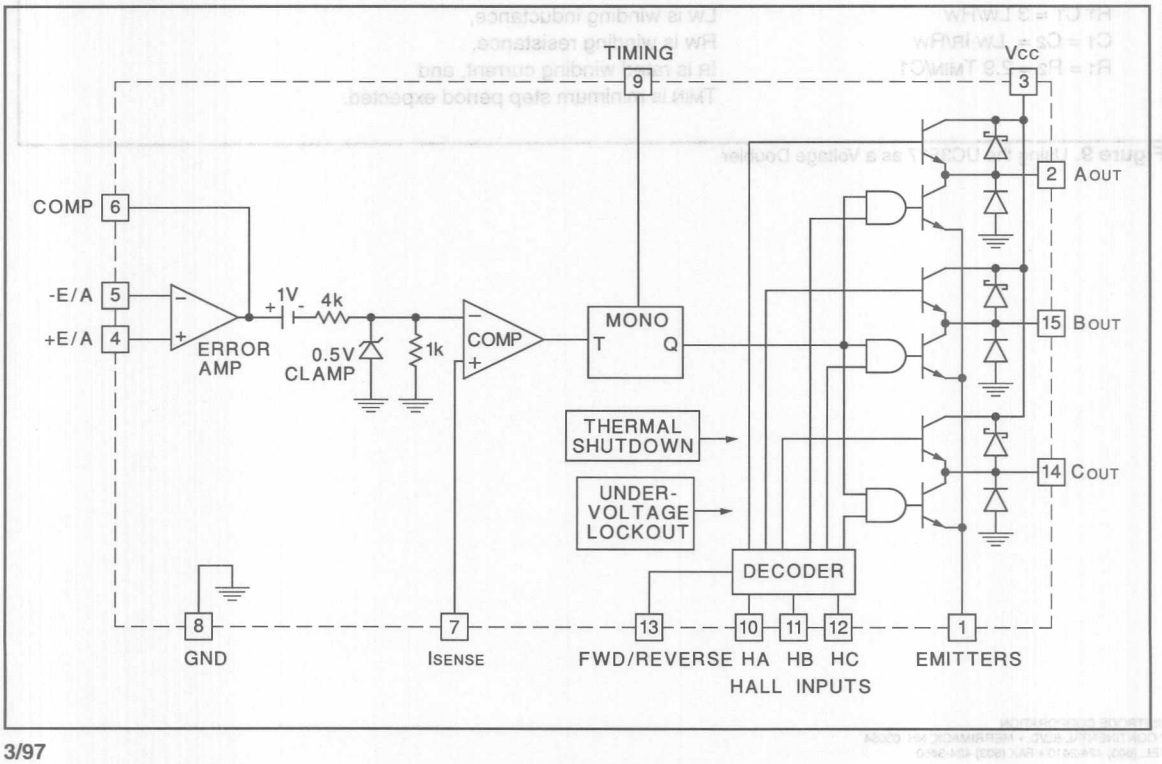
- 2A Continuous, 3A Peak Output Current
- 8V to 40V Operation
- Internal High Gain Amplifier for Velocity Control Applications
- TTL Compatible Hall Inputs
- Mask Programmable Decode Logic
- Pulse-by-Pulse Current Limiting
- Internal Thermal Shutdown Protection
- Under-Voltage Lockout
- Available in SP Hermetic Package

DESCRIPTION

The UC3620 is a brushless DC motor driver capable of decoding and driving all 3 windings of a 3-phase brushless DC motor. In addition, an on-board current comparator, oscillator, and high gain Op-Amp provide all necessary circuitry for implementing a high performance, chopped mode servo amplifier. Full protection, including thermal shutdown, pulse-by-pulse current limiting, and under-voltage lockout aid in the simple implementation of reliable designs. Both conducted and radiated EMI have been greatly reduced by limiting the output dv/dt to 150V/µs for any load condition.

The UC1620SP is characterized for operation over the full military temperature range of -55°C to +125°C, while the UC3620SP is characterized for 0°C to +70°C.

BLOCK DIAGRAM



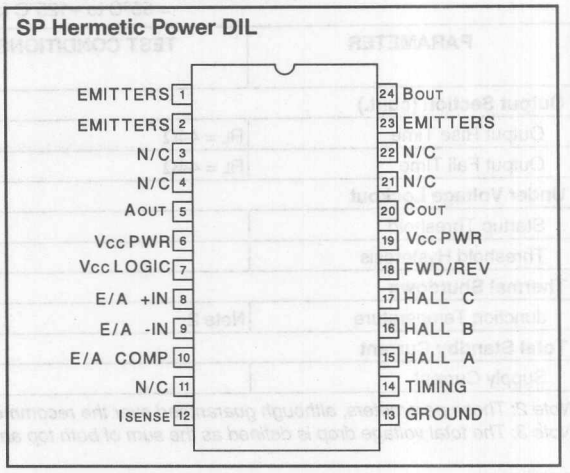
ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage, Vcc 40V
Output Current, Source or Sink
  Non-Repetitive (t = 100µsec), Io 3A
  Repetitive (80% on - 20% off; tON = 10ms) 2.5A
  DC Operation 2A
Analog Inputs . . . . . -0.3 to +Vcc
Logic Inputs . . . . . -0.3 to +Vcc
Total Power Dissipation (at TCASE = 75° C)
  for SP Package (Note 2) 15W
Storage Temperature . . . . . -65°C to +150°C
Operating Junction Temperature . . . . . -55°C to +150°C

Note 1: All voltages are with respect to ground. Currents are positive into, negative out of the specified terminal.
Note 2: Consult Packaging Section of Databook for thermal limitations and considerations of package.

CONNECTION DIAGRAMS

SP Hermetic Power DIL



ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, these specifications apply for TA = 0°C to 70°C for 3620; TA = 55°C to +125°C for UC1620; Vcc = 20V, RT = 20V, RT = 10k, CT = -2.2nF. TA=TJ.

PARAMETER	TEST CONDITIONS	UC3620			UC1620			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Error Amplifier Section								
Input Offset Voltage			1.5	10		1.5	10	mV
Input Bias Current			-.25	-2.0		-.25	-2.0	µA
Input Offset Current			15	250		15	250	nA
Common Mode Range	Vcc = 8V to 40V	0		VIN-2	0		VIN-2	V
Open Loop Gain	ΔVCOMP = 1V to 4V	80	100		75	100		dB
Unity Gain Bandwidth	TJ = 25°C, Note 2		0.8			0.8		MHz
Output Sink Current	VCOMP = 1V		2			2		mA
Output Source Current	VCOMP = 4V		8			8		mA
Current Sense Section								
Input Bias Current			-2.0	-5		-2.0	-5	µA
Internal Clamp		.425	0.5	.575	.405	0.5	.595	V
Divider Gain		.180	0.2	.220	.170	0.2	.230	V/V
Internal Offset Voltage		.8	1.0	1.2	.75	1.0	1.25	V
Timing Section								
Output Off Time		18	20	22	17	20	23	µs
Upper Mono Threshold			5.0			5.0		V
Lower Mono Threshold			2.0			2.0		V
Decoder Section								
High-Level Input Voltage		2.2			2.5			V
Low-Level Input Voltage				0.8			0.8	V
High-Level Input Current				10			10	µA
Low-Level Input Current		-10			-10			µA
Output Section								
Output Leakage Current	Vcc = 40V			500			1500	µA
VF1 Schottky Diode	Io = 2A		1.5	2.0		1.5	2.0	V
VF1 Substrate Diode	Io = 2A		2.2	3.0		2.2	3.0	V
Total Output Voltage Drop	Io = 2A, Note 3		3.0	3.6		3.0	3.6	V

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C for 3620; T_A = 55°C to +125°C for UC1620; V_{CC} = 20V, R_T = 20V, R_T = 10k, C_T = -2.2nF. T_A=T_J.

PARAMETER	TEST CONDITIONS	UC3620			UC1620			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Output Section (cont.)								
Output Rise Time	R_L = 44Ω		150			150		ns
Output Fall Time	R_L = 44Ω		150			150		ns
Under Voltage Lockout								
Startup Threshold				8.0			8.0	V
Threshold Hysteresis			0.5			0.5		V
Thermal Shutdown								
Junction Temperature	Note 2	150		180	150		180	°C
Total Standby Current								
Supply Current			32	55		32	55	mA

Note 2: These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.
Note 3: The total voltage drop is defined as the sum of both top and bottom side driver.

TABLE 1

STEP	FWD/ REV	Ha	Hb	Hc	AOUT	BOUT	COUT
1	1	1	0	1	H	L	O
2	1	1	0	0	H	O	L
3	1	1	1	0	O	H	L
4	1	0	1	0	L	H	O
5	1	0	1	1	L	O	H
6	1	0	0	1	O	L	H
1	0	1	0	1	L	H	O
2	0	1	0	0	L	O	H
3	0	1	1	0	O	L	H
4	0	0	1	0	H	L	O
5	0	0	1	1	H	O	L
6	0	0	0	1	O	H	L

H = HIGH OUTPUT
L = LOW OUTPUT
O = OPEN OUTPUT

CIRCUIT DESCRIPTION

The UC3620 is designed for implementation of a complete 3-Ø brushless DC servo drive using a minimum number of external components. Below is a functional description of each major circuit feature.

DECODER

Table 1 shows the decoding scheme used in the UC3620 to decode and drive each of three high current totem pole output stages. A forward/reverse signal, pin 13, is used to provide direction. At any point in time, one driver is sourcing, one driver is sinking, and the remaining driver is off or tri-stated. Pulse width modulation is accomplished by turning the sink driver off during the monostable reset time, producing a fixed off-time chop mode. Controlled output rise and fall times help reduce electrical switching noise while maintaining relatively small switching losses. Hall lines require pull-up resistors.

CURRENT SENSING

Referring to Figure 1, emitter current is sensed across Rs and fed back through a low pass filter to the current sense pin 7. This filter is required to eliminate false triggering of the monostable due to leading edge current spikes. Actual filter values, although somewhat dependent on external loads, will generally be in the 1kΩ and 1000pF range.

TIMING

An R-C time constant on pin 9 is used by the monostable to generate a fixed off time at the outputs according to the formula:

$$T_{OFF} = .916R_TC_T$$

As the peak current in the emitters approaches the value at the minus (-) input of the on-board comparator, the monostable is triggered, causing the outputs to be turned

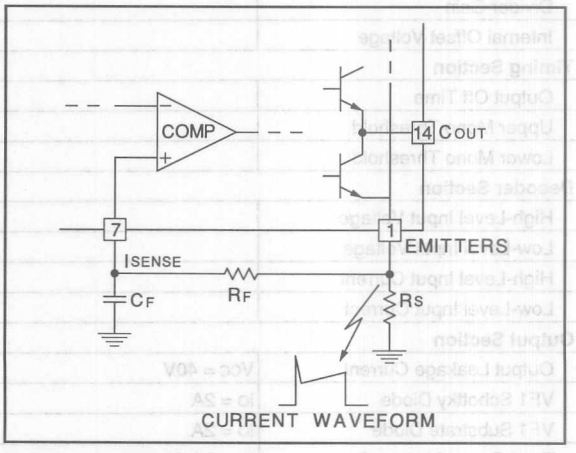


Figure 1. Current Sense Filter

CIRCUIT DESCRIPTION (cont.)

off. On time is determined by the amount of time required for motor current to increase to the value required to re-trip the monostable. A timing sequence of these events is shown in Figure 2.

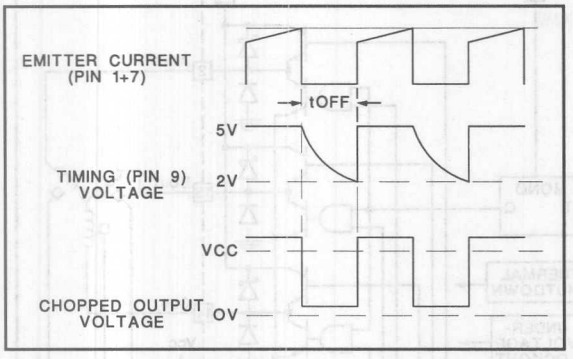


Figure 2. Chopped Mode Timing Diagram

CURRENT LIMIT

Since peak current is being controlled at all times by the internal comparator, a simple voltage clamp at its negative (-) input will limit peak current to a maximum value. A fixed 0.5V internal clamp has been included on the UC3620, and any current spike in the output which generates a sensed voltage greater than 0.5V will immediately shut down the outputs. Actual peak current values may be programmed by selecting the appropriate value of Rs according to the formula:

$$Rs = \frac{0.5}{I_{CURRENTLIMIT}}$$

Since peak current is being controlled at all times by the internal comparator, a simple voltage clamp at its negative (-) input will limit peak current to a maximum value. A fixed 0.5V internal clamp has been included on the UC3620, and any current spike in the output which generates a sensed voltage greater than 0.5V will immediately shut down the outputs. Actual peak current values may be programmed by selecting the appropriate value of Rs according to the formula:

$$Rs = \frac{0.5}{I_{CURRENTLIMIT}}$$

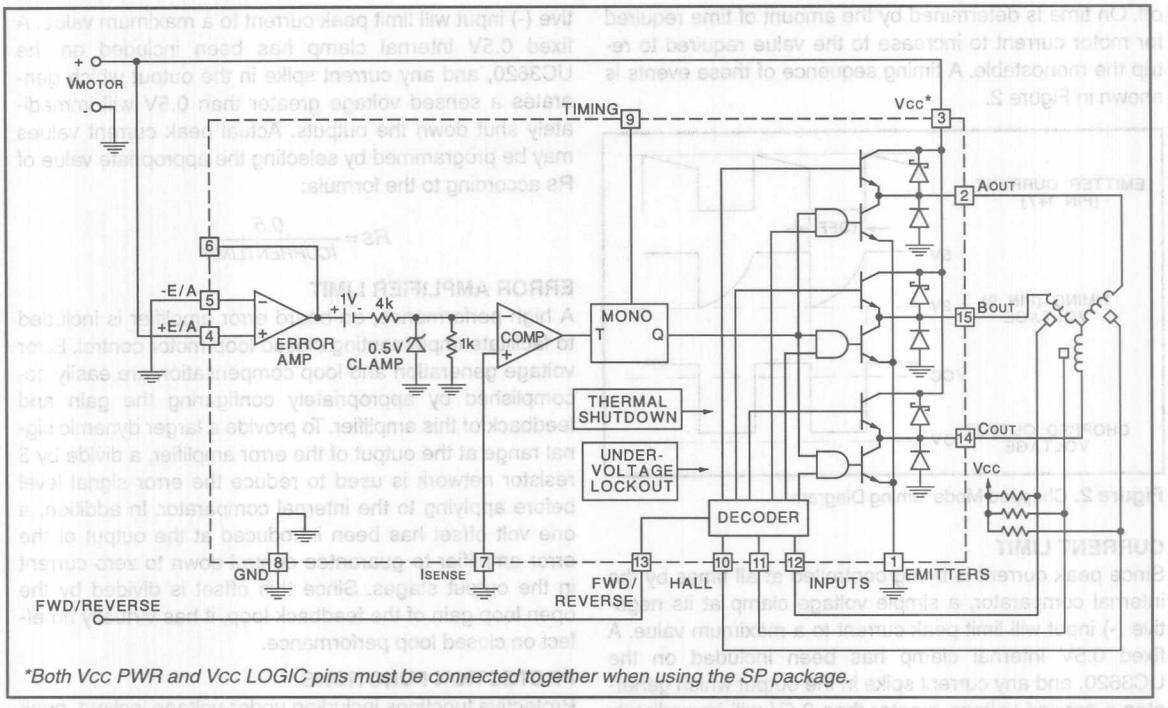
ERROR AMPLIFIER LIMIT

A high performance, on-board error amplifier is included to facilitate implementing closed loop motor control. Error voltage generation and loop compensation are easily accomplished by appropriately configuring the gain and feedback of this amplifier. To provide a larger dynamic signal range at the output of the error amplifier, a divide by 5 resistor network is used to reduce the error signal level before applying to the internal comparator. In addition, a one volt offset has been introduced at the output of the error amplifier to guarantee control down to zero current in the output stages. Since this offset is divided by the open loop gain of the feedback loop, it has virtually no effect on closed loop performance.

PROTECTION FUNCTIONS

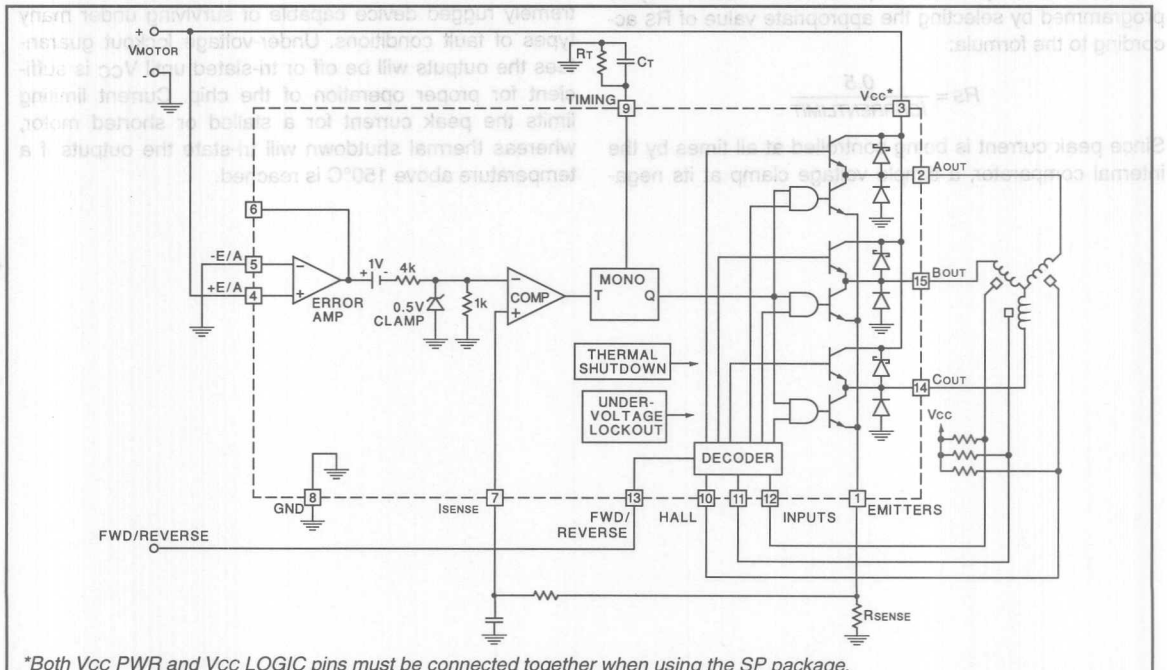
Protective functions including under-voltage lockout, peak current limiting, and thermal shutdown, provide an extremely rugged device capable of surviving under many types of fault conditions. Under-voltage lockout guarantees the outputs will be off or tri-slated until V_{CC} is sufficient for proper operation of the chip. Current limiting limits the peak current for a stalled or shorted motor, whereas thermal shutdown will tri-state the outputs if a temperature above 150°C is reached.

TYPICAL APPLICATIONS



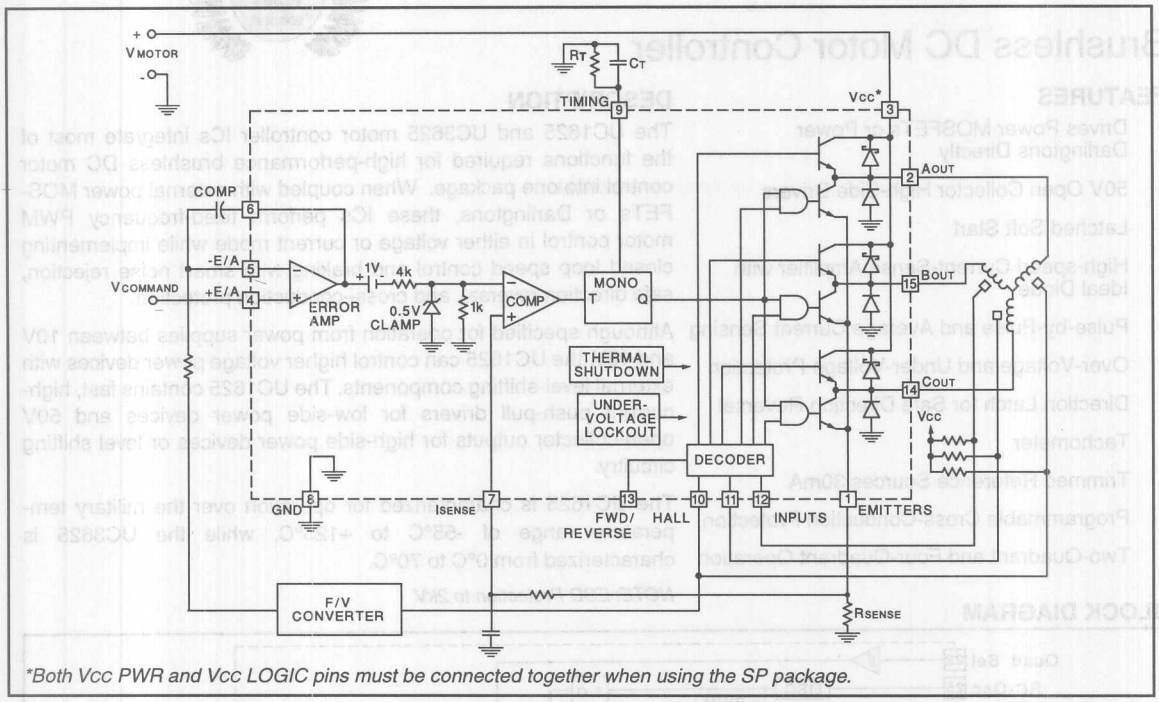
Both Vcc PWR and Vcc LOGIC pins must be connected together when using the SP package.

3-∅ Brushless DC Open Loop Motor Drive



Both Vcc PWR and Vcc LOGIC pins must be connected together when using the SP package.

3-∅ Brushless DC Open Loop Motor with Current Limit at 2A.



Both Vcc PWR and Vcc LOGIC pins must be connected together when using the SP package.

Closed Loop Speed Control Servo

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

UNITRODE

UC1625
UC3625

Brushless DC Motor Controller

FEATURES

- Drives Power MOSFETs or Power Darlingtons Directly
- 50V Open Collector High-Side Drivers
- Latched Soft Start
- High-speed Current-Sense Amplifier with Ideal Diode
- Pulse-by-Pulse and Average Current Sensing
- Over-Voltage and Under-Voltage Protection
- Direction Latch for Safe Direction Reversal
- Tachometer
- Trimmed Reference Sources 30mA
- Programmable Cross-Conduction Protection
- Two-Quadrant and Four-Quadrant Operation

DESCRIPTION

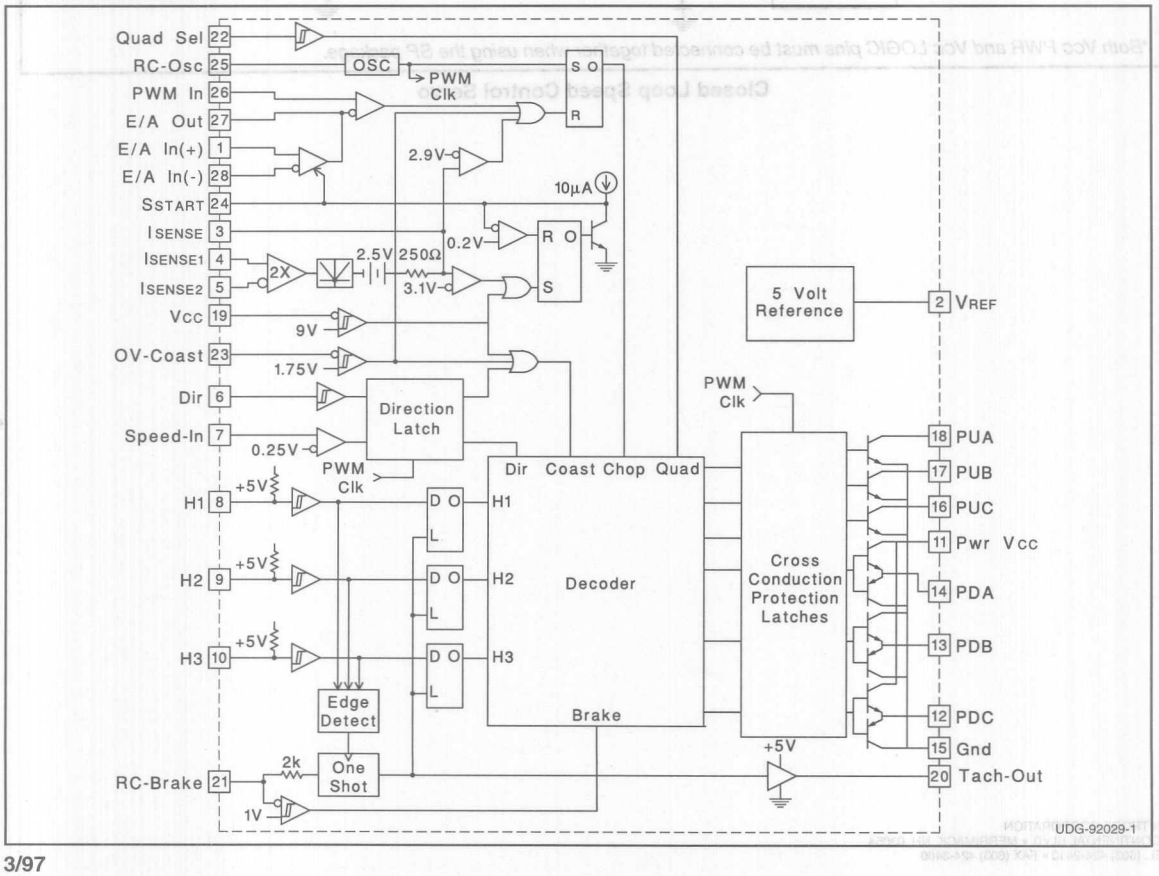
The UC1625 and UC3625 motor controller ICs integrate most of the functions required for high-performance brushless DC motor control into one package. When coupled with external power MOSFETs or Darlingtons, these ICs perform fixed-frequency PWM motor control in either voltage or current mode while implementing closed loop speed control and braking with smart noise rejection, safe direction reversal, and cross–conduction protection.

Although specified for operation from power supplies between 10V and 18V, the UC1625 can control higher voltage power devices with external level-shifting components. The UC1625 contains fast, high-current push-pull drivers for low-side power devices and 50V open-collector outputs for high-side power devices or level shifting circuitry.

The UC1625 is characterized for operation over the military temperature range of -55°C to +125°C, while the UC3625 is characterized from 0°C to 70°C.

NOTE: ESD Protection to 2kV

BLOCK DIAGRAM



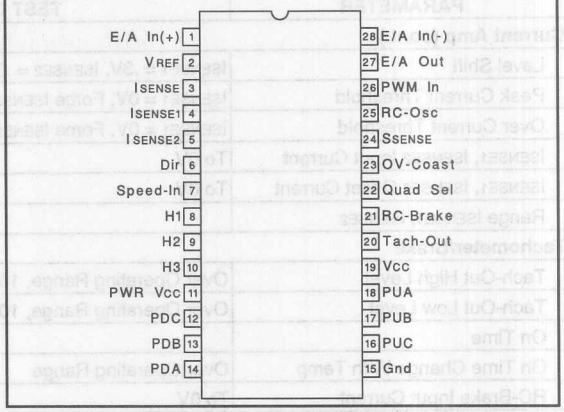
ABSOLUTE MAXIMUM RATINGS

V_{CC} Supply Voltage ..... +20V
Pwr V_{CC} Supply Voltage ..... +20V
PWM In ..... -0.3 to 6V
E/A IN(+), E/A IN(–) ..... -0.3 to 12V
I_{SENSE1}, I_{SENSE2} ..... -1.3 to 6V
OV–Coast, Dir, Speed-In, S_{START}, Quad Sel ..... -0.3 to 8V
H1, H2, H3 ..... -0.3 to 12V
PU Output Voltage ..... -0.3 to 50V
PU Output Current ..... +200 mA continuous
PD Output Current ..... ±200 mA continuous
E/A Output Current ..... ±10 mA
I SENSE Output Current ..... -10 mA
Tach Out Output Current ..... ±10 mA
V_{REF} Output Current ..... -50 mA continuous
Operating Temperature Range UC1625 ..... -55°C to 125°C
Operating Temperature Range UC3625 ..... 0°C to 70°C

Note 1: Currents are positive into and negative out of the specified terminal.
Note 2: Consult Unitrode Integrated Circuits databook for information regarding thermal specifications and limitations of packages.

CONNECTION DIAGRAM

DIL-28 (TOP VIEW)
J or N PACKAGE



Note 3: This pinout applies to the SOIC (DW), PLCC (Q), and LCC (L) packages (ie. pin 22 has the same function on all packages.)

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, these specifications apply for: T_A = 25°C; Pwr V_{CC} = V_{CC} = 12V; R_{OSC} = 20k to V_{REF}; C_{OSC} = 2nF; R_{TACH} = 33k; C_{TACH} = 10nF; and all outputs unloaded. T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Overall					
Supply current	Over Operating Range		14.5	30.0	mA
V_{CC} Turn-On Threshold	Over Operating Range	8.65	8.95	9.45	V
V_{CC} Turn-Off Threshold	Over Operating Range	7.75	8.05	8.55	V
Overvoltage/Coast					
OV-Coast Inhibit Threshold	Over Operating Range	1.65	1.75	1.85	V
OV-Coast Restart Threshold		1.55	1.65	1.75	V
OV-Coast Hysteresis		0.05	0.10	0.15	V
OV-Coast Input Current		-10	-1	0	µA
Logic Inputs					
H1, H2, H3 Low Threshold	Over Operating Range	0.8	1.0	1.2	V
H1, H2, H3 High Threshold	Over Operating Range	1.6	1.9	2.0	V
H1, H2, H3 Input Current	Over Operating Range, to 0V	-400	-250	-120	µA
Quad Sel, Dir Thresholds	Over Operating Range	0.8	1.4	2.0	V
Quad Sel Hysteresis			70		mV
Dir Hysteresis			0.6		V
Quad Sel Input Current		-30	50	150	µA
Dir Input Current		-30	-1	30	µA
PWM Amp/Comparator					
E/A In(+), E/A In(-) Input Current	To 2.5V	-5.0	-0.1	5.0	µA
PWM In Input Current	To 2.5V	0	3	30	µA
Error Amp Input Offset	0V < $V_{COMMON-MODE}$ < 3V	-10		10	mV
Error Amp Voltage Gain		70	90		dB
E/A Out Range		0.25		3.50	V
S_{START} Pull-up Current	To 0V	-16	-10	-5	µA
S_{START} Discharge Current	To 2.5V	0.1	0.4	3.0	mA
S_{START} Restart Threshold		0.1	0.2	0.3	V
Current Amp					
Gain	I_{SENSE1} = .3V, I_{SENSE2} = .5V to .7V	1.75	1.95	2.15	V/V

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, these specifications apply for: T_A = 25°C; PWR-V_{CC} = V_{CC} = 12V; R_{OSC} = 20k to V_{REF}; C_{OSC} = 2nF; R_{TACH} = 33k; C_{TACH} = 10nF; and all outputs unloaded. T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Current Amp (cont.)					
Level Shift	I_{SENSE1} = .3V, I_{SENSE2} = .3V	2.4	2.5	2.65	V
Peak Current Threshold	I_{SENSE1} = 0V, Force I_{SENSE2}	0.14	0.20	0.26	V
Over Current Threshold	I_{SENSE1} = 0V, Force I_{SENSE2}	0.26	0.30	0.36	V
I_{SENSE1}, I_{SENSE2} Input Current	To 0V	-850	-320	0	µA
I_{SENSE1}, I_{SENSE2} Offset Current	To 0V		±2	±12	µA
Range I_{SENSE1}, I_{SENSE2}		-1		2	V
Tachometer/Brake					
Tach-Out High Level	Over Operating Range, 10k to 2.5V	4.7	5	5.3	V
Tach-Out Low Level	Over Operating Range, 10k to 2.5V			0.2	V
On Time		170	220	280	µs
On Time Change With Temp	Over Operating Range		.1		%
RC-Brake Input Current	To 0V	-4.0	-1.9		mA
Threshold to Brake, RC-Brake	Over Operating Range	0.8	1.0	1.2	V
Brake Hysteresis, RC-Brake			0.09		V
Speed-In Threshold	Over Operating Range	220	257	290	mV
Speed-In Input Current		-30	-5	30	µA
Low-Side Drivers					
Voh, -1mA, Down From V_{CC}	Over Operating Range		1.60	2.1	
V Voh, -50mA, Down From V_{CC}	Over Operating Range		1.75	2.2	V
Vol, 1mA	Over Operating Range		0.05	0.4	V
Vol, 50mA	Over Operating Range		0.36	0.8	V
Rise/Fall Time	10% to 90% Slew Time, into 1nF		50		ns
High-Side Drivers					
Vol, 1mA	Over Operating Range		0.1	0.4	V
Vol, 50mA	Over Operating Range		1.0	1.8	V
Leakage Current	Output Voltage = 50V			25	µA
Fall Time	10% to 90% Slew Time, 50mA Load		50		ns
Oscillator					
Frequency		40	50	60	kHz
Frequency	Over Operating Range	35		65	kHz
Reference					
Output Voltage		4.9	5.0	5.1	V
Output Voltage	Over Operating Range	4.7	5.0	5.3	V
Load Regulation	0mA to -20mA Load	-40	-5		mV
Line Regulation	10V to 18V V_{CC}	-10	-1	10	mV
Short Circuit Current	Over Operating Range	50	100	150	mA
Miscellaneous					
Output Turn-On Delay			1		µs
Output Turn-Off Delay			1		µs

PIN DESCRIPTIONS:

Dir, Speed-In: The position decoder logic translates the Hall signals and the Dir signal to the correct driver signals (PUs and PDs). To prevent output stage damage, the signal on Dir is first loaded into a direction latch, then shifted through a two-bit register.

As long as Speed-In is less than 250mV, the direction latch is transparent. When Speed-In is higher than 250mV, the direction latch inhibits all changes in direction. Speed-In can be connected to Tach-Out through a filter, so that the direction latch is only transparent when the motor is spinning slowly, and has too little stored energy to damage power devices.

PIN DESCRIPTIONS (cont.):

Additional circuitry detects when the input and output of the direction latch are different, or when the input and output of the shift register are different, and inhibits all output drives during that time. This can be used to allow the motor to coast to a safe speed before reversing.
The shift register guarantees that direction can't be changed instantaneously. The register is clocked by the PWM oscillator, so the delay between direction changes is always going to be between one and two oscillator periods. At 40kHz, this corresponds to a delay of between 25µs and 50µs. Regardless of output stage, 25µs dead time should be adequate to guarantee no overlap cross-conduction. Toggling DIR will cause an output pulse on Tach-Out regardless of motor speed.

E/A In(+), E/A In(-), E/A Out, PWM In: E/A In(+) and E/A In(-) are not internally committed to allow for a wide variety of uses. They can be connected to the ISENSE, to Tach-Out through a filter, to an external command voltage, to a D/A converter for computer control, or to another op amp for more elegant feedback loops. The error amplifier is compensated for unity gain stability, so E/A Out can be tied to E/A In(-) for feedback and major loop compensation.
E/A Out and PWM In drive the PWM comparator. For voltage-mode PWM systems, PWM In can be connected to RC-Osc. The PWM comparator clears the PWM latch, commanding the outputs to chop.
The error amplifier can be biased off by connecting E/A In(-) to a higher voltage than E/A In(+). When biased off, E/A Out will appear to the application as a resistor to ground. E/A Out can then be driven by an external amplifier.

GND: All thresholds and outputs are referred to the GND pin except for the PD and PU outputs.

H1, H2, H3: The three shaft-position sensor inputs consist of hysteresis comparators with input pull-up resistors. Logic thresholds meet TTL specifications and can be driven by 5V CMOS, 12V CMOS, NMOS, or open-collectors.
Connect these inputs to motor shaft position sensors that are positioned 120 electrical degrees apart. If noisy signals are expected, zener clamp and filter these inputs with 6V zeners and an RC filter. Suggested filtering components are 1k and 2nF. Edge skew in the filter is not a problem, because sensors normally generate modified Gray code with only one output changing at a time, but rise and fall times must be shorter than 20µs for correct tachometer operation.
Motors with 60 electrical degree position sensor coding can be used if one or two of the position sensor signals is inverted.

ISENSE1, ISENSE2, ISENSE: The current sense amplifier has a fixed gain of approximately two. It also has a built-in level shift of approximately 2.5 volts. The signal appearing on ISENSE is:

$$I_{SENSE} = 2.5V + (2 * ABS (I_{SENSE1} - I_{SENSE2}))$$

ISENSE1 and ISENSE2 are interchangeable and can be used as differential inputs. The differential signal applied can be as high as ±0.5V before saturation.
If spikes are expected on ISENSE1 or ISENSE2, they are best filtered by a capacitor from ISENSE to ground. Filtering this way allows fast signal inversions to be correctly processed by the absolute value circuit. The peak-current comparator allows the PWM to enter a current-limit mode with current in the windings never exceeding approximately 0.2V/RSENSE. The over current comparator provides a fail-safe shutdown in the unlikely case of current exceeding 0.3V/RSENSE. Then, soft start is commanded, and all outputs are turned off until the high current condition is removed.
It is often essential to use some filter driving ISENSE1 and ISENSE2 to reject extreme spikes and to control slew rate. Reasonable starting values for filter components might be 250Ω series resistors and a 5nF capacitor between ISENSE1 and ISENSE2. Input resistors should be kept small and matched to maintain gain accuracy.

OV-Coast: This input can be used as an over-voltage shutdown in put, as a coast input, or both. This input can be driven by TTL, 5V CMOS, or 12V CMOS.

PDA, PDB, PDC: These outputs can drive the gates of N-Channel power MOSFETs directly or they can drive the bases of power Darlingtons if some form of current limiting is used. They are meant to drive low-side power devices in high-current output stages. Current available from these pins can peak as high as 0.5A. These outputs feature a true totem-pole output stage. Beware of exceeding IC power dissipation limits when using these outputs for high continuous currents. These outputs pull high to turn a "low-side" device on (active high).

PUA, PUB, PUC: These outputs are open-collector, high-voltage drivers that are meant to drive high-side power devices in high-current output stages. These are active low outputs, meaning that these outputs pull low to command a high-side device on. These outputs can drive low-voltage PNP Darlingtons and P-channel MOSFETs directly, and can drive any high-voltage device using external charge-pump techniques, transformer signal coupling, cascode level-shift transistors, or opto-isolated drive. (See applications).

PWR VCC: This supply pin carries the current sourced by the PD outputs. When connecting PD outputs directly to the bases of power Darlingtons, the PWR VCC pin can be current limited with a resistor. Darlington outputs can also be "Baker Clamped" with diodes from collectors back to PWR VCC. (See Applications)

PIN DESCRIPTIONS (cont.):

Quad Sel: The IC can chop power devices in either of two modes, referred to as "two-quadrant" (Quad Sel low) and "four-quadrant" (Quad Sel high). When two-quadrant chopping, the pull-down power devices are chopped by the output of the PWM latch while the pull-up drivers remain on. The load will chop into one commutation diode, and except for back-EMF, will exhibit slow discharge current and faster charge current. Two-quadrant chopping can be more efficient than four-quadrant.

When four-quadrant chopping, all power drivers are chopped by the PWM latch, causing the load current to flow into two diodes during chopping. This mode exhibits better control of load current when current is low, and is preferred in servo systems for equal control over acceleration and deceleration. The Quad Sel input has no effect on operation during braking.

RC-Brake: Each time the Tach-Out pulses, the capacitor tied to RC-Brake discharges from approximately 3.33V down to 1.67V through a resistor. The tachometer pulse width is approximately $T = 0.67\ R_T\ C_T$, where R_T and C_T are a resistor and capacitor from RC-Brake to ground. Recommended values for R_T are 10k to 500k, and recommended values for C_T are 1nF to 100nF, allowing times between 5µs and 10ms. Best accuracy and stability are achieved with values in the centers of those ranges.

RC-Brake also has another function. If RC-Brake pin is pulled below the brake threshold, the IC will enter brake mode. This mode consists of turning off all three high-side devices, enabling all three low-side devices, and disabling the tachometer. The only things that inhibit low-side device operation in braking are low-supply, exceeding peak current, OV-Coast command, and the PWM comparator signal. The last of these means that if current sense is implemented such that the signal in the current sense amplifier is proportional to braking current, the low-side devices will brake the motor with current control. (See applications) Simpler current sense connections will result in uncontrolled braking and potential damage to the power devices.

RC-Osc: The UC3625 can regulate motor current using fixed-frequency pulse width modulation (PWM). The RC-Osc pin sets oscillator frequency by means of timing resistor R_{OSC} from the RC-Osc pin to V_{REF} and capacitor C_{OSC} from RC-Osc to Gnd. Resistors 10k to 100k and capacitors 1nF to 100nF will work best, but frequency should always be below 500kHz. Oscillator frequency is approximately:

$$F = 2 / R_{OSC}C_{OSC}$$

Additional components can be added to this device to cause it to operate as a fixed off-time PWM rather than a fixed frequency PWM, using the RC-Osc pin to select the monostable time constant.

The voltage on the RC-Osc pin is normally a ramp of about 1.2V peak-to-peak, centered at approximately 1.6V. This ramp can be used for voltage-mode PWM control, or can be used for slope compensation in current-mode control.

S_{START}: Any time that V_{CC} drops below threshold or the sensed current exceeds the over-current threshold, the soft-start latch is set. When set, it turns on a transistor that pulls down on S_{START}. Normally, a capacitor is connected to this pin, and the transistor will completely discharge the capacitor. A comparator senses when the NPN transistor has completely discharged the capacitor, and allows the soft-start latch to clear when the fault is removed. When the fault is removed, the soft-start capacitor will charge from the on-chip current source.

S_{START} clamps the output of the error amplifier, not allowing the error amplifier output voltage to exceed S_{START} regardless of input. The ramp on RC-Osc can be applied to PWM In and compared to E/A Out. With S_{START} discharged below 0.2V and the ramp minimum being approximately 1.0V, the PWM comparator will keep the PWM latch cleared and the outputs off. As S_{START} rises, the PWM comparator will begin to duty-cycle modulate the PWM latch until the error amplifier inputs overcome the clamp. This provides for a safe and orderly motor start-up from an off or fault condition.

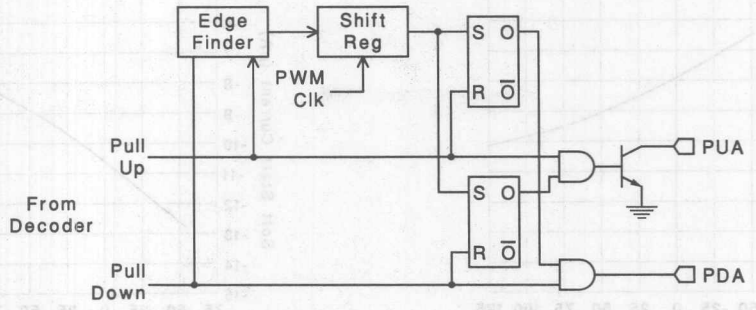
Tach-Out: Any change in the H1, H2, or H3 inputs loads data from these inputs into the position sensor latches. At the same time data is loaded, a fixed-width 5V pulse is triggered on Tach-Out. The average value of the voltage on Tach-Out is directly proportional to speed, so this output can be used as a true tachometer for speed feedback with an external filter or averaging circuit.

Whenever Tach-Out is high, the position latches are inhibited, such that during the noisiest part of the commutation cycle, additional commutations are not possible. Although this will effectively set a maximum rotational speed, the maximum speed can be set above the highest expected speed, preventing false commutation and chatter.

V_{CC}: This device operates with supplies between 10V and 18V. Under-voltage lockout keeps all outputs off below 7.5V, insuring that the output transistors never turn on until full drive capability is available. Bypass V_{CC} to ground with an 0.1µF ceramic capacitor. Using a 10µF electrolytic bypass capacitor as well can be beneficial in applications with high supply impedance.

V_{REF}: This pin provides regulated 5 volts for driving Hall-effect devices and speed control circuitry. V_{REF} will reach +5V before V_{CC} enables, ensuring that Hall-effect devices powered from V_{REF} will become active before the UC3625 drives any output. Although V_{REF} is current limited, operation over 30mA is not advised. For proper performance V_{REF} should be bypassed with at least a 0.1µF capacitor to ground.

CROSS CONDUCTION PREVENTION



The UC3625 inserts delays to prevent cross conduction due to overlapping drive signals. However, some thought must always be given to cross conduction in output stage design because no amount of dead time can prevent fast slewing signals from coupling drive to a power device through a parasitic capacitance.

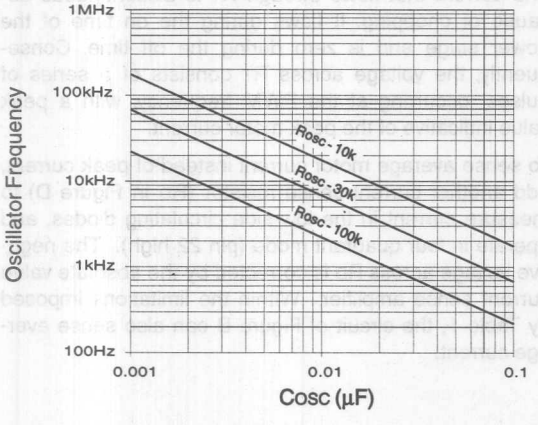
The UC3625 contains input latches that serve as noise blanking filters. These latches remain transparent through any phase of a motor rotation and latch immediately after an input transition is detected. They remain latched for two cycles of the PWM oscillator. At a PWM oscillator speed of 20kHz, this corresponds to 50µs to 100µs of blank time which limits maximum rotational speed to 100kRPM for a motor with six transitions per rotation or 50kRPM for a motor with 12 transitions per rotation.

This prevents noise generated in the first 50µs of a transition from propagating to the output transistors and causing cross–conduction or chatter.

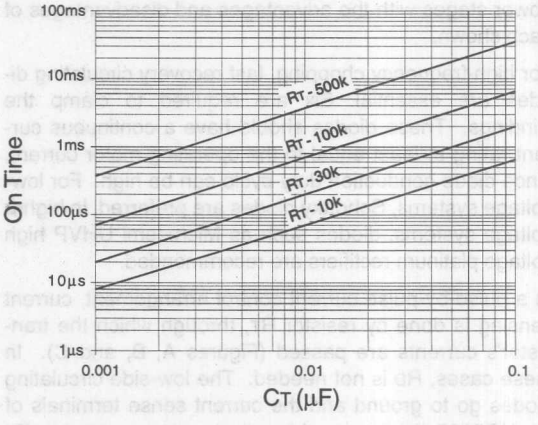
The UC3625 also contains six flip flops corresponding to the six output drive signals. One of these flip flops is set every time that an output drive signal is turned on, and cleared two PWM oscillator cycles after that drive signal is turned off. The output of each flip flop is used to inhibit drive to the opposing output. (see below) In this way, it is impossible to turn on driver PUA and PDA at the same time. It is also impossible for one of these drivers to turn on without the other driver having been off for at least two PWM oscillator clocks.

TYPICAL CHARACTERISTICS:

Oscillator Frequency vs Cosc and Rosc

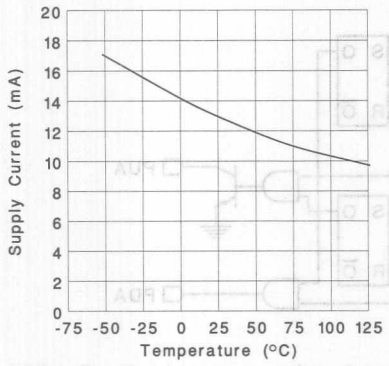


Tachometer On Time vs RT and CT

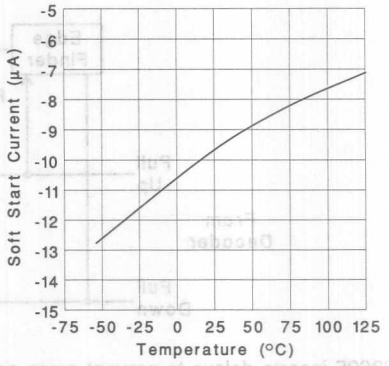


TYPICAL CHARACTERISTICS (cont.):

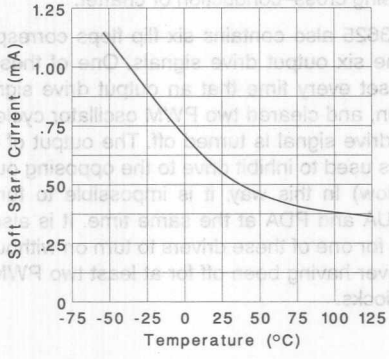
Supply Current vs Temperature



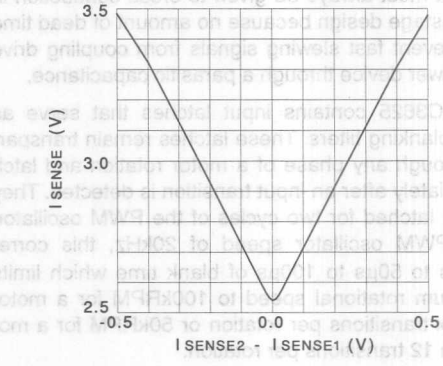
Soft Start Pull-Up Current vs Temperature



Soft Start Discharge Current vs Temperature



Current Sense Amplifier Transfer Function



POWER STAGE DESIGN:

The UC3625 is useful in a wide variety of applications, including high-power in robotics and machinery. The power output stages used in such equipment can take a number of forms, according to the intended performance and purpose of the system. Below are four different power stages with the advantages and disadvantages of each shown.

For high-frequency chopping, fast recovery circulating diodes are essential. Six are required to clamp the windings. These diodes should have a continuous current rating at least equal to the operating motor current, since diode conduction duty-cycle can be high. For low-voltage systems, Schottky diodes are preferred. In higher voltage systems, diodes such as Microsemi UHVP high voltage platinum rectifiers are recommended.

In a pulse-by-pulse current control arrangement, current sensing is done by resistor R_T, through which the transistor's currents are passed (Figures A, B, and C). In these cases, R_D is not needed. The low-side circulating diodes go to ground and the current sense terminals of the UC3625 (I_{SENSE1} and I_{SENSE2}) are connected to R_T through an R_C filter. The input bias current of the current sense amplifier will cause a common mode offset voltage to appear at both inputs, so for best accuracy, keep the filter resistors below 2k and matched.

The current that flows through R_T is discontinuous because of chopping. It flows during the on time of the power stage and is zero during the off time. Consequently, the voltage across R_T consists of a series of pulses, occurring at the PWM frequency, with a peak value indicative of the peak motor current.

To sense average motor current instead of peak current, add another current sense resistor (R_D in Figure D) to measure current in the low-side circulating diodes, and operate in four quadrant mode (pin 22 high). The negative voltage across R_D is corrected by the absolute value current sense amplifier. Within the limitations imposed by Table 1, the circuit of Figure B can also sense average current.

POWER STAGE DESIGN (cont.):

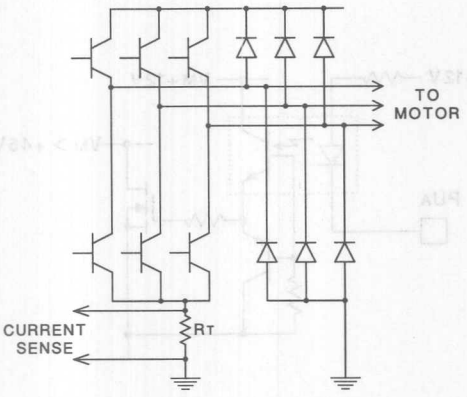


FIGURE A

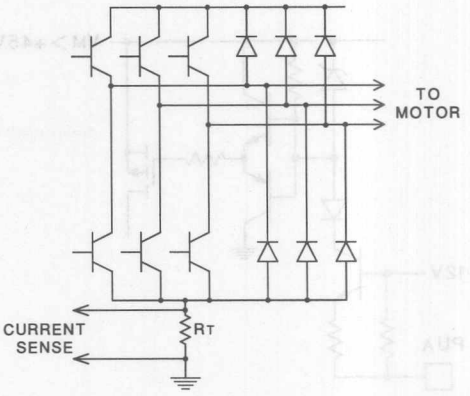


FIGURE B

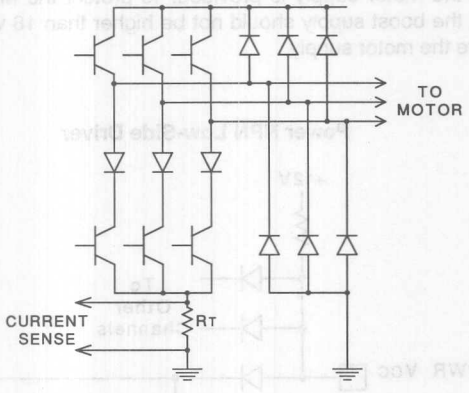


FIGURE C

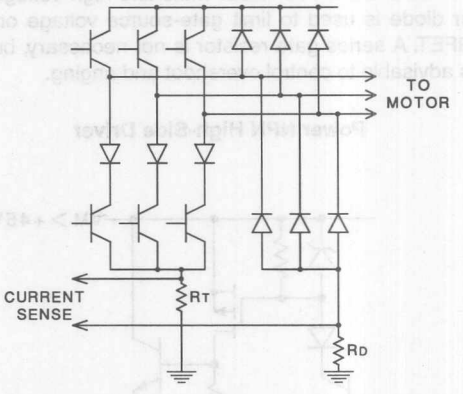
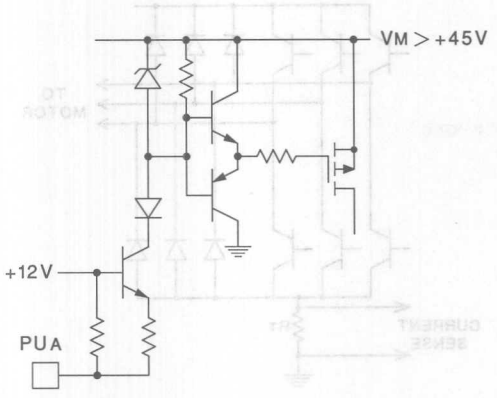


FIGURE D

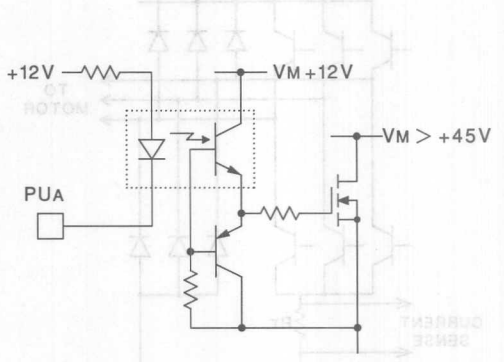
	2 QUADRANT	4 QUADRANT	SAFE BRAKING	POWER REVERSE	CURRENT SENSE	
					PULSE BY PULSE	AVERAGE
FIGURE A	YES	NO	NO	NO	YES	NO
FIGURE B	YES	YES	NO	IN 4QUAD MODE ONLY	YES	YES
FIGURE C	YES	YES	YES	IN 4QUAD MODE ONLY	YES	NO
FIGURE D	YES	YES	YES	IN 4QUAD MODE ONLY	YES	YES

Fast High-Side P-Channel Driver



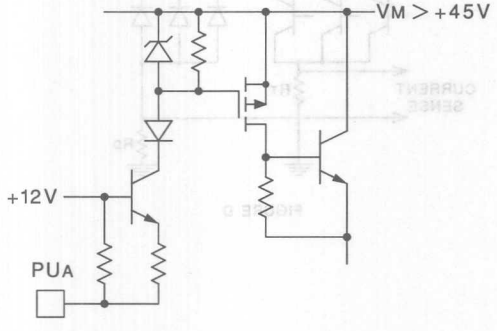
For drives where speed is critical, P-Channel MOSFETs can be driven by emitter followers. Here, both the level shift NPN and the PNP must withstand high voltages. A zener diode is used to limit gate-source voltage on the MOSFET. A series gate resistor is not necessary, but always advisable to control overshoot and ringing.

Optocoupled N-Channel High-Side Driver



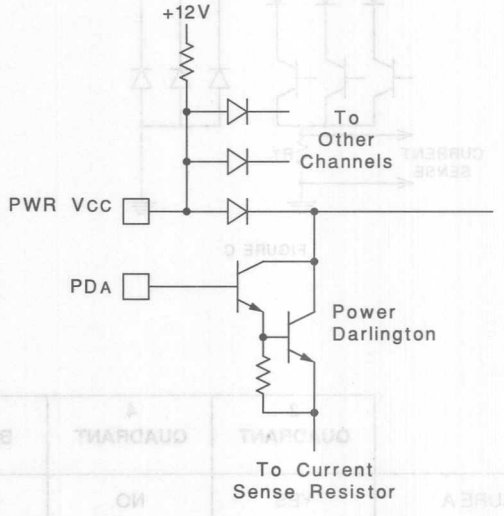
High-voltage optocouplers can quickly drive high-voltage MOSFETs if a boost supply of at least 10 volts greater than the motor supply is provided. To protect the MOSFET, the boost supply should not be higher than 18 volts above the motor supply.

Power NPN High-Side Driver



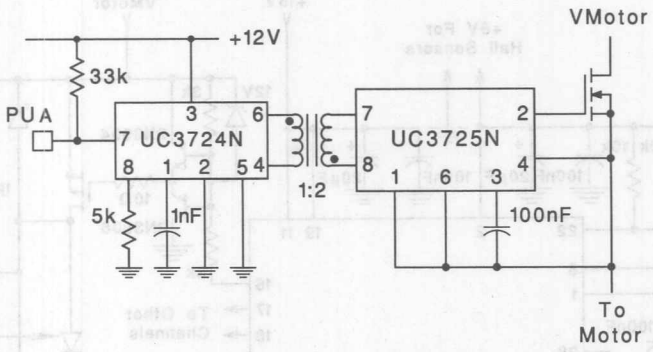
For under 200V 2-quadrent applications, a power NPN driven by a small P-Channel MOSFET will perform well as a high-side driver. A high voltage small-signal NPN is used as a level shift and a high voltage low-current MOSFET provides drive. Although the NPN will not saturate if used within its limitations, the base-emitter resistor on the NPN is still the speed limiting component.

Power NPN Low-Side Driver



This power NPN Darlington drive technique uses a clamp to prevent deep saturation. By limiting saturation of the power device, excessive base drive is minimized and turn-off time is kept fairly short. Lack of base series resistance also adds to the speed of this approach.

Fast High-Side N-Channel Driver with Transformer Isolation



A small pulse transformer can provide excellent isolation between the UC3625 and a high-voltage N-Channel MOSFET while also coupling gate drive power. In this circuit, a UC3724 is used as a transformer driver/encoder that duty-cycle modulates the transformer with a 150kHz pulse train. The UC3725 rectifies this pulse train for gate drive power, demodulates the signal, and drives the gate with over 2 amp peak current.

Both the UC3724 and the UC3725 can operate up to 500kHz if the pulse transformer is selected appropriately. To raise the operating frequency, either lower the timing resistor of the UC3724 (1k minimum), lower the timing capacitor of the UC3724 (500pF minimum) or both.

If there is significant capacitance between transformer primary and secondary, together with very high output slew rate, then it may be necessary to add clamp diodes from the transformer primary to +12V and ground. Signal diodes such as 1N4148 are normally adequate.

The UC3725 also has provisions for MOSFET current limiting. Consult the UC3725 data sheet for more information on implementing this.

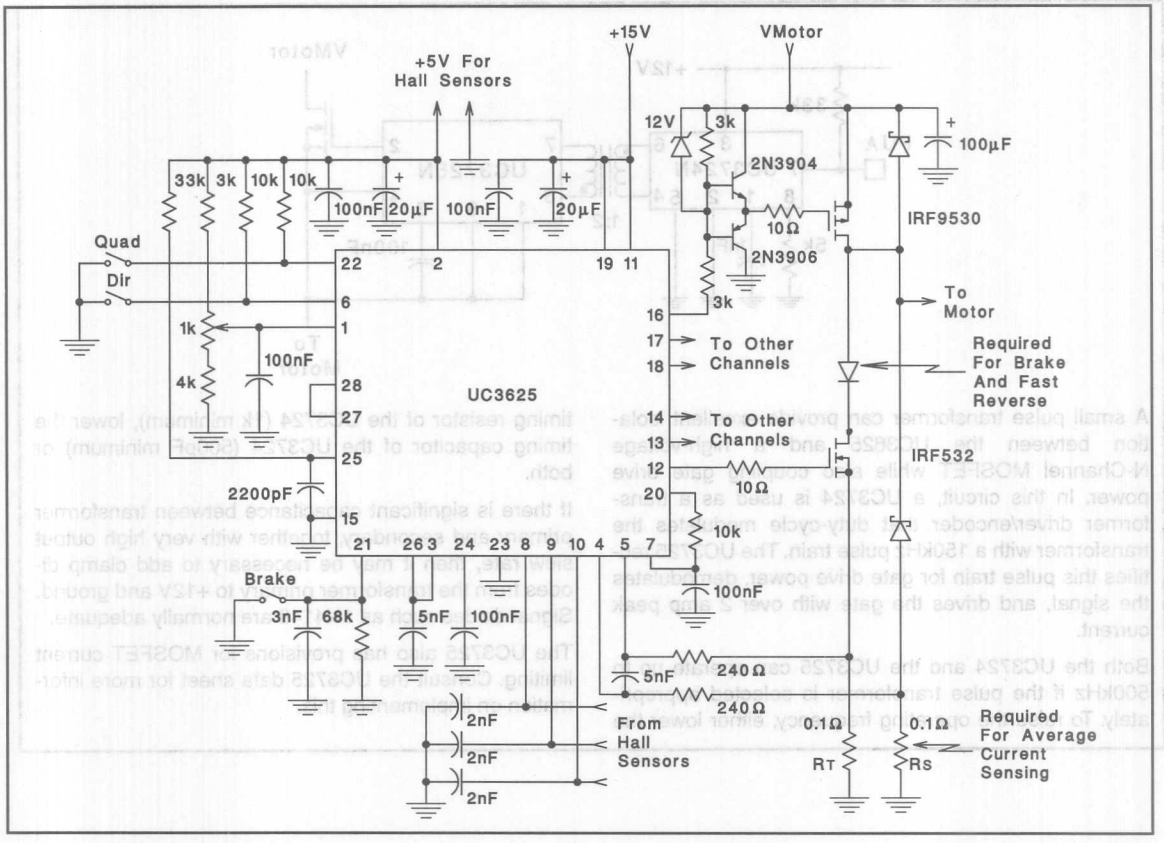
COMMUTATION TRUTH TABLE

This table shows the outputs of the gate drive and open collector outputs for given hall input codes and direction signals. Numbers at the top of the columns are pin numbers.

These ICs operate with position sensor encoding that has either one or two signals high at a time, never all low or all high. This coding is sometimes referred to as "120° Coding" because the coding is the same as coding with position sensors spaced 120 magnetic degrees about the rotor. In response to these position sense signals, only one low-side driver will turn on (go high) and one high-side driver will turn on (pull low) at any time.

INPUTS				OUTPUTS					
DIR	H1	H2	H3	Low-Side			High-Side		
6	8	9	10	12	13	14	16	17	18
1	0	0	1	L	H	L	L	H	H
1	0	1	1	L	L	H	L	H	H
1	0	1	0	L	L	H	H	L	H
1	1	1	0	H	L	L	H	L	H
1	1	0	0	H	L	L	H	H	L
1	1	0	1	L	H	L	H	H	L
0	1	0	1	L	L	H	H	L	H
0	1	0	0	L	L	H	L	H	H
0	1	1	0	L	H	L	L	H	H
0	0	1	0	L	H	L	H	H	L
0	0	1	1	H	L	L	H	H	L
0	0	0	1	H	L	L	H	L	H
X	1	1	1	L	L	L	H	H	H
X	0	0	0	L	L	L	H	H	H

TYPICAL APPLICATION: A 45V/8A Brushless DC Motor Drive Circuit



N–Channel power MOSFETs are used for low–side drivers, while P–Channel power MOSFETs are shown for high–side drivers. Resistors are used to level shift the UC3625 open–collector outputs, driving emitter followers into the MOSFET gate. A 12V zener clamp insures that the MOSFET gate–source voltage will never exceed 12V. Series 10Ω gate resistors tame gate reactance, preventing oscillations and minimizing ringing.

The oscillator timing capacitor should be placed close to pins 15 and 25, to keep ground current out of the capacitor. Ground current in the timing capacitor causes oscillator distortion and slaving to the commutation signal.

The potentiometer connected to pin 1 controls PWM duty cycle directly, implementing a crude form of speed control. This control is often referred to as "voltage mode" because the potentiometer position sets the average motor voltage. This controls speed because steady–state motor speed is closely related to applied voltage.

Pin 20 (Tach-Out) is connected to pin 7 (SPEED IN) through an RC filter, preventing direction reversal while the motor is spinning quickly. In two–quadrant operation, this reversal can cause kinetic energy from the motor to be forced into the power MOSFETs.

A diode in series with the low-side MOSFETs facilitates PWM current control during braking by insuring that braking current will not flow backwards through low–side MOSFETs. Dual current–sense resistors give continuous current sense, whether braking or running in four–quadrant operation, an unnecessary luxury for two–quadrant operation.

The 68k ohm and 3nF tachometer components set maximum commutation time at 140µs. This permits smooth operation up to 35,000 RPM for four–pole motors, yet gives 140µs of noise blanking after commutation.

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

Brushless DC Motor Controller

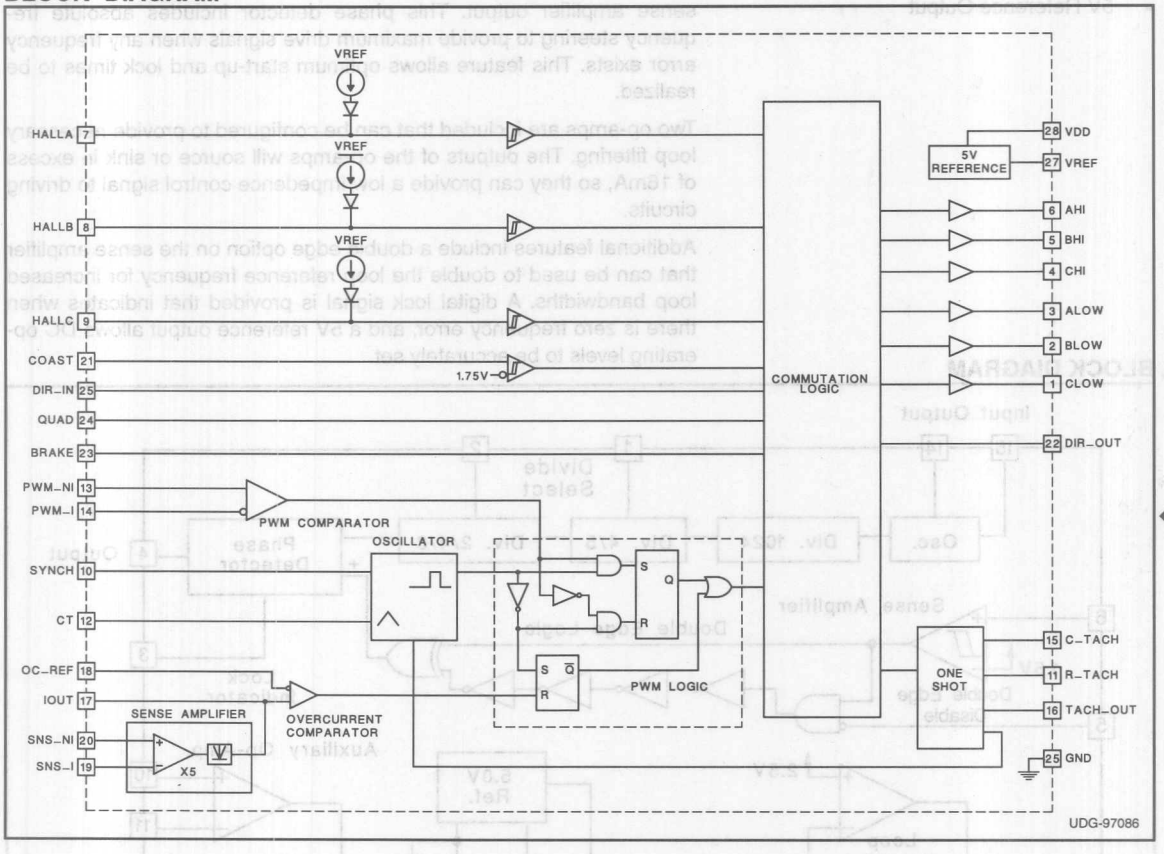
FEATURES

- Two Quadrant and Four Quadrant Operation
- Integrated Absolute Value Current Amplifier
- Pulse-by-Pulse and Average Current Sensing
- Accurate, Variable Duty Cycle Tachometer Output
- Trimmed Precision Reference
- Precision Oscillator
- Direction Output

DESCRIPTION

The UCC3626 motor controller incorporates many of the functions required in designing a high performance, 3-phase brushless DC motor controller. Three rotor position inputs are decoded to provide six digital outputs which can be used to control the switches of an external power stage. In addition commutation logic, direction ,braking and coast functions are also included. A precision oscillator and uncommitted latched comparator can be used to implement a PWM motor control in either voltage or current mode configuration. A precision tachometer, direction output and current sense amplifier are also provided to further integrate the design. Oscillator accuracy is 5% over operating temperature range. Improved noise immunity is obtained by increasing the peak to peak oscillator voltage. The TACH has a tolerance range of 2% over full operating range.

BLOCK DIAGRAM



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Phase Locked Frequency Controller

FEATURES

- Precision Phase Locked Frequency Control System
- Crystal Oscillator
- Programmable Reference Frequency Dividers
- Phase Detector with Absolute Frequency Steering
- Digital Lock Indicator
- Double Edge Option on the Frequency Feedback Sensing Amplifier
- Two High Current Op-Amps
- 5V Reference Output

DESCRIPTION

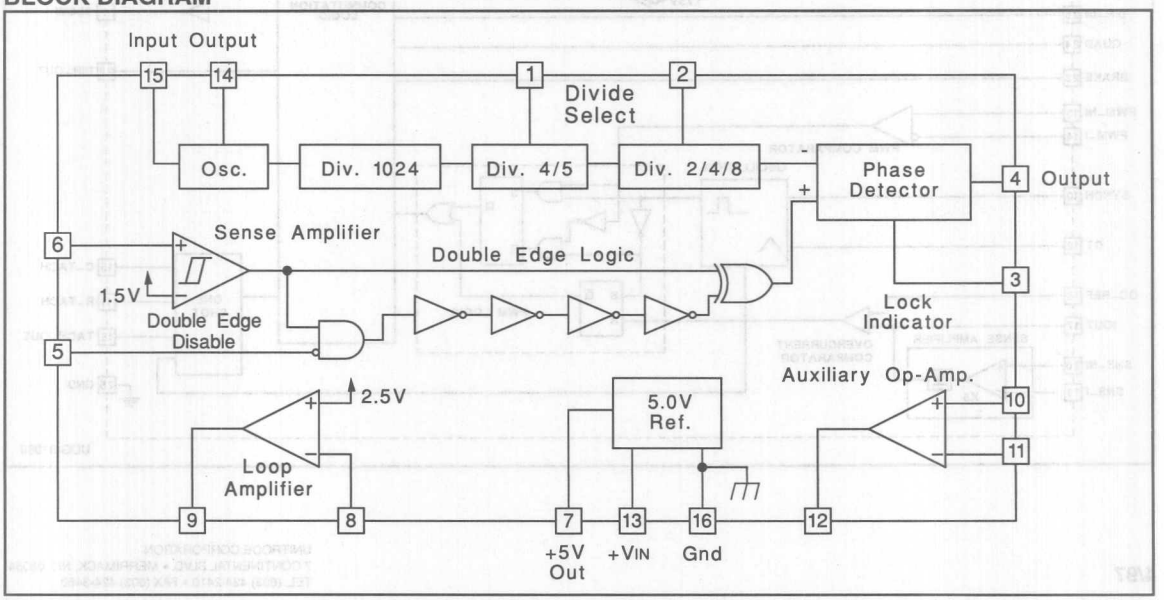
The UC1633 family of integrated circuits was designed for use in phase locked frequency control loops. While optimized for precision speed control of DC motors, these devices are universal enough for most applications that require phase locked control. A precise reference frequency can be generated using the device's high frequency oscillator and programmable frequency dividers. The oscillator operates using a broad range of crystals, or, can function as a buffer stage to an external frequency source.

The phase detector on these integrated circuits compares the reference frequency with a frequency/phase feedback signal. In the case of a motor, feedback is obtained at a hall output of other speed detection device. This signal is buffered by a sense ampilfier that squares up the signal as it goes into the digital phase detector. The phase detector responds proportionally to the phase error between the reference and the sense amplifier output. This phase detector includes absolute frequency steering to provide maximum drive signals when any frequency error exists. This feature allows optimum start-up and lock times to be realized.

Two op-amps are included that can be configured to provide necessary loop filtering. The outputs of the op-amps will source or sink in excess of 16mA, so they can provide a low impedence control signal to driving circuits.

Additional features include a double edge option on the sense amplifier that can be used to double the loop reference frequency for increased loop bandwidths. A digital lock signal is provided that indicates when there is zero frequency error, and a 5V reference output allows DC operating levels to be accurately set.

BLOCK DIAGRAM

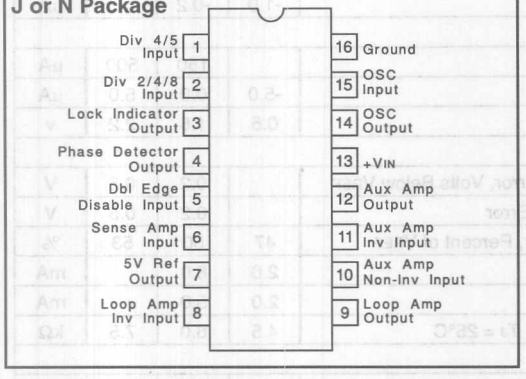


ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage (+VIN) . . . . . +20V
Reference Output Current . . . . . -30mA
Op-Amp Output Currents . . . . . ±30mA
Op-Amp Input Voltages . . . . . -.3V to +20V
Phase Detector Output Current . . . . . ±10mA
Lock Indicator Output Current . . . . . +15mA
Lock Indicator Output Voltage . . . . . +20V
Divide Select Input Voltages . . . . . -.3V to +10V
Double Edge Disable Input Voltage . . . . . -.3V to +10V
Oscillator Input Voltage . . . . . -.3V to +5V
Sense Amplifier Input Voltage . . . . . .3V to +20V
Power Dissipation at TA = 25°C (Note 2 . . . . . 1000mW
Power dissipation at TC = 25°C (Note 2) 2000mW
Operating Junction Temperature . . . . . -55°C to +150°C
Storage Temperature . . . . . -65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) . . . . . 300°C

Note1: Voltages are referenced to ground, (Pin 16). Currents are positive into, negative out of, the specified terminals.
Note 2: Consult Packaging Section of Databook for thermal limitations and considerations of package.

DIL-16 (TOP VIEW)
J or N Package



CONNECTION DIAGRAMS

PLCC-20 (TOP VIEW)
Q Package



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
Div 4/5 Input	2
Div 2/4/8 Input	3
Lock Indicator Output	4
Phase Detector Output	5
N/C	6
Dbl Edge Disable Input	7
Sense Amp Input	8
5V Ref Output	9
Loop Amp Inv Input	10
N/C	11
Loop Amp Output	12
Aux Amp Non-Inv Input	13
Aux Amp Inv Input	14
Aux Amp Output	15
N/C	16
+VIN	17
OSC Output	18
OSC Input	19
Ground	20

ELECTRICAL CHARACTERISTICS:

(Unless otherwise stated, these specifications apply for TA = 0°C to +70°C for the UC3633, -25°C to +85°C for the UC2633, -55°C to +125°C for the UC1633, +VIN = 12V; TA=TJ.)

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current	+VIN = 15V		20	28	mA
Reference					
Output Voltage (VREF)		4.75	5.0	5.25	V
Load Regulation	IOUT = 0V to 7mA		5.0	20	mV
Line Regulation	+VIN = 8V to 15V		2.0	20	mV
Short Circuit Current	VOUT = 0V	12	30		mA
Oscillator					
DC Voltage Gain	Oscillator Input to Oscillator Output	12	16	20	dB
Input DC Level (VIB)	Oscillator Input Pin Open, TJ = 25°C	1.15	1.3	1.45	V
Input Impedance (Note 3)	VIN = VIB ±0.5V, TJ = 25°C	1.3	1.6	1.9	kΩ
Output DC Level	Oscillator Input Pin Open, TJ = 25°C	1.2	1.4	1.6	V
Maximum Operating Frequency		10			MHz
Dividers					
Maximum Input Frequency	Input = 1VPP at Oscillator Input	10			MHz
Div. 4/5 Input Current	Input = 5V (Div. by 4)		150	500	µA
	Input = 0V (Div. by 5)	-5.0	0.0	5.0	µA
Div. 4/5 Threshold		0.5	1.6	2.2	V

Note 3: These impedence levels will vary with TJ at about 1700ppm/°C

ELECTRICAL CHARACTERISTICS (cont.): (Unless otherwise stated, these specifications apply for T_A = 0°C to +70°C for the UC3633, -25°C to +85°C for the UC2633, -55°C to +125°C for the UC1633, $+V_{IN}$ = 12V; T_A=T_J.)

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Dividers (cont.)					
Div. 2/4/8 Input Current	Input = 5V (Div. by 8)		150	500	µA
	Input = 0V (Div. by 2)	-500	-150		µA
Div. 2/4/8 Open Circuit Voltage	Input Current = 0µA (Div. by 4)	1.5	2.5	3.5	V
Div. by 2 Threshold		0.20	0.8		V
Div. by 4 Threshold		1.5		3.5	V
Div. by 8 Threshold	Volts Below V_{REF}	0.20	0.8		V
Sense Amplifier					
Threshold Voltage	Percent of V_{REF}	27	30	33	%
Threshold Hysteresis			10		mV
Input Bias Current	Input = 1.5V	-1.0	-0.2		µA
Double Edge Disable Input					
Input Current	Input = 5V (Disabled)		150	500	µA
	Input = 0V (Enabled)	-5.0	0.0	5.0	µA
Threshold Voltage		0.5	1.6	2.2	v
Phase Detector					
High Output Level	Positive Phase/Freq. Error, Volts Below V_{REF}		0.2	0.5	V
Low Output Level	Negative Phase/Freq. Error		0.2	0.5	V
Mid Output Level	Zero Phase/Freq. Error, Percent of V_{REF}	47	50	53	%
High Level Maximum Source Current	V_{OUT} = 4.3V	2.0	8.0		mA
Low Level Maximum Sink Current	V_{OUT} = 0.7V	2.0	5.0		mA
Mid Level Output Impedance (Note 3)	I_{OUT} = -200 to +200µA, T_J = 25°C	4.5	6.0	7.5	kΩ
Lock Indicator Output					
Saturation Voltage	Freq. Error, I_{OUT} = 5mA		0.3	0.45	V
Leakage Current	Zero Freq. Error, V_{OUT} = 15V		0.1	1.0	µA
Loop Amplifier					
NON INV. Reference Voltage	Percent of V_{REF}	47	50	53	%
Input Bias Current	Input = 2.5V	-0.8	-0.2		µA
AVOL		60	75		dB
PSRR	$+V_{IN}$ = 8V to 15V	70	100		dB
Short Circuit Current	Source, V_{OUT} = 0V	16	35		mA
	Sink, V_{OUT} = 5V	16	30		mA
Auxiliary Op-Amp					
Input Offset Voltage	V_{CM} = 2.5V			8	mV
Input Bias Current	V_{CM} = 2.5V	-0.8	-0.2		µA
Input Offset Current	V_{CM} = 2.5V		.01	0.1	µA
AVOL		70	120		dB
PSRR	$+V_{IN}$ = 8V to 15V	70	100		dB
CMRR	V_{CM} = 0V to 10V	70	100		dB
Short Circuit Current	Source, V_{OUT} = 0V	16	35		mA
	Sink, V_{OUT} = 5V	16	30		mA

Note 3: These impedence levels will vary with T_J at about 1700ppm/°C

APPLICATION AND OPERATING INFORMATION

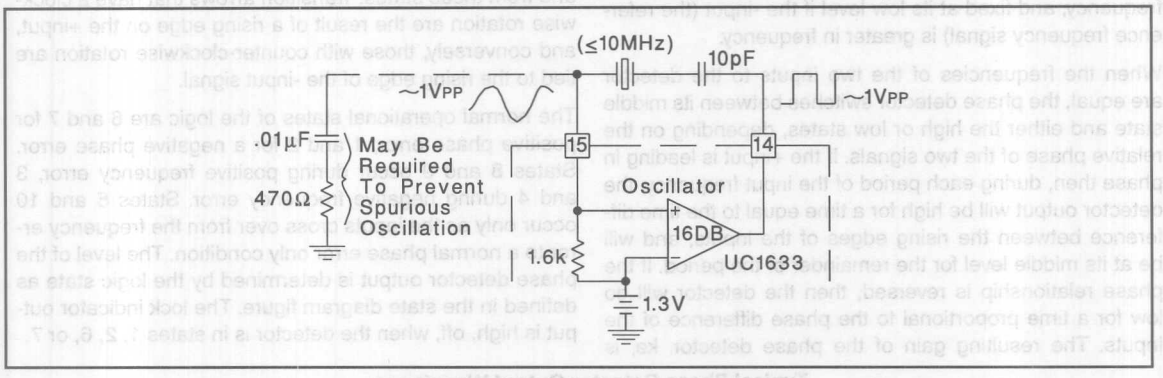
Determining the Oscillator Frequency

The frequency at the oscillator is determined by the desired RPM of the motor, the divide ratio selected, the number of poles in the motor, and the state of the double edge select pin.

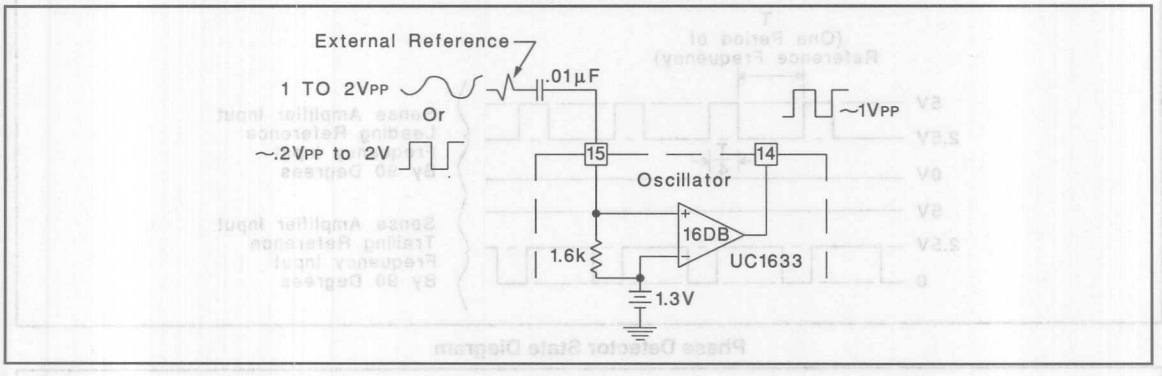
fosc(Hz) = (Divide Ratio) • (Motor RPM) • (1/60 SEC/MIN) • (No. of Rotor Poles/2) • (x 2 if Pin 5 Low)

The resulting reference frequency appearing at the phase detector inputs is equal to the oscillator frequency divided by the selected divide ratio. If the double edge option is used, (Pin 5 low), the frequency of the sense amplifier input signal is doubled by responding to both the rising and falling edges of the input signal. Using this option, the loop reference frequency can be doubled for a given motor RPM.

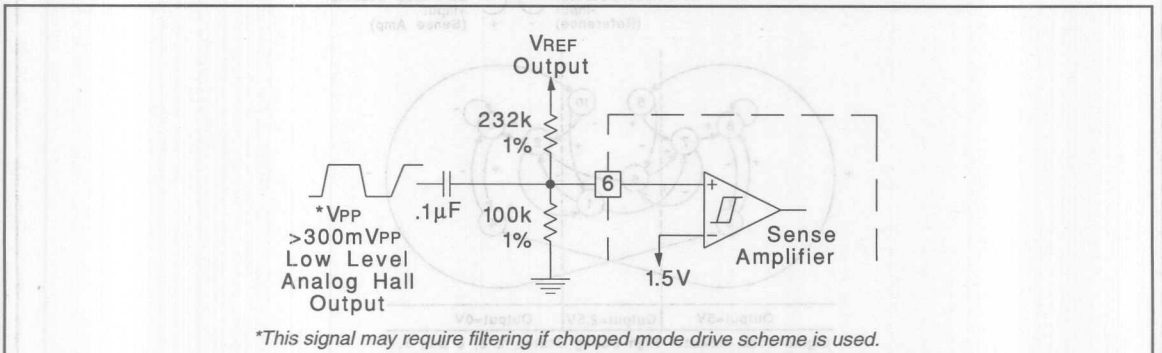
Recommended Oscillator Configuration Using AT Cut Quartz Crystal



External Reference Frequency Input



Method for Deriving Rotation Feedback Signal from Analog Hall Effect Device



**This signal may require filtering if chopped mode drive scheme is used.*

APPLICATION AND OPERATION INFORMATION

Phase Detector Operation

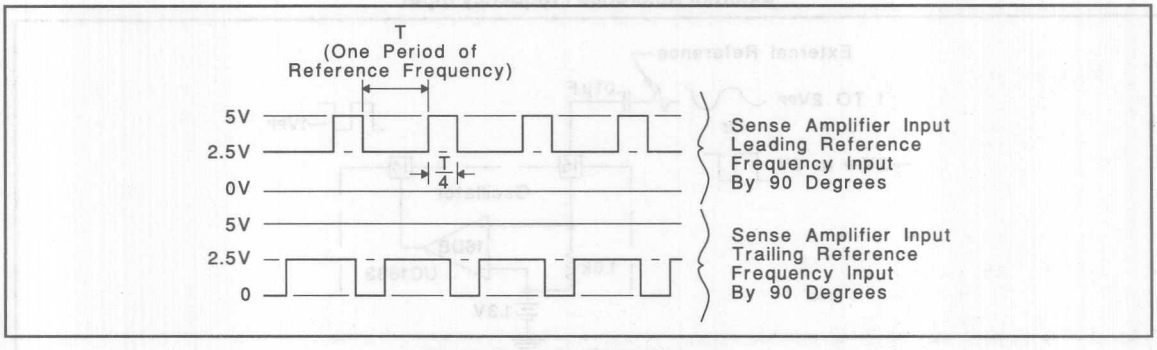
The phase detector on these devices is a digital circuit that responds to the rising edges of the detector's two inputs. The phase detector output has three states: a high, 5V state, a low, 0V state, and a middle, 2.5V state. In the high and low states the output impedance of the detector is low and the middle state output impedence is high, typically 6.0kΩ. When there is any static frequency difference between the inputs, the detector output is fixed at its high level if the +input (the sense amplifier signal) is greater in frequency, and fixed at its low level if the -input (the reference frequency signal) is greater in frequency.

When the frequencies of the two inputs to the detector are equal, the phase detector switches between its middle state and either the high or low states, depending on the relative phase of the two signals. If the +input is leading in phase then, during each period of the input frequency, the detector output will be high for a time equal to the time difference between the rising edges of the inputs, and will be at its middle level for the remainder of the period. If the phase relationship is reversed, then the detector will go low for a time proportional to the phase difference of the inputs. The resulting gain of the phase detector. kø, is 5V/4π radians or about 0.4V/radian. The dynamic range of the detector is ±2π radians.

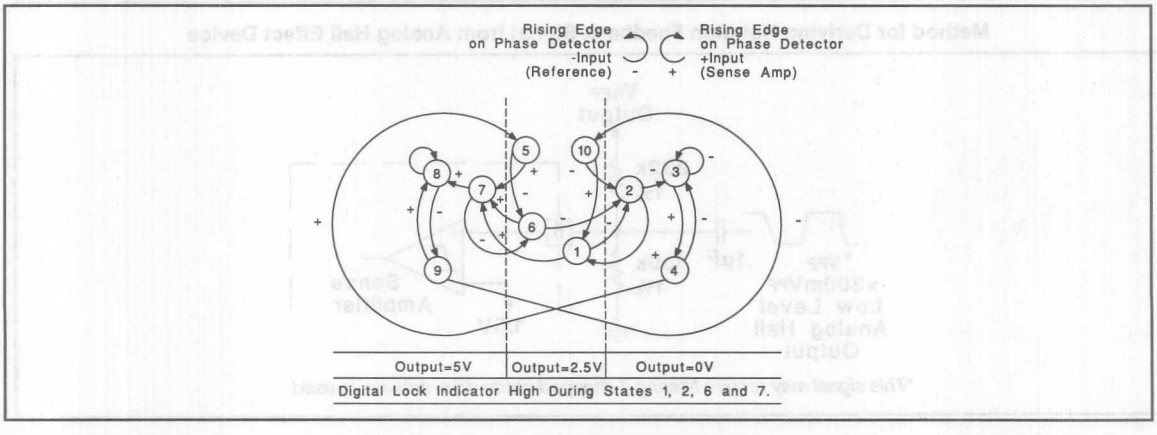
The operation of the phase detector is illustrated in the figures below. The upper figure shows typical voltage waveforms seen at the detector output for leading and lagging phase conditions. The lower figure is a state diagram of the phase detector logic. In this figure, the circles represent the 10 possible states of the logic, and the connecting arrows represent the transition events/paths to and from these states. Transition arrows that have a clockwise rotation are the result of a rising edge on the +input, and conversely, those with counter-clockwise rotation are tied to the rising edge of the -input signal.

The normal operational states of the logic are 6 and 7 for positive phase error, 1 and 2 for a negative phase error. States 8 and 9 occur during positive frequency error, 3 and 4 during negative frequency error. States 5 and 10 occur only as the inputs cross over from the frequency error to a normal phase error only condition. The level of the phase detector output is determined by the logic state as defined in the state diagram figure. The lock indicator output is high, off, when the detector is in states 1, 2, 6, or 7.

Typical Phase Detector Output Waveforms

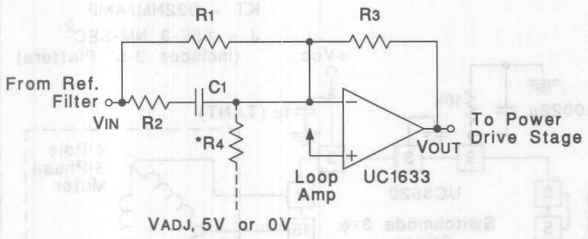


Phase Detector State Diagram



APPLICATION AND OPERATION INFORMATION

Suggested Loop Filter Configuration



$$\frac{V_{OUT}}{V_{IN}}(s) = \frac{R_3}{R_1} \bullet \frac{1 + s/\omega_z}{1 + s/\omega_p}$$

$$\omega_p = \frac{1}{R_2 C_1}$$

$$\omega_z = \frac{1}{(R_1 + R_2)\, C_1}$$

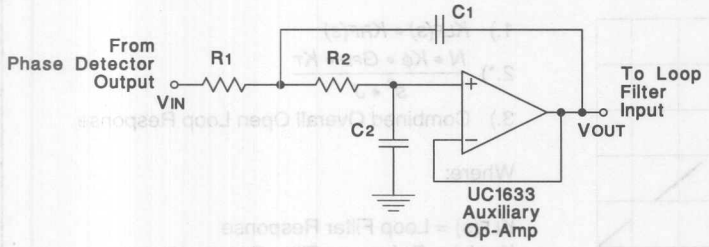
* The static phase error of the loop is easily adjusted by adding resistor, R4, as shown. To lock at zero phase error R4 is determined by:

$$R_4 = \frac{2.5V \bullet R_3}{|\Delta V_{OUT}|}$$

Where: $|\Delta V_{OUT}| = |V_{OUT} - 2.5V|$
and V_{OUT} = DC Operating Voltage At Loop Amplifier Output During Phase Lock

If: $(V_{OUT} - 2.5) > 0$, R4 Goes to 0V
$(V_{OUT} - 2.5) < 0$, R4 Goes to 5.0V

Reference Filter Configuration



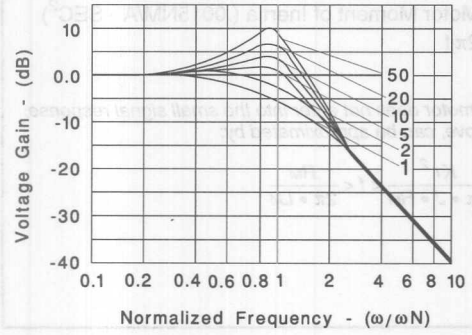
$$\frac{V_{OUT}}{V_{IN}}(s) = \frac{1}{1 + \frac{s\,2\zeta}{\omega_N} + \frac{s^2}{\omega_N^2}}$$

$$\omega_N = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}}$$

$$\zeta = \frac{1}{2Q} = \frac{1}{2}\sqrt{\frac{C_2}{C_1}}\ \frac{R_1 + R_2}{\sqrt{R_1 R_2}}$$

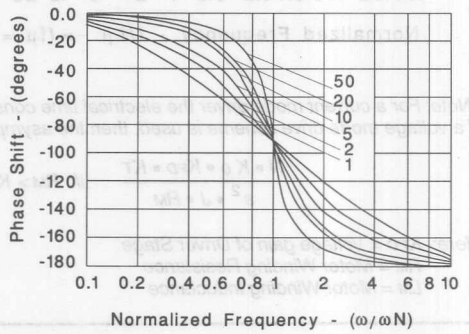
Note: with $R_1 = R_2$, $\zeta = \sqrt{\frac{C_2}{C_1}}$

Reference Filter Design Aid - Gain Response



Variable is $1/\zeta^2$
(For R1=R2, $1/\zeta^2$=C1/C2)

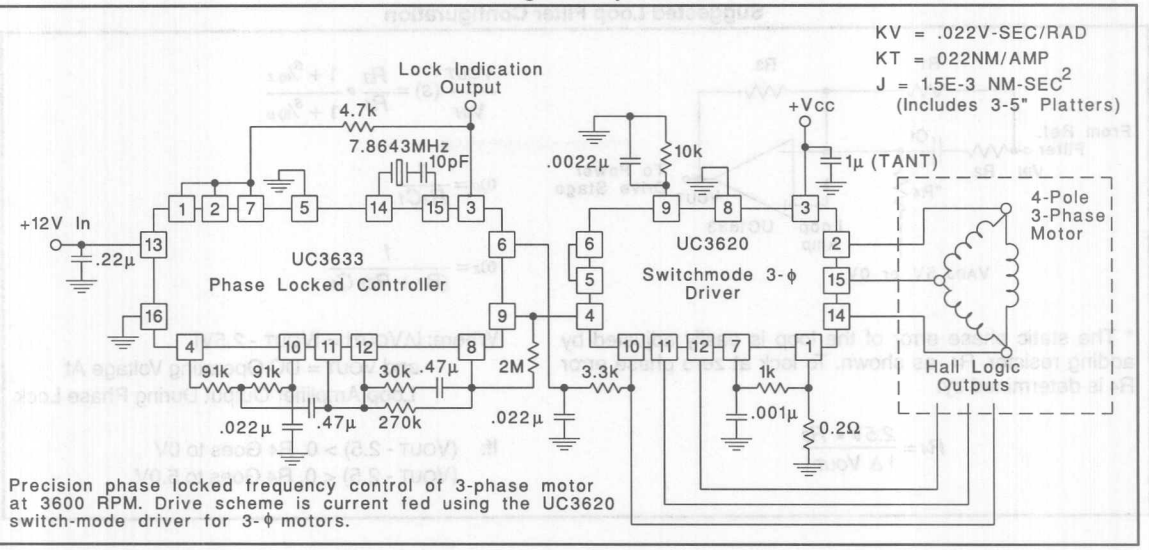
Reference Filter Design Aid - Phase Response



Variable is $1/\zeta^2$
(For R1=R2, $1/\zeta^2$=C1/C2)

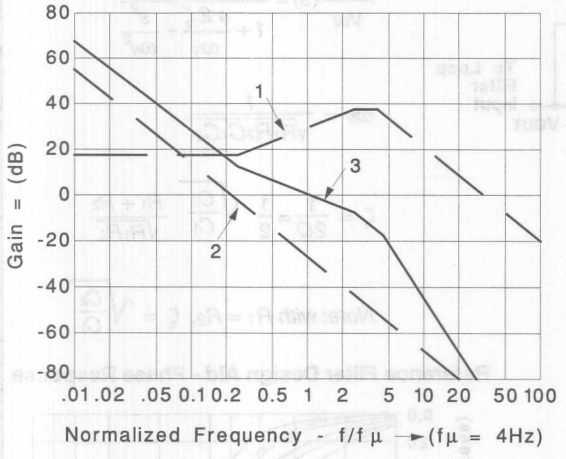
APPLICATION AND OPERATION INFORMATION

Design Example



Precision phase locked frequency control of 3-phase motor at 3600 RPM. Drive scheme is current fed using the UC3620 switch-mode driver for 3-ϕ motors.

Bode Plots - Design Example Open Loop Response



1.) $K_{LF}(s) \bullet K_{RF}(s)$

2.*) $\dfrac{N \bullet K\phi \bullet G_{PD} \bullet K_T}{s^2 \bullet J}$

3.) Combined Overall Open Loop Response

Where:

$K_{LF}(s)$ = Loop Filter Response
$K_{RF}(s)$ = Reference Filter Response
N = 4 (Using Double Edge Sensing With 4 Pole Motor)
$K\phi$ = Phase Detector Gain (.4V/RAD)
G_{PD} = Power Stage Transductance (1A/V)
K_T = Motor Torque Constant (.022NM/A)
J = Motor Moment of Inertia (.0015NM/A - SEC²)
s = 2πjf

Note: For a current mode driver the electrical time constant, L_M / R_M, of the motor does not enter into the small signal response. If a voltage mode drive scheme is used, then the asymptote, plotted as **2 above, can be approximated by:*

$$\frac{N \bullet K\phi \bullet K_{PD} \bullet K_T}{s^2 \bullet J \bullet R_M} \quad \text{if: } R_M > K_T \sqrt{\frac{L_M}{J}} \quad \text{and,} \quad \frac{K_T{}^2}{2\pi \bullet J \bullet R_M} < f < \frac{R_M}{2\pi \bullet L_M}$$

Here: K_{PD} = Voltage gain of Driver Stage
R_M = Motor Winding Resistance
L_M = Motor Winding Inductance

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UNITRODE

UC1634
UC2634
UC3634

Phase Locked Frequency Controller

FEATURES

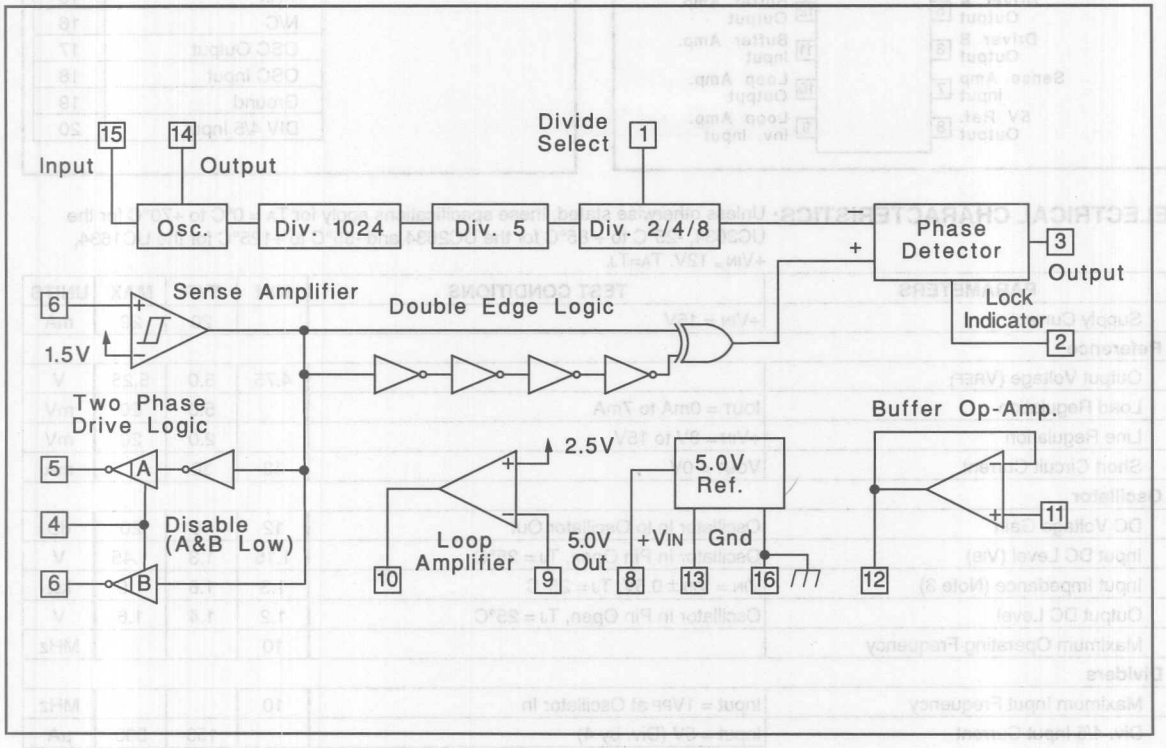
- Precision Phase Locked Frequency Control System
- Communication Logic for 2-Phase Motors
- Disable Input for Motor Inhibit
- Crystal Oscillator
- Programmable Reference Frequency Dividers
- Phase Detector with Absolute Frequency Steering
- Digital Lock Indicator
- Two High Current Op-Amps
- 5V Reference Output

DESCRIPTION

The UC1634 series of devices is optimized to provide precision phase locked frequency control for two phase DC brushless motors. These devices include most of the features of the general purpose UC1633 Phase Locked Control family and also provide the out-of-phase commutation signals required for driving two phase brushless motors. Only an external power booster stage is required for a complete drive and control system.

The two commutation outputs are open collector devices that can sink in excess of 16mA. A disable input allows the user to simultaneously force both of these outputs to an active low state. Double edge logic, following the sense amplifier, doubles the reference frequency at the phase detector by responding to both edges of the input signal at Pin 7.

BLOCK DIAGRAM



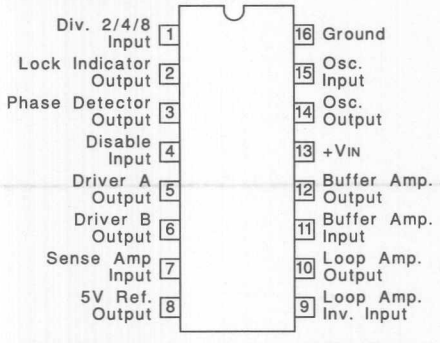
6/93

ABSOLUTE MAXIMUM RATINGS (Note 1, 2)

Input Supply Voltage (+VIN) . . . . . +20V
Reference Output Current . . . . . -30mA
Op-Amp Output Currents . . . . . ±30mA
Op-Amp Input Voltages . . . . . -.3V to +20V
Phase Detector Output Current . . . . . ±10mA
Lock Indicator Output Current . . . . . +15mA
Lock Indicator Output Voltage . . . . . +20V
Divide Select Input Voltage . . . . . -.3V to +10V
Disable Input Voltage . . . . . -.3V to +10V
Oscillator Input Voltage . . . . . -.3V to +5V
Sense Amplifier Input Voltage . . . . . -.3V to +20V
Driver Output Currents . . . . . +30mA
Driver Output Voltages . . . . . +20V
Power Dissipation at T_A = 25°C(Note 2) 1000mW
Power Dissipation at T_C = 25°C (Note 2) 2000mW
Operating Junction Temperature . . . . . -55°C to +150°C
Storage Temperature . . . . . -65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) . . . . . 300°C

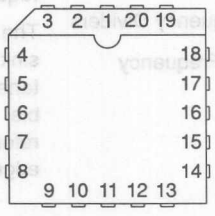
Note 1: Voltages are referenced to ground, (Pin 16, DIL Package). Currents are positive into, negative out of, the specified terminals.
Note 2: Consult Packaging Section of Databook for thermal limitations and considerations of package.

DIL-16, SOIC-16 (TOP VIEW)
J or N Package, DW Package



CONNECTION DIAGRAMS

PLCC-20 (TOP VIEW)
Q Package



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
DIV 2/4/8	2
Lock Indicator Output	3
Phase Detector Output	4
Disable Input	5
N/C	6
Driver A Output	7
Driver B Output	8
Sense Amp Output	9
5V Ref Output	10
Loop Amp Inv Input	11
Loop Amp Output	12
Buffer Amp Input	13
Buffer Amp Output	14
+VIN	15
N/C	16
OSC Output	17
OSC Input	18
Ground	19
DIV 4/5 Input	20

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, these specifications apply for T_A = 0°C to +70°C for the UC3634, -25°C to + 85°C for the UC2634 and -55°C to +125°C for the UC1634, +VIN = 12V. TA=TJ.

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	+VIN = 15V		20	29	mA
Reference					
Output Voltage (V_{REF})		4.75	5.0	5.25	V
Load Regulation	I_{OUT} = 0mA to 7mA		5.0	20	mV
Line Regulation	+VIN = 8V to 15V		2.0	20	mV
Short Circuit Current	VOUT = 0V	12	30		mA
Oscillator					
DC Voltage Gain	Oscillator In to Oscillator Out	12	16	20	dB
Input DC Level (V_{IB})	Oscillator In Pin Open, T_J = 25°C	1.15	1.3	1.45	V
Input Impedance (Note 3)	V_{IN} = V_{IB} ± 0.5V, T_J = 25°C	1.3	1.6	1.9	kΩ
Output DC Level	Oscillator In Pin Open, T_J = 25°C	1.2	1.4	1.6	V
Maximum Operating Frequency		10			MHz
Dividers					
Maximum Input Frequency	Input = 1V_{PP} at Oscillator In	10			MHz
Div. 4/5 Input Current	Input = 5V (Div. by 4)		150	500	µA
(Q Package Only, Note 4)	Input = 0V (Div. by 5)	-5.0	0.0	5.0	µA

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = 0°C to +70°C for the UC3634, -25°C to + 85°C for the UC2634 and -55°C to +125°C for the UC1634, $+V_{IN}$ = 12V. T_A=T_J

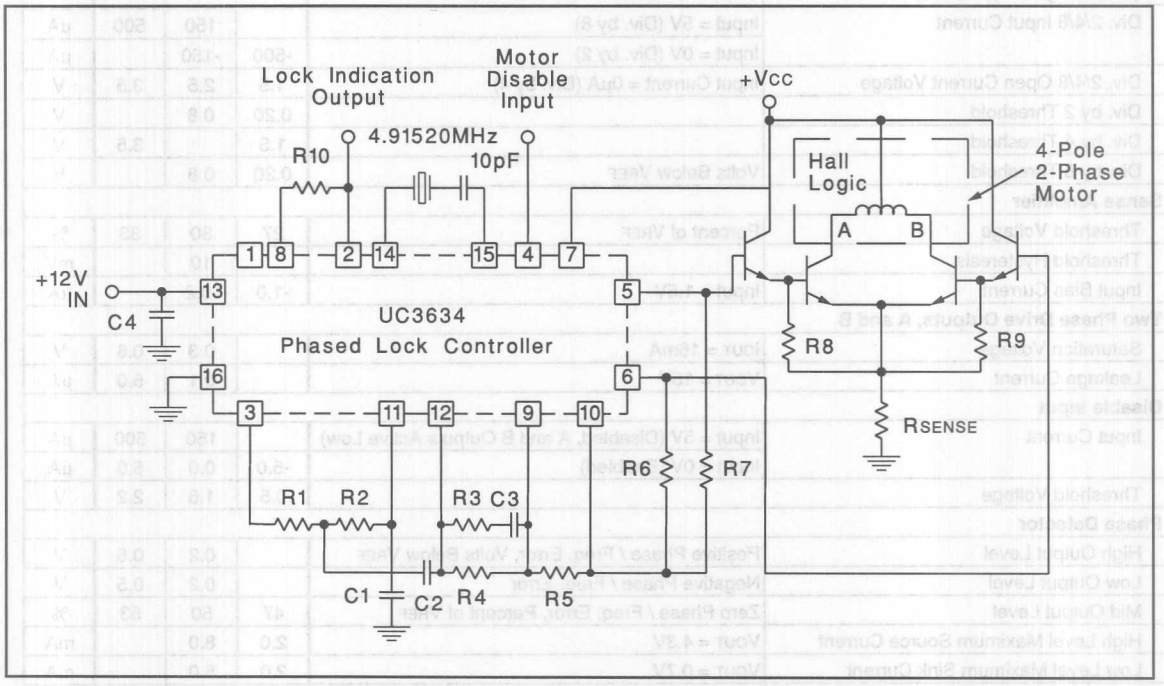
PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Dividers (cont.)					
Div. 4/5 Input Threshold (Q Package Only, Note 4)		0.5	1.6	2.2	V
Div. 2/4/8 Input Current	Input = 5V (Div. by 8)		150	500	µA
	Input = 0V (Div. by 2)	-500	-150		µA
Div. 2/4/8 Open Current Voltage	Input Current = 0µA (Div. by 4)	1.5	2.5	3.5	V
Div. by 2 Threshold		0.20	0.8		V
Div. by 4 Threshold		1.5		3.5	V
Div. by 8 Threshold	Volts Below V_{REF}	0.20	0.8		V
Sense Amplifier					
Threshold Voltage	Percent of V_{REF}	27	30	33	%
Threshold Hysteresis			10		mV
Input Bias Current	Input = 1.5V	-1.0	-0.2		µA
Two Phase Drive Outputs, A and B					
Saturation Voltage	I_{OUT} = 16mA		0.3	0.6	V
Leakage Current	V_{OUT} = 15V		0.1	5.0	µA
Disable Input					
Input Current	Input = 5V (Disabled, A and B Outputs Active Low)		150	500	µA
	Input = 0V (Enabled)	-5.0	0.0	5.0	µA
Threshold Voltage		0.5	1.6	2.2	V
Phase Detector					
High Output Level	Positive Phase / Freq. Error, Volts Below V_{REF}		0.2	0.5	V
Low Output Level	Negative Phase / Freq. Error		0.2	0.5	V
Mid Output Level	Zero Phase / Freq. Error, Percent of V_{REF}	47	50	53	%
High Level Maximum Source Current	V_{OUT} = 4.3V	2.0	8.0		mA
Low Level Maximum Sink Current	V_{OUT} = 0.7V	2.0	5.0		mA
Mid Level Output Impedance (Note 3)	I_{OUT} = -200 to +200µA, T_J = 25°C	4.5	6.0	7.5	kΩ
Lock Indicator Output					
Saturation Voltage	Freq. Error, I_{OUT} = 5mA		0.3	0.45	V
Leakage Current	Zero Freq. Error, V_{OUT} = 15V		0.1	1.0	µA
Loop Amplifier					
N INV. Reference Voltage	Percent of V_{REF}	47	50	53	%
Input Bias Current	Input = 2.5V	-0.8	-0.2		µA
AVOL		60	75		dB
PSRR	$+V_{IN}$ = 8V to 15V	70	100		dB
Short Circuit Current	Source, V_{OUT} = 0V	16	35		mA
	Sink, V_{OUT} = 5V	16	30		mA
Buffer Op-Amp					
Input Offset Voltage	V_{CM} = 2.5V			8	mV
Input Bias Current	V_{CM} = 2.5V	-0.8	-0.2		µA
PSRR	$+V_{IN}$ = 8 to 15V	70	100		dB
CMRR	V_{CM} = 0 to 10V	70	100		dB
Short Circuit Current	Source, V_{OUT} = 0V	16	35		mA
	Sink, V_{OUT} = 5V	16	30		mA

Note 3: These impedance levels will vary with T_J at about 1700ppm/°C.
Note 4: This part is also available in a 20 pin plastic leadless chip carrier, Q designator, where a divide by 4/5 select pin is available. Consult factory for details.

APPLICATION AND OPERATION INFORMATION (For additional information see UC1633 data sheet)

Design Example:

Precision phased locked frequency control of a 2-phase motor at 3600 RPM. Using the commutation logic on the UC3634, a simple discrete drive scheme is possible.



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Phase Locked Frequency Controller

FEATURES

- Precision Phase Locked Frequency Control System
- Crystal Oscillator
- Programmable Reference Frequency Dividers
- Phase Detector with Absolute Frequency Steering
- Separate Divider Outputs and Phase Detector Input Pins
- Double Edge Option on the Frequency Feedback Sensing Amplifier
- Two High Current Op Amps
- 5V Reference Output

DESCRIPTION

The UC1635 family of integrated circuits was designed for use in precision speed control of DC motors. An extension to the UC1633 line of phase locked controllers, these devices provide access to both of the digital phase detector's inputs, and include a reference frequency divider output pin. With this added flexibility, this family of controllers can be used to obtain phase synchronization of multiple motors.

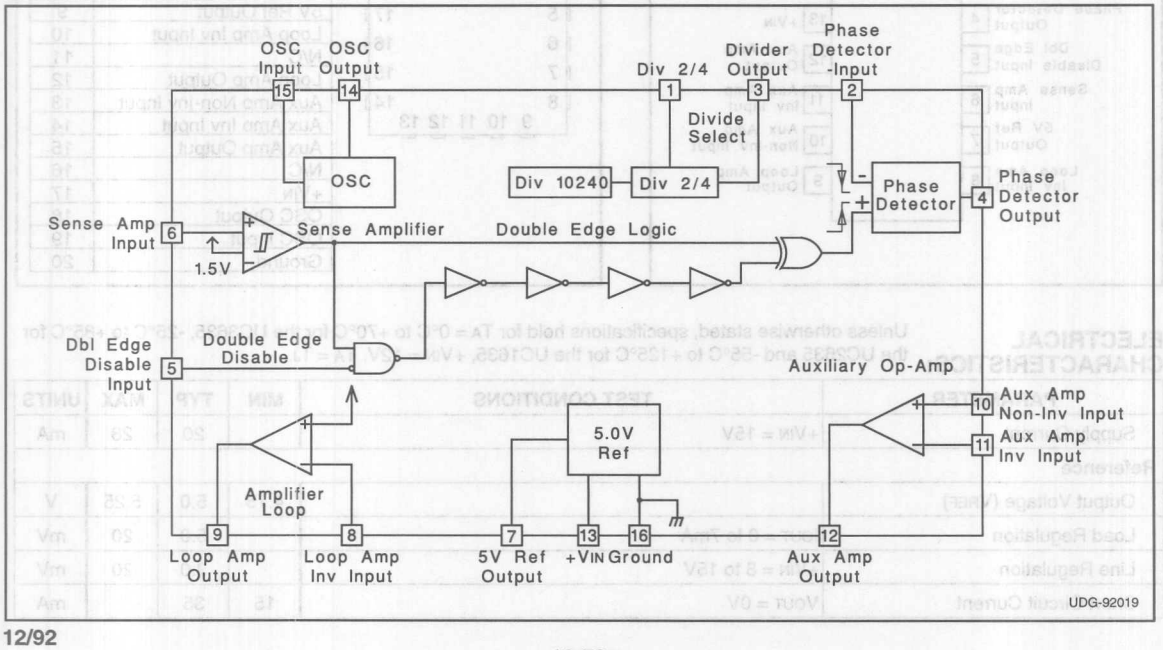
A reference frequency can be generated using the device's crystal oscillator and programmable dividers. The oscillator operates using a broad range of crystals, or, can function as a buffer stage to an external frequency source.

The phase detector responds proportionally to the phase error between the detector's minus input pin and the sense amplifier output. This phase detector includes absolute frequency steering to provide maximum drive signals when any frequency error exists. This feature allows optimum start-up and lock times to be realized.

Two op-amps are included that can be configured to provide necessary loop filtering. The outputs of these op-amps will source or sink in excess of 16mA, so they can provide a low impedance control signal to driving circuits.

Additional features include a double edge option on the sense amplifier that can be used to double the loop reference frequency for increased loop bandwidths. A 5V reference output can be used to accurately set DC operating levels.

BLOCK DIAGRAM



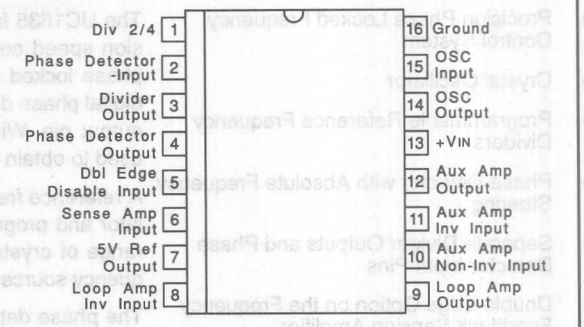
ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage (+VIN) ..... +20V
Reference Output Current ..... -30mA
Op-Amp Output Currents ..... ±30mA
Op-Amp Input Voltages ..... -0.3 to +20V
Phase Detector Input Voltage ..... -0.3V to +5V
Phase Detector Output Current ..... ±10mA
Lock Indicator Output Current ..... +15mA
Lock Indicator Output Voltage ..... +20V
Divide Select Input Voltages ..... -0.3V to +10V
Double Edge Disable Input Voltage ..... -0.3V to +10V
Oscillator Input Voltage ..... -0.3V to +5V
Sense Amplifier Input Voltage ..... -0.3V to +20V
Power Dissipation at TA = 25°C, (Note 2) 1000mW
Power Dissipation at TC = 25°C, (Note 2) 2000mW
Operating Junction Temperature ..... -55° to 150°C
Storage Temperature ..... -65° to +150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

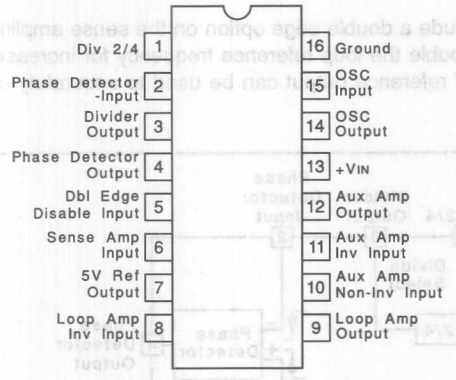
Note 1: Voltages are referenced to ground, (Pin 16). Currents are positive into, negative out of, the specified terminals.
Note 2: Consult Unitrode Integrated Circuits databook for information regarding thermal specifications and limitations of packages.

CONNECTION DIAGRAMS

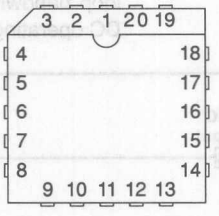
SOIC–16 (Top View)
DW Package



DIL–16 (Top View)
J & N Packages



PLCC-20 & LCC-20
(Top View)
Q & L Packages



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
Div 2/4	2
Phase Detector Input	3
Divider Output	4
Phase Detector Output	5
N/C	6
Dbl Edge Disable Input	7
Sense Amp Input	8
5V Ref Output	9
Loop Amp Inv Input	10
N/C	11
Loop Amp Output	12
Aux Amp Non-Inv Input	13
Aux Amp Inv Input	14
Aux Amp Output	15
N/C	16
+VIN	17
OSC Output	18
OSC Input	19
Ground	20

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, specifications hold for TA = 0°C to +70°C for the UC3635, -25°C to +85°C for the UC2635 and -55°C to +125°C for the UC1635, +VIN = 12V. TA = TJ.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	+VIN = 15V		20	28	mA
Reference					
Output Voltage (VREF)		4.75	5.0	5.25	V
Load Regulation	IOUT = 0 to 7mA		5.0	20	mV
Line Regulation	+VIN = 8 to 15V		2.0	20	mV
Short Circuit Current	VOUT = 0V	15	35		mA

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, specifications hold for T_A = 0°C to +70°C for the UC3635, -25°C to +85°C for the UC2635 and -55°C to +125°C for the UC1635, +Vin = 12V. $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator					
DC Voltage Gain	Oscillator Input to Oscillator Output	12	16	20	dB
Input DC Level (V_{IB})	Oscillator Input Pin Open, T_J = 25°C	1.15	1.3	1.45	V
Input Impedance (Note 2)	$V_{IN} = V_{IB} \pm 0.5V$, T_J = 25°C	1.3	1.6	1.9	kΩ
Output DC Level	Oscillator Input Pin Open, T_J = 25°C	1.2	1.4	1.6	V
Maximum Operating Frequency		10			MHz
Dividers					
Maximum Input Frequency	Input = 1Vpp at Oscillator Input	10			MHz
Div 2/4 Input Current	Input = 5V (Div. by 2)		150	500	µA
	Input = 0V (Div. by 4)	-5.0	0.0	5.0	µA
Div 2/4 Threshold		0.5	1.6	2.2	V
Divider Output	High Level (w/6.8k Load to GND)	4.0	4.5		V
	Low Level (Open Collector Leakage)			10	µA
Sense Amplifier					
Threshold Voltage	Percent of V_{REF}	27	30	33	%
Threshold Hysteresis			10		µV
Input Bias Current	Input = 1.5V	-1.0	-0.2		µA
Double Edge Disable Input					
Input Current	Input = 5V (Disabled)		150	500	µA
	Input = 0V (Enabled)	-5.0	0.0	5.0	µA
Threshold Voltage		0.5	1.6	2.2	V
Phase Detector					
-Input Threshold	Detector Responds to Falling Edge	0.5	1.6	2.2	V
-Input Current	Input = 2.2V		100	250	µA
High Output Level	Positive Phase/Freq. Error, Volts Below V_{REF}		0.2	0.5	V
Low Output Level	Negative Phase/Freq. Error		0.2	0.5	V
Mid Output Level	Zero Phase/Freq. Error, Percent of V_{REF}	47	50	53	%
High Level Maximum Source Current	V_{OUT} = 4.3V	2.0	8.0		mA
Low Level Maximum Sink Current	V_{OUT} 0.7V	2.0	5.0		mA
Mid Level Output Impedance (Note 3)	I_{OUT} = -200 to +200µA, T_J = 25°C	4.5	6.0	7.5	kΩ
Loop Amplifier					
Non-Inv Reference Voltage	Percent of V_{REF}	47	50	53	%
Input Bias Current	Input = 2.5V	-0.8	-0.2		µA
AVOL		60	75		dB
PSRR	$+V_{IN}$ = 8 to 15V	70	100		dB
Short Circuit Current	Source, V_{OUT} = 0V	16	35		mA
	Sink, V_{OUT} = 5V	16	30		mA

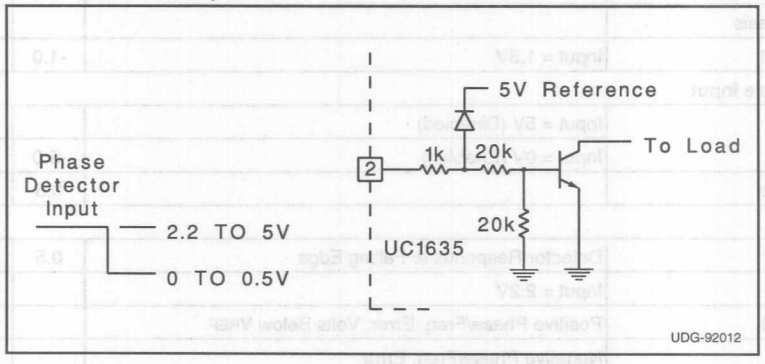
Note 3: These impedance levels will vary with T_J at about 1700ppm/°C.

ELECTRICAL CHARACTERISTICS (cont.): Unless otherwise stated, specifications hold for T_A = 0°C to +70°C for the UC3635, -25°C to +85°C for the UC2635 and -55°C to +125°C for the UC1635, +Vin = 12V. $T_A = T_J$.

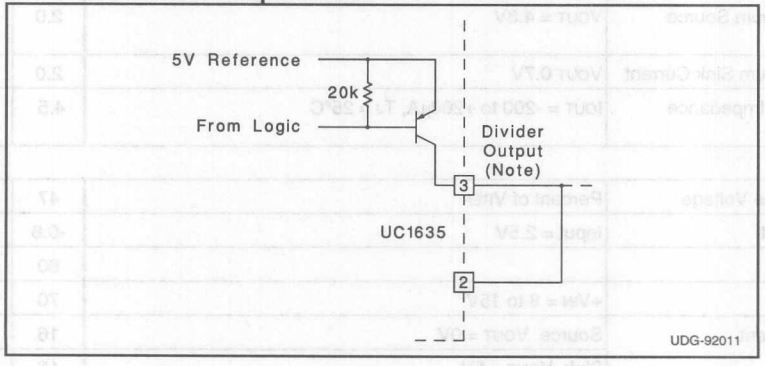
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Auxiliary Op-Amp					
Input Offset Voltage	V_{CM} = 2.5V			8	mV
Input Bias Current	V_{CM} = 2.5V	-0.8	-0.2		µA
Input Offset Current	V_{CM} = 2.5V		.01	0.1	µA
AVOL		70	120		dB
PSRR	$+V_{IN}$ = 8 to 15V	70	100		dB
CMRR	V_{CM} = 0 to 10V	70	100		dB
Short Circuit Current	Source, V_{OUT} = 0V	16	35		mA
	Sink, V_{OUT} = 5V	16	30		mA

Application and Operation Information
(For Additional Application Information see the UC1633 Data Sheet)
(Pin numbers refer to DIL and SOIC packages)

Phase Detector Input



Reference Divider Output Detail



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UNITRODE

UC1637
UC2637
UC3637

Switched Mode Controller for DC Motor Drive

FEATURES

- Single or Dual Supply Operation
- ±2.5V to ±20V Input Supply Range
- ±5% Initial Oscillator Accuracy; ± 10% Over Temperature
- Pulse-by-Pulse Current Limiting
- Under-Voltage Lockout
- Shutdown Input with Temperature Compensated 2.5V Threshold
- Uncommitted PWM Comparators for Design Flexibility
- Dual 100mA, Source/Sink Output Drivers

DESCRIPTION

The UC1637 is a pulse width modulator circuit intended to be used for a variety of PWM motor drive and amplifier applications requiring either uni-directional or bi-directional drive circuits. When used to replace conventional drivers, this circuit can increase efficiency and reduce component costs for many applications. All necessary circuitry is included to generate an analog error signal and modulate two bi-directional pulse train outputs in proportion to the error signal magnitude and polarity.

This monolithic device contains a sawtooth oscillator, error amplifier, and two PWM comparators with ±100mA output stages as standard features. Protection circuitry includes under-voltage lockout, pulse-by-pulse current limiting, and a shutdown port with a 2.5V temperature compensated threshold.

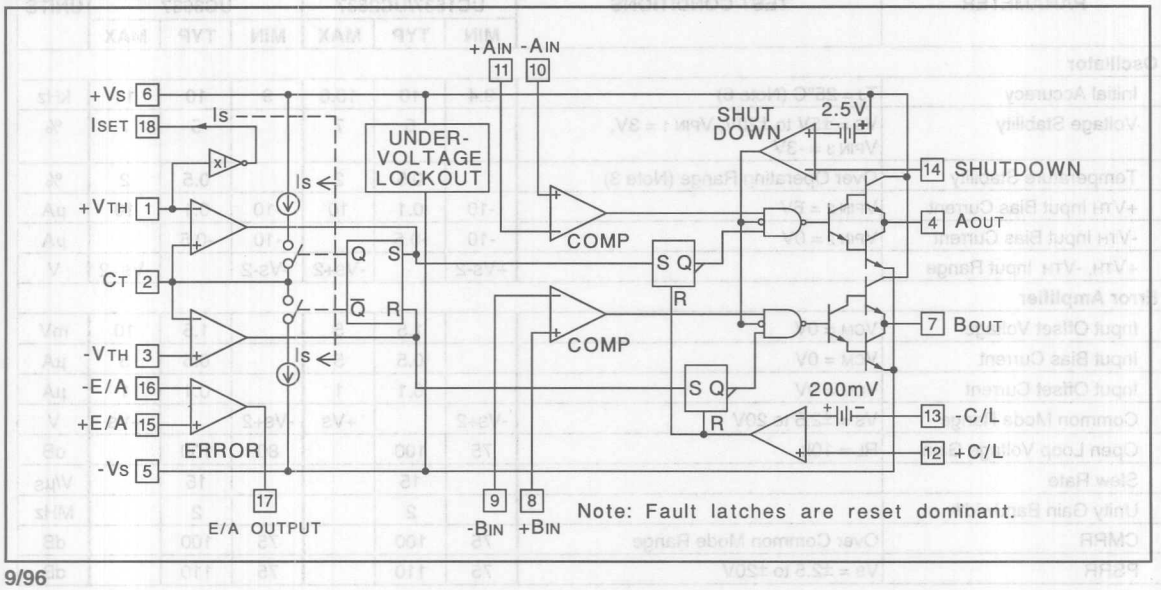
The UC1637 is characterized for operation over the full military temperature range of -55°C to +125°C, while the UC2637 and UC3637 are characterized for -25°C to +85°C and 0°C to +70°C, respectively.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (±Vs)	±20V
Output Current, Source/Sink (Pins 4, 7)	500mA
Analog Inputs (Pins 1, 2, 3, 8, 9, 10, 11 12, 13, 14, 15, 16)	±Vs
Error Amplifier Output Current (Pin 17)	±20mA
Oscillator Charging Current (Pin 18)	-2mA
Power Dissipation at T_A = 25°C (Note 2)	1000mW
Power Dissipation at T_C = 25°C (Note 2)	2000mW
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 Seconds)	+300°C

Note 1: Currents are positive into, negative out of the specified terminal.
Note 2: Consult Packaging Section of Databook for thermal limitations and considerations of package.

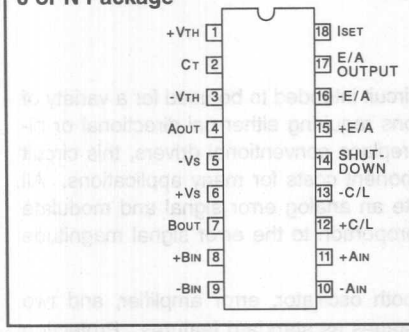
BLOCK DIAGRAM



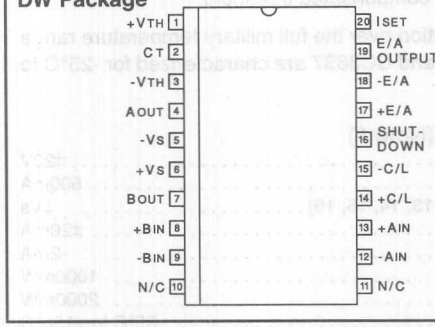
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CONNECTION DIAGRAM

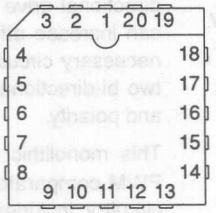
DIL-18 (TOP VIEW)
J or N Package



SOIC-20 (TOP VIEW)
DW Package



PLCC-20, LCC-20
(TOP VIEW)
Q, L Packages



PACKAGE PIN FUNCTION	
FUNCTION	**PIN**
+VTH	1
CT	2
-VTH	3
AOUT	4
-VS	5
N/C	6
+VS	7
BOUT	8
+BIN	9
-BIN	10
-AIN	11
+AIN	12
+C/L	13
-C/L	14
SHUTDOWN	15
N/C	16
+E/A	17
-E/A	18
E/A OUTPUT	19
ISET	20

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1637; -25°C to +85°C for the UC2637; and 0°C to +70°C for the UC3637; +Vs = +15V, -Vs = - 15V, +VTH = 5V, -VTH = -5V, RT = 16.7kΩ, CT = 1500pF, T_A=T_J.

PARAMETER	TEST CONDITIONS	UC1637/UC2637			UC3637			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Oscillator								
Initial Accuracy	T_J = 25°C (Note 6)	9.4	10	10.6	9	10	11	kHz
Voltage Stability	Vs = ±5V to ±20V, VPIN 1 = 3V, VPIN 3 = -3V		5	7		5	7	%
Temperature Stability	Over Operating Range (Note 3)		0.5	2		0.5	2	%
+VTH Input Bias Current	VPIN 2 = 6V	-10	0.1	10	-10	0.1	10	µA
-VTH Input Bias Current	VPIN 2 = 0V	-10	-0.5		-10	-0.5		µA
+VTH, -VTH Input Range		+Vs-2		-Vs+2	+Vs-2		-Vs+2	V
Error Amplifier								
Input Offset Voltage	VCM = 0V		1.5	5		1.5	10	mV
Input Bias Current	VCM = 0V		0.5	5		0.5	5	µA
Input Offset Current	VCM = 0V		0.1	1		0.1	1	µA
Common Mode Range	Vs = ±2.5 to 20V	-Vs+2		+Vs	-Vs+2		+Vs	V
Open Loop Voltage Gain	RL = 10k	75	100		80	100		dB
Slew Rate			15			15		V/µs
Unity Gain Bandwidth			2			2		MHz
CMRR	Over Common Mode Range	75	100		75	100		dB
PSRR	Vs = ±2.5 to ±20V	75	110		75	110		dB

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1637; -25°C to +85°C for the UC2637; and 0°C to +70°C for the UC3637: V_S = +15V, -V_S = - 15V, +V_{TH} = 5V, -V_{TH} = -5V, R_T = 16.7kΩ, C_T = 1500pF, T_A=T_J.

PARAMETERS	TEST CONDITIONS	UC1637/UC2637			UC3637			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Error Amplifier (Continued)								
Output Sink Current	$V_{PIN\ 17}$ = 0V		-50	-20		-50	-20	mA
Output Source Current	$V_{PIN\ 17}$ = 0V	5	11		5	11		mA
High Level Output Voltage		13	13.6		13	13.6		V
Low Level Output Voltage			-14.8	-13		-14.8	-13	V
PWM Comparators								
Input Offset Voltage	V_{CM} = 0V		20			20		mV
Input Bias Current	V_{CM} = 0V		2	10		2	10	µA
Input Hysteresis	V_{CM} = 0V		10			10		mV
Common Mode range	V_S = ±5V to ±20V	-V_S+1		+V_S-2	-V_S+1		+V_S-2	V
Current Limit								
Input Offset Voltage	V_{CM} = 0V, T_J = 25°C	190	200	210	180	200	220	mV
Input Offset Voltage T.C.			-0.2			-0.2		mV/°C
Input Bias Current		-10	-1.5		-10	-1.5		µA
Common Mode Range	V_S = ±2.5V to ±20V	-V_S		+V_S-3	-V_S		+V_S-3	V
Shutdown								
Shutdown Threshold	(Note 4)	-2.3	-2.5	-2.7	-2.3	-2.5	-2.7	V
Hysteresis			40			40		mV
Input Bias Current	$V_{PIN\ 14}$ = +V_S to -V_S	-10	-0.5		-10	-0.5		µA
Under-Voltage Lockout								
Start Threshold	(Note 5)		4.15	5.0		4.15	5.0	V
Hysteresis			0.25			0.25		mV
Total Standby Current								
Supply Current			8.5	15		8.5	15	mA
Output Section								
Output Low Level	I_{SINK} = 20mA		-14.9	-13		-14.9	-13	V
	I_{SINK} = 100mA		-14.5	-13		-14.5	-13	
Output High Level	I_{SOURCE} = 20mA	13	13.5		13	13.5		V
	I_{SOURCE} = 100mA	12	13.5		12	13.5		
Rise Time	(Note 3) C_L = Inf, T_J = 25°C		100	600		100	600	ns
Fall Time	(Note 3) C_L = Inf, T_J = 25°C		100	300		100	300	ns

Note 3: These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.
Note 4: Parameter measured with respect to +Vs (Pin 6).
Note 5: Parameter measured at +Vs (Pin 6) with respect to -Vs (Pin 5).
Note 6: R_T and C_T referenced to Ground.

FUNCTIONAL DESCRIPTION

Following is a description of each of the functional blocks shown in the Block Diagram.

Oscillator

The oscillator consists of two comparators, a charging and discharging current source, a current source set terminal, ISET and a flip-flop. The upper and lower threshold of the oscillator waveform is set externally by applying a voltage at pins +VTH and -VTH respectively. The +VTH terminal voltage is buffered internally and also applied to the ISET terminal to develop the capacitor charging current through RT. If RT is referenced to -Vs as shown in Figure 1, both the threshold voltage and charging current will vary proportionally to the supply differential, and the oscillator frequency will remain constant. The triangle waveform oscillators frequency and voltage amplitude is determined by the external components using the formulas given in Figure 1.

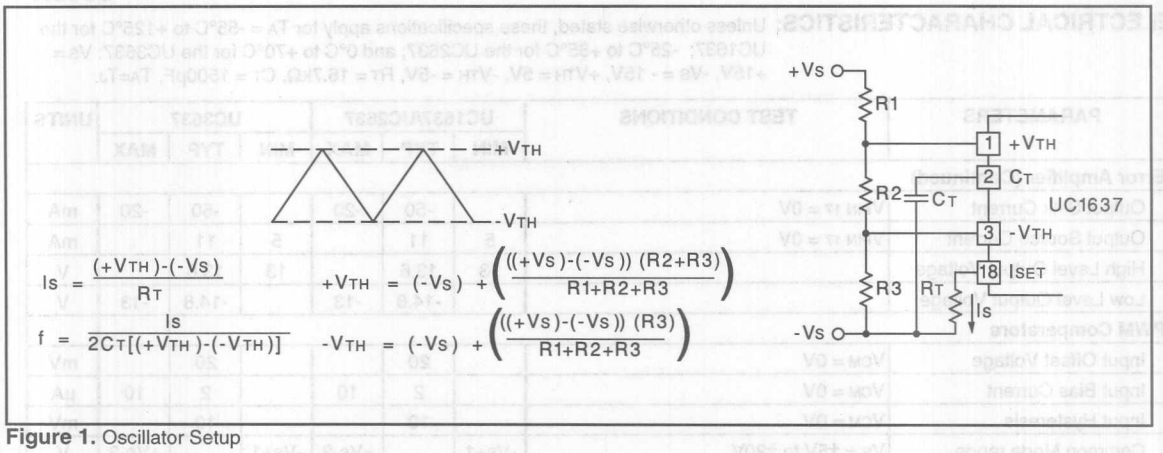


Figure 1. Oscillator Setup

PWM Comparators

Two comparators are provided to perform pulse width modulation for each of the output drivers. Inputs are uncommitted to allow maximum flexibility. The pulse width of the outputs A and B is a function of the sign and amplitude of the error signal. A negative signal at Pin 10 and 8 will lengthen the high state of output A and shorten the high state of output B. Likewise, a positive error signal reverses the procedure. Typically, the oscillator waveform is compared against the summation of the error signal and the level set on Pin 9 and 11.

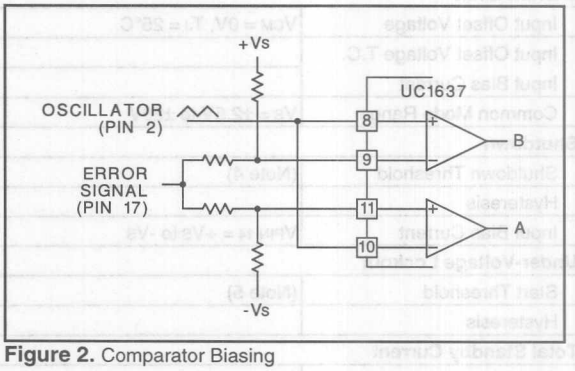


Figure 2. Comparator Biasing

MODULATION SCHEMES

Case A Zero Deadtime (Equal voltage on Pin 9 and Pin 11)
In this configuration, maximum holding torque or stiffness and position accuracy is achieved. However, the power input into the motor is increased. Figure 3A shows this configuration.

Case B Small Deadtime (Voltage on Pin 9 > Pin 11)
A small differential voltage between Pin 9 and 11 provides the necessary time delay to reduce the chances of momentary short circuit in the output stage during transitions, especially where power-amplifiers are used. Refer to Figure 3B.

Case C Increased Deadtime and Deadband Mode
(Voltage on Pin 9 > Pin 11)
With the reduction of stiffness and position accuracy, the power input into the motor around the null point of the servo loop can be reduced or eliminated by widening the window of the comparator circuit to a degree of acceptance. Where position accuracy and mechanical stiffness is unimportant, deadband operation can be used. This is shown in Figure 3C.

Output Drivers

Each output driver is capable of both sourcing and sinking 100mA steady state and up to 500mA on a pulsed basis for rapid switching of either POWERFET or bipolar transistors. Output levels are typically -Vs + 0.2V @50mA low level and +Vs - 2.0V @50mA high level.

Error Amplifier

The error amplifier consists of a high slew rate (15V/µs) op-amp with a typical 1MHz bandwidth and low output impedance. Depending on the ±Vs supply voltage, the common mode input range and the voltage output swing is within 2V of the Vs supply.

Under-Voltage Lockout

An under-voltage lockout circuit holds the outputs in the low state until a minimum of 4V is reached. At this point, all internal circuitry is functional and the output drivers are enabled. If external circuitry requires a higher starting voltage, an over-riding voltage can be programmed through the shutdown terminal as shown in Figure 4.

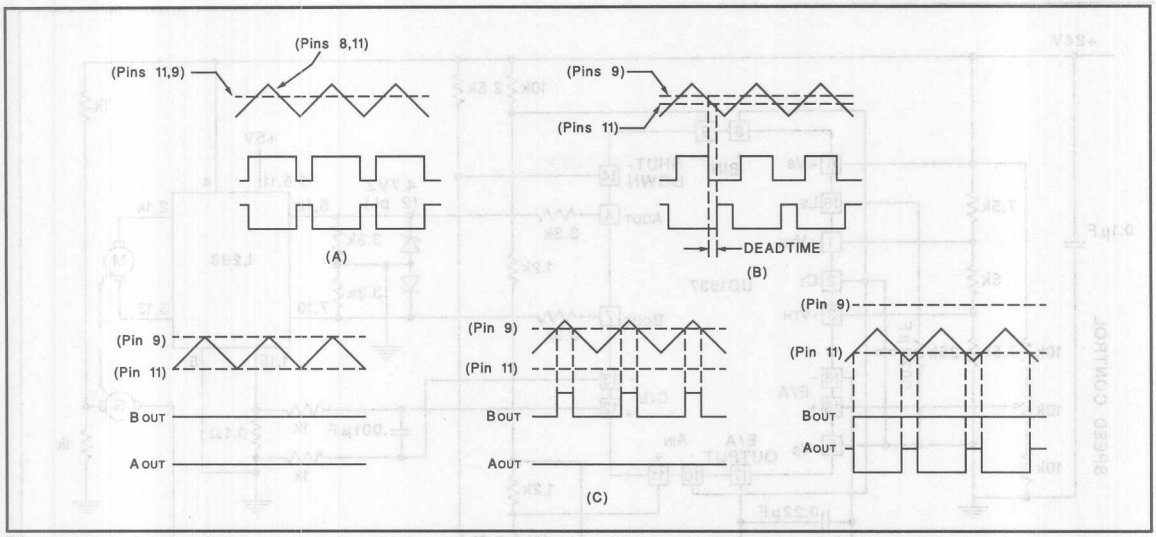


Figure 3. Modulation Schemes Showing (A) Zero Deadtime (B) Deadtime and (C) Deadband Configurations

Shutdown Comparator

The shutdown terminal may be used for implementing various shutdown and protection schemes. By pulling the terminal more than 2.5V below VIN, the output drivers will be enabled. This can be realized using an open collector gate or NPN transistor biased to either ground or the negative supply. Since the threshold is temperature stabilized, the comparator can be used as an accurate low voltage lockout (Figure 4) and/or delayed start as in Figure 5. In the shutdown mode the outputs are held in the low state.

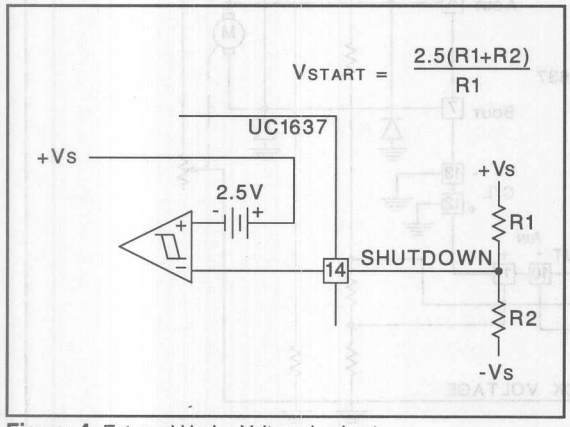


Figure 4. External Under-Voltage Lockout

Current Limit

A latched current limit amplifier with an internal 200mV offset is provided to allow pulse-by-pulse current limiting. Differential inputs will accept common mode signals from -Vs to within 3V of the +Vs supply while providing excellent noise rejection. Figure 6 shows a typical current sense circuit.

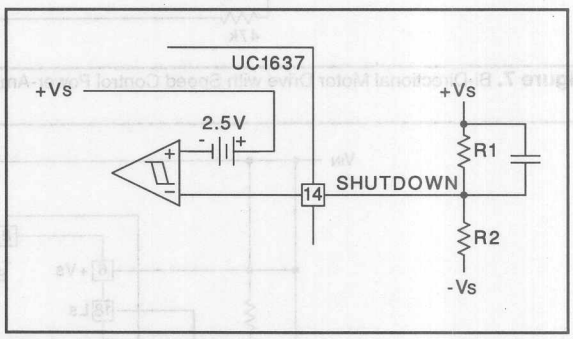


Figure 5. Delayed Start-Up

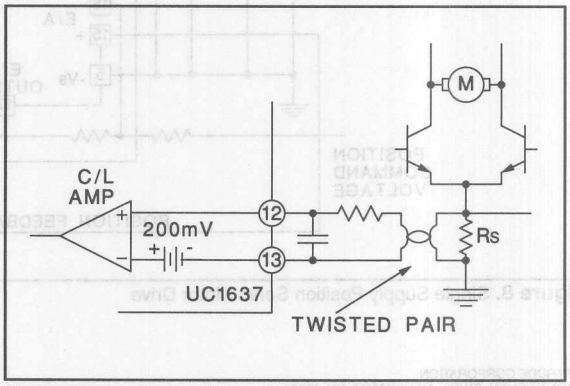


Figure 6. Current Limit Sensing

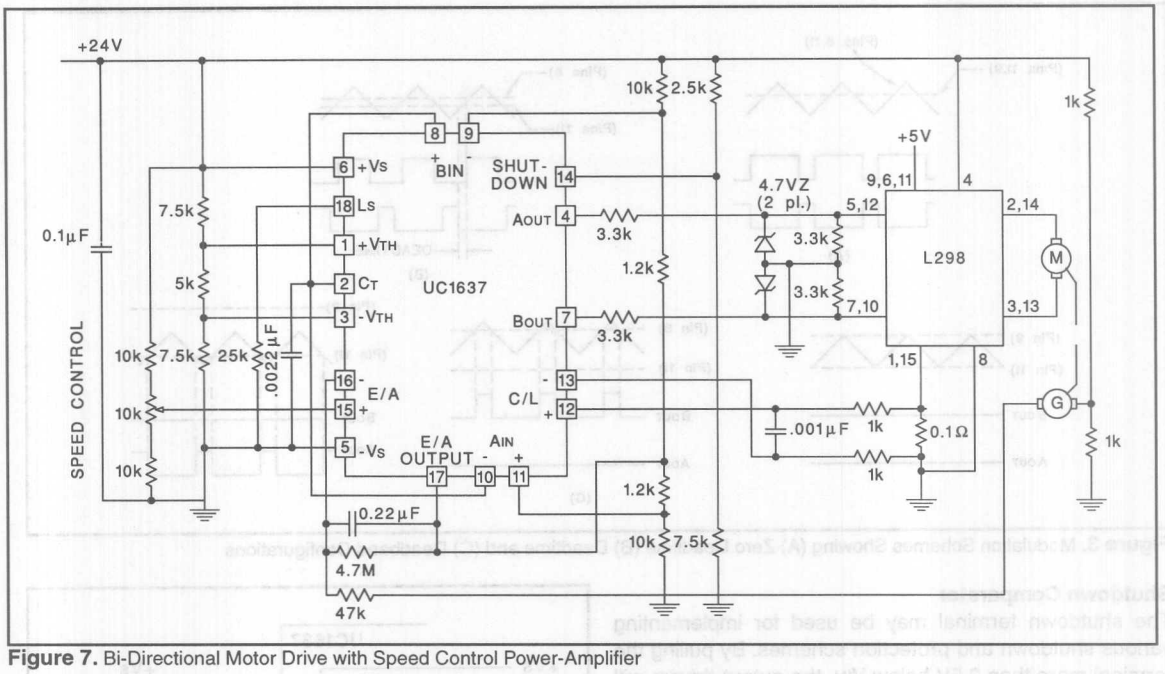


Figure 7. Bi-Directional Motor Drive with Speed Control Power-Amplifier

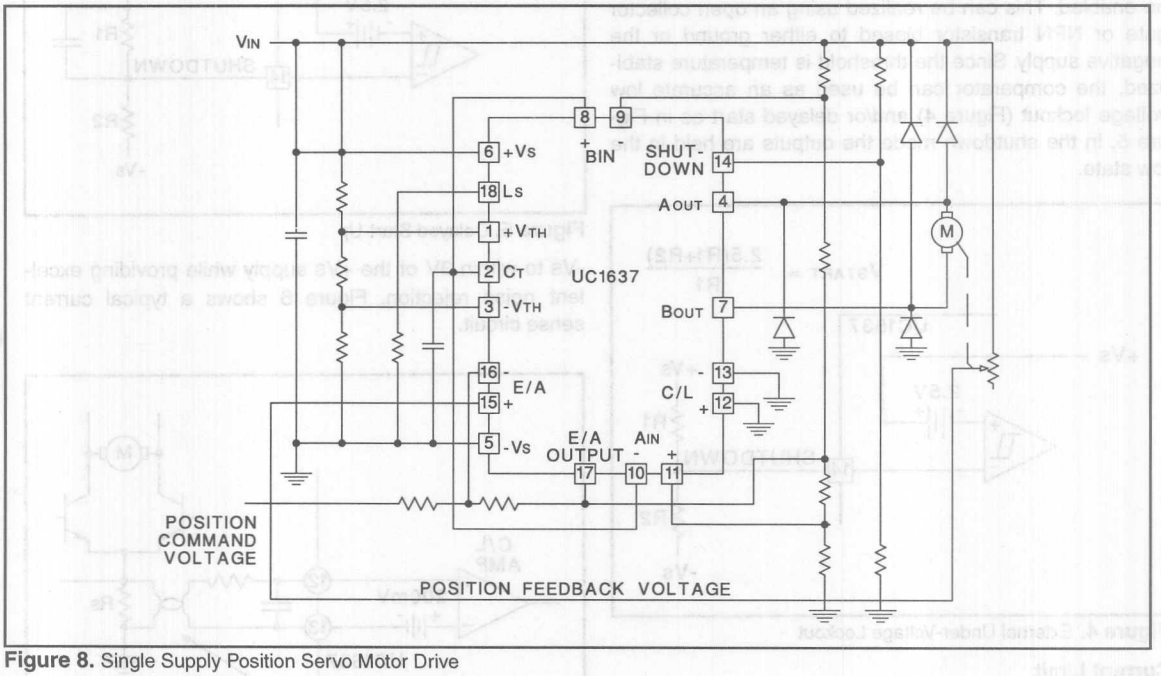


Figure 8. Single Supply Position Servo Motor Drive

UNITRODE CORPORATION
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Advanced PWM Motor Controller

FEATURES

- Single or Dual Supply Operation
- Accurate High Speed Oscillator
- Differential X5 Current Sense Amplifier
- Bidirectional Pulse-by-Pulse Current Limiting
- Programmable Oscillator Amplitude and PWM Deadband
- Dual 500mA Totem Pole Output Drivers
- Dual 60V, 50mA Open Collector Drivers
- Undervoltage Lockout

DESCRIPTION

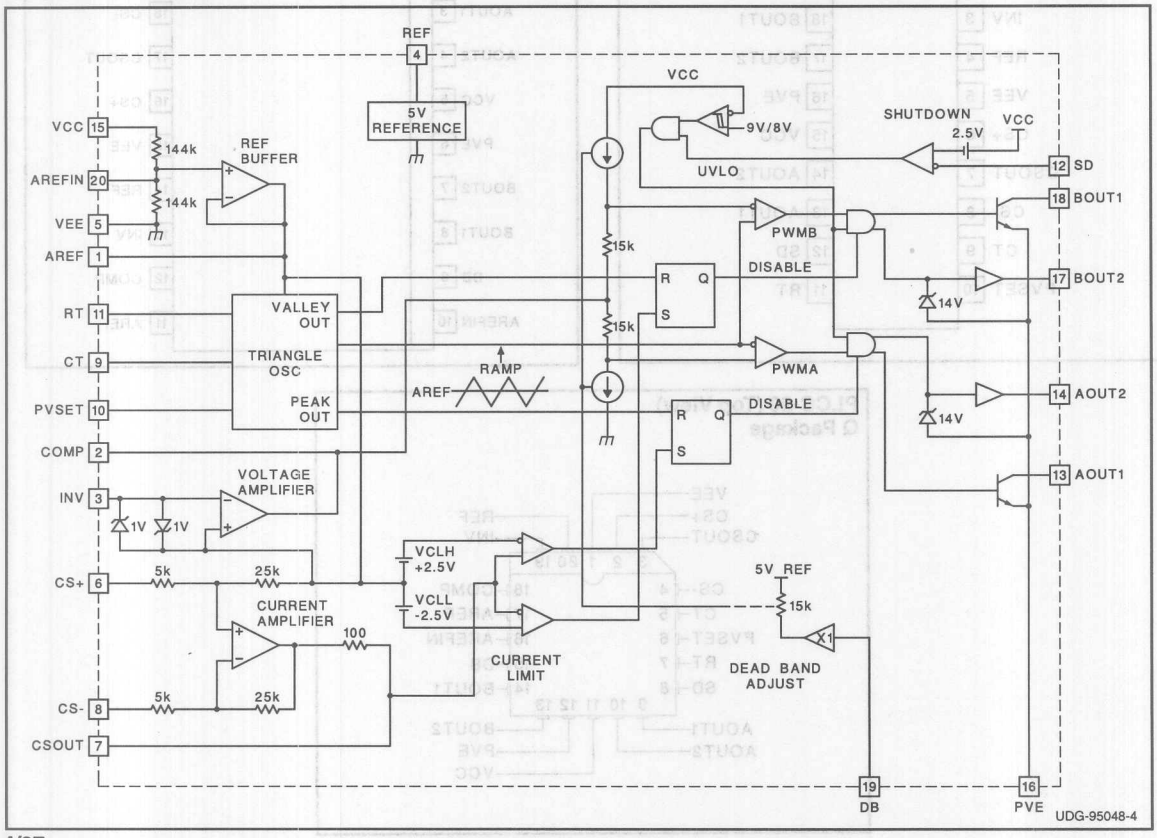
The UC1638 family of integrated circuits are advanced pulse width modulators intended for a variety of PWM motor drive and amplifier applications requiring either uni-directional or bi-directional drive circuits. Similar in architecture to the UC1637, all necessary circuitry is included to generate an analog error signal and modulate two bi-directional pulse train outputs in proportion to the error signal magnitude and polarity.

Key features of the UC1638 include a programmable high speed triangle oscillator, a 5X differential current sensing amplifier, a high slew rate error amplifier, high speed PWM comparators, and two 50mA open collector as well as two ±500mA totem pole output stages. The individual circuit blocks are designed to provide practical operation to switching frequencies of 500kHz.

Significant improvements in circuit speed, elimination of many external programming components, and the inclusion of a differential current sense amplifier, allow this controller to be specified for higher performance applications, yet maintain the flexibility of the UC1637. The current sense amplifier in conjunction with the error amplifier can be configured for average current feedback. The additional open collector outputs provide a drive signal

continued

BLOCK DIAGRAM



DESCRIPTION (cont.)

for the highside switches in a full bridge configuration. The programmable AREFIN pin allows for single or dual supply operation. Oscillator ramp amplitude and PWM deadband are programmable by tapping a voltage divider off the 5V reference to the appropriate programming input (PVSET or DB).

Additional features include a precision externally available 5V reference, undervoltage lockout, pulse-by-pulse peak current limiting, and a remote shutdown port. The UC1638 family is available in the 20 pin N, DW and J packages. Consult the factory for other packaging options.

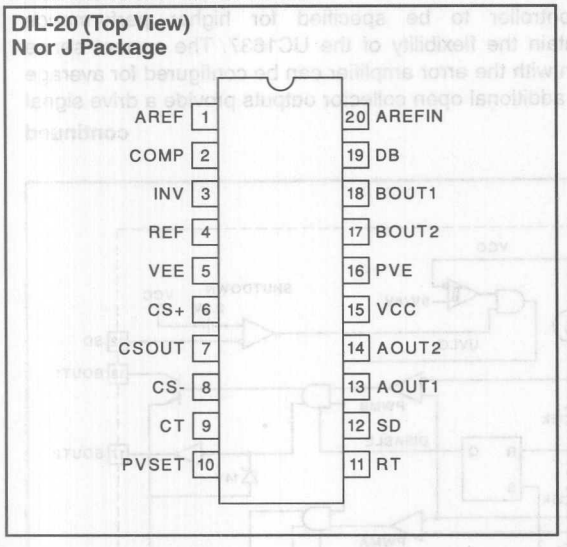
ABSOLUTE MAXIMUM RATINGS

Supply Voltage VCC (referenced to VEE) 40V
Output Drivers (AOUT2, BOUT2)
Currents (continuous) . . . . . ±0.25A
Currents (peak) . . . . . ±500mA
REF Output Current . . . . . Internally Limited
PVSET, DB, RT, INV, REF, CSOUT . . . . . 0.3 to 10V
CS+, CS- . . . . . –1V to VCC
CT, AREF, AREFIN, COMP, SD . . . . . VEE – 0.3
Output Voltage (AOUT1, BOUT1) 60V
Storage temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead temperature (soldering, 10 sec.) . . . . . +300°C

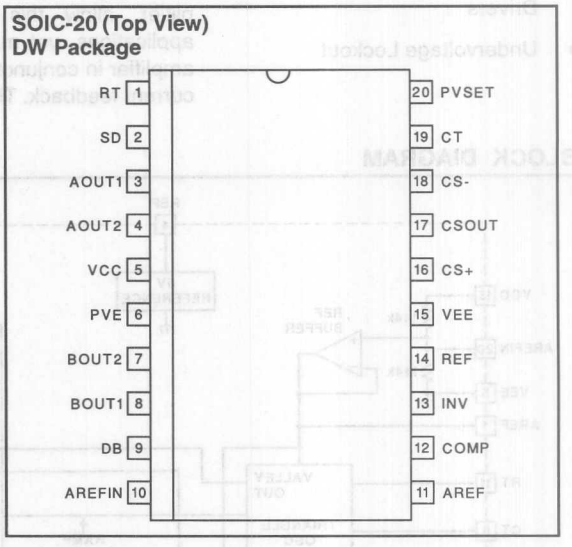
Currents are positive into, negative out of the specified terminal. Consult packaging section of data book for thermal limitation considerations of packages.

CONNECTION DIAGRAMS

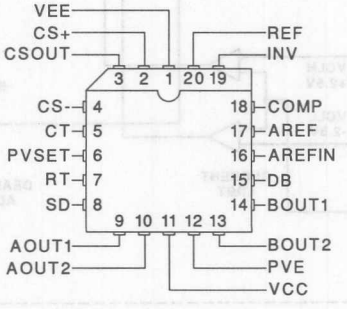
DIL-20 (Top View)
N or J Package



SOIC-20 (Top View)
DW Package



PLCC-20 (Top View)
Q Package



ELECTRICAL CHARACTERISTICS Unless otherwise specified; VCC = 15V, VEE =-15V, CT = 680pF, RT = 3k, V_{PVSET} = 1.5V, V_{COMP} = 0V, V_{CSOUT} = 0V, V_{DB} = REF, V_{EXTREF} = 0V, V_{SD} = VCC - 3V, T_A = –55°C to 125°C for the UC1638, –25°C to 85°C for the UC2638, 0°C to 70°C for the UC3638. T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Overall					
Supply Current, Operating			15	23	mA
UVLO Threshold	Reference to VEE		9	10	V
UVLO Hysteresis	Reference to VEE		1		V
Voltage Amplifier					
Input Offset Voltage	COMP = 0V	–15	0	15	mV
V_{SENSE} Bias Current		0	0.5	2	mA
Open Loop Gain	COMP = –5V to +5V	75	100		dB
CMRR	V_{CM} = –5V to +5V		100		dB
PSRR	VCM = 0V, VCC – VEE = 10V to 36V		90		dB
V_{OUT} High	INV = –0.1V, RL = 10k		13.6		V
V_{OUT} Low	INV = +0.1V, RL = 10k		–13.8		V
Slew Rate Rising and Falling	Overdrive = ±1V		12		Vμs
Output Source Current	COMP Shorted to VEE		5		mA
Output Sink Current	COMP Shorted to VCC		8		mA
Gain Bandwidth Product	F_{IN} = 100kHz, 10mV p-p		5		MHz
5V Reference					
Output Voltage	I_{REF} = –1mA, T_A = 25°C	4.925	5	5.075	V
Output Voltage	I_{REF} = –1mA	4.875	5	5.125	V
Load Regulation	I_{REF} = –1mA to –10mA	–15	2	15	mV
Line Regulation	VCC - VEE = 10V to 36V	–15	2	15	mV
Short Circuit Current	V_{REF} = 0V	15	70		mA
Oscillator					
Initial Accuracy	T_A = 25°C		98		kHz
	T_A = 25°C, PV = 1V, RT = 1.5k		196		kHz
Voltage Stability	VCC – VEE = 10V to 36V		2		%
Total Variation	Line, Temperature		98		kHz
PVSET Input Bias Current			0.5	3	μA
PVSET Input Voltage Range	(Note 1)	0.5		VREF	V
Amplitude Limit	(Note 1)	VEE+3		VCC–3	V
AOUT1, BOUT1 Output Drivers					
Output Low Voltage	I_{OUT} = 1mA, Ref. to PVE, PVE = 0V		0.9	1.3	V
	I_{OUT} = 50mA		1.2	1.8	V
Leakage Current	Output Voltage = 50V		0.1	25	μA
AOUT2, BOUT2 Output Drivers					
Output High Voltage	I_{OUT} = –20mA, Ref. to PVE, PVE = 0V	12.5	13.5		V
	I_{OUT} = –100mA, Ref. to PVE, PVE = 0V	12	13.5		V
Output High Clamp Level	I_{OUT} = –20mA, Ref. to PVE, PVE = VEE		14.4	16.5	V
Output Low Voltage	I_{OUT} = 20mA, Ref. to PVE, PVE = 0V		0.4	1	V
	I_{OUT} = 100mA, Ref. to PVE, PVE = 0V		0.6	2.2	V
Output Rise Time	C_{OUT} = 1nF		50		ns
Output Fall Time	C_{OUT} = 1nF		50		ns

ELECTRICAL CHARACTERISTICS(cont.) Unless otherwise specified; VCC = 15V, VEE =-15V, CT = 680pF, RT = 3k, V_{PVSET} = 1.5V, V_{COMP} = 0V, V_{CSOUT} = 0V, V_{DB} = REF, V_{EXTREF} = 0V, V_{SD} = VCC - 3V, T_A = –55°C to 125°C for the UC1638, –25°C to 85°C for the UC2638, 0°C to 70°C for the UC3638. T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
X5 Amplifier					
Gain	V_{ID} = 100mV to 400mV		5		V/V
Output Offset Voltage	V_{HI} = V_{LO}		0		V
Common Mode Rejection	V_{CS+}, V_{CS-} = AREF ±5V		65		dB
–3dB Bandwidth			300		kHz
Slew Rate Rising			2		V/µs
Slew Rate Falling			2		V/µs
Shutdown					
Threshold	Ref. to VCC	–1.9	–2.25	–2.5	V/V
Input Bias Current	V_{SD} = SD Threshold		–0.5	–10	µA
Current Limit					
Threshold Positive	Measured Between CS+ and CS-		500		mV
Threshold Negative	Measured Between CS+ and CS-		–500		mV
Propagation Delay to Outputs	Overdrive = 200mV		150	250	ns
Deadband Adjust					
Maximum Deadband	V_{DB} = 0V		±5		V
Zero Deadband	V_{DB} = REF		0		V
Deadband Adjustment Gain	V_{DB} = 1V to 4V (Note 2)		±1		V/V
Input Bias Current	V_{DB} = VREF		3	15	µA
AREF Buffer					
Gain	AREF / VCC – VEE		0.5		V/V
Offset	(Note 3)		30	100	mV

Note 1: Oscillator triangle amplitude = 2.5 • PV ±AREF.

Note 2: Deadband = ±(REF – DB), referenced to COMP.

Note 3: Offset = AREFIN – AREF.

PIN DESCRIPTIONS

AOUT1, BOUT1: AOUT1 and BOUT1 are open collector output drivers capable of sinking 50mA. These outputs can be pulled up to 60V maximum. With a few external components, these outputs can drive the opposite high side switches in a full bridge arrangement.

AOUT2, BOUT2: AOUT2 and BOUT2 are totem pole output drivers capable of driving external power MOSFETs directly. The peak current ratings are ±500mA. An integrated zener clamp limits the drive output amplitude to approximately 14V to prevent MOSFET gate oxide overstress. These outputs are configured to drive the opposite low side switches in a full bridge arrangement.

AREF: The voltage on AREF is simply a buffered version of the voltage on AREFIN. In single supply applications, AREF should be bypassed to VEE with a 0.1µF ceramic capacitor to provide a stable reference level for the internal circuitry.

AREFIN: The voltage on AREFIN is generated internally by a 50% voltage divider tied between VCC and VEE. As such, it provides the mid supply reference needed for the oscillator, voltage amplifier, current amplifier and current limit comparators when operating in single supply mode. A buffer amplifier is connected between AREFIN and AREF. In bipolar supply applications AREFIN is usually connected to VEE, which disables the buffer amplifier, and AREF is connected to 0V.

COMP: This is the output of the high slew rate error amplifier. The level on COMP modulates the controller duty cycle via the PWM comparators and the oscillator ramp. Compensation and DC gain setting resistors are connected between COMP and INV.

CS-: This is the inverting input to the X5 current sense amplifier. The common mode input range for this pin extends from –1V to VCC–4V. A low value resistor in se-

PIN DESCRIPTIONS (cont.)

ries with the source or emitter of the low side switch in the full bridge develops the signal that is applied to this pin. At differential inputs of ±500mV typical (referenced to CS+)the controller reaches the current limit level, which truncates the output pulse.

CS+: This is the non-inverting input to the X5 current sense amplifier. The common mode input range for this pin extends from –1V to VCC–4V. The characteristics for this pin are identical to CS-.

CSOUT: This is the output of the X5 current sense amplifier. Voltage levels greater than ±2.5V referenced to AREF will cause the device to enter current limit. An internal 100 ohm resistor between the amplifier output and CSOUT is provided to create a high frequency noise filter with an external capacitor to VEE. When used for average current feedback, CSOUT is summed into INV.

CT: A capacitor from CT to VEE will will set the triangle oscillator frequency according to the following equation:

$$F = \frac{1}{5 \bullet R_T \bullet C_T}.$$

The waveform on CT is symmetrical about the voltage on AREF and is applied internally to the inputs of the PWM comparators. Use a high quality ceramic capacitor with low ESL and ESR for best results. A minimum C_T value of 200pF insures good accuracy and less susceptibility to circuit layout parasitics. The oscillator and PWM are designed to provide practical operation to 500kHz.

DB: This high impedance input programs output pulse train deadtime. A stable DC voltage between 0V and REF will set a bi-directional deadband centered about the level on COMP. The deadband level is equal to: 5V – VDB. That is, 1V on DB will program ±4V of deadband centered about the COMP pin level. A convenient method for generating the programming level is a voltage divider tap off of REF.

INV: This is the inverting input to the Voltage amplifier. The common mode input range for this pin extends from VEE+2V to VCC–1V. It can be tied to a command signal generated by a rate feedback element or to a position control signal. In average current feedback applications, this input is tied to the output of the X5 current sensing amplifier (CSOUT).

PVE: This is the high current ground for the IC. The external MOSFET driver transistors are referenced to this ground. Internal level shifting circuitry gives the option of tying this pin to VEE, or the system ground in split supply applications.

PVSET: A DC voltage on PVSET programs the upper and lower thresholds for the oscillator by the following relationship:

$$V_{PK} - V_{VLY} = 5 \bullet V_{PVSET}.$$

The input voltage range on PVSET is 0.5V to REF.

REF: REF is the output of the precision reference. The output is capable of supplying 15mA to peripheral circuitry and is internally short circuit current limited. Bypass REF to VEE with a 0.1µF ceramic capacitor for best performance.

RT: A single resistor from RT to VEE sets the charging and discharging currents for the triangle oscillator. The actual charge and discharge is 2X the current programmed by RT and PVSET. For best performance the current out of RT should be limited to 1mA. The voltage level on the RT pin is a buffered version of the PVSET pin voltage. Therefore, if the PVSET voltage divider is tied between VCC and VEE to incorporate line feedforward, the triangle waveform frequency will remain constant.

SD: A voltage on SD within 2.5V (typical) of VCC will cause the UC3638 to enter a UVLO condition which disables all of the driver outputs. With an external voltage divider across VCC and VEE, and a capacitor between SD and VCC, a delayed turn-on characteristic can be generated. Since the 2.5V threshold is temperature stabilized it can also be used as a higher UVLO threshold for applications which require a starting voltage higher than the internal 9V UVLO threshold.

VEE: All voltages are measured with respect to this pin. All bypass capacitors and timing components except those listed under the PVE section should be connected to this pin. Component leads should be as short and direct as possible. VEE is generally connected to the most negative voltage supply in the system. In single supply applications, VEE is tied to the system ground.

VCC: Positive supply rail for the IC. Bypass this pin to VEE and PVE with 0.1 to 1µF low ESL, ESR ceramic capacitor(s). The maximum voltage for VCC is 40V referenced to VEE. The turn on voltage level on VCC is 9V with 1V of hysteresis.

APPLICATION INFORMATION

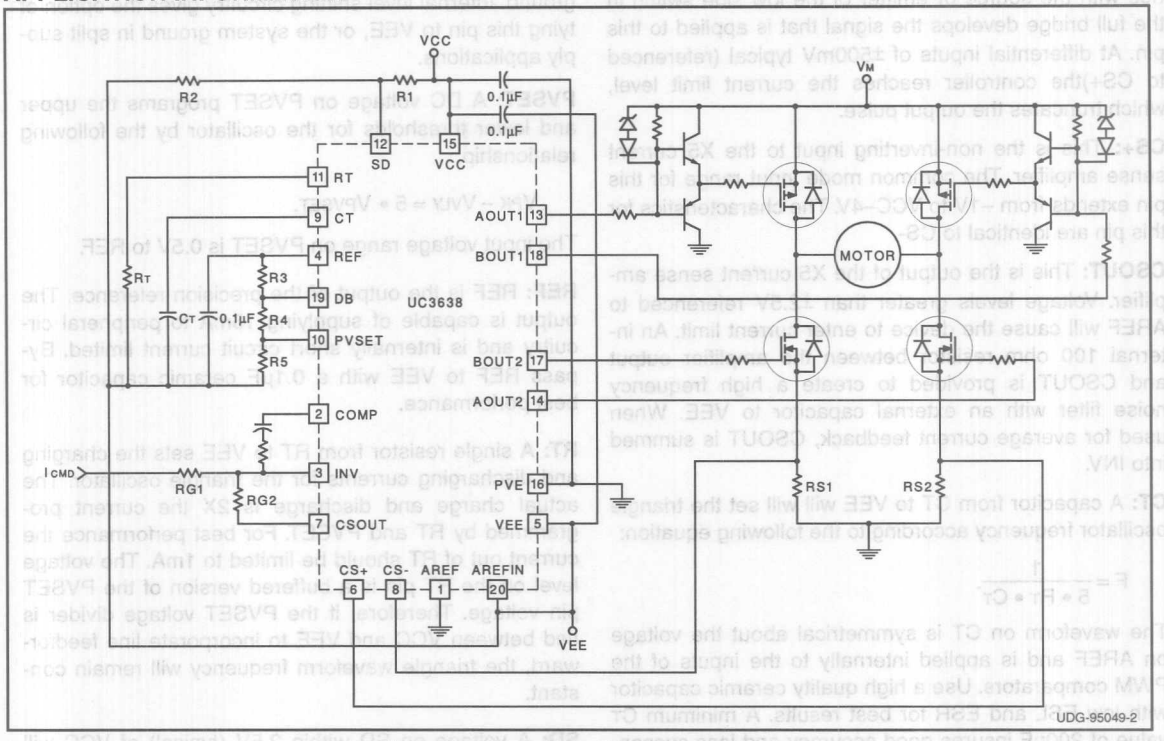


Figure 1. Average Motor Current Control Loop

The UC3638 is designed to provide pulse width modulation control of DC brush motors in applications requiring precision torque, velocity, or position control. Due to its high frequency capability, other high power applications such as switch mode audio amplifiers can also be addressed. Through a combination of circuit sophistication and integration, the designer can maintain a high level of flexibility, while reducing cost compared to solutions using other PWM ICs.

Figure 1 shows a typical application circuit for the UC3638. By taking advantage of the UC3638's many integrated functions, a low cost and compact average current mode motor controller can be designed. Depending on the level of complexity, as many as 15 discrete components and an additional high bandwidth amplifier can be saved compared to a similar circuit using the UC3637 PWM controller.

Oscillator Section and Modulation Scheme

Figure 2 depicts the UC3638 oscillator and PWM waveforms for the condition where the output of the voltage amplifier (COMP) is at the null point (same voltage as AREF). For applications using split voltage supply rails, AREF will normally be tied to system ground. This results in a voltage null point of zero volts. For this condition, AREFIN should be tied to the negative voltage supply rail (VEE), which disables the internal voltage buffer, allowing AREF to be tied to ground. For a single supply system, AREFIN should be left open circuit, and AREF should be decoupled to VEE (system ground) with at least 0.1µF. The resulting voltage null point for this case

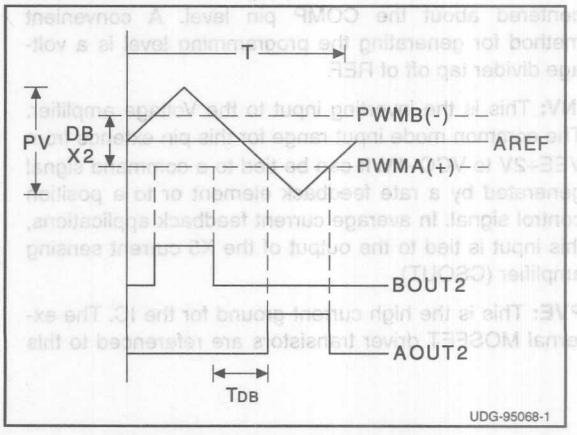


Figure 2. Oscillator and PWM Waveforms

APPLICATION INFORMATION (cont.)

will be half way between ground and VCC, and will automatically track changes in VCC. For cases where a different null point is desired, AREF can be tied to any voltage between VEE + 2V and VCC – 2V. Of course the user must also allow sufficient headroom for the triangle waveform.

Once the system null point has been chosen, the triangle wave amplitude and PWM deadband must be programmed. The amplitude of the triangle wave is determined by trading off noise immunity and gain requirements. In general, the larger the triangle wave amplitude, the greater the immunity to premature termination of PWM pulses due to switching noise. However, high amplitude triangle waves require a greater voltage swing at the output of the voltage amplifier which ultimately reduces forward loop gain.

Programming the PWM deadband allows the user to trade off gain linearity requirements with power amplifier efficiency. If the modulator is configured as in Figure 1, motor current is alternately pulsed by diagonally opposite drive FETs when the servo loop is at null. By adjusting the deadband, the user can program the offset voltage at the input of the PWM comparators. This offset results in deadtime, or time when neither PWM signal is active.

A minimum amount of deadtime is always recommended to provide cross conduction protection at the power amplifier. Setting the deadtime to this minimum level will provide the maximum motor stiffness or holding torque, at the expense of power losses in the output stage. These losses result from the fact that the power amplifier is always sourcing motor current, even at null. As deadtime is increased, amplifier losses at null become less, at the expense of nonlinearity in the gain function. Eventually, if the deadband voltage is increased to equal the amplitude of the triangle wave, error voltages at the null point will result in no PWM pulsing, or a dead zone. After the triangle waveform amplitude and deadband are selected, the operating frequency is easily set by proper selection of CT and RT.

Referring to Figure 1, if the voltage supply rails are ±15V, and the desired triangle wave oscillator amplitude is 6V p-p, PVSET is set by:

$$V_{PK} - V_{VLY} = 5 \bullet V_{PVSET}$$

$$V_{PVSET} = \frac{6}{5} = 1.2V$$

If 1V of deadband is chosen:

$$5 - V_{DB} = 1V$$

$$V_{DB} = 4V$$

In order to select the programming resistors, a source current for the reference is first selected. For a 1mA source current:

$$R3 + R4 + R5 = \frac{5}{I_{SOURCE}} = \frac{5}{1mA} = 5k$$

$$R3 = \frac{5 - V_{DB}}{I_{SOURCE}} = \frac{1V}{1mA} = 1k$$

$$R4 = \frac{V_{DB} - V_{PVSET}}{I_{SOURCE}} = \frac{4V - 1.2V}{1mA} = 2.8k$$

$$R5 = 5k - 1k - 2.8k = 1.2k$$

All of the voltages described by these equations are referenced to the negative supply rail. In other words, for a split supply system, VREF is actually a negative voltage referenced to ground.

The oscillator frequency is programmed by proper selection of RT and CT. If 220pF is chosen for CT, and an operating frequency of 30kHz is desired, RT is chosen by:

$$F = \frac{1}{5 \bullet RT \bullet CT}$$

$$30kHz = \frac{1}{5 \bullet 220pF \bullet RT}$$

$$RT = 30k$$

With RT = 30k, the charge current out of the RT pin is limited to

$$\frac{1.2V}{30k} = 40\mu A,$$

which is well within the specified maximum of 1mA.

To calculate the actual deadtime or minimum time between PWM pulses (T_{DB}), the ratio of the deadband voltage to the triangle wave amplitude is multiplied by half the oscillator period:

$$T_{DB} = \frac{DB}{V_{PK} - V_{VLY}} \bullet \frac{1}{f}$$

$$= \frac{5 - V_{DB}}{5 \bullet V_{PVSET}} \bullet (5 \bullet R_T \bullet C_T)$$

$$= \frac{(5 - V_{DB}) \bullet R_T \bullet C_T}{V_{PVSET}}$$

For this example the deadtime is:

$$T_{DB} = \frac{1 \bullet 30k \bullet 220pF}{1.2} = 5.5\mu sec$$

If voltage feedforward is desired, PVSET should be derived off of the supply rails instead of VREF. This way changes in the supply voltage will linearly regulate the modulator gain, which decreases control loop susceptibility to line voltage variations. Since the voltage on the RT pin is a buffered version of PVSET, charge current

APPLICATION INFORMATION (cont.)

tracks oscillator amplitude, and therefore the frequency remains constant, preventing low frequency oscillator modulation in the presence of line voltage changes.

Output Drivers

The output driver section provides separate output drivers for high and low side drive of both PWM signals. For many applications, the 500mA peak output current capability of the low side drivers (AOUT2 and BOUT2) is sufficient to directly connect to the appropriate low side MOSFETs of the H-bridge. A current limiting gate resistor may be used to control switching time if high levels of dv/dt or di/dt are expected at the drains of the MOSFETs. If more current drive capability is required, the PWM drive signals can be buffered with bipolar transistors.

The open collector high side drivers (AOUT1 and BOUT1) are designed to control high side P-channel MOSFETs. Depending on voltage and speed requirements, the driver stage can be simplified from the one shown on Figure 1. If high side N-channel MOSFETs are desired, a boot strap or charge pump based drive circuit can be used as long as 100% duty cycle operation is not required.

Average Current Control

The UC3638 incorporates all of the necessary features for precise average current loop control of a DC motor. In the circuit shown in Figure 1, motor current is sensed differentially across two current sense resistors.By using two current sense resistors both the current sourced from the motor voltage supply (Vm) and the flyback current are sensed in the correct polarity to provide true torque control. If only one current sensed resistor is used, the flyback current will circulate through the body diodes of the lower MOSFETs and bypass the current sense resistor. The result will be a duty cycle dependent error term in the loop torque control function. In order to prevent high frequency spikes from contributing excessive error to the current control loop, the switching speed of the MOSFETs must be controlled so that significant transient current spikes do not couple across the drain to source capacitance of the MOSFETs.

The X5 current amplifier multiplies the current signal by a factor of 5 and feeds the average current signal into the error amplifier. A window comparator detects if the peak current signal at the output of the current amplifier has a magnitude greater than 2.5V in either polarity and provides pulse-by-pulse peak current limiting. The loop should be designed so that peak motor current never reaches this level during normal operation.

With integral compensation, the average current loop will have very high DC gain, resulting in effectively no average DC motor current error. For stability purposes, the high frequency gain of the voltage error amplifier must be designed such that magnitude of the slope of the error amplifier output (COMP) must be less than or equal to the magnitude of the slope of the triangle waveform.

If RS1 = RS2 = RS, the DC gain of the current control loop can be calculated as:

$$\frac{I_{MOTOR}}{I_{CMD}} = \frac{RG2}{5 \bullet RG1 \bullet RS}$$

If the UC3638 is set up in a simple velocity or position control loop, the feedback voltage (speed or position) is summed directly into the voltage error amplifier, and the current sense amplifier is only used for peak current limit control. The motor can also be replaced by another high power device, such as an audio speaker, and the same type of amplifier can be used. In the case of audio however, a higher switching frequency will probably be desired to prevent switching noise from infiltrating the audio frequency range.

UVLO and Shutdown

The UC3638 contains undervoltage lockout (UVLO) circuitry to prevent unwanted bridge turn-on before sufficient supply voltage is available. The open collector drivers (AOUT1 and BOUT1) are held off (no sink current) and the totem pole drivers (AOUT 2 and BOUT2) are pulled low until the voltage between VCC and VEE reaches 9V typical. The UVLO circuitry becomes active at approximately 1V, and before this level the totem pole drivers are held low with passive pull down resistors.

The shutdown pin holds the output drivers in their inactive state unless it is pulled 2.5V below VCC. An open collector gate or transistor can be used as an external enable signal, or a turn-on voltage higher than UVLO can be programmed with a resistive divider. In the case of Figure 1, the turn on voltage V_{START} can be calculated as:

$$V_{START} = \frac{2.5 \bullet (R1+R2)}{R1}$$

If a delayed start is desired, a capacitor can be placed in parallel with R1 to slow down the change in voltage at the shutdown pin, and thus provide a user programmable startup time.

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UNITRODE

Stepper Motor Drive Circuit

UC1717
UC2717
UC3717

FEATURES

- Half-step and Full-step Capability
- Bipolar Constant Current Motor Drive
- Built-in Fast Recovery Schottky Commutating Diodes
- Wide Range of Current Control 5-1000mA
- Wide Voltage Range 10-45V
- Designed for Unregulated Motor Supply Voltage
- Current Levels can be Selected in Steps or Varied Continuously
- Thermal Overload Protection

DESCRIPTION

The UC3717 has been designed to control and drive the current in one winding of a bipolar stepper motor. The circuit consists of an LS-TTL-compatible logic input, a current sensor, a monostable and an output stage with built-in protection diodes. Two UC3717s and a few external components form a complete control and drive unit for LS-TTL or micro-processor controlled stepper motor systems.

The UC1717 is characterized for operation over the full military temperature range of -55°C to +125°C, the UC2717 is characterized for -25°C to +85°C, and the UC3717 is characterized for 0°C to +70°C.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage
- Logic Supply, Vcc 7V
- Output Supply, VM 45V

Input Voltage
- Logic Inputs (Pins 7, 8, 9) 6V
- Analog Input (Pin 10) Vcc
- Reference Input (Pin 11) 15V

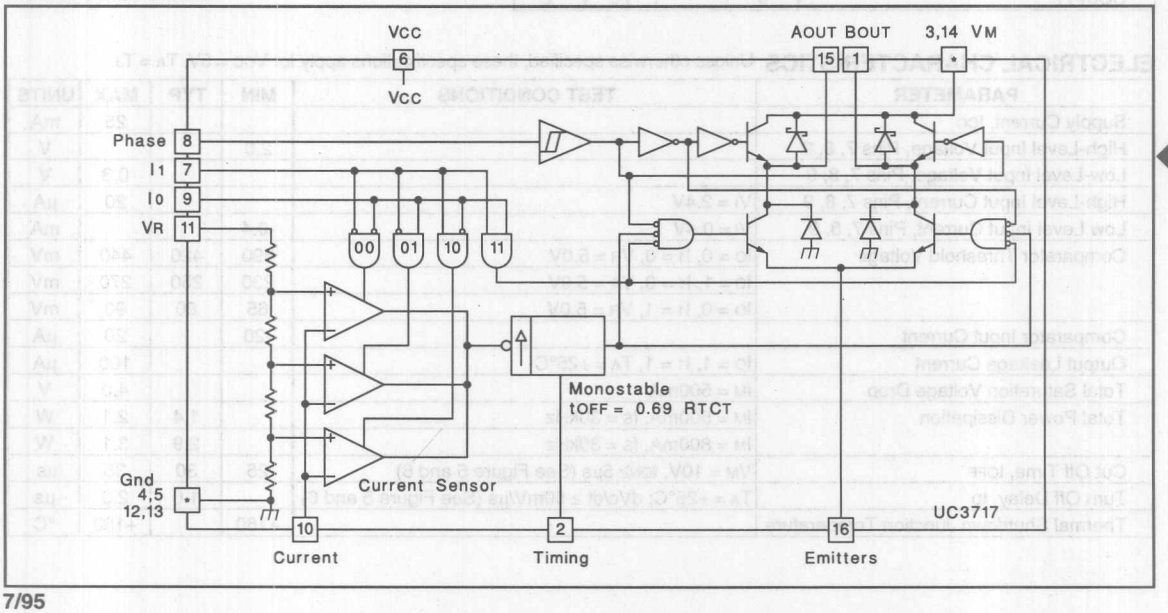
Input Current
- Logic Inputs (Pins 7, 8, 9) ..... -10mA
- Analog Inputs (Pins 10, 11) ..... -10mA

Output Current (Pins 1, 15) ..... ±1A
Junction Temperature, TJ ..... +150°C
Storage Temperature Range, TS ..... -55°C to +150°C

Note 1: All voltages are with respect to ground, Pins 4,5, 12, 13. Pin numbers refer to DIL-16 package. Currents are positive into, negative out of the specified terminal.

Note 2: Consult Packaging Section of Databook for information on thermal limitations and considerations of package.

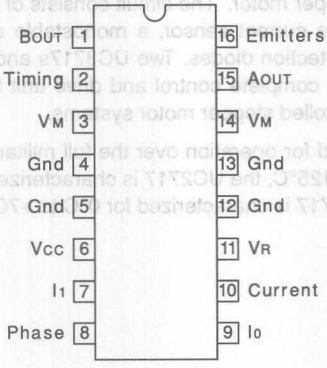
BLOCK DIAGRAM



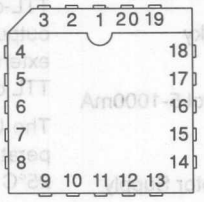
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CONNECTION DIAGRAMS

DIL-16 (TOP VIEW)
J or N Package



PLCC-20 (TOP VIEW)
Q Package



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
BOUT	2
Timing	3
VM	4
Gnd	5
N/C	6
Gnd	7
VCC	8
I1	9
Phase	10
N/C	11
IO	12
Current	13
VR	14
Gnd	15
N/C	16
Gnd	17
Vm	18
AOUT	19
Emitters	20

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	TYP	MAX	UNITS
Supply Voltage, VCC	4.75	5	5.25	V
Supply Voltage, VM	10		40	V
Output Current. IM	20		800	mA
Rise Time Logic Inputs, tR			2	µs
Fall Time Logic Inputs, tF			2	µs
Ambient Temperature, TA				
UC1717	-55		125	°C
UC2717	-25		85	°C
UC3717	0		70	°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, these specifications apply for VCC = 5V, TA = TJ.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current, ICC				25	mA
High-Level Input Voltage, Pins 7, 8, 9		2.0			V
Low-Level Input Voltage, Pins 7, 8, 9				0.8	V
High-Level Input Current, Pins 7, 8, 9	VI = 2.4V			20	µA
Low Level Input Current, Pins 7, 8, 9	VI = 0.4V	-0.4			mA
Comparator Threshold Voltage	IO = 0, I1 = 0, VR = 5.0V	390	420	440	mV
	IO = 1, I1 = 0, VR = 5.0V	230	250	270	mV
	IO = 0, I1 = 1, VR = 5.0V	65	80	90	mV
Comparator Input Current		-20		20	µA
Output Leakage Current	IO = 1, I1 = 1, TA = +25°C			100	µA
Total Saturation Voltage Drop	IM = 500mA			4.0	V
Total Power Dissipation	IM = 500mA, fS = 30kHz		1.4	2.1	W
	IM = 800mA, fS = 30kHz		2.9	3.1	W
Cut Off Time, tOFF	VM = 10V, tON≥ 5µs (See Figure 5 and 6)	25	30	35	µs
Turn Off Delay, tD	TA = +25°C; dVc/dt ≥ 50mV/µs (See Figure 5 and 6)		1.6	2.0	µs
Thermal Shutdown Junction Temperature		+160		+180	°C

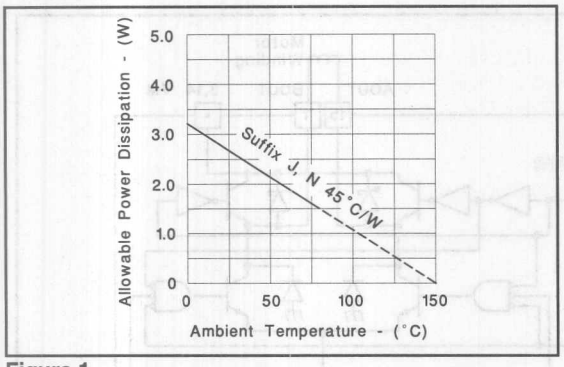


Figure 1

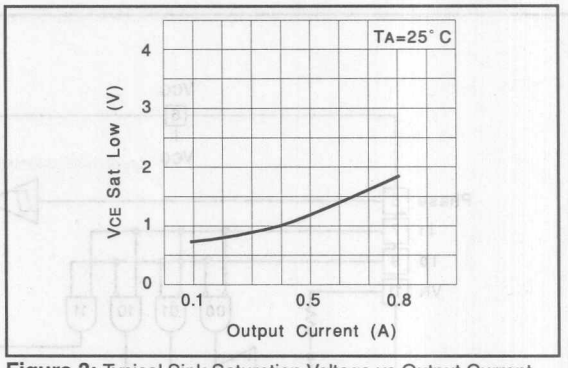


Figure 3: Typical Sink Saturation Voltage vs Output Current

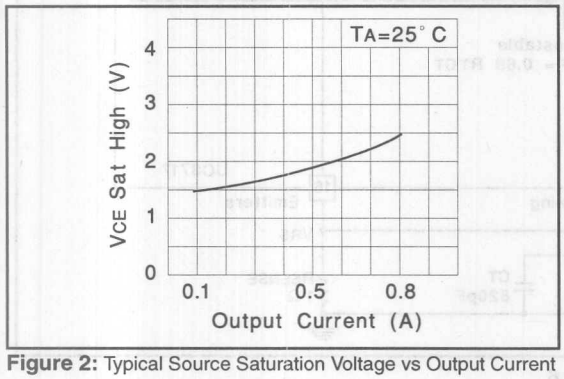


Figure 2: Typical Source Saturation Voltage vs Output Current

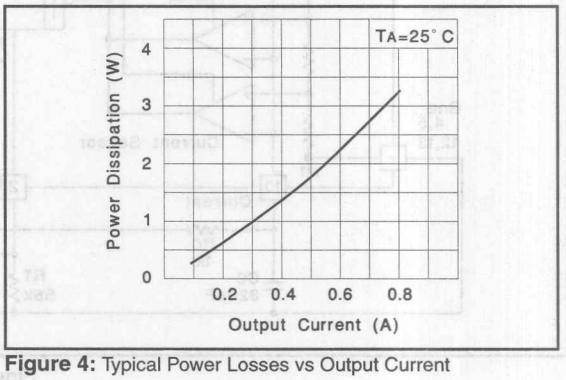


Figure 4: Typical Power Losses vs Output Current

FUNCTIONAL DESCRIPTION

The UC3717 drive circuit shown in the block diagram includes the following functions:

(1) Phase Logic and H-Bridge Output Stage
(2) Voltage Divider with three Comparators for current control
(3) Two Logic inputs for Digital current level select
(4) Monostable for off time generation

Input Logic: If any of the logic inputs are left open, the circuit will treat it as a high level input.

Phase Input: The phase input terminal, pin 18, controls the direction of the current through the motor winding. The Schmidt-Trigger input coupled with a fixed time delay assures noise immunity and eliminates cross conduction in the output stage during phase changes. A low level on the phase input will turn Q2 on and enable Q3 while a high level will turn Q1 on and enable Q4. (See Figure 7).

Output Stage: The output stage consists of four Darlington transistors and associated diodes connected in an H-Bridge configuration. The diodes are needed to provide a current path when the transistors are being switched. For fast recovery, Schottky diodes are used across the source transistors. The Schottky diodes allow the current

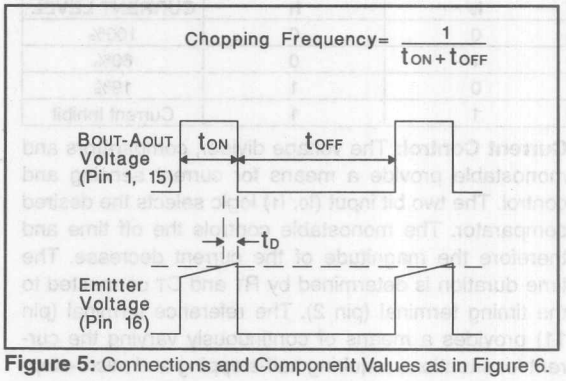


Figure 5: Connections and Component Values as in Figure 6.

to circulate through the winding while the sink transistors are being switched off. The diodes across the sink transistors in conjunction with the Schottkys provide the path for the decaying current during phase reversal. (See Figure 7).

PHASE INPUT	Q1, Q4	Q2, Q3
Low	Off	On
High	On	Off

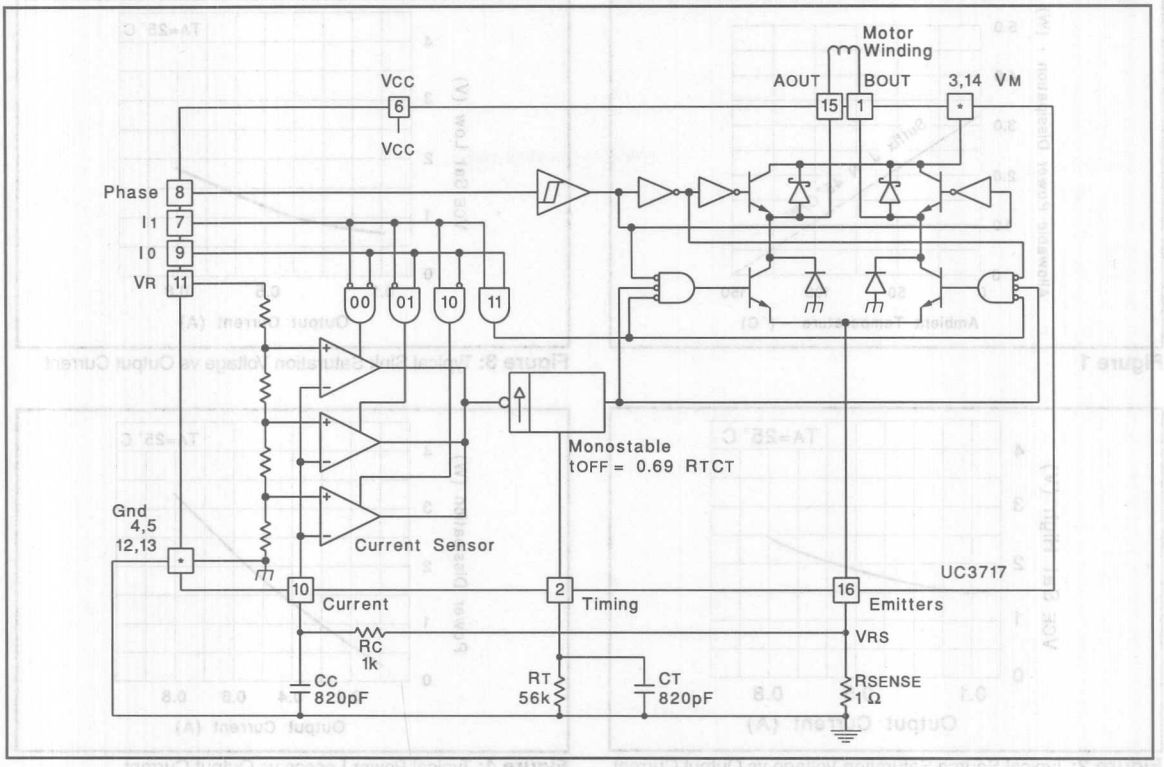


Figure 6

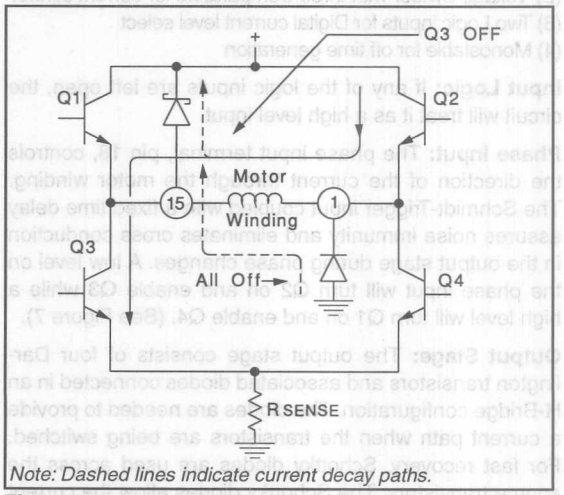
I0	I1	CURRENT LEVEL
0	0	100%
1	0	60%
0	1	19%
1	1	Current Inhibit

Current Control: The voltage divider, comparators and monostable provide a means for current sensing and control. The two bit input (I_0, I_1) logic selects the desired comparator. The monostable controls the off time and therefore the magnitude of the current decrease. The time duration is determined by R_T and C_T connected to the timing terminal (pin 2). The reference terminal (pin 11) provides a means of continuously varying the current for situations requiring half-stepping and micro-stepping. The relationship between the logic input signals at pin 7 and 9 in reference to the current level is shown in Table 1. The values of the different current levels are determined by the reference voltage together with the value of the external sense resistor R_S (pin 16).

Single-Pulse Generator: The pulse generator is a monostable triggered on the positive going edge of the comparator. Its output is high during the pulse time and this pulse switches off the power feed to the motor winding causing the current to decay. The time is determined by the external timing components R_T and C_T as:

$$T_{OFF} = 0.69\ R_T C_T$$

If a new trigger signal should occur during T_{OFF}, it is ignored.



Note: Dashed lines indicate current decay paths.

Figure 7: Simplified Schematic of Output Stage

FUNCTIONAL DESCRIPTION (cont.)

Overload Protection: The circuit is equipped with a thermal shutdown function, which will limit the junction temperature by reducing the output current. It should be noted however, that a short circuit of the output is not permitted.

Operation: When the voltage is applied across the motor winding the current rises linearly and appears across the external sense resistor as an analog voltage. This voltage is fed through a low pass filter Rc, Cc to the voltage comparator (pin 10). At the moment the voltage rises beyond the comparator threshold voltage the monostable is triggered and its output turns off the sink transistors. The current then circulates through the source transistor and the appropriate Schottky diode. After the one shot has timed out, the sink transistsor is turned on again and the procedure repeated until a current reverse command is given. By reversing the logic level of the phase input (pin 8), both active transistors are being turned off and the opposite pair turned on. When this happens the current must first decay to zero before it can reverse. The current path then provided is through the two diodes and the power-supply. Refer to Figure 7. It should be noted at this time that the slope of the current decay is steeper, and this is due to the higher voltage build up across the winding. For better speed performance of the stepping motor at half step mode, the phase logic level should be changed at the same time the current inhibit is applied. A typical current wave form is shown in Figure 8.

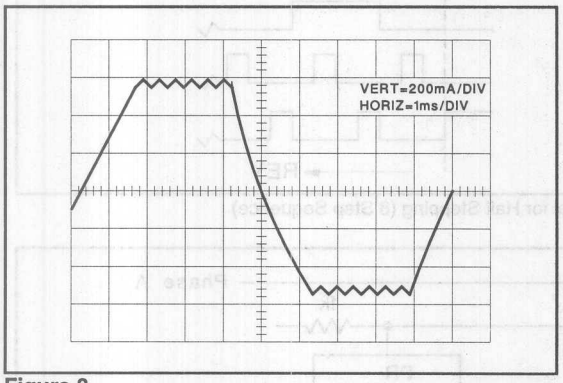


Figure 8

APPLICATIONS

A typical chopper drive for a two phase bipolar permanent magnet or hybrid stepping motor is shown in Figure 9. The input can be controlled by a microprocessor, TTL, LS or CMOS logic.

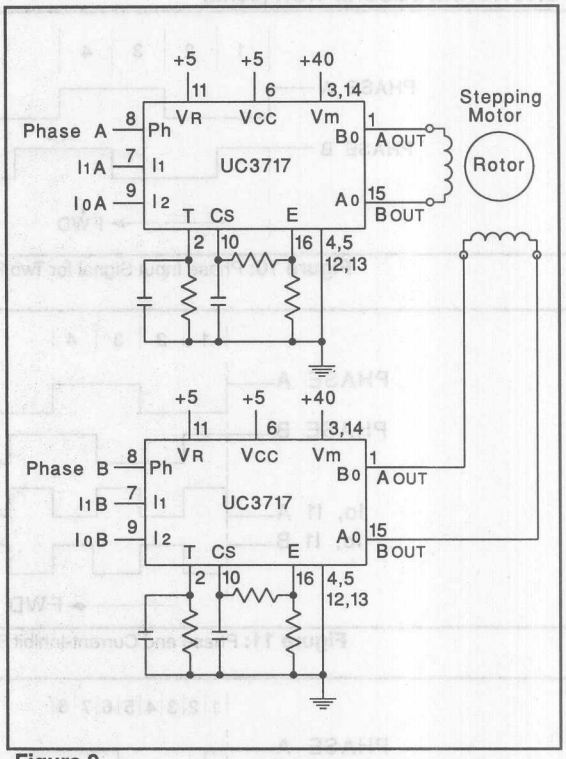


Figure 9

The timing diagram in Figure 10 shows the required signal input for a two phase, full step, stepping sequence. Figure 11 shows a one phase, full step, stepping sequence, commonly referred to as wave drive. Figure 12 shows the required input signal for a one phase-two phase stepping sequence called half-stepping.

The circuit of Figure 13 provides the signal shown in Figure 10, and in conjunction with the circuit shown in Figure 9, will implement a pulse-to-step two phase, full step, bidirectional motor drive.

The schematic of Figure 14 shows a pulse to half step circuit generating the signal shown in Figure 12. Care has been taken to change the phase signal the same time the current inhibit is applied. This will allow the current to decay faster and therefore enhance the motor performance at higher step rates.

Using the UC3717 to drive the L298 provides a uniquely packaged state-of-the-art high power stepper motor control and drive. See Figure 15.

FUNCTIONAL DESCRIPTION (cont.)

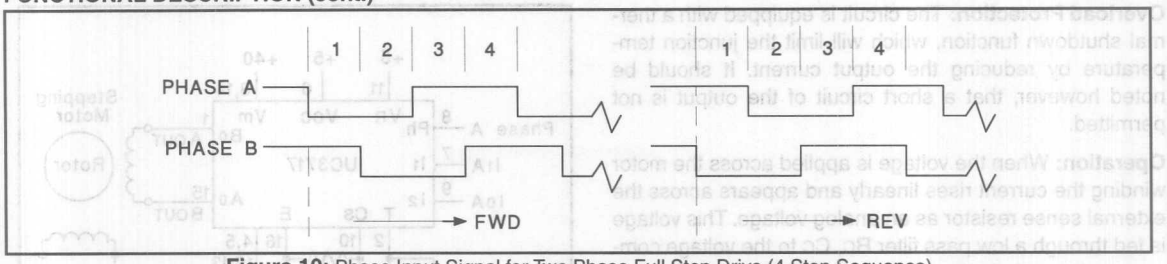


Figure 10: Phase Input Signal for Two Phase Full Step Drive (4 Step Sequence)

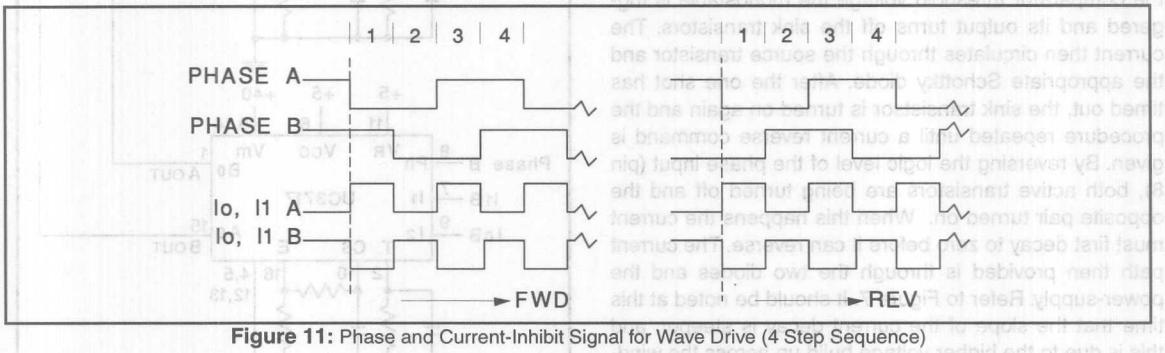


Figure 11: Phase and Current-Inhibit Signal for Wave Drive (4 Step Sequence)

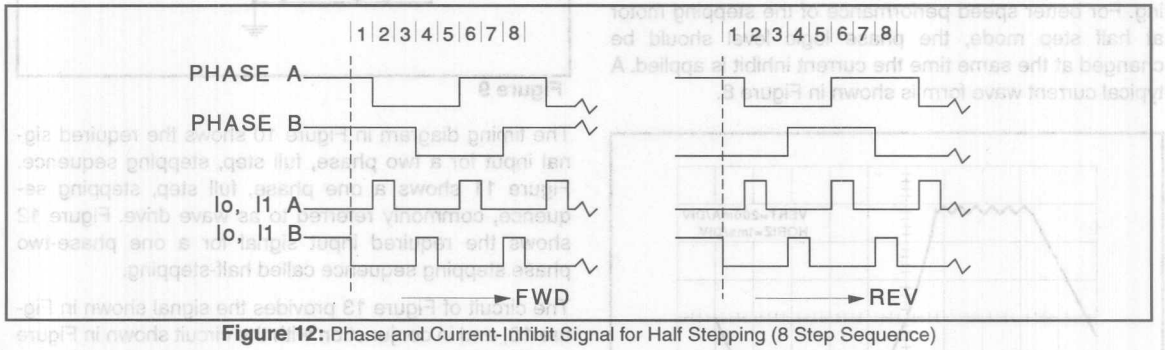


Figure 12: Phase and Current-Inhibit Signal for Half Stepping (8 Step Sequence)

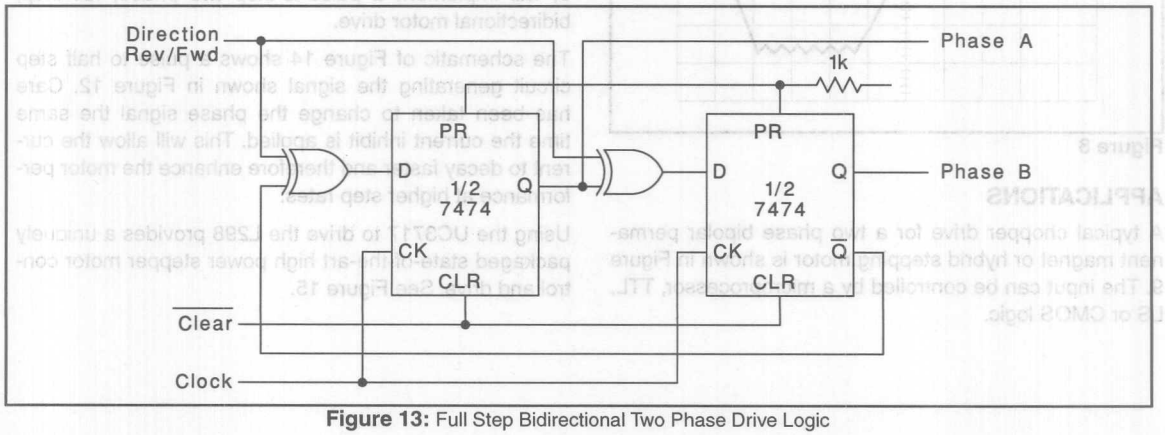


Figure 13: Full Step Bidirectional Two Phase Drive Logic

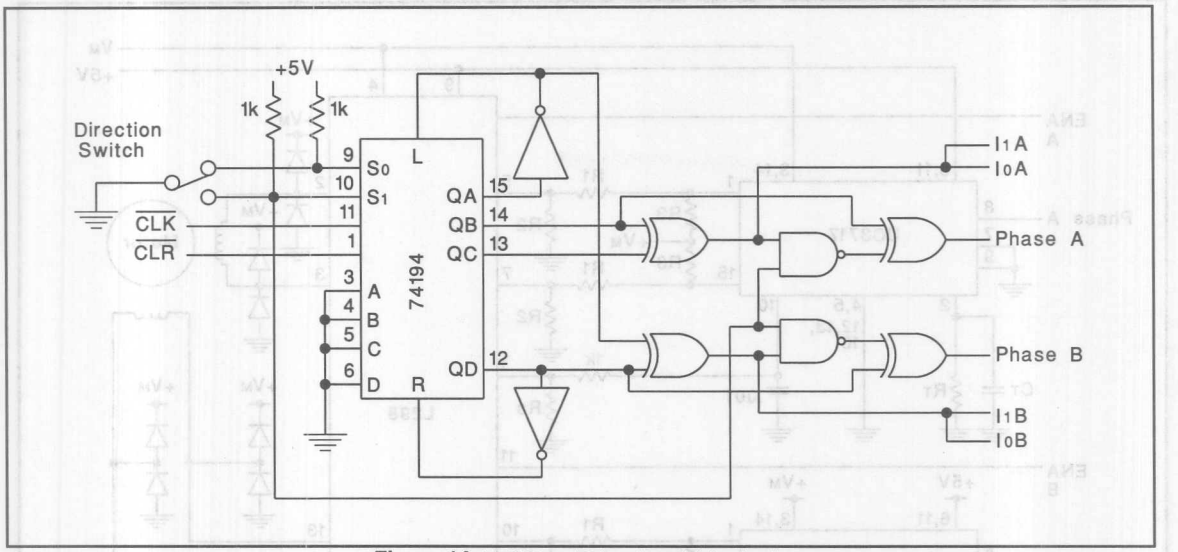


Figure 14: Half-Step, Bidirectional Drive Logic

CONSIDERATION

Half-Stepping: In the half step sequence the power input to the motor alternates between one or two phases being energized. In a two phase motor the electrical phase shift between the windings is 90 degrees. The torque developed is the vector sum of the two windings energized. Therefore when only one winding is energized the torque of the motor is reduced by approximately 30%. This causes a torque ripple and if it is necessary to compensate for this, the V_R input can be used to boost the current of the single energized winding.

Ramping: Every drive system has inertia and must be considered in the drive scheme. The rotor and load inertia plays a big role at higher speeds. Unlike the DC motor the stepping motor is a synchronous motor and does not change its speed due to load variations. Examining typical stepping motors, torque vs. speed curves indicates a sharp torque drop off for the start-stop without error curve, even with a constant current drive. The reason for this is that the torque requirements increase by the square of the speed change, and the power need increases by the cube of the speed change. As it can be seen, for good motor performance controlled acceleration and deceleration should be considered.

Iron Core Losses: Some motors, especially the Tin-Can type, exhibit high iron losses mostly due to eddy currents which rise in an exponential manner as the frequency or step rate is increased. The power losses can not be calculated by I^2R where I is the chopping current level and R the DC resistance of the coil. Actual measurements indicate the effective resistance may be many times larger. Therefore, for 100% duty cycle the current must be limited to a value which will not overheat the motor. This may not be necessary for lower duty cycle operation.

Interference: Electrical noise generated by the chopping action can cause interference problems, particularly in the vicinity of magnetic storage media. With this in mind, printed circuit layouts, wire runs and decoupling must be considered. 0.01 to 0.1µF ceramic capacitors for high frequency bypass located near the drive package across V+ and ground might be very helpful. The connection and ground leads of the current sensing components should be kept as short as possible.

Ordering Information

UNITRODE TYPE NUMBER
UC3717N - 16 Pin Dual-in-line (DIL) "Bat Wing" Package
UC1717J - 16 Pin Dual-in-line Ceramic Package
UC1717SP - 16 Pin Dual-in-line Hermetic Power Package

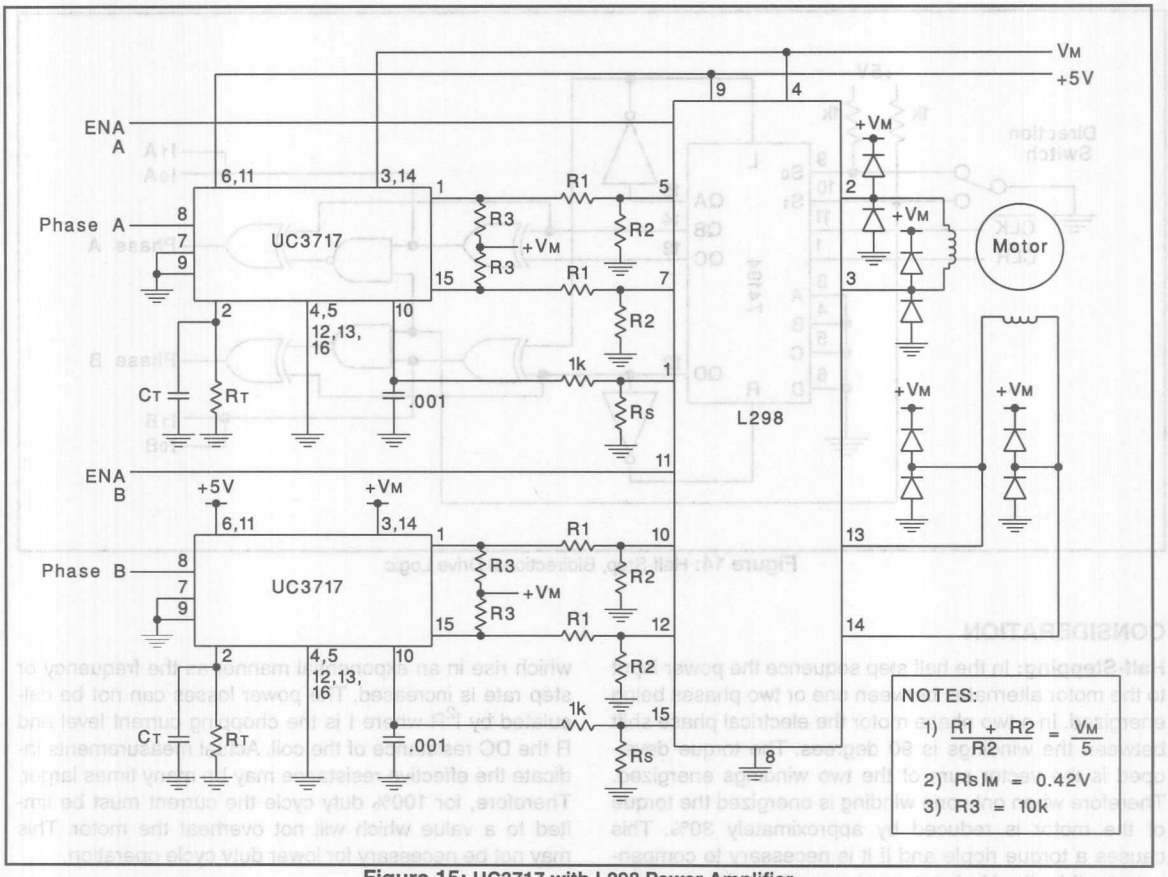


Figure 15: UC3717 with L298 Power Amplifier

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UNITRODE

Stepper Motor Drive Circuit

FEATURES

- Full-Step, Half-Step and Micro-Step Capability
- Bipolar Output Current up to 1A
- Wide Range of Motor Supply Voltage 10-46V
- Low Saturation Voltage with Integrated Bootstrap
- Built-In Fast Recovery Commutating Diodes
- Current Levels Selected in Steps or Varied Continuously
- Thermal Protection with Soft Intervention

DESCRIPTION

The UC3717A is an improved version of the UC3717, used to switch drive the current in one winding of a bipolar stepper motor. The UC3717A has been modified to supply higher winding current, more reliable thermal protection, and improved efficiency by providing integrated bootstrap circuitry to lower recirculation saturation voltages. The diagram shown below presents the building blocks of the UC3717A. Included are an LS-TTL compatible logic input, a current sensor, a monostable, a thermal shutdown network, and an H-bridge output stage. The output stage features built-in fast recovery commutating diodes and integrated bootstrap pull up. Two UC3717As and a few external components form a complete control and drive unit for LS-TTL or micro-processor controlled stepper motor systems.

The UC3717A is characterized for operation over the temperature range of 0°C to +70°C.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage
- Logic Supply, Vcc 7V
- Output Supply, Vm 50V

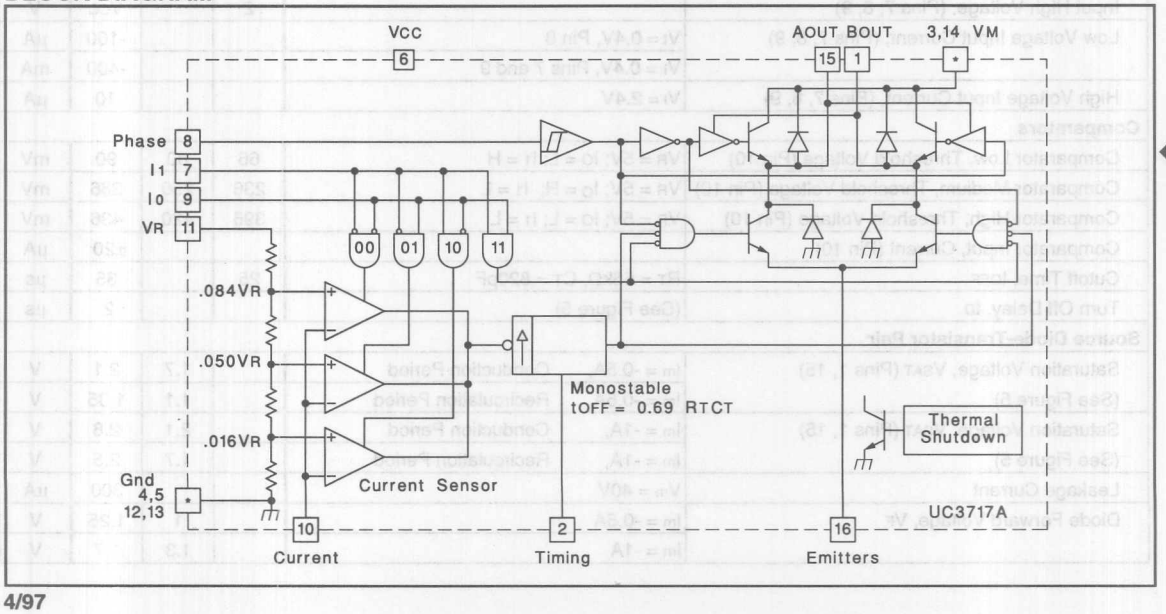
Input Voltage
- Logic Inputs (Pins 7, 8, 9) 6V
- Analog Input (Pin 10) Vcc
- Reference Input (Pin 11) 15V

Input Current
- Logic Inputs (Pins 7, 8, 9) ..... -10mA
- Analog Inputs (Pins 10, 11) ..... -10mA

Output Current (Pins 1, 15) ..... ±1.2A
Junction Temperature, TJ ..... +150°C
Storage Temperature Range, Ts ..... -55°C to +150°C

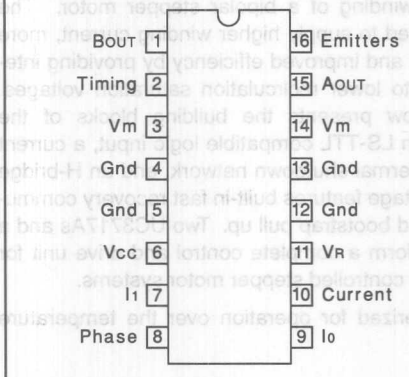
Note 1: All voltages are with respect to ground, Pins 4, 5, 12, 13. Currents are positive into, negative out of the specified terminal. Pin numbers refer to DIL-16 package. Consult Packaging Section of Databook for thermal limitations and considerations of package.

BLOCK DIAGRAM

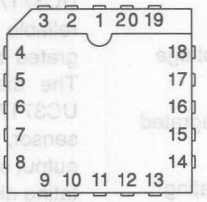


CONNECTION DIAGRAMS

DIL-16 (TOP VIEW)
J or N Package



PLCC-20 (TOP VIEW)
Q Package



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
BOUT	2
Timing	3
Vm	4
Gnd	5
N/C	6
Gnd	7
Vcc	8
I1	9
Phase	10
N/C	11
Io	12
Current	13
VR	14
Gnd	15
N/C	16
Gnd	17
Vm	18
AOUT	19
Emitters	20

ELECTRICAL CHARACTERISTICS

(Refer to the test circuit, Figure 6. V_m = 36V, V_{CC} = 5V, V_R = 5V, T_A = 0°C to 70°C, unless otherwise stated, $T_A = T_J$.)

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage, V_m (Pins 3, 14)		10		46	V
Logic Supply Voltage, V_{CC} (Pin 6)		4.75		5.25	V
Logic Supply Current, I_{CC} (Pin 6)	$I_O = I_1 = 0$		7	15	mA
Thermal Shutdown Temperature		+160		+180	°C
Logic Inputs					
Input Low Voltage, (Pins 7, 8, 9)				0.8	V
Input High Voltage, (Pins 7, 8, 9)		2		V_{CC}	V
Low Voltage Input Current, (Pins 7, 8, 9)	V_I = 0.4V, Pin 8			-100	µA
	V_I = 0.4V, Pins 7 and 9			-400	mA
High Voltage Input Current, (Pins 7, 8, 9)	V_I = 2.4V			10	µA
Comparators					
Comparator Low, Threshold Voltage (Pin 10)	V_R = 5V; I_O = L; I_1 = H	66	80	90	mV
Comparator Medium, Threshold Voltage (Pin 10)	V_R = 5V; I_O = H; I_1 = L	236	250	266	mV
Comparator High, Threshold Voltage (Pin 10)	V_R = 5V; I_O = L; I_1 = L	396	420	436	mV
Comparator Input, Current (Pin 10)				±20	µA
Cutoff Time, t_{OFF}	R_T = 56kΩ, C_T = 820pF	25		35	µs
Turn Off Delay, t_D	(See Figure 5)			2	µs
Source Diode-Transistor Pair					
Saturation Voltage, V_{SAT} (Pins 1, 15)	I_m = -0.5A, Conduction Period		1.7	2.1	V
(See Figure 5)	I_m = -0.5A, Recirculation Period		1.1	1.35	V
Saturation Voltage, V_{SAT} (Pins 1, 15)	I_m = -1A, Conduction Period		2.1	2.8	V
(See Figure 5)	I_m = -1A, Recirculation Period		1.7	2.5	V
Leakage Current	V_m = 40V			300	µA
Diode Forward Voltage, V_F	I_m = -0.5A		1	1.25	V
	I_m = -1A		1.3	1.7	V

ELECTRICAL CHARACTERISTICS (cont.)

(Refer to the test circuit, Figure 6. V_M = 36V, V_{CC} = 5V, V_R = 5V, T_A = 0°C to 70°C, unless otherwise stated, T_A = T_J.)

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Sink Diode-Transistor Pair					
Saturation Voltage, V_{SAT} (Pins 1, 15)	I_M = 0.5A	0.8	1.1	1.35	V
	I_M = 1A		1.6	2.3	V
Leakage Current	V_M = 40V			300	µA
Diode Forward Voltage, V_F	I_M = 0.5A		1.1	1.5	V
	I_M = 1A		1.4	2	V

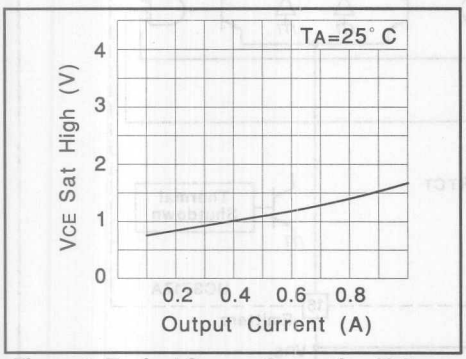


Figure 1. Typical Source Saturation Voltage vs Output Current (Recirculation Period)

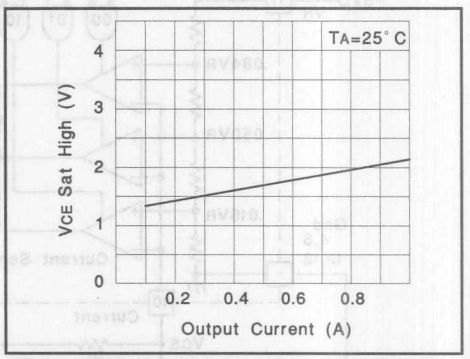


Figure 2. Typical Source Saturation Voltage vs Output Current (Conduction Period)

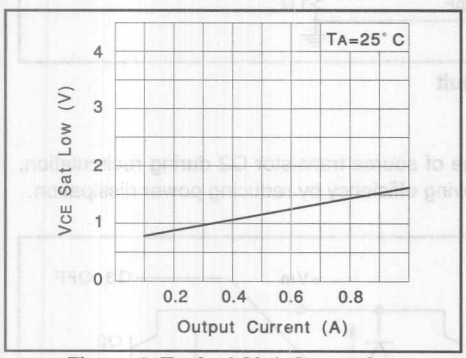


Figure 3. Typical Sink Saturation Voltage vs Output Current

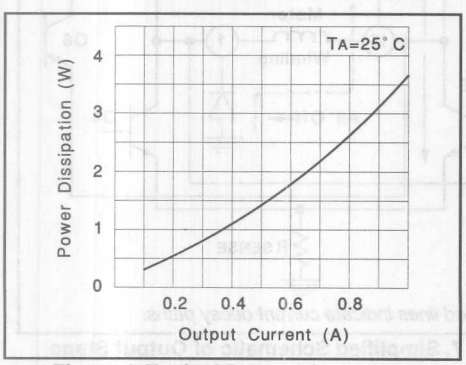


Figure 4. Typical Power Dissipation vs Output Current

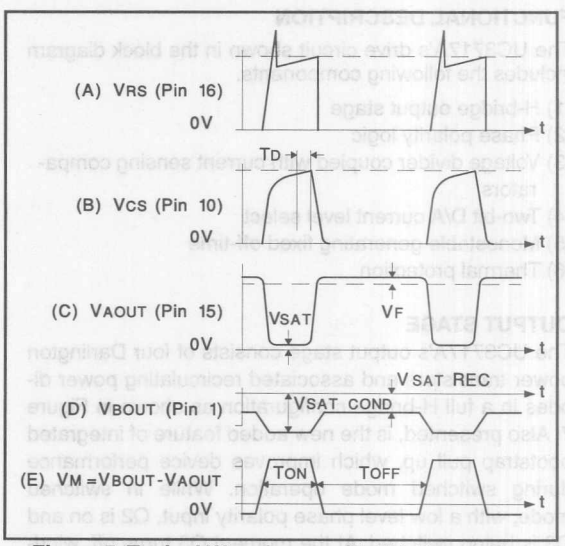


Figure 5. Typical Waveforms with MA Regulating (phase = 0)

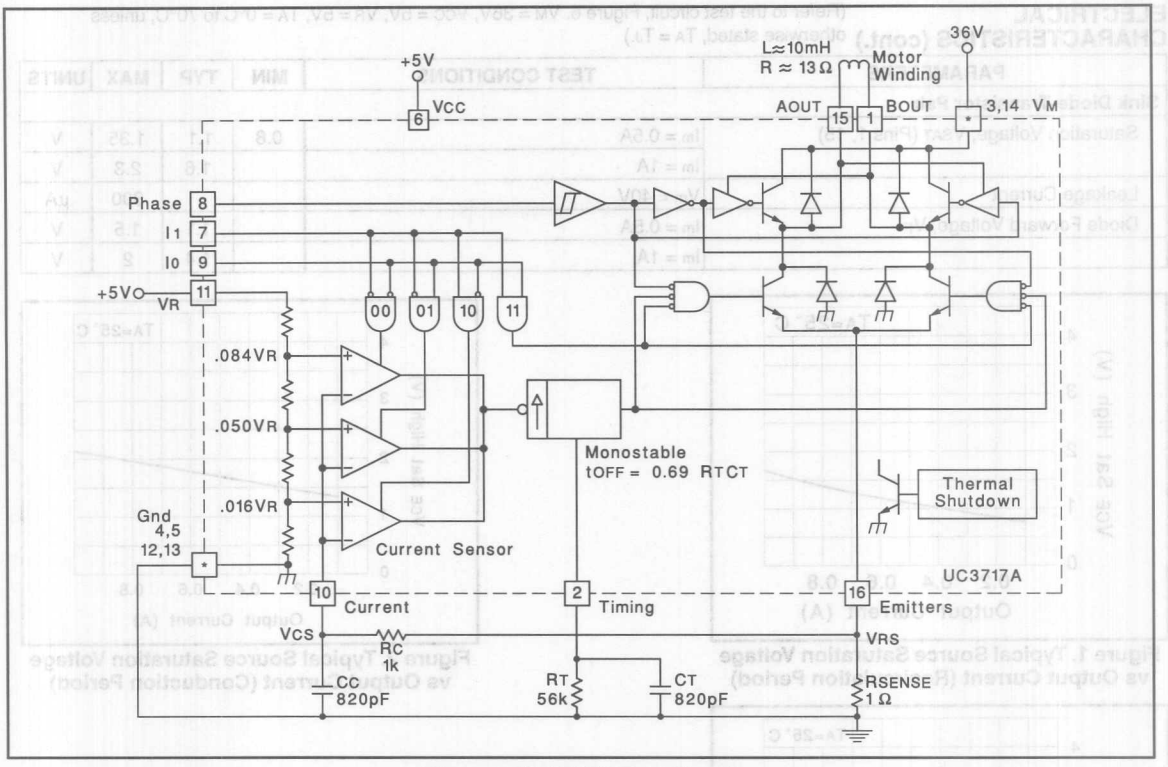


Figure 6. UC3717A Test Circuit

FUNCTIONAL DESCRIPTION

The UC3717A's drive circuit shown in the block diagram includes the following components.

(1) H-bridge output stage
(2) Phase polarity logic
(3) Voltage divider coupled with current sensing comparators
(4) Two-bit D/A current level select
(5) Monostable generating fixed off-time
(6) Thermal protection

OUTPUT STAGE

The UC3717A's output stage consists of four Darlington power transistors and associated recirculating power diodes in a full H-bridge configuration as shown in Figure 7. Also presented, is the new added feature of integrated bootstrap pull up, which improves device performance during switched mode operation. While in switched mode, with a low level phase polarity input, Q2 is on and Q3 is being switched. At the moment Q3 turns off, winding current begins to decay through the commutating diode pulling the collector of Q3 above the supply voltage. Meanwhile, Q6 turns on pulling the base of Q2 higher than its previous value. The net effect lowers the saturation voltage of source transistor Q2 during recirculation, thus improving efficiency by reducing power dissipation.

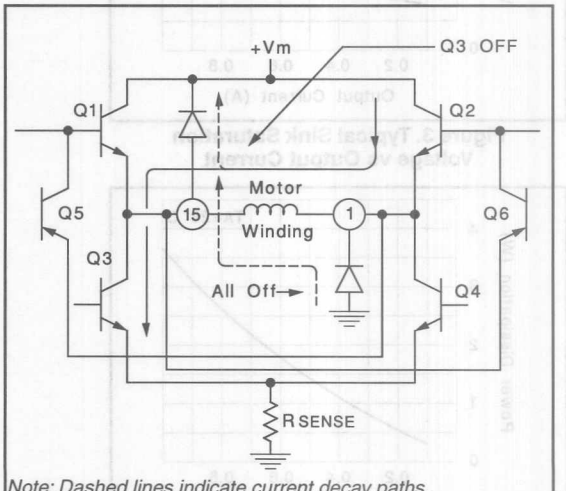


Figure 7. Simplified Schematic of Output Stage

FUNCTIONAL DESCRIPTION (cont.)

PHASE POLARITY INPUT

The UC3717A phase polarity input controls current direction in the motor winding. Built-in hysteresis insures immunity to noise, something frequently present in switched drive environments. A low level phase polarity input enables Q2 and Q3 as shown in Figure 7. During phase reversal, the active transistors are both turned off while winding current delays through the commutating diodes shown. As winding current decays to zero, the inactive transistors Q1 and Q4 turn on and charge the winding with current of the reverse direction. This delay insures noise immunity and freedom from power supply current spikes caused by overlapping drive signals.

PHASE INPUT	Q1, Q4	Q2, Q3
LOW	OFF	ON
HIGH	ON	OFF

CURRENT CONTROL

The voltage divider, comparators, monostable, and two-bit D/A provide a means to sense winding peak current, select winding peak current, and disable the winding sink transistors.

The UC3717A switched driver accomplishes current control using an algorithm referred to as "fixed off-time." When a voltage is applied across the motor winding, the current through the winding increases exponentially. The current can be sensed across an external resistor as an analog voltage proportional to instantaneous current. This voltage is normally filtered with a simple RC low-pass network to remove high frequency transients, and then compared to one of the three selectable thresholds. The two bit D/A input signal determines which one of the three thresholds is selected, corresponding to a desired winding peak current level. At the moment the sense voltage rises above the selected threshold, the UC3717A's monostable is triggered and disables both output sink drivers for a fixed off-time. The winding current then circulates through the source transistor and appropriate diode. The reference terminal of the UC3717A provides a means of continuously adjusting the current threshold to allow microstepping. Table 1 presents the relationship between the two-bit D/A input signal and selectable current level.

TABLE 1

I_0	I_1	CURRENT LEVEL
0	0	100%
1	0	60%
0	1	19%
1	1	Current Inhibit

OVERLOAD PROTECTION

The UC3717A is equipped with a new, more reliable thermal shutdown circuit which limits the junction temperature to a maximum of 180C by reducing the winding current.

PERFORMANCE CONSIDERATIONS

In order to achieve optimum performance from the UC3717A careful attention should be given to the following items.

External Components: The UC3717A requires a minimal number of external components to form a complete control and switch drive unit. However, proper selection of external components is necessary for optimum performance. The timing pin, (pin 2) is normally connected to an RC network which sets the off-time for the sink power transistor during switched mode. As shown in Figure 8, prior to switched mode, the winding current increases exponentially to a peak value. Once peak current is attained the monostable is triggered which turns off the lower sink drivers for a fixed off-time. During off-time winding current decays through the appropriate diode and source transistor. The moment off-time times out, the motor current again rises exponentially producing the ripple waveform shown. The magnitude of winding ripple is a direct function of off-time. For a given off-time T_{OFF}, the values of R_T and C_T can be calculated from the expression:

$$T_{OFF} = 0.69 R_T C_T$$

with the restriction that R_T should be in the range of 10-100k. As shown in Figure 5, the switch frequency F_S is a function of T_{OFF} and T_{ON}. Since T_{ON} is a function of the reference voltage, sense resistor, motor supply, and winding electrical characteristics, it generally varies during different modes of operation. Thus, F_S may be approximated nominally as:

$$F_S = 1/1.5\ (T_{OFF}).$$

Normally, Switch Frequency Is Selected Greater than 20kHz to prevent audible noise, and lower than 100kHz to limit power consumed during the switching cycle.

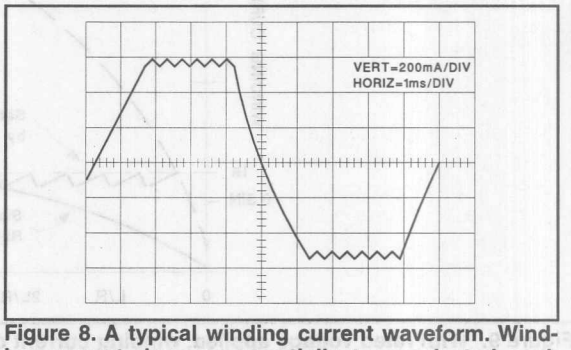


Figure 8. A typical winding current waveform. Winding current rises exponentially to a selected peak value. The peak value is limited by switched mode operation producing a ripple in winding current. A phase polarity reversal command is given and winding current decays to zero, then increases exponentially.

FUNCTIONAL DESCRIPTION (cont.)

Low-pass filter components Rc Cc should be selected so that all switching transients from the power transistors and commutating diodes are well smoothed, but the primary signal, which can be in the range of 1/TOFF or higher must be passed. Figure 5A shows the waveform which must be smoothed, Figure 5B presents the desired waveform that just smoothes out overshoot without radical distortion.

The sense resistor should be chosen as small as practical to allow as much of the winding supply voltage to be used as overdrive to the motor winding. V_{RS}, the voltage across the sense resistor, should not exceed 1.5V.

Voltage Overdrive: In many applications, maximum speed or step rate is a desirable performance characteristic. Maximum step rate is a direct function of the time necessary to reverse winding current with each step. In response to a constant motor supply voltage, the winding current changes exponentially with time, whose shape is determined by the winding time constant and expressed as:

$$I_m = \frac{V_m}{R\,[1-EXP\,(-R T/L)]}$$

as presented in Figure 9. With rated voltage applied, the time required to reach rated current is excessive when compared with the time required with over-voltage applied, even though the time constant L/R remains constant. With over-voltage however, the final value of current is excessive and must be prevented. This is accomplished with switch drive by repetitively switching the sink drivers on and off, so as to maintain an average value of current equal to the rated value. This results in a small amount of ripple in the controlled current, but the increase in step rate and performance may be considerable.

Interference: Electrical noise generated by the chopping action can cause interference problems, particularly in the vicinity of magnetic storage media. With this in mind, printed circuit layouts, wire runs and decoupling must be considered. 0.01 to 0.1µF ceramic capacitors for high frequency bypass located near the drive package across V+ and ground might be very helpful. The connection and ground leads of the current sensing components should be kept as short as possible.

Half-Stepping: In half step sequence the power input to the motor alternates between one or two phases being energized. In a two phase motor the electrical phase shift between the windings is 90°. The torque developed is the vector sum of the two windings energized. Therefore when only one winding is energized the torque of the motor is reduced by approximately 30%. This causes a torque ripple and if it is necessary to compensate for this, the V_R input can be used to boost the current of the single energized winding.

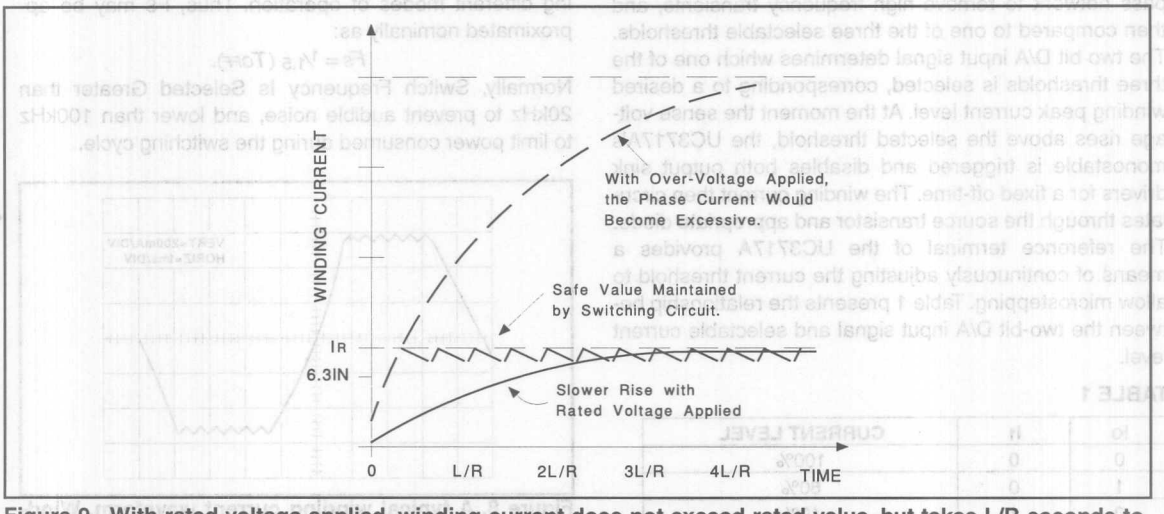


Figure 9. With rated voltage applied, winding current does not exceed rated value, but takes L/R seconds to reach 63% of its final value - probably too long. Increased performance requires an increase in applied voltage, of overdrive, and therefore a means to limit current. The UC3717A motor driver performs this task efficiently.

MOUNTING INSTRUCTIONS

The θJA of the UC3717AN plastic package can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board or to an external heat sink. Due to different lead frame design, θJA of the ceramic J package cannot be similarly reduced.

The diagram of Figure 11 shows the maximum package power PTOT and the θJA as a function of the side " l " of two equal square copper areas having a thickness of 35µ (see Figure 10).

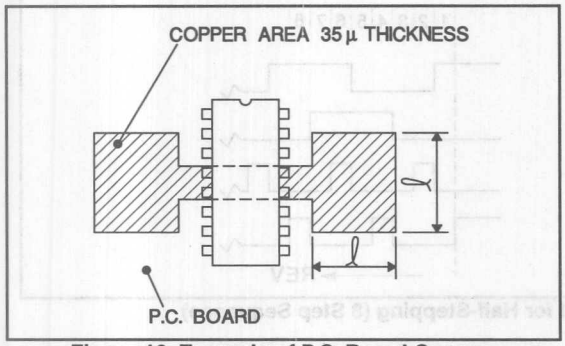


Figure 10. Example of P.C. Board Copper Area which is used as Heatsink.

During soldering the pins' temperature must not exceed 260°C and the soldering time must not be longer than 12 seconds.

The printed circuit copper area must be connected to electrical ground.

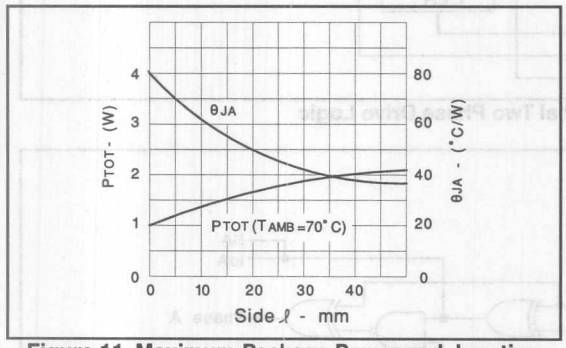


Figure 11. Maximum Package Power and Junction to Ambient Thermal Resistance vs Side "l".

APPLICATIONS

A typical chopper drive for a two phase bipolar permanent magnet or hybrid stepping motor is shown in Figure 12. The input can be controlled by a microprocessor, TTL, LS, or CMOS logic.

The timing diagram in Figure 13 shows the required signal input for a two phase, full step stepping sequence. Figure 14 shows the required input signal for a one phase-two phase stepping sequence called half-stepping.

The circuit of Figure 15 provides the signal shown in Figure 13, and in conjunction with the circuit shown in Figure 12 will implement a pulse-to-step two phase, full step, bi-directional motor drive.

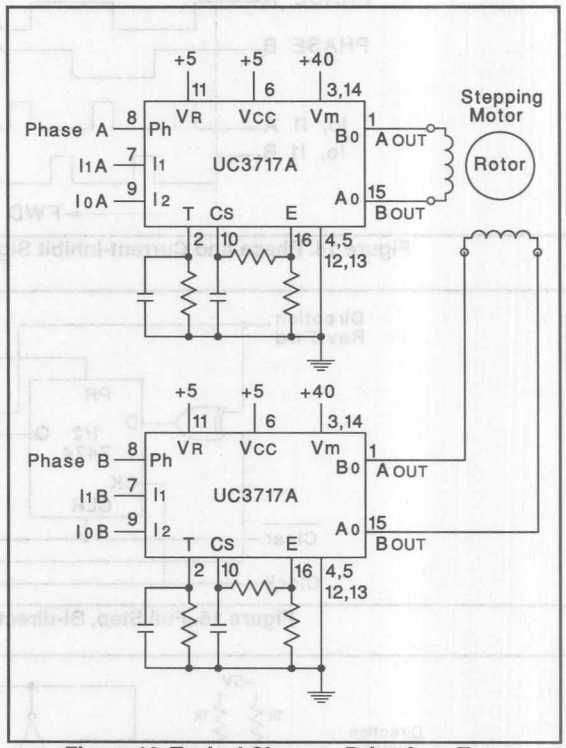


Figure 12. Typical Chopper Drive for a Two Phase Permanent Magnet Motor.

The schematic of Figure 16 shows a pulse to half step circuit generating the signal shown in Figure 14. Care has been taken to change the phase signal the same time the current inhibit is applied. This will allow the current to decay faster and therefore enhance the motor performance at high step rates.

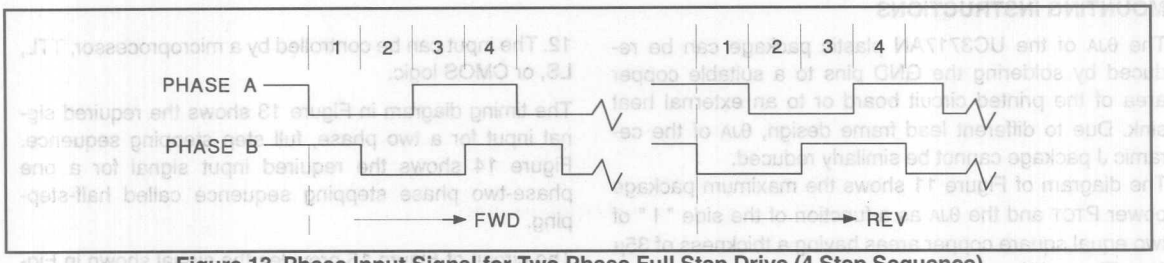


Figure 13. Phase Input Signal for Two Phase Full Step Drive (4 Step Sequence)

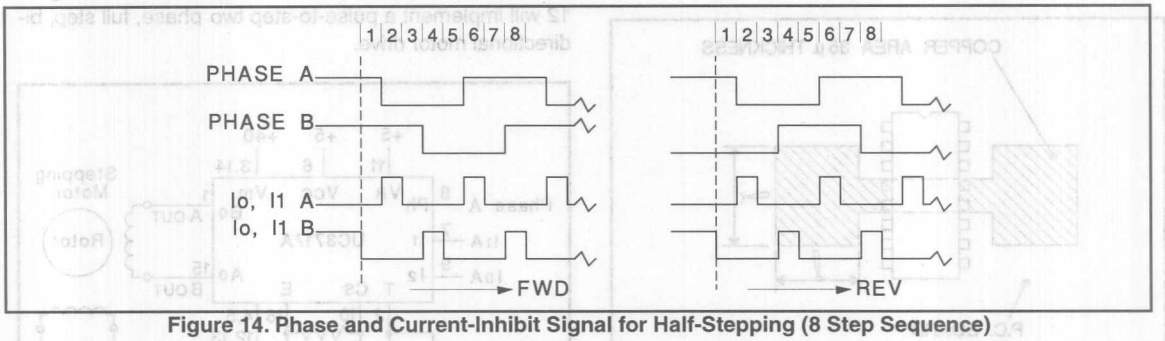


Figure 14. Phase and Current-Inhibit Signal for Half-Stepping (8 Step Sequence)

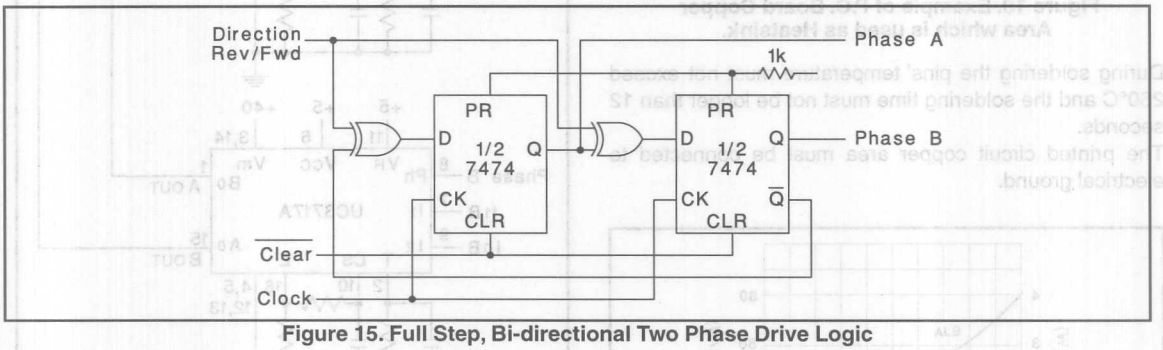


Figure 15. Full Step, Bi-directional Two Phase Drive Logic

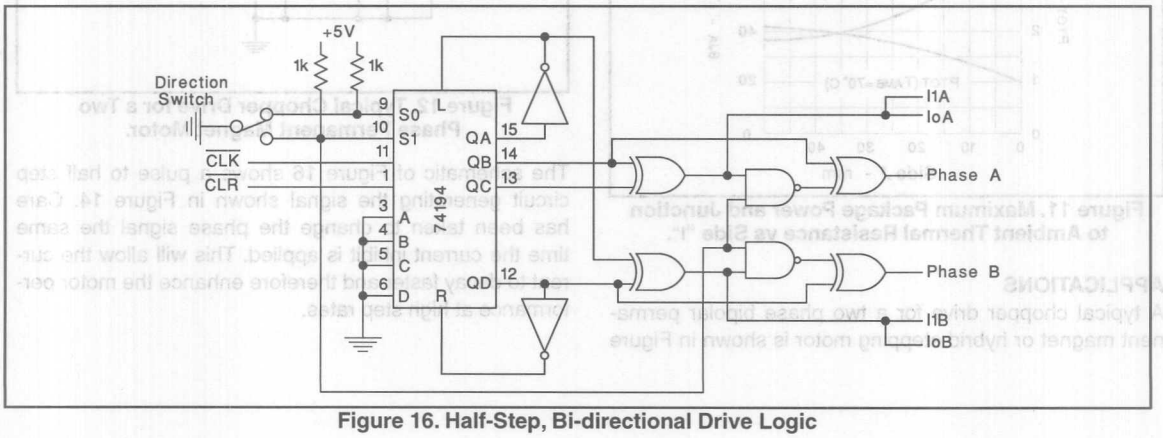


Figure 16. Half-Step, Bi-directional Drive Logic

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- Wide Range of Current Control: 5mA–2A.
- Current Levels Selected in Steps or Varied Continuously.
- Thermal Protection and Soft Intervention.

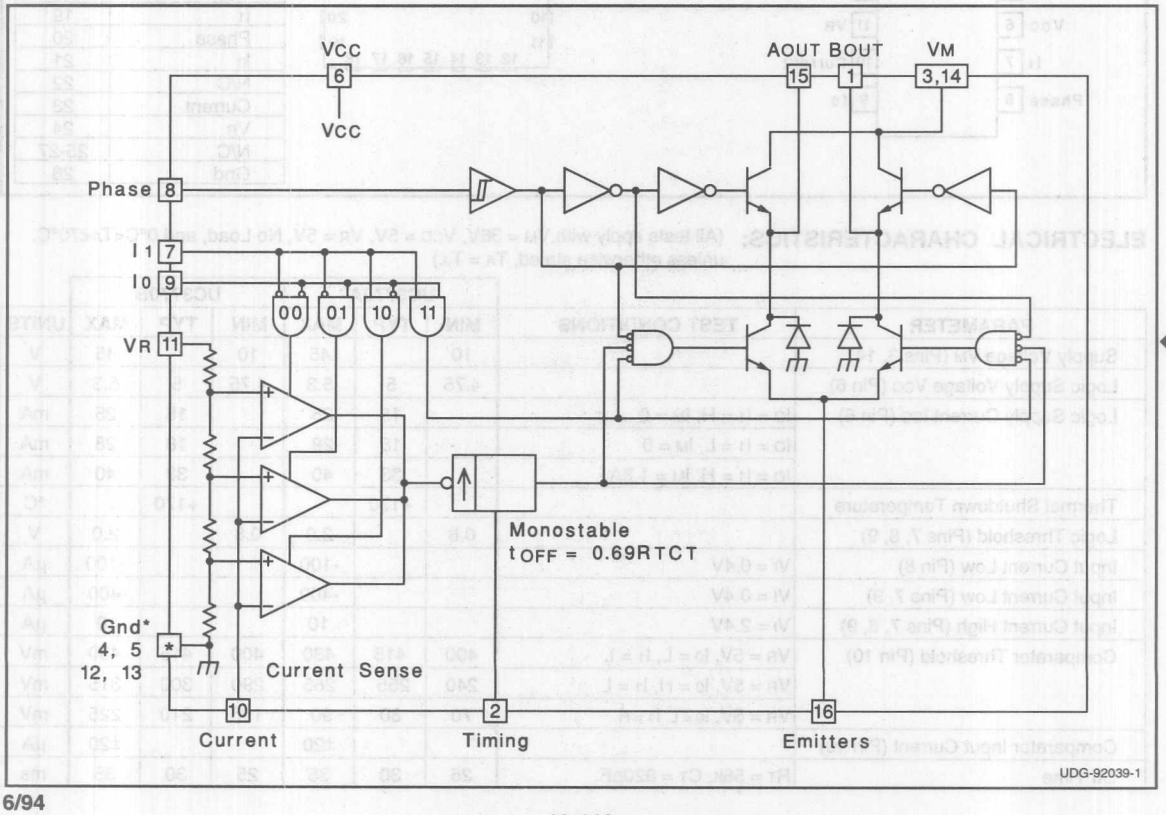
DESCRIPTION

The UC3770A and UC3770B are high-performance full bridge drivers that offer higher current and lower saturation voltage than the UC3717 and the UC3770. Included in these devices are LS-TTL compatible logic inputs, current sense, monostable, thermal shutdown, and a power H-bridge output stage. Two UC3770As or UC3770Bs and a few external components form a complete microprocessor-controllable stepper motor power system.

Unlike the UC3717, the UC3770A and the UC3770B require external high-side clamp diodes. The UC3770A and UC3770B are identical in all regards except for the current sense thresholds. Thresholds for the UC3770A are identical to those of the older UC3717 permitting drop-in replacement in applications where high-side diodes are not required. Thresholds for the UC3770B are tailored for half stepping applications where 50%, 71%, and 100% current levels are desirable.

The UC3770A and UC3770B are specified for operation from 0°C to 70°C ambient.

BLOCK DIAGRAM



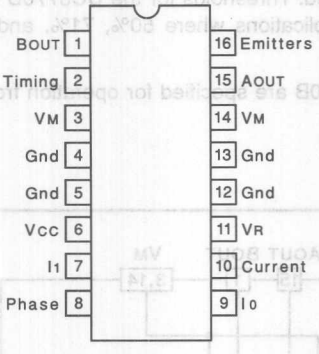
ABSOLUTE MAXIMUM RATINGS

Logic Supply Voltage, V_{CC} 7V
Output Supply Voltage, V_{MM} 50V
Logic Input Voltage (Pins 7, 8, 9) 6V
Analog Input Voltage (Pin 10) ..... V_{CC}
Reference Input Voltage (Pin 11) 15V
Logic Input Current (Pins 7, 8, 9) ..... -10mA
Analog Input Current (Pins 10, 11) ..... -10mA
Output Current (Pins 1, 15) ..... ±2A
Junction Temperature, T_J ..... +150°C

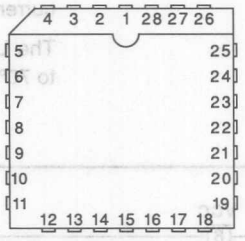
Note 1: All voltages are with respect to Gnd (DIL Pins 4, 5, 12, 13); all currents are positive into, negative out of the specified terminal.
Note 2: Consult Unitrode Integrated Circuits databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAMS

DIL-16 (Top View)
J Or N Package



PLCC-28 (Top View)
Q Package



PACKAGE PIN FUNCTION	
FUNCTION	PIN
Gnd	1-3
V_M	4
N/C	5
A_{OUT}	6
N/C	7
Emitters	8
Gnd	9
B_{OUT}	10
Timing	11
V_M	12
Gnd	13-17
V_{CC}	18
I_1	19
Phase	20
I_O	21
N/C	22
Current	23
V_R	24
N/C	25-27
Gnd	28

ELECTRICAL CHARACTERISTICS:

(All tests apply with V_M = 36V, V_{CC} = 5V, V_R = 5V, No Load, and 0°C<T_A<70°C, unless otherwise stated, T_A = T_J.)

		UC3770A			UC3770B			
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Supply Voltage V_M (Pins 3, 14)		10		45	10		45	V
Logic Supply Voltage V_{CC} (Pin 6)		4.75	5	5.3	4.75	5	5.3	V
Logic Supply Current I_{CC} (Pin 6)	I_O = I_1 = H, I_M = 0		15	25		15	25	mA
	I_O = I_1 = L, I_M = 0		18	28		18	28	mA
	I_O = I_1 = H, I_M = 1.3A		33	40		33	40	mA
Thermal Shutdown Temperature			+170			+170		°C
Logic Threshold (Pins 7, 8, 9)		0.8		2.0	0.8		2.0	V
Input Current Low (Pin 8)	V_I = 0.4V			-100			-100	µA
Input Current Low (Pins 7, 9)	V_I = 0.4V			-400			-400	µA
Input Current High (Pins 7, 8, 9)	V_I = 2.4V			10			10	µA
Comparator Threshold (Pin 10)	V_R = 5V, I_O = L, I_1 = L	400	415	430	400	415	430	mV
	V_R = 5V, I_O = H, I_1 = L	240	255	265	290	300	315	mV
	V_R = 5V, I_O = L, I_1 = H	70	80	90	195	210	225	mV
Comparator Input Current (Pin 10)				±20			±20	µA
Off Time	R_T = 56k, C_T = 820pF	25	30	35	25	30	35	ms

ELECTRICAL CHARACTERISTICS (cont.): (All tests apply with V_M = 36V, V_{CC} = 5V, V_R = 5V, No Load, and 0°C<T_A<70°C, unless otherwise stated, T_A = T_J.)

PARAMETER	TEST CONDITIONS	UC3770A MIN	UC3770A TYP	UC3770A MAX	UC3770B MIN	UC3770B TYP	UC3770B MAX	UNITS
Turn Off Delay				2			2	ms
Sink Driver Saturation Voltage	I_M = 1.0A			0.8			0.8	V
	I_M = 1.3A			1.3			1.3	V
Source Driver Saturation Voltage	I_M = 1.0A			1.3			1.3	V
	I_M = 1.3A			1.6			1.6	V
Output Leakage Current	V_M = 45V			100			100	µA

Figure 1: Typical Source Saturation Voltages vs. Load Current

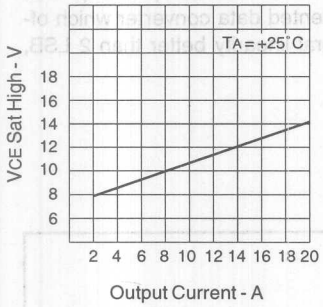


Figure 2: Typical Sink Saturation Voltages vs. Load Current

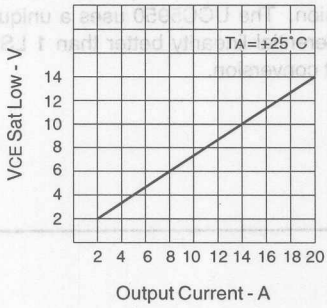
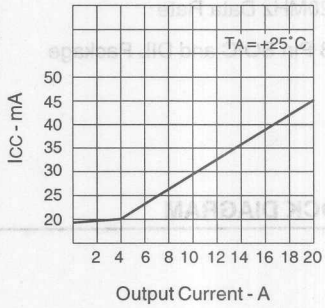


Figure 3: Typical Supply Current vs. Load Current



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FEATURES

- 10 Bit Resolution
- 1.1µs Output Rise Time
- 2.5µs Settling Time to 1%
- Single +5V Supply
- Monotonic
- Low Power Sleep Mode
- Three-wire Serial Interface
- 20MHz Data Rate
- 8 Pin SOIC and DIL Package

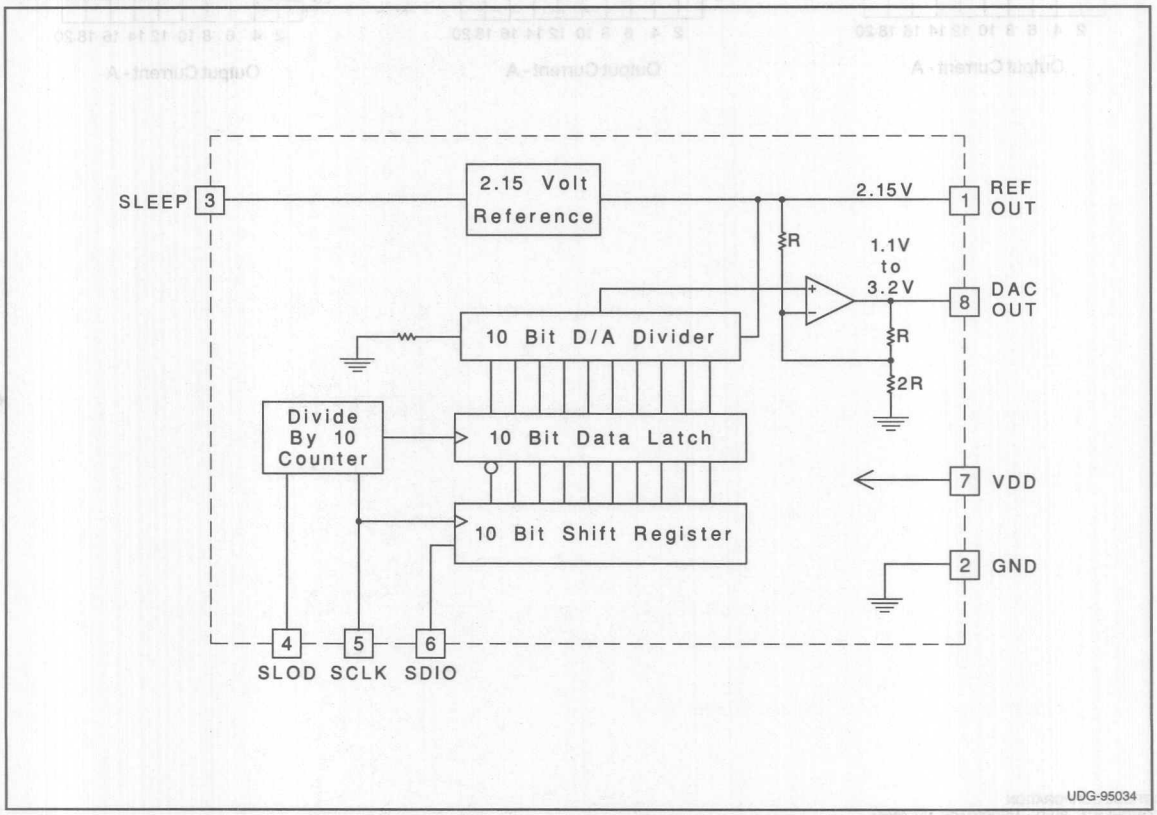
DESCRIPTION

The UCC5950 is a self-contained, microprocessor-compatible 10-bit D/A converter. It contains all of the functions required to take data directly from a three-wire serial data bus and convert it to a precise voltage, including: an input shift register, data latches, a precision voltage reference, a precision 10-bit digital to analog converter, and an output buffer amplifier.

The serial data interface is capable of clock frequencies as high as 20MHz, allowing update rates as high as two words per microsecond. The UCC5950 accepts commands encoded as 2's-complement binary.

The data converter in the UCC5950 is inherently monotonic, making this part ideal for use in closed-loop servo control systems as well as open-loop data conversion. The UCC5950 uses a unique segmented data converter which offers differential linearity better than 1 LSB, integral linearity better than 2 LSB, and fast conversion.

BLOCK DIAGRAM



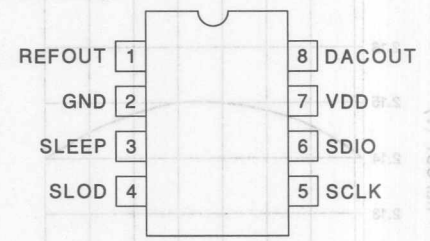
ABSOLUTE MAXIMUM RATINGS

VDD Supply Voltage 6.5V
Input Voltage, Any Input ..... –0.3V to VDD+0.3V
Output Current, Any Output ..... ±5mA
Operating Temperature ..... –55°C to +150°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature ..... 300°C

All voltages with respect to GND. All currents are positive into, negative out of, the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

DIL-8, SOIC-8 (Top View)
N or J, D Package



ELECTRICAL CHARACTERISTICS

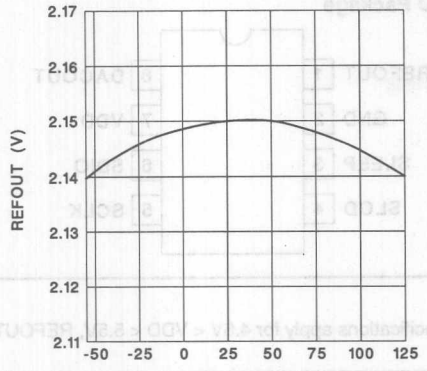
Unless otherwise stated, all specifications apply for 4.5V < VDD < 5.5V, REFOUT Load < 100pF, DACOUT Load < 100pF, 0°C < TA < +70°C, and TA = TJ.

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
OVERALL SECTION					
Supply Current	SLEEP = 0V		1.5	5	mA
Supply Current	SLEEP = 5V		0.1	10	µA
REFERENCE SECTION					
REFOUT Output Voltage		2.10	2.15	2.20	V
REFOUT Change with VDD	4.5V < VDD < 5.5V		1	10	mV
REFOUT Change with Load	–1mA < IREFOUT < 1mA		1	10	mV
D/A SECTION					
Integral Nonlinearity	(Note 1)			2	LSB
Differential Nonlinearity				1	LSB
Full Scale Difference from 1.4924 x REF		–8		8	LSB
Zero Scale Difference from 0.5089 x REF		–8		8	LSB
DACOUT Full Scale Rise/Fall Time	From 10% to 90% of swing (Note 4)		0.7	1.1	µs
DACOUT Full Scale Settling Time (TS)	(Note 2, 3, 4)		1.4	2.5	µs
DACOUT Change with VDD	4.5V < VDD < 5.5V		1.5	10	mV
DACOUT Change with Load	–1mA < IDACOUT < 1mA		1.2	10	mV
LOGIC SECTION					
Logic Input Threshold		1.5	2.5	3.5	V
Logic Input Current	0V < VIN < VDD			5	µA
Logic Input Capacitance	(Note 4)		2.7	10	pF
SLOD Setup Time to SCLK low (TSLS)	(Note 4)	50			ns
SLOD Hold Time from SCLK high (TSLH)	From 10TH SCLK high (Note 4)	50			ns
SDIO Setup Time to SCLK high (TDS)	(Note 4)	15			ns
SDIO Hold Time from SCLK high (TDH)	(Note 4)	7			ns

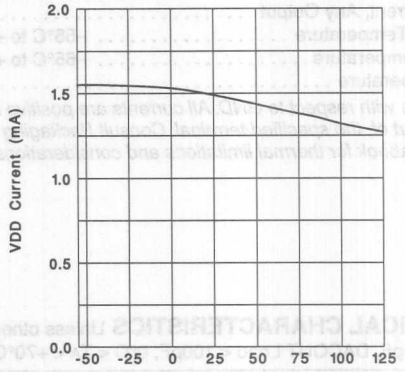
Note 1: Integral nonlinearity is defined as the worst deviation of the converter output from the best-fit straight line through all converter output codes.
Note 2: From 10TH Rising Edge of SCLK.
Note 3: Settling time is to 1% of final value.
Note 4: Guaranteed by design. Not 100% tested in production.

TYPICAL CHARACTERISTICS

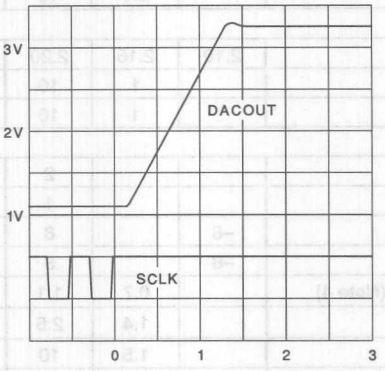
REFOUT vs Temperature



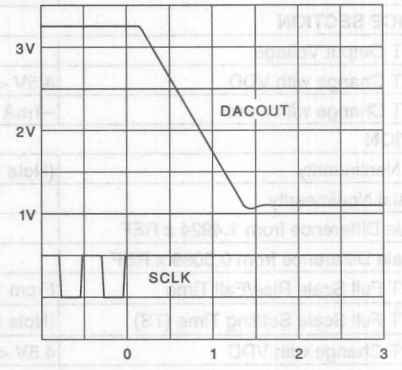
Supply Current vs Temperature



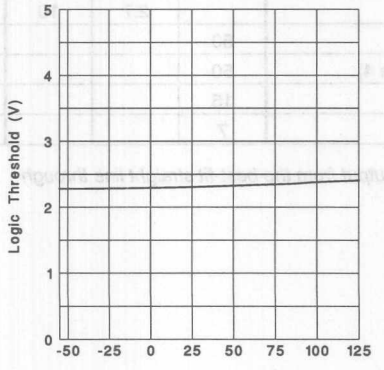
DACOUT Rising Full Scale Step Response



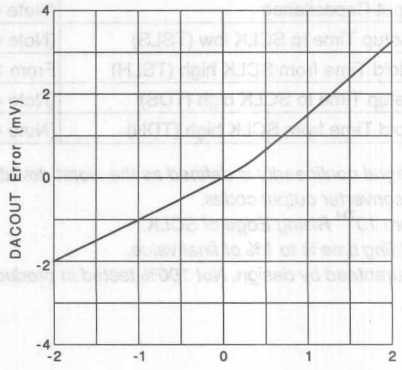
DACOUT Falling Full Scale Step Response



Logic Input Threshold vs Temperature



DACOUT Change with DACOUT Load Current



PIN DESCRIPTIONS

DACOUT: The output of the 10-bit D/A Converter. For best settling time, minimize load capacitance.

DACOUT will go to a voltage between 1.094V and 3.208V depending on the digital code loaded into the latches. The digital code follows this pattern:

Input Code	Typical DACOUT	Significance
1000000000	1.094V	Zero Scale
1000000001	1.096V	
1000000010	1.098V	
...		
1111111111	2.151V	
0000000000	2.153V	Mid Scale
0000000001	2.155V	
...		
0111111110	3.206V	
0111111111	3.208V	Full Scale

GND: All signals are referenced to GND.

REFOUT: The output of the temperature-compensated 2.15V reference. *DO NOT BYPASS REFOUT!* For best stability and transient response, minimize capacitance on REFOUT.

SCLK: Data is clocked into the D/A after SLOD goes low on rising edges of SCLK. After 10 rising edges of SCLK, the data is latched into the D/A output register and the output is updated. Further clock signals on SCLK are ignored until SLOD initiates a new read cycle.

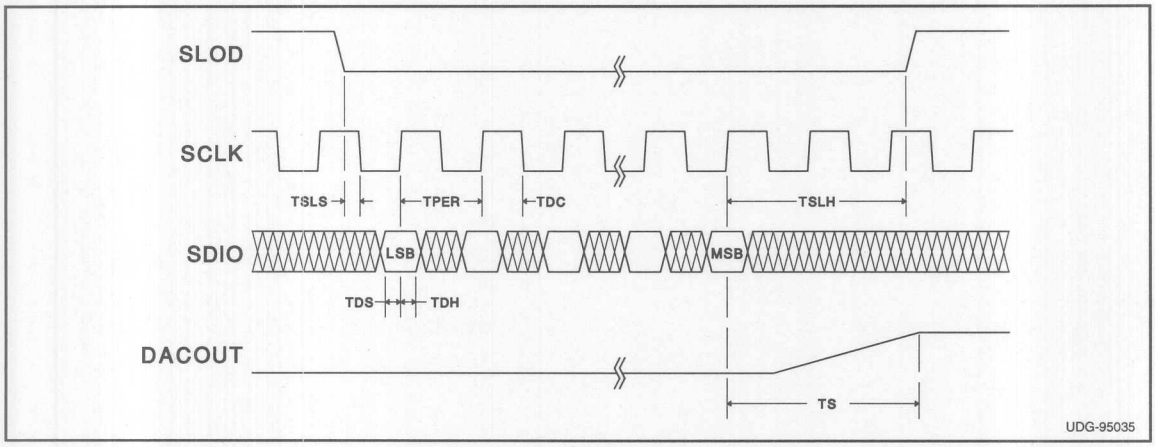
SDIO: After SLOD goes low, data is clocked into the D/A from the SDIO input, on rising edges of SCLK, LSB first. After 10 rising edges, data is latched and converted, and further SCLK and SDIO information is ignored.

SLEEP: SLEEP is the power-down input to the D/A. In systems not requiring this function, wire SLEEP to GND.

SLOD: SLOD is the chip-select input to the UCC5950. SLOD going low selects the D/A and enables clocking of data from SDIO into the D/A. After 10 SCLK pulses, the D/A is updated and SLOD is ignored until SLOD goes high and again goes low.

VDD: All analog and digital functions are powered from VDD. VDD should be a well-regulated supply to minimize output variations. Bypass VDD to GND with a ceramic capacitor very close to the UCC5950.

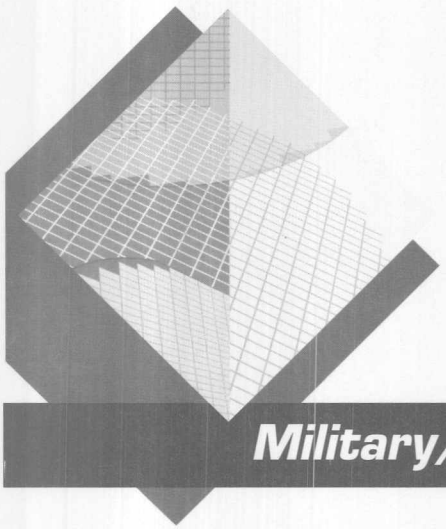
SERIAL DATA INTERFACE TIMING AND LOGIC TABLE



SLOD	Internal Flag	SCLK	SDIO	Internal Count	Action	DACOUT
1	1	*don't care*	*don't care*	0	*no action*	V(t)
0	0	rising edge	DATA	<10	Shift In DATA	V(t)
0	0	rising edge	DATA	10	Latch New DATA Set Internal Flag Reset Count	V(t+1)
0	1	*don't care*	*don't care*	0	*no action*	V(t)

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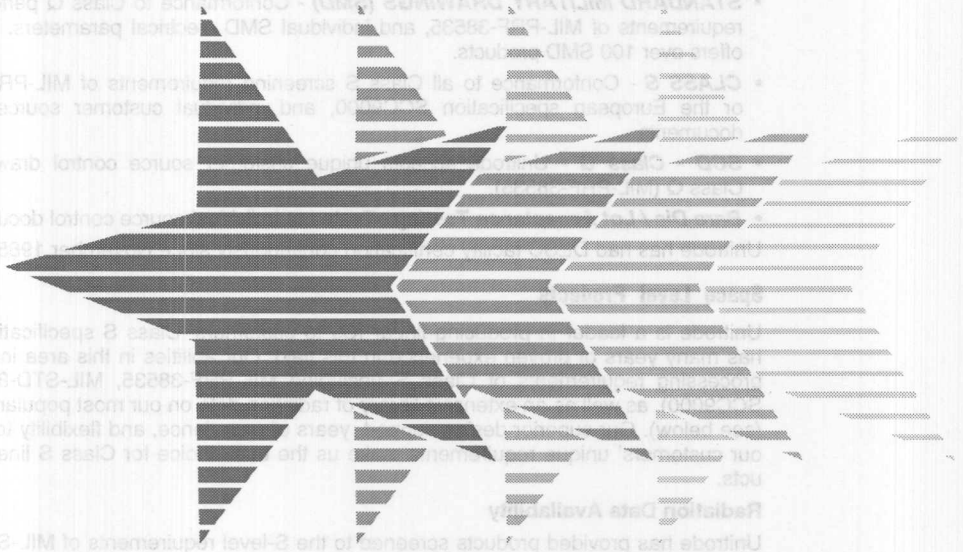


Military/Aerospace Products

11

11


UNITRODE



Military/Aerospace Products

Military/Aerospace Products

Unitrode provides military/aerospace and high reliability products and has a history of innovative, quality products. Our certification to MIL-PRF-38535 demonstrates our commitment to our customers' requirements in this important market. Our product offering includes:

- ***STANDARD MILITARY DRAWINGS (SMD)*** - Conformance to Class Q performance requirements of MIL-PRF-38535, and individual SMD electrical parameters. Unitrode offers over 100 SMD products.
- ***CLASS S*** - Conformance to all Class S screening requirements of MIL-PRF-38535 or the European specification SCC9000, and individual customer source control documents.
- ***SCD - Class Q*** - Unitrode accepts unique customer source control drawings for Class Q (MIL-PRF-38535).
- ***Bare Die / Lot Acceptance Testing*** - Tested to individual source control documents.

Unitrode has had DESC facility certification continuously since November 1985.

Space Level Products

Unitrode is a leader in producing linear ICs to customers' Class S specifications and has many years of proven experience in this field. Our abilities in this area include all processing requirements of Class S (including MIL-PRF-38535, MIL-STD-883, and SCC9000), as well as an extensive library of radiation data on our most popular devices (see below). Our superior design support, years of experience, and flexibility to service our customers' unique requirements make us the best choice for Class S linear products.

Radiation Data Availability

Unitrode has provided products screened to the S-level requirements of MIL-STD-883, MIL-PRF-38535, and the European specification SCC9000. Due to our participation in this market, we have collected a variety of radiation reports including SEU, total dose (including low dose rate), and neutron fluence, which are available upon customer request (see listing below). These reports are results of independent testing by our customers and do not represent guaranteed levels of radiation tolerance by Unitrode.

Radiation Data Available:

UC1524A	UC1525A	UC1527A	UC1637
UC1707	UC1708	UC1710	UC1711
UCC1806	UC1825	UC1825A	UC1834
UC1840	UC1842A	UC1842	UC1843A
UC1843	UC1845A	UC1845	UC1846
UC1847	UC1854	UC1875	UC1901
UC1903	UCC3805	UCC3912	UC5601

Standardized Military Drawings (SMDs) Listing Unitrode as an Approved Supplier

SMD PART NUMBER	UNITRODE PART NUMBER	DESCRIPTION
5962-8670401PA	UC1842J/883B	Current Mode PWM
5962-8670401XA	UC1842L/883B	Current Mode PWM
5962-8670402PA	UC1843J/883B	Current Mode PWM
5962-8670402XA	UC1843L/883B	Current Mode PWM
5962-8670403PA	UC1844J/883B	Current Mode PWM
5962-8670403XA	UC1844L/883B	Current Mode PWM
5962-8670404PA	UC1845J/883B	Current Mode PWM
5962-8670404XA	UC1845L/883B	Current Mode PWM
5962-8670405PA	UC1842AJ/883B	Current Mode PWM
5962-8670405XA	UC1842AL/883B	Current Mode PWM
5962-8670406PA	UC1843AJ/883B	Current Mode PWM
5962-8670406XA	UC1843AL/883B	Current Mode PWM
5962-8670407PA	UC1844AJ/883B	Current Mode PWM
5962-8670407XA	UC1844AL/883B	Current Mode PWM
5962-8670408PA	UC1845AJ/883B	Current Mode PWM
5962-8670408XA	UC1845AL/883B	Current Mode PWM
5962-86806012A	UC1846L/883B	Current Mode PWM
5962-8680601EA	UC1846J/883B	Current Mode PWM
5962-86806022A	UC1847L/883B	Current Mode PWM
5962-8680602EA	UC1847J/883B	Current Mode PWM
5962-87619012A	UC1707L/DESC	Dual Output Driver
5962-8761901EA	UC1707J/DESC	Dual Output Driver
5962-8764502EA	UC1524AJ/DESC	Regulating PWM
5962-87681012A	UC1825L/883B	High Speed PWM
5962-8768101EA	UC1825J/883B	High Speed PWM
5962-87681022A	UC1825AL/883B	High Speed PWM
5962-8768102EA	UC1825AJ/883B	High Speed PWM
5962-8768102XA	UC1825ALP/883B	High Speed PWM
5962-87681032A	UC1825BL/883B	High Speed PWM
5962-8768103EA	UC1825BJ/883B	High Speed PWM
5962-8768103XA	UC1825BLP/883B	High Speed PWM
5962-8774001EA	UC1543J/883B	Supervisory Circuit
5962-8774002EA	UC1544J/883B	Supervisory Circuit

Standardized Military Drawings (SMDs) (cont'd)

Standardized Military Drawings (SMDs) Listing Unitrode as an Approved Supplier

SMD PART NUMBER	UNITRODE PART NUMBER	DESCRIPTION
5962-87742012A	UC1834L/883B	High Efficiency Linear Regulator
5962-8774201EA	UC1834J/883B	High Efficiency Linear Regulator
5962-88697012A	UC1903L/883B	Quad Supply/Line Monitor
5962-8869701VA	UC1903J/883B	Quad Supply/Line Monitor
5962-89441012A	UC1901L/883B	Isolated Feedback Generator
5962-8944101CA	UC1901J/883B	Isolated Feedback Generator
5962-89511012A	UC1525AL/DESC	Regulating PWM
5962-8951101EA	UC1525AJ/DESC	Regulating PWM
5962-89511032A	UC1525AL/883B	Regulating PWM
5962-8951103EA	UC1525AJ/883B	Regulating PWM
5962-8951104EA	UC1527AJ/883B	Regulating PWM
5962-89611012A	UC1706L/DESC	Dual Output Driver
5962-8961101EA	UC1706J/DESC	Dual Output Driver
5962-89899012A	UC1838AL/883B	Mag Amp Controller
5962-8989901EA	UC1838AJ/883B	Mag Amp Controller
5962-89905012A	UC1823L/883B	High Speed PWM
5962-8990501EA	UC1823J/883B	High Speed PWM
5962-89905022A	UC1823AL/883B	High Speed PWM
5962-8990502EA	UC1823AJ/883B	High Speed PWM
5962-89905032A	UC1823BL/883B	High Speed PWM
5962-8990503EA	UC1823BJ/883B	High Speed PWM
5962-89920012A	UC1840L/883B	Programmable PWM
5962-8992001VA	UC1840J/883B	Programmable PWM
5962-89920022A	UC1841L/883B	Programmable PWM
5962-8992002VA	UC1841J/883B	Programmable PWM
5962-89957012A	UC1637L/883B	Switched Mode Controller
5962-8995701VA	UC1637J/883B	Switched Mode Controller
5962-90538012A	UC1611L/883B	Quad Schottky Diode Array
5962-9053801PA	UC1611J/883B	Quad Schottky Diode Array
5962-90650012A	UC1835L/883B	Phase Locked Frequency Controller
5962-9065001PA	UC1835J/883B	Phase Locked Frequency Controller
5962-9098701Q2A	UC1633L/883B	Phase Locked Frequency Controller
5962-9098701QEA	UC1633J/883B	Phase Locked Frequency Controller

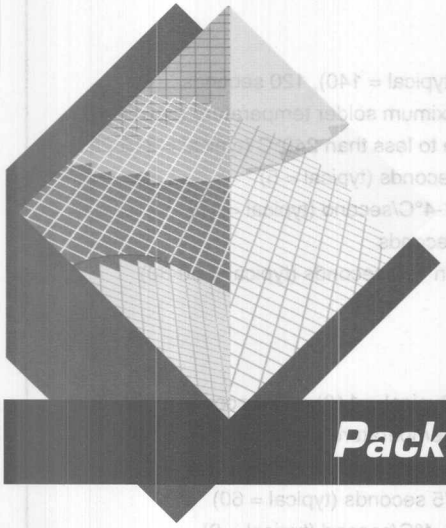
Standardized Military Drawings (SMDs) (cont'd)

Standardized Military Drawings (SMDs) Listing Unitrode as an Approved Supplier

SMD PART NUMBER	UNITRODE PART NUMBER	DESCRIPTION
5962-9168901QXA	UC1625J/883B	Brushless DC Motor Controller
5962-9203101Q2A	UC1864L/883B	Resonant Mode Controller
5962-9203101QEA	UC1864J/883B	Resonant Mode Controller
5962-9203102QEA	UC1865J/883B	Resonant Mode Power Supply Controller
5962-9235001QXC	L293DSP/883B	Four Channel Driver
5962-9320601Q2A	UC1907L/883B	Load Share Controller
5962-9320601QEA	UC1907J/883B	Load Share Controller
5962-9321501Q2A	UC1517L/883B	Stepper Motor Driver
5962-9321501QEA	UC1517J/883B	Stepper Motor Driver
5962-9326101Q2A	UC1854L/883B	Power Factor Preregulator
5962-9326101QEA	UC1854J/883B	Power Factor Preregulator
5962-9326102Q2A	UC1854BL/883B	Power Factor Preregulator
5962-9326102QEA	UC1854BJ/883B	Power Factor Preregulator
5962-9326103Q2A	UC1854AL/883B	Power Factor Preregulator
5962-9326103QEA	UC1854AJ/883B	Power Factor Preregulator
5962-9326501Q2A	UC1832L/883B	Low Dropout Linear Controller
5962-9326501QCA	UC1832J/883B	Low Dropout Linear Controller
5962-9326502Q2A	UC1833L/883B	Low Dropout Linear Controller
5962-9326502QPA	UC1833J/883B	Low Dropout Linear Controller
5962-9451301QPA	UCC1801J/883B	Low Power BiCMOS PWM
5962-9451302QPA	UCC1802J/883B	Low Power BiCMOS PWM
5962-9451303QPA	UCC1803J/883B	Low Power BiCMOS PWM
5962-9451304QPA	UCC1804J/883B	Low Power BiCMOS PWM
5962-9451305QPA	UCC1805J/883B	Low Power BiCMOS PWM
5962-9453001Q2A	UC1856L/883B	Advanced Current Mode PWM
5962-9453001QEA	UC1856J/883B	Advanced Current Mode PWM
5962-9455501Q3A	UC1875L/883B	Phase Shift Resonant Controller
5962-9455501QRA	UC1875J/883B	Phase Shift Resonant Controller
5962-9455501QXA	UC1875LP/883B	Phase Shift Resonant Controller
5962-9457501QEA	UCC1806J/883B	Low Power BiCMOS PWM
5962-9462201Q2A	UC1871L/883B	Resonant Fluorescent Lamp Driver
5962-9462201QVA	UC1871J/883B	Resonant Fluorescent Lamp Driver

Standardized Military Drawings (SMDs) Listing Unitrode as an Approved Supplier

SMD PART NUMBER	UNITRODE PART NUMBER	DESCRIPTION
5962-9474601Q2A	UC1717L/883B	Stepper Motor Drive Circuit
5962-9474601QEA	UC1717J/883B	Stepper Motor Drive Circuit
5962-9554401QJC	UC1620SP/883B	Switchmode Driver for 3-Phase Brushless Motors
5962-9558601QVA	UC1851J/883B	Programmable, Off-Line, PWM Controller
5962-9579801Q2A	UC1705L/883B	High Speed Power Driver
5962-9579801QPA	UC1705J/883B	High Speed Power Driver
77034012A	UC117L/883B	1.5A, 3-Terminal Voltage Regulator
77034052A	UC117AL/DESC	1.5A, 3-Terminal Voltage Regulator
7802801EA	UC1524J/DESC	Advanced Regulating PWM
85515012A	UC1526L/883B	Regulating PWM
8551501VA	UC1526J/883B	Regulating PWM
85515022A	UC1526AL/883B	Regulating PWM
8551502VA	UC1526AJ/883B	Regulating PWM



Packaging Information

12

Packaging Information

The following represents Unitrode's recommended profile limits for various plastic SMD surface mounting approaches. Times and temperatures noted apply to component body and leads. Time/temperature profiles of the surface mount processing equipment may need to be different from what is noted below in order to achieve and maintain the recommended conditions in the immediate proximity of the plastic SMD.

Wave Solder:

- ramp up 1-6°C/second (typical = 4)
- preheat temperature (final stage): 130-150°C (typical = 140)
- total preheat time: less than 120 seconds
- ramp up 1-6°C/second to maximum solder temperature (typical = 4)
- control maximum solder temp to less than 260°C (typical = 240)
- maximum temp dwell: 1-4 seconds (typical = 3 seconds)
- ramp down to room temperature at 1-6°C/second (typical = 4)
- total time spent over 183°C: less than 160 seconds

IR Reflow or Convection:

- ramp up 1-4°C/second (typical = 2)
- soak time/temperature: 130-150°C (typical = 140), 120 seconds
- maximum ramp 1-4°C/second to maximum solder temperature (typical = 2)
- control maximum reflow temperature to less than 240°C (typical = 215-225)
- maximum temperature dwell: 1-10 seconds (typical = 5)
- ramp down to room temperature at 1-4°C/second (typical = 2)
- total time spent over 210°C: 10-40 seconds
- total time spent over 183°C: less than 120 seconds (typical = 60-80)

Vapor Phase Reflow:

- ramp up 1-4°C/second (typical = 2)
- dwell time/temperature: 130-150°C (typical = 140), 120 seconds maximum
- ramp 1-4°C/sec to maximum solder temperature (typical = 2)
- control maximum reflow temperature to less than 219°C (typical = 215)
- maximum temperature dwell: up to 75 seconds (typical = 60)
- ramp down to room temperature at 1-4°C/second (typical = 2)
- total time spent over 183°C: less than 120 seconds (typical = 60-80)

Index

Device Temperature Management 12-3
Thermal Characteristics of Surface Mount Packages 12-7

Package Drawings:

8-Pin Plastic DIP (N) 12-12
14-Pin Plastic DIP (N) 12-12
16-Pin Plastic DIP (N) 12-13
18-Pin Plastic DIP (N) 12-13
20-Pin Plastic DIP (N) 12-14
24-Pin Plastic DIP (N) 12-14
28-Pin Plastic DIP (N) 12-15
20-Pin Plastic PLCC (Q) 12-15
28-Pin Plastic PLCC (Q, QP) 12-16
44-Pin Plastic PLCC (Q, QP) 12-16
8-Pin SOIC (D, DP) 12-17
14-Pin SOIC (D) 12-17
16-Pin SOIC (D, DP, DS) 12-18
16-Pin SOIC (DW) 12-18
18-Pin SOIC (DW) 12-19
20-Pin SOIC (DW) 12-19
24-Pin SOIC (DW) 12-20
28-Pin SOIC (DW, DWP) 12-20
8-Pin Ceramic DIP (J) 12-21
14-Pin Ceramic DIP (J) 12-21
16-Pin Ceramic DIP (J) 12-22
18-Pin Ceramic DIP (J) 12-22
20-Pin Ceramic DIP (J) 12-23
24-Pin Ceramic DIP (J) 12-23
28-Pin Ceramic DIP (J) 12-24
3-Pin TO-220 Plastic (T) 12-24
5-Pin TO-220 Plastic (T) 12-25
20-Pin Ceramic Leadless (L) 12-25
28-Pin Ceramic Leadless (L) 12-26
28-Pin Ceramic Leadless (LP) 12-26
48-Pin LQFP (FQ) 12-27
16-Pin Sidebraze DIP (SP) 12-27
24-Pin Sidebraze DIP (SP) 12-28
16-Pin Zig-Zag Inline (Z) 12-28
36-Pin QSOP (MWP) 12-29
44-Pin QSOP (MWP) 12-29
16-Pin SSOP (M) 12-30
20-Pin SSOP (M) 12-30
8-Pin TSSOP (PW) . . . . . *
20-Pin TSSOP (PW) 12-31
24-Pin TSSOP (PW, PWP) 12-31
28-Pin TSSOP (PWP) 12-32
64-Pin MQFP (FP) 12-33
3-Pin Plastic TO-263 Power Surface Mount (TD) 12-34
5-Pin Plastic TO-263 Power Surface Mount (TD) 12-34

*Consult factory.


UNITRODE

Device Temperature Management

Introduction

All circuit components will dissipate some power while operating and this causes their temperature to rise. Unitrode integrated circuits are designed to handle a considerable range of temperatures, but there are limits. Each part is characterized for a particular temperature range, and the user must see to it that the specified limits are not exceeded. This brief note will give a few hints on how to do this.

Junction Temperature (Tj)

In order to ensure the reliability and long-term operating life of the device, it is essential that the system designer manage the power dissipated by the device in the system such that the junction temperature (Tj) not only does not exceed specified limits, but is kept as low as possible. This is because higher junction temperatures are known to adversely affect the operating life of the device.

Power Dissipation (Pd) and Thermal Resistance (θ)

With the power turned off, all components of a given circuit will be at the same temperature as the ambient provided that sufficient time has elapsed for all differences to settle. With the power on, the various components will be warmed up due to their internal power dissipation, until a new state of equilibrium is reached. The electrical power dissipated by an integrated circuit (Pd) during operation materializes in the form of heat, thus causing its junction temperature to rise. The effectiveness of the I.C. package and the system in dissipating this heat is expressed by the term thermal resistance (θ), which is analogous to electrical resistance in the sense that the materials of the I.C., package and system restrict the flow of heat from the higher junction temperature (Tj) to the lower ambient temperature of the system (Ta). Understanding the thermal resistance characteristics of the package and system will facilitate management of the device junction temperature within desired limits.

The rate of heat flow depends on the temperature difference (ΔT) between the two endpoints (Tj and Ta), and also on the thermal resistance, θ, of the package and system. Heat is a form of energy, and if we choose the joule as the measuring unit we can specify the rate of heat flow in units of joules per second. Therefore,

$$\text{Pd [joules per second]} = \frac{\Delta T}{\theta}$$

and since one joule per second is the same as a watt (W), we have

$$\theta = \frac{\Delta T}{Pd} \ (°C/W)$$

Thermal resistance is typically expressed in terms of resistance from junction-to-ambient (θja), which incorporates not only the internal resistance of the I.C. package, but also the resistance of the system as well. θja can be broken down into the sum of these two different thermal resistances, from junction-to-case, θjc (or in the case of power surface mount packages, junction-to-lead, θjl) and case-to-ambient, θca. Therefore,

$$\theta ja = \frac{Tj - Ta}{Pd} = \theta jc + \theta ca$$

Variables Which Affect θja

The thermal resistance of the package is a function of many variables, such as the leadframe material and design configuration, the plastic encapsulant material, the silicon die area, the die attach material and others. However, as previously indicated, the effectiveness of the system in removing heat from the package also has a significant impact on

Device Temperature Management (cont'd)

θja. These variables include the material and configuration of the circuit board on which the package is mounted, the type of cooling used (i.e. conduction or convection), the size of the traces on the circuit board, the use of heatsinks, etc. It is essential that the system designer understand these variables and how they affect θja.

Unitrode Test Procedures

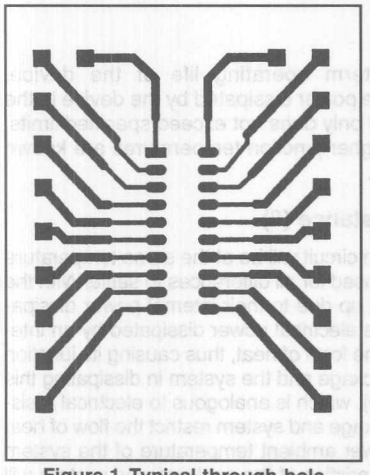


Figure 1. Typical through-hole pc-board design.

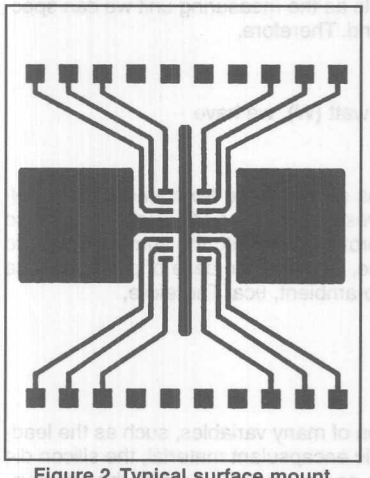


Figure 2. Typical surface mount pc-board design for power leadframe SOIC package.

Table 1 shows thermal resistance values for Unitrode IC packages. Thermal resistance junction-to-case (θjc) is measured by mounting the device to an essentially infinite heat sink. Power leadframe surface mount packages and the batwing DIP conduct a majority of the dissipated power through their leads rather than through the case. For these noted packages, the specified thermal resistance is junction-to-lead (θjl).

Junction-to-ambient (θja) thermal resistance is measure on a 5.0 square inch printed circuit board in 1 cubic foot of still air. For through-hole packages, single side FR-4 boards with 1 oz copper traces are used (see figure 1). However, since surface mount devices, including those without power leadframes, conduct a significant amount of heat through their leads to the pc-board, various types of surface mount boards are measured (see figure 2). To indicate the effect of the pc-board on θja, a range of values is given. The lower value is for a device mounted on a 5.0 square inch, 0.062 inch thick aluminum pc-board. The highest value is for a device mounted on a 5.0 square inch single-sided pc-board. These values are intended to give the system designer an indication of the best and worst case conditions. Some interpolation may be needed based on an individual application to arrive at an accurate estimate of the actual θja.

In order to determine the device θja, a measurement of the device junction temperature is made under the above conditions by utilizing a technique called the "temperature sensitive parameter" method. This technique involves measuring the voltage drop of calibrated component, typically a diode, which then allows calculation of the device junction temperature. Since Pd, Tj, and Ta are known, θja can be determined. For the case of power leadframe surface mount packages, θjl is determined by measuring the temperature of the pc-board at the device leads and then using this temperature in place of the ambient temperature in the calculation. For a more detailed discussion on surface mount packages, refer to "Thermal Characteristics of Surface Mount Packages" found elsewhere in this section.

Example

Estimate the junction temperature of a UC5601DWP 18-Line SCSI Active Terminator on a 4-layer 0.062 inch thick multilayer pc-board at 1.0 watt power dissipation in a still air environment at 30°C.

1. Determine θja.

From Table 1, the DWP package is shown to be a power leadframe surface mount device, so use of thermal resistance junction-to-lead (θjl) is appropriate. For the DWP package, θjl = 16°C/W. From Figure 8 in "Thermal Characteristics of Surface Mount Packages", thermal resistance board-to-ambient (θba) = 19°C/W. We know that for a power leadframe surface mount package, θja = θjl + θba, so

θja = 16°C/W + 19°C/W = 35°C/W.

Device Temperature Management (cont'd)

2. Calculate the junction temperature, Tj.

Tj = (Pd x θja) + Ta

Tj = (1.0 W x 35°C/W) + 30°C

Tj = 65°C

This is well below the maximum rated junction temperature of 150°C listed in the Absolute Maximum Ratings section of the UC5601 product data sheet, so the thermal dissipation is found to be satisfactory.

System Design Considerations

Through-hole devices such as dual in-line packages (DIPs) can be cooled by forcing airflow over the device in order to improve the convection cooling performance, or by conduction cooling of the package case to a heatsink such as the system chassis or cold-wall. Plastic DIPs are not particularly well suited to either of these techniques since the plastic encapsulant is a relatively poor thermal conductor. However, Unitrode offers several through-hole packages which have been optimized for conduction cooling techniques, namely the batwing DIP, the SP power ceramic DIP and the power leadframe Zig-Zag (ZIP) package. All of these packages provide low thermal resistance paths from the junction to the pc-board. Refer to Table 1 for the applicable ratings.

Surface mount packages are well suited to conduction cooling since, as previously indicated, the package leads conduct a significant amount of heat to the pc-board. The pc-board itself can be utilized effectively as a heatsink when designed properly. For example, as seen in the discussion "Thermal Characteristics of Surface Mount Packages", when a power leadframe package is mounted on a multi-layer pc-board such that the heatsink leads are thermally coupled to a ground plane in the board, or an area of copper fan-out on the board, then the overall thermal resistance is considerably lower than on a single-sided board with no heatsinking. Additionally, Unitrode offers a power ceramic leadless chip carrier with a metallized thermal grid on the package case, which can be soldered directly to the board, thus greatly reducing it's overall thermal resistance.

In general, the system designer should attempt to use larger traces on the pc-board where possible in order to spread the heat away from the device more effectively. Also, one should avoid grouping higher power devices tightly together on the board. A better approach would be to spread out the higher power devices to the cooler areas of the board. The choice of pc-board material will greatly affect the overall thermal performance of the system as well, although there are many factors involved when selecting the board material, such as cost, mechanical properties and environmental requirements.

Summary

Thermal management has been shown to be an essential factor in the reliable use of Unitrode integrated circuits. Thermal characteristics of Unitrode packages have been provided to the system designer in order to ensure that the system design effectively dissipates the power generated by the integrated circuit during operation.

Unitrode Package Ratings

PACKAGE SUFFIX	PACKAGE PINS	PACKAGE DESCRIPTION	θjc(°C/W)	θja(°C/W)(2)
D	8	SOIC	42	84-160
D,DS	14, 16	SOIC	35	50-120
DP	8	SOIC Power Lead Frame	22 (1)	40-70
DP	16	SOIC Power Lead Frame	20 (1)	36-58
DW	16	SOIC	27	50-100
DW	20	SOIC	25	45-95
DWP	28	SOIC Power Lead Frame	16 (1)	30-50
FQ	48	LQFP	N/A	76-140
FP	64	MQFP Power Lead Frame	TBD	TBD
J	8	Ceramic Dip	28	160
J	14, 16	Ceramic Dip	28	120
J	18	Ceramic Dip	28	90
J	20	Ceramic Dip	28	85
J	24, 28	Ceramic Dip	20	65
L	20	CLCC	20	70
L	28	CLCC	20	65
LP	28	Power CLCC	20	TBD
N	8	Plastic Dip	50	110
N	14, 16	Plastic Dip	45	90
N	16	Plastic Batwing Dip	12 (1)	25-50 (3)
N	18	Plastic Dip	40	85
N	20	Plastic Dip	35	80
N	24, 28	Plastic Dip	30	60
M	16, 20	SSOP	TBD	TBD
MWP	36, 44	QSOP	TBD	TBD
PW	8	TSSOP	TBD	TBD
PW	20, 24	TSSOP	N/A	150
PWP	24, 28	Power TSSOP	20 (1)	30-70
Q	20	PLCC	34	43-75
Q	28	PLCC	30	40-65
Q	44	PLCC	20	35-50
QP	28	PLCC Power Lead Frame	14 (1)	28-50
QP	44	PLCC Power Lead Frame	12 (1)	24-38
SP	16	Power Ceramic DIP	5	45-63 (4)
SP	24	Power Ceramic DIP	3	28-40 (4)
T	3, 5	TO-220	3 (5)	60 (5)
TD	3, 5	TO-263	3	TBD
Z	16	Power ZIP	24	40-54 (3)

Table 1. Thermal resistance of Unitrode IC package.

TBD : To be determined.
N/A: Not available.
Note 1: Specified thermal resistance is θjl (junction to lead) where noted.
Note 2: Specified θja (junction to ambient) is for devices mounted to 5.0 square inch FR4 PC board with one ounce copper. When resistance range is given, lower values are for 5.0 square inch aluminum PC board – see text.
Note 3: Lower value is for 5.0 square inch multi-layer PC board – see text.
Note 4: Lower value is with a finned heatsink.
Note 5: Values listed are for packages with Eutectic die attach.

UNITRODE

THERMAL CHARACTERISTICS OF SURFACE MOUNT PACKAGES

John A. O'Connor

Introduction

Surface mount packaging continues to expand market share, displacing dual in-line packages (DIPs) at an ever increasing rate. Smaller surface mount devices allow a significant increase in circuit density with a corresponding decrease in system size. Miniaturization is not without penalty however, as thermal management can quickly dominate system packaging design.

With the familiar DIP, the majority of heat is removed through the case. Typically, this is accomplished by convection air currents, although forced air or conduction cooling is often used in more demanding applications. Unlike the DIP however, the majority of heat is removed from surface mount packages through the leads. This means that the PC board design directly affects the thermal capability of surface mounted circuitry. For optimal thermal design, the integrated circuit, the package, and the PC board must be considered as a system.

Many designers use steady-state thermal behavior (thermal resistance) to predict IC junction temperature. While this approach certainly is valid for devices subjected to continuous power dissipation, it often results in an overly conservative design when dissipation varies over time. Generating a model which accounts for transient thermal behavior allows the designer to fully exploit the system's thermal mass. Instantaneous junction temperature can then be calculated, insuring reliability with minimal system size.

Thermal Model

Figure 1 shows the basic model which is expanded for more complex situations. The power dissipated is represented by the current source. Resistance to heat flow is represented by the resistor, and the thermal mass is represented by the capacitor. The analogous thermal units for the current, thermal resistance, and thermal capacitance are also shown in figure 1. Ground is ambient temperature, so all values are temperature rise above ambient. With more complex systems, it is usually easiest to initially convert to electrical units, analyze the circuit, then convert back to thermal units. This approach allows standard electrical circuit analysis tools and techniques to be used without unnecessary confusion.

A surface mounted device on a PC board can be modeled as in figure 2. Each R-C section roughly

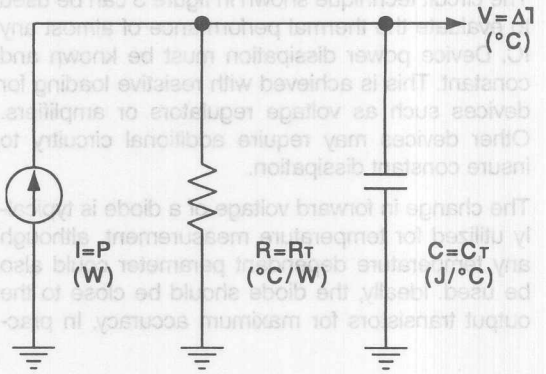


Figure 1. Basic Thermal Model

correlates to the physical system. The first R-C is the device die. The second is the lead frame and package, and the third is the PC board. Other parameters such as the junction to case and case to ambient thermal resistances, are lumped into the three R-C sections. This simplification does cause transient thermal response errors, although normally these errors are small. The additional elements can be broken out separately if greater accuracy is required. Although the physical correlation is far from perfect for the 3 R-C model, the thermal correlation can be very good.

Thermal Characteristics of Surface Mount Packages (cont'd)

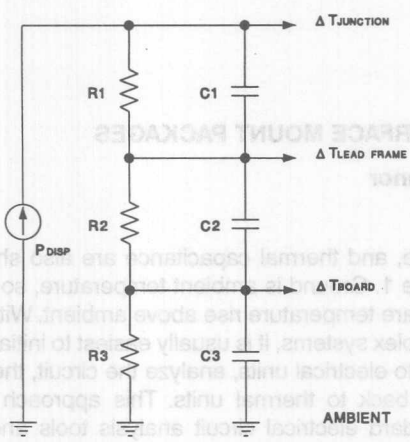


Figure 2. Surface Mounted Device on a PC Board Model

Parameter Measurement

The circuit technique shown in figure 3 can be used to evaluate the thermal performance of almost any IC. Device power dissipation must be known and constant. This is achieved with resistive loading for devices such as voltage regulators or amplifiers. Other devices may require additional circuitry to insure constant dissipation.

The change in forward voltage of a diode is typically utilized for temperature measurement, although any temperature dependant parameter could also be used. Ideally, the diode should be close to the output transistors for maximum accuracy. In practice, this is not critical since the temperature drop across the die will only be a few degrees C in a surface mountable IC. During the test, the measurement diode must not have any current other than the fixed bias current. The bias current should be as small as possible to avoid self-heating the diode.

Many devices have a diode intended for forward biased operation in the actual application circuit such as an output stage clamping diode. If such a diode is not available it may be necessary to forward bias a parasitic diode for measurement. While this approach should be considered a last resort, it can yield acceptable data. If a parasitic diode is forward biased, erratic or unspecified behavior is likely, even with low bias currents. Evaluate the test circuit carefully, insuring that dissipation is constant over the measurement temperature range.

Kelvin all connections to avoid interconnect voltage drops. Every 2mV is approximately 1°C, so even small DC offsets can cause significant error. Without any power applied to the device other than the diode bias current, characterize the diode's forward voltage in an oven at several temperatures over the expected operating junction temperature range. The slope of a best-fit line gives the thermal coefficient (T_C) which is used in subsequent calculations.

Thermocouples are used to sense PC board and ambient temperature. PC board temperature is measured as close to the device as possible.

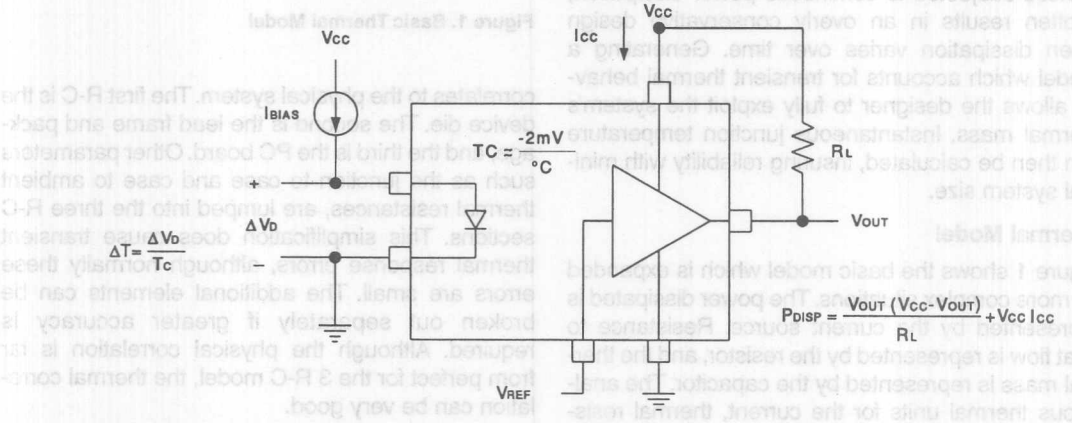


Figure 3. Typical Thermal Test Circuit

Thermal Characteristics of Surface Mount Packages (cont'd)

Some parameters are measured directly while others are derived by curve fitting. Junction to PC board, and PC board to ambient thermal resistance are measured by dissipating a constant power. Allow 15 minutes for the temperature to stabilize. The change in diode forward voltage and PC board temperature give the junction to ambient and board to ambient thermal resistance:

$$R_{(j\text{-}a)} = \Delta V_D / (T_C P_{DISP})$$

$$R_{(b\text{-}a)} = \Delta T_B / P_{DISP}$$

Note that these resistances are based on change in temperature - ambient is assumed constant for the duration of the test. These values correlate to R1, R2, and R3 by:

$$R1 + R2 = R_{(j\text{-}a)} - R_{(b\text{-}a)} \quad (1)$$

$$R3 = R_{(b\text{-}a)} \quad (2)$$

The thermal capacitance of the die is measured by applying a pulsed load and recording the junction temperature waveform. Varying the dissipation pulse width allows observation of each capacitance's effect, although only the die's thermal capacitance can be measured directly. A typical 10ms transient dissipation waveform is shown in figure 4. The thermal time constant of the die is on the order of 30ms. To minimize exponential decay error, the slope of the waveform is measured at (t) = 3ms. The die's thermal capacitance is then:

$$C1 = P_{DISP}\, \Delta t\, T_C / \Delta V_D \quad (3)$$

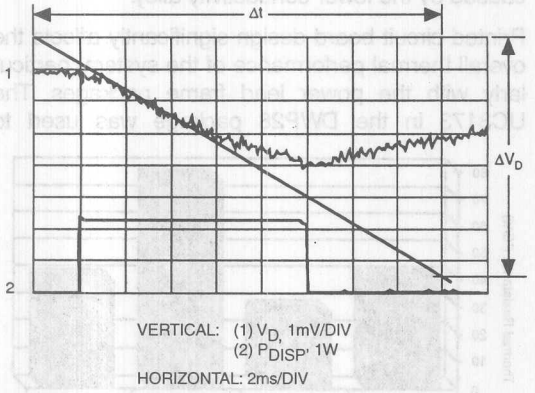


Figure 4: 10ms Transient Dissipation Waveform

Transient waveforms should also be taken for 100ms, 1s, and 10s dissipation intervals to generate an accurate temperature versus time curve. If transient thermal behavior is critical beyond 10 seconds then additional curves must be taken. The thermal time constant of the PC board can go out to several minutes, so a strip chart recorder or computer based data acquisition system will be required. For most systems, this additional data is unnecessary.

The remaining parameters are determined by curve fitting. Visual comparison of measured versus calculated curves is easily done with a spread sheet program. Measured junction temperature versus time data (4 points per decade is sufficient) is entered into the spread sheet. Junction temperature is then calculated at each point with estimated values for R2 and C2 and C3 using:

$$T(t) = P_{DISP}\,[R1(1-e^{-t/\tau 1}) + R2(1-e^{-t/\tau 2}) + R3(1-e^{-t/\tau 3})] \quad (4)$$

Data presented in the following section will help in estimating initial values. This procedure is iterated until an acceptable curve fit is achieved. C3's value is iterated only if the measured curve goes out to several minutes. Figure 5 is a typical measured and calculated junction temperature versus time curve. A logarithmic time axis aids in curve fitting by spreading data points evenly.

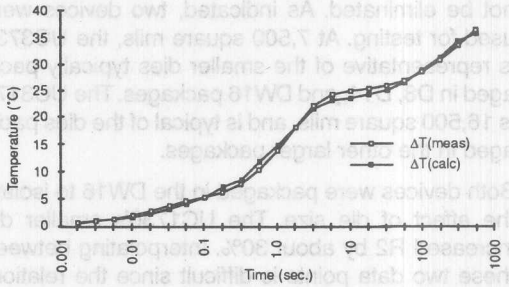


Figure 5. Juction Temperature versus Time for FQP48 Package Dissipating 1W.

Typical Data

The preceding technique was used to characterize two devices in nine different packages. Five different PC board types were also tested to provide relative comparison. This information should be used to help initially determine package, PC board type, and layout. It must be stressed that this typical data should not substitute for a rigorous thermal analysis of the actual application.

Thermal Characteristics of Surface Mount Packages (cont'd)

PACKAGE	R1 (°C/W)	C1 (J/°C)	τ1 (sec)	R2 (°C/W)	C2 (J/°C)	τ2 (sec)	R3 (°C/W)	C3 (J/°C)	τ3 (sec)	R(J-a) (°C/W)
D8	5	0.0035	0.02	64	0.030	1.9	15	24	360	84
D14	4	0.0045	0.02	45	0.035	1.6	16	24	384	65
DW16	4	0.0045	0.02	44	0.070	3.1	15	24	360	63
DW16	4	0.011	0.04	34	0.11	3.7	13	24	312	51
DWP28	2.5	0.008	0.02	13	0.13	1.7	15	24	360	30
Q20	3	0.010	0.02	26	0.12	3.1	14	24	336	43
Q28	2.5	0.008	0.02	25	0.12	2.9	13	24	312	40
QP28	2.5	0.009	0.02	12	0.25	3.0	14	24	336	28
FQ48	4	0.006	0.02	57	0.07	4.0	15	24	360	76
FQP48	4	0.005	0.02	21	0.08	1.7	14	25	350	39

Figure 6. Model Values Versus Package Type for 1W Dissipation on Aluminum PC Board.

Figure 6 shows model values and time constants versus package type, mounted on an aluminum PC board [1]. Junction to ambient thermal resistance is also shown to indicate overall steady state thermal performance. All data was taken with one watt dissipated. The values that were determined by curve fitting result in a fairly conservative model. Values were chosen which tended to predict higher temperature than actually measured where errors could not be eliminated. As indicated, two devices were used for testing. At 7,500 square mils, the UC3730 is representative of the smaller dies typically packaged in D8, D14, and DW16 packages. The UC3173 is 16,500 square mils, and is typical of the dies packaged in the other larger packages.

Both devices were packaged in the DW16 to isolate the effect of die size. The UC1730's smaller die increased R2 by about 30%. Interpolating between these two data points is difficult since the relationship between die size and thermal resistance is nonlinear. Curves are available which account for this dimensional difference [2], although the actual conditions differ and are more complicated than the configuration used to generate the curves. Fortunately, the resulting error will be small in most applications. Conservatively estimating R2 will minimally impact system size, but if a more accurate value is required the actual device can be characterized on a test PC board.

Figure 7 illustrates the power lead frame's dramatic improvement in thermal performance over standard lead frames by comparing the junction to ambient thermal resistances of the QP28 to the Q28, and the FQP48 to the FQ48. Standard lead frames connect the die to the leads thermally through the epoxy molding compound. Power lead frame packages incorporate a single piece for die attachment and ground leads. This uninterrupted, high thermal conductivity path offers a significant improvement over standard lead frames. Occasionally a stiffer but less conductive alloy is used for standard lead frames. The FQ48's poorer thermal performance is partially caused by the lower conductivity alloy.

Printed circuit board design significantly affects the overall thermal performance of the system, particularly with the power lead frame packages. The UC3173 in the DWP28 package was used to

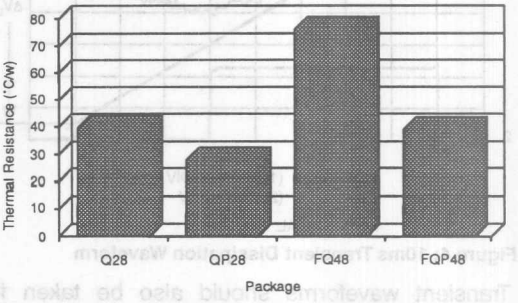


Figure 7. Power lead frames significantly reduce thermal resistance.

Thermal Characteristics of Surface Mount Packages (cont'd)

compare PC board thermal performance. Five different PC board types were evaluated with one watt dissipated:

1. Single side 1 oz. copper, 0.062 aluminum
2. Single side 1 oz. copper, 0.062 FR4 epoxy fiberglass
3. Single side 2 oz. copper, 0.062 FR4 epoxy fiberglass
4. Four layer (signal, ground, Vcc, signal) 1 oz. copper, 0.031 FR4 epoxy fiberglass
5. Four layer (signal, ground, Vcc, signal) 1 oz. copper, 0.062 FR4 epoxy fiberglass

PCB TYPE	R(b-a) (°C/W)	C(b-a) (J/°C)	τ (sec)
Aluminum	15	24	360
FR4 -1oz.	31	2.5	78
FR4 -2oz.	25	3	74
4 layer - 0.031	21	4	84
4 layer - 0.062	19	5	94

Figure 8. Board to ambient thermal resistance and capacitance versus PC board type for DWP28 package dissipating 1W.

The thermal resistance, capacitance, and time constants for the five PC boards are shown in figure 8. The PC board layouts used for testing are shown in figure 9. Only the component side is shown for the four layer boards. The back side, which has 10 mil traces on 50 mil centers to provide a typical amount of interconnect copper, and the Vcc plane were unconnected. The inner ground plane is connected to the small component side ground plane through 16 feed-throughs.

As expected, the aluminum PC board's significantly higher specific heat results in nearly an order of magnitude increase in thermal capacitance. Surprisingly the four layer 0.062 board's thermal resistance is nearly as low as the aluminum board's, indicating good heat distribution through the inner planes. Note that although the Vcc plane is unconnected, it does help distribute the heat across the board. Conduction or forced air cooling is necessary to fully exploit the aluminum board's capability.

Summary

A method for accurately modeling the thermal behavior of a surface mounted IC has been presented. The model relies on measured data, insuring excellent correlation to the physical system. Typical thermal behavior of nine different packages and five different PC boards were also presented, indicating relative thermal performance differences. Optimum thermal system design is achievable using the techniques and data presented.

References

1. Thermal Clad insulated metal substrates, The Bergquist Company, 5300 Edina Industrial Blvd., Minneapolis, MN 55439, 612-835-2322
2. R. Tummala, E. Rymaszewski, "Microelectronics Packaging Handbook", Van Nostrand Reinhold, 1989, pp173-179

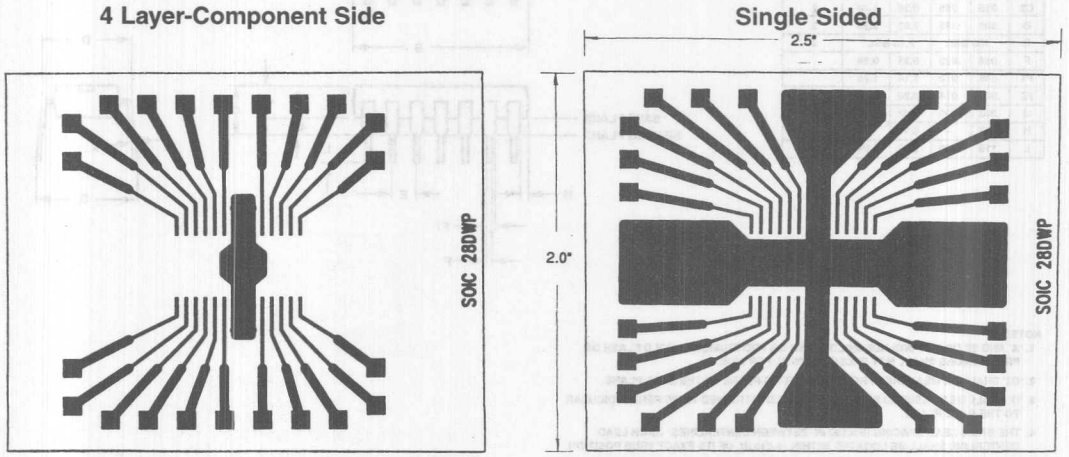
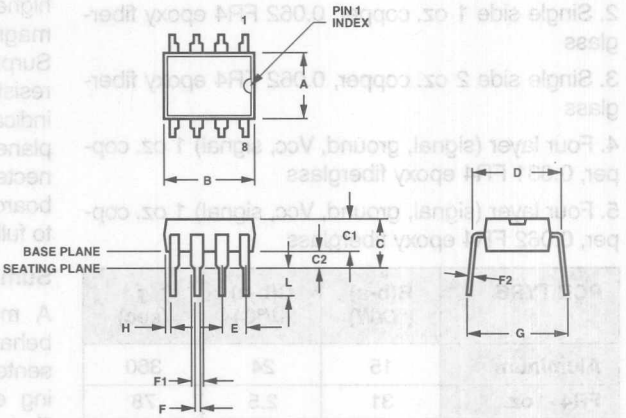


Figure 9. Test PC Board Layouts (SOIC 28DWP)

Mechanical Drawings

8-PIN PLASTIC DIP ~ N PACKAGE SUFFIX

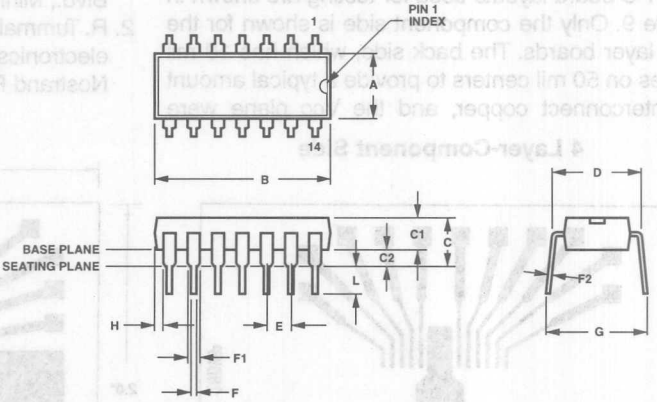
DIMENSIONS					
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	.245	.260	6.22	6.60	1
B	.320	.400	9.40	10.16	1
C	–	.210	–	5.33	
C1	.125	.150	3.18	3.81	
C2	.015	.055	0.38	1.40	2
D	.300	.325	7.62	8.26	3
E	.100 BSC		2.54 BSC		4
F	.014	.022	0.35	0.56	
F1	.045	.070	1.14	1.78	
F2	.008	.014	0.20	0.35	
G	.300	.400	7.62	10.16	5
H	.005	–	0.13	–	
L	.115	.160	2.92	4.06	



NOTES:
1. 'A' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. 'C2' SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
3. 'D' SHALL BE MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO THE BASE PLANE.
4. THE BASIC LEAD SPACING IS 0.100 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.010 IN. OF ITS EXACT TRUE POSITION.
5. 'G' SHALL BE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
6. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.

14-PIN PLASTIC DIP ~ N PACKAGE SUFFIX

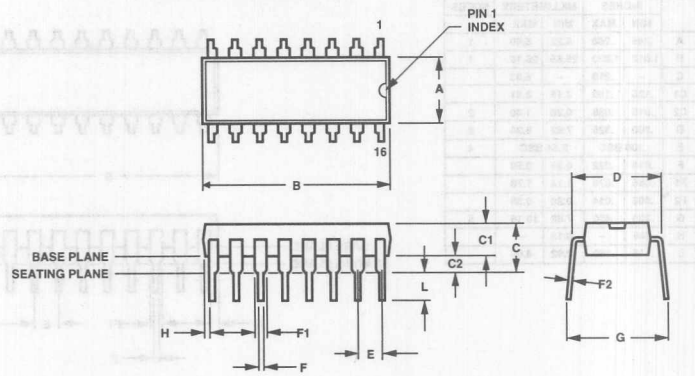
DIMENSIONS					
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	.245	.260	6.22	6.60	1
B	.745	.775	18.92	19.68	1
C	–	.210	–	5.33	
C1	.125	.150	3.18	3.81	
C2	.015	.055	0.38	1.40	2
D	.300	.325	7.62	8.26	3
E	.100 BSC		2.54 BSC		4
F	.014	.022	0.35	0.56	
F1	.045	.070	1.14	1.78	
F2	.008	.014	0.20	0.35	
G	.300	.400	7.62	10.16	5
H	.005	–	0.13	–	
L	.115	.160	2.92	4.06	



NOTES:
1. 'A' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. 'C2' SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
3. 'D' SHALL BE MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO THE BASE PLANE.
4. THE BASIC LEAD SPACING IS 0.100 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.010 IN. OF ITS EXACT TRUE POSITION.
5. 'G' SHALL BE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
6. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.

16-PIN PLASTIC DIP ~ N PACKAGE SUFFIX

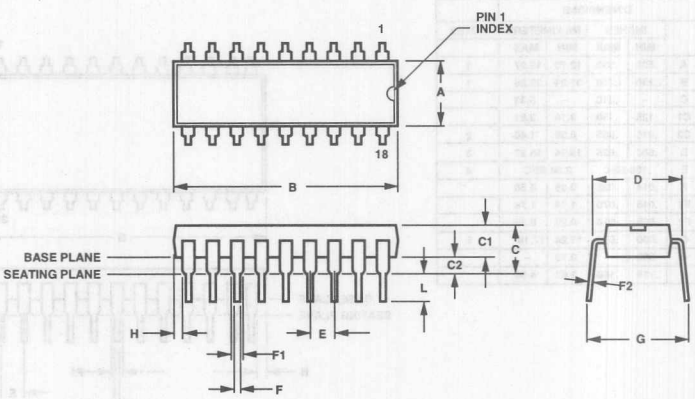
	DIMENSIONS				
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	.245	.260	6.22	6.60	1
B	.745	.775	18.92	19.68	1
C	–	.210	–	5.33	
C1	.125	.150	3.18	3.81	
C2	.015	.055	0.38	1.40	2
D	.300	.325	7.62	8.26	3
E	.100 BSC		2.54 BSC		4
F	.014	.022	0.35	0.56	
F1	.045	.070	1.14	1.78	
F2	.008	.014	0.20	0.35	
G	.300	.400	7.62	10.16	5
H	.005	–	0.13	–	
L	.115	.160	2.92	4.06	



NOTES:
1. 'A' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. 'C2' SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
3. 'D' SHALL BE MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO THE BASE PLANE.
4. THE BASIC LEAD SPACING IS 0.100 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.010 IN. OF ITS EXACT TRUE POSITION.
5. 'G' SHALL BE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
6. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.

18-PIN PLASTIC DIP ~ N PACKAGE SUFFIX

	DIMENSIONS				
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	.245	.260	6.22	6.60	1
B	.890	.920	22.61	23.39	1
C	–	.210	–	5.33	
C1	.125	.150	3.18	3.81	
C2	.015	.055	0.38	1.40	2
D	.300	.325	7.62	8.26	3
E	.100 BSC		2.54 BSC		4
F	.014	.022	0.35	0.56	
F1	.045	.070	1.14	1.78	
F2	.008	.014	0.20	0.35	
G	.300	.400	7.62	10.16	5
H	.005	–	0.13	–	
L	.115	.160	2.92	4.06	

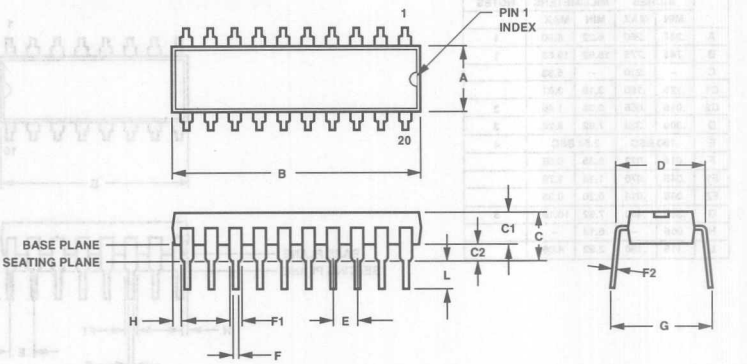


NOTES:
1. 'A' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. 'C2' SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
3. 'D' SHALL BE MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO THE BASE PLANE.
4. THE BASIC LEAD SPACING IS 0.100 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.010 IN. OF ITS EXACT TRUE POSITION.
5. 'G' SHALL BE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
6. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.

Mechanical Drawings (cont'd)

20-PIN PLASTIC DIP ~ N PACKAGE SUFFIX

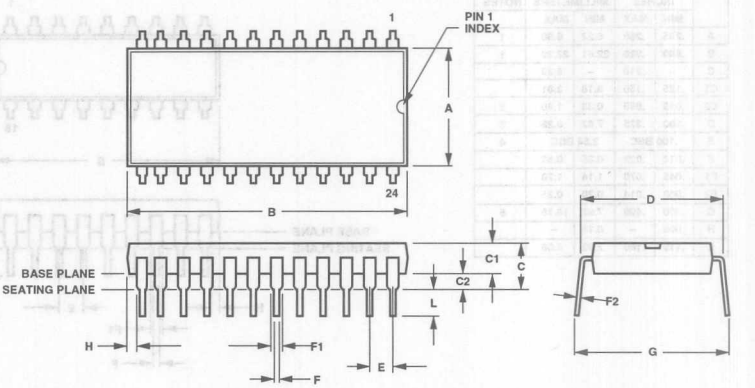
	DIMENSIONS				
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	.245	.260	6.22	6.60	1
B	1.010	1.030	25.65	26.16	1
C	–	.210	–	5.33	
C1	.125	.150	3.18	3.81	
C2	.015	.055	0.38	1.40	2
D	.300	.325	7.62	8.26	3
E	.100 BSC		2.54 BSC		4
F	.014	.022	0.35	0.56	
F1	.045	.070	1.14	1.78	
F2	.008	.014	0.20	0.35	
G	.300	.400	7.62	10.16	5
H	.005	–	0.13	–	
L	.115	.160	2.92	4.06	



NOTES:
1. 'A' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. 'C2' SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
3. 'D' SHALL BE MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO THE BASE PLANE.
4. THE BASIC LEAD SPACING IS 0.100 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.010 IN. OF ITS EXACT TRUE POSITION.
5. 'G' SHALL BE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
6. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.

24-PIN PLASTIC DIP ~ N PACKAGE SUFFIX

	DIMENSIONS				
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	.500	.550	12.70	13.97	1
B	1.230	1.270	31.24	32.26	1
C	–	.210	–	5.33	
C1	.125	.150	3.18	3.81	
C2	.015	.055	0.38	1.40	2
D	.600	.625	15.24	15.87	3
E	.100 BSC		2.54 BSC		4
F	.014	.022	0.35	0.56	
F1	.045	.070	1.14	1.78	
F2	.008	.014	0.20	0.35	
G	.600	.675	15.24	17.15	5
H	.005	–	0.13	–	
L	.115	.160	2.92	4.06	

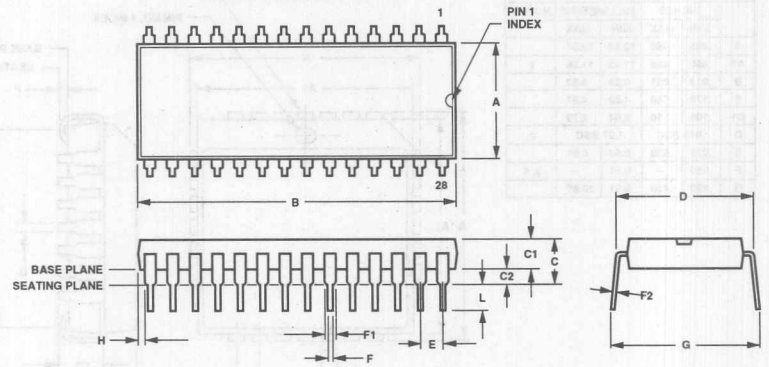


NOTES:
1. 'A' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. 'C2' SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
3. 'D' SHALL BE MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO THE BASE PLANE.
4. THE BASIC LEAD SPACING IS 0.100 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.010 IN. OF ITS EXACT TRUE POSITION.
5. 'G' SHALL BE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
6. CONTROLLING DIMENSIONS: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.

Mechanical Drawings (cont'd)

28-PIN PLASTIC DIP ~ N PACKAGE SUFFIX

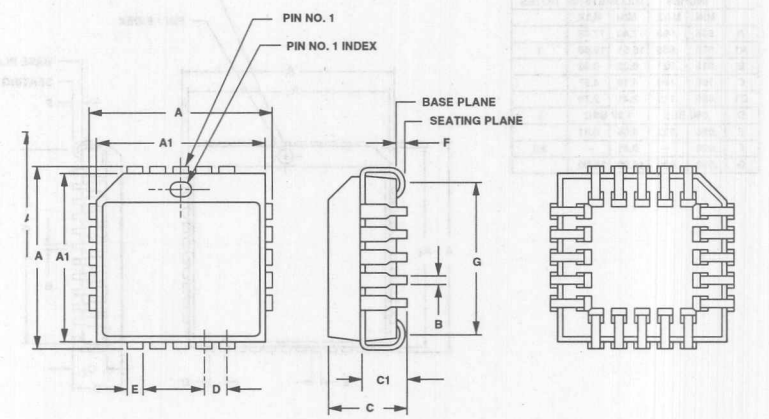
	DIMENSIONS				
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	.500	.550	12.70	13.97	1
B	1.380	1.470	35.10	37.34	1
C	–	.210	–	5.33	
C1	.125	.150	3.18	3.81	
C2	.015	.055	0.38	1.40	2
D	.600	.625	15.24	15.87	3
E	.100 BSC		2.54 BSC		4
F	.014	.022	0.35	0.56	
F1	.045	.070	1.14	1.78	
F2	.008	.014	0.20	0.35	
G	.600	.675	15.24	17.15	5
H	.005	–	0.13	–	
L	.115	.160	2.92	4.06	



NOTES:
1. 'A' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. 'C2' SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
3. 'D' SHALL BE MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO THE BASE PLANE.
4. THE BASIC LEAD SPACING IS 0.100 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.010 IN. OF ITS EXACT TRUE POSITION.
5. 'G' SHALL BE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
6. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.

20-PIN PLASTIC PLCC SURFACE MOUNT ~ Q PACKAGE SUFFIX

	DIMENSIONS				
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	.385	.395	9.78	10.03	
A1	.350	.356	8.89	9.04	1
B	.013	.021	0.33	0.53	
C	.170	.180	4.32	4.57	
C1	.100	.110	2.54	2.79	
D	.050 BSC		1.27 BSC		2
E	.026	.032	0.66	0.81	
F	.020	–	0.51	–	3, 4
G	.290	.330	7.37	8.38	

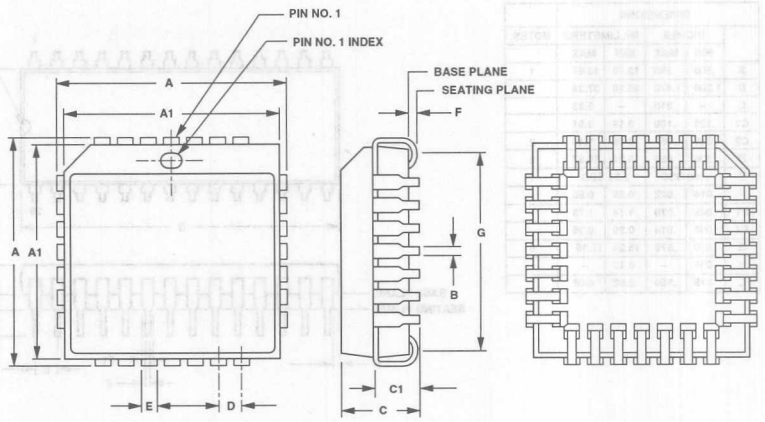


NOTES:
1. 'A1' DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. THE BASIC LEAD SPACING IS 0.050 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.004 IN. OF ITS EXACT TRUE POSITION.
3. 'F' IS MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
4. LEADS SHALL BE COPLANAR WITHIN 0.004 IN. AT THE SEATING PLANE.
5. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.

Mechanical Drawings (cont'd)

28-PIN PLASTIC PLCC SURFACE MOUNT ~ Q, QP PACKAGE SUFFIX

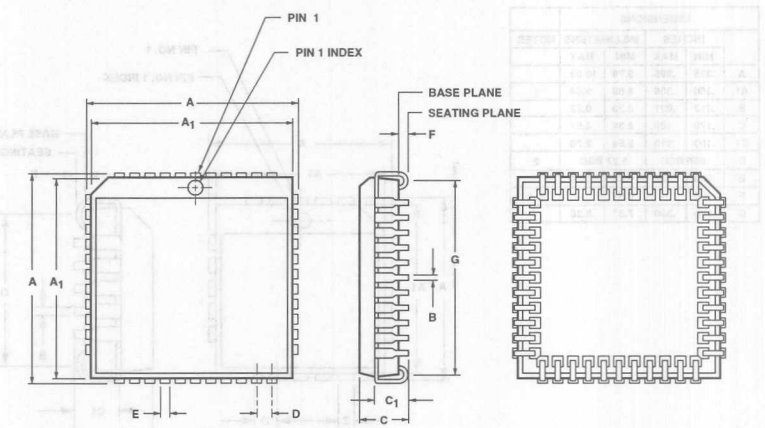
	DIMENSIONS				
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	.485	.495	12.32	12.57	
A1	.450	.456	11.43	11.58	1
B	.013	.021	0.33	0.53	
C	.170	.180	4.32	4.57	
C1	.100	.110	2.54	2.79	
D	.050 BSC		1.27 BSC		2
E	.026	.032	0.66	0.81	
F	.020	–	0.51	–	3, 4
G	.390	.430	9.91	10.92	



NOTES:
1. 'A1' DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. THE BASIC LEAD SPACING IS 0.050 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.004 IN. OF ITS EXACT TRUE POSITION.
3. 'F' IS MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
4. LEADS SHALL BE COPLANAR WITHIN 0.004 IN. AT THE SEATING PLANE.
5. CONTROLLING DIMENSION : INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.

44-PIN PLASTIC PLCC SURFACE MOUNT ~ Q, QP PACKAGE SUFFIX

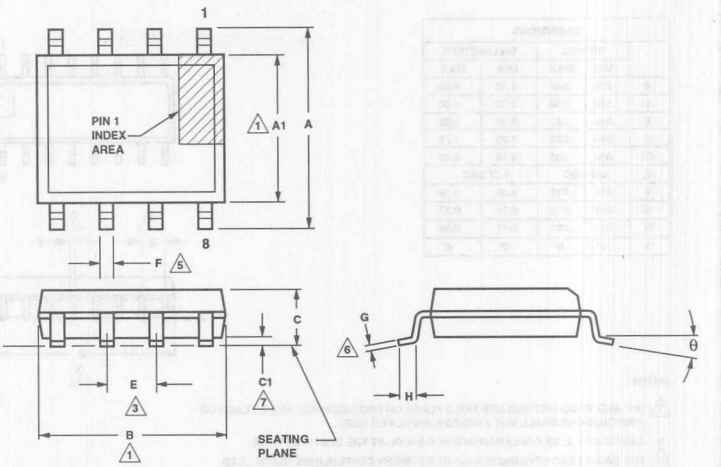
	DIMENSIONS				
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	.685	.695	17.40	17.65	
A1	.650	.656	16.51	16.66	1
B	.013	.021	0.33	0.53	
C	.165	.180	4.19	4.57	
C1	.095	.110	2.41	2.79	
D	.050 BSC		1.27 BSC		2
E	.026	.032	0.66	0.81	
F	.020	–	0.51	–	3,4
G	.590	.630	14.99	16.00	



NOTES:
1. 'A1' DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. THE BASIC LEAD SPACING IS 0.050 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.004 IN. OF ITS EXACT TRUE POSITION.
3. 'F' IS MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
4. LEADS SHALL BE COPLANAR WITHIN 0.004 IN. AT THE SEATING PLANE.
5. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.

8-PIN SOIC SURFACE MOUNT ~ D, DP PACKAGE SUFFIX

DIMENSIONS				
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.228	.244	5.80	6.20
A1	.150	.158	3.80	4.00
B	.189	.196	4.80	4.98
C	.053	.069	1.35	1.75
C1	.004	.009	0.10	0.23
E	.050 BSC		1.27 BSC	
F	.014	.019	0.35	0.48
G	.007	.010	0.19	0.25
H	.016	.035	0.41	0.89
θ	0°	8°	0°	8°

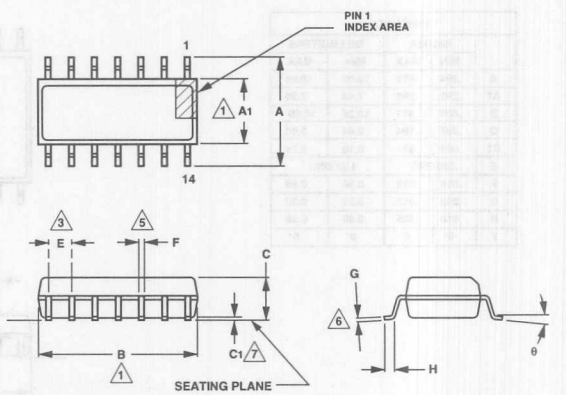


NOTES:

1. 'A1' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. LEADS SHALL BE COPLANAR WITHIN 0.004 IN. AT THE SEATING PLANE.
3. THE BASIC LEAD SPACING IS 0.050 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.004 IN. OF ITS EXACT TRUE POSITION.
4. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
5. DIMENSION 'F' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'F' MAXIMUM BY MORE THAN 0.003 IN. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.004 IN. AND 0.010 IN. FROM THE LEAD TIP.
7. 'C1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

14-PIN SOIC SURFACE MOUNT ~ D PACKAGE SUFFIX

DIMENSIONS				
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.228	.244	5.80	6.20
A1	.150	.158	3.80	4.00
B	.336	.344	8.55	8.75
C	.053	.069	1.35	1.75
C1	.004	.009	0.10	0.22
E	.050 BSC		1.27 BSC	
F	.014	.019	0.36	0.48
G	.007	.010	0.19	0.25
H	.016	.035	0.41	0.89
θ	0°	8°	0°	8°



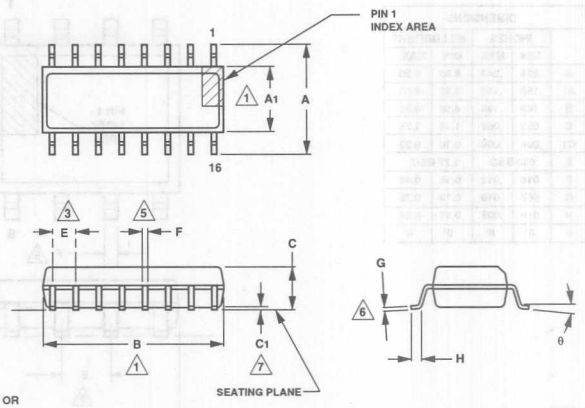
NOTES:

1. 'A1' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. LEADS SHALL BE COPLANAR WITHIN 0.004 IN. AT THE SEATING PLANE.
3. THE BASIC LEAD SPACING IS 0.050 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.004 IN. OF ITS EXACT TRUE POSITION.
4. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
5. DIMENSION 'F' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'F' MAXIMUM BY MORE THAN 0.003 IN. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.004 IN. AND 0.010 IN. FROM THE LEAD TIP.
7. 'C1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

Mechanical Drawings (cont'd)

16-PIN SOIC SURFACE MOUNT ~ D, DP, DS PACKAGE SUFFIX

	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.228	.244	5.80	6.20
A1	.150	.158	3.80	4.00
B	.386	.393	9.80	9.98
C	.053	.069	1.35	1.75
C1	.004	.009	0.10	0.22
E	.050 BSC		1.27 BSC	
F	.014	.019	0.36	0.48
G	.007	.010	0.19	0.25
H	.016	.035	0.41	0.89
θ	0°	8°	0°	8°

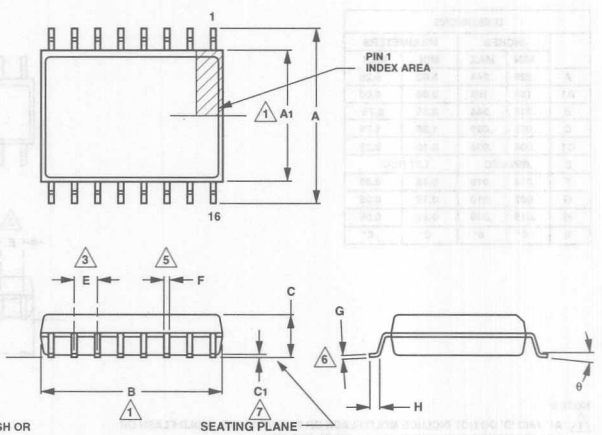


NOTES:

1. 'A1' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. LEADS SHALL BE COPLANAR WITHIN 0.004 IN. AT THE SEATING PLANE.
3. THE BASIC LEAD SPACING IS 0.050 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.004 IN. OF ITS EXACT TRUE POSITION.
4. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
5. DIMENSION 'F' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'F' MAXIMUM BY MORE THAN 0.003 IN. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.004 IN. AND 0.010 IN. FROM THE LEAD TIP.
7. 'C1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

16-PIN SOIC SURFACE MOUNT ~ DW PACKAGE SUFFIX

	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.394	.419	10.00	10.64
A1	.292	.299	7.42	7.59
B	.403	.413	10.24	10.49
C	.097	.104	2.46	2.64
C1	.004	.011	0.10	0.28
E	.050 BSC		1.27 BSC	
F	.014	.019	0.36	0.48
G	.009	.012	0.23	0.30
H	.018	.035	0.46	0.89
θ	0°	8°	0°	8°

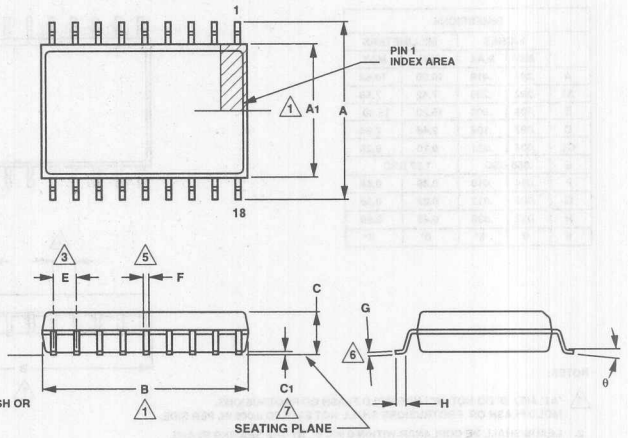


NOTES:

1. 'A1' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. LEADS SHALL BE COPLANAR WITHIN 0.004 IN. AT THE SEATING PLANE.
3. THE BASIC LEAD SPACING IS 0.050 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.004 IN. OF ITS EXACT TRUE POSITION.
4. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
5. DIMENSION 'F' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'F' MAXIMUM BY MORE THAN 0.003 IN. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.004 IN. AND 0.010 IN. FROM THE LEAD TIP.
7. 'C1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

18-PIN SOIC SURFACE MOUNT ~ DW PACKAGE SUFFIX

	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.394	.419	10.00	10.64
A1	.292	.299	7.42	7.59
B	.453	.462	11.51	11.73
C	.097	.104	2.46	2.64
C1	.004	.011	0.10	0.28
E	.050 BSC		1.27 BSC	
F	.014	.019	0.36	0.48
G	.009	.012	0.23	0.30
H	.018	.035	0.46	0.89
θ	0°	8°	0°	8°

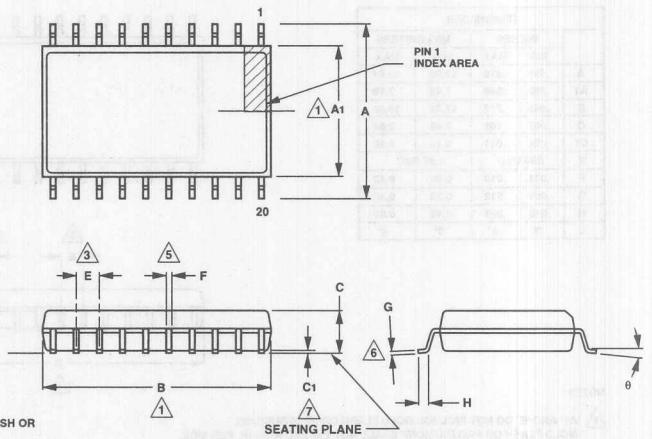


NOTES:

1. 'A1' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. LEADS SHALL BE COPLANAR WITHIN 0.004 IN. AT THE SEATING PLANE.
3. THE BASIC LEAD SPACING IS 0.050 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.004 IN. OF ITS EXACT TRUE POSITION.
4. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
5. DIMENSION 'F' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'F' MAXIMUM BY MORE THAN 0.003 IN. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.004 IN. AND 0.010 IN. FROM THE LEAD TIP.
7. 'C1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

20-PIN SOIC SURFACE MOUNT ~ DW PACKAGE SUFFIX

	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.394	.419	10.00	10.64
A1	.292	.299	7.42	7.59
B	.504	.511	12.80	12.98
C	.097	.104	2.46	2.64
C1	.004	.011	0.10	0.28
E	.050 BSC		1.27 BSC	
F	.014	.019	0.36	0.48
G	.009	.012	0.23	0.30
H	.018	.035	0.46	0.89
θ	0°	8°	0°	8°



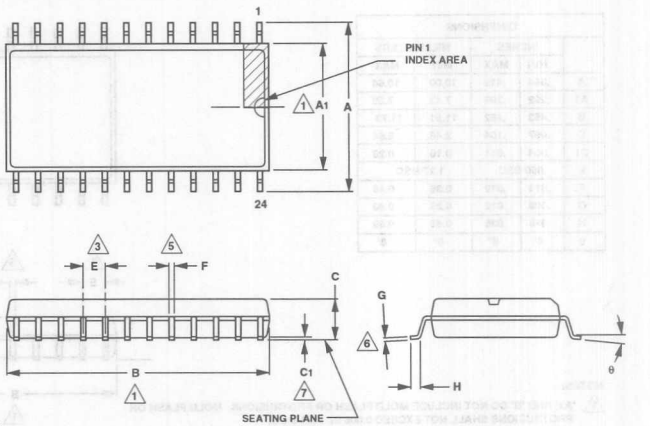
NOTES:

1. 'A1' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. LEADS SHALL BE COPLANAR WITHIN 0.004 IN. AT THE SEATING PLANE.
3. THE BASIC LEAD SPACING IS 0.050 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.004 IN. OF ITS EXACT TRUE POSITION.
4. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
5. DIMENSION 'F' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'F' MAXIMUM BY MORE THAN 0.003 IN. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.004 IN. AND 0.010 IN. FROM THE LEAD TIP.
7. 'C1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

Mechanical Drawings (cont'd)

24-PIN SOIC SURFACE MOUNT ~ DW PACKAGE SUFFIX

	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.394	.419	10.00	10.64
A1	.292	.299	7.42	7.59
B	.598	.606	15.20	15.40
C	.097	.104	2.46	2.64
C1	.004	.011	0.10	0.28
E	.050 BSC		1.27 BSC	
F	.014	.019	0.36	0.48
G	.009	.012	0.23	0.30
H	.019	.035	0.46	0.89
θ	0°	8°	0°	8°

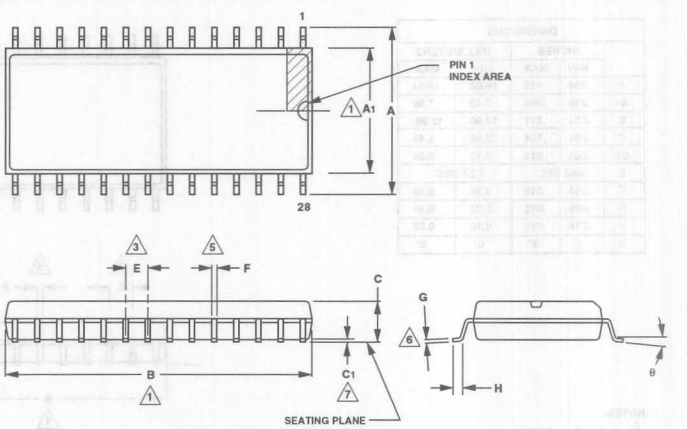


NOTES:

1. 'A1' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. LEADS SHALL BE COPLANAR WITHIN 0.004 IN. AT THE SEATING PLANE.
3. THE BASIC LEAD SPACING IS 0.050 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.004 IN. OF ITS EXACT TRUE POSITION.
4. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
5. DIMENSION 'F' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'F' MAXIMUM BY MORE THAN 0.003 IN. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.004 IN. AND 0.010 IN. FROM THE LEAD TIP.
7. 'C1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

28-PIN SOIC SURFACE MOUNT ~ DW, DWP PACKAGE SUFFIX

	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.394	.419	10.00	10.64
A1	.292	.299	7.42	7.59
B	.698	.712	17.73	18.08
C	.097	.104	2.46	2.64
C1	.004	.011	0.10	0.28
E	.050 BSC		1.27 BSC	
F	.014	.019	0.36	0.48
G	.009	.012	0.23	0.30
H	.018	.035	0.46	0.89
θ	0°	8°	0°	8°



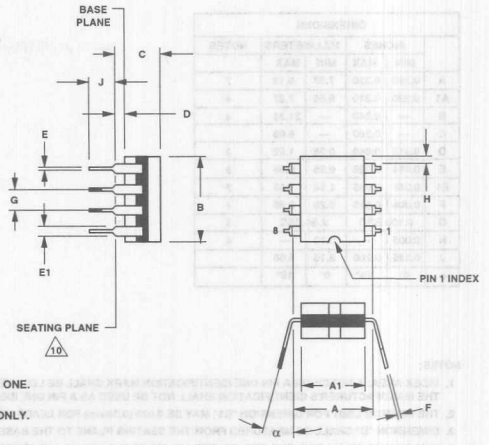
NOTES:

1. 'A1' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. LEADS SHALL BE COPLANAR WITHIN 0.004 IN. AT THE SEATING PLANE.
3. THE BASIC LEAD SPACING IS 0.050 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.004 IN. OF ITS EXACT TRUE POSITION.
4. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
5. DIMENSION 'F' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'F' MAXIMUM BY MORE THAN 0.003 IN. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.004 IN. AND 0.010 IN. FROM THE LEAD TIP.
7. 'C1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

Mechanical Drawings (cont'd)

8-PIN CERAMIC DIP ~ J PACKAGE SUFFIX

	DIMENSIONS				
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.290	0.320	7.37	8.13	7
A1	0.220	0.310	5.59	7.87	4
B	—	0.405	—	10.29	4
C	—	0.200	—	5.08	
D	0.015	0.060	0.38	1.52	3
E	0.014	0.026	0.36	0.66	8
E1	0.045	0.065	1.14	1.65	2
F	0.008	0.018	0.20	0.46	8
G	0.100 BSC		2.54 BSC		5
H	0.005	—	0.13	—	6
J	0.125	0.200	3.18	5.08	
α	0°	15°	0°	15°	

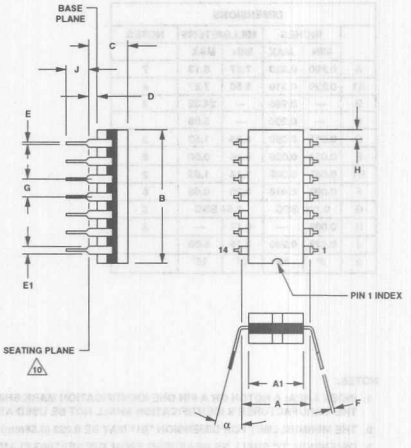


NOTES:

1. INDEX AREA: A NOTCH OR A PIN ONE IDENTIFICATION MARK SHALL BE LOCATED ADJACENT TO PIN ONE. THE MANUFACTURER'S IDENTIFICATION SHALL NOT BE USED AS A PIN ONE IDENTIFICATION MARK.
2. THE MINIMUM LIMIT FOR DIMENSION "E1" MAY BE 0.023 (0.58mm) FOR LEADS NUMBER 1, 4, 5 AND 8 ONLY.
3. DIMENSION "D" SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
4. THIS DIMENSION ALLOWS FOR OFF-CENTER LID, MENISCUS AND GLASS OVERRUN.
5. THE BASIC PIN SPACING IS 0.100 (2.54mm) BETWEEN CENTERLINES. EACH PIN CENTERLINE SHALL BE LOCATED WITHIN ±0.010 (0.25mm) OF ITS EXACT TRUE POSITION.
6. APPLIES TO ALL FOUR CORNERS (LEADS NUMBER 1, 4, 5 AND 8).
7. DIMENSION "A" SHALL BE MEASURED AT THE CENTERLINE OF THE LEADS WHEN $\alpha = 0°$.
8. THE MAXIMUM LIMITS OF DIMENSIONS "E" AND "F" SHALL BE MEASURED AT THE CENTER OF THE FLAT WHEN SOLDER DIP IS APPLIED.
9. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
10. THE SEATING PLANE IS LOCATED AT THE LOWEST POINT ON THE LEAD AT WHICH THE LEAD WIDTH EXCEEDS 0.040 (1.02mm) MINIMUM, EXCLUDING ANY HALF LEADS AT THE PACKAGE ENDS.

14-PIN CERAMIC DIP ~ J PACKAGE SUFFIX

	DIMENSIONS				
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.290	0.320	7.37	8.13	7
A1	0.220	0.310	5.59	7.87	4
B	—	0.785	—	19.94	4
C	—	0.200	—	5.08	
D	0.015	0.060	0.38	1.52	3
E	0.014	0.026	0.36	0.66	8
E1	0.045	0.065	1.14	1.65	2
F	0.008	0.018	0.20	0.46	8
G	0.100 BSC		2.54 BSC		5
H	0.005	—	0.13	—	6
J	0.125	0.200	3.18	5.08	
α	0°	15°	0°	15°	



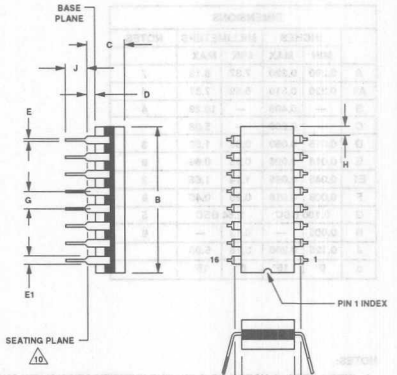
NOTES:

1. INDEX AREA: A NOTCH OR A PIN ONE IDENTIFICATION MARK SHALL BE LOCATED ADJACENT TO PIN ONE. THE MANUFACTURER'S IDENTIFICATION SHALL NOT BE USED AS A PIN ONE IDENTIFICATION MARK.
2. THE MINIMUM LIMIT FOR DIMENSION "E1" MAY BE 0.023 (0.58mm) FOR LEADS NUMBER 1, 7, 8 AND 14 ONLY.
3. DIMENSION "D" SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
4. THIS DIMENSION ALLOWS FOR OFF-CENTER LID, MENISCUS AND GLASS OVERRUN.
5. THE BASIC PIN SPACING IS 0.100 (2.54mm) BETWEEN CENTERLINES. EACH PIN CENTERLINE SHALL BE LOCATED WITHIN ±0.010 (0.25mm) OF ITS EXACT TRUE POSITION.
6. APPLIES TO ALL FOUR CORNERS (LEADS NUMBER 1, 7, 8 AND 14).
7. DIMENSION "A" SHALL BE MEASURED AT THE CENTERLINE OF THE LEADS WHEN $\alpha = 0°$.
8. THE MAXIMUM LIMITS OF DIMENSIONS "E" AND "F" SHALL BE MEASURED AT THE CENTER OF THE FLAT WHEN SOLDER DIP IS APPLIED.
9. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
10. THE SEATING PLANE IS LOCATED AT THE LOWEST POINT ON THE LEAD AT WHICH THE LEAD WIDTH EXCEEDS 0.040 (1.02mm) MINIMUM, EXCLUDING ANY HALF LEADS AT THE PACKAGE ENDS.

Mechanical Drawings (cont'd)

16-PIN CERAMIC DIP ~ J PACKAGE SUFFIX

	DIMENSIONS				
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.290	0.320	7.37	8.13	7
A1	0.220	0.310	5.59	7.87	4
B	—	0.840	—	21.34	4
C	—	0.200	—	5.08	
D	0.015	0.060	0.38	1.52	3
E	0.014	0.026	0.36	0.66	8
E1	0.045	0.065	1.14	1.65	2
F	0.008	0.018	0.20	0.46	8
G	0.100 BSC		2.54 BSC		5
H	0.005	—	0.13	—	6
J	0.125	0.200	3.18	5.08	
α	0°	15°	0°	15°	



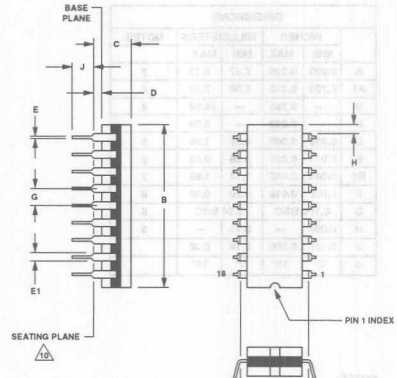
NOTES:

1. INDEX AREA: A NOTCH OR A PIN ONE IDENTIFICATION MARK SHALL BE LOCATED ADJACENT TO PIN ONE. THE MANUFACTURER'S IDENTIFICATION SHALL NOT BE USED AS A PIN ONE IDENTIFICATION MARK.
2. THE MINIMUM LIMIT FOR DIMENSION "E1" MAY BE 0.023 (0.58mm) FOR LEADS NUMBER 1, 8, 9 AND 16 ONLY.
3. DIMENSION "D" SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
4. THIS DIMENSION ALLOWS FOR OFF–CENTER LID, MENISCUS AND GLASS OVERRUN.
5. THE BASIC PIN SPACING IS 0.100 (2.54mm) BETWEEN CENTERLINES. EACH PIN CENTERLINE SHALL BE LOCATED WITHIN ±0.010 (0.25mm) OF ITS EXACT TRUE POSITION.
6. APPLIES TO ALL FOUR CORNERS (LEADS NUMBER 1, 8, 9 AND 16).
7. DIMENSION "A" SHALL BE MEASURED AT THE CENTERLINE OF THE LEADS WHEN α = 0°.
8. THE MAXIMUM LIMITS OF DIMENSIONS "E" AND "F" SHALL BE MEASURED AT THE CENTER OF THE FLAT WHEN SOLDER DIP IS APPLIED.
9. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.

10 THE SEATING PLANE IS LOCATED AT THE LOWEST POINT ON THE LEAD AT WHICH THE LEAD WIDTH EXCEEDS 0.040 (1.02mm) MINIMUM, EXCLUDING ANY HALF LEADS AT THE PACKAGE ENDS.

18-PIN CERAMIC DIP ~ J PACKAGE SUFFIX

	DIMENSIONS				
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.290	0.320	7.37	8.13	7
A1	0.220	0.310	5.59	7.87	4
B	—	0.960	—	24.38	4
C	—	0.200	—	5.08	
D	0.015	0.060	0.38	1.52	3
E	0.014	0.026	0.36	0.66	8
E1	0.045	0.065	1.14	1.65	2
F	0.008	0.018	0.20	0.46	8
G	0.100 BSC		2.54 BSC		5
H	0.005	—	0.13	—	6
J	0.125	0.200	3.18	5.08	
α	0°	15°	0°	15°	



NOTES:

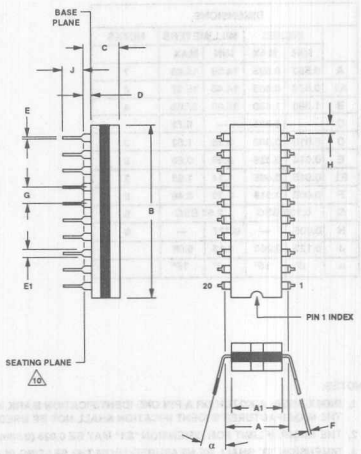
1. INDEX AREA: A NOTCH OR A PIN ONE IDENTIFICATION MARK SHALL BE LOCATED ADJACENT TO PIN ONE. THE MANUFACTURER'S IDENTIFICATION SHALL NOT BE USED AS A PIN ONE IDENTIFICATION MARK.
2. THE MINIMUM LIMIT FOR DIMENSION "E1" MAY BE 0.023 (0.58mm) FOR LEADS NUMBER 1, 9, 10 AND 18 ONLY.
3. DIMENSION "D" SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
4. THIS DIMENSION ALLOWS FOR OFF–CENTER LID, MENISCUS AND GLASS OVERRUN.
5. THE BASIC PIN SPACING IS 0.100 (2.54mm) BETWEEN CENTERLINES. EACH PIN CENTERLINE SHALL BE LOCATED WITHIN ±0.010 (0.25mm) OF ITS EXACT TRUE POSITION.
6. APPLIES TO ALL FOUR CORNERS (LEADS NUMBER 1, 9, 10 AND 18).
7. DIMENSION "A" SHALL BE MEASURED AT THE CENTERLINE OF THE LEADS WHEN α = 0°.
8. THE MAXIMUM LIMITS OF DIMENSIONS "E" AND "F" SHALL BE MEASURED AT THE CENTER OF THE FLAT WHEN SOLDER DIP IS APPLIED.
9. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.

10 THE SEATING PLANE IS LOCATED AT THE LOWEST POINT ON THE LEAD AT WHICH THE LEAD WIDTH EXCEEDS 0.040 (1.02mm) MINIMUM, EXCLUDING ANY HALF LEADS AT THE PACKAGE ENDS.

Mechanical Drawings (cont'd)

20-PIN CERAMIC DIP ~ J PACKAGE SUFFIX

DIMENSIONS					
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.290	0.320	7.37	8.13	7
A1	0.220	0.310	5.59	7.87	4
B	—	0.840	—	21.34	4
C	—	0.200	—	5.08	
D	0.015	0.060	0.38	1.52	3
E	0.014	0.026	0.36	0.66	8
E1	0.045	0.065	1.14	1.65	2
F	0.008	0.018	0.20	0.46	8
G	0.100 BSC		2.54 BSC		5
H	0.005	—	0.13	—	6
J	0.125	0.200	3.18	5.08	
α	0°	15°	0°	15°	



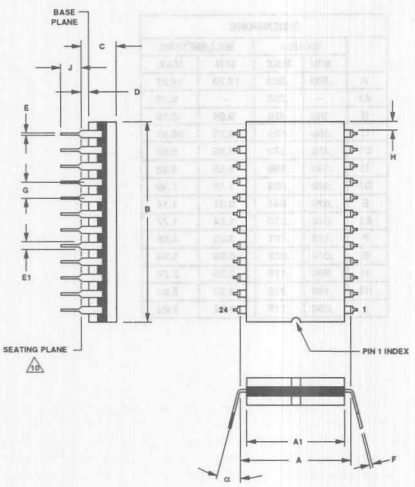
NOTES:

1. INDEX AREA: A NOTCH OR A PIN ONE IDENTIFICATION MARK SHALL BE LOCATED ADJACENT TO PIN ONE. THE MANUFACTURER'S IDENTIFICATION SHALL NOT BE USED AS A PIN ONE IDENTIFICATION MARK.
2. THE MINIMUM LIMIT FOR DIMENSION "E1" MAY BE 0.023 (0.58mm) FOR LEADS NUMBER 1, 10, 11 AND 20 ONLY.
3. DIMENSION "D" SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
4. THIS DIMENSION ALLOWS FOR OFF–CENTER LID, MENISCUS AND GLASS OVERRUN.
5. THE BASIC PIN SPACING IS 0.100 (2.54mm) BETWEEN CENTERLINES. EACH PIN CENTERLINE SHALL BE LOCATED WITHIN ±0.010 (0.25mm) OF ITS EXACT TRUE POSITION.
6. APPLIES TO ALL FOUR CORNERS (LEADS NUMBER 1, 10, 11 AND 20).
7. DIMENSION "A" SHALL BE MEASURED AT THE CENTERLINE OF THE LEADS WHEN α = 0°.
8. THE MAXIMUM LIMITS OF DIMENSIONS "E" AND "F" SHALL BE MEASURED AT THE CENTER OF THE FLAT WHEN SOLDER DIP IS APPLIED.
9. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY,

10 THE SEATING PLANE IS LOCATED AT THE LOWEST POINT ON THE LEAD AT WHICH THE LEAD WIDTH EXCEEDS 0.040 (1.02mm) MINIMUM, EXCLUDING ANY HALF LEADS AT THE PACKAGE ENDS.

24-PIN CERAMIC DIP ~ J PACKAGE SUFFIX

DIMENSIONS					
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.590	0.625	14.99	15.88	7
A1	0.515	0.605	13.08	15.37	4
B	1.180	1.260	29.97	32.00	4
C	—	0.225	—	5.72	
D	0.015	0.055	0.38	1.40	3
E	0.014	0.026	0.36	0.66	8
E1	0.045	0.065	1.14	1.65	2
F	0.008	0.018	0.20	0.46	8
G	0.100 BSC		2.54 BSC		5
H	0.005	0.065	0.127	1.65	6
J	0.125	0.200	3.18	5.08	
α	0°	15°	0°	15°	



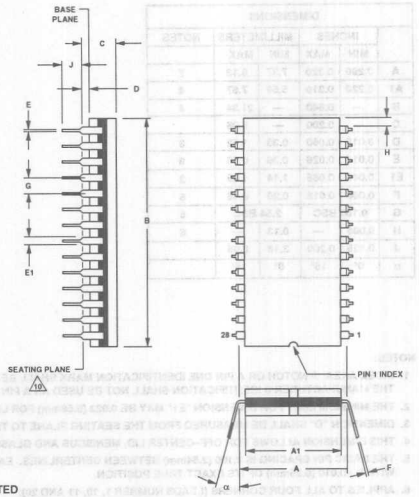
NOTES:

1. INDEX AREA: A NOTCH OR A PIN ONE IDENTIFICATION MARK SHALL BE LOCATED ADJACENT TO PIN ONE. THE MANUFACTURER'S IDENTIFICATION SHALL NOT BE USED AS A PIN ONE IDENTIFICATION MARK.
2. THE MINIMUM LIMIT FOR DIMENSION "E1" MAY BE 0.023 (0.58mm) FOR LEADS NUMBER 1, 12, 13 AND 24 ONLY.
3. DIMENSION "D" SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
4. THIS DIMENSION ALLOWS FOR OFF–CENTER LID, MENISCUS AND GLASS OVERRUN.
5. THE BASIC PIN SPACING IS 0.100 (2.54mm) BETWEEN CENTERLINES. EACH PIN CENTERLINE SHALL BE LOCATED WITHIN ±0.010 (0.25mm) OF ITS EXACT TRUE POSITION.
6. APPLIES TO ALL FOUR CORNERS (LEADS NUMBER 1, 12, 13 AND 24).
7. DIMENSION "A" SHALL BE MEASURED AT THE CENTERLINE OF THE LEADS WHEN α = 0°.
8. THE MAXIMUM LIMITS OF DIMENSIONS "E" AND "F" SHALL BE MEASURED AT THE CENTER OF THE FLAT WHEN SOLDER DIP IS APPLIED.
9. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.

10 THE SEATING PLANE IS LOCATED AT THE LOWEST POINT ON THE LEAD AT WHICH THE LEAD WIDTH EXCEEDS 0.040 (1.02mm) MINIMUM, EXCLUDING ANY HALF LEADS AT THE PACKAGE ENDS.

28-PIN CERAMIC DIP ~ J PACKAGE SUFFIX

	DIMENSIONS				
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.590	0.625	14.99	15.88	7
A1	0.570	0.605	14.48	15.37	4
B	1.380	1.460	35.05	37.08	4
C	—	0.225	—	5.72	
D	0.015	0.060	0.38	1.52	3
E	0.014	0.026	0.36	0.66	8
E1	0.045	0.065	1.14	1.65	2
F	0.008	0.018	0.20	0.46	8
G	0.100 BSC		2.54 BSC		5
H	0.005	—	0.127	—	6
J	0.125	0.200	3.18	5.08	
α	0°	15°	0°	15°	



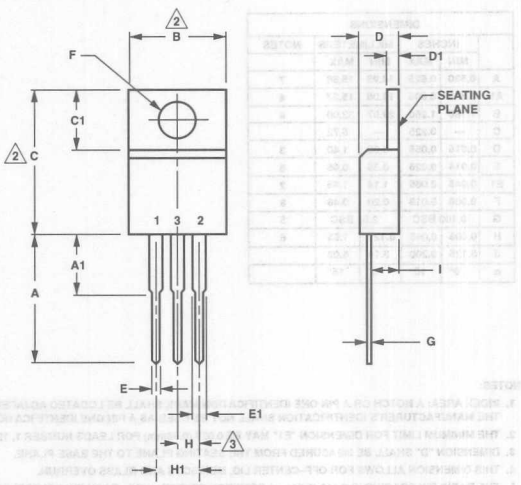
NOTES:

1. INDEX AREA: A NOTCH OR A PIN ONE IDENTIFICATION MARK SHALL BE LOCATED ADJACENT TO PIN ONE. THE MANUFACTURER'S IDENT IFICATION SHALL NOT BE USED AS A PIN ONE IDENTIFICATION MARK.
2. THE MINIMUM LIMIT FOR DIMENSION "E1" MAY BE 0.023 (0.58mm) FOR LEADS NUMBER 1, 14, 15 AND 28 ONLY.
3. DIMENSION "D" SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
4. THIS DIMENSION ALLOWS FOR OFF–CENTER LID, MENISCUS AND GLASS OVERRUN.
5. THE BASIC PIN SPACING IS 0.100 (2.54mm) BETWEEN CENTERLINES. EACH PIN CENTERLINE SHALL BE LOCATED WITHIN ±0.010 (0.25mm) OF ITS EXACT TRUE POSITION.
6. APPLIES TO ALL FOUR CORNERS (LEADS NUMBER 1, 14, 15 AND 28).
7. DIMENSION "A" SHALL BE MEASURED AT THE CENTERLINE OF THE LEADS WHEN $\alpha = 0°$.
8. THE MAXIMUM LIMITS OF DIMENSIONS "E" AND "F" SHALL BE MEASURED AT THE CENTER OF THE FLAT WHEN SOLDER DIP IS APPLIED.
9. CONTROLLING DIMENSION INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.

10 THE SEATING PLANE IS LOCATED AT THE LOWEST POINT ON THE LEAD AT WHICH THE LEAD WIDTH EXCEEDS 0.040 (1.02mm) MINIMUM, EXCLUDING ANY HALF LEADS AT THE PACKAGE ENDS.

3-PIN TO-220 PLASTIC ~ T PACKAGE SUFFIX

	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.500	.562	12.70	14.27
A1	–	.250	–	6.35
B	.380	.420	9.66	10.66
C	.560	.625	14.23	15.87
C1	.230	.270	5.85	6.85
D	.140	.190	3.56	4.82
D1	.045	.055	1.14	1.39
E	.020	.045	0.51	1.14
E1	.045	.070	1.14	1.77
F	.139	.161	3.53	4.09
G	.014	.022	0.36	0.56
H	.090	.110	2.29	2.79
H1	.190	.210	4.83	5.33
I	.080	.115	2.04	2.92



NOTES:

1. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.

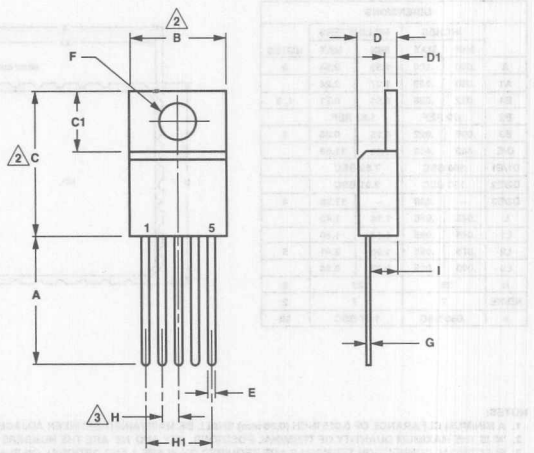
2 'B' AND 'C' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.

3 THE BASIC LEAD SPACING IS 0.100 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.010 IN. OF ITS EXACT TRUE POSITION.

Mechanical Drawings (cont'd)

5-PIN TO-220 PLASTIC ~ T PACKAGE SUFFIX

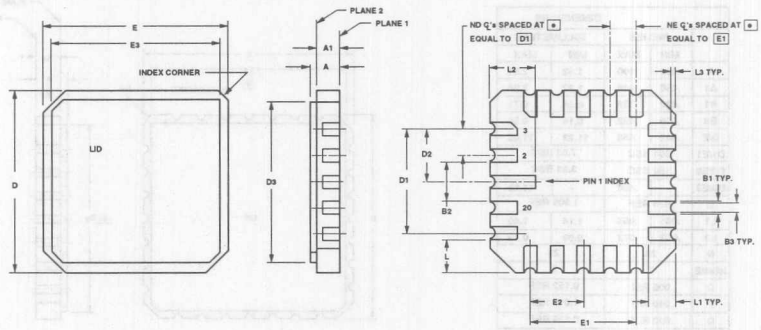
	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.500	.580	12.70	14.73
B	.380	.420	9.65	10.67
C	.560	.650	14.22	16.51
C1	.230	.270	5.84	6.86
D	.140	.190	3.56	4.83
D1	.045	.055	1.14	1.40
E	.020	.045	0.51	1.14
F	.139	.161	3.53	4.09
G	.014	.022	0.36	0.56
H	.057	.077	1.45	1.96
H1	.258	.278	6.55	7.06
I	.080	.115	2.03	2.92



NOTES:
1. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
2. 'B' AND 'C' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
3. THE BASIC LEAD SPACING IS 0.067 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.010 IN. OF ITS EXACT TRUE POSITION.

20-PIN CERAMIC LEADLESS SURFACE MOUNT ~ L PACKAGE SUFFIX

	DIMENSIONS				
	INCHES		MILLIMETERS		
	MIN	MAX	MIN	MAX	NOTES
A	.060	.100	1.52	2.54	6
A1	.050	.088	1.27	2.24	
B1	.022	.028	0.56	0.71	1, 3
B2	.072 REF.		1.83 REF.		
B3	.006	.022	0.15	0.56	8
D/E	.342	.358	8.69	9.09	
D1/E1	.200 BSC		5.08 BSC		
D2/E2	.100 BSC		2.54 BSC		
D3/E3	–	.358	–	9.09	4
L	.045	.055	1.14	1.40	
L1	.045	.055	1.14	1.40	
L2	.075	.095	1.90	2.41	5
L3	.003	.015	0.08	0.38	
N	20		20		2
ND/NE	5		5		2
e	.050 BSC		1.27 BSC		10

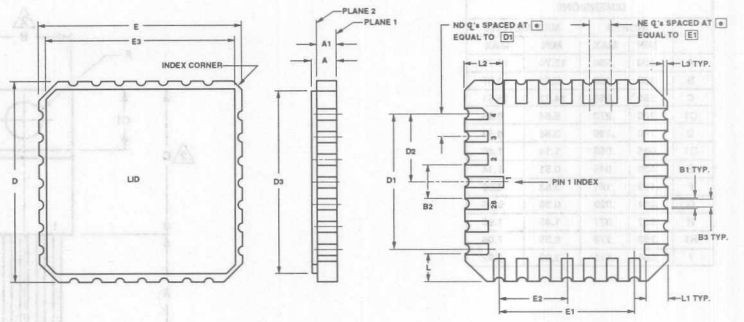


NOTES:
1. A MINIMUM CLEARANCE OF 0.015 INCH (0.38 mm) SHALL BE MAINTAINED BETWEEN ADJACENT TERMINALS.
2. 'N' IS THE MAXIMUM QUANTITY OF TERMINAL POSITIONS. 'ND' AND 'NE' ARE THE NUMBERS OF TERMINALS ALONG THE SIDES OF LENGTH 'D' AND 'E' RESPECTIVELY.
3. ELECTRICAL CONNECTION TERMINALS ARE REQUIRED ON PLANE 1 AND OPTIONAL ON PLANE 2. HOWEVER, IF PLANE 2 HAS SUCH TERMINALS THEY SHALL BE ELECTRICALLY CONNECTED TO OPPOSING TERMINALS ON PLANE 1.
4. A MINIMUM CLEARANCE OR 0.015 INCH (0.38 mm) SHALL BE MAINTAINED BETWEEN A METAL LID AND OTHER METAL FEATURES (E.G., PLANE 2 TERMINALS, METALLIZED CASTELLATIONS, ETC.) THE LID SHALL NOT EXTEND BEYOND THE EDGES OF THE BODY.
5. THE INDEX FEATURE FOR NUMBER 1 TERMINAL IDENTIFICATION, OPTIONAL ORIENTATION OR HANDLING PURPOSES SHALL BE WITHIN THE AREA DEFINED BY DIMENSIONS 'B2' AND 'L2' ON PLANE 1.
6. DIMENSION 'A' CONTROLS THE OVERALL PACKAGE THICKNESS.
7. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
8. CASTELLATIONS ARE REQUIRED ON BOTTOM TWO LAYERS. CASTELLATIONS IN THE TOP LAYER ARE OPTIONAL.
9. WHEN SOLDER DIP LEAD FINISH APPLIES, SOLDER BUMP HEIGHT SHALL NOT EXCEED 0.007 INCHES AND SOLDER BUMP COPLANARITY SHALL NOT EXCEED 0.006 INCHES.
10. THE BASIC TERMINAL SPACING IS 0.050 INCHES BETWEEN CENTERLINES. EACH TERMINAL CENTERLINE SHALL BE LOCATED WITHIN ±0.004 INCHES OF ITS EXACT TRUE POSITION.

Mechanical Drawings (cont'd)

28-PIN CERAMIC LEADLESS SURFACE MOUNT ~ L PACKAGE SUFFIX

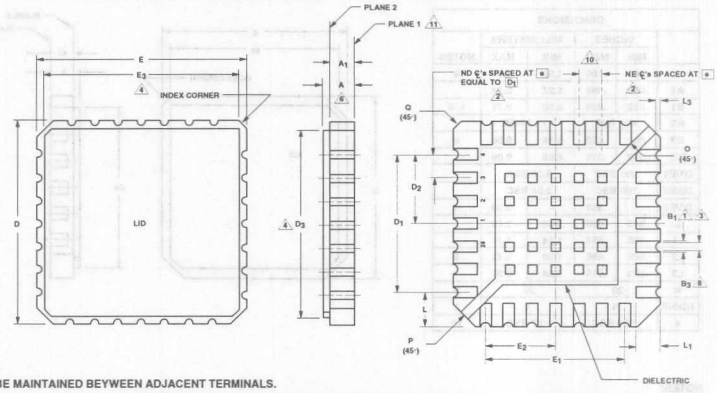
DIMENSIONS					
	INCHES		MILLIMETERS		
	MIN	MAX	MIN	MAX	NOTES
A	.060	.100	1.52	2.54	6
A1	.050	.088	1.27	2.24	
B1	.022	.028	0.56	0.71	1, 3
B2	.072 REF.		1.83 REF.		
B3	.006	.022	0.15	0.56	8
D/E	.442	.460	11.23	11.68	
D1/E1	.300 BSC		7.62 BSC		
D2/E2	.150 BSC		3.81 BSC		
D3/E3	–	.460	–	11.68	4
L	.045	.055	1.14	1.40	
L1	.045	.055	1.14	1.40	
L2	.075	.095	1.90	2.41	5
L3	.003	.015	0.08	0.38	
N	28		28		2
ND/NE	7		7		2
e	.050 BSC		1.27 BSC		10



NOTES:
1. A MINIMUM CLEARANCE OF 0.015 INCH (0.38 mm) SHALL BE MAINTAINED BETWEEN ADJACENT TERMINALS.
2. 'N' IS THE MAXIMUM QUANTITY OF TERMINAL POSITIONS. 'ND' AND 'NE' ARE THE NUMBERS OF TERMINALS ALONG THE SIDES OF LENGTH 'D' AND 'E' RESPECTIVELY.
3. ELECTRICAL CONNECTION TERMINALS ARE REQUIRED ON PLANE 1 AND OPTIONAL ON PLANE 2. HOWEVER, IF PLANE 2 HAS SUCH TERMINALS THEY SHALL BE ELECTRICALLY CONNECTED TO OPPOSING TERMINALS ON PLANE 1.
4. A MINIMUM CLEARANCE OR 0.015 INCH (0.38 mm) SHALL BE MAINTAINED BETWEEN A METAL LID AND OTHER METAL FEATURES (E.G., PLANE 2 TERMINALS, METALLIZED CASTELLATIONS, ETC.) THE LID SHALL NOT EXTEND BEYOND THE EDGES OF THE BODY.
5. THE INDEX FEATURE FOR NUMBER 1 TERMINAL IDENTIFICATION, OPTIONAL ORIENTATION OR HANDLING PURPOSES SHALL BE WITHIN THE AREA DEFINED BY DIMENSIONS 'B2' AND 'L2' ON PLANE 1.
6. DIMENSION 'A' CONTROLS THE OVERALL PACKAGE THICKNESS.
7. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
8. CASTELLATIONS ARE REQUIRED ON BOTTOM TWO LAYERS. CASTELLATIONS IN THE TOP LAYER ARE OPTIONAL.
9. WHEN SOLDER DIP LEAD FINISH APPLIES, SOLDER BUMP HEIGHT SHALL NOT EXCEED 0.007 INCHES AND SOLDER BUMP COPLANARITY SHALL NOT EXCEED 0.006 INCHES.
10. THE BASIC TERMINAL SPACING IS 0.050 INCHES BETWEEN CENTERLINES. EACH TERMINAL CENTERLINE SHALL BE LOCATED WITHIN ±0.004 INCHES OF ITS EXACT TRUE POSITION.

28-PIN CERAMIC LEADLESS SURFACE MOUNT ~ LP PACKAGE SUFFIX

DIMENSIONS				
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.060	.100	1.52	2.54
A1	.050	.088	1.27	2.24
B1	.022	.028	0.56	0.71
B3	.006	.022	0.15	0.56
D/E	.442	.458	11.23	11.63
D1/E1	.300 BSC		7.62 BSC	
D2/E2	.150 BSC		3.81 BSC	
D3/E3	–	.460	–	11.68
L	.075 REF		1.905 REF	
L1	.045	.055	1.14	1.40
L3	.003	.013	0.08	0.33
N	28		28	
ND/NE	7		7	
O	.006 REF		0.152 REF	
P	.040 REF		1.016 REF	
Q	.020 REF		0.508 REF	
e	.050 BSC		1.27 BSC	

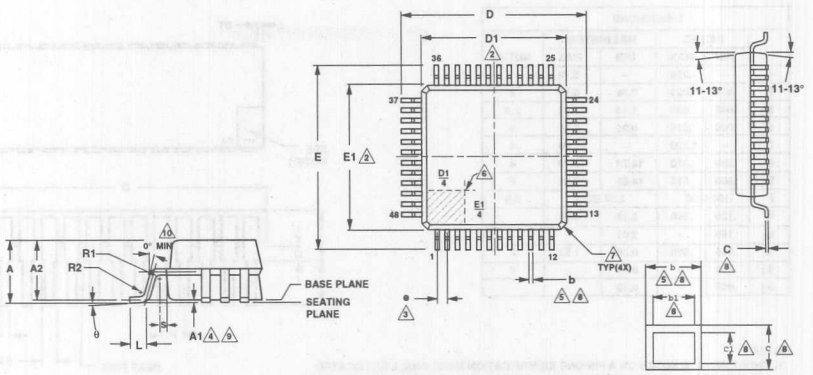


NOTES:
1. A MINIMUM CLEARANCE OF 0.015 INCH (0.38mm) SHALL BE MAINTAINED BEYWEEN ADJACENT TERMINALS.
2. 'N' IS THE MAXIMUM QUANTITY OF TERMINAL POSITIONS, 'ND' AND 'NE' ARE THE NUMBERS OF TERMINALS ALONG THE SIDES OF LENGTH 'D' AND 'E' RESPECTIVELY.
3. ELECTRICAL CONNECTION TERMINAL ARE REQUIRED ON PLANE 1 AND OPTIONAL ON PLANE 2. HOWEVER, IF PLANE 2 HAS SUCH TERMINALS THEY SHALL BE ELECTRICALLY CONNECTED TO THE OPPOSING TERMINALS ON PLANE1.
4. A MINIMUM CLEARANCE OR 0.015 INCH (0.38mm) SHALL BE MAINTAINED BETWEEN A METAL LID AND OTHER METAL FEATURES (E.G.,PLANE 2 TERMINALS, METALLIZED CASTELLATIONS, ETC.) THE LID SHALL NOT EXTEND BEYOND THE EDGES OF THE BODY.
5. THE INDEX FEATURE FOR NUMBER 1 TERMINAL IDENTIFICATION ON PLANE 1 IS DEFINED BY DELETION OF THE THERMAL PAD AJACENT TO TERMINAL 1.
6. DIMENSION 'A' CONTROLS THE OVERALL PACKAGE THICKNESS.
7. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
8. CASTELLATIONS ARE REQUIRED ON BOTTOM TWO LAYERS. CASTELLATIONS IN THE TOP LAYER ARE OPTIONAL.
9. WHEN SOLDER DIP LEAD FINISH APPLIES, SOLDER BUMP HEIGHT SHALL NOT EXCEED 0.007 INCHES AND SOLDER BUMP COPLANARITY SHALL NOT EXCEED 0.006 INCHES.
10. THE BASIC TERMINAL SPACING IS 0.050 INCHES BETWEEN CENTERLINES. EACH TERMINAL CENTERLINE SHALL BE LOCATED WITHIN ±0.004 INCHES OF ITS EXACT TRUE POSITION.
11. PLANE 1 IS THE HEAT RADIATION SURFACE. THIS SURFACE IS METALIZED WITH A CHECKERBOARD PATTERN OF THERMAL CONDUCTION PADS. THE PAD CENTERLINES ARE ALIGNED WITH TERMINAL CENTERLINES. THERMAL PADS ARE NOT ELECTRICALLY TIED TO ANY TERMINAL.

Mechanical Drawings (cont'd)

48-PIN LQFP ~ FQ PACKAGE SUFFIX

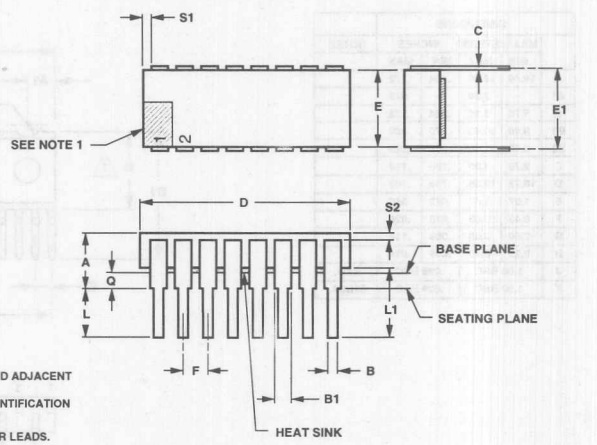
DIMENSIONS				
	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	–	1.60	–	.063
A1	0.05	0.15	.002	.006
A2	1.35	1.45	.053	.057
b	0.17	0.27	.007	.011
b1	0.17	0.23	.007	.009
C	0.09	0.20	.003	.008
C1	0.09	0.16	.003	.006
D	9.00 BSC		.354 BSC	
D1	7.00 BSC		.276 BSC	
E	9.00 BSC		.354 BSC	
E1	7.00 BSC		.276 BSC	
e	0.50 BSC		.020 BSC	
L	0.45	0.75	.018	.030
R1	0.08	–	.003	–
R2	0.08	0.20	.003	.008
S	0.20	–	.008	–



NOTES:
1. CONTROLLING DIMENSION: MILLIMETERS. INCHES SHOWN FOR REFERENCE ONLY.
2. 'D1'AND 'E1' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.25mm PER SIDE. 'D1'AND 'E1' INCLUDE MOLD MISMATCH.
3. THE BASIC LEAD SPACING IS 0.50mm BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.10mm OF ITS EXACT TRUE POSITION.
4. LEADS SHALL BE COPLANAR WITHIN 0.08mm AT THE SEATING PLANE.
5. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'b' MAXIMUM BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm.
6. DETAILS OF PIN1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
9. 'A1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).
10. THE TOP PACKAGE BODY MAY BE SMALLER THAN THE BOTTOM PACKAGE BODY SIZE BY AS MUCH AS 0.15mm.

16-PIN SIDEBRAZE DIP ~ SP PACKAGE SUFFIX

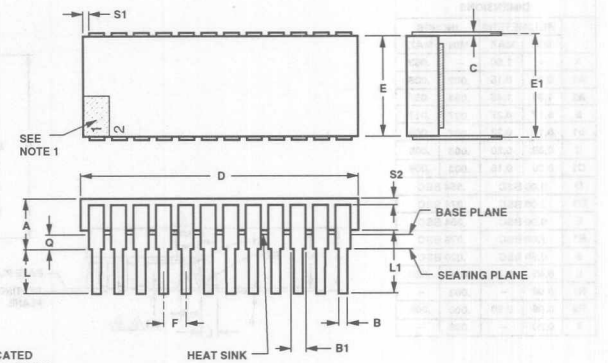
DIMENSIONS					
	INCHES		MILLIMETERS		
	MIN	MAX	MIN	MAX	NOTES
A	–	.200	–	5.08	
B	.014	.023	0.36	0.58	8
B_1	.045	.065	1.14	1.65	2,8
C	.008	.015	0.20	0.38	8
D	–	.840	–	21.34	4
E	.220	.310	5.59	7.78	4
E_1	.290	.320	7.37	8.13	7
F	.100 BSC		2.54 BSC		5,9
L	.125	.200	3.18	5.08	
L_1	.150	–	3.81	–	
Q	.015	.060	0.38	1.52	3
S_1	.005	–	0.13	–	6
S_2	.005	–	0.13	–	



NOTES:
1. INDEX AREA; A NOTCH OR A PIN ONE IDENTIFICATION MARK SHALL BE LOCATED ADJACENT TO ONE AND SHALL BE LOCATED WITHIN THE SHADED AREA SHOWN. THE MANUFACTURER'S IDENTIFICATION SHALL NOT BE USED AS A PIN ONE IDENTIFICATION MARK.
2. THE MINIMUM LIMIT FOR DIMENSION 'B1' MAY BE 0.023 IN. (0.58mm) FOR CORNER LEADS.
3. DIMENSION 'Q' SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
4. THIS DIMENSION ALLOWS FOR OFF-CENTER LID, MENISCUS, AND GLASS OVERRUN.
5. THE BASIC LEAD SPACING IS 0.100 IN. (2.54mm) BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.010 IN. (0.25mm) OF ITS EXACT TRUE POSITION.
6. MEASURE ALL FOUR CORNERS.
7. E1 SHALL BE MEASURED AT THE CENTERLINE OF THE LEADS.
8. ALL LEADS - INCREASE MAXIMUM LIMIT BY 0.003 IN.(0.08mm) MEASURED AT THE CENTER OF THE FLAT, WHEN SOLDER DIP IS APPLIED.
9. 14 SPACES
10. BRAZE FILLET SHALL BE CONCAVE.
11. CONTROLLING DIMENSIONS: INCHES. MILLIMETERS SHOWN FOR REFERENCEONLY.

24-PIN SIDEBRAZE DIP ~ SP PACKAGE SUFFIX

DIMENSIONS					
	INCHES		MILLIMETERS		
	MIN	MAX	MIN	MAX	NOTES
A	–	.225	–	5.72	
B	.014	.023	0.36	0.58	8
B_1	.045	.065	1.14	1.65	2,8
C	.008	.015	0.20	0.38	8
D	–	1.220	–	30.99	4
E	.580	.610	14.73	15.49	4
E_1	.585	.615	14.86	15.62	7
F	.100 BSC		2.54 BSC		5,9
L	.125	.200	3.18	5.08	
L_1	.150	–	3.81	–	
Q	.015	.060	0.38	1.52	3
S_1	.005	–	0.13	–	6
S_2	.005	–	0.13	–	

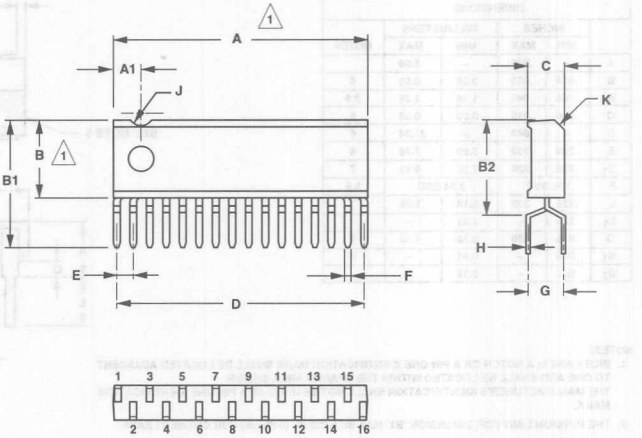


NOTES:

1. INDEX AREA; A NOTCH OR A PIN ONE IDENTIFICATION MARK SHALL BE LOCATED ADJACENT TO PIN ONE AND SHALL BE LOCATED WITHIN THE SHADED AREA SHOWN. THE MANUFACTURER'S IDENTIFICATION SHALL NOT BE USED AS A PIN ONE IDENTIFICATION MARK.
2. THE MINIMUM LIMIT FOR DIMENSION 'B1' MAY BE 0.023 IN.(0.58mm) FOR CORNER LEADS.
3. DIMENSION "Q" SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
4. THIS DIMENSION ALLOWS FOR OFF-CENTER LID, MENISCUS, AND GLASS OVERRUN.
5. THE BASIC LEAD SPACING IS 0.100 IN.(2.54mm) BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.010 IN. (0.25mm) OF ITS EXACT TRUE POSITION.
6. MEASURE ALL FOUR CORNERS.
7. E1 SHALL BE MEASURED AT THE CENTERLINE OF THE LEADS.
8. ALL LEADS - INCREASE MAXIMUM LIMIT BY 0.003 IN. (0.08mm) MEASURED AT THE CENTER OF THE FLAT, WHEN SOLDER DIP IS APPLIED.
9. 22 SPACES
10. BRAZE FILLET SHALL BE CONCAVE.
11. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.

16-PIN ZIG-ZAG INLINE ~ Z PACKAGE SUFFIX

DIMENSIONS					
	MILLIMETERS		INCHES		NOTES
	MIN	MAX	MIN	MAX	
A	19.40	19.60	.764	.772	
A1	–	2.00	–	.079	
B	5.70	5.90	.224	.232	
B1	9.40	10.40	.370	.409	
B2	6.50	7.50	.256	.295	
C	2.70	2.90	.106	.114	
D	18.75	19.35	.738	.762	
E	1.07	1.47	.042	.058	
F	0.45	0.65	.018	.026	
G	2.50	3.00	.098	.118	
H	0.23	0.35	.009	.014	
J	1.00 BSC		.039 BSC		RAD.
K	1.00 BSC		.039 BSC		CHAM.



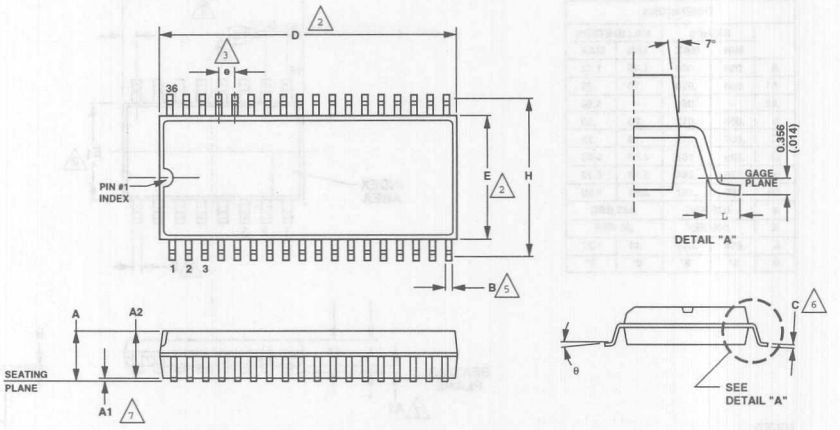
NOTES:

1. DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15mm (0.006 IN.) PER SIDE.

Mechanical Drawings (cont'd)

36-PIN QSOP ~ MWP PACKAGE SUFFIX

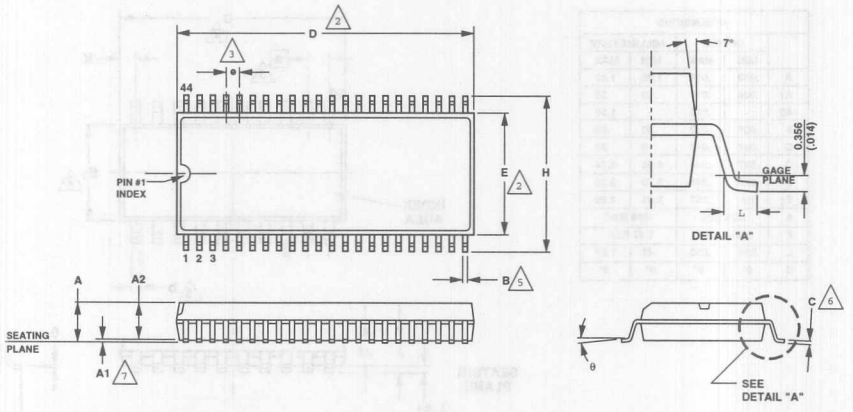
SYMBOL	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.093	.104	2.35	2.65
A1	.004	.012	0.10	0.30
A2	.092 TYP		2.34 TYP	
B	.011	.015	0.28	0.39
C	.006	.0125	0.15	0.32
D	.598	.614	15.20	15.60
E	.291	.299	7.40	7.60
e	.031 BSC		0 .80 BSC	
H	.394	.419	10.00	10.65
L	.016	.050	0.40	1.27
θ	0°	8°	0°	8°



NOTES:
1. CONTROLLING DIMENSION: INCHES. MILLIMETERS CONTROL LEAD PITCH ONLY.
2. 'D' AND 'E' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15mm PER SIDE.
3. THE BASIC LEAD SPACING IS 0.80mm BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.10mm OF ITS EXACT TRUE POSITION.
4. LEADS SHALL BE COPLANAR WITHIN 0.10mm AT THE SEATING PLANE.
5. DIMENSION 'B' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'B' MAXIMUM BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
7. 'A1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

44-PIN QSOP ~ MWP PACKAGE SUFFIX

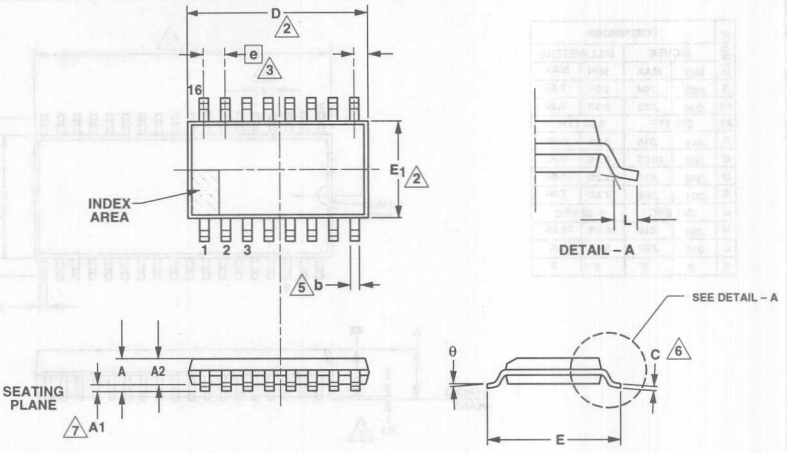
SYMBOL	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.093	.104	2.35	2.65
A1	.004	.012	0.10	0.30
A2	.092 TYP		2.34 TYP	
B	.011	.015	0.28	0.39
C	.006	.0125	0.15	0.32
D	.697	.712	17.70	18.10
E	.291	.299	7.40	7.60
e	.031 BSC		0 .80 BSC	
H	.394	.419	10.00	10.65
L	.016	.050	0.40	1.27
θ	0°	8°	0°	8°



NOTES:
1. CONTROLLING DIMENSION: INCHES. MILLIMETERS CONTROL LEAD PITCH ONLY.
2. 'D' AND 'E' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15mm PER SIDE.
3. THE BASIC LEAD SPACING IS 0.80mm BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.10mm OF ITS EXACT TRUE POSITION.
4. LEADS SHALL BE COPLANAR WITHIN 0.10mm AT THE SEATING PLANE.
5. DIMENSION 'B' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'B' MAXIMUM BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
7. 'A1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

16-PIN SSOP ~ M PACKAGE SUFFIX

DIMENSIONS				
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.053	.069	1.35	1.42
A1	.004	.010	.10	.25
A2	–	.059	–	1.50
b	.008	.012	.20	.30
C	.007	.010	.18	.25
D	.189	.197	4.80	5.00
E	.228	.244	5.79	6.20
E_1	.150	.157	3.81	3.99
e	.025 BSC		.635 BSC	
K	.009 REF		.23 REF	
L	.016	.050	.41	1.27
θ	0°	8°	0°	8°

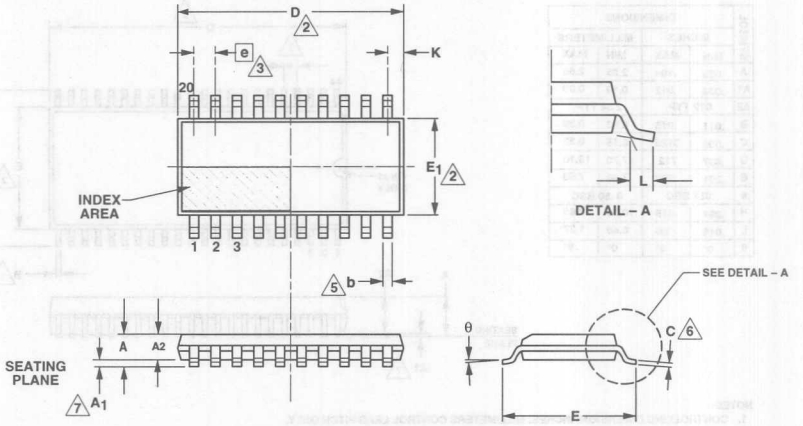


NOTES:

1. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
2. 'D' AND 'E_1' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
3. THE BASIC LEAD SPACING IS 0.025 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.004 IN. OF ITS EXACT TRUE POSITION.
4. LEADS SHALL BE COPLANAR WITHIN 0.004 IN. AT THE SEATING PLANE.
5. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'b' MAXIMUM BY MORE THAN 0.003 IN. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.004 IN. AND 0.010 IN. FROM THE LEAD TIP.
7. 'A1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

20-PIN SSOP ~ M PACKAGE SUFFIX

DIMENSIONS				
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.053	.069	1.35	1.42
A_1	.004	.010	.10	.25
A2	–	.059	–	1.50
b	.008	.012	.20	.30
C	.007	.010	.18	.25
D	.337	.344	8.56	8.74
E	.228	.244	5.79	6.20
E_1	.150	.157	3.81	3.99
e	.025 BSC		.635 BSC	
K	.058 REF		1.47 REF	
L	.016	.050	.41	1.27
θ	0°	8°	0°	8°



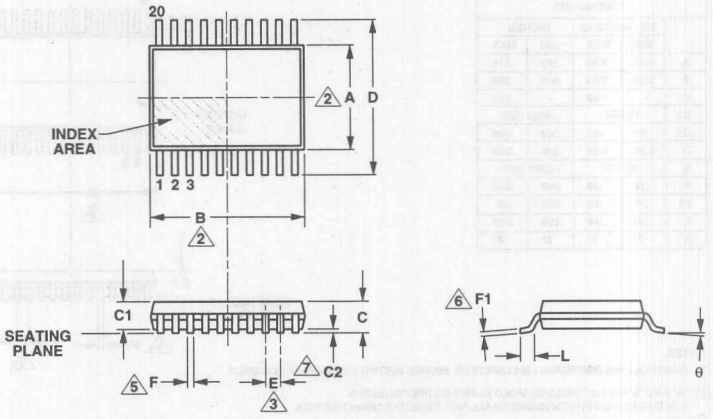
NOTES:

1. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
2. 'D' AND 'E_1' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
3. THE BASIC LEAD SPACING IS 0.025 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.004 IN. OF ITS EXACT TRUE POSITION.
4. LEADS SHALL BE COPLANAR WITHIN 0.004 IN. AT THE SEATING PLANE.
5. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED "b" MAXIMUM BY MORE THAN 0.003 IN. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.004 IN. AND 0.010 IN. FROM THE LEAD TIP.
7. 'A1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

Mechanical Drawings (cont'd)

20-PIN TSSOP ~ PW PACKAGE SUFFIX

DIMENSIONS				
	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.30	4.48	.169	.176
B	6.40	6.60	.252	.260
C	–	1.10	–	.043
C1	.90 REF.		.0354 REF.	
C2	.05	.15	.002	.006
D	6.25	6.50	.246	.256
E	.65 BSC		.0256 BSC	
F	.18	.30	.007	.012
F1	.09	.18	.003	.007
L	.50	.70	.020	.028
θ	0°	8°	0°	8°

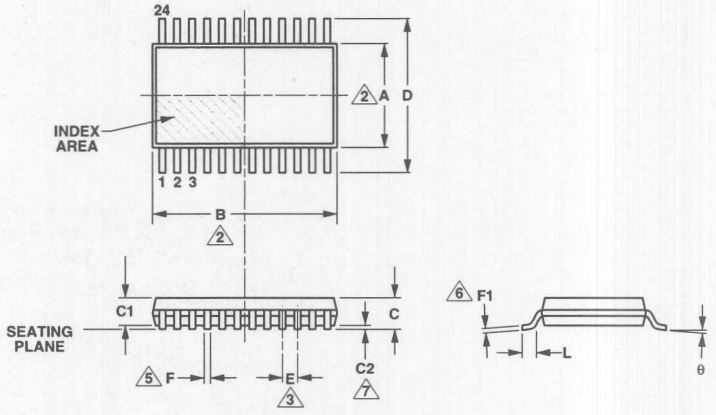


NOTES:

1. CONTROLLING DIMENSION: MILLIMETERS. INCHES SHOWN FOR REFERENCE ONLY.
2. 'A' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15mm PER SIDE.
3. THE BASIC LEAD SPACING IS 0.65mm BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.10mm OF ITS EXACT TRUE POSITION.
4. LEADS SHALL BE COPLANAR WITHIN 0.08mm AT THE SEATING PLANE.
5. DIMENSION 'F' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'F' MAXIMUM BY MORE THAN 0.08mm.
   DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
7. 'C2' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

24-PIN TSSOP ~ PW, PWP PACKAGE SUFFIX

DIMENSIONS				
	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.30	4.48	.169	.176
B	7.70	7.90	.303	.311
C	–	1.10	–	.043
C1	.90 REF.		.0354 REF.	
C2	.05	.15	.002	.006
D	6.25	6.50	.246	.256
E	.65 BSC		.0256 BSC	
F	.18	.30	.007	.012
F1	.09	.18	.003	.007
L	.50	.70	.020	.028
θ	0°	8°	0°	8°

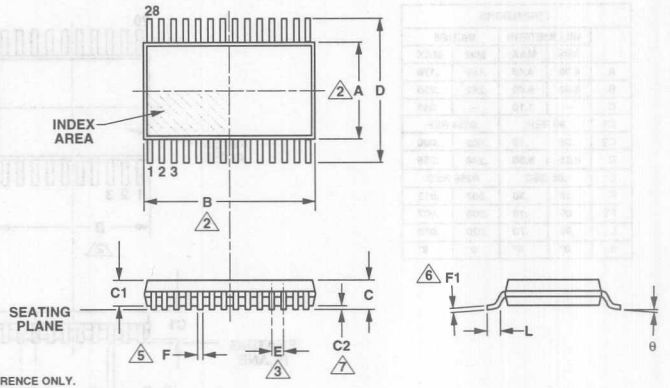


NOTES:

1. CONTROLLING DIMENSION : MILLIMETERS. INCHES SHOWN FOR REFERENCE ONLY.
2. 'A' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15mm PER SIDE.
3. THE BASIC LEAD SPACING IS 0.65 MM BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.10mm OF ITS EXACT TRUE POSITION.
4. LEADS SHALL BE COPLANAR WITHIN 0.08mm AT THE SEATING PLANE.
5. DIMENSION 'F' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'F' MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
7. 'C2' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

28-PIN TSSOP~ PWP PACKAGE SUFFIX

DIMENSIONS				
	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.30	4.48	.169	.176
B	9.60	9.80	.378	.386
C	–	1.10	–	.043
C1	.90 REF.		.0354 REF.	
C2	.05	.15	.002	.006
D	6.25	6.50	.246	.256
E	.65 BSC		.0256 BSC	
F	.18	.30	.007	.012
F1	.09	.18	.003	.007
L	.50	.70	.020	.028
θ	0°	8°	0°	8°



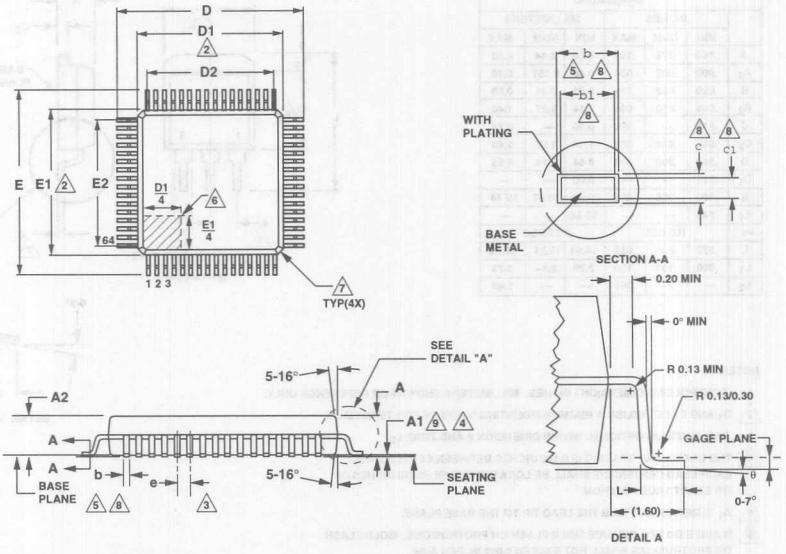
NOTES:

1. CONTROLLING DIMENSION : MILLIMETERS. INCHES SHOWN FOR REFERENCE ONLY.
2. 'A' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15mm PER SIDE.
3. THE BASIC LEAD SPACING IS 0.65 MM BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.10mm OF ITS EXACT TRUE POSITION.
4. LEADS SHALL BE COPLANAR WITHIN 0.08mm AT THE SEATING PLANE.
5. DIMENSION 'F' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'F' MAXIMUM BY MORE THAN 0.08mm DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
7. 'C2' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

Mechanical Drawings (cont'd)

64-PIN MQFP ~ FP PACKAGE SUFFIX

DIMENSIONS				
	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	–	3.40	–	0.13
A1	0.25	0.50	0.0098	0.020
A2	2.50	2.90	0.098	0.11
b	0.29	0.45	0.011	0.018
b1	0.29	0.41	0.011	0.016
C	0.11	0.23	0.0043	0.0091
C1	0.11	0.19	0.0043	0.0074
D	17.20 BSC		0.67 BSC	
D1	14.00 BSC		0.55 BSC	
D2	12.00 REF		0.47 REF	
E	17.20 BSC		0.67 BSC	
E1	14.00 BSC		0.55 BSC	
E2	12.00 REF		0.47 REF	
e	0.80 BSC		0.031 BSC	
L	0.73	1.03	0.029	0.041
L1	0.25 BSC		0.0098 BSC	
θ	0°	7°	0°	7°



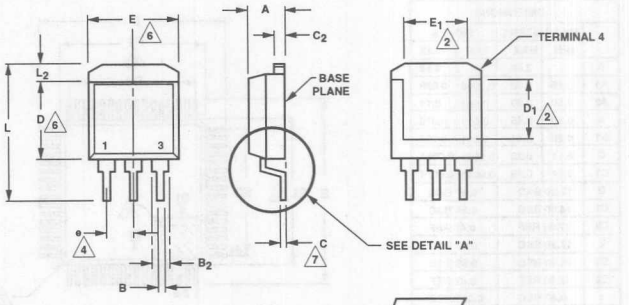
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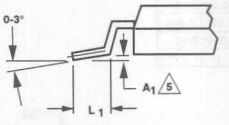
1. CONTROLLING DIMENSION: MILLIMETERS. INCHES SHOWN FOR REFERENCE ONLY.
2. 'D1' AND 'E1' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.25mm PER SIDE. 'D1' AND 'E1' INCLUDE MOLD MISMATCH.
3. THE BASIC LEAD SPACING IS 0.80mm BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.10mm OF ITS EXACT TRUE POSITION.
4. LEADS SHALL BE COPLANAR WITHIN 0.08mm AT THE SEATING PLANE.
5. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'b' MAXIMUM BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. DETAILS OF PIN1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
9. 'A1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

Mechanical Drawings (cont'd)

3-PIN PLASTIC TO-263 POWER SURFACE MOUNT ~ TD PACKAGE SUFFIX

DIMENSIONS						
	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.160	.175	.190	4.06	4.44	4.83
A_1	.000	.002	.004	0.00	0.051	0.10
B	.020	.032	.039	0.51	0.81	0.99
B_2	.045	.050	.055	1.14	1.27	1.40
C	.018	—	.029	0.46	—	0.74
C_2	.045	.050	.055	1.14	1.27	1.40
D	.340	.360	.380	8.64	9.14	9.65
D_1	.315	—	—	8.00	—	—
E	.380	.395	.405	9.65	10.03	10.44
E_1	.245	—	—	10.44	—	—
e	.100 BSC			2.54 BSC		
L	.575	.600	.625	14.61	15.24	15.88
L_1	.090	.100	.110	2.29	2.54	2.79
L_2	—	—	.055	—	—	1.40





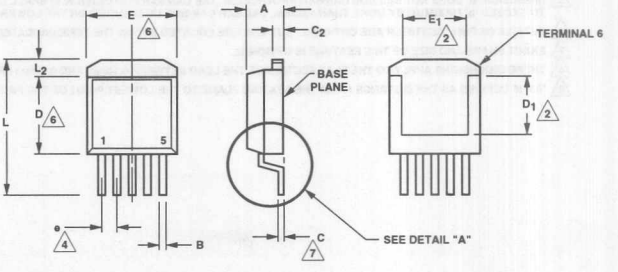
DETAIL "A" ROTATED 90°

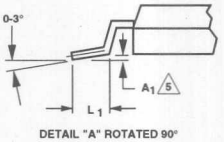
NOTES:

1. CONTROLLING DIMENSION : INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
2. D_1 AND E_1 ESTABLISH A MINIMUM MOUNTING SURFACE FOR TERMINAL 4.
3. TAB CONTOUR OPTIONAL WITHIN DIMENSION E AND ZONE L_2.
4. THE BASIC LEAD SPACING IS 0.100 INCHES BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.010 INCHES OF ITS EXACT TRUE POSITION.
5. A_1 IS MEASURED FROM THE LEAD TIP TO THE BASE PLANE.
6. D AND E DO NOT INCLUDE MOLD FLASH ON PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
7. LEAD TIPS SHALL BE COPLANAR WITHIN 0.004 INCHES.

5-PIN PLASTIC TO-263 POWER SURFACE MOUNT ~ TD PACKAGE SUFFIX

DIMENSIONS						
	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.160	.175	.190	4.06	4.44	4.83
A_1	.000	.002	.004	0.00	0.051	0.10
B	.020	.032	.039	0.51	0.81	0.99
C	.018	—	.029	0.46	—	0.74
C_2	.045	.050	.055	1.14	1.27	1.40
D	.340	.360	.380	8.64	9.14	9.65
D_1	.315	—	—	8.00	—	—
E	.380	.395	.405	9.65	10.03	10.44
E_1	.245	—	—	10.44	—	—
e	.067 BSC			1.70 BSC		
L	.575	.600	.625	14.61	15.24	15.88
L_1	.090	.100	.110	2.29	2.54	2.79
L_2	—	—	.055	—	—	1.40





DETAIL "A" ROTATED 90°

NOTES:

1. CONTROLLING DIMENSION : INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
2. D_1 AND E_1 ESTABLISH A MINIMUM MOUNTING SURFACE FOR TERMINAL 6.
3. TAB CONTOUR OPTIONAL WITHIN DIMENSION E AND ZONE L_2.
4. THE BASIC LEAD SPACING IS 0.067 INCHES BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.010 INCHES OF ITS EXACT TRUE POSITION.
5. A_1 IS MEASURED FROM THE LEAD TIP TO THE BASE PLANE.
6. D AND E DO NOT INCLUDE MOLD FLASH ON PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
7. LEAD TIPS SHALL BE COPLANAR WITHIN 0.004 INCHES.